

The S-1410/1411 Series is a watchdog timer developed using CMOS technology, which can operate with low current consumption of 3.8 μ A typ. The reset function and the low voltage detection function are available.

■ Features

- Detection voltage: 2.0 V to 5.0 V, selectable in 0.1 V step
- Detection voltage accuracy: $\pm 1.5\%$
- Input voltage: $V_{DD} = 0.9$ V to 6.0 V
- Hysteresis width: 5% typ.
- Current consumption: 3.8 μ A typ.
- Reset time-out period: 14.5 ms typ. ($C_{POR} = 2200$ pF)
- Watchdog operation is switchable: Enable, Disable
- Watchdog operation voltage range: $V_{DD} = 2.5$ V to 6.0 V
- Watchdog mode switching function*1: Time-out mode, window mode
- Watchdog input edge is selectable: Rising edge, falling edge, both rising and falling edges
- Product type is selectable: S-1410 Series
(Product with \overline{W} / T pin (Output: \overline{WDO} pin))
S-1411 Series
(Product without \overline{W} / T pin (Output: \overline{RST} pin, \overline{WDO} pin))
- Operation temperature range: $T_a = -40^\circ\text{C}$ to $+105^\circ\text{C}$
- Lead-free (Sn 100%), halogen-free

*1. The S-1411 Series is fixed to the window mode.

■ Application

- Power supply monitoring and system monitoring in microcontroller mounted apparatus

■ Packages

- TMSOP-8
- HSNT-8(2030)

■ Block Diagrams

1. S-1410 Series A / B / C Type

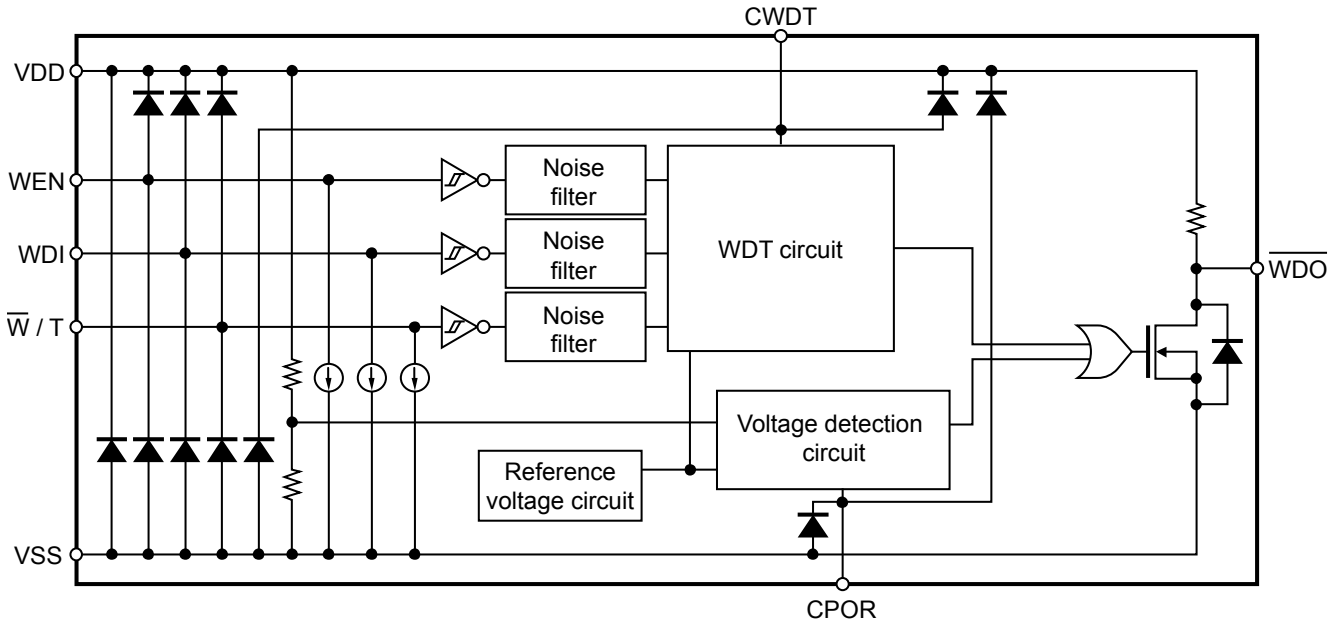


Figure 1

2. S-1410 Series D / E / F Type

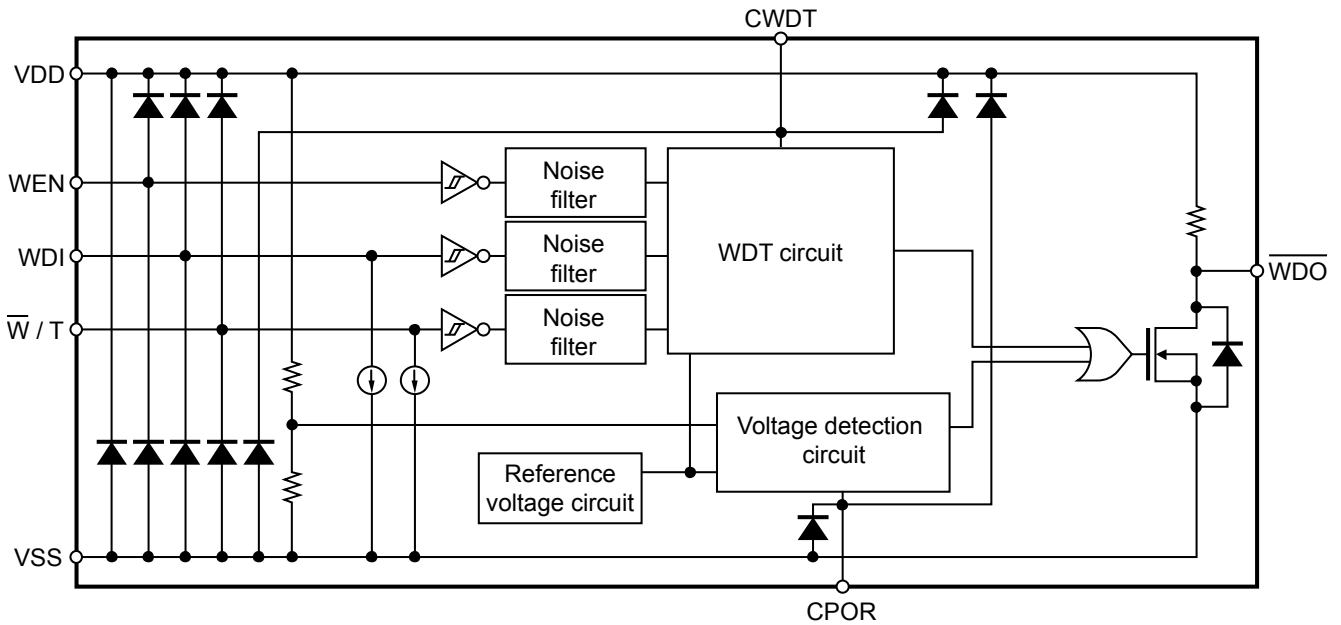


Figure 2

3. S-1410 Series G / H / I Type

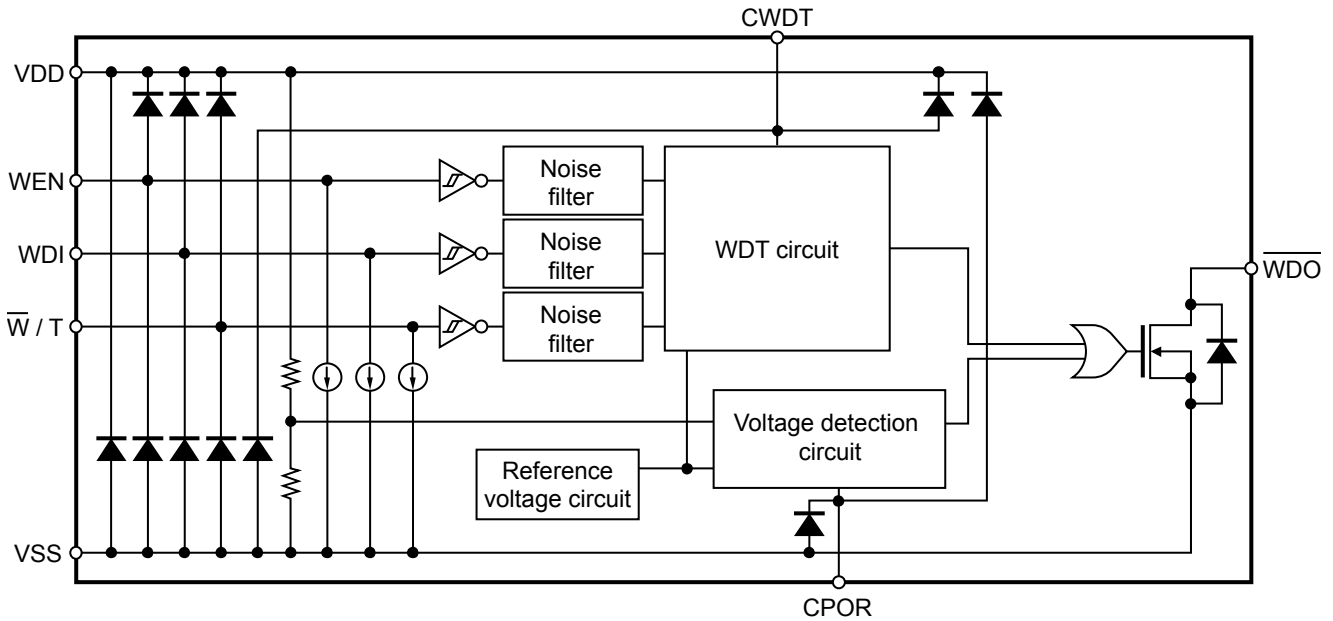


Figure 3

4. S-1410 Series J / K / L Type

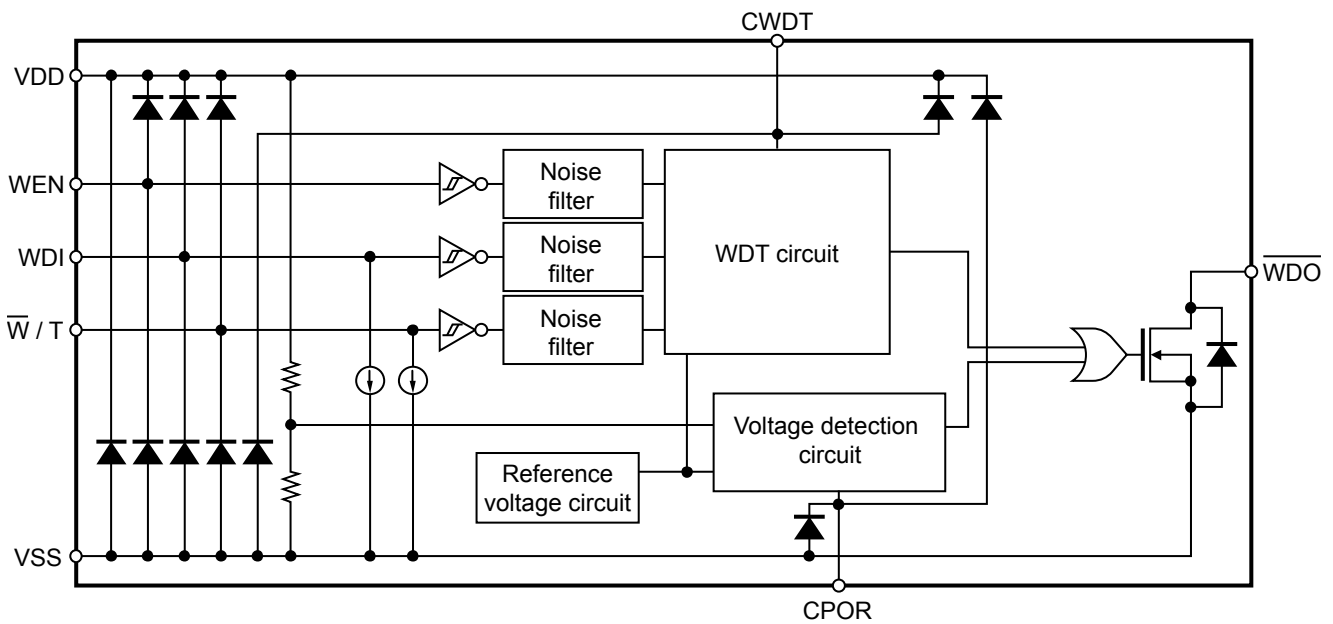


Figure 4

5. S-1411 Series A / B / C Type

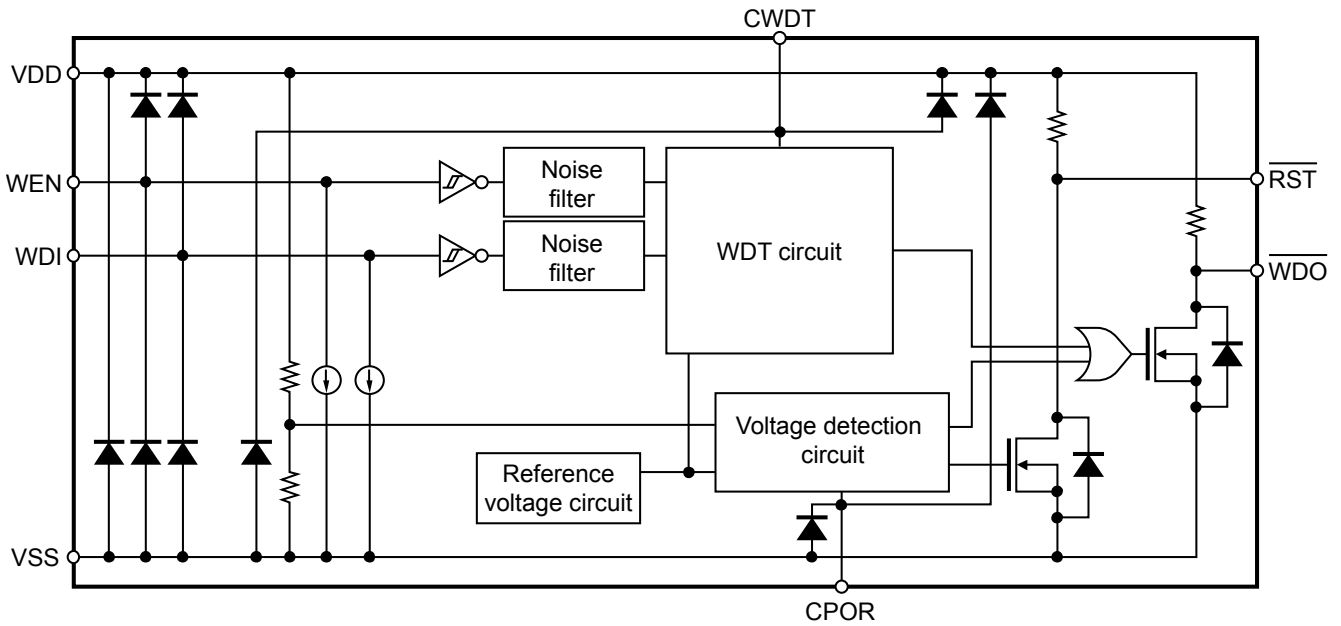


Figure 5

6. S-1411 Series D / E / F Type

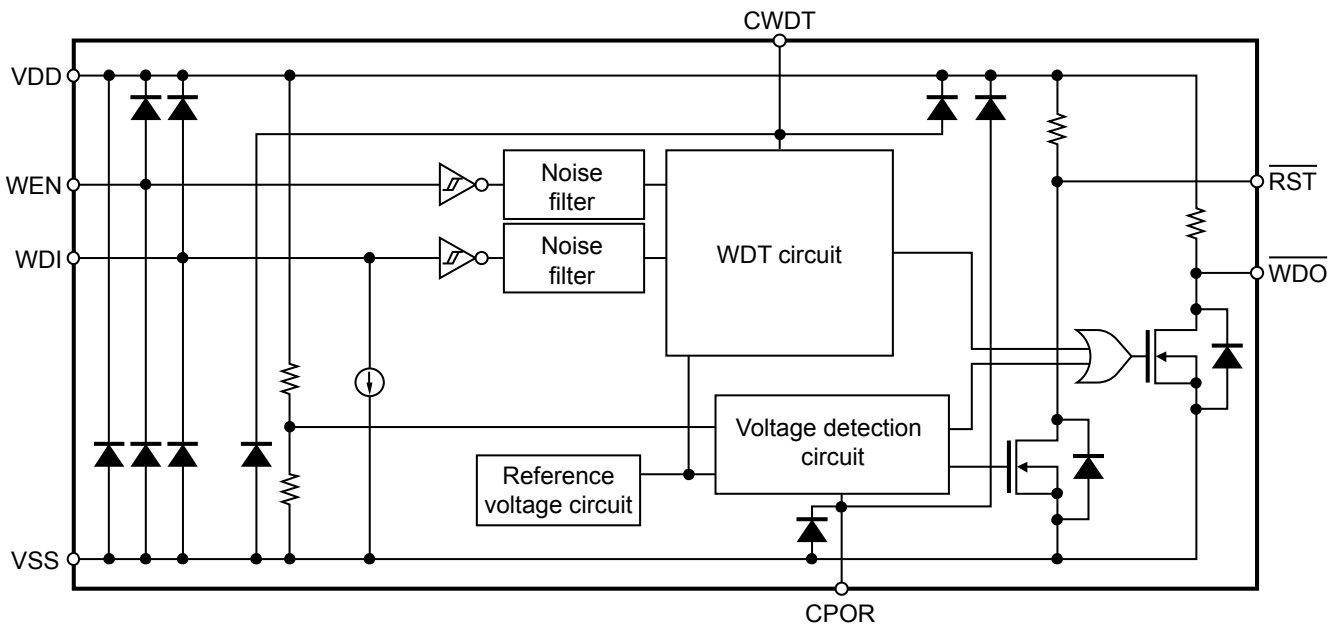


Figure 6

7. S-1411 Series G / H / I Type

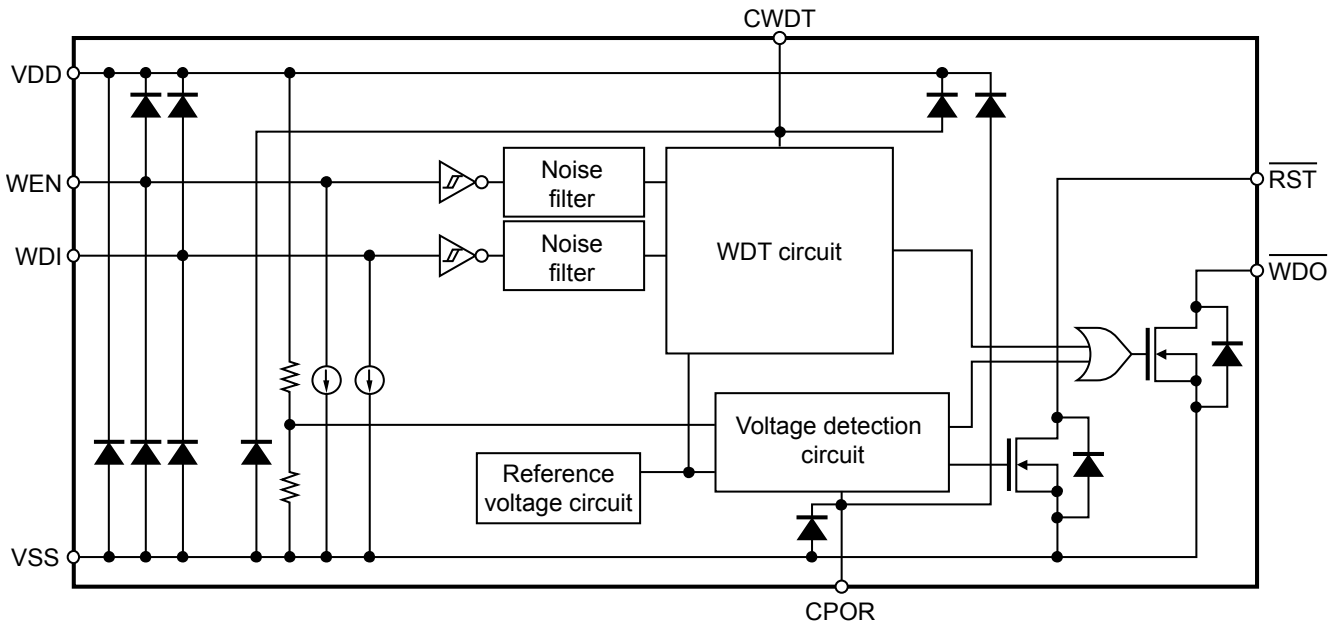


Figure 7

8. S-1411 Series J / K / L Type

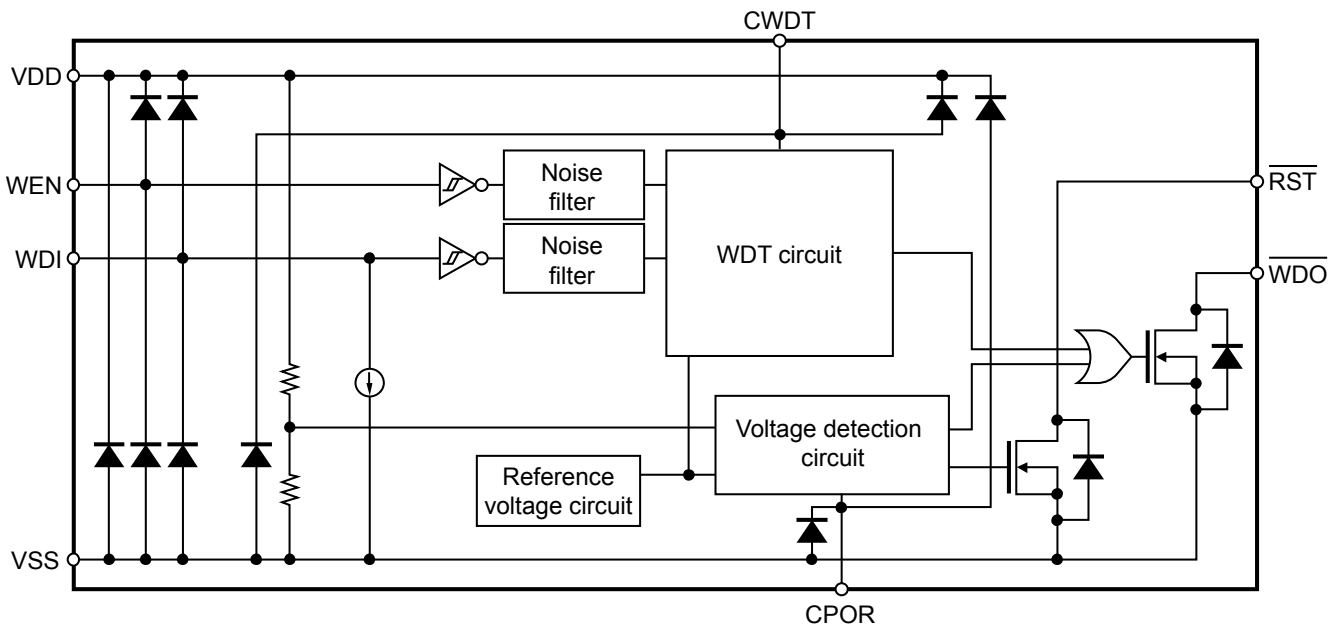
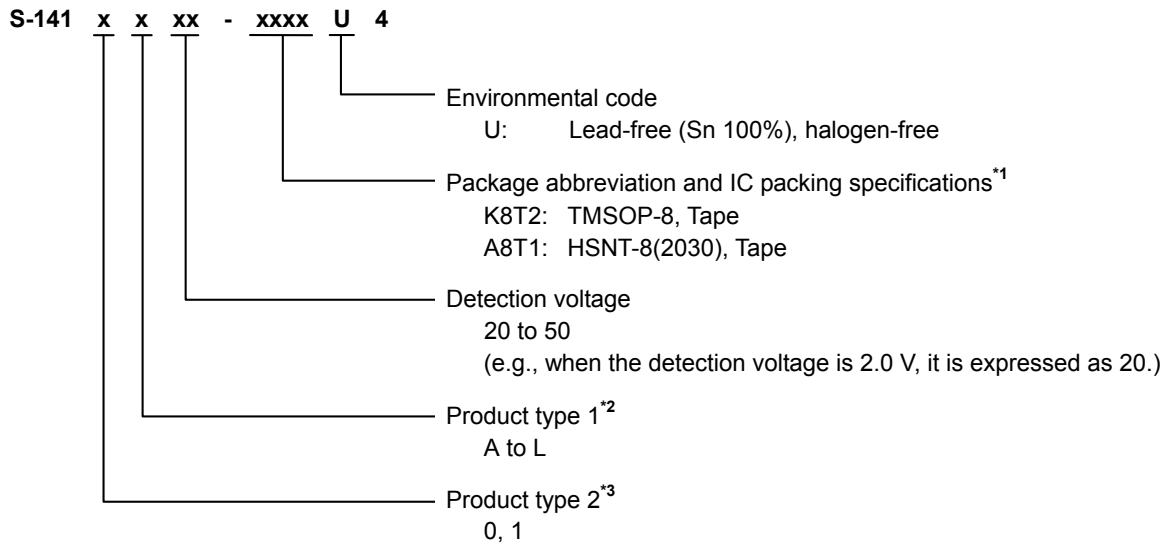


Figure 8

■ Product Name Structure

Users can select the product type, detection voltage, and package type for the S-1410/1411 Series. Refer to "1. Product name" regarding the contents of product name, "2. Product type list" regarding the product types, "3. Packages" regarding the package drawings.

1. Product name



*1. Refer to the tape drawing.

*2. Refer to "2. Product type list".

*3. 0: S-1410 Series (Product with \overline{W} / T pin)

The \overline{WDO} pin outputs the signals which are from the watchdog timer circuit and the voltage detection circuit.

1: S-1411 Series (Product without \overline{W} / T pin)

The \overline{WDO} pin outputs the signals which are from the watchdog timer circuit and the voltage detection circuit.

The \overline{RST} pin outputs the signal which is from the voltage detection circuit.

The watchdog mode is fixed to the window mode.

2. Product type list

Table 1

Product Type	WEN Pin Logic	Constant Current Source Pull-down for WEN Pin	Input Edge	Output Pull-up Resistor
A	Active "H"	Available	Rising edge	Available
B	Active "H"	Available	Falling edge	Available
C	Active "H"	Available	Both rising and falling edges	Available
D	Active "L"	Unavailable	Rising edge	Available
E	Active "L"	Unavailable	Falling edge	Available
F	Active "L"	Unavailable	Both rising and falling edges	Available
G	Active "H"	Available	Rising edge	Unavailable
H	Active "H"	Available	Falling edge	Unavailable
I	Active "H"	Available	Both rising and falling edges	Unavailable
J	Active "L"	Unavailable	Rising edge	Unavailable
K	Active "L"	Unavailable	Falling edge	Unavailable
L	Active "L"	Unavailable	Both rising and falling edges	Unavailable

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	–
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD

■ Pin Configurations

1. TMSOP-8

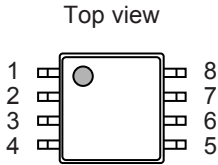


Figure 9

Table 3 S-1410 Series

Pin No.	Symbol	Description
1	\overline{W} / T^{*1}	Watchdog mode switching pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	WDO	Watchdog output and reset output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

Table 4 S-1411 Series

Pin No.	Symbol	Description
1	RST	Reset output pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	\overline{WDO}	Watchdog output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

*1. \overline{W} / T pin = "H": Time-out mode
 \overline{W} / T pin = "L": Window mode

2. HSNT-8(2030)

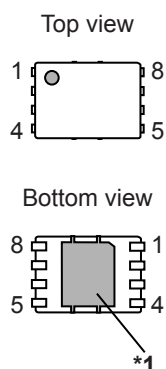


Figure 10

Table 5 S-1410 Series

Pin No.	Symbol	Description
1	\overline{W} / T^2	Watchdog mode switching pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	\overline{WDO}	Watchdog output and reset output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

Table 6 S-1411 Series

Pin No.	Symbol	Description
1	\overline{RST}	Reset output pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	\overline{WDO}	Watchdog output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

- *1. Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
 However, do not use it as the function of electrode.
- *2. \overline{W} / T pin = "H": Time-out mode
 \overline{W} / T pin = "L": Window mode

■ Pin Functions

Refer to "■ Operations" for details.

1. \overline{W} / T pin (S-1410 Series only)

This is a pin to switch the watchdog mode.

The S-1410 Series changes to the time-out mode when the \overline{W} / T pin is "H", and changes to the window mode when the \overline{W} / T pin is "L". Switching the mode is prohibited during the operation.

The \overline{W} / T pin is connected to a constant current source (0.3 μA typ.) and is pulled down internally.

1.1 Time-out mode (\overline{W} / T pin = "H")

The S-1410 Series detects an abnormality when not inputting an edge to the WDI pin during the watchdog time-out period (t_{WDU}). And then "L" is output from the \overline{WDO} pin.

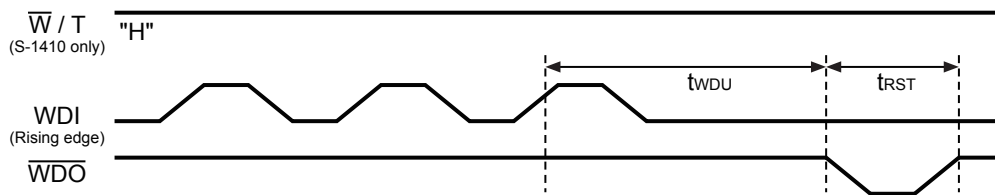


Figure 11 Abnormality Detection in Time-out Mode

1.2 Window mode (\overline{W} / T pin = "L")

When not inputting an edge to the WDI pin during t_{WDU} , or when an edge is input to the WDI pin again within a specific period of time (the discharge time due to an edge detection + 1 charge-discharge time (t_{WDL})) after inputting an edge to the WDI pin, the \overline{WDO} pin output changes from "H" to "L".

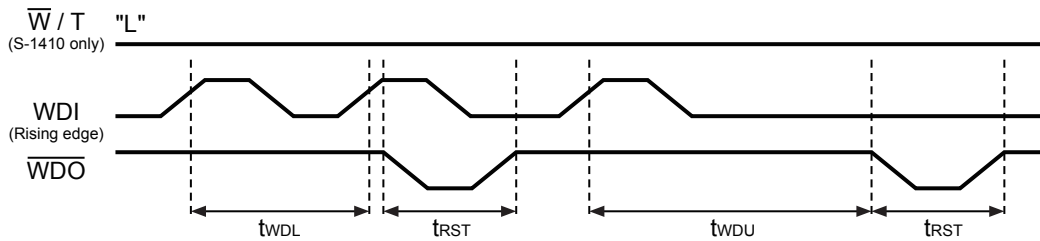


Figure 12 Abnormality Detection in Window Mode

2. $\overline{\text{RST}}$ pin (S-1411 Series only)

This is a reset output pin. It outputs "L" when detecting a low voltage.

Be sure to connect an external pull-up resistor (R_{extR}) to the $\overline{\text{RST}}$ pin in the product without an output pull-up resistor.

3. $\overline{\text{WDO}}$ pin

3.1 S-1410 Series

This pin combines the reset output and the watchdog output (time-out detection, double pulse detection).

Be sure to connect an external pull-up resistor (R_{extW}) to the $\overline{\text{WDO}}$ pin in the product without an output pull-up resistor. **Table 7** shows the $\overline{\text{WDO}}$ pin output status.

Table 7

Operation Status	$\overline{\text{WDO}}$ Pin	
	$\overline{\text{W}} / \text{T Pin} = \text{"H"}$	$\overline{\text{W}} / \text{T Pin} = \text{"L"}$
Normal operation	"H"	"H"
Low voltage detection	"L"	"L"
Time-out detection	"L"	"L"
Double pulse detection	"H"	"L"
When watchdog timer is Disable	"H"	"H"

3.2 S-1411 Series

This is the watchdog output (time-out detection, double pulse detection) pin.

Be sure to connect an external pull-up resistor (R_{extW}) to the $\overline{\text{WDO}}$ pin in the product without an output pull-up resistor. **Table 8** shows the $\overline{\text{WDO}}$ pin and $\overline{\text{RST}}$ pin output statuses.

Table 8

Operation Status	$\overline{\text{WDO}}$ Pin	$\overline{\text{RST}}$ Pin
Normal operation	"H"	"H"
Low voltage detection	"L"	"L"
Time-out detection	"L"	"H"
Double pulse detection	"L"	"H"
When watchdog timer is Disable	"H"	"H"

4. CPOR pin

This is a pin to connect an adjustment capacitor for reset output delay time (C_{POR}) in order to generate the reset time-out period (t_{RST}). C_{POR} is charged and discharged by an internal constant current circuit, and the charge-discharge duration is t_{RST} .

t_{RST} is calculated by using the following equation. Take into consideration C_{POR} variation.

$$t_{\text{RST}} = 6,500,000 \times C_{\text{POR}} [\text{F}] + 0.0002$$

5. CWDT pin

This is a pin to connect an adjustment capacitor for watchdog output delay time (C_{WDT}) in order to generate the watchdog time-out period (t_{WDU}) and the watchdog double pulse detection time (t_{WDL}). C_{WDT} is charged and discharged by an internal constant current circuit.

t_{WDU} is calculated by using the following equation. Take into consideration C_{WDT} variation.

$$t_{\text{WDU}} = 50,000,000 \times C_{\text{WDT}} [\text{F}] + 0.0011$$

Moreover, t_{WDL} is calculated by using the following equation.

$$t_{\text{WDL}} = \frac{t_{\text{WDU}}}{32}$$

6. WEN pin

This is a pin to switch Enable / Disable of the watchdog timer.

The voltage detection circuit independently operates at all times regardless of the watchdog timer operation.

6.1 S-1410/1411 Series A / B / C / G / H / I type (WEN pin logic active "H" product)

The watchdog timer becomes Enable if the input is "H", and the charge-discharge operation is performed at the CWDT pin.

The WEN pin is connected to a constant current source (0.3 μ A typ.) and is pulled down internally.

6.2 S-1410/1411 Series D / E / F / J / K / L type (WEN pin logic active "L" product)

The watchdog timer becomes Enable if the input is "L", and the charge-discharge operation is performed at the CWDT pin.

The WEN pin is not pulled down internally.

7. WDI pin

This is an input pin to receive a signal from the monitored object. By inputting an edge at an appropriate timing, the WDI pin confirms the normal operation of the monitored object.

The WDI pin is connected to a constant current source (0.3 μ A typ.) and is pulled down internally.

Absolute Maximum Ratings

Table 9

(Ta = +25°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit	
VDD pin voltage	V _{DD}	V _{SS} - 0.3 to V _{SS} + 7.0	V	
WDI pin voltage	V _{WDI}	V _{SS} - 0.3 to V _{DD} + 0.3 ≤ V _{SS} + 7.0	V	
WEN pin voltage	V _{WEN}	V _{SS} - 0.3 to V _{DD} + 0.3 ≤ V _{SS} + 7.0	V	
\overline{W} / T pin voltage	V _{\overline{W} / T}	V _{SS} - 0.3 to V _{DD} + 0.3 ≤ V _{SS} + 7.0	V	
CPOR pin voltage	V _{CPOR}	V _{SS} - 0.3 to V _{DD} + 0.3 ≤ V _{SS} + 7.0	V	
CWDT pin voltage	V _{CWDT}	V _{SS} - 0.3 to V _{DD} + 0.3 ≤ V _{SS} + 7.0	V	
\overline{RST} pin voltage	A / B / C / D / E / F type	V _{\overline{RST}}	V _{SS} - 0.3 to V _{DD} + 0.3 ≤ V _{SS} + 7.0	V
	G / H / I / J / K / L type		V _{SS} - 0.3 to V _{SS} + 7.0	V
\overline{WDO} pin voltage	A / B / C / D / E / F type	V _{\overline{WDO}}	V _{SS} - 0.3 to V _{DD} + 0.3 ≤ V _{SS} + 7.0	V
	G / H / I / J / K / L type		V _{SS} - 0.3 to V _{SS} + 7.0	V
Operation ambient temperature	T _{opr}	-40 to +105	°C	
Storage temperature	T _{stg}	-40 to +150	°C	

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

Thermal Resistance Value

Table 10

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	-	160	-	°C/W
			Board B	-	133	-	°C/W
			Board C	-	-	-	°C/W
			Board D	-	-	-	°C/W
			Board E	-	-	-	°C/W
		HSNT-8(2030)	Board A	-	181	-	°C/W
			Board B	-	135	-	°C/W
			Board C	-	40	-	°C/W
			Board D	-	42	-	°C/W
			Board E	-	32	-	°C/W

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "Power Dissipation" and "Test Board" for details.

Recommended Operation Conditions

Table 11

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VDD pin voltage	V _{DD}	Detector block	0.9	-	6.0	V
		Watchdog timer block	2.5	-	6.0	V
Set detection voltage	-V _{DET(S)}	0.1 V step	2.0	-	5.0	V
External pull-up resistor for \overline{RST} pin	R _{extR}	S-1411 Series G / H / I / J / K / L type	10	100	-	kΩ
External pull-up resistor for \overline{WDO} pin	R _{extW}	S-1410/1411 Series G / H / I / J / K / L type	10	100	-	kΩ
Adjustment capacitor for reset output delay time	C _{POR}	-	0.1	2.2	1000	nF
Adjustment capacitor for watchdog output delay time	C _{WDT}	-	0.1	0.47	1000	nF

■ Electrical Characteristics

1. S-1410 Series

Table 12 (1 / 2)

(WEN pin logic active "H" product, V_{DD} = 5.0 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Detection voltage*1	-V _{DET}	-	-V _{DET(S)} × 0.985	-V _{DET(S)}	-V _{DET(S)} × 1.015	V	1	
Hysteresis width	V _{HYS}	-	-V _{DET} × 0.03	-V _{DET} × 0.05	-V _{DET} × 0.07	V	1	
Current consumption during operation	I _{SS1}	When watchdog timer operates	-	3.8	7.8	μA	2	
Reset time-out period	t _{RST}	C _{POR} = 2200 pF	8.7	14.5	20	ms	3	
Watchdog time-out period	t _{WDT}	C _{WDT} = 470 pF	15	24.6	34	ms	3	
Watchdog double pulse detection time	t _{WDL}	C _{WDT} = 470 pF	461	769	1077	μs	4	
Watchdog output voltage "H"	V _{WOH}	A / B / C / D / E / F type only	V _{DD} - 1.0	-	-	V	5	
Watchdog output voltage "L"	V _{WOL}	External pull-up resistor of 100 kΩ is connected for G / H / I / J / K / L type	-	-	0.4	V	6	
Watchdog output pull-up current	I _{WUP}	V _{WDO} = 0 V, A / B / C / D / E / F type only	-	-0.85	-0.4	μA	7	
Watchdog output current	I _{WOUT}	V _{DS} = 0.4 V	V _{DD} = 1.5 V	0.6	1.1	-	mA	8
			V _{DD} = 1.8 V	1.1	1.6	-	mA	8
			V _{DD} = 2.5 V	2.1	2.6	-	mA	8
			V _{DD} = 3.0 V	2.8	3.3	-	mA	8
Watchdog output leakage current	I _{WLEAK}	V _{DS} = 6.0 V, V _{DD} = 6.0 V	-	-	0.096	μA	9	
Input pin voltage 1 "H"	V _{SH1}	WEN pin	0.7 × V _{DD}	-	-	V	10	
Input pin voltage 1 "L"	V _{SL1}	WEN pin	-	-	0.3 × V _{DD}	V	10	
Input pin voltage 2 "H"	V _{SH2}	\bar{W} / T pin	0.7 × V _{DD}	-	-	V	10	
Input pin voltage 2 "L"	V _{SL2}	\bar{W} / T pin	-	-	0.3 × V _{DD}	V	10	
Input pin voltage 3 "H"	V _{SH3}	WDI pin	0.7 × V _{DD}	-	-	V	10	
Input pin voltage 3 "L"	V _{SL3}	WDI pin	-	-	0.3 × V _{DD}	V	10	

Table 12 (2 / 2)

(WEN pin logic active "H" product, $V_{DD} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Input pin current 1 "H"	I_{SH1}	WEN pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 6.0 V	A / B / C / G / H / I type	–	0.3	1.0	μA	10
			D / E / F / J / K / L type	–0.1	–	0.1	μA	10
Input pin current 1 "L"	I_{SL1}	WEN pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 0 V	–0.1	–	0.1	μA	10	
Input pin current 2 "H"	I_{SH2}	\bar{W} / T pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 6.0 V	–	0.3	1.0	μA	10	
Input pin current 2 "L"	I_{SL2}	\bar{W} / T pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 0 V	–0.1	–	0.1	μA	10	
Input pin current 3 "H"	I_{SH3}	WDI pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 6.0 V	–	0.3	1.0	μA	10	
Input pin current 3 "L"	I_{SL3}	WDI pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 0 V	–0.1	–	0.1	μA	10	
Input pulse width "H" ^{*2}	t_{high1}	–	1.5	–	–	μs	10	
Input pulse width "L" ^{*2}	t_{low1}	–	1.5	–	–	μs	10	
Watchdog output delay time	t_{WOUT}	–	–	25	40	μs	3	
Reset output delay time	t_{ROUT}	–	–	25	40	μs	3	
Input setup time	t_{iset}	–	1.0	–	–	μs	3	

*1. $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Set detection voltage

*2. The input pulse width "H" (t_{high1}) and the input pulse width "L" (t_{low1}) are defined as shown in **Figure 13**. Inputs to the WEN pin and the WDI pin should be greater than or equal to the min. value specified in "■ Electrical Characteristics".

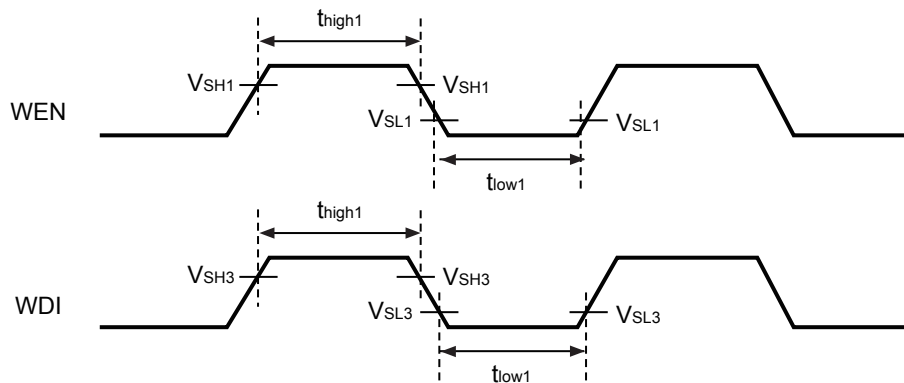


Figure 13

2. S-1411 Series

Table 13 (1 / 2)

(WEN pin logic active "H" product, $V_{DD} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Detection voltage**1	$-V_{DET}$	–	$-V_{DET(S)} \times 0.985$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.015$	V	11	
Hysteresis width	V_{HYS}	–	$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	11	
Current consumption during operation	I_{SS1}	When watchdog timer operates	–	3.8	7.8	μA	12	
Reset time-out period	t_{RST}	$C_{POR} = 2200\text{ pF}$	8.7	14.5	20	ms	13	
Watchdog time-out period	t_{WDO}	$C_{WDT} = 470\text{ pF}$	15	24.6	34	ms	13	
Watchdog double pulse detection time	t_{WDL}	$C_{WDT} = 470\text{ pF}$	461	769	1077	μs	14	
Reset output voltage "H"	V_{ROH}	A / B / C / D / E / F type only	$V_{DD} - 1.0$	–	–	V	15	
Reset output voltage "L"	V_{ROL}	External pull-up resistor of 100 kΩ is connected for G / H / I / J / K / L type	–	–	0.4	V	16	
Reset output pull-up current	I_{RUP}	$V_{RST} = 0\text{ V}$, A / B / C / D / E / F type only	–	–0.85	–0.4	μA	17	
Reset output current	I_{ROUT}	$V_{DS} = 0.4\text{ V}$	$V_{DD} = 1.5\text{ V}$	0.6	1.1	–	mA	18
			$V_{DD} = 1.8\text{ V}$	1.1	1.6	–	mA	18
			$V_{DD} = 2.5\text{ V}$	2.1	2.6	–	mA	18
			$V_{DD} = 3.0\text{ V}$	2.8	3.3	–	mA	18
Reset output leakage current	I_{RLEAK}	$V_{DS} = 6.0\text{ V}$, $V_{DD} = 6.0\text{ V}$	–	–	0.096	μA	19	
Watchdog output voltage "H"	V_{WOH}	A / B / C / D / E / F type only	$V_{DD} - 1.0$	–	–	V	20	
Watchdog output voltage "L"	V_{WOL}	External pull-up resistor of 100 kΩ is connected for G / H / I / J / K / L type	–	–	0.4	V	21	
Watchdog output pull-up current	I_{WUP}	$V_{WDO} = 0\text{ V}$, A / B / C / D / E / F type only	–	–0.85	–0.4	μA	22	
Watchdog output current	I_{WOUT}	$V_{DS} = 0.4\text{ V}$	$V_{DD} = 1.5\text{ V}$	0.6	1.1	–	mA	23
			$V_{DD} = 1.8\text{ V}$	1.1	1.6	–	mA	23
			$V_{DD} = 2.5\text{ V}$	2.1	2.6	–	mA	23
			$V_{DD} = 3.0\text{ V}$	2.8	3.3	–	mA	23
Watchdog output leakage current	I_{WLEAK}	$V_{DS} = 6.0\text{ V}$, $V_{DD} = 6.0\text{ V}$	–	–	0.096	μA	24	
Input pin voltage 1 "H"	V_{SH1}	WEN pin	$0.7 \times V_{DD}$	–	–	V	25	
Input pin voltage 1 "L"	V_{SL1}	WEN pin	–	–	$0.3 \times V_{DD}$	V	25	
Input pin voltage 3 "H"	V_{SH3}	WDI pin	$0.7 \times V_{DD}$	–	–	V	25	
Input pin voltage 3 "L"	V_{SL3}	WDI pin	–	–	$0.3 \times V_{DD}$	V	25	

Table 13 (2 / 2)

(WEN pin logic active "H" product, $V_{DD} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Input pin current 1 "H"	I_{SH1}	WEN pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 6.0 V	A / B / C / G / H / I type	–	0.3	1.0	μA	25
			D / E / F / J / K / L type	–0.1	–	0.1	μA	25
Input pin current 1 "L"	I_{SL1}	WEN pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 0 V	–0.1	–	0.1	μA	25	
Input pin current 3 "H"	I_{SH3}	WDI pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 6.0 V	–	0.3	1.0	μA	25	
Input pin current 3 "L"	I_{SL3}	WDI pin, $V_{DD} = 6.0\text{ V}$, Input pin voltage = 0 V	–0.1	–	0.1	μA	25	
Input pulse width "H"*2	t_{high1}	–	1.5	–	–	μs	25	
Input pulse width "L"*2	t_{low1}	–	1.5	–	–	μs	25	
Watchdog output delay time	t_{WOUT}	–	–	25	40	μs	13	
Reset output delay time	t_{ROUT}	–	–	25	40	μs	13	
Input setup time	t_{set}	–	1.0	–	–	μs	13	

*1. $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Set detection voltage

*2. The input pulse width "H" (t_{high1}) and the input pulse width "L" (t_{low1}) are defined as shown in **Figure 14**. Inputs to the WEN pin and the WDI pin should be greater than or equal to the min. value specified in "■ **Electrical Characteristics**".

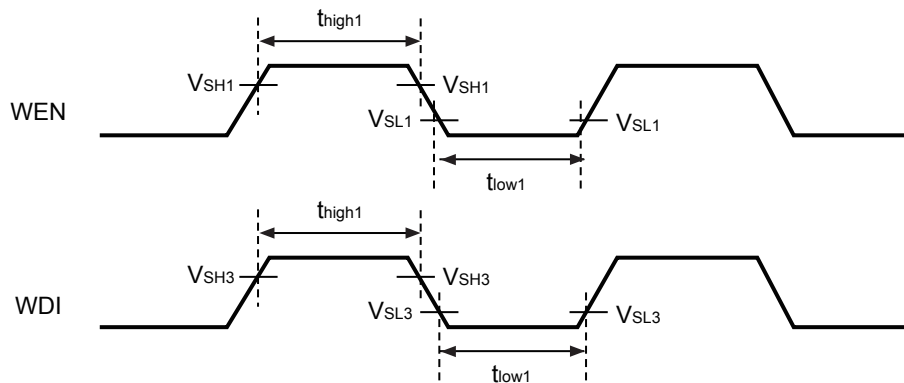


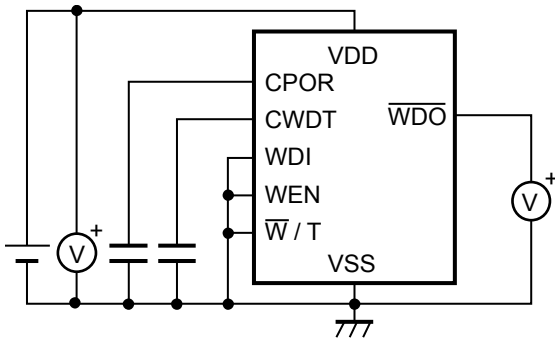
Figure 14

■ Test Circuits

Refer to "■ Recommended Operation Conditions" when setting constants of external pull-up resistors (R_{extR} , R_{extW}) and external capacitors (C_{POR} , C_{WDT}).

1. S-1410 Series

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

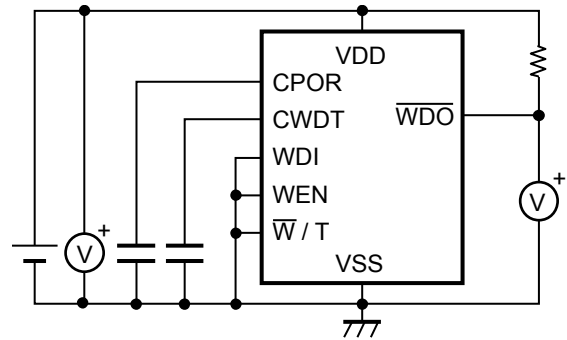


Figure 15 Test Circuit 1

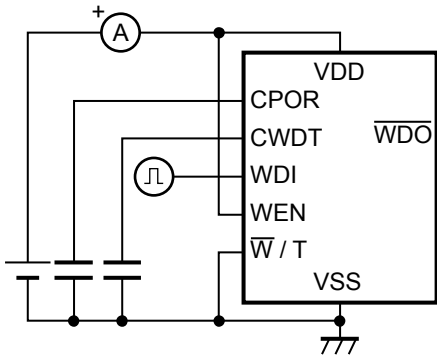
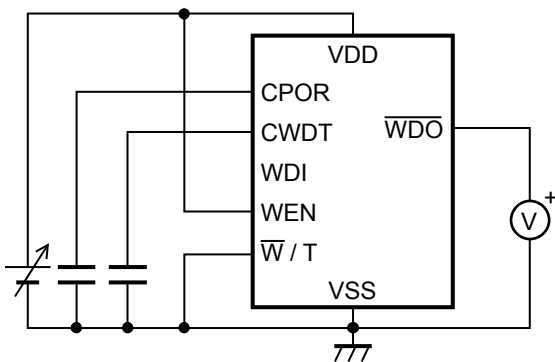


Figure 16 Test Circuit 2

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

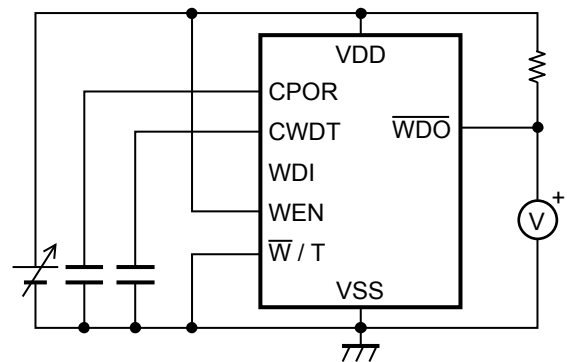
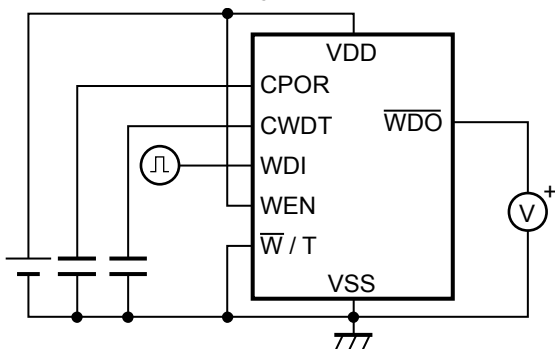


Figure 17 Test Circuit 3

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

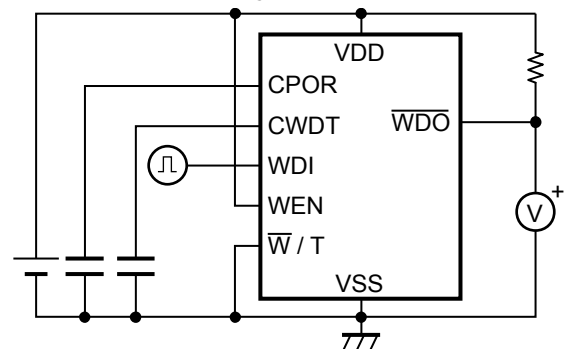


Figure 18 Test Circuit 4

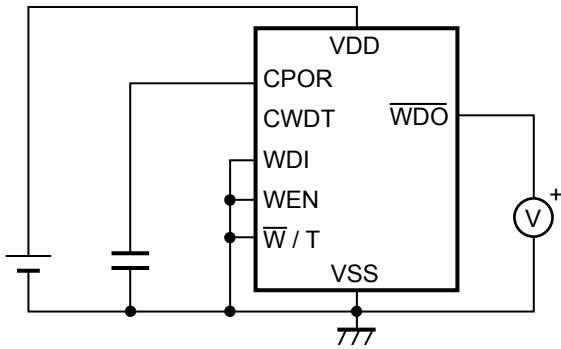
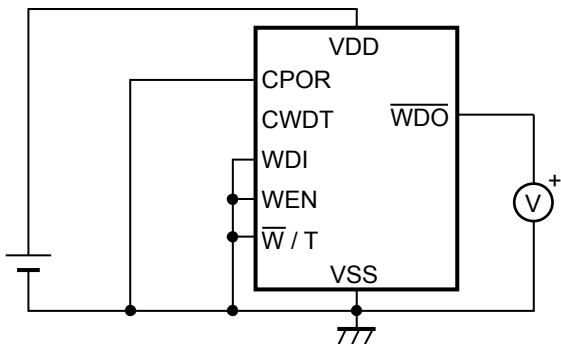


Figure 19 Test Circuit 5

(1) A/B/C/D/E/F type



(2) G/H/I/J/K/L type

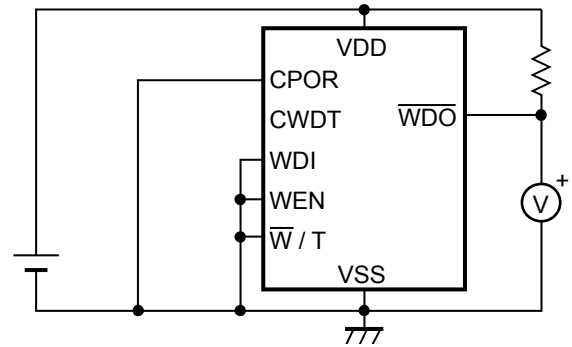


Figure 20 Test Circuit 6

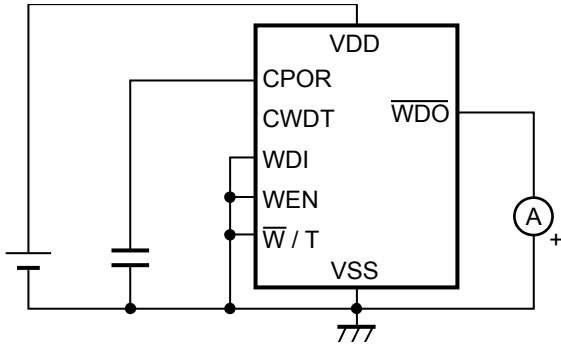


Figure 21 Test Circuit 7

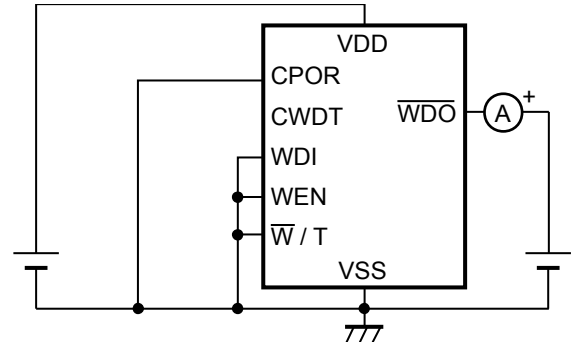


Figure 22 Test Circuit 8

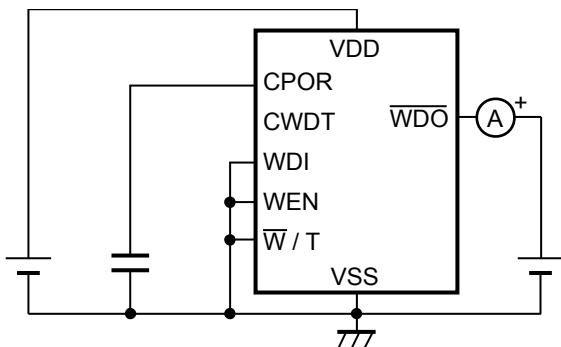


Figure 23 Test Circuit 9

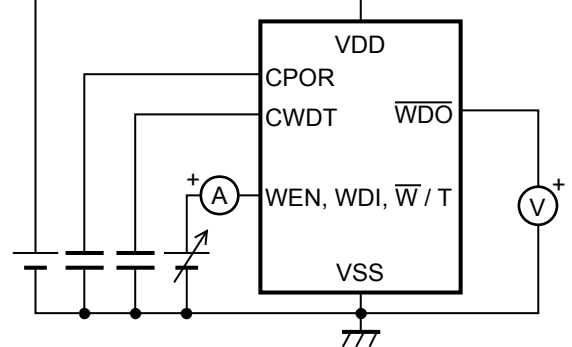
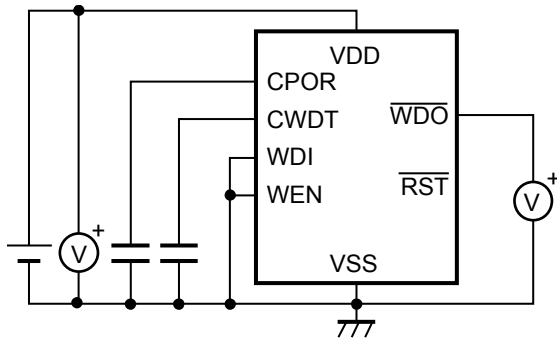


Figure 24 Test Circuit 10

2. S-1411 Series

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

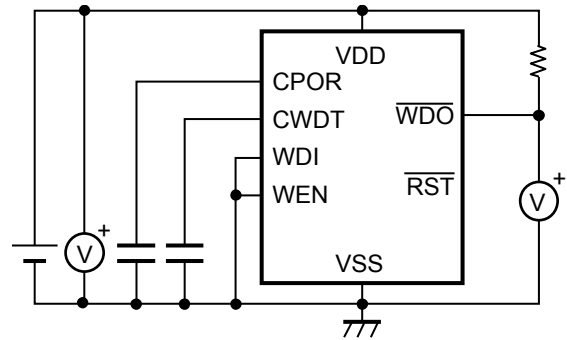


Figure 25 Test Circuit 11

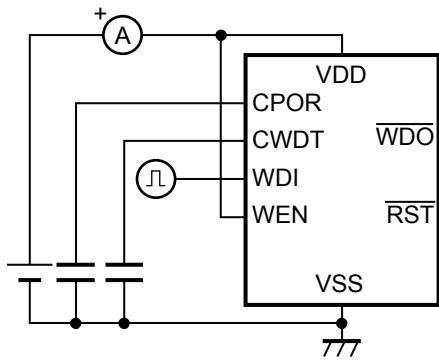
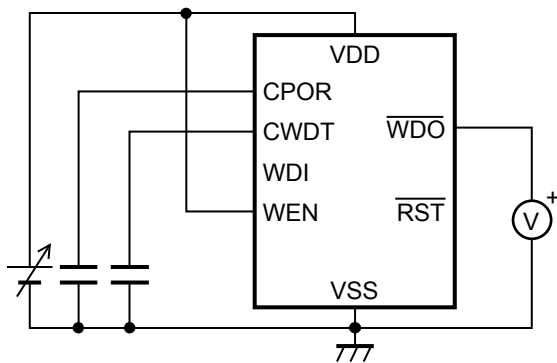


Figure 26 Test Circuit 12

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

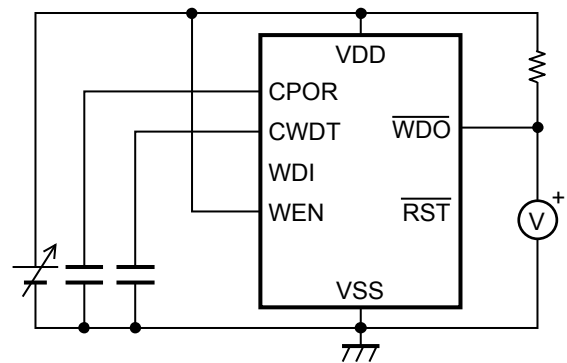
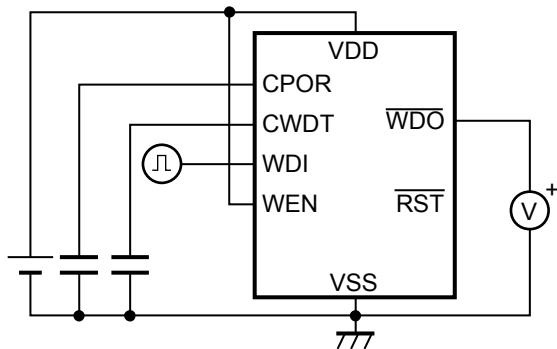


Figure 27 Test Circuit 13

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

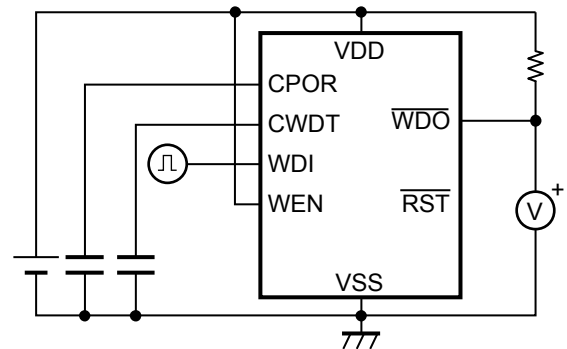


Figure 28 Test Circuit 14

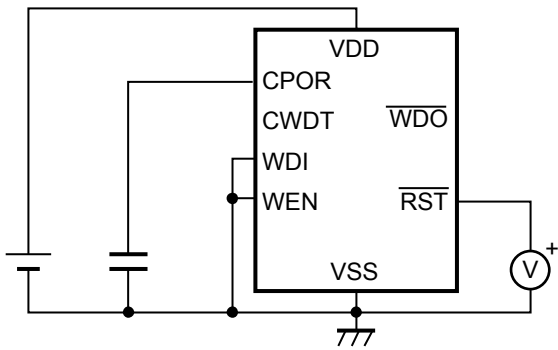
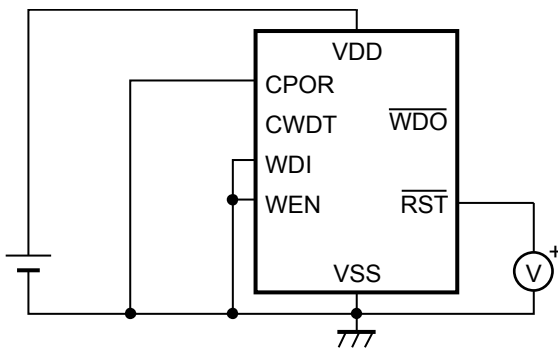


Figure 29 Test Circuit 15

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

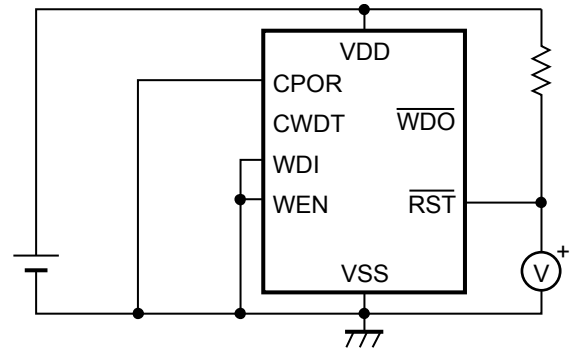


Figure 30 Test Circuit 16

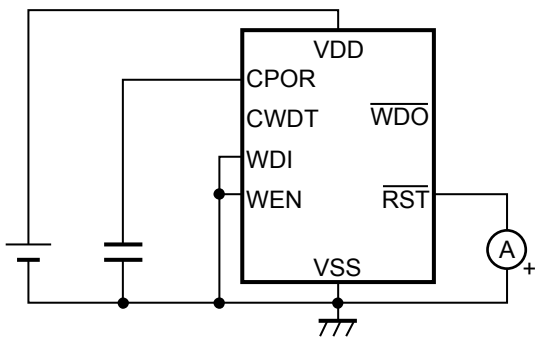


Figure 31 Test Circuit 17

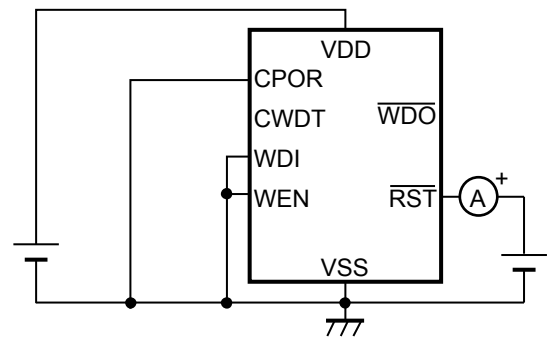


Figure 32 Test Circuit 18

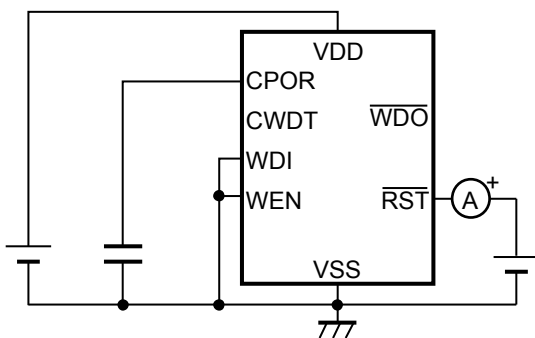


Figure 33 Test Circuit 19

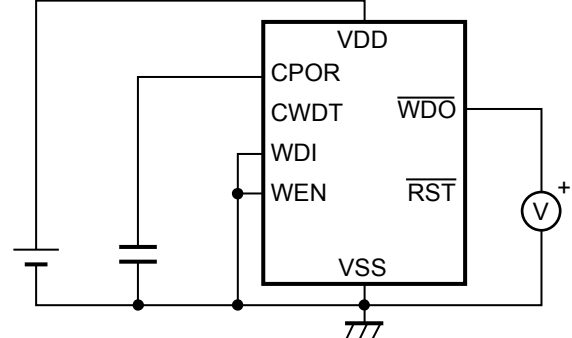
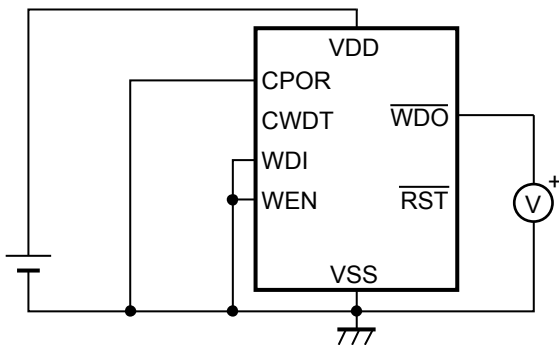


Figure 34 Test Circuit 20

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

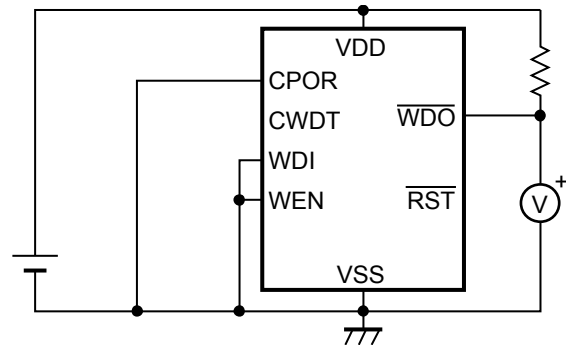


Figure 35 Test Circuit 21

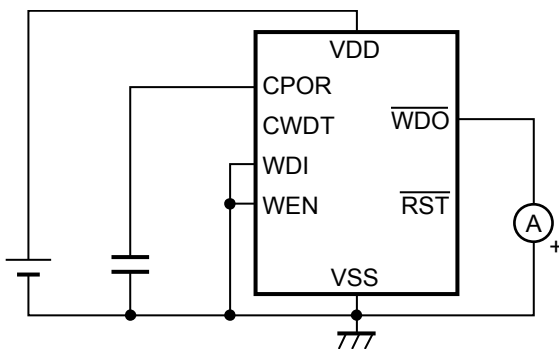


Figure 36 Test Circuit 22

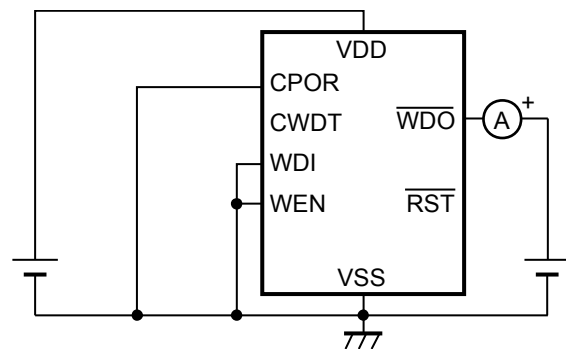


Figure 37 Test Circuit 23

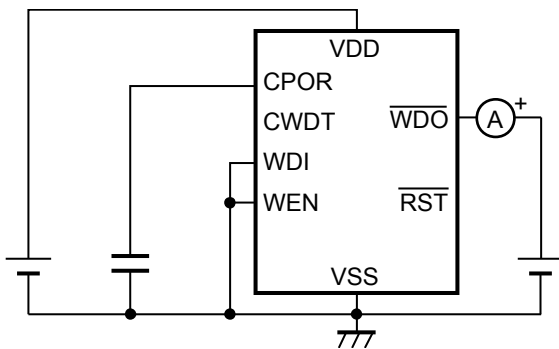


Figure 38 Test Circuit 24

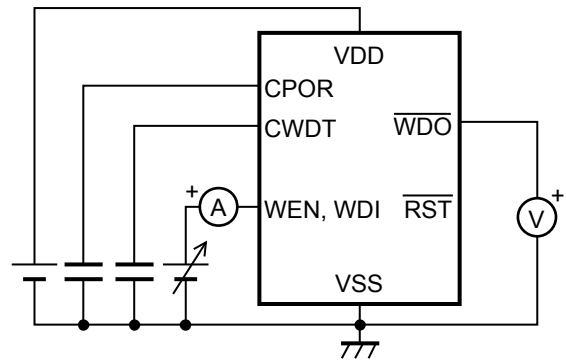
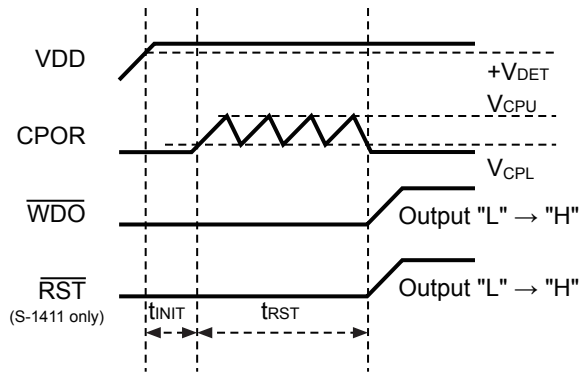


Figure 39 Test Circuit 25

■ Operations

1. From power-on to reset release

The S-1410/1411 Series initiates the initialization if the VDD pin voltage exceeds the release voltage (+V_{DET}). The charge-discharge operation to the CPOR pin is initiated after the passage of the initialization time (t_{INIT}), and the $\overline{\text{WDO}}$ pin output and the $\overline{\text{RST}}$ pin output change from "L" to "H" after the operation is performed 4 times.



Remark V_{CPU}: CPOR charge upper limit threshold (1.25 V typ.)
 V_{CPL}: CPOR charge lower limit threshold (0.20 V typ.)

Figure 40

t_{INIT} changes according to the power supply rising time. Refer to Figure 41 for the relation between t_{INIT} and the power supply rising time.

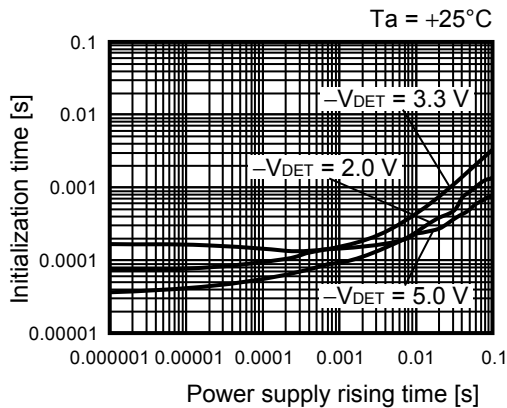
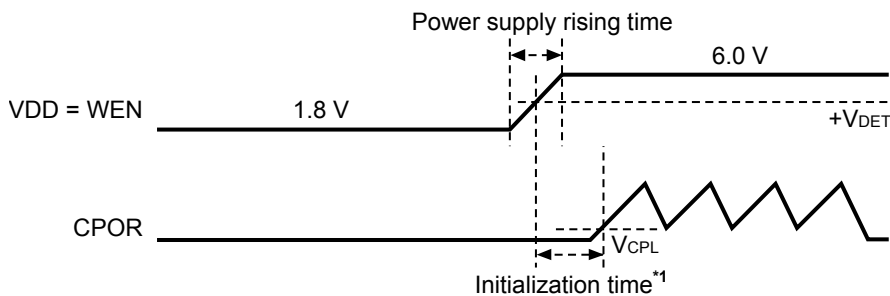


Figure 41 Power Supply Rising Time Dependency of Initialization Time



*1. The initialization time is the time period from when the VDD pin voltage reaches +V_{DET} to when C_{POR} rises.

Figure 42 Initialization Time

2. From reset release to initiation of charge-discharge operation to CWDT pin

The charge-discharge operation to the CWDT pin differs depending on the status of the WEN pin at the reset release.

2.1 When WEN pin is "H" at reset release (Active "H")

Since the watchdog timer is Enable, the S-1410/1411 Series initiates the charge-discharge operation to the CWDT pin.

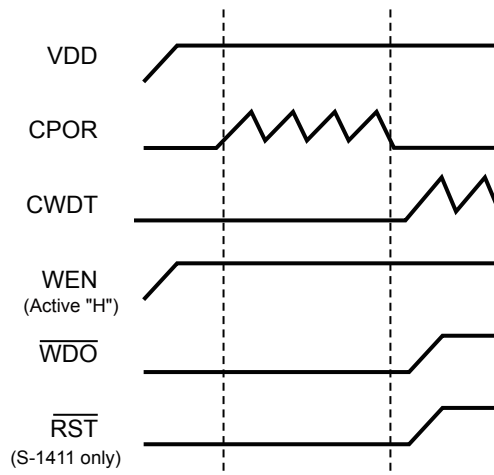


Figure 43 WEN Pin = "H"

2.2 When WEN pin is "L" at reset release (Active "H")

Since the watchdog timer is Disable after the CPOR pin performs the charge-discharge operation 4 times, the S-1410/1411 Series does not initiate the charge-discharge operation to the CWDT pin. If the input to the WEN pin changes to "H" in this status, the S-1410/1411 Series initiates the charge-discharge operation to the CWDT pin.

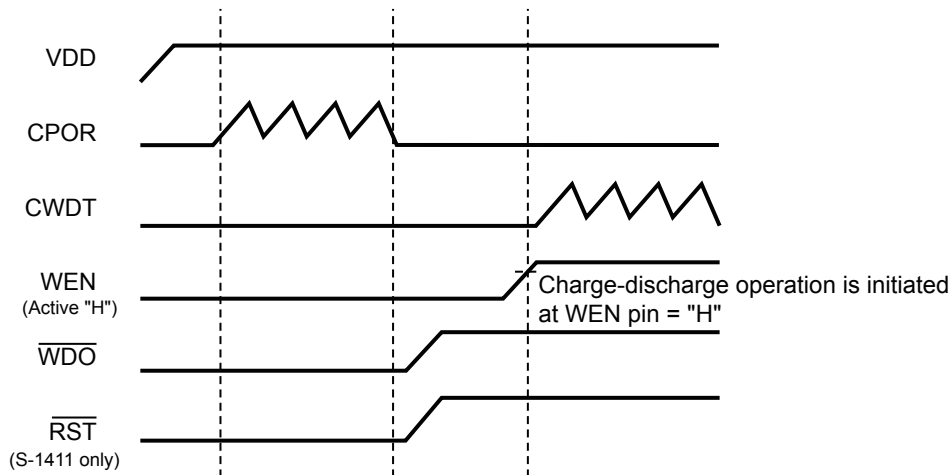


Figure 44 WEN Pin = "L" → "H"

3. Watchdog time-out detection

The watchdog timer detects a time-out after the charge-discharge operation to the CWDT pin is performed 32 times, then the \overline{WDO} pin output changes from "H" to "L".

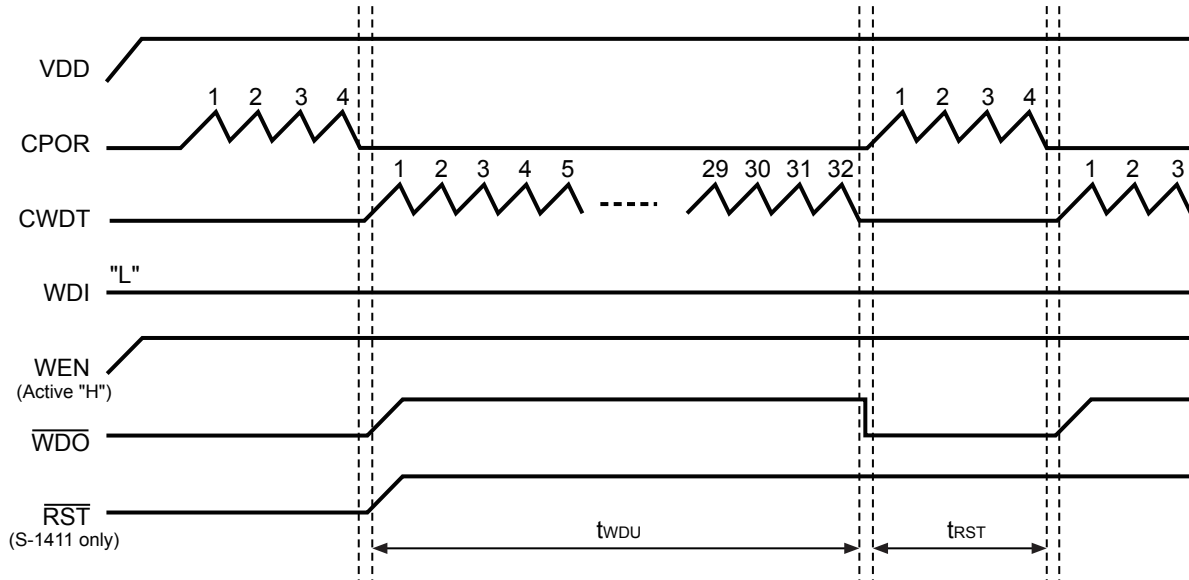


Figure 45

4. Internal counter reset due to edge detection

When the WDI pin detects an edge during the charge-discharge operation to the CWDT pin, the internal counter which counts the number of times of the charge-discharge operation is reset. The CWDT pin initiates the discharge operation when an edge is detected, and initiates the charge-discharge operation again after the discharge operation is completed.

4.1 Counter reset due to rising edge detection (S-141xAxx, S-141xDxx, S-141xGxx, S-141xJxx)

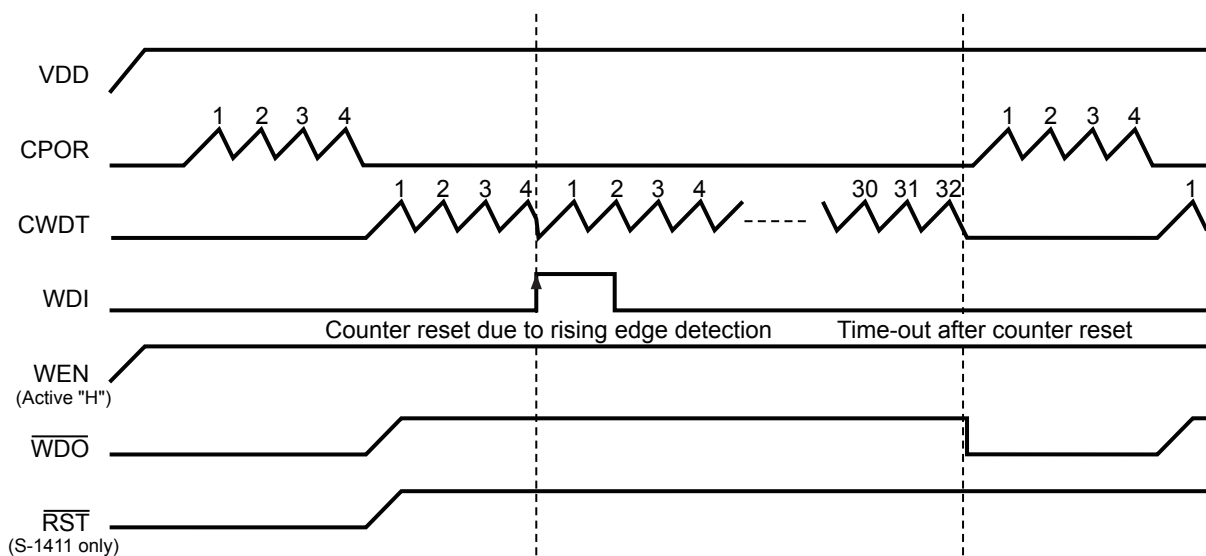


Figure 46

4.2 Counter reset due to falling edge detection
 (S-141xBxx, S-141xExx, S-141xHxx, S-141xKxx)

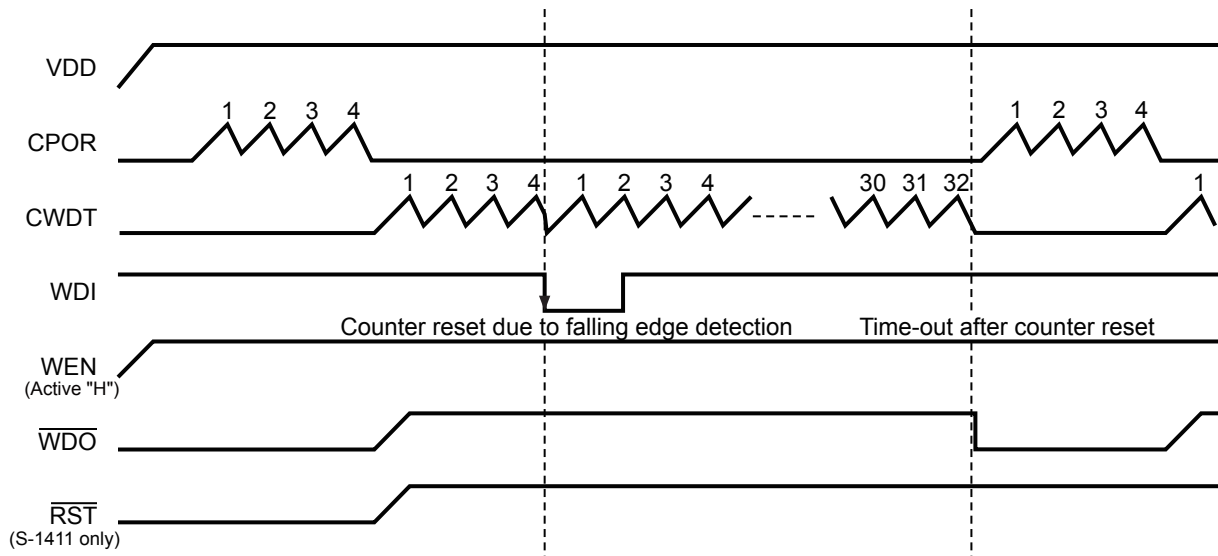


Figure 47

4.3 Counter reset due to both rising and falling edges detection 1
 (S-141xCxx, S-141xFxx, S-141xIxx, S-141xLxx)

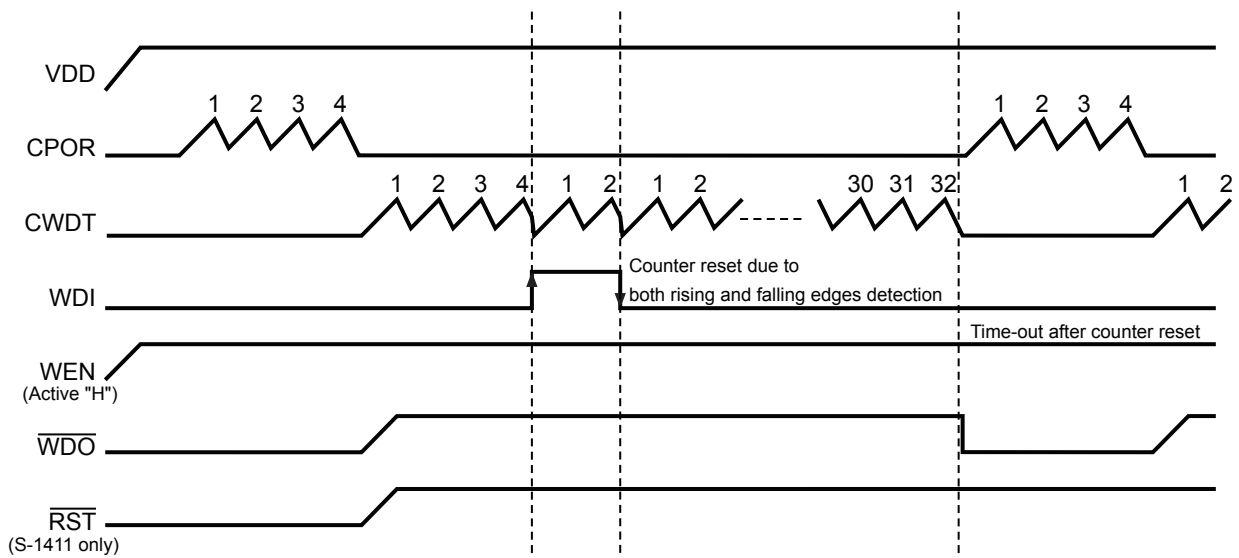


Figure 48

4. 4 Counter reset due to both rising and falling edges detection 2
 (S-141xCxx, S-141xFxx, S-141xLxx, S-141xLxx)

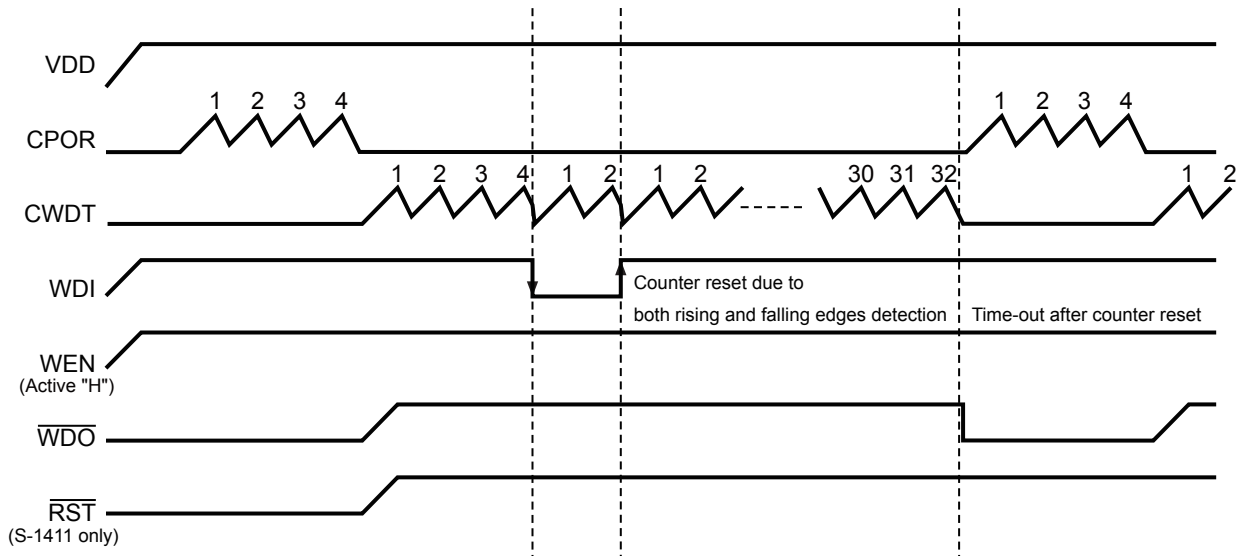


Figure 49

5. WEN pin operation during charge-discharge operation to CWDT pin

When the WEN pin changes from "H" to "L" during the charge-discharge operation to the CWDT pin, the CWDT pin performs the discharge operation. Moreover, the internal counter which counts the number of times of the charge-discharge operation for the CWDT pin is also reset. If the WEN pin changes to "H" again in this status, the CWDT pin initiates the charge-discharge operation.

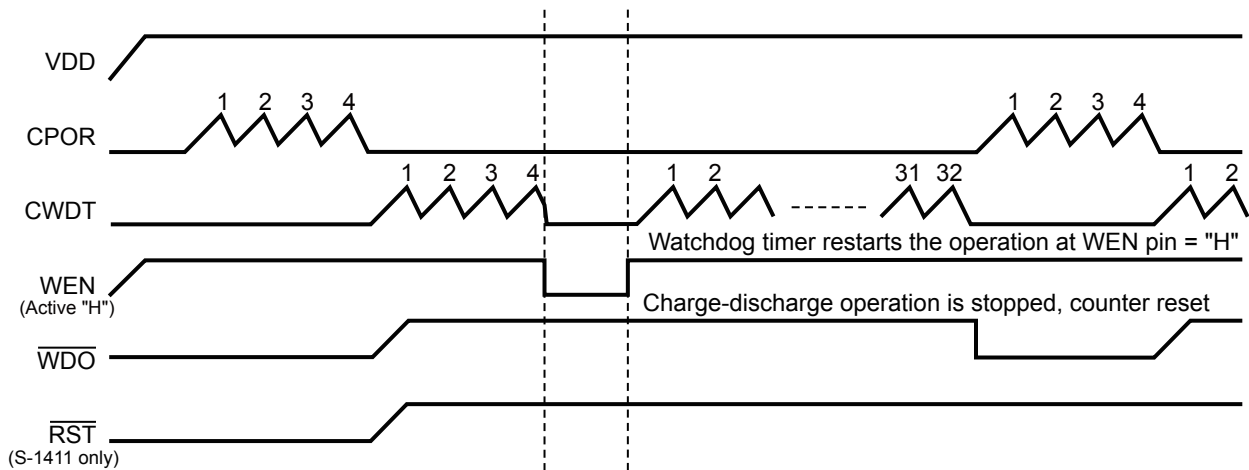


Figure 50

6. Watchdog double pulse detection

If an edge is input to the WDI pin again within a specific period of time (the discharge time due to an edge detection + 1 charge-discharge time (t_{WDL})) after inputting an edge to the WDI pin when the S-1410/1411 Series is the window mode, the \overline{WDO} pin output changes from "H" to "L".

When the watchdog timer becomes Disable due to a change of the WEN pin ("H" → "L" → "H") after inputting an edge to the WDI pin, the \overline{WDO} pin continues outputting "H" even if an edge is input to the WDI pin within the specific period of time mentioned above.

6.1 Double pulse detection due to rising edge detection
 (S-141xAxx, S-141xDxx, S-141xGxx, S-141xJxx)

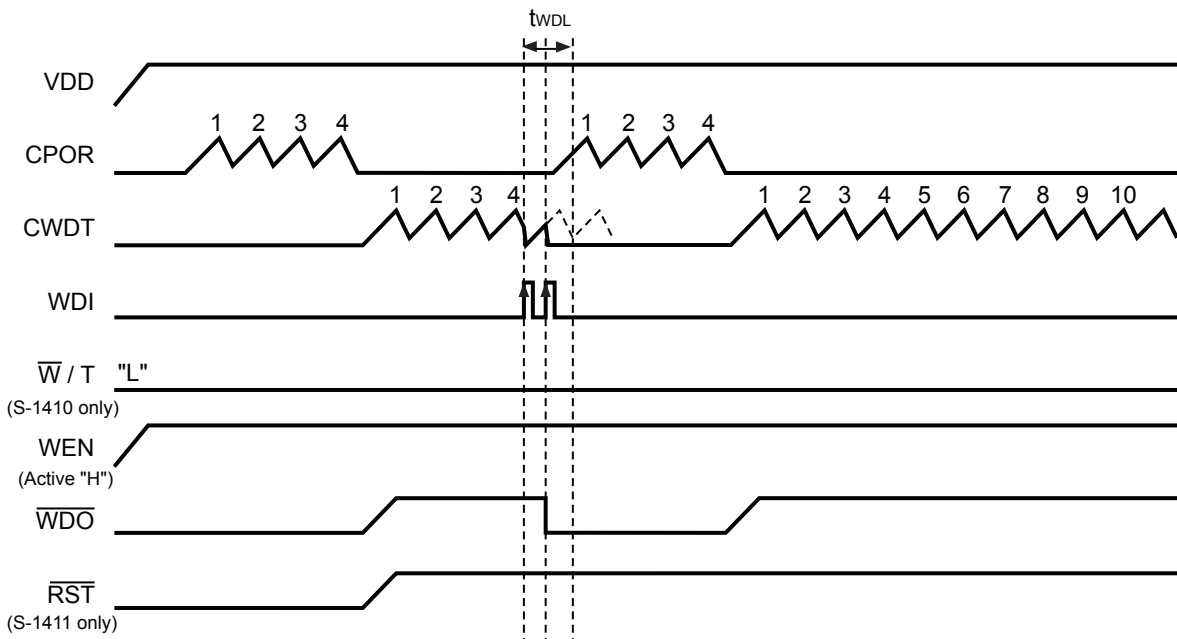


Figure 51

6.2 Double pulse detection due to falling edge detection
 (S-141xBxx, S-141xExx, S-141xHxx, S-141xKxx)

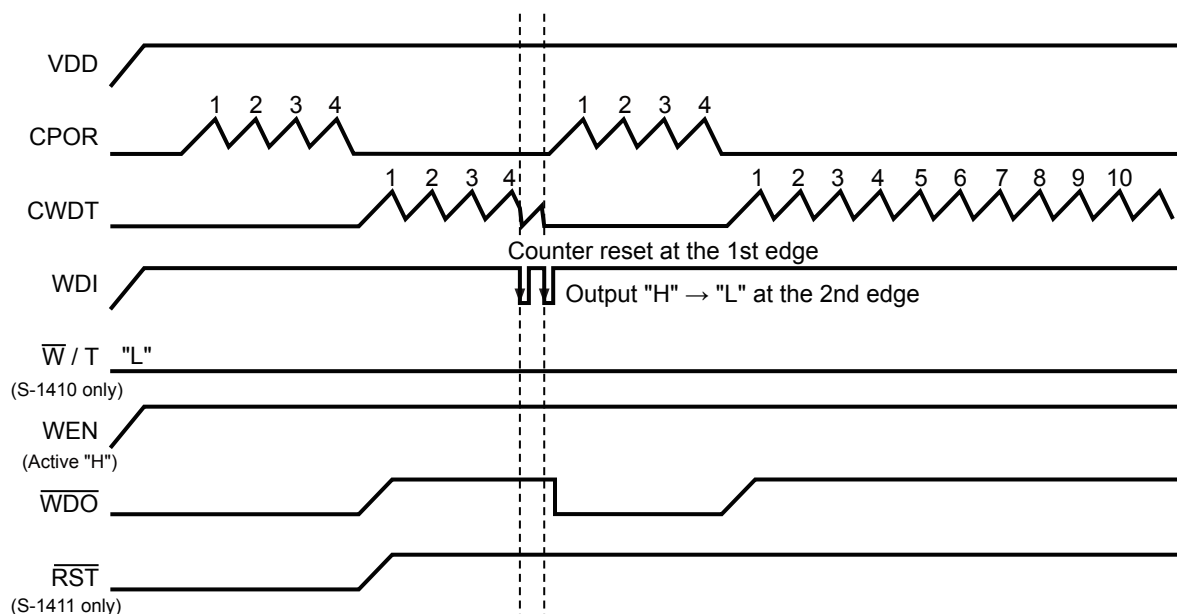


Figure 52

6.3 Double pulse detection due to both rising and falling edges detection
 (S-141xCxx, S-141xFxx, S-141xlxx, S-141xLxx)

The double pulse is detected only when edges are input in order of rising and falling.

6.3.1 When edges are input to WDI pin in order of rising and falling

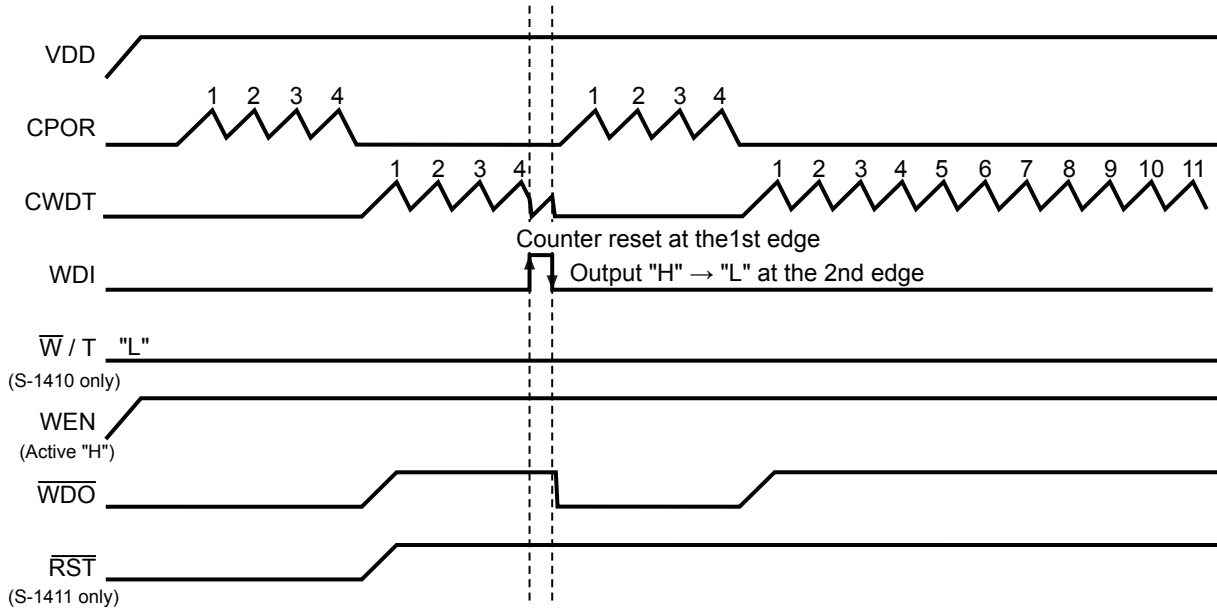


Figure 53 Double Pulse Detection

6.3.2 When edges are input to WDI pin in order of falling and rising

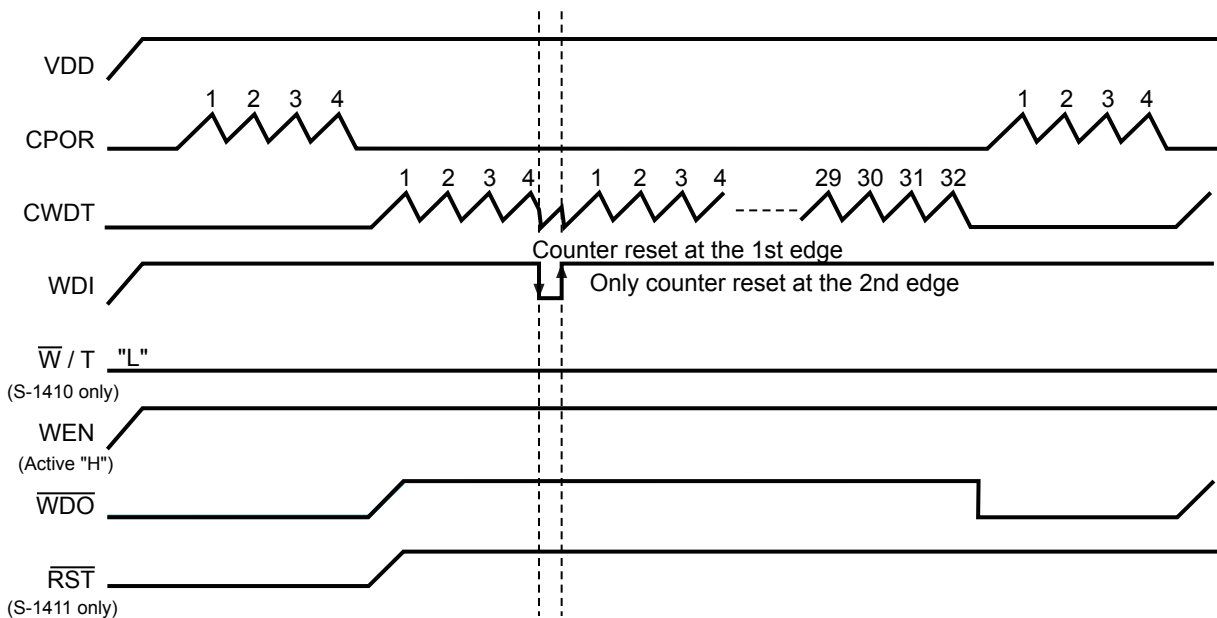


Figure 54 Double Pulse Non-detection

7. Operation of low voltage detection

The voltage detection circuit detects a low voltage if the power supply voltage falls below the detection voltage, and then "L" is output from the \overline{WDO} pin and the \overline{RST} pin (Only the S-1411 Series). The output is maintained until the charge-discharge operation of the CPOR pin is performed 4 times.

The S-1410/1411 Series can detect a low voltage even if either the CPOR pin or the WDT pin performs the charge-discharge operation. In this case, the status of the WEN pin or the \overline{W} / T pin does not have an affect.

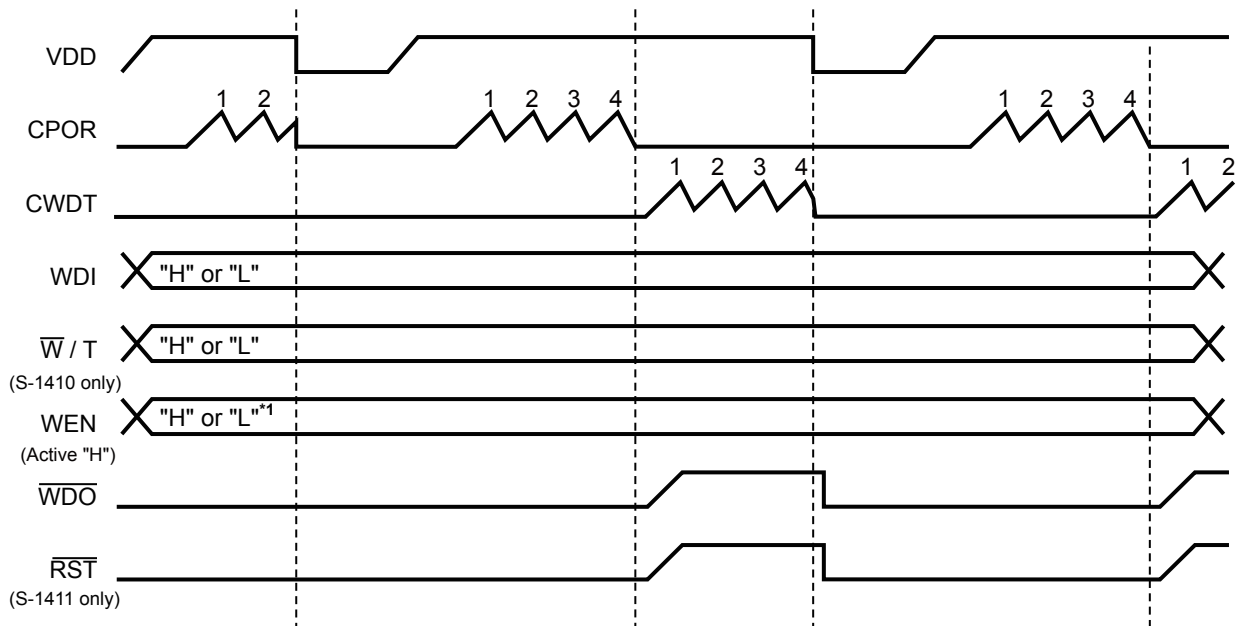


Figure 55

*1. When the WEN pin is Disable, the charge-discharge operation of CWDT pin is not performed.

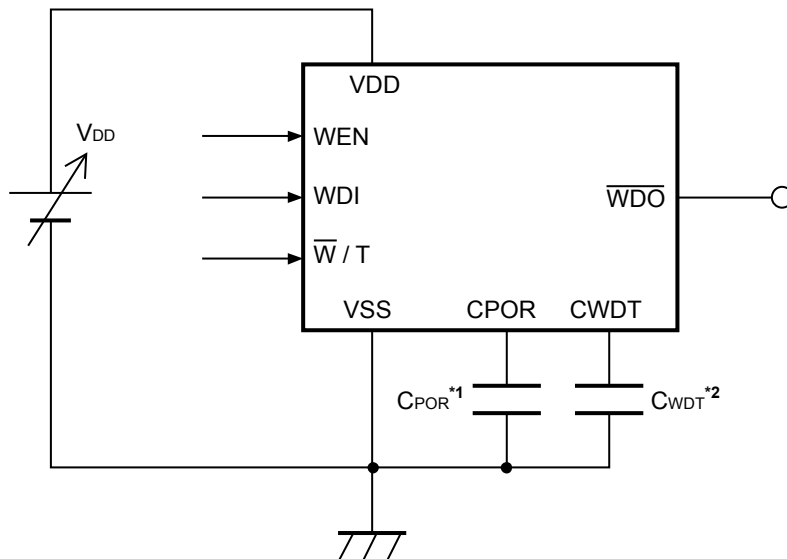
8. WEN pin, WDI pin and \overline{W} / T pin

Each of the WEN pin, the WDI pin and the \overline{W} / T pin has a noise filter.

If the power supply voltage is 5.0 V, noise with a minimum pulse width of 200 ns can be eliminated.

■ Standard Circuits

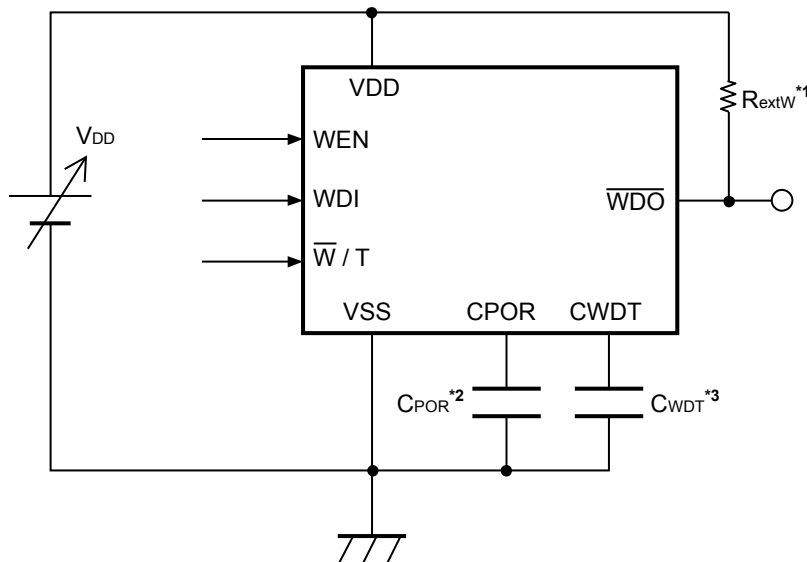
1. S-1410 Series A / B / C / D / E / F type



- *1. Adjustment capacitor for reset output delay time (C_{POR}) should be connected directly to the CPOR pin and the VSS pin.
- *2. Adjustment capacitor for watchdog output delay time (C_{WDT}) should be connected directly to the CWDT pin and the VSS pin. A capacitor of 100 pF to 1 μF can be used for C_{POR} and C_{WDT} .

Figure 56

2. S-1410 Series G / H / I / J / K / L type

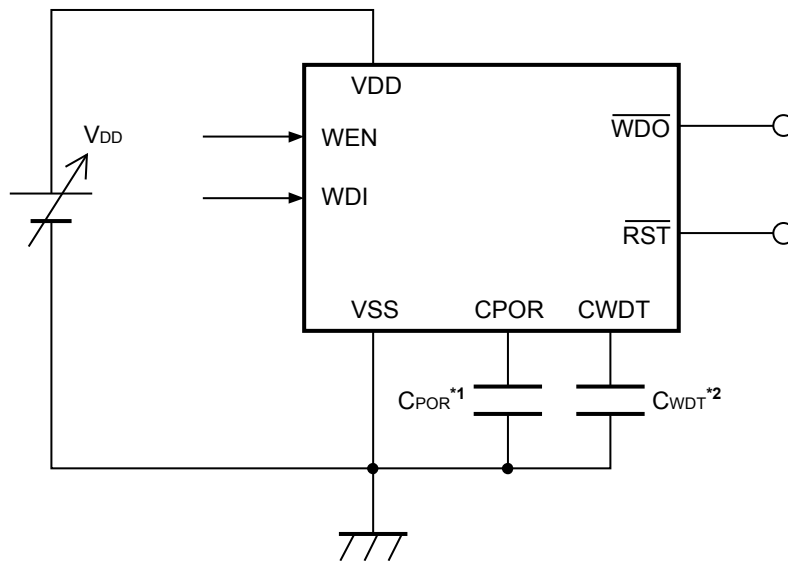


- *1. R_{extW} is an external pull-up resistor for the \overline{WDO} pin.
- *2. Adjustment capacitor for reset output delay time (C_{POR}) should be connected directly to the CPOR pin and the VSS pin.
- *3. Adjustment capacitor for watchdog output delay time (C_{WDT}) should be connected directly to the CWDT pin and the VSS pin. A capacitor of 100 pF to 1 μF can be used for C_{POR} and C_{WDT} .

Figure 57

Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

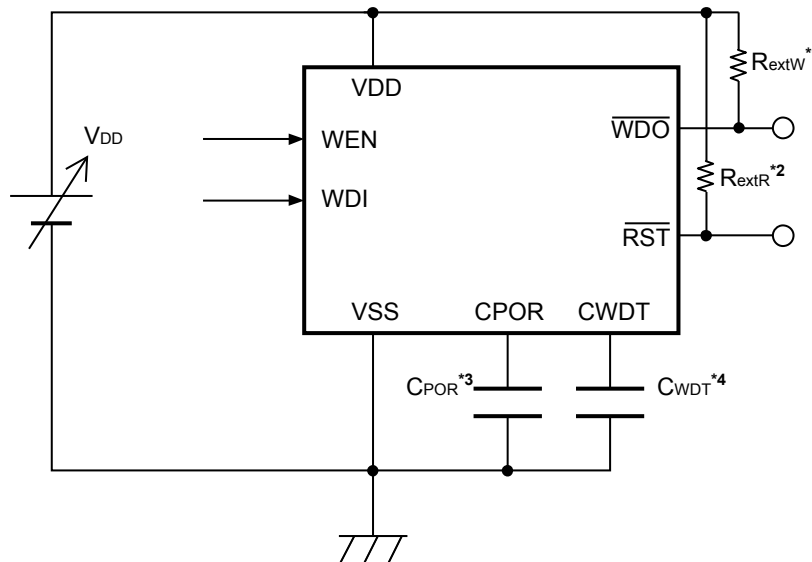
3. S-1411 Series A / B / C / D / E / F type



- *1. Adjustment capacitor for reset output delay time (C_{POR}) should be connected directly to the CPOR pin and the VSS pin.
- *2. Adjustment capacitor for watchdog output delay time (C_{WDT}) should be connected directly to the CWDT pin and the VSS pin. A capacitor of 100 pF to 1 μF can be used for C_{POR} and C_{WDT} .

Figure 58

4. S-1411 Series G / H / I / J / K / L type



- *1. R_{extW} is an external pull-up resistor for the \overline{WDO} pin.
- *2. R_{extR} is an external pull-up resistor for the \overline{RST} pin.
- *3. Adjustment capacitor for reset output delay time (C_{POR}) should be connected directly to the CPOR pin and the VSS pin.
- *4. Adjustment capacitor for watchdog output delay time (C_{WDT}) should be connected directly to the CWDT pin and the VSS pin. A capacitor of 100 pF to 1 μF can be used for C_{POR} and C_{WDT} .

Figure 59

Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Precautions

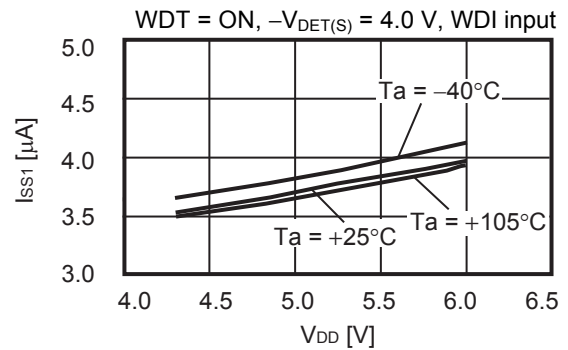
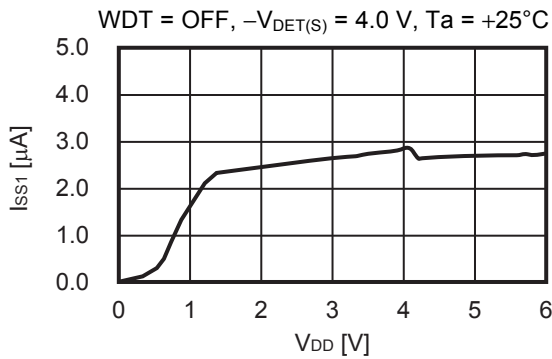
- It will take time for the discharge operation to be performed if the capacitance of C_{POR} is extremely large at the low voltage detection, so the discharge operation may not be completed by the time the power supply voltage exceeds the detection voltage. In that case, since the charge-discharge operation of the CPOR pin is performed after the discharge operation is completed, the delay time of the same time length as the discharge operation occurs in reset time-out period (t_{RST}).
- Select a capacitor which satisfies the following equation for C_{POR} and C_{WDT} . If this condition is not satisfied, the delay time of the same time length as the discharge operation occurs in t_{RST} since the discharge operation of an external capacitor connected to the CWDT pin is not completed by the time the CWDT pin initiates the next charge-discharge operation.

$$C_{WDT} / C_{POR} \leq 600$$

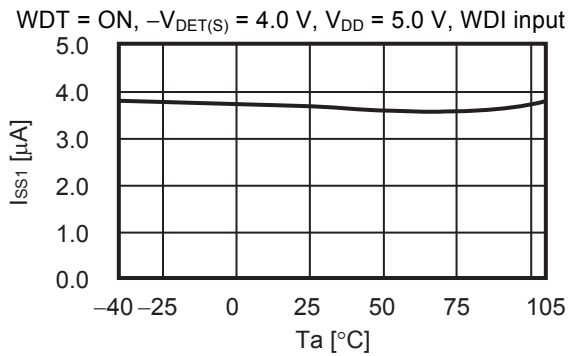
- When the power supply voltage falls to 0.9 V or lower, set a time interval of 20 μs or longer by the time the power supply is raised again. If the appropriate time length is not secured, the time-out period after raising the power supply voltage may get delayed.
- When the time that the power supply voltage falls below the detection voltage is short, the S-1410/1411 Series may not detect a voltage. In that case, the time-out period after raising the power supply voltage may get delayed.
- Since input pins (the WEN pin, the WDI pin and the \overline{W} / T pin) in the S-1410/1411 Series are CMOS configurations, make sure that an intermediate potential is not input when the S-1410/1411 Series operates.
- Since the \overline{WDO} pin and the \overline{RST} pin are affected by external resistance and external capacitance, use the S-1410/1411 Series after performing thorough evaluation with the actual application.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

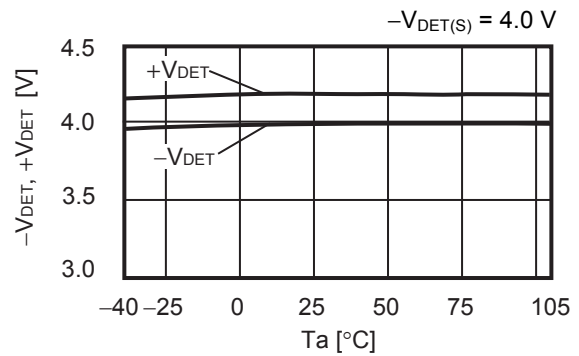
1. Current consumption during operation (I_{SS1}) vs. Input voltage (V_{DD})



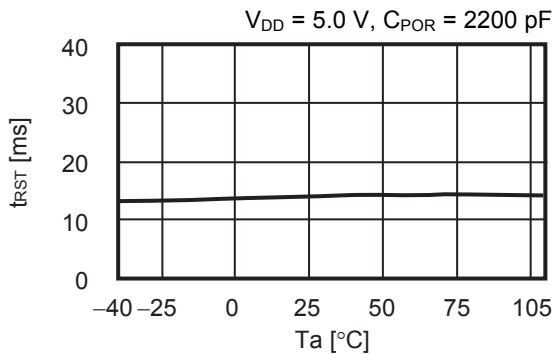
2. Current consumption during operation (I_{SS1}) vs. Temperature (T_a)



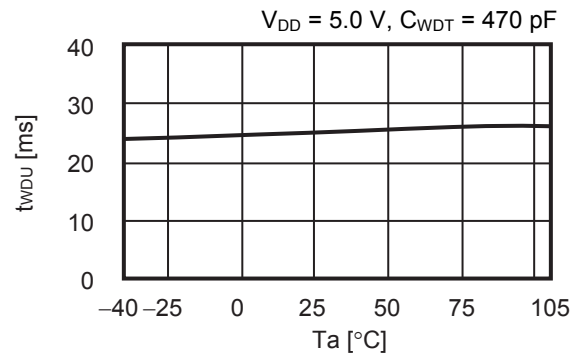
3. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Temperature (T_a)



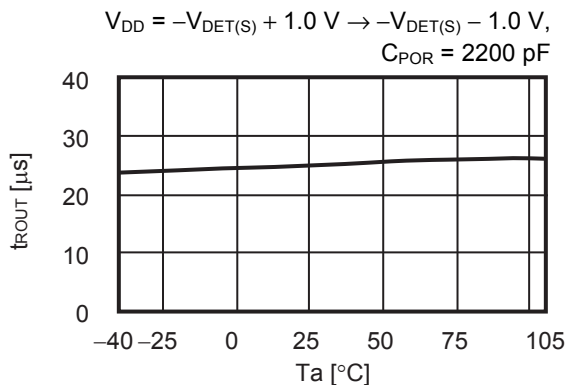
4. Reset time-out period (t_{RST}) vs. Temperature (T_a)



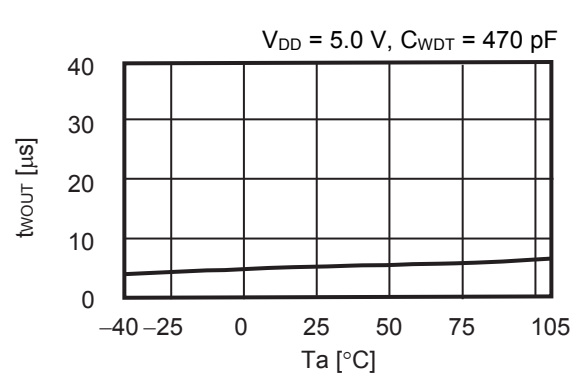
5. Watchdog time-out period (t_{WDU}) vs. Temperature (T_a)



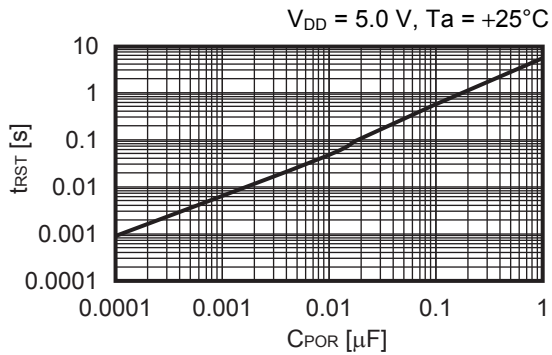
6. Reset output delay time (t_{ROUT}) vs. Temperature (T_a)



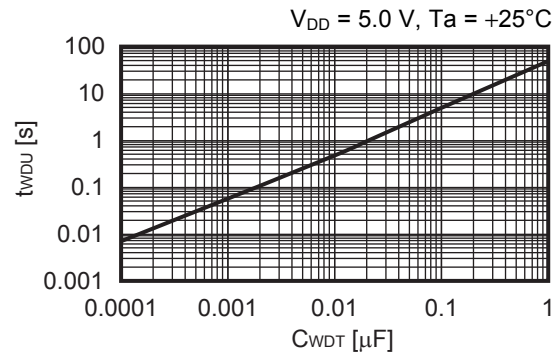
7. Watchdog output delay time (t_{WOUT}) vs. Temperature (T_a)



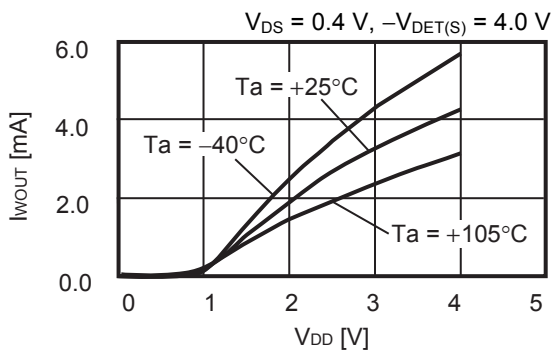
8. Reset time-out period (t_{RST}) vs. C_{POR}



9. Watchdog time-out period (t_{WDT}) vs. C_{WDT}

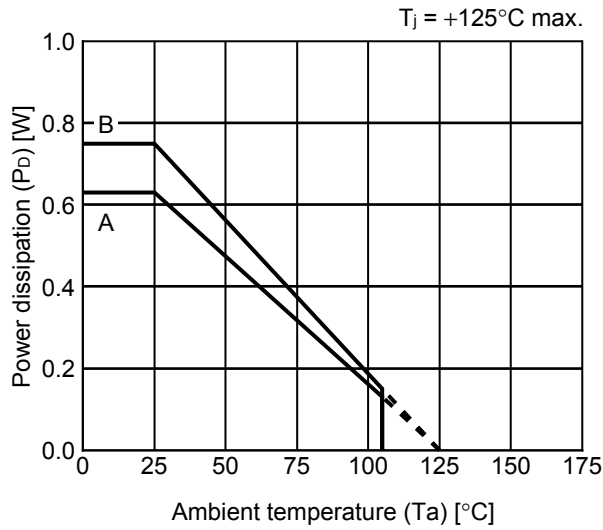


10. Nch driver output current (I_{WOUT}) vs. Input voltage (V_{DD})



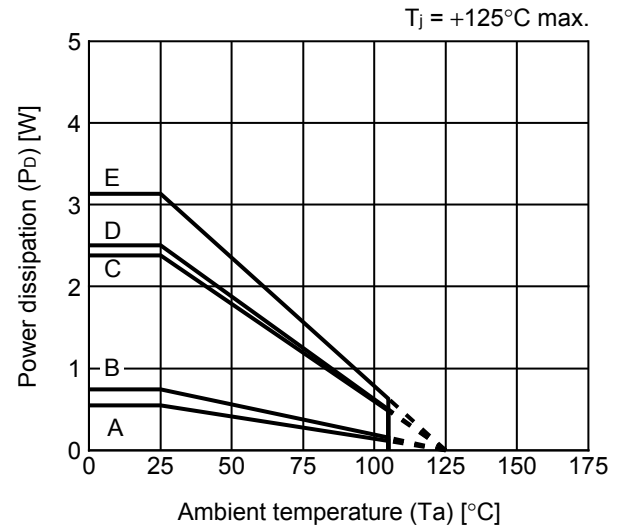
■ Power Dissipation

TMSOP-8



Board	Power Dissipation (P_D)
A	0.63 W
B	0.75 W
C	–
D	–
E	–

HSNT-8(2030)

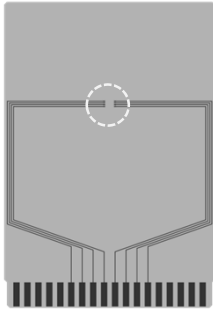


Board	Power Dissipation (P_D)
A	0.55 W
B	0.74 W
C	2.50 W
D	2.38 W
E	3.13 W

TMSOP-8 Test Board

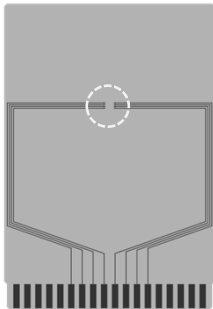
(1) Board A

 IC Mount Area



Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	2	
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via	-	

(2) Board B



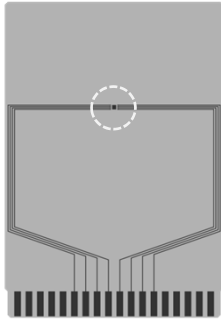
Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	4	
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via	-	

No. TMSOP8-A-Board-SD-1.0

HSNT-8(2030) Test Board

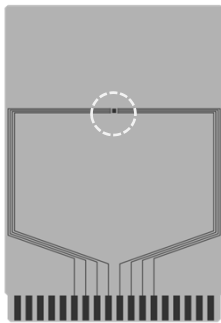
 IC Mount Area

(1) Board A



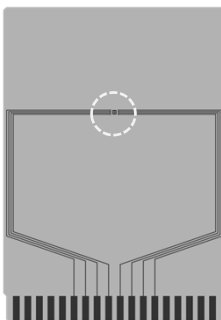
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C




Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



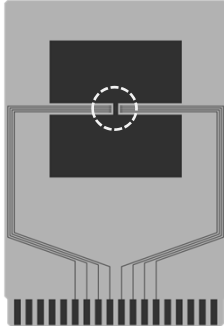
enlarged view

No. HSNT8-A-Board-SD-2.0

HSNT-8(2030) Test Board

 IC Mount Area

(4) Board D

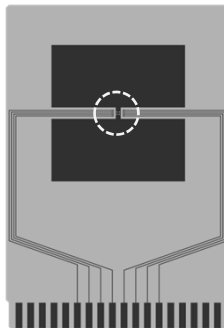


Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	4	
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm ² t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via	-	



enlarged view

(5) Board E

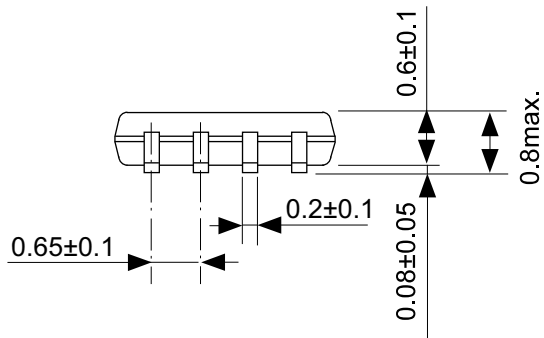
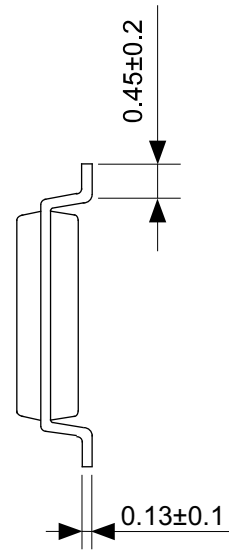
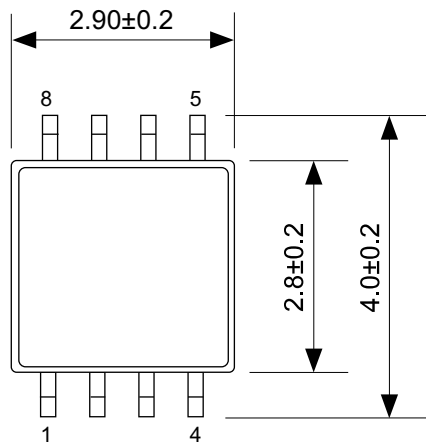


Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	4	
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm ² t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via	Number: 4 Diameter: 0.3 mm	



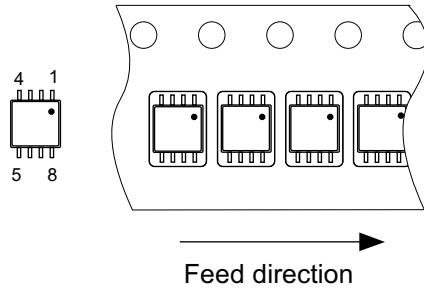
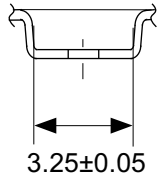
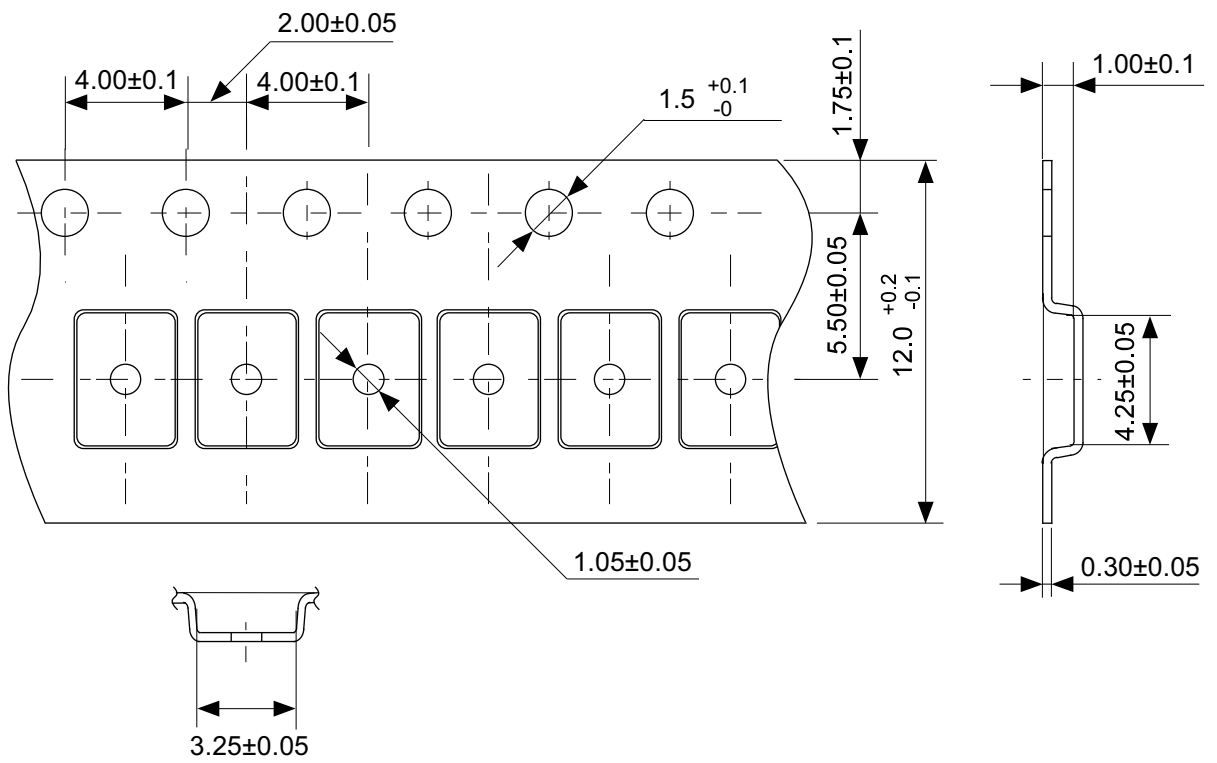
enlarged view

No. HSNT8-A-Board-SD-2.0



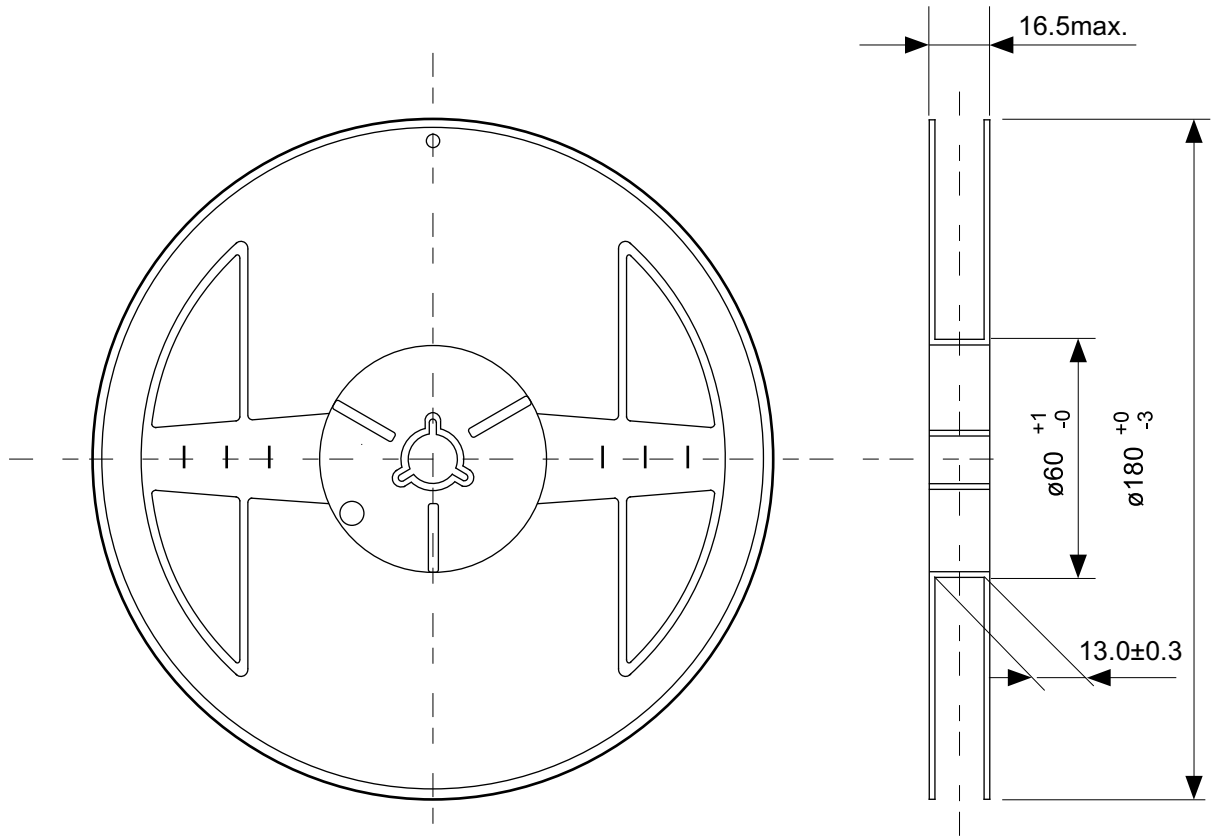
No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	

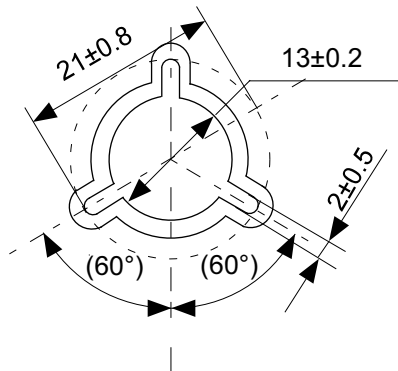


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

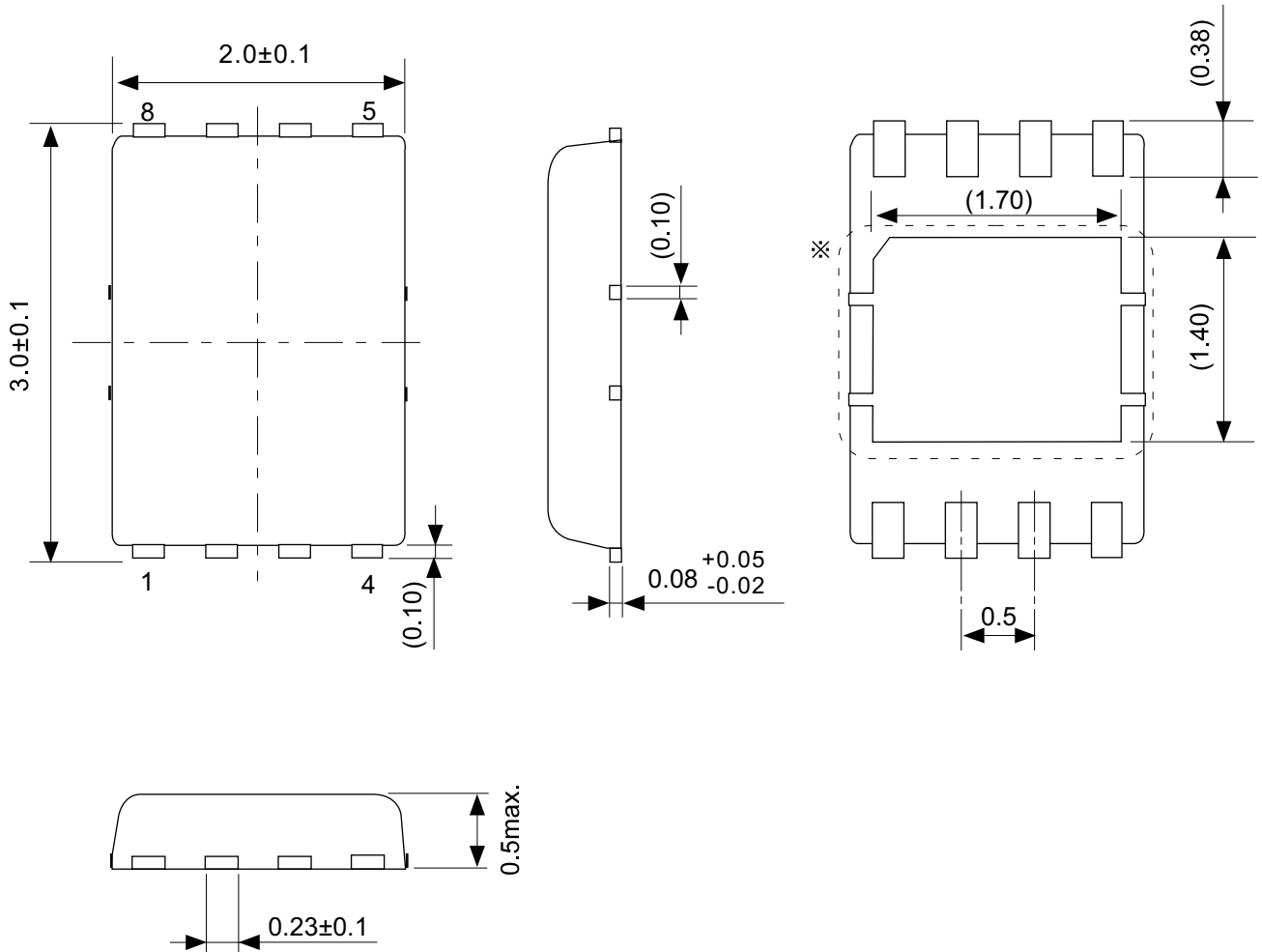


Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

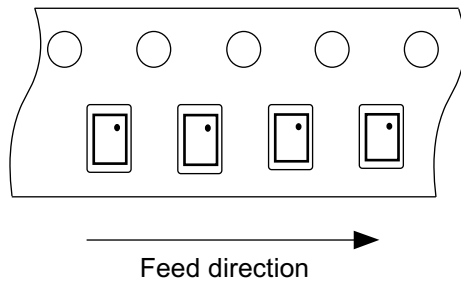
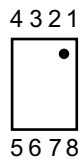
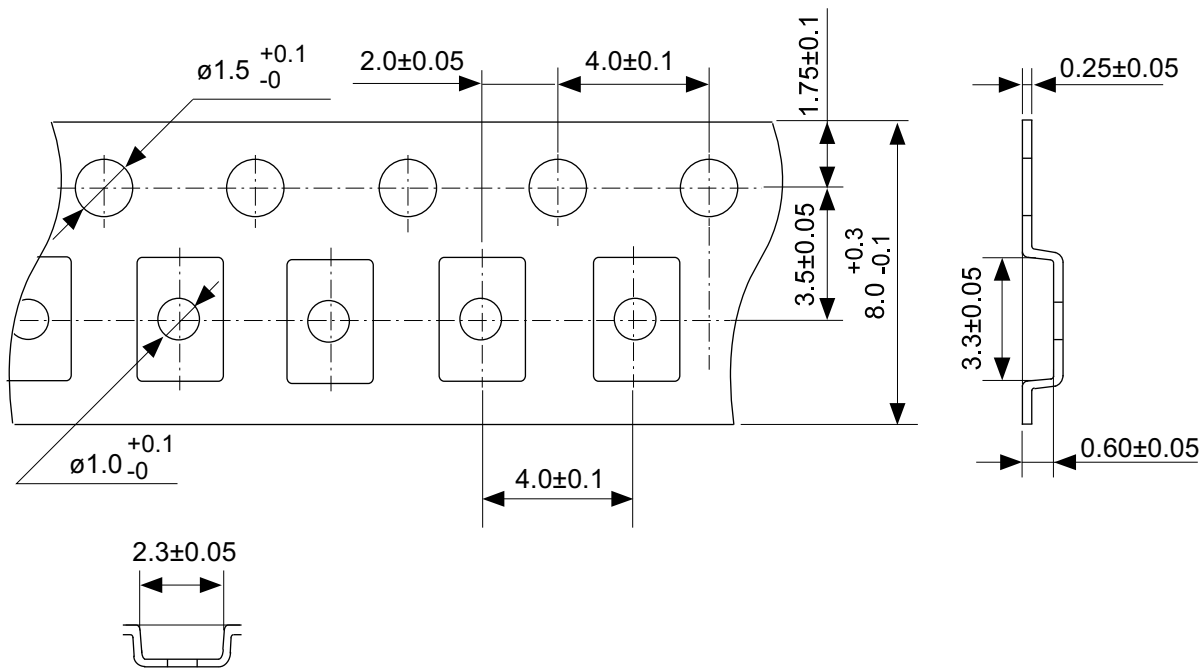
TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



\ast The heat sink of back side has different electric potential depending on the product.
 Confirm specifications of each product.
 Do not use it as the function of electrode.

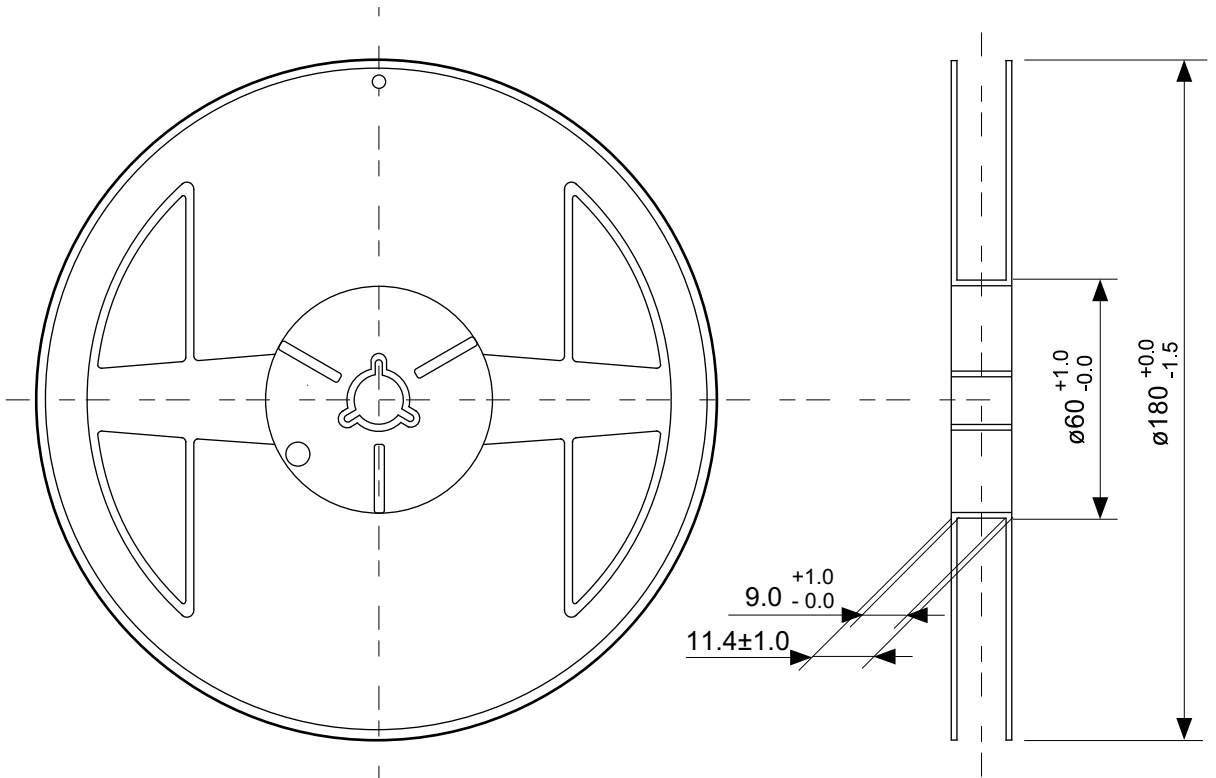
No. PP008-A-P-SD-2.0

TITLE	HSNT-8-A-PKG Dimensions
No.	PP008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

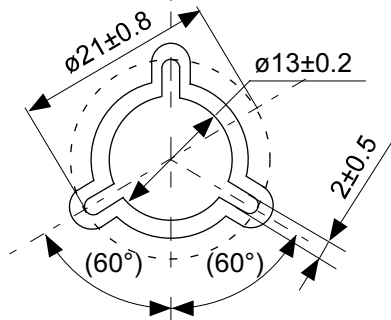


No. PP008-A-C-SD-1.0

TITLE	HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

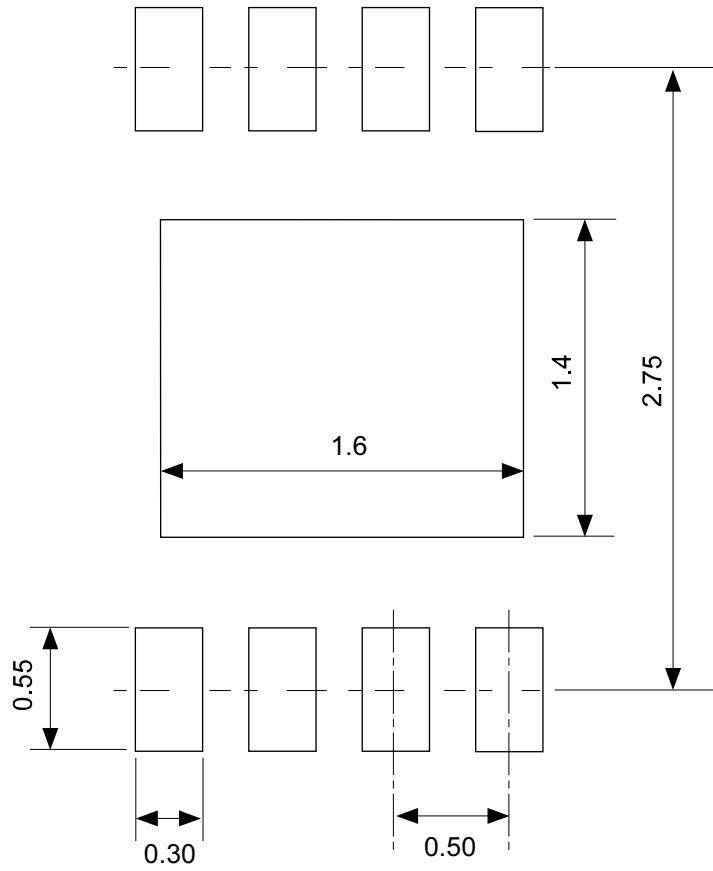


Enlarged drawing in the central part



No. PP008-A-R-SD-1.0

TITLE	HSNT-8-A-Reel		
No.	PP008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



No. PP008-A-L-SD-1.0

TITLE	HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.2-2018.06