S-1410/1411 Series

LOW CURRENT CONSUMPTION WATCHDOG TIMER WITH RESET FUNCTION

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Rev.1.0_01

The S-1410/1411 Series is a watchdog timer developed using CMOS technology, which can operate with low current consumption of 3.8 μA typ. The reset function and the low voltage detection function are available.

■ Features

- Detection voltage: 2.0 V to 5.0 V, selectable in 0.1 V step
- Detection voltage accuracy: ±1.5%
- Input voltage: V_{DD} = 0.9 V to 6.0 V
- Hysteresis width: 5% typ.
- Current consumption: 3.8 μA typ.
- Reset time-out period: 14.5 ms typ. (C_{POR} = 2200 pF)
- Watchdog operation is switchable: Enable, Disable
- Watchdog operation voltage range: 2.5 V to 6.0 V
- Watchdog mode switching function*1: Time-out mode, window mode
- Watchdog input edge is selectable: Rising edge, falling edge, both rising and falling edges
- Product type is selectable: S-1410 Series
  (Product with $\overline{W}$ / T pin (Output: $\overline{WDO}$ pin))
  S-1411 Series
  (Product without $\overline{W}$ / T pin (Output: $\overline{RST}$ pin, $\overline{WDO}$ pin))
- Operation temperature range: Ta = −40°C to +105°C
- Lead-free (Sn 100%), halogen-free

***1.** The S-1411 Series is fixed to the window mode.

■ Applications

- Power supply monitoring of microcontroller mounted apparatus and system monitoring

■ Package

- TMSOP-8

■ Block Diagrams

1. S-1410 Series (Product with $\overline{W}$ / T pin)

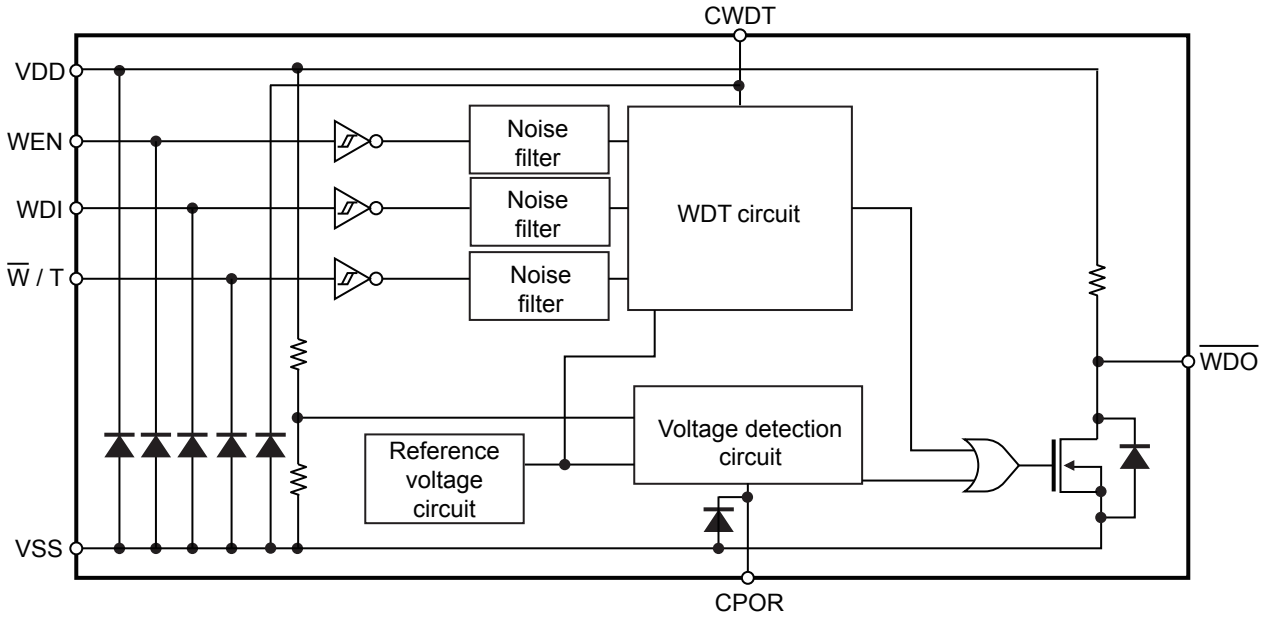


Figure 1

2. S-1411 Series (Product without $\overline{W}$ / T pin)

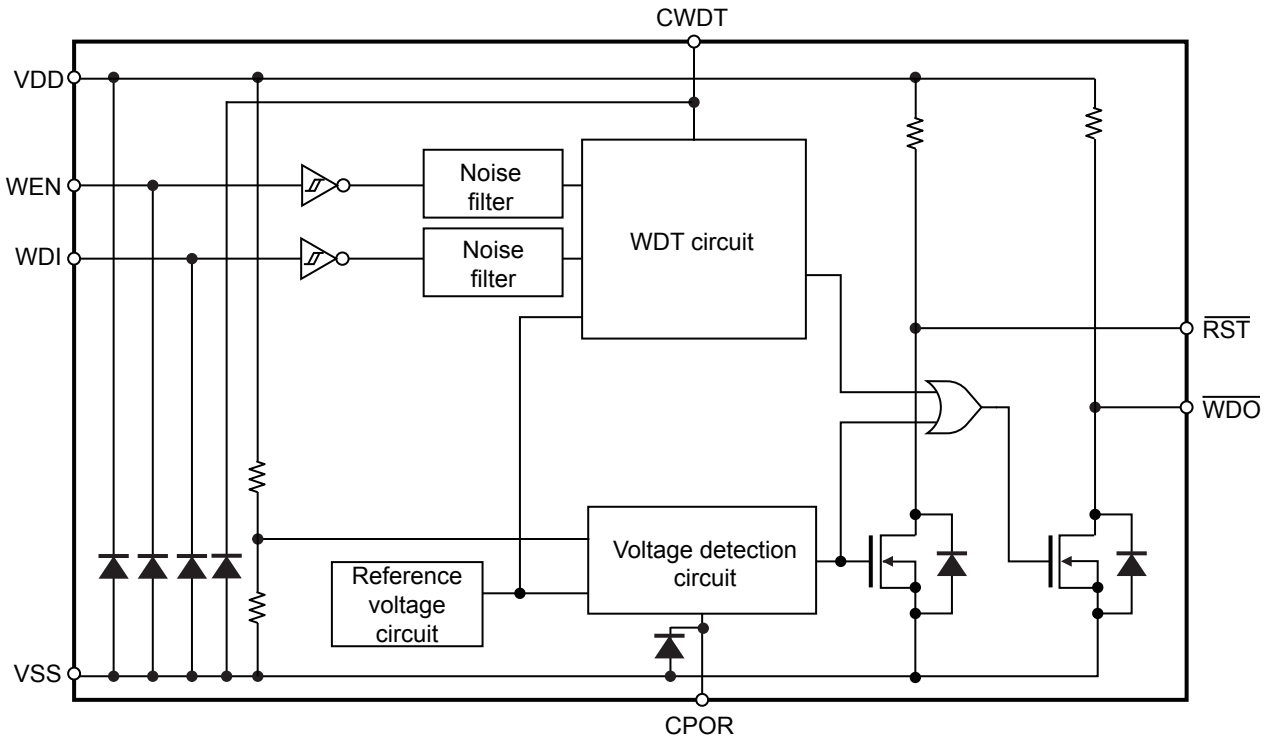


Figure 2

■ Product Name Structure

Users can select the product types, detection voltage for the S-1410/1411 Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Product type list**" regarding the product types, "**3. Package**" regarding the package drawings.

1. Product name

S-141 x x xx - K8T2 U 4

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - K8T2: TMSOP-8, Tape
- Detection voltage
  - 20 to 50
  - (e.g., when the detection voltage is 2.0 V, it is expressed as 20.)
- Product type 1*2
  - A to L
- Product type 2*3
  - 0, 1

***1.** Refer to the tape drawing.
***2.** Refer to "**2. Product type list**".
***3.** 0: S-1410 Series (Product with $\overline{W}$ / T pin)
The $\overline{WDO}$ pin outputs the signals which are from the watchdog timer circuit and the voltage detection circuit.
1: S-1411 Series (Product without $\overline{W}$ / T pin)
The $\overline{WDO}$ pin outputs the signals which are from the watchdog timer circuit and the voltage detection circuit.
The $\overline{RST}$ pin outputs the signal which is from the voltage detection circuit.
The watchdog mode is fixed to the window mode.

2. Product type list

Table 1

Product Type	WEN Pin Logic	Input Edge	Output Pull-up Resistor
A	Active "H"	Rising edge	Available
B	Active "H"	Falling edge	Available
C	Active "H"	Both rising and falling edges	Available
D	Active "L"	Rising edge	Available
E	Active "L"	Falling edge	Available
F	Active "L"	Both rising and falling edges	Available
G	Active "H"	Rising edge	Unavailable
H	Active "H"	Falling edge	Unavailable
I	Active "H"	Both rising and falling edges	Unavailable
J	Active "L"	Rising edge	Unavailable
K	Active "L"	Falling edge	Unavailable
L	Active "L"	Both rising and falling edges	Unavailable

3. Package

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

■ Pin Configuration

1. TMSOP-8

Top view

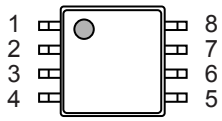


Figure 3

Table 3 S-1410 Series (Product with $\overline{W}$ / T pin)

Pin No.	Symbol	Description
1	$\overline{W}$ / T*1	Watchdog mode switching pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	$\overline{WDO}$	Watchdog output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

***1.** $\overline{W}$ / T pin = "H": Time-out mode
$\overline{W}$ / T pin = "L": Window mode

Table 4 S-1411 Series (Product without $\overline{W}$ / T pin)

Pin No.	Symbol	Description
1	$\overline{RST}$	Reset output pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	$\overline{WDO}$	Watchdog output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

■ Pin Functions

Refer to "■ **Operation**" for details.

1. $\overline{W}$ / T pin (S-1410 Series only)

This is a pin to switch the watchdog mode.
The S-1410 Series changes to the time-out mode when the $\overline{W}$ / T pin is "H", and changes to the window mode when the $\overline{W}$ / T pin is "L". Switching the mode is prohibited during the operation.
The $\overline{W}$ / T pin has a built-in pull-down resistor.

1. 1 Time-out mode ($\overline{W}$ / T pin = "H")

The S-1410 Series detects an abnormality when not inputting an edge to the WDI pin during the watchdog time-out period (t_{WDU}). And then "L" is output from the $\overline{WDO}$ pin.

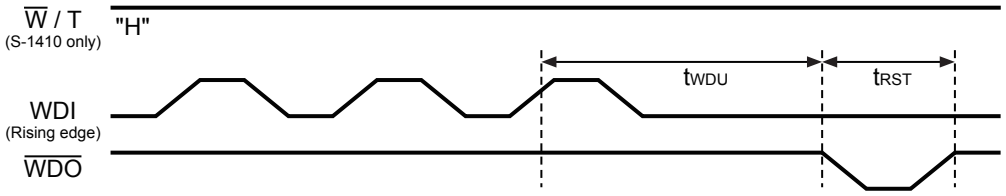


Figure 4 Abnormality Detection in Time-out Mode

1. 2 Window mode ($\overline{W}$ / T pin = "L")

When not inputting an edge to the WDI pin during t_{WDU}, or when an edge is input to the WDI pin again within a specific period of time (the discharge time due to an edge detection + 1 charge-discharge time (t_{WDL})) after inputting an edge to the WDI pin, the $\overline{WDO}$ pin output changes from "H" to "L".

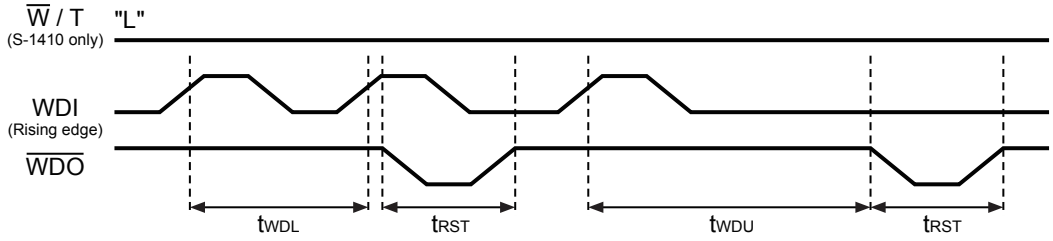


Figure 5 Abnormality Detection in Window Mode

2. $\overline{RST}$ pin (S-1411 Series only)

This is a reset output pin. It outputs "L" when detecting a low voltage.
Be sure to connect a pull-up resistor to the $\overline{RST}$ pin in the product without an output pull-up resistor.

3. CPOR pin

This is a pin to connect an external capacitor in order to generate the reset time-out period (t_{RST}).
The capacitor is charged and discharged by an internal constant current circuit, and the charge-discharge duration is t_{RST}.
t_{RST} is calculated by using the following equation.

$$t_{RST} = 6{,}500{,}000 \times C_{POR}\ [F] + 0.0002$$

4. CWDT pin

This is a pin to connect an external capacitor in order to generate the watchdog time-out period (t_{WDU}) and the watchdog double pulse detection time (t_{WDL}). The capacitor is charged and discharged by an internal constant current circuit.
t_{WDU} is calculated by using the following equation.

$$t_{WDU} = 50{,}000{,}000 \times C_{WDT}\ [F] + 0.0011$$

Moreover, t_{WDL} is calculated by using the following equation.

$$t_{WDL} = \frac{t_{WDU}}{32}$$

5. WEN pin

This is a pin to switch Enable / Disable of the watchdog timer.
When the WEN pin logic is active "H", the watchdog timer becomes Enable if the input is "H", and the charge-discharge operation is performed at the CWDT pin. In the active "H" product, the WEN pin has a built-in pull-down resistor.

6. $\overline{\text{WDO}}$ pin

This pin combines the reset output and the watchdog output.
Be sure to connect a pull-up resistor to the $\overline{\text{WDO}}$ pin in the product without an output pull-up resistor.

7. WDI pin

This is an input pin to receive a signal from the monitored object. By being input an edge at an appropriate timing, the WDI pin confirms the normal operation of the monitored object.
The WDI pin has a built-in pull-down resistor.

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
VDD pin voltage	V_{DD}	V_{SS} – 0.3 to V_{SS} + 7.0	V
WDI pin voltage	V_{WDI}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
WEN pin voltage	V_{WEN}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
$\overline{W}$ / T pin voltage	$V_{\overline{W}/T}$	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
CPOR pin voltage	V_{CPOR}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
CWDT pin voltage	V_{CWDT}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
$\overline{RST}$ pin voltage	$V_{\overline{RST}}$	V_{SS} – 0.3 to V_{DD} + 0.3	V
$\overline{WDO}$ pin voltage	$V_{\overline{WDO}}$	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{ja}	TMSOP-8	Board 1	–	160	–	°C/W
			Board 2	–	133	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Thermal Characteristics**" for details of power dissipation and test board.

■ Electrical Characteristics

Table 7

(WEN pin logic active "H" product, V_{DD} = 5.0 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	–		$-V_{DET(S)} \times 0.985$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.015$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	1
Current consumption during operation	I_{SS1}	When watchdog timer operates		–	3.8	7.8	µA	2
Reset time-out period	t_{RST}	C_{POR} = 2200 pF		8.7	14.5	20	ms	3
Watchdog time-out period	t_{WDU}	C_{WDT} = 470 pF		15	24.6	34	ms	3
Watchdog double pulse detection time	t_{WDL}	C_{WDT} = 470 pF		461	769	1077	µs	4
Reset output voltage "H"	V_{ROH}	S-1411 Series A / B / C / D / E / F type only		V_{DD} – 1.0	–	–	V	5
Reset output voltage "L"	V_{ROL}	–		–	–	0.4	V	6
Reset output pull-up current	I_{RUP}	$V_{\overline{RST}}$ = 0 V, S-1411 Series A / B / C / D / E / F type only		–	–0.85	–0.4	µA	7
Reset output current	I_{ROUT}	V_{DS} = 0.4 V, S-1411 Series only	V_{DD} = 1.5 V	0.6	1.1	–	mA	8
			V_{DD} = 1.8 V	1.1	1.6	–	mA	8
			V_{DD} = 2.5 V	2.1	2.6	–	mA	8
			V_{DD} = 3.0 V	2.8	3.3	–	mA	8
Reset output leakage current	I_{RLEAK}	V_{DS} = 6.0 V, V_{DD} = 6.0 V, S-1411 Series only		–	–	0.096	µA	9
Watchdog output voltage "H"	V_{WOH}	A / B / C / D / E / F type only		V_{DD} – 1.0	–	–	V	10
Watchdog output voltage "L"	V_{WOL}	–		–	–	0.4	V	11
Watchdog output pull-up current	I_{WUP}	$V_{\overline{WDO}}$ = 0 V, A / B / C / D / E / F type only		–	–0.85	–0.4	µA	12
Watchdog output current	I_{WOUT}	V_{DS} = 0.4 V	V_{DD} = 1.5 V	0.6	1.1	–	mA	13
			V_{DD} = 1.8 V	1.1	1.6	–	mA	13
			V_{DD} = 2.5 V	2.1	2.6	–	mA	13
			V_{DD} = 3.0 V	2.8	3.3	–	mA	13
Watchdog output leakage current	I_{WLEAK}	V_{DS} = 6.0 V, V_{DD} = 6.0 V		–	–	0.096	µA	14
Input pin voltage 1 "H"	V_{SH1}	WEN pin, WDI pin		$0.7 \times V_{DD}$	–	–	V	15
Input pin voltage 1 "L"	V_{SL1}	WEN pin, WDI pin		–	–	$0.3 \times V_{DD}$	V	15
Input pin voltage 2 "H"	V_{SH2}	$\overline{W}$ / T pin, S-1410 Series only		$0.7 \times V_{DD}$	–	–	V	15
Input pin voltage 2 "L"	V_{SL2}	$\overline{W}$ / T pin, S-1410 Series only		–	–	$0.3 \times V_{DD}$	V	15
Input pulse width "H"	t_{high1}	–		1.5	–	–	µs	15
Input pulse width "L"	t_{low1}	–		1.5	–	–	µs	15
Watchdog output delay time	t_{WOUT}	–		–	25	40	µs	3
Reset output delay time	t_{ROUT}	–		–	25	40	µs	3
Input setup time	t_{iset}	–		1.0	–	–	µs	3

***1.** $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Set detection voltage

■ Test Circuits

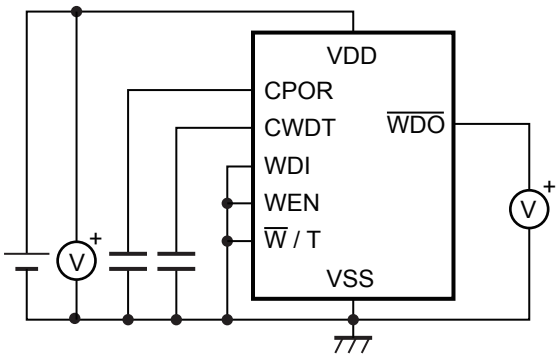


Figure 6 Test Circuit 1

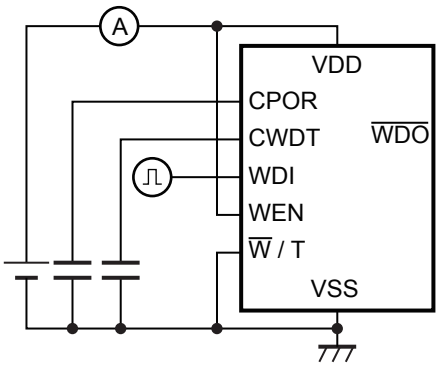


Figure 7 Test Circuit 2

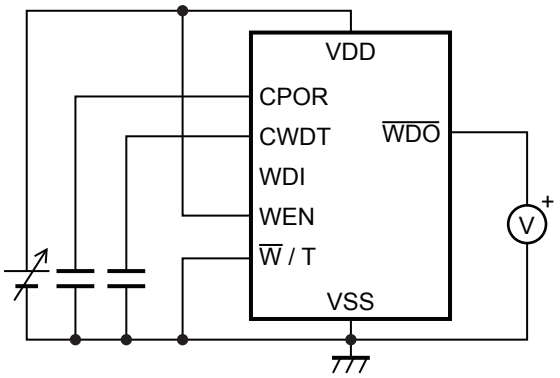


Figure 8 Test Circuit 3

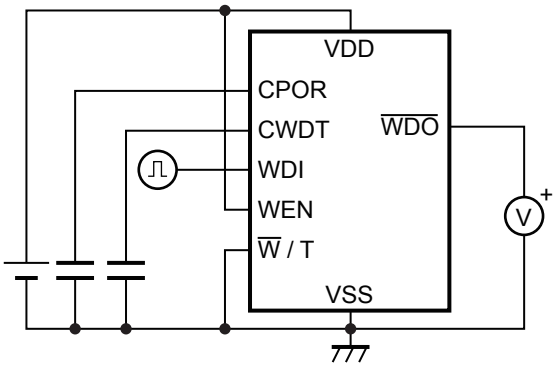


Figure 9 Test Circuit 4

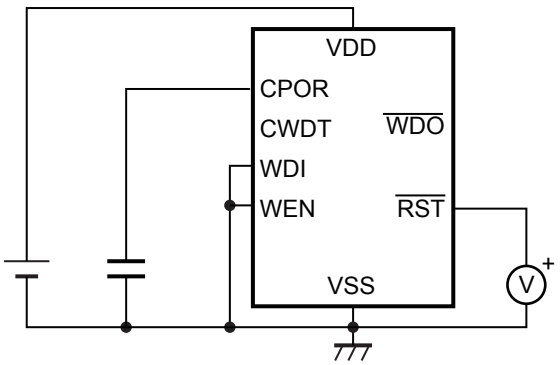


Figure 10 Test Circuit 5

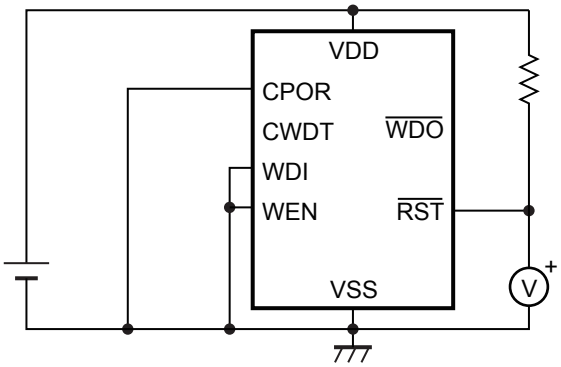


Figure 11 Test Circuit 6

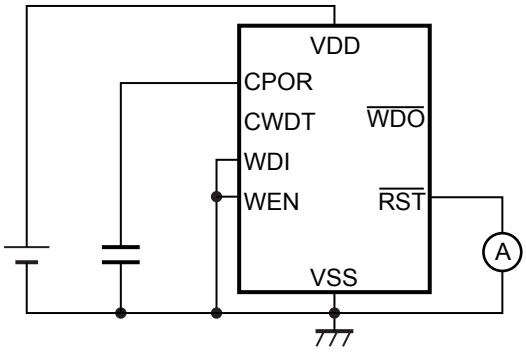


Figure 12 Test Circuit 7

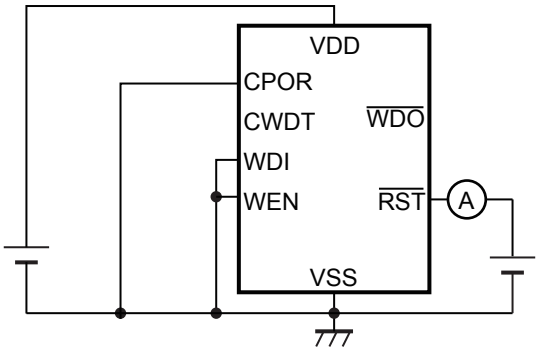


Figure 13 Test Circuit 8

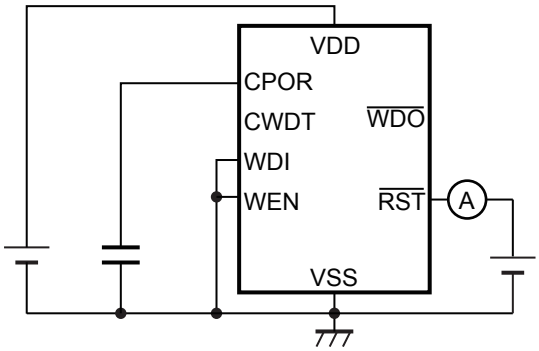


Figure 14 Test Circuit 9

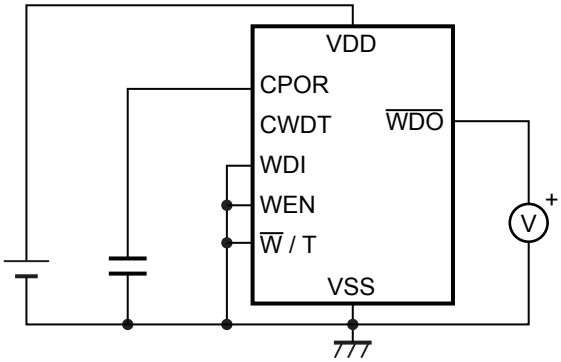


Figure 15 Test Circuit 10

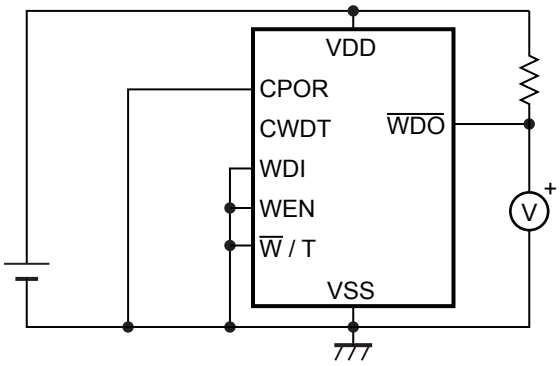


Figure 16 Test Circuit 11

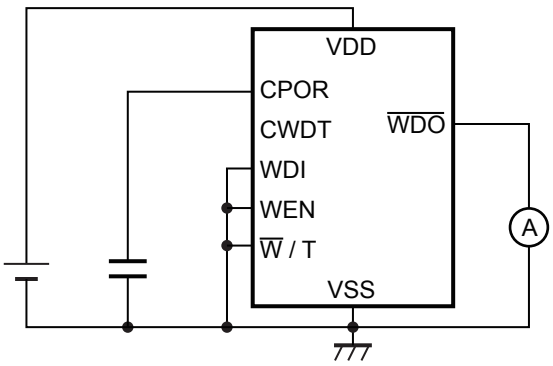


Figure 17 Test Circuit 12

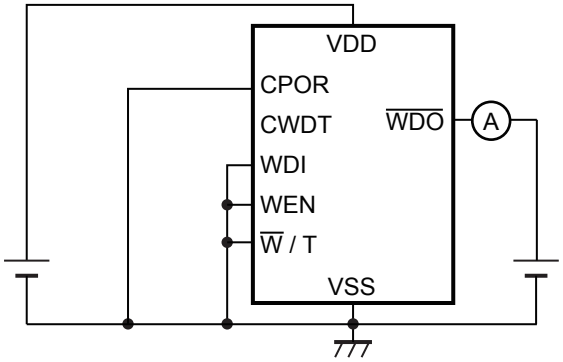


Figure 18 Test Circuit 13

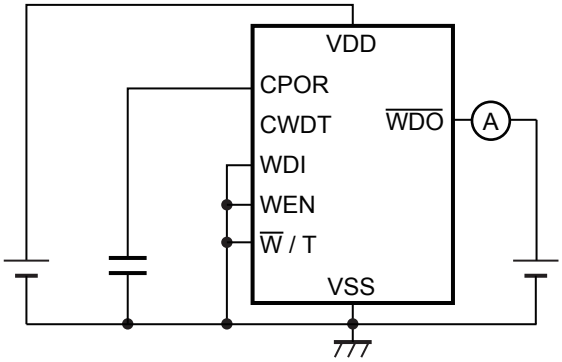


Figure 19 Test Circuit 14

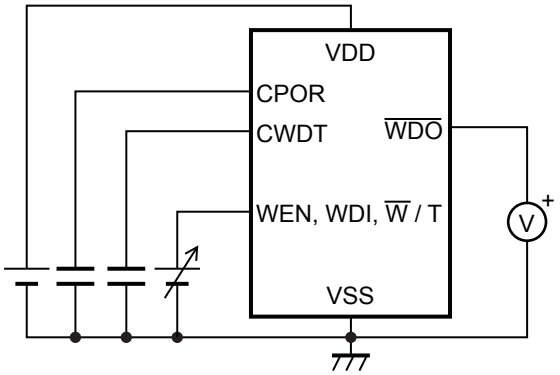
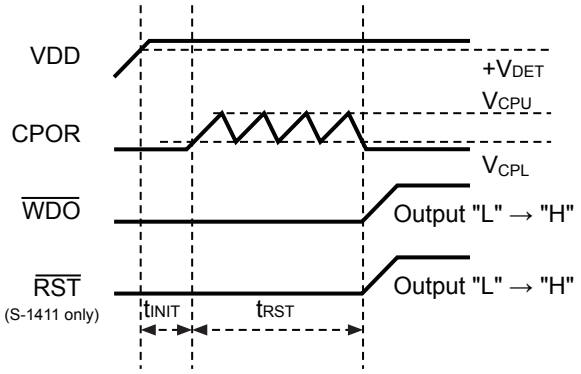


Figure 20 Test Circuit 15

■ Operation

1. From power-on to reset release

The S-1410/1411 Series initiates the initialization if the VDD pin voltage exceeds the release voltage ($+V_{DET}$).
The charge-discharge operation to the CPOR pin is initiated after the passage of the initialization time (t_{INIT}), and the $\overline{WDO}$ pin output and the $\overline{RST}$ pin output change from "L" to "H" after the operation is performed 4 times.



Remark V_{CPU}: CPOR charge upper limit threshold (1.35 V typ.)
V_{CPL}: CPOR charge lower limit threshold (0.20 V typ.)

Figure 21

t_{INIT} changes according to the power supply rising time. Refer to **Figure 22** for the relation between t_{INIT} and the power supply rising time.

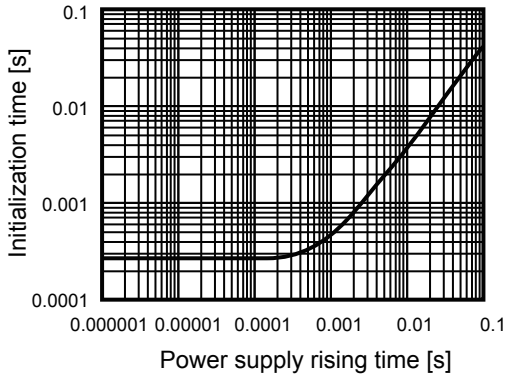
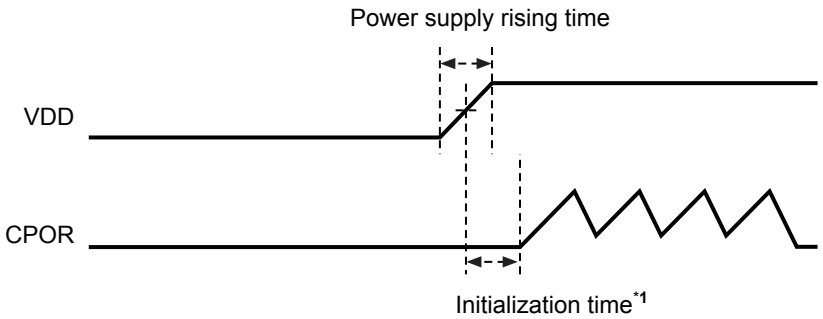


Figure 22 Power Supply Rising Time Dependency of Initialization Time



***1.** The initialization time is the time period from when the VDD pin voltage reaches V_{DD} / 2 to when C_{POR} rises.

Figure 23 Initialization Time

2. From reset release to initiation of charge-discharge operation to CWDT pin

The charge-discharge operation to the CWDT pin differs depending on the status of the WEN pin at the reset release.

2. 1 When WEN pin is "H" at reset release (Active "H")

Since the watchdog timer is Enable, the S-1410/1411 Series initiates the charge-discharge operation to the CWDT pin.

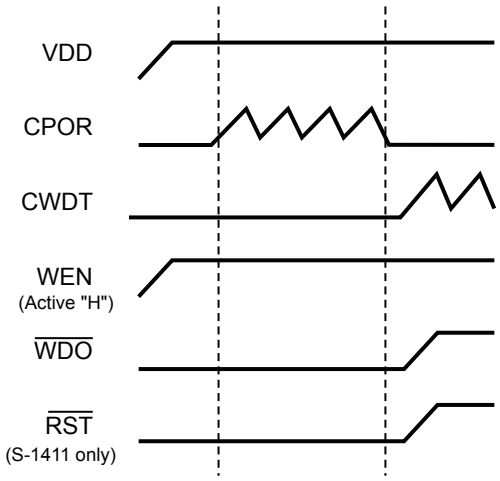


Figure 24 WEN Pin = "H"

2. 2 When WEN pin is "L" at reset release (Active "H")

Since the watchdog timer is Disable after the CPOR pin performs the charge-discharge operation 4 times, the S-1410/1411 Series does not initiate the charge-discharge operation to the CWDT pin. If the input to the WEN pin changes to "H" in this status, the S-1410/1411 Series initiates the charge-discharge operation to the CWDT pin.

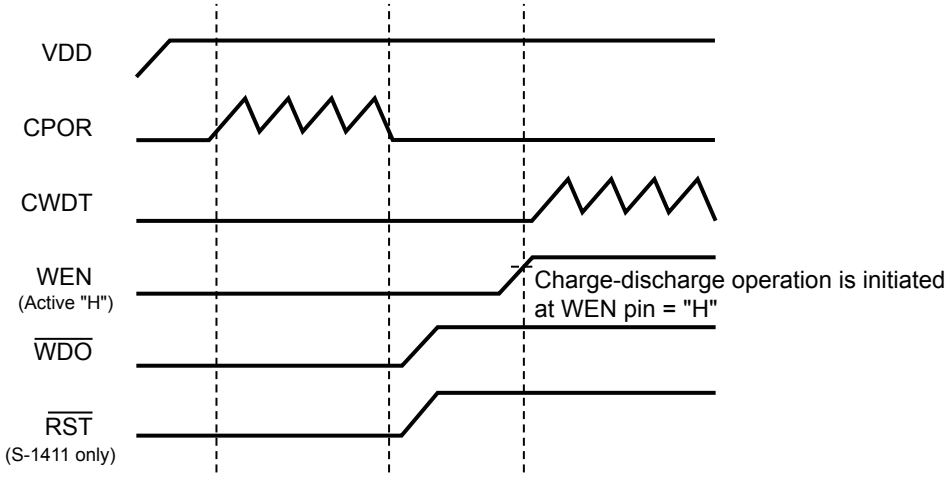


Figure 25 WEN Pin = "L" → "H"

3. Watchdog time-out detection

The watchdog timer detects a time-out after the charge-discharge operation to the CWDT pin is performed 32 times, then the $\overline{WDO}$ pin output changes from "H" to "L".

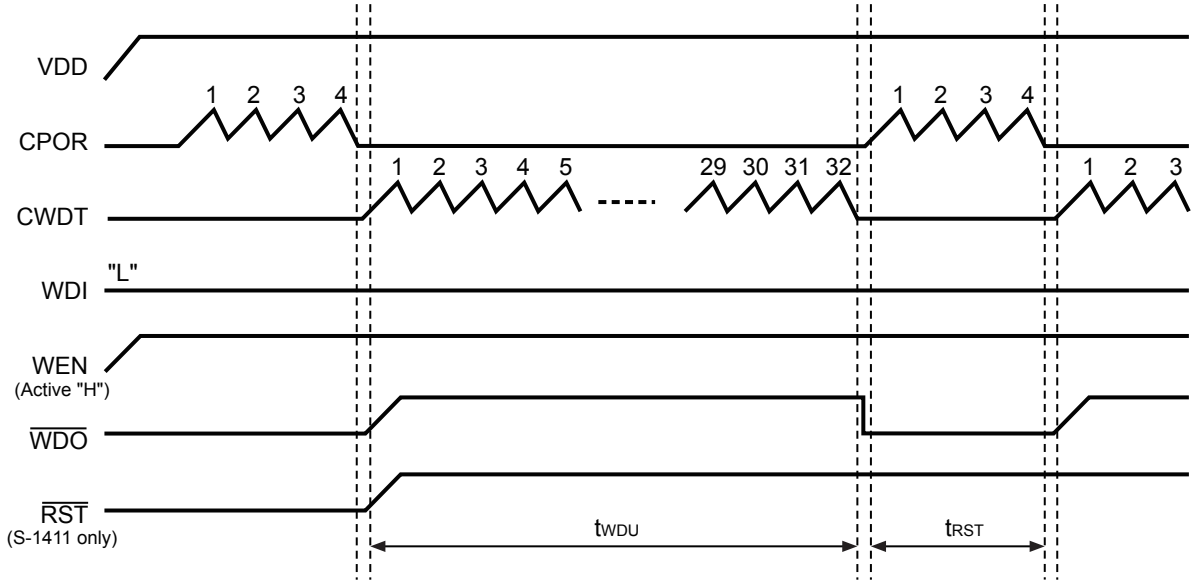


Figure 26

4. Internal counter reset due to edge detection

When the WDI pin detects an edge during the charge-discharge operation to the CWDT pin, the internal counter which counts the number of times of the charge-discharge operation is reset. The CWDT pin initiates the discharge operation when an edge is detected, and initiates the charge-discharge operation again after the discharge operation is completed.

4. 1 Counter reset due to rising edge detection (S-141xAxx, S-141xDxx, S-141xGxx, S-141xJxx)

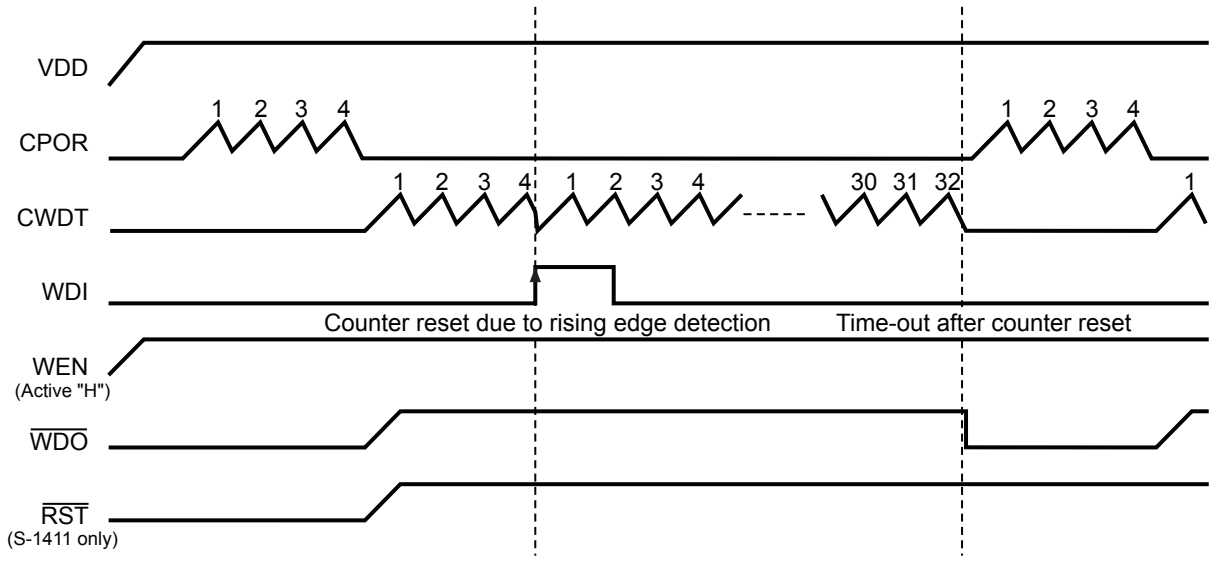


Figure 27

4. 2 Counter reset due to falling edge detection (S-141xBxx, S-141xExx, S-141xHxx, S-141xKxx)

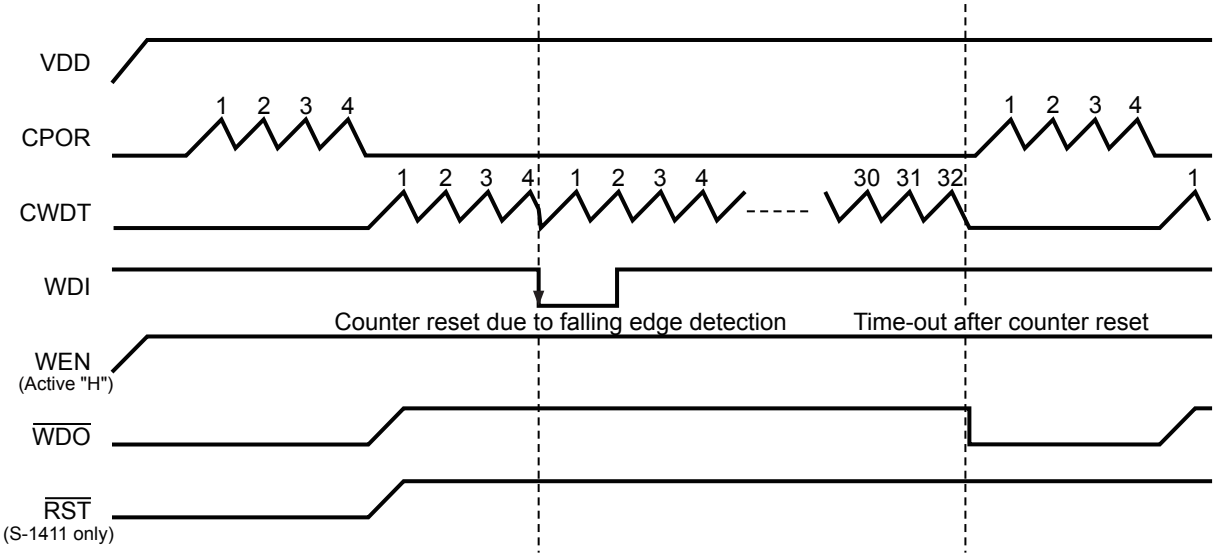


Figure 28

4. 3 Counter reset due to both rising and falling edges detection 1 (S-141xCxx, S-141xFxx, S-141xIxx, S-141xLxx)

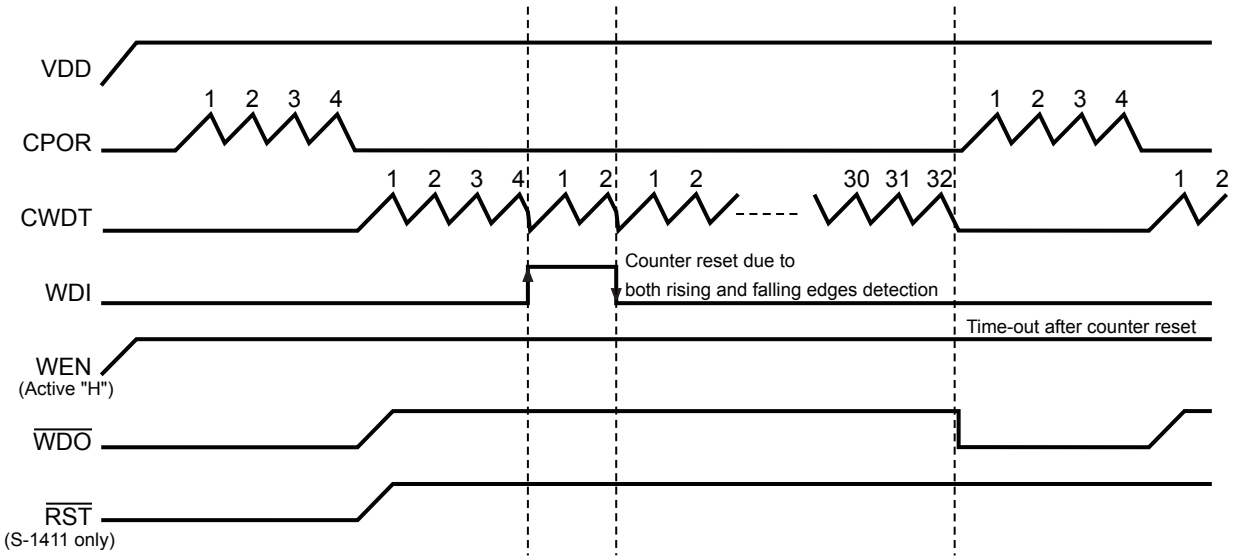


Figure 29

4. 4 Counter reset due to both rising and falling edges detection 2 (S-141xCxx, S-141xFxx, S-141xIxx, S-141xLxx)

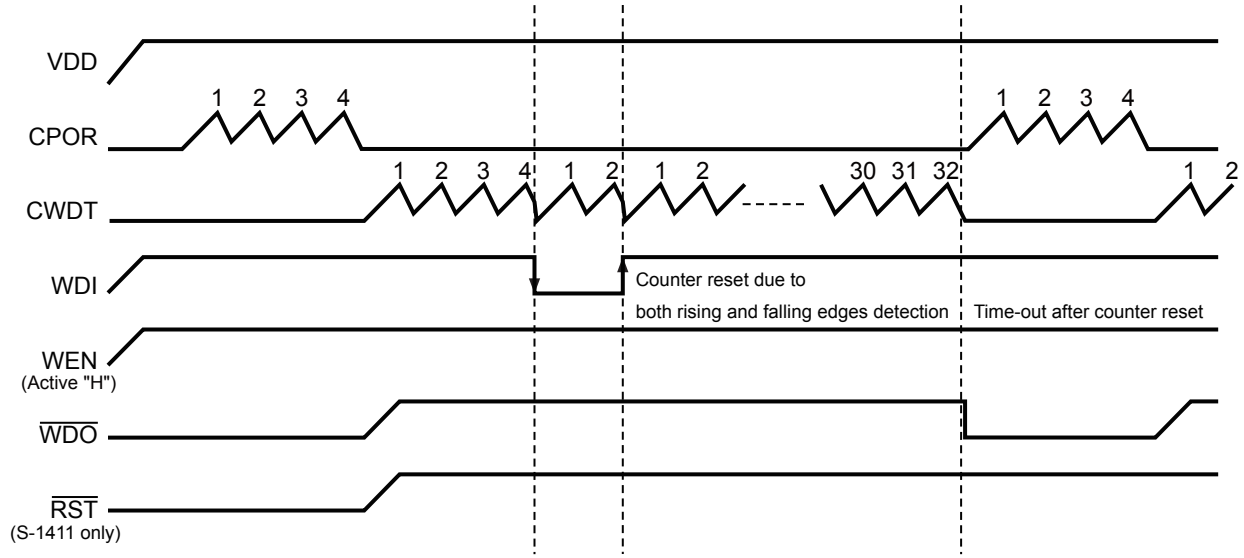


Figure 30

5. WEN pin operation during charge-discharge operation to CWDT pin

When the WEN pin changes from "H" to "L" during the charge-discharge operation to the CWDT pin, the CWDT pin performs the discharge operation. Moreover, the internal counter which counts the number of times of the charge-discharge operation for the CWDT pin is also reset.
If the WEN pin changes to "H" again in this status, the CWDT pin initiates the charge-discharge operation.

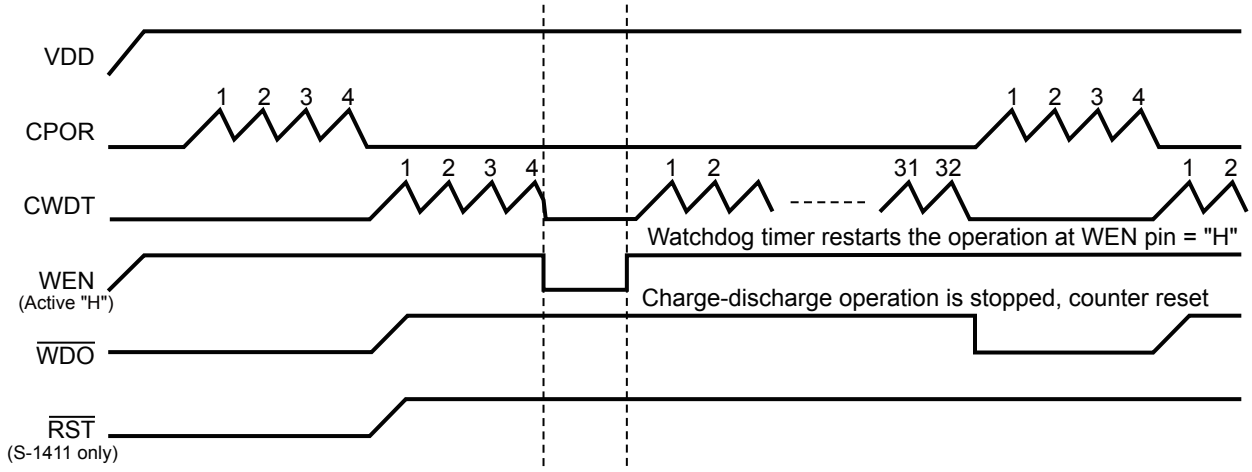


Figure 31

6. Watchdog double pulse detection

If an edge is input to the WDI pin again within a specific period of time (the discharge time due to an edge detection + 1 charge-discharge time (t_{WDL})) after inputting an edge to the WDI pin when the S-1410/1411 Series is the window mode, the $\overline{WDO}$ pin output changes from "H" to "L".
When the watchdog timer becomes Disable due to a change of the WEN pin ("H" → "L" → "H") after inputting an edge to the WDI pin, the $\overline{WDO}$ pin continues outputting "H" even if an edge is input to the WDI pin within the specific period of time mentioned above.

6. 1 Double pulse detection due to rising edge detection (S-141xAxx, S-141xDxx, S-141xGxx, S-141xJxx)

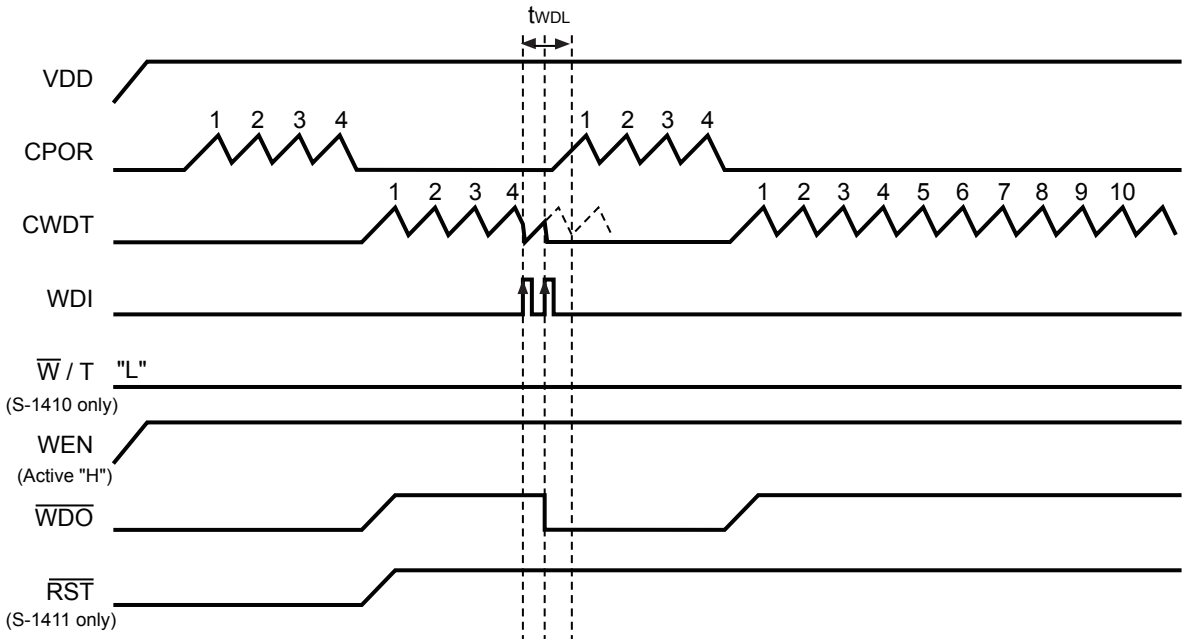


Figure 32

6. 2 Double pulse detection due to falling edge detection (S-141xBxx, S-141xExx, S-141xHxx, S-141xKxx)

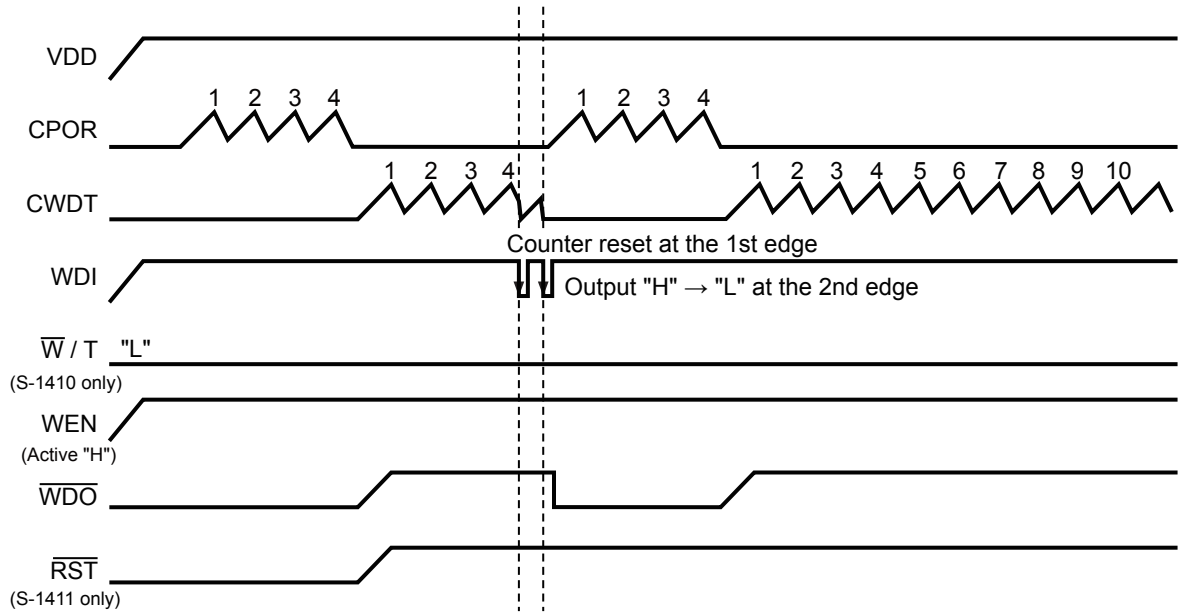


Figure 33

6. 3 Double pulse detection due to both rising and falling edges detection (S-141xCxx, S-141xFxx, S-141xIxx, S-141xLxx)

The double pulse is detected only when edges are input in order of rising and falling.

6. 3. 1 When edges are input to WDI pin in order of rising and falling

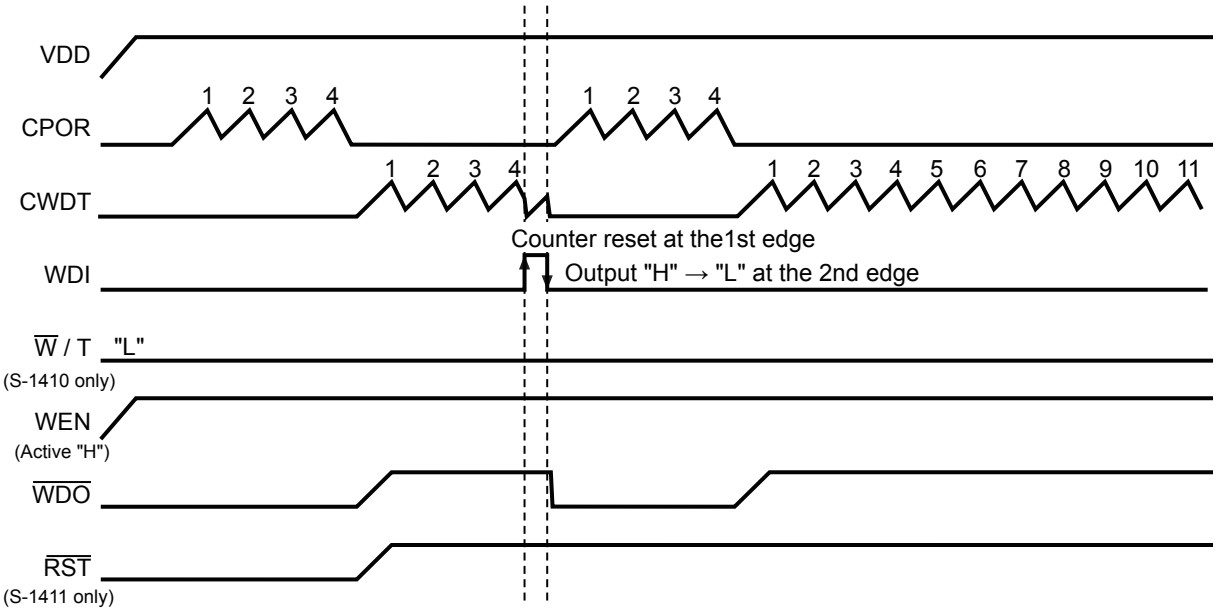


Figure 34 Double Pulse Detection

6. 3. 2 When edges are input to WDI pin in order of falling and rising

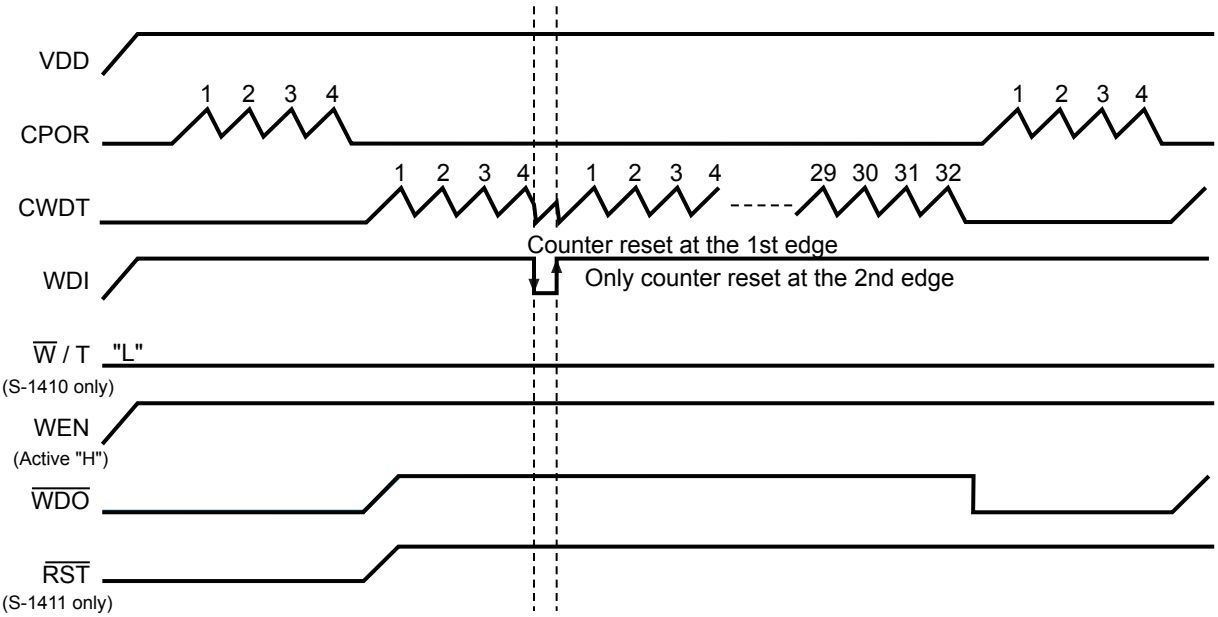


Figure 35 Double Pulse Non-detection

7. Operation of low voltage detection

The voltage detection circuit detects a low voltage if the power supply voltage falls below the detection voltage, and then "L" is output from the $\overline{\text{WDO}}$ pin and the $\overline{\text{RST}}$ pin (Only the S-1411 Series). The output is maintained until the charge-discharge operation of the CPOR pin is performed 4 times.
The S-1410/1411 Series can detect a low voltage even if either the CPOR pin or the WDT pin performs the charge-discharge operation. In this case, the status of the WEN pin or the $\overline{\text{W}}$ / T pin does not have an affect.

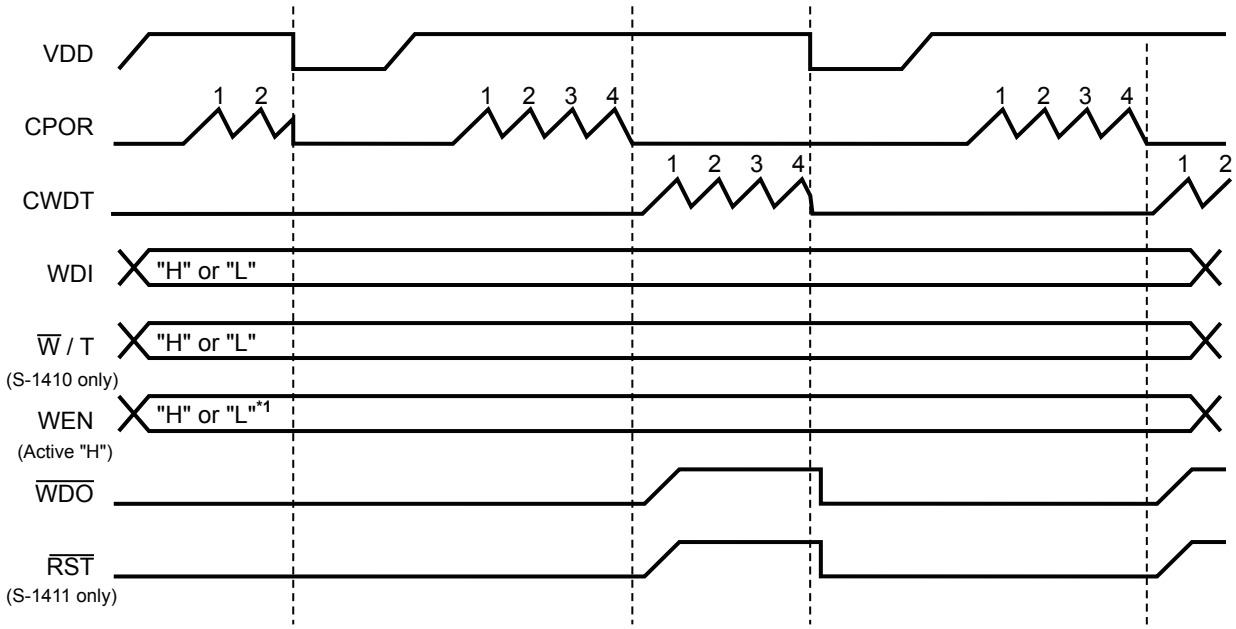


Figure 36

***1.** When the WEN pin is Disable, the charge-discharge operation of CWDT pin is not performed.

8. WEN pin, WDI pin and $\overline{\text{W}}$ / T pin

Each of the WEN pin, the WDI pin and the $\overline{\text{W}}$ / T pin has a noise filter.
If the power supply voltage is 5.0 V, noise with a minimum pulse width of 200 ns can be eliminated.

■ Standard Circuits

1. S-1410 Series (Product with $\overline{W}$ / T pin)

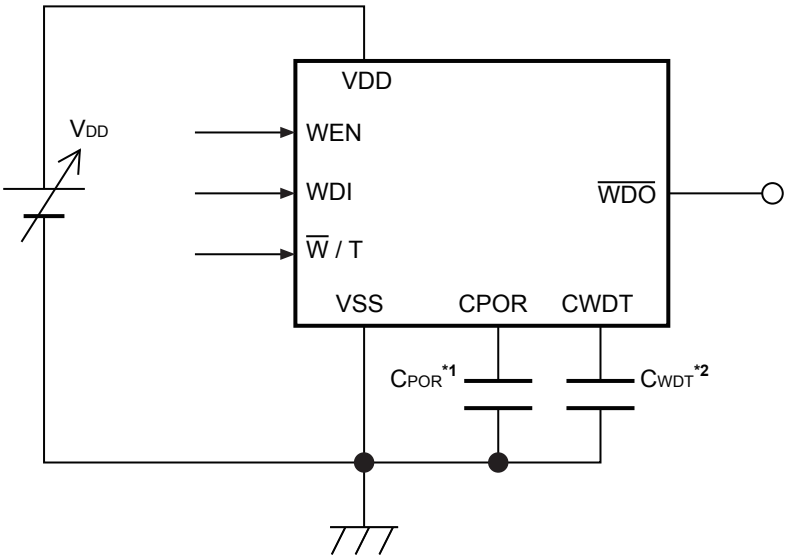


Figure 37

2. S-1411 Series (Product without $\overline{W}$ / T pin)

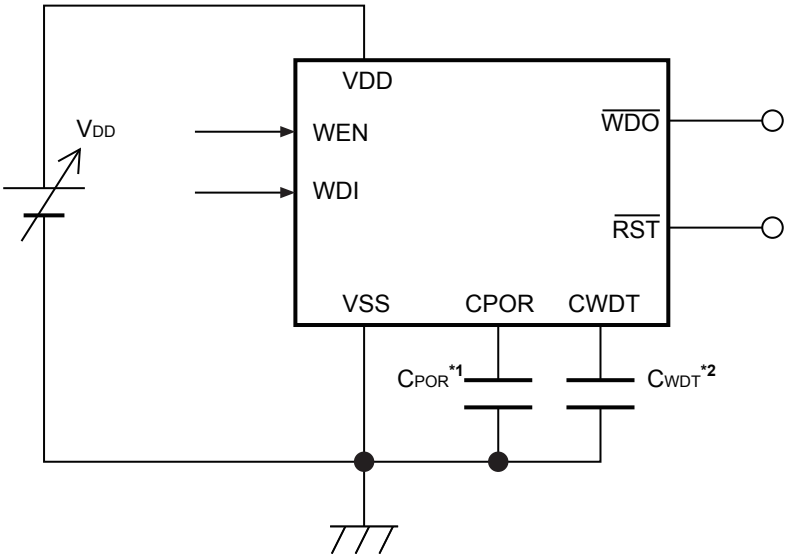


Figure 38

***1.** Adjustment capacitor for reset output delay time (C_{POR}) should be connected directly to the CPOR pin and the VSS pin.

***2.** Adjustment capacitor for watchdog output delay time (C_{WDT}) should be connected directly to the CWDT pin and the VSS pin.
A capacitor of 100 pF to 1 μF can be used for C_{POR} and C_{WDT}.

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Precautions

- It will take time for the discharge operation to be performed if the capacitance of C_{POR} is extremely large at the low voltage detection, so the discharge operation may not be completed by the time the power supply voltage exceeds the detection voltage. In that case, since the charge-discharge operation of the CPOR pin is performed after the discharge operation is completed, the delay time of the same time length as the discharge operation occurs in reset time-out period (t_{RST}).

- Select a capacitor which satisfies the following equation for C_{POR} and C_{WDT}. If this condition is not satisfied, the delay time of the same time length as the discharge operation occurs in t_{RST} since the discharge operation of an external capacitor connected to the CWDT pin is not completed by the time the CWDT pin initiates the next charge-discharge operation.

$$C_{WDT} / C_{POR} \leq 600$$

- When the power supply voltage falls to 0.9 V or lower, set a time interval of 20 μs or longer by the time the power supply is raised again. If the appropriate time length is not secured, the time-out period after raising the power supply voltage may get delayed.

- When the time that the power supply voltage falls below the detection voltage is short, the S-1410/1411 Series may not detect a voltage. In that case, the time-out period after raising the power supply voltage may get delayed.

- Since input pins (the WEN pin, the WDI pin and the $\overline{W}$ / T pin) in the S-1410/1411 Series are CMOS configurations, make sure that an intermediate potential is not input when the S-1410/1411 Series operates.

- Since the $\overline{WDO}$ pin and the $\overline{RST}$ pin are affected by external resistance and external capacitance, use the S-1410/1411 Series after performing thorough evaluation with the actual application.

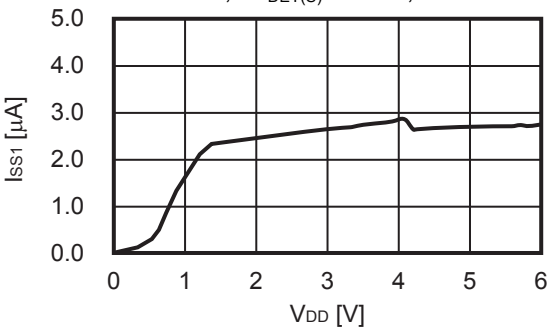
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

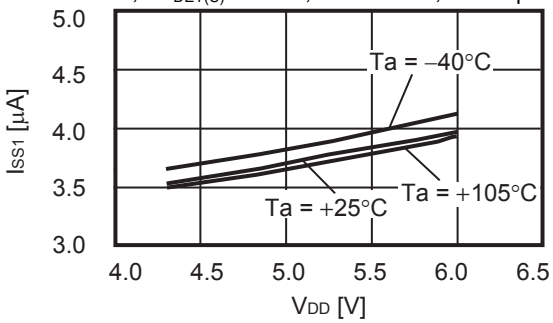
■ Characteristics (Typical Data)

1. Current consumption during operation (I_{SS1}) vs. Input voltage (V_{DD})

WDT = OFF, $-V_{DET(S)}$ = 4.0 V, Ta = +25°C

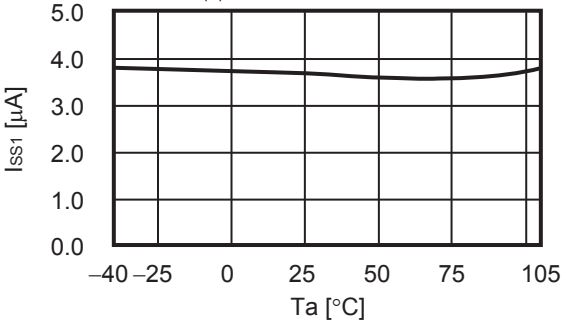


WDT = ON, $-V_{DET(S)}$ = 4.0 V, Ta = +25°C, WDI input



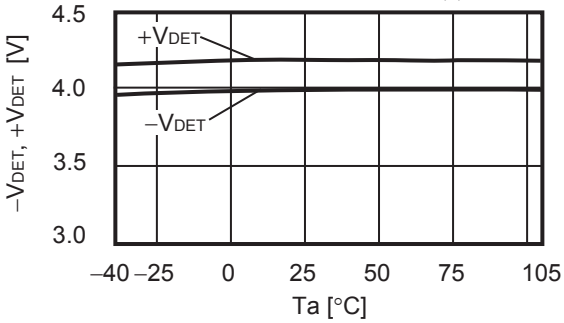
2. Current consumption during operation (I_{SS1}) vs. Temperature (Ta)

WDT = ON, $-V_{DET(S)}$ = 4.0 V, V_{DD} = 5.0 V, WDI input



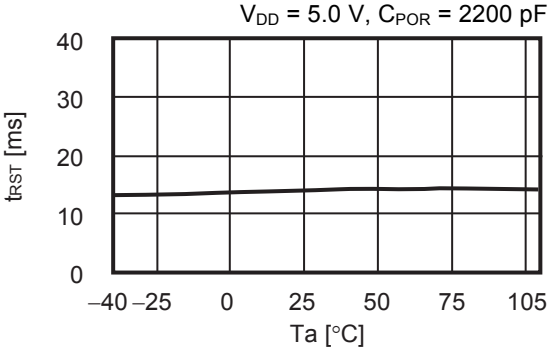
3. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Temperature (Ta)

$-V_{DET(S)}$ = 4.0 V



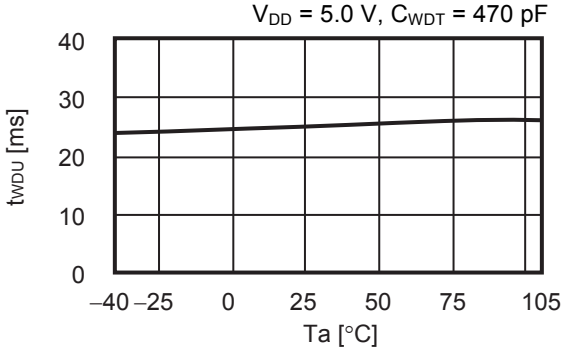
4. Reset time-out period (t_{RST}) vs. Temperature (Ta)

V_{DD} = 5.0 V, C_{POR} = 2200 pF



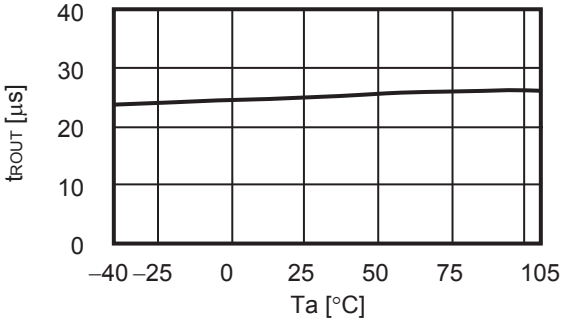
5. Watchdog time-out period (t_{WDU}) vs. Temperature (Ta)

V_{DD} = 5.0 V, C_{WDT} = 470 pF



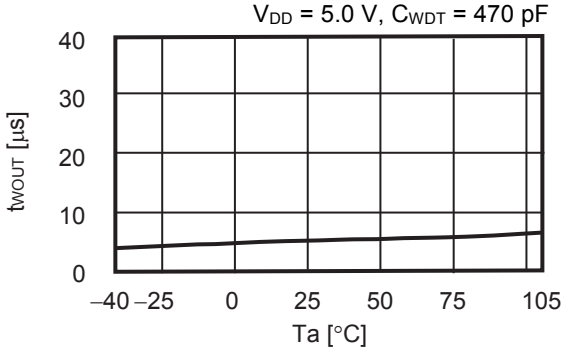
6. Reset output delay time (t_{ROUT}) vs. Temperature (Ta)

V_{DD} = $-V_{DET(S)}$ + 1.0 V → $-V_{DET(S)}$ − 1.0 V,
C_{POR} = 2200 pF

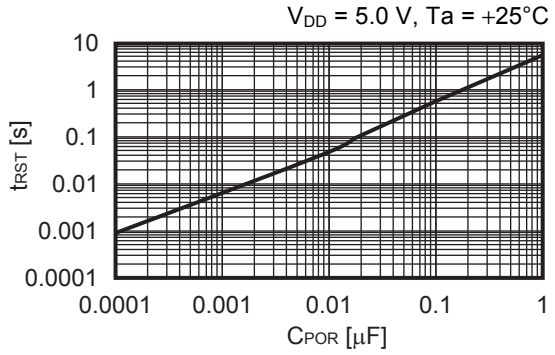


7. Watchdog output delay time (t_{WOUT}) vs. Temperature (Ta)

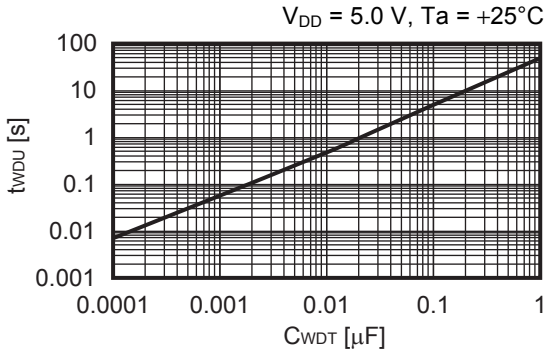
V_{DD} = 5.0 V, C_{WDT} = 470 pF



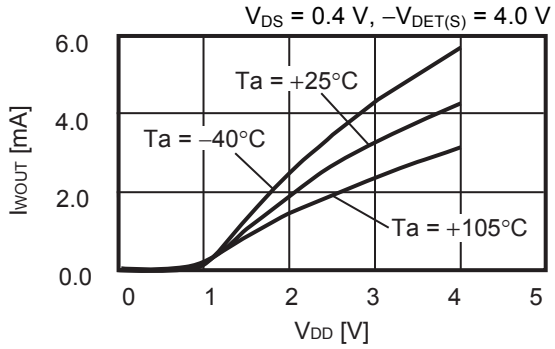
8. Reset time-out period (t_{RST}) vs. C_{POR}



9. Watchdog time-out period (t_{WDU}) vs. C_{WDT}



10. Nch driver output current (I_{WOUT}) vs. Input voltage (V_{DD})



■ Thermal Characteristics

1. TMSOP-8

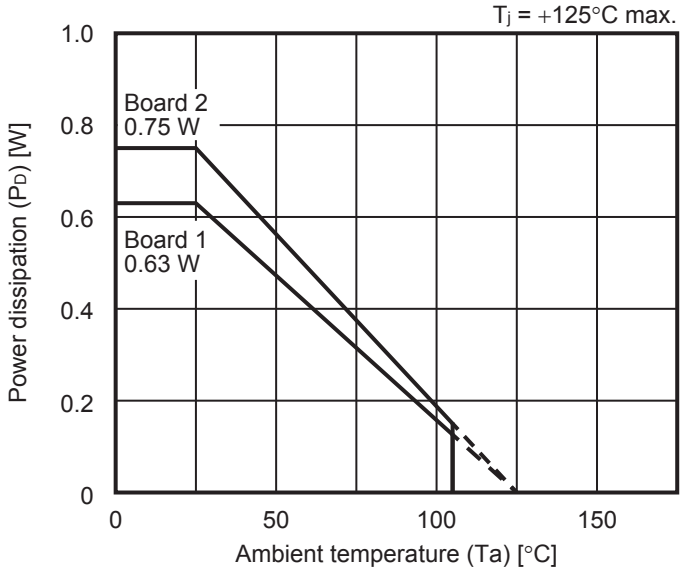


Figure 39 Power Dissipation of Package (When Mounted on Board)

1. 1 Board 1

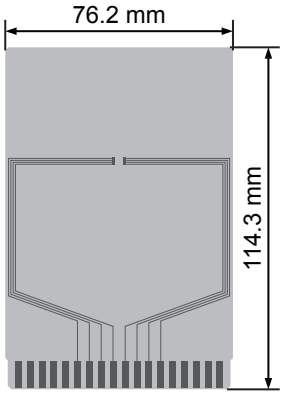


Figure 40

Table 8

Item		Specification
Thermal resistance value (θ_{ja})		160°C/W
Size		114.3 mm × 76.2 mm × t1.6 mm
Material		FR-4
Number of copper foil layer		2
Copper foil layer	1	Land pattern and wiring for testing: t0.070 mm
	2	–
	3	–
	4	74.2 mm × 74.2 mm × t0.070 mm
Thermal via		–

1. 2 Board 2

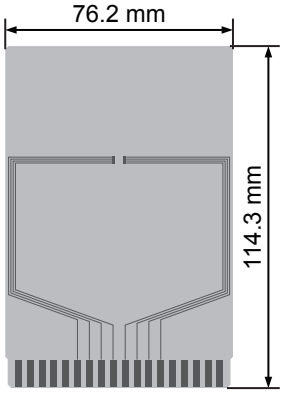
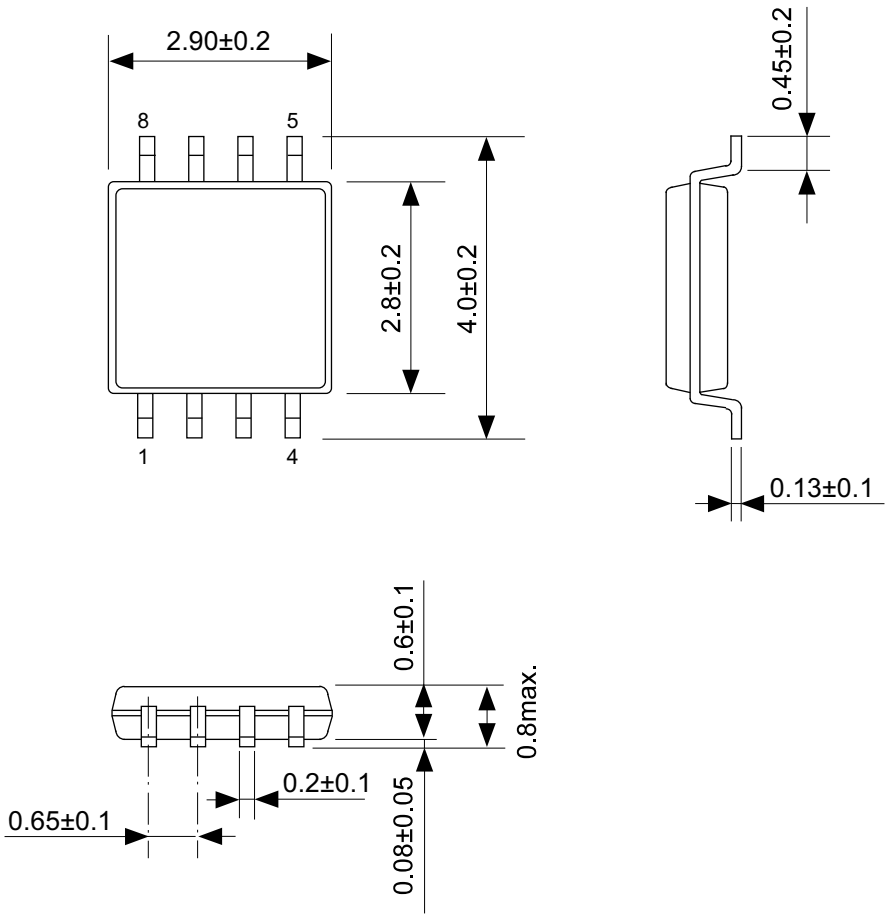


Figure 41

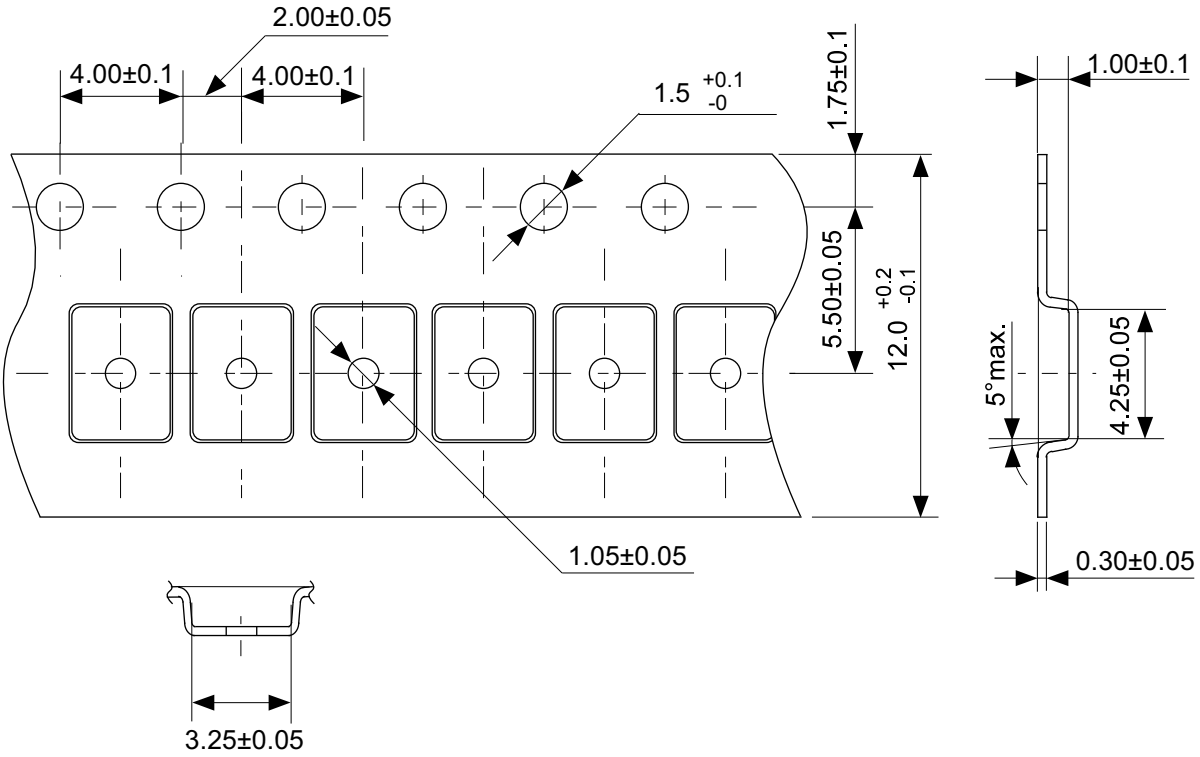
Table 9

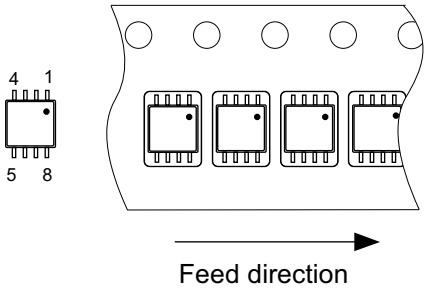
Item		Specification
Thermal resistance value (θ_{ja})		133°C/W
Size		114.3 mm × 76.2 mm × t1.6 mm
Material		FR-4
Number of copper foil layer		4
Copper foil layer	1	Land pattern and wiring for testing: t0.070 mm
	2	74.2 mm × 74.2 mm × t0.035 mm
	3	74.2 mm × 74.2 mm × t0.035 mm
	4	74.2 mm × 74.2 mm × t0.070 mm
Thermal via		–



No. FM008-A-P-SD-1.1

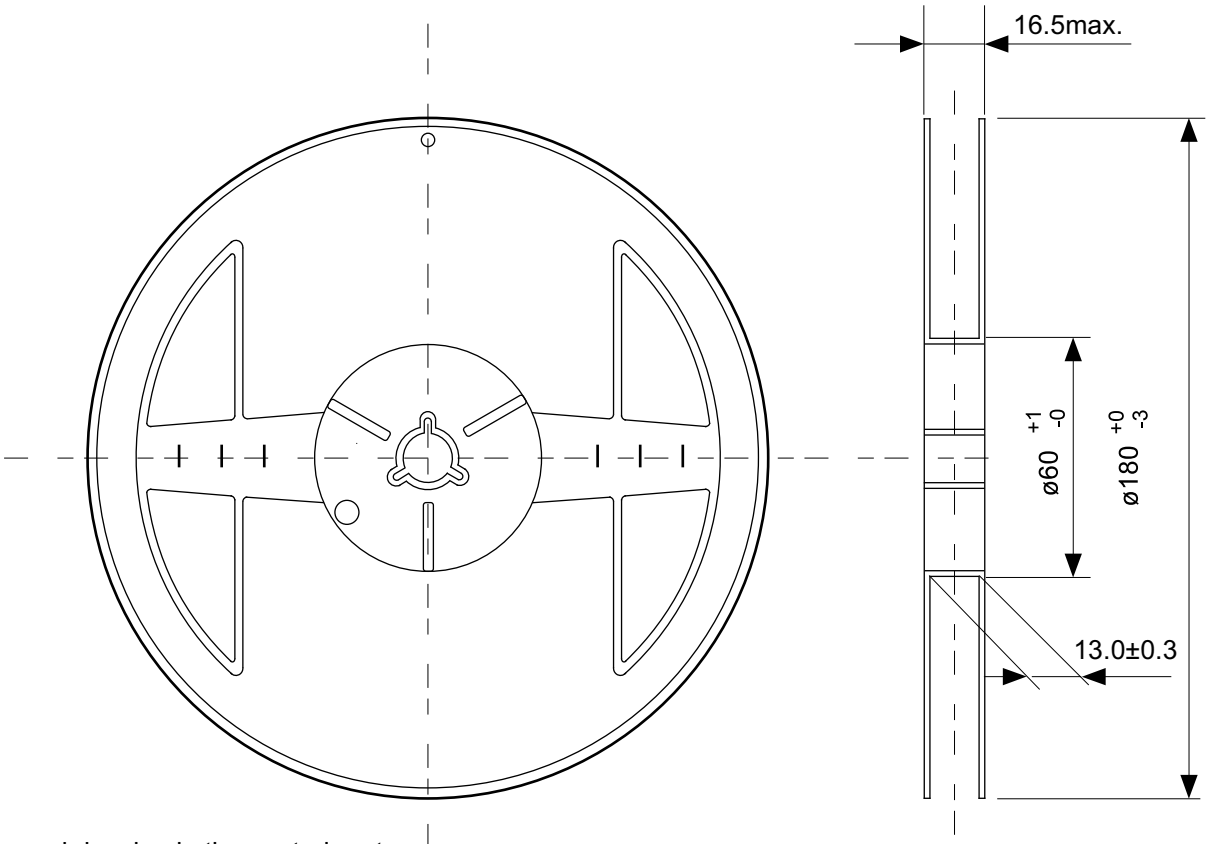
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



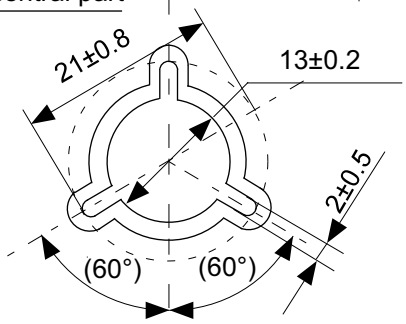


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
SCALE		QTY.	4,000
UNIT	mm		
	Seiko Instruments Inc.		

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