S-19104/19106 Series

FOR AUTOMOTIVE 105°C OPERATION BUILT-IN DELAY CIRCUIT (EXTERNAL DELAY TIME SETTING) VOLTAGE DETECTOR WITH SENSE PIN

www.sii-ic.com

Rev.1.0_00

The S-19104/19106 Series is a high-accuracy voltage detector developed using CMOS technology. The detection voltage is fixed internally with an accuracy of ±3.5% ($-V_{DET(S)} \geq 2.2$ V). It operates with current consumption of 500 nA typ.
Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared, so the output is stable even if the SENSE pin falls to 0 V.
The release signal can be delayed by setting a capacitor externally, and the release delay time accuracy is ±34% (C_D = 4.7 nF, Ta = –40°C to +105°C).
Two output forms Nch open-drain output and CMOS output are available.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to SII is indispensable.

■ Features

- Detection voltage: 1.2 V to 5.0 V (0.1 V step)
- Detection voltage accuracy: ±3.5% (2.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V, Ta = –40°C to +105°C)
  ±(2.5% + 22 mV) (1.2 V ≤ $-V_{DET(S)}$ < 2.2 V, Ta = –40°C to +105°C)
- Current consumption: 500 nA typ.
- Operation voltage range: 0.95 V to 10.0 V
- Hysteresis width: 5% ± 2% (Ta = –40°C to +105°C)
- Release delay time accuracy: ±34% (C_D = 4.7 nF, Ta = –40°C to +105°C)
- Output form: Nch open-drain output (Active "L")
  CMOS output (Active "L")
- Operation temperature range: Ta = –40°C to +105°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 in process*1

***1.** Contact our sales office for details.

■ Applications

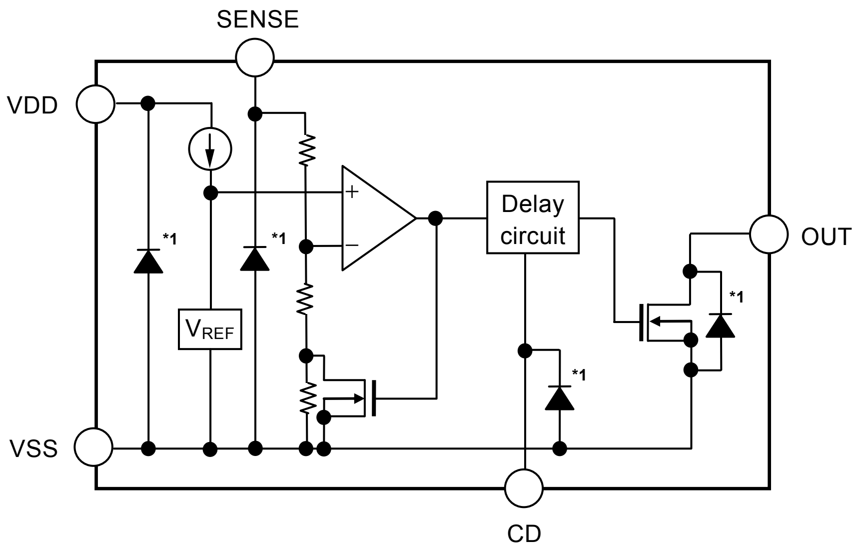
- For automotive use (accessory, car navigation system, car audio system, etc.)

■ Package

- SOT-23-5

■ Block Diagrams

1. S-19104/19106 Series N type (Nch open-drain output)

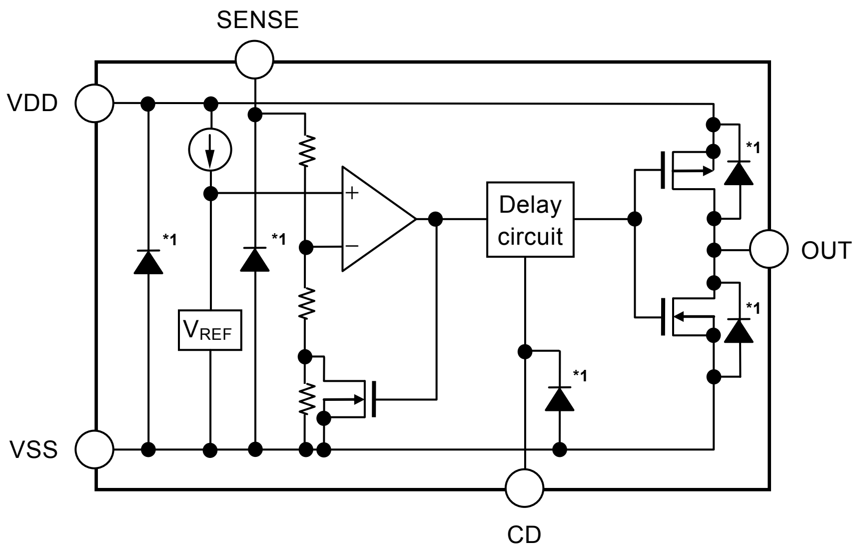


Function	Status
Output logic	Active "L"

***1.** Parasitic diode

Figure 1

2. S-19104/19106 Series C type (CMOS output)



Function	Status
Output logic	Active "L"

***1.** Parasitic diode

Figure 2

■ AEC-Q100 in Process

Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

Users can select the output form and detection voltage value for the S-19104/19106 Series.
Refer to "**1. Product name**" regarding the contents of product name, "**2. Function list of product types**" regarding the product types, "**3. Package**" regarding the package drawings and "**4. Product name list**" regarding details of product name.

1. Product name

S-1910 x x xx H - M5T1 U

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- M5T1: Package abbreviation and IC packing specifications*1
  - M5T1: SOT-23-5, Tape
- H: Operation temperature
  - H: Ta = –40°C to +105°C
- xx: Detection voltage value
  - 12 to 50
  - (e.g., when the detection voltage is 1.2 V, it is expressed as 12.)
- x: Output form*2
  - N: Nch open-drain output (Active "L")*3
  - C: CMOS output (Active "L")*3
- x: Pin configuration*4
  - 4, 6

***1.** Refer to the tape drawing.
***2.** Refer to "**2. Function list of product types**".
***3.** If you request the product with output logic active "H", contact our sales office.
***4.** Refer to "**■ Pin Configurations**".

2. Function list of product types

Table 1

Product Type	Output Form	Output Logic	Package
N	Nch open-drain output	Active "L"	SOT-23-5
C	CMOS output	Active "L"	SOT-23-5

3. Package

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD

4. Product name list

4. 1 S-19104 Series N type

Output form: Nch open-drain output (Active "L")

Table 3

Detection Voltage	SOT-23-5
1.2 V ± (2.5% + 22 mV)	S-19104N12H-M5T1U
1.3 V ± (2.5% + 22 mV)	S-19104N13H-M5T1U
1.4 V ± (2.5% + 22 mV)	S-19104N14H-M5T1U
1.5 V ± (2.5% + 22 mV)	S-19104N15H-M5T1U
1.6 V ± (2.5% + 22 mV)	S-19104N16H-M5T1U
1.7 V ± (2.5% + 22 mV)	S-19104N17H-M5T1U
1.8 V ± (2.5% + 22 mV)	S-19104N18H-M5T1U
1.9 V ± (2.5% + 22 mV)	S-19104N19H-M5T1U
2.0 V ± (2.5% + 22 mV)	S-19104N20H-M5T1U
2.1 V ± (2.5% + 22 mV)	S-19104N21H-M5T1U
2.2 V ± 3.5%	S-19104N22H-M5T1U
2.3 V ± 3.5%	S-19104N23H-M5T1U
2.4 V ± 3.5%	S-19104N24H-M5T1U
2.5 V ± 3.5%	S-19104N25H-M5T1U
2.6 V ± 3.5%	S-19104N26H-M5T1U
2.7 V ± 3.5%	S-19104N27H-M5T1U
2.8 V ± 3.5%	S-19104N28H-M5T1U
2.9 V ± 3.5%	S-19104N29H-M5T1U
3.0 V ± 3.5%	S-19104N30H-M5T1U
3.1 V ± 3.5%	S-19104N31H-M5T1U
3.2 V ± 3.5%	S-19104N32H-M5T1U
3.3 V ± 3.5%	S-19104N33H-M5T1U
3.4 V ± 3.5%	S-19104N34H-M5T1U
3.5 V ± 3.5%	S-19104N35H-M5T1U
3.6 V ± 3.5%	S-19104N36H-M5T1U
3.7 V ± 3.5%	S-19104N37H-M5T1U
3.8 V ± 3.5%	S-19104N38H-M5T1U
3.9 V ± 3.5%	S-19104N39H-M5T1U
4.0 V ± 3.5%	S-19104N40H-M5T1U
4.1 V ± 3.5%	S-19104N41H-M5T1U
4.2 V ± 3.5%	S-19104N42H-M5T1U
4.3 V ± 3.5%	S-19104N43H-M5T1U
4.4 V ± 3.5%	S-19104N44H-M5T1U
4.5 V ± 3.5%	S-19104N45H-M5T1U
4.6 V ± 3.5%	S-19104N46H-M5T1U
4.7 V ± 3.5%	S-19104N47H-M5T1U
4.8 V ± 3.5%	S-19104N48H-M5T1U
4.9 V ± 3.5%	S-19104N49H-M5T1U
5.0 V ± 3.5%	S-19104N50H-M5T1U

4. 2 S-19104 Series C type

Output form: CMOS output (Active "L")

Table 4

Detection Voltage	SOT-23-5
1.2 V ± (2.5% + 22 mV)	S-19104C12H-M5T1U
1.3 V ± (2.5% + 22 mV)	S-19104C13H-M5T1U
1.4 V ± (2.5% + 22 mV)	S-19104C14H-M5T1U
1.5 V ± (2.5% + 22 mV)	S-19104C15H-M5T1U
1.6 V ± (2.5% + 22 mV)	S-19104C16H-M5T1U
1.7 V ± (2.5% + 22 mV)	S-19104C17H-M5T1U
1.8 V ± (2.5% + 22 mV)	S-19104C18H-M5T1U
1.9 V ± (2.5% + 22 mV)	S-19104C19H-M5T1U
2.0 V ± (2.5% + 22 mV)	S-19104C20H-M5T1U
2.1 V ± (2.5% + 22 mV)	S-19104C21H-M5T1U
2.2 V ± 3.5%	S-19104C22H-M5T1U
2.3 V ± 3.5%	S-19104C23H-M5T1U
2.4 V ± 3.5%	S-19104C24H-M5T1U
2.5 V ± 3.5%	S-19104C25H-M5T1U
2.6 V ± 3.5%	S-19104C26H-M5T1U
2.7 V ± 3.5%	S-19104C27H-M5T1U
2.8 V ± 3.5%	S-19104C28H-M5T1U
2.9 V ± 3.5%	S-19104C29H-M5T1U
3.0 V ± 3.5%	S-19104C30H-M5T1U
3.1 V ± 3.5%	S-19104C31H-M5T1U
3.2 V ± 3.5%	S-19104C32H-M5T1U
3.3 V ± 3.5%	S-19104C33H-M5T1U
3.4 V ± 3.5%	S-19104C34H-M5T1U
3.5 V ± 3.5%	S-19104C35H-M5T1U
3.6 V ± 3.5%	S-19104C36H-M5T1U
3.7 V ± 3.5%	S-19104C37H-M5T1U
3.8 V ± 3.5%	S-19104C38H-M5T1U
3.9 V ± 3.5%	S-19104C39H-M5T1U
4.0 V ± 3.5%	S-19104C40H-M5T1U
4.1 V ± 3.5%	S-19104C41H-M5T1U
4.2 V ± 3.5%	S-19104C42H-M5T1U
4.3 V ± 3.5%	S-19104C43H-M5T1U
4.4 V ± 3.5%	S-19104C44H-M5T1U
4.5 V ± 3.5%	S-19104C45H-M5T1U
4.6 V ± 3.5%	S-19104C46H-M5T1U
4.7 V ± 3.5%	S-19104C47H-M5T1U
4.8 V ± 3.5%	S-19104C48H-M5T1U
4.9 V ± 3.5%	S-19104C49H-M5T1U
5.0 V ± 3.5%	S-19104C50H-M5T1U

4. 3 S-19106 Series N type

Output form: Nch open-drain output (Active "L")

Table 5

Detection Voltage	SOT-23-5
1.2 V ± (2.5% + 22 mV)	S-19106N12H-M5T1U
1.3 V ± (2.5% + 22 mV)	S-19106N13H-M5T1U
1.4 V ± (2.5% + 22 mV)	S-19106N14H-M5T1U
1.5 V ± (2.5% + 22 mV)	S-19106N15H-M5T1U
1.6 V ± (2.5% + 22 mV)	S-19106N16H-M5T1U
1.7 V ± (2.5% + 22 mV)	S-19106N17H-M5T1U
1.8 V ± (2.5% + 22 mV)	S-19106N18H-M5T1U
1.9 V ± (2.5% + 22 mV)	S-19106N19H-M5T1U
2.0 V ± (2.5% + 22 mV)	S-19106N20H-M5T1U
2.1 V ± (2.5% + 22 mV)	S-19106N21H-M5T1U
2.2 V ± 3.5%	S-19106N22H-M5T1U
2.3 V ± 3.5%	S-19106N23H-M5T1U
2.4 V ± 3.5%	S-19106N24H-M5T1U
2.5 V ± 3.5%	S-19106N25H-M5T1U
2.6 V ± 3.5%	S-19106N26H-M5T1U
2.7 V ± 3.5%	S-19106N27H-M5T1U
2.8 V ± 3.5%	S-19106N28H-M5T1U
2.9 V ± 3.5%	S-19106N29H-M5T1U
3.0 V ± 3.5%	S-19106N30H-M5T1U
3.1 V ± 3.5%	S-19106N31H-M5T1U
3.2 V ± 3.5%	S-19106N32H-M5T1U
3.3 V ± 3.5%	S-19106N33H-M5T1U
3.4 V ± 3.5%	S-19106N34H-M5T1U
3.5 V ± 3.5%	S-19106N35H-M5T1U
3.6 V ± 3.5%	S-19106N36H-M5T1U
3.7 V ± 3.5%	S-19106N37H-M5T1U
3.8 V ± 3.5%	S-19106N38H-M5T1U
3.9 V ± 3.5%	S-19106N39H-M5T1U
4.0 V ± 3.5%	S-19106N40H-M5T1U
4.1 V ± 3.5%	S-19106N41H-M5T1U
4.2 V ± 3.5%	S-19106N42H-M5T1U
4.3 V ± 3.5%	S-19106N43H-M5T1U
4.4 V ± 3.5%	S-19106N44H-M5T1U
4.5 V ± 3.5%	S-19106N45H-M5T1U
4.6 V ± 3.5%	S-19106N46H-M5T1U
4.7 V ± 3.5%	S-19106N47H-M5T1U
4.8 V ± 3.5%	S-19106N48H-M5T1U
4.9 V ± 3.5%	S-19106N49H-M5T1U
5.0 V ± 3.5%	S-19106N50H-M5T1U

4. 4 S-19106 Series C type

Output form: CMOS output (Active "L")

Table 6

Detection Voltage	SOT-23-5
1.2 V ± (2.5% + 22 mV)	S-19106C12H-M5T1U
1.3 V ± (2.5% + 22 mV)	S-19106C13H-M5T1U
1.4 V ± (2.5% + 22 mV)	S-19106C14H-M5T1U
1.5 V ± (2.5% + 22 mV)	S-19106C15H-M5T1U
1.6 V ± (2.5% + 22 mV)	S-19106C16H-M5T1U
1.7 V ± (2.5% + 22 mV)	S-19106C17H-M5T1U
1.8 V ± (2.5% + 22 mV)	S-19106C18H-M5T1U
1.9 V ± (2.5% + 22 mV)	S-19106C19H-M5T1U
2.0 V ± (2.5% + 22 mV)	S-19106C20H-M5T1U
2.1 V ± (2.5% + 22 mV)	S-19106C21H-M5T1U
2.2 V ± 3.5%	S-19106C22H-M5T1U
2.3 V ± 3.5%	S-19106C23H-M5T1U
2.4 V ± 3.5%	S-19106C24H-M5T1U
2.5 V ± 3.5%	S-19106C25H-M5T1U
2.6 V ± 3.5%	S-19106C26H-M5T1U
2.7 V ± 3.5%	S-19106C27H-M5T1U
2.8 V ± 3.5%	S-19106C28H-M5T1U
2.9 V ± 3.5%	S-19106C29H-M5T1U
3.0 V ± 3.5%	S-19106C30H-M5T1U
3.1 V ± 3.5%	S-19106C31H-M5T1U
3.2 V ± 3.5%	S-19106C32H-M5T1U
3.3 V ± 3.5%	S-19106C33H-M5T1U
3.4 V ± 3.5%	S-19106C34H-M5T1U
3.5 V ± 3.5%	S-19106C35H-M5T1U
3.6 V ± 3.5%	S-19106C36H-M5T1U
3.7 V ± 3.5%	S-19106C37H-M5T1U
3.8 V ± 3.5%	S-19106C38H-M5T1U
3.9 V ± 3.5%	S-19106C39H-M5T1U
4.0 V ± 3.5%	S-19106C40H-M5T1U
4.1 V ± 3.5%	S-19106C41H-M5T1U
4.2 V ± 3.5%	S-19106C42H-M5T1U
4.3 V ± 3.5%	S-19106C43H-M5T1U
4.4 V ± 3.5%	S-19106C44H-M5T1U
4.5 V ± 3.5%	S-19106C45H-M5T1U
4.6 V ± 3.5%	S-19106C46H-M5T1U
4.7 V ± 3.5%	S-19106C47H-M5T1U
4.8 V ± 3.5%	S-19106C48H-M5T1U
4.9 V ± 3.5%	S-19106C49H-M5T1U
5.0 V ± 3.5%	S-19106C50H-M5T1U

■ Pin Configurations

1. S-19104 Series

1. 1 SOT-23-5

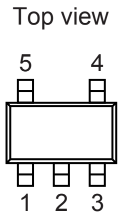


Figure 3

Table 7

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Power supply pin
3	VSS	GND pin
4	CD	Connection pin for delay capacitor
5	SENSE	Detection voltage input pin

2. S-19106 Series

2. 1 SOT-23-5

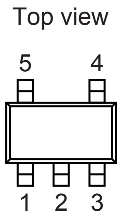


Figure 4

Table 8

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VSS	GND pin
3	VDD	Power supply pin
4	SENSE	Detection voltage input pin
5	CD	Connection pin for delay capacitor

■ Absolute Maximum Ratings

Table 9

(Ta = –40°C to +105°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		$V_{DD} - V_{SS}$	12.0	V
SENSE pin input voltage		V_{SENSE}	V_{SS} – 0.3 to 12.0	V
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} – 0.3 to 12.0	V
	CMOS output product		V_{SS} – 0.3 to V_{DD} + 0.3	V
Output current		I_{OUT}	50	mA
Power dissipation		P_D	600*1	mW
Operation ambient temperature		T_{opr}	–40 to +105	°C
Storage temperature		T_{stg}	–40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

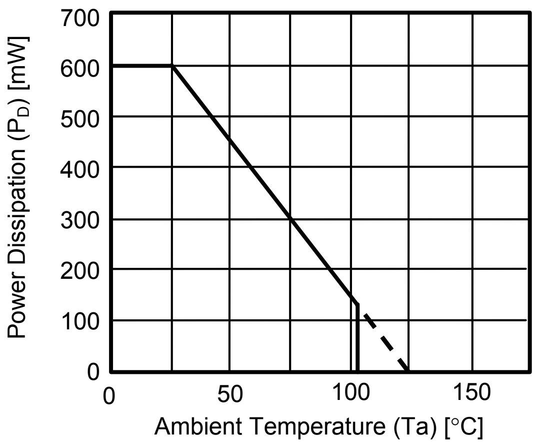


Figure 5 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Nch open-drain output product

Table 10

(Ta = –40°C to +105°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage[*1]	$-V_{DET}$	$0.95\ V \le V_{DD} \le 10.0\ V$	$1.2\ V \le -V_{DET(S)} < 2.2\ V$	$-V_{DET(S)} \times 0.975 - 0.022$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025 + 0.022$	V	1
			$2.2\ V \le -V_{DET(S)} \le 5.0\ V$	$-V_{DET(S)} \times 0.965$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.035$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	1
Current consumption[*2]	I_{SS}	V_{DD} = 10.0 V, $V_{SENSE} = -V_{DET(S)} + 1.0$ V		–	0.50	0.90	μA	2
Operation voltage	V_{DD}	–		0.95	–	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}[*3] = 0.5 V V_{SENSE} = 0.0 V	V_{DD} = 0.95 V	0.50	1.00	–	mA	3
			V_{DD} = 1.2 V	0.73	1.33	–	mA	3
			V_{DD} = 2.4 V	1.17	2.39	–	mA	3
			V_{DD} = 4.8 V	1.49	2.50	–	mA	3
Leakage current	I_{LEAK}	Output transistor Nch V_{DD} = 10.0 V, V_{DS}[*3] = 10.0 V, V_{SENSE} = 10.0 V		–	–	1.2	μA	3
Detection delay time[*4]	t_{DET}	V_{DD} = 5.0 V		–	40	–	μs	4
Release delay time[*5]	t_{RESET}	$V_{DD} = -V_{DET(S)} + 1.0$ V, C_D = 4.7 nF		8.38	12.69	17.00	ms	4
SENSE pin resistance	R_{SENSE}	–		4.0	30.0	189.0	MΩ	2

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 3** or **Table 5**)

***2.** The current flowing through the SENSE pin resistance is not included.

***3.** V_{DS}: Drain-to-source voltage of the output transistor

***4.** The time period from when the pulse voltage of 6.0 V → $-V_{DET(S)}$ – 2.0 V or 0 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} / 2, after the output pin is pulled up to 5 V by the resistance of 470 kΩ.

***5.** The time period from when the pulse voltage of 0.95 V → 10.0 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} × 90%, after the output pin is pulled up to V_{DD} by the resistance of 100 kΩ.

2. CMOS output product

Table 11

(Ta = −40°C to +105°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage[*1]	$-V_{DET}$	$0.95\ V \le V_{DD} \le 10.0\ V$	$1.2\ V \le -V_{DET(S)} < 2.2\ V$	$-V_{DET(S)} \times 0.975 - 0.022$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025 + 0.022$	V	1
			$2.2\ V \le -V_{DET(S)} \le 5.0\ V$	$-V_{DET(S)} \times 0.965$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.035$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	1
Current consumption[*2]	I_{SS}	$V_{DD} = 10.0\ V$, $V_{SENSE} = -V_{DET(S)} + 1.0\ V$		–	0.50	2.10	μA	2
Operation voltage	V_{DD}	–		0.95	–	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}[*3] = 0.5 V V_{SENSE} = 0.0 V	$V_{DD} = 0.95\ V$	0.50	1.00	–	mA	3
			$V_{DD} = 1.2\ V$	0.73	1.33	–	mA	3
			$V_{DD} = 2.4\ V$	1.17	2.39	–	mA	3
			$V_{DD} = 4.8\ V$	1.49	2.50	–	mA	3
		Output transistor Pch V_{DS}[*3] = 0.5 V V_{SENSE} = 10.0 V	$V_{DD} = 4.8\ V$	1.62	2.60	–	mA	5
			$V_{DD} = 6.0\ V$	1.78	2.86	–	mA	5
Detection delay time[*4]	t_{DET}	$V_{DD} = 5.0\ V$		–	40	–	μs	4
Release delay time[*5]	t_{RESET}	$V_{DD} = -V_{DET(S)} + 1.0\ V$, $C_D = 4.7\ nF$		8.38	12.69	17.00	ms	4
SENSE pin resistance	R_{SENSE}	–		4.0	30.0	189.0	MΩ	2

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 4** or **Table 6**)

***2.** The current flowing through the SENSE pin resistance is not included.

***3.** V_{DS}: Drain-to-source voltage of the output transistor

***4.** The time period from when the pulse voltage of 6.0 V → $-V_{DET(S)}$ − 2.0 V or 0 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} / 2.

***5.** The time period from when the pulse voltage of 0.95 V → 10.0 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} × 90%.

■ Test Circuits

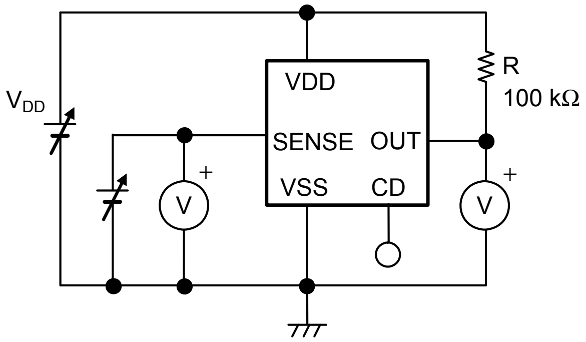


Figure 6 Test Circuit 1
(Nch open-drain output product)

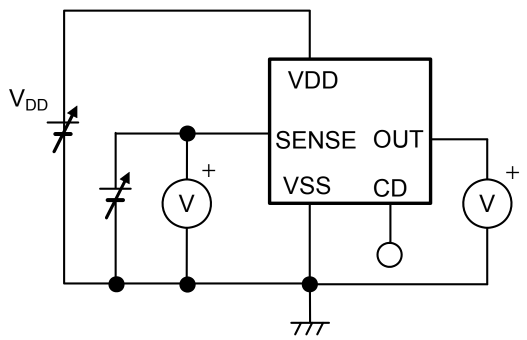


Figure 7 Test Circuit 1
(CMOS output product)

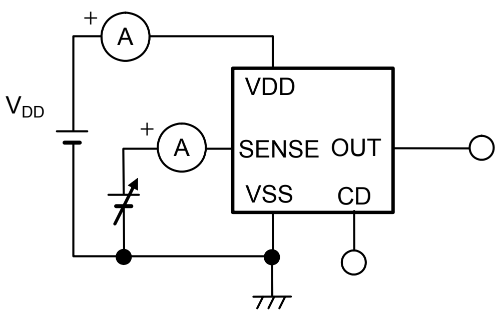


Figure 8 Test Circuit 2

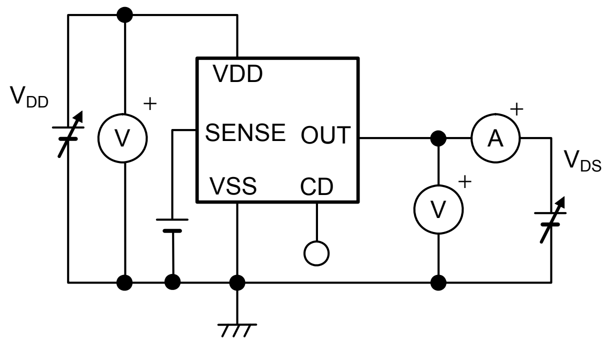


Figure 9 Test Circuit 3

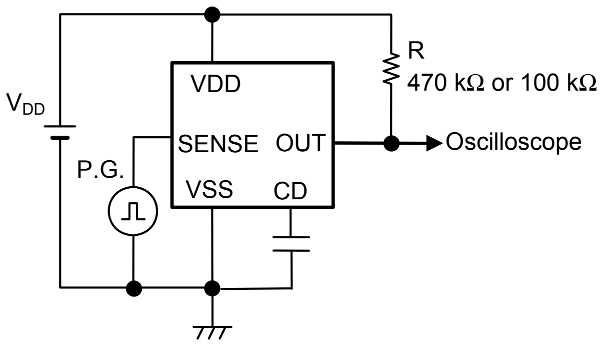


Figure 10 Test Circuit 4
(Nch open-drain output product)

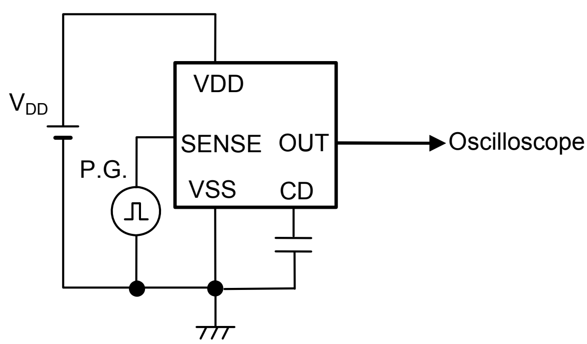


Figure 11 Test Circuit 4
(CMOS output product)

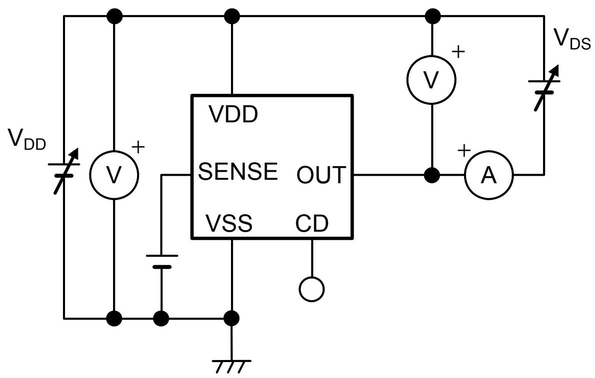
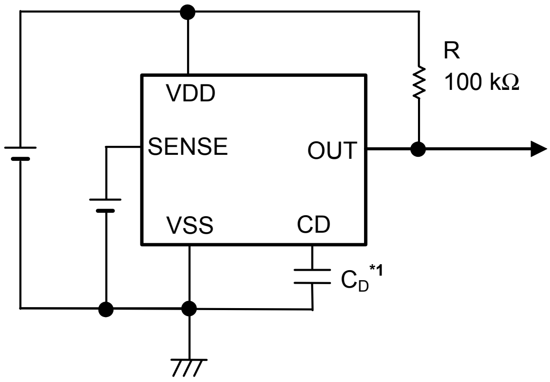


Figure 12 Test Circuit 5

■ Standard Circuits

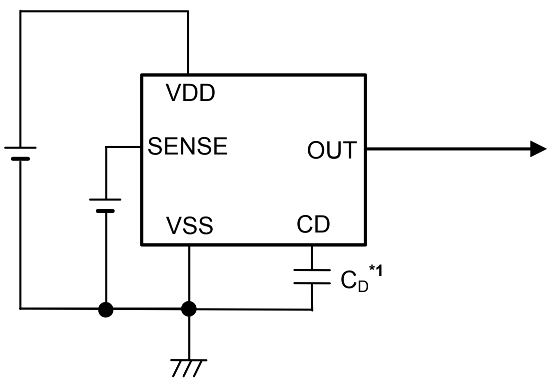
1. Nch open-drain output product



***1.** The delay capacitor (C_D) should be connected directly to the CD pin and the VSS pin.

Figure 13

2. CMOS output product



***1.** The delay capacitor (C_D) should be connected directly to the CD pin and the VSS pin.

Figure 14

Caution **The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

■ Explanation of Terms

1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 17** or **Figure 18** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (Refer to **Figure 15**).

Example: In the S-19104C18, the detection voltage is either one in the range of 1.733 V $\le -V_{DET} \le$ 1.867 V.
This means that some S-19104C18 have $-V_{DET}$ = 1.733 V and some have $-V_{DET}$ = 1.867 V.

2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 17** or **Figure 18** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (Refer to **Figure 16**). The range is calculated from the actual detection voltage ($-V_{DET}$) of a product and is in the range of $-V_{DET} \times 1.03 \le +V_{DET} \le -V_{DET} \times 1.07$.

Example: For the S-19104C18, the release voltage is either one in the range of 1.785 V $\le +V_{DET} \le$ 1.997 V.
This means that some S-19104C18 have $+V_{DET}$ = 1.785 V and some have $+V_{DET}$ = 1.997 V.

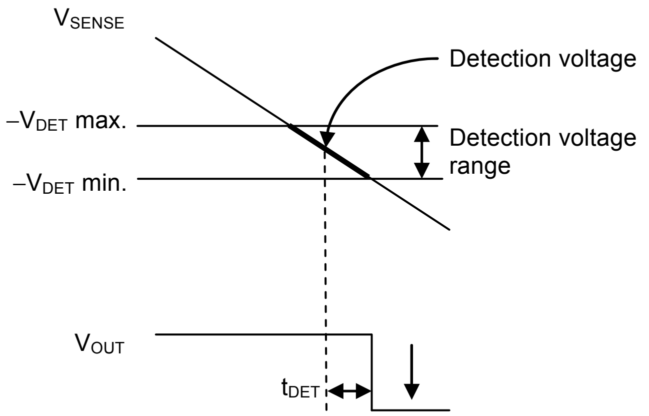


Figure 15 Detection Voltage

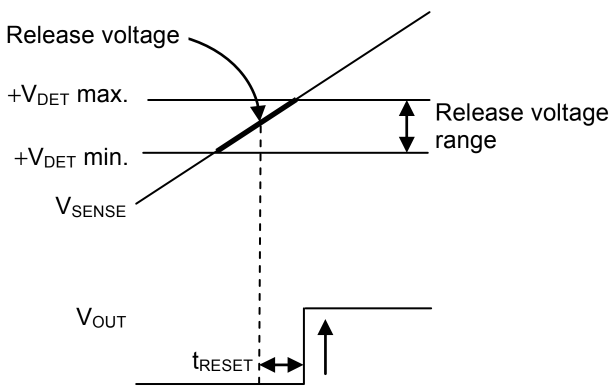


Figure 16 Release Voltage

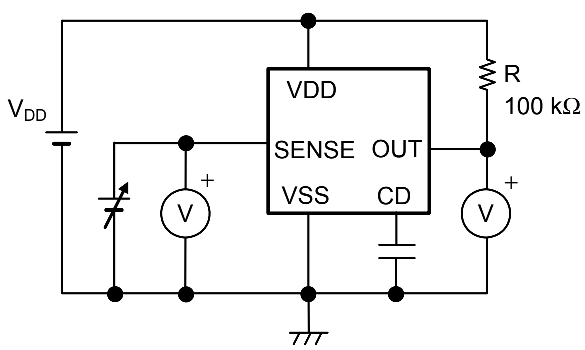


Figure 17 Test Circuit of Detection Voltage and Release Voltage (Nch open-drain output product)

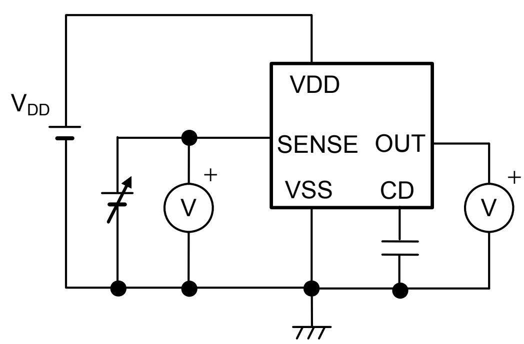


Figure 18 Test Circuit of Detection Voltage and Release Voltage (CMOS output product)

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B − the voltage at point A = V_{HYS} in "**Figure 22 Timing Chart of S-19104/19106 Series N Type**" and "**Figure 24 Timing Chart of S-19104/19106 Series C Type**"). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

4. Release delay time (t_{RESET})

The release delay time is the time period from when the input voltage to the SENSE pin exceeds the release voltage ($+V_{DET}$) to when the output from the OUT pin inverts. The release delay time changes according to the delay capacitor (C_D).

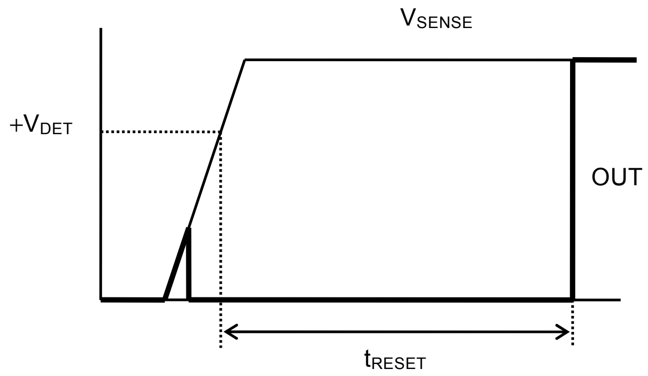


Figure 19 Release Delay Time

5. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

6. Oscillation

In applications where an input resistance is connected (**Figure 20**), taking a CMOS output (active "L") product for example, the feed-through current which is generated when the output goes from "L" to "H" (at the time of release) causes a voltage drop equal to [feed-through current] × [input resistance]. Since the VDD pin and the SENSE pin are shorted as in **Figure 20**, the SENSE pin voltage drops at the time of release. Then the SENSE pin voltage drops below the detection voltage and the output goes from "H" to "L". In this status, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

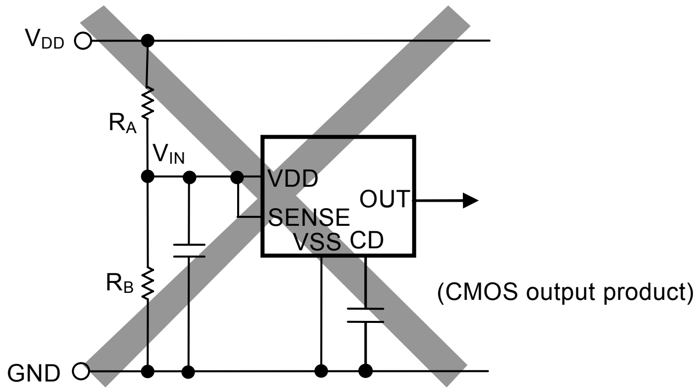


Figure 20 Example for Bad Implementation Due to Detection Voltage Change

■ Operation

1. Basic operation

1. 1 S-19104/19106 Series N type

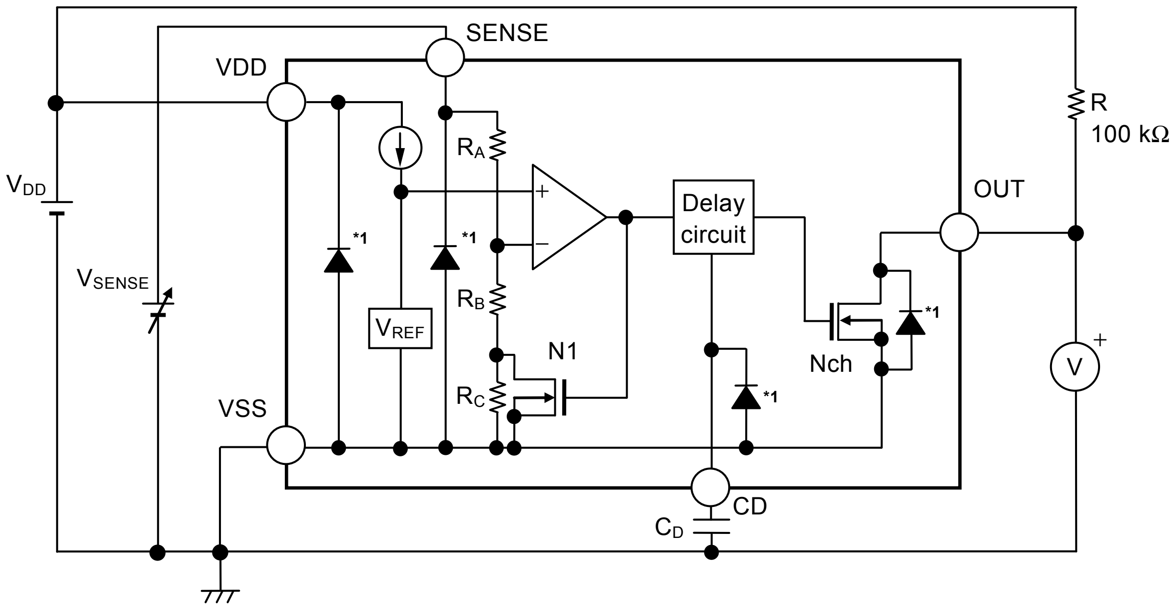
(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or more, and the SENSE pin voltage (V_{SENSE}) is the release voltage ($+V_{DET}$) or more, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up. Since the Nch transistor (N1) is turned off, the comparator input voltage is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if V_{SENSE} decreases to $+V_{DET}$ or less, V_{DD} is output when V_{SENSE} is higher than the detection voltage ($-V_{DET}$).
When V_{SENSE} decreases to $-V_{DET}$ or less (point A in **Figure 22**), the Nch transistor is turned on. And then V_{SS} ("L") is output.
At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or less, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or more.

(4) Even if V_{SENSE} exceeds $-V_{DET}$, V_{SS} is output when V_{SENSE} is less than $+V_{DET}$.

(5) When V_{SENSE} increases to $+V_{DET}$ or more (point B in **Figure 22**), the Nch transistor is turned off. And then V_{DD} is output if the output is pulled up.



***1.** Parasitic diode

Figure 21 Operation of S-19104/19106 Series N Type

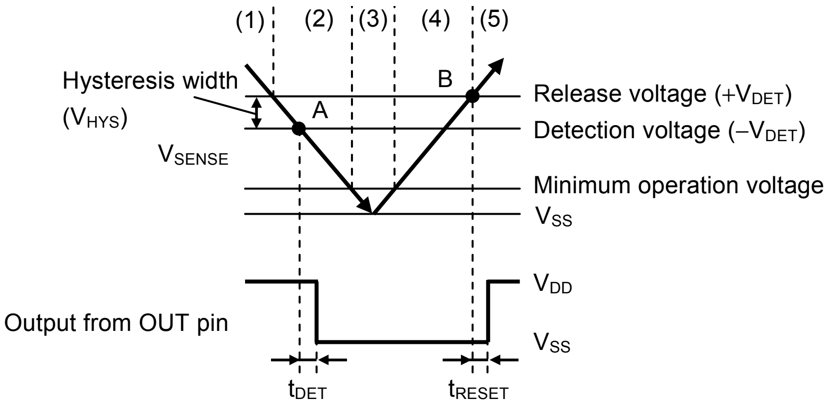


Figure 22 Timing Chart of S-19104/19106 Series N Type

1. 2 S-19104/19106 Series C type

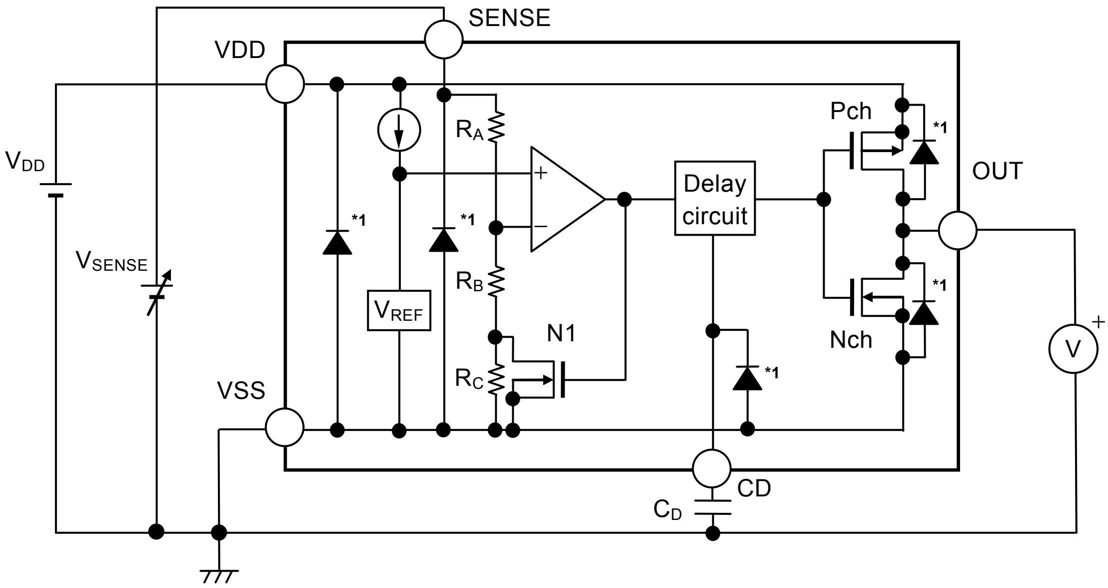
(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or more, and the SENSE pin voltage (V_{SENSE}) is the release voltage ($+V_{DET}$) or more, the Nch transistor is turned off and the Pch transistor is turned on to output V_{DD} ("H"). Since the Nch transistor (N1) is turned off, the comparator input voltage is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if V_{SENSE} decreases to $+V_{DET}$ or less, V_{DD} is output when V_{SENSE} is higher than the detection voltage ($-V_{DET}$).
When V_{SENSE} decreases to $-V_{DET}$ or less (point A in **Figure 24**), the Nch transistor is turned on and the Pch transistor is turned off. And then V_{SS} ("L") is output.
At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or less, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or more.

(4) Even if V_{SENSE} exceeds $-V_{DET}$, V_{SS} is output when V_{SENSE} is less than $+V_{DET}$.

(5) When V_{SENSE} increases to $+V_{DET}$ or more (point B in **Figure 24**), the Nch transistor is turned off and the Pch transistor is turned on. And then V_{DD} is output.



***1.** Parasitic diode

Figure 23 Operation of S-19104/19106 Series C Type

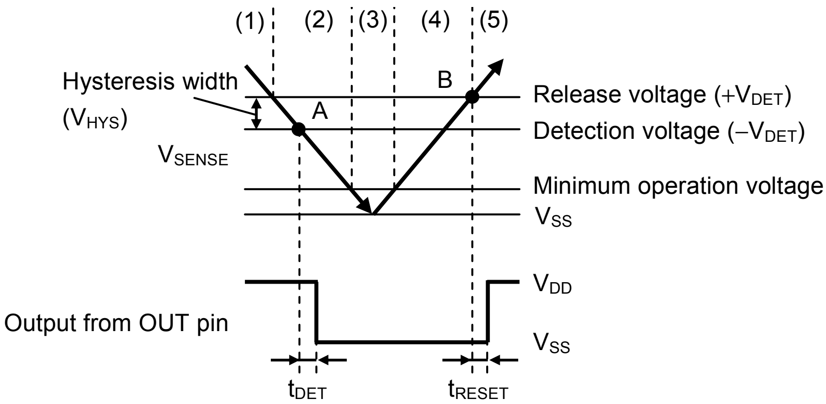


Figure 24 Timing Chart of S-19104/19106 Series C Type

2. SENSE pin

2. 1 Error when detection voltage is set externally

By connecting a node that was resistance-divided by resistance (R_A) and resistance (R_B) to the SENSE pin as seen in **Figure 25**, the detection voltage can be set externally.
For conventional products without the SENSE pin, R_A cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if R_A is large, problems such as oscillation or larger error in the hysteresis width may occur.
In the S-19104/19106 Series, R_A and R_B are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance (R_{SENSE}) that may occur.
Although R_{SENSE} in the S-19104/19106 Series is large (4 MΩ min.) to make the error small, R_A and R_B should be selected such that the error is within the allowable limits.

2. 2 Selection of R_A and R_B

In **Figure 25**, the relation between the external setting detection voltage (V_{DX}) and the actual detection voltage ($-V_{DET}$) is ideally calculated by the equation below.

$$V_{DX} = -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) \qquad \cdots (1)$$

However, in reality there is an error in the current flowing through R_{SENSE}.
When considering this error, the relation between V_{DX} and $-V_{DET}$ is calculated as follows.

$$\begin{aligned} V_{DX} &= -V_{DET} \times \left(1 + \frac{R_A}{R_B \parallel R_{SENSE}}\right) \\ &= -V_{DET} \times \left(1 + \frac{R_A}{\frac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right) \\ &= -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times -V_{DET} \qquad \cdots (2) \end{aligned}$$

By using equations (1) and (2), the error is calculated as $-V_{DET} \times \frac{R_A}{R_{SENSE}}$.
The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100\ [\%] = \frac{R_A \parallel R_B}{R_{SENSE}} \times 100\ [\%] \qquad \cdots (3)$$

As seen in equation (3), the smaller the resistance values of R_A and R_B compared to R_{SENSE}, the smaller the error rate becomes.
Also, the relation between the external setting hysteresis width (V_{HX}) and the hysteresis width (V_{HYS}) is calculated by equation below. Error due to R_{SENSE} also occurs to the relation in a similar way to the detection voltage.

$$V_{HX} = V_{HYS} \times \left(1 + \frac{R_A}{R_B}\right) \qquad \cdots (4)$$

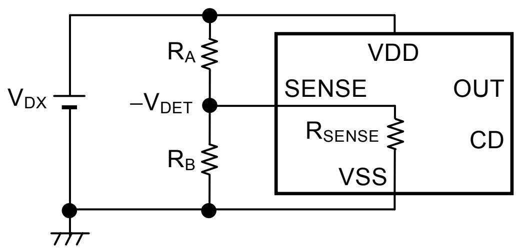


Figure 25 Detection Voltage External Setting Circuit

Caution If R_A and R_B are large, the SENSE pin input impedance becomes high and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.

2. 3 Power on sequence

Apply power in the order, the VDD pin then the SENSE pin.
As seen in **Figure 26**, when $V_{SENSE} \geq +V_{DET}$, the OUT pin output (V_{OUT}) rises and the S-19104/19106 Series becomes the release status (normal operation).

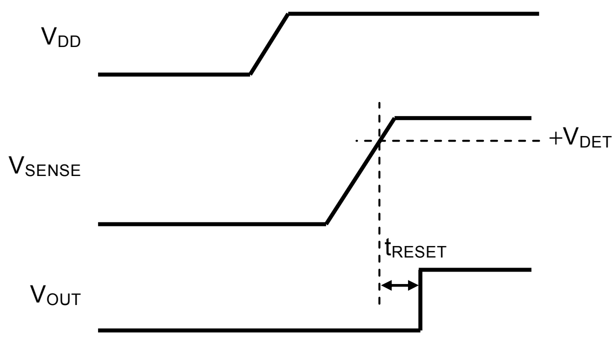


Figure 26

Caution If power is applied in the order the SENSE pin then the VDD pin, an erroneous release may occur even if $V_{SENSE} < +V_{DET}$.

2. 4 Precautions when shorting between the VDD pin and the SENSE pin

2. 4. 1 Input resistance

Do not connect an input resistance (R_A) when shorting between the VDD pin and the SENSE pin.
A feed-through current flows through the VDD pin at the time of release. When connecting the circuit shown as **Figure 27**, the feed-through current of the VDD pin flowing through R_A will cause a drop in V_{SENSE} at the time of release.
At that time, oscillation may occur if $V_{SENSE} \leq -V_{DET}$.

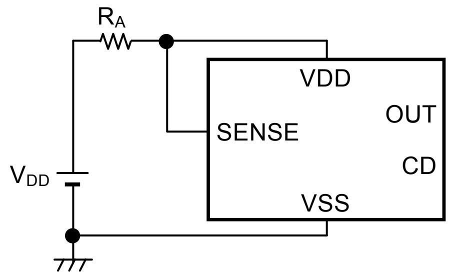


Figure 27

2. 4. 2 Parasitic resistance and parasitic capacitance

Due to the difference in parasitic resistance and parasitic capacitance of the VDD pin and the SENSE pin, power may be applied to the SENSE pin first.
Note that an erroneous release may occur if this happens (refer to "**2. 3 Power on sequence**").

Caution In CMOS output product, make sure that the VDD pin input impedance does not become too high, regardless of the above. Since a feed-through current is large, a malfunction may occur if the VDD pin voltage changes greatly at the time of release.

2. 5 Malfunction when V_{DD} falls

As seen in **Figure 28**, note that if the VDD pin voltage (V_{DD}) drops steeply below 1.2 V when $-V_{DET} < V_{SENSE} < +V_{DET}$, erroneous detection may occur.
When $V_{DD\_Low} \geq 1.2$ V, erroneous detection does not occur.
When $V_{DD\_Low} < 1.2$ V, the more the V_{DD} falling amplitude increases or the shorter the falling time becomes, the easier the erroneous detection.
Perform thorough evaluation in actual application.

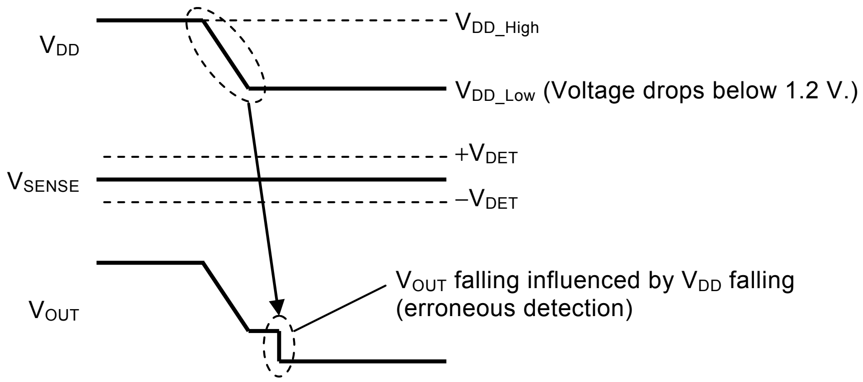


Figure 28

The S-19104C50 example in **Figure 29** shows an example of erroneous detection boundary conditions.

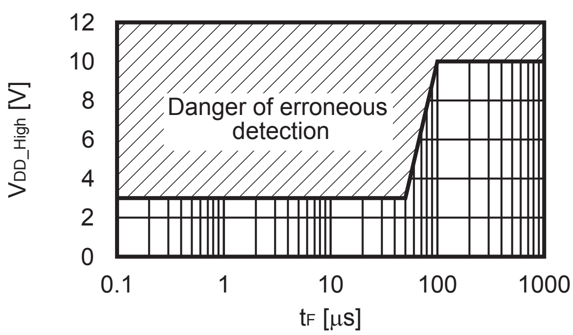


Figure 29

Remark Test conditions

Product name:	S-19104C50
V_{SENSE}:	$-V_{DET(S)} + 0.1$ V
V_{DD_High}:	VDD pin voltage before falling
V_{DD_Low}:	VDD pin voltage after falling (0.95 V)
ΔV_{DD} :	$V_{DD\_High} - V_{DD\_Low}$
t_F :	Falling time of V_{DD} from $V_{DD\_High} - \Delta V_{DD} \times 10\%$ to $V_{DD\_Low} + \Delta V_{DD} \times 10\%$

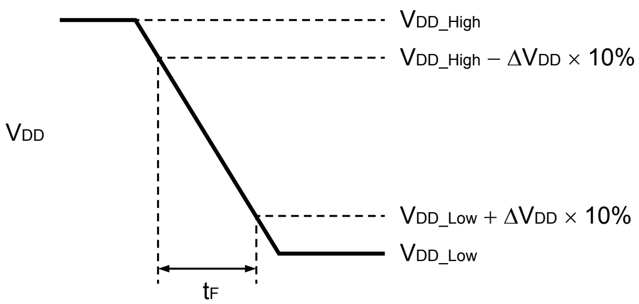


Figure 30

3. Delay circuit

The delay circuit has the function that adjusts the release delay time (t_{RESET}) from when the SENSE pin voltage (V_{SENSE}) reaches release voltage ($+V_{DET}$) to when the output from OUT pin inverts.
t_{RESET} is determined by the delay coefficient, the delay capacitor (C_D), and the release delay time when the CD pin is open (t_{RESET0}), and calculated by the equation below.

$$t_{RESET}\ [\text{ms}] = \text{Delay coefficient} \times C_D\ [\text{nF}] + t_{RESET0}\ [\text{ms}]$$

Table 12

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +105°C	1.98	2.29	3.09
Ta = +25°C	2.34	2.66	3.02
Ta = −40°C	2.68	3.09	3.57

Table 13

Operation Temperature	Release Delay Time when CD Pin is Open (t_{RESET0})		
	Min.	Typ.	Max.
Ta = +105°C	0.020 ms	0.049 ms	0.130 ms
Ta = +25°C	0.021 ms	0.059 ms	0.164 ms
Ta = −40°C	0.024 ms	0.074 ms	0.202 ms

Caution 1. Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.

2. There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value (30 nA to 200 nA).

3. The detection delay time (t_{DET}) cannot be adjusted by C_D.

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- In CMOS output product of the S-19104/19106 Series, the feed-through current flows at the time of detection and release. If the VDD pin input impedance is high, malfunction may occur due to the voltage drop by the feed-through current when releasing.

- In CMOS output product, oscillation may occur if a pull-down resistor is connected and falling speed of the SENSE pin voltage (V_{SENSE}) is slow near the detection voltage when the VDD pin and the SENSE pin are shorted.

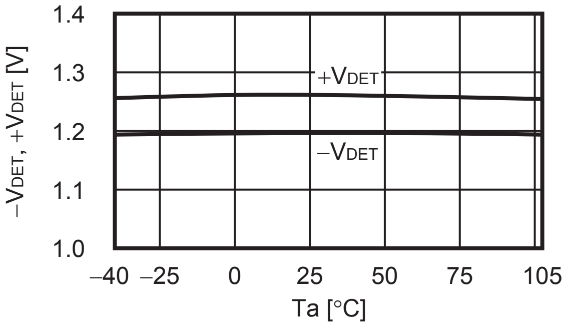
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. SII shall not bear any responsibility for patent infringements related to products using the circuits described herein.

- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

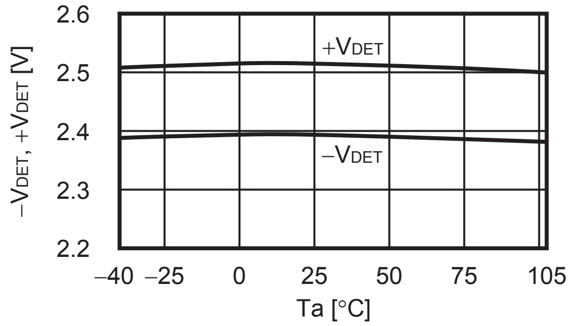
■ Characteristics (Typical Data)

1. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Temperature (Ta)

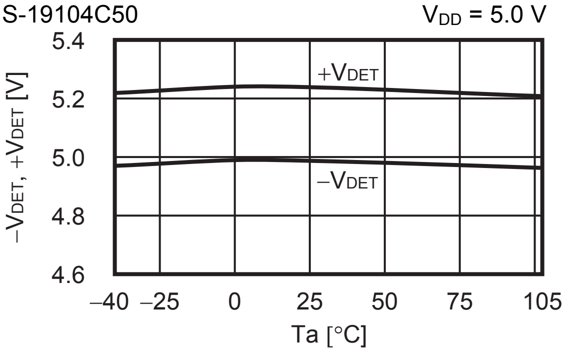
S-19104C12 V_{DD} = 5.0 V



S-19104C24 V_{DD} = 5.0 V

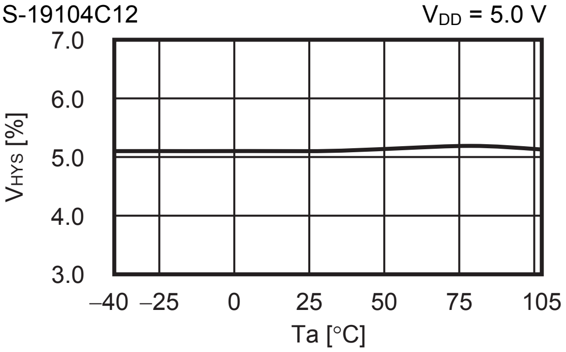


S-19104C50 V_{DD} = 5.0 V

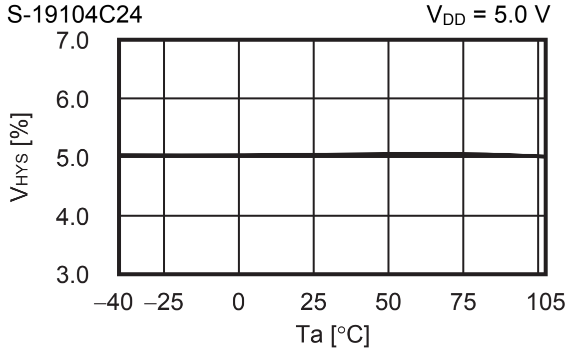


2. Hysteresis width (V_{HYS}) vs. Temperature (Ta)

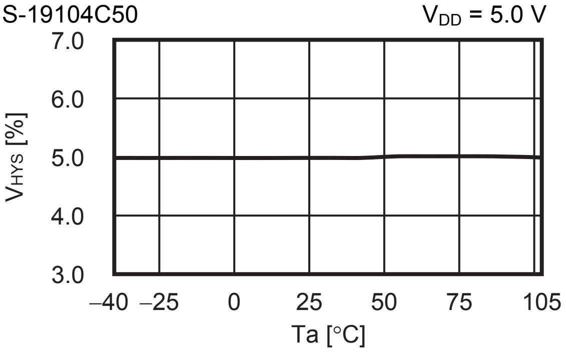
S-19104C12 V_{DD} = 5.0 V



S-19104C24 V_{DD} = 5.0 V

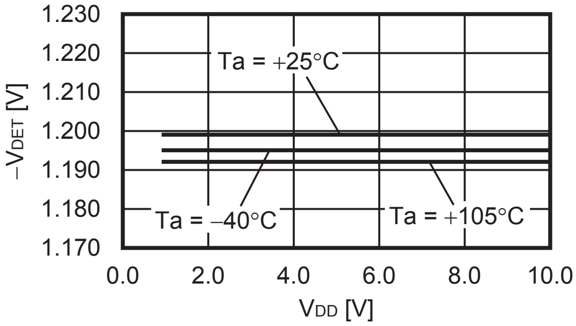


S-19104C50 V_{DD} = 5.0 V

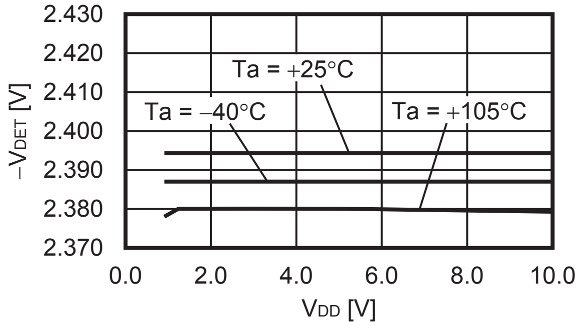


3. Detection voltage ($-V_{DET}$) vs. Power supply voltage (V_{DD})

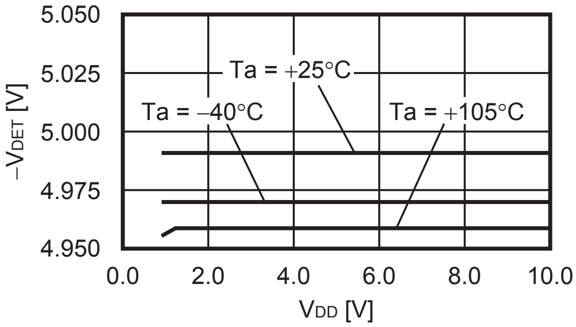
S-19104C12



S-19104C24

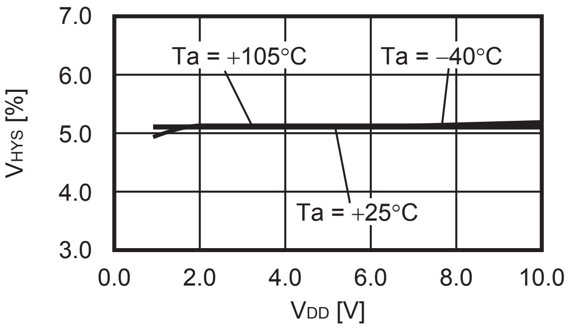


S-19104C50

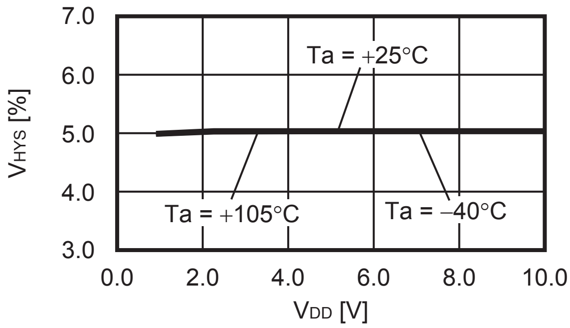


4. Hysteresis width (V_{HYS}) vs. Power supply voltage (V_{DD})

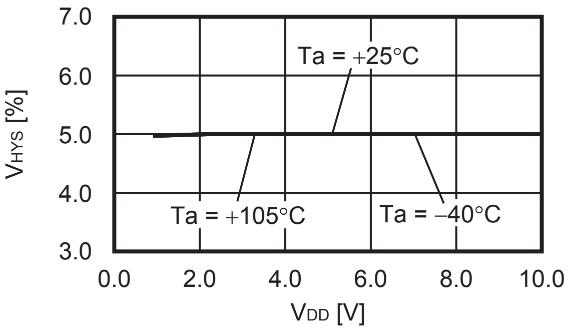
S-19104C12



S-19104C24

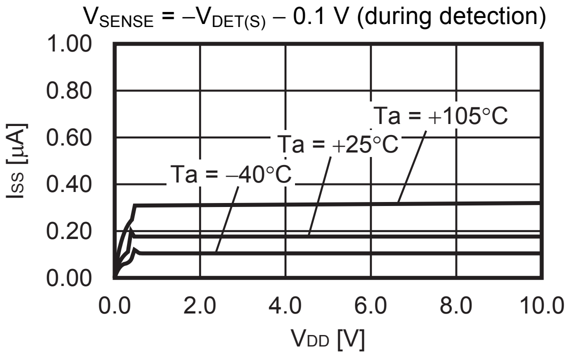


S-19104C50

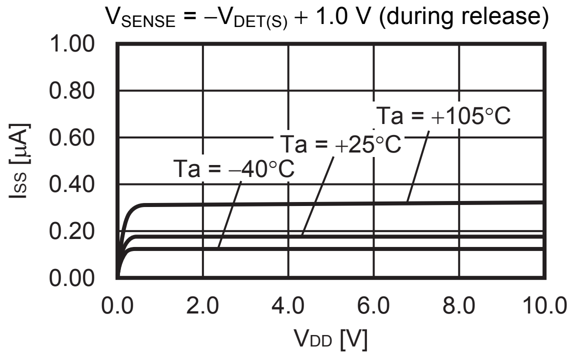


5. Current consumption (I_{SS}) vs. Power supply voltage (V_{DD})

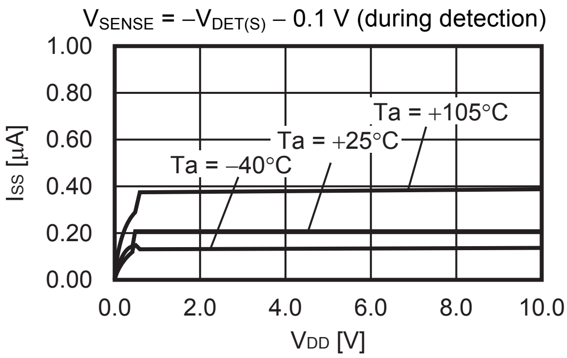
S-19104C12



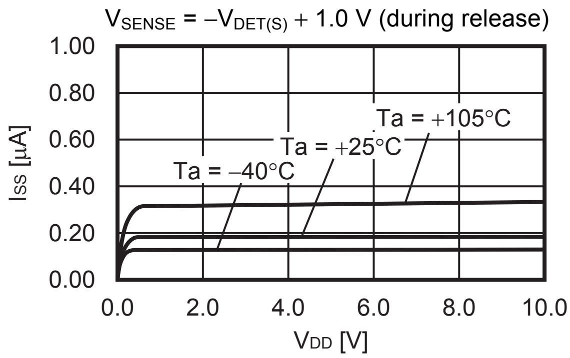
S-19104C12



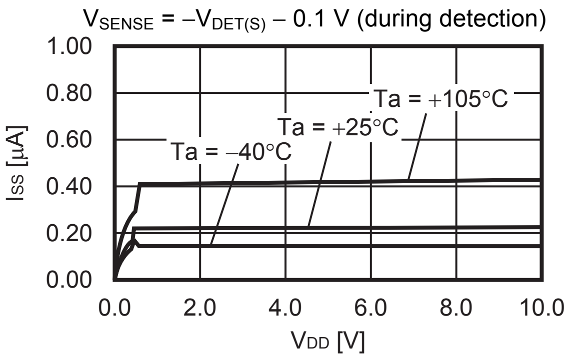
S-19104C24



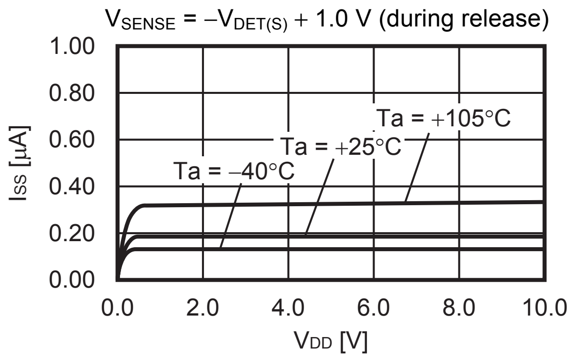
S-19104C24



S-19104C50



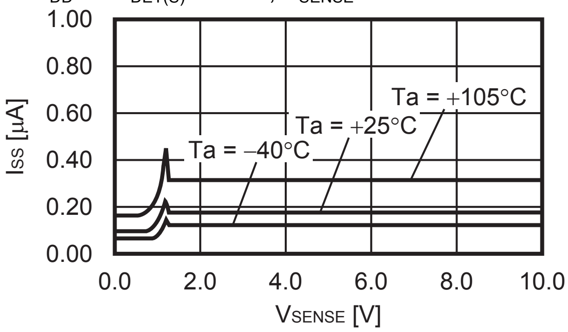
S-19104C50



6. Current consumption (I_{SS}) vs. SENSE pin input voltage (V_{SENSE})

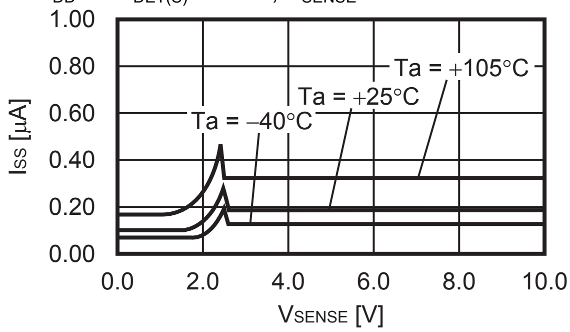
S-19104C12

$V_{DD} = -V_{DET(S)} + 1.0$ V, $V_{SENSE} = 0.0$ V → 10.0 V



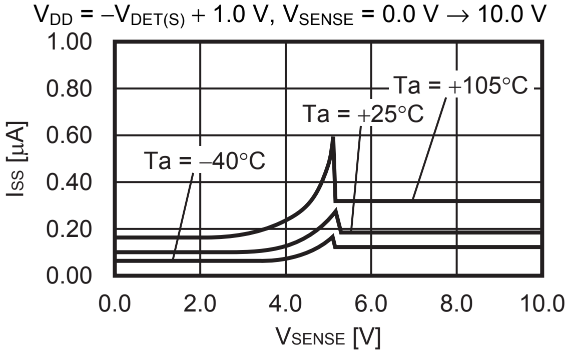
S-19104C24

$V_{DD} = -V_{DET(S)} + 1.0$ V, $V_{SENSE} = 0.0$ V → 10.0 V



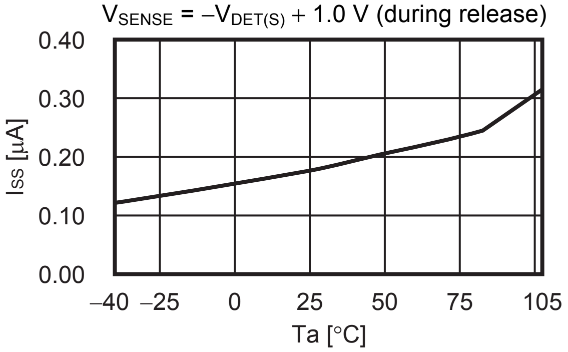
S-19104C50

$V_{DD} = -V_{DET(S)} + 1.0$ V, $V_{SENSE} = 0.0$ V → 10.0 V

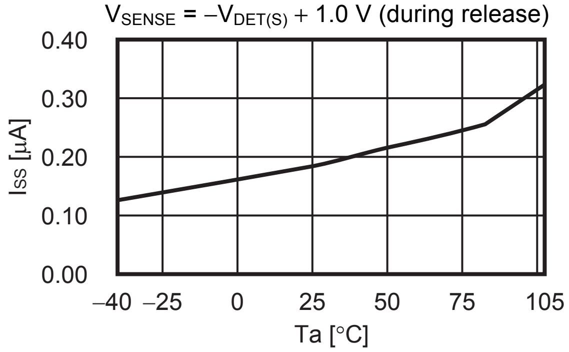


7. Current consumption (I_{SS}) vs. Temperature (Ta)

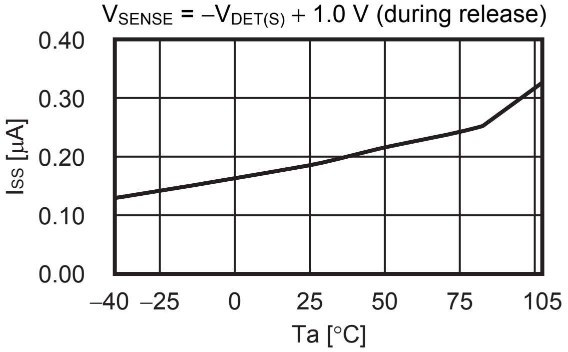
S-19104C12 $V_{DD} = -V_{DET(S)} + 1.0$ V,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)



S-19104C24 $V_{DD} = -V_{DET(S)} + 1.0$ V,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)

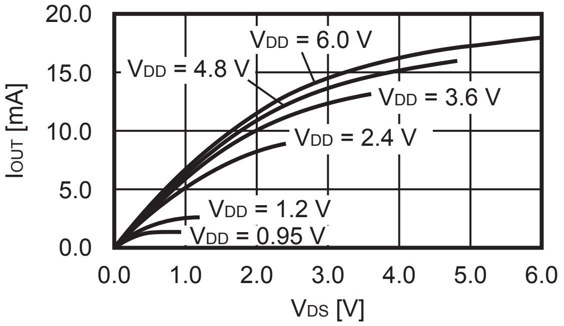


S-19104C50 $V_{DD} = -V_{DET(S)} + 1.0$ V,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)

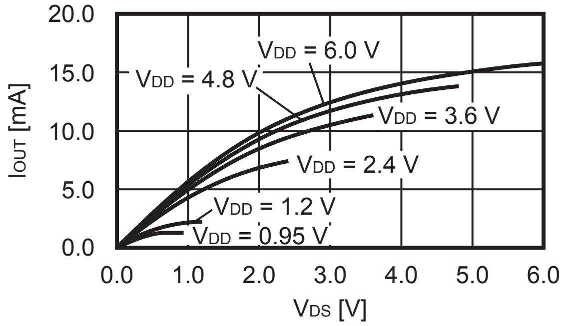


8. Nch transistor output current (I_{OUT}) vs. V_{DS}

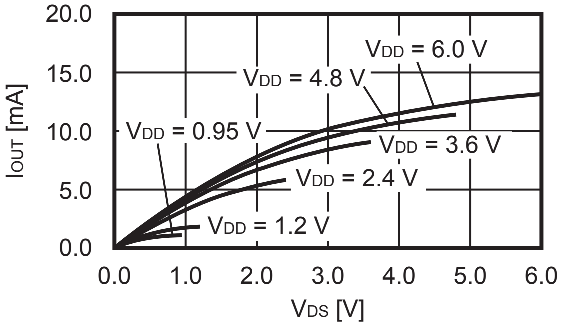
S-19104N12 Ta = −40°C, V_{SENSE} = 0.0 V (during detection)



S-19104N12 Ta = +25°C, V_{SENSE} = 0.0 V (during detection)

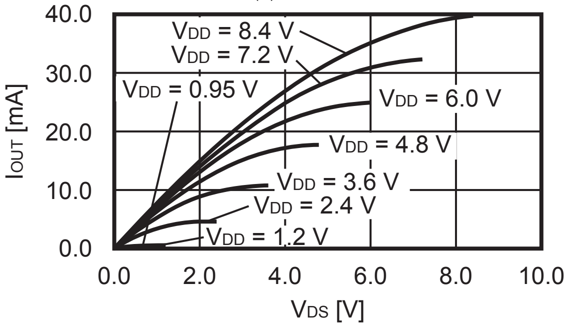


S-19104N12 Ta = +105°C, V_{SENSE} = 0.0 V (during detection)

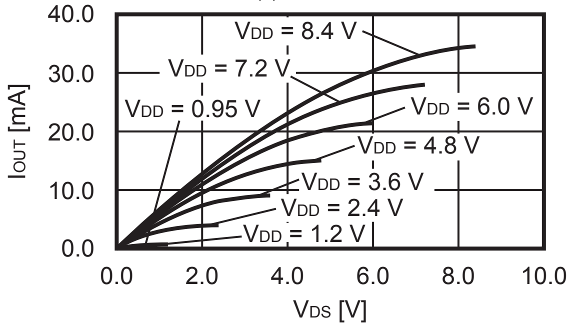


9. Pch transistor output current (I_{OUT}) − V_{DS}

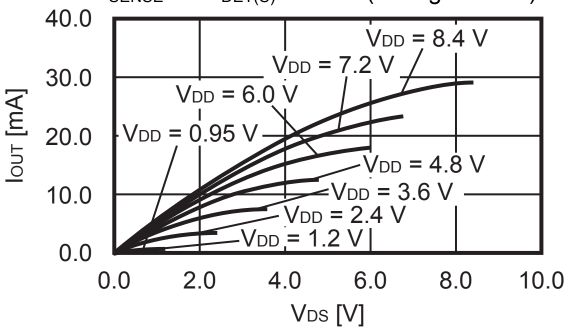
S-19104C12 Ta = −40°C, V_{SENSE} = $-V_{DET(S)}$ + 1.0 V (during release)



S-19104C12 Ta = +25°C, V_{SENSE} = $-V_{DET(S)}$ + 1.0 V (during release)



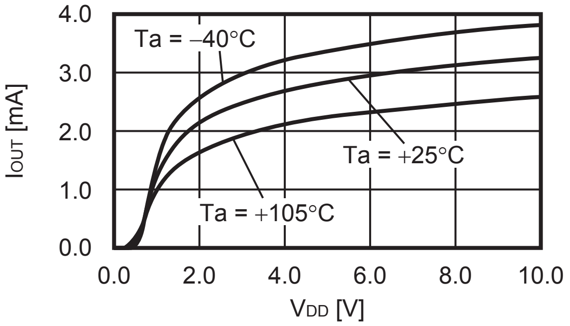
S-19104C12 Ta = +105°C, V_{SENSE} = $-V_{DET(S)}$ + 1.0 V (during release)



Remark V_{DS}: Drain-to-source voltage of the output transistor

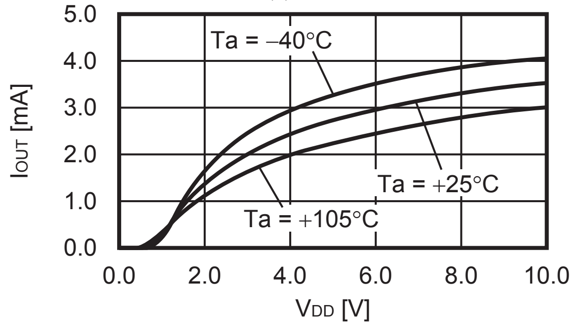
10. Nch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})

S-19104N12 V_{DS} = 0.5 V, V_{SENSE} = 0.0 V (during detection)



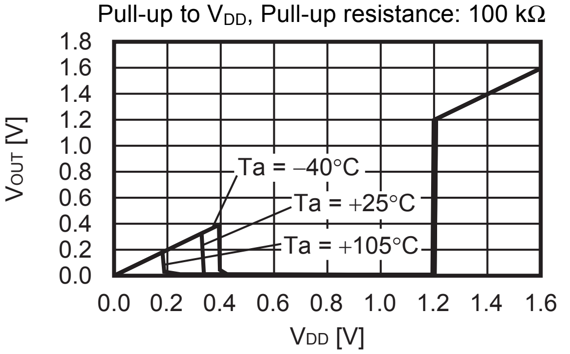
11. Pch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})

S-19104C12 V_{DS} = 0.5 V, V_{SENSE} = $-V_{DET(S)}$ + 1.0 V (during release)

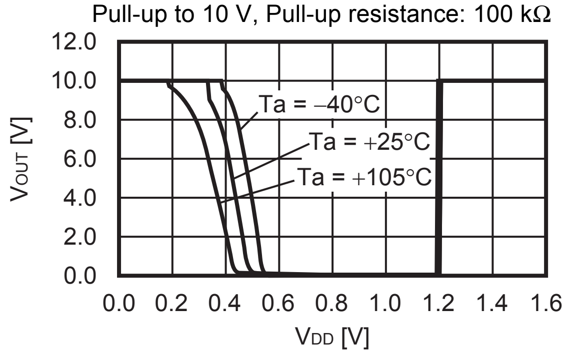


12. Minimum operation voltage (V_{OUT}) vs. Input voltage (V_{DD})

S-19104N12 V_{SENSE} = V_{DD}, Pull-up to V_{DD}, Pull-up resistance: 100 kΩ



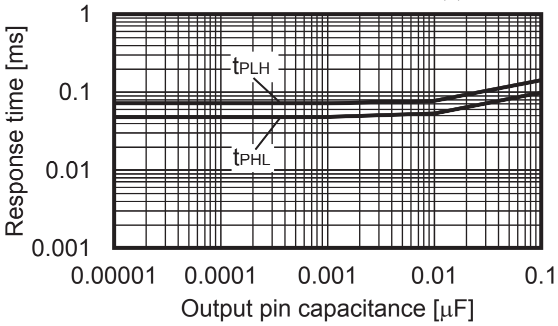
S-19104N12 V_{SENSE} = V_{DD}, Pull-up to 10 V, Pull-up resistance: 100 kΩ



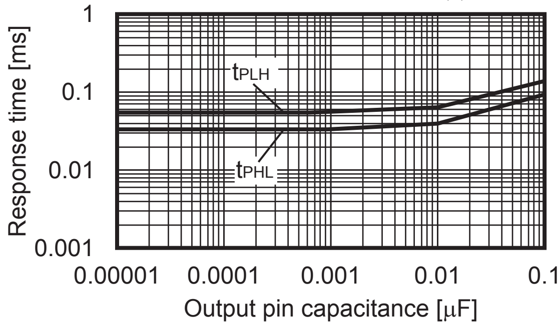
Remark V_{DS}: Drain-to-source voltage of the output transistor

13. Dynamic response vs. Output pin capacitance (C_{OUT}) (CD pin; open)

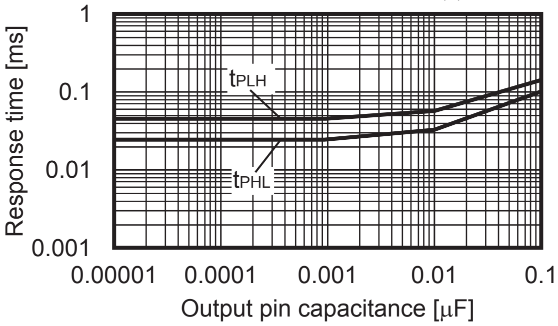
S-19104C12 Ta = –40°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



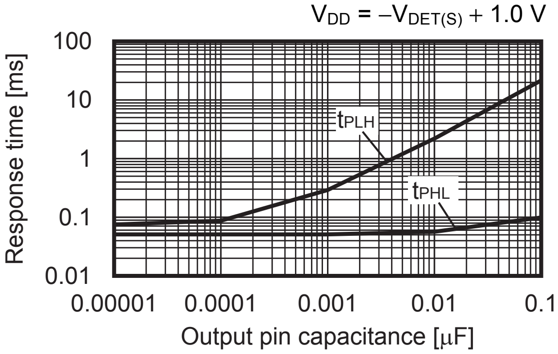
S-19104C12 Ta = +25°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



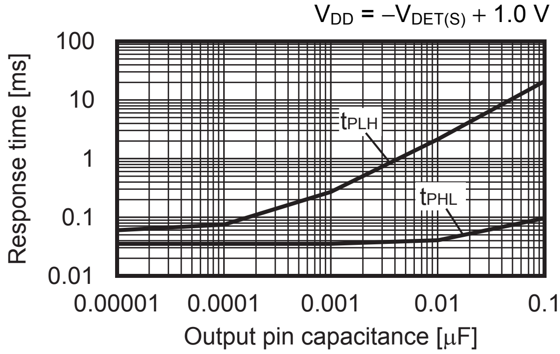
S-19104C12 Ta = +105°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



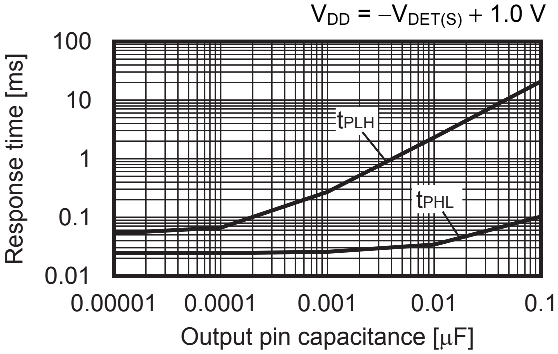
S-19104N12 Ta = –40°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



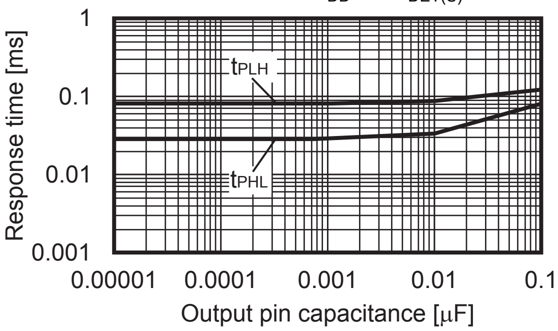
S-19104N12 Ta = +25°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



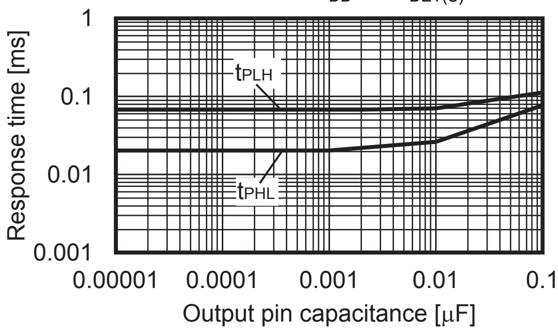
S-19104N12 Ta = +105°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



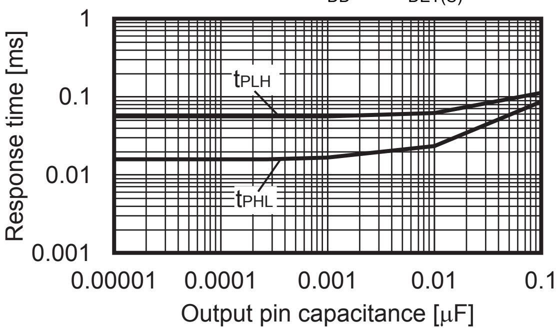
S-19104C50 Ta = −40°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



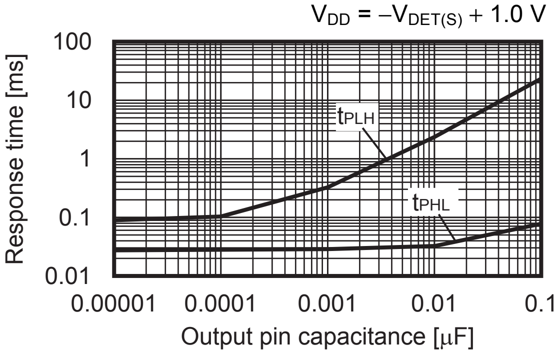
S-19104C50 Ta = +25°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



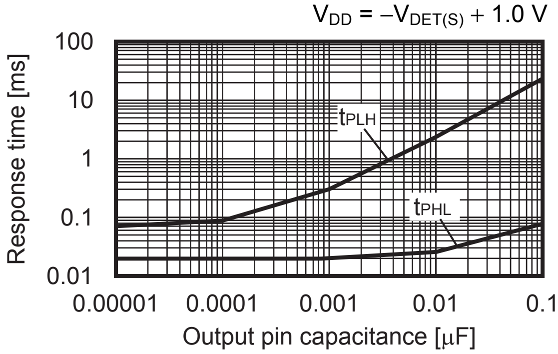
S-19104C50 Ta = +105°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



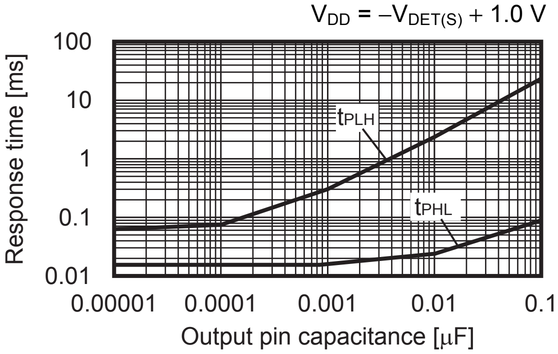
S-19104N50 Ta = −40°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V

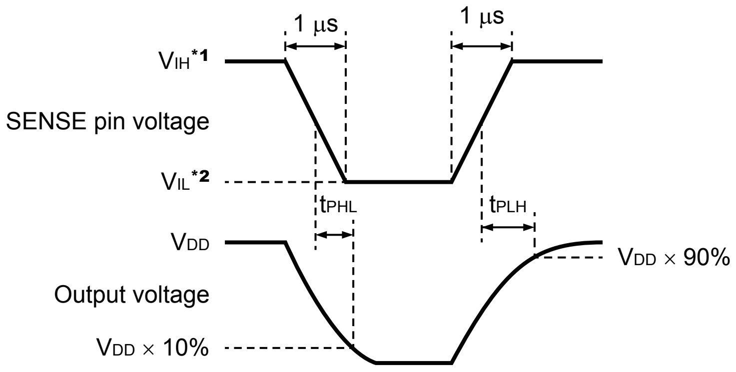


S-19104N50 Ta = +25°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V



S-19104N50 Ta = +105°C, V_{DD} = $-V_{DET(S)}$ + 1.0 V





***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.95 V

Figure 31 Test Condition of Response Time

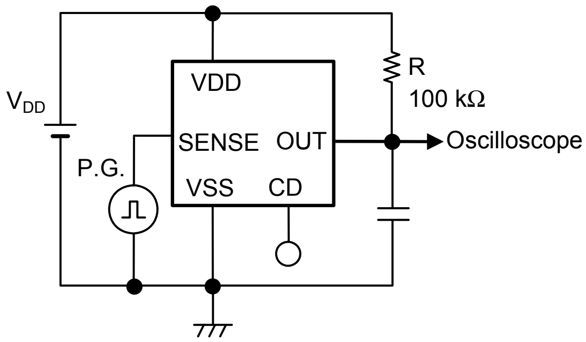


Figure 32 Test Circuit of Response Time (Nch open-drain output product)

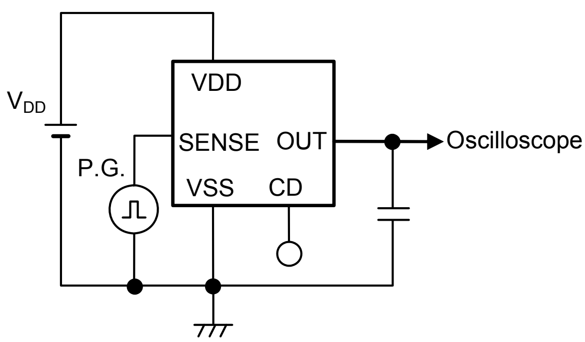
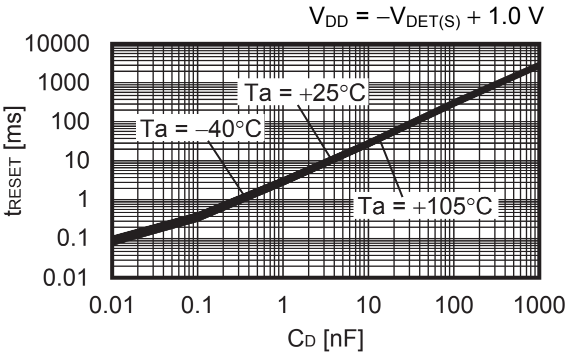


Figure 33 Test Circuit of Response Time (CMOS output product)

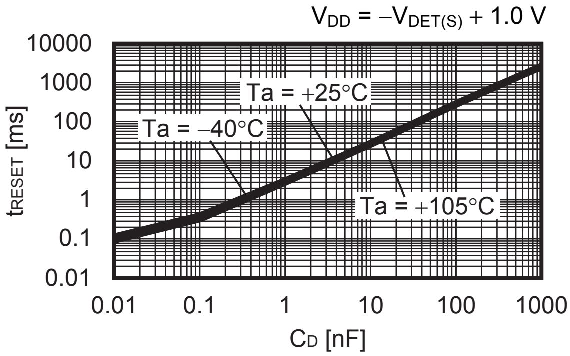
Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

14. Release delay time (t_{RESET}) vs. CD pin capacitance (C_D) (Without output pin capacitance)

S-19104C12

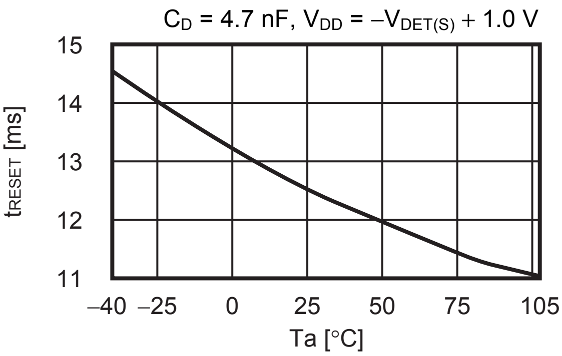


S-19104C50

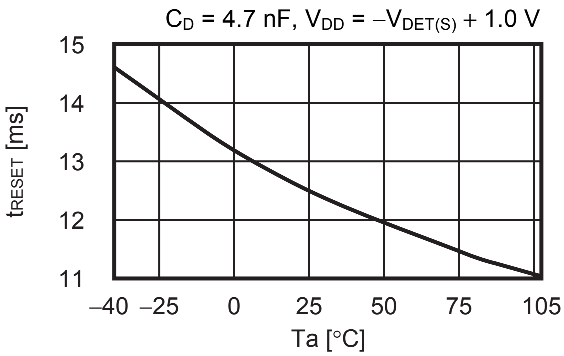


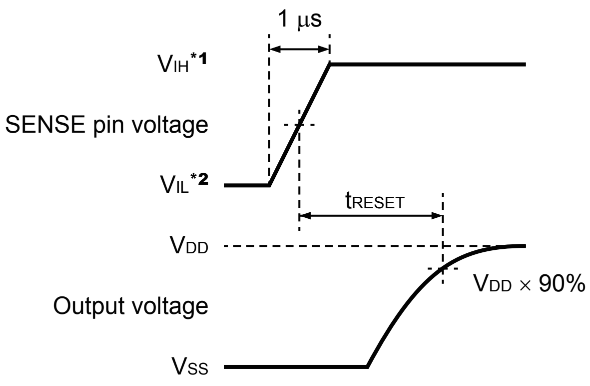
15. Release delay time (t_{RESET}) vs. Temperature (Ta)

S-19104C12



S-19104C50





***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.95 V

Figure 34 Test Condition of Release Delay Time

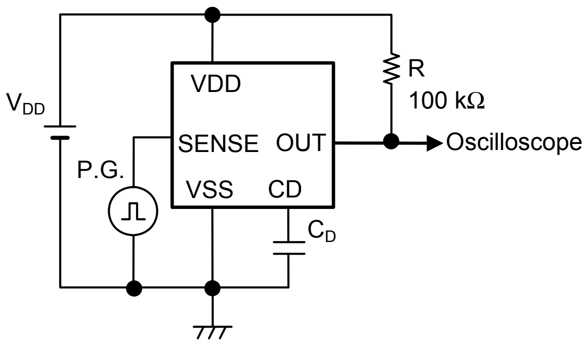


Figure 35 Test Circuit of Release Delay Time (Nch open-drain output product)

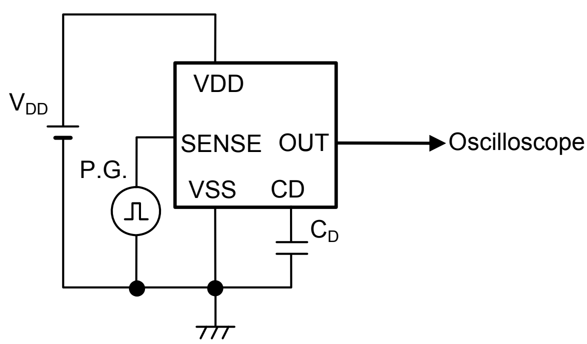


Figure 36 Test Circuit of Release Delay Time (CMOS output product)

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Application Circuit Examples

1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the minimum operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.

Using the S-19104/19106 Series which has the low minimum operation voltage, the high-accuracy detection voltage and the hysteresis width, reset circuits can be easily constructed as seen in **Figure 37** and **Figure 38**.

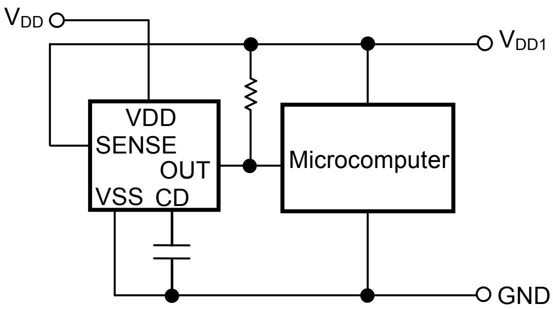


Figure 37 Example of Reset Circuit (Nch open-drain output product)

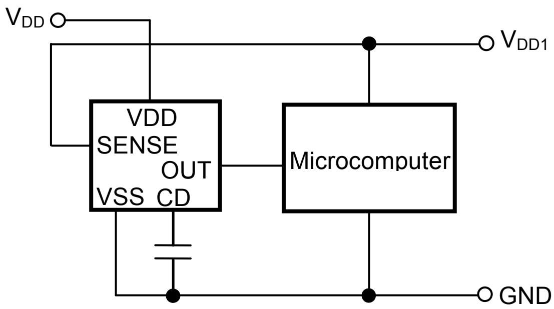


Figure 38 Example of Reset Circuit (CMOS output product)

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Change of detection voltage

If there is not a product with a specified detection voltage value in the S-19104/19106 Series, the detection voltage can be changed by using a resistance divider or a diode, as seen in **Figure 39** to **Figure 42**.
In **Figure 39** and **Figure 40**, hysteresis width also changes.

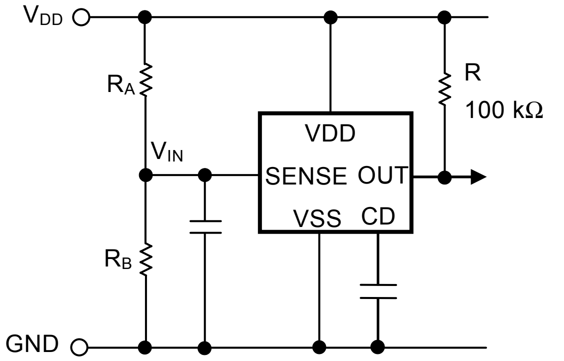


Figure 39 Detection voltage change when using a resistance divider (Nch open-drain output product)

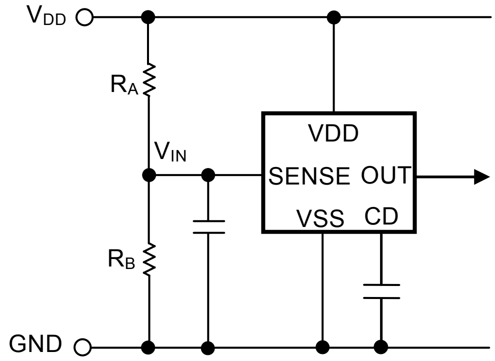


Figure 40 Detection voltage change when using a resistance divider (CMOS output product)

Remark Detection voltage = $\frac{R_A + R_B}{R_B} \bullet -V_{DET}$

Hysteresis width = $\frac{R_A + R_B}{R_B} \bullet V_{HYS}$

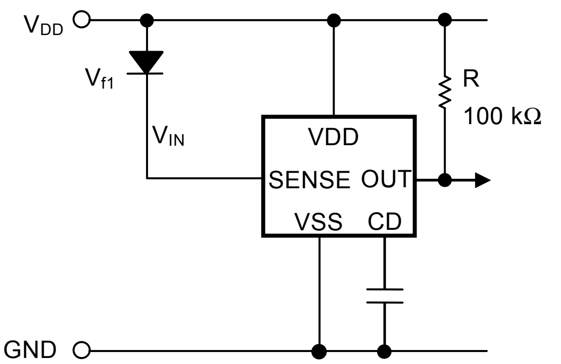


Figure 41 Detection voltage change when using a diode (Nch open-drain output product)

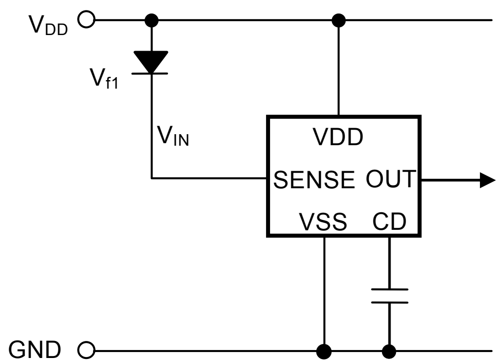
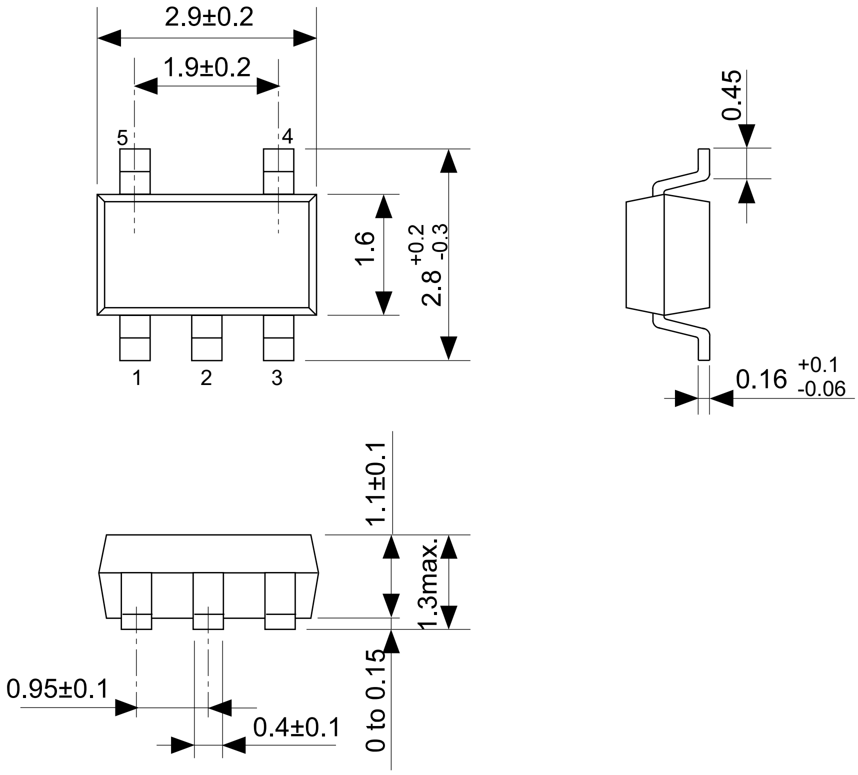


Figure 42 Detection voltage change when using a diode (CMOS output product)

Remark Detection voltage = $V_{f1} + (-V_{DET})$

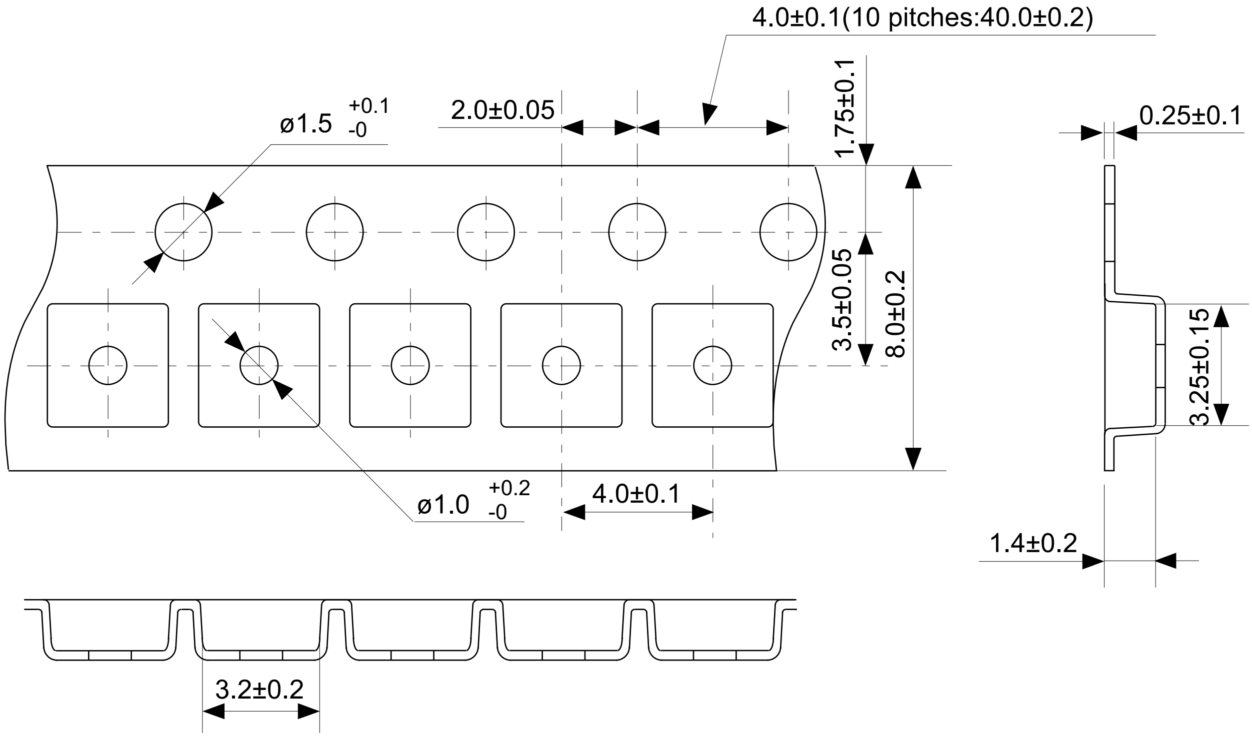
Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
2. Set the constants referring to "2. 1 Error when detection voltage is set externally" in "■ Operation".

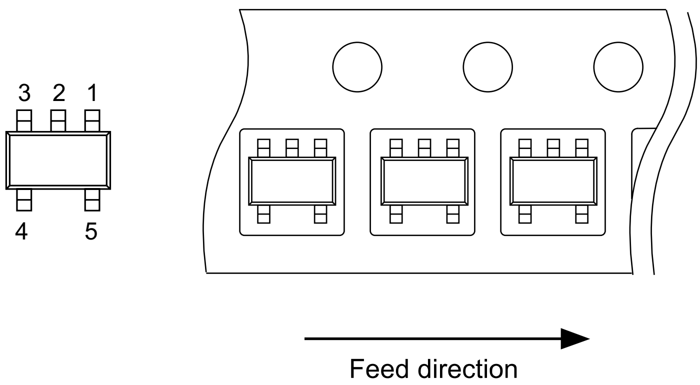


No. MP005-A-P-SD-1.2

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.2
SCALE	
UNIT	mm

Seiko Instruments Inc.

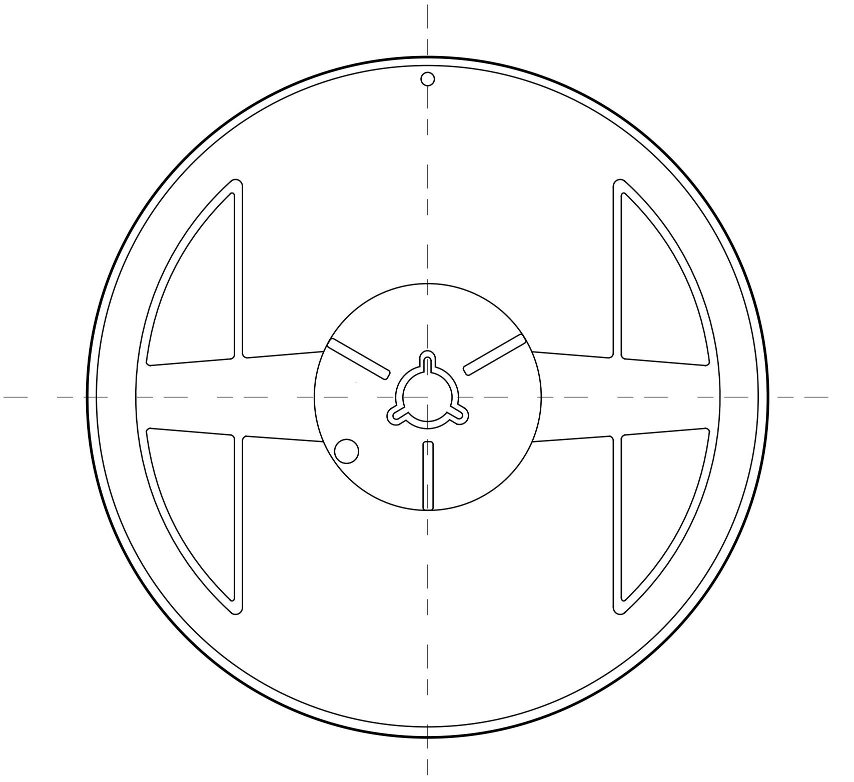


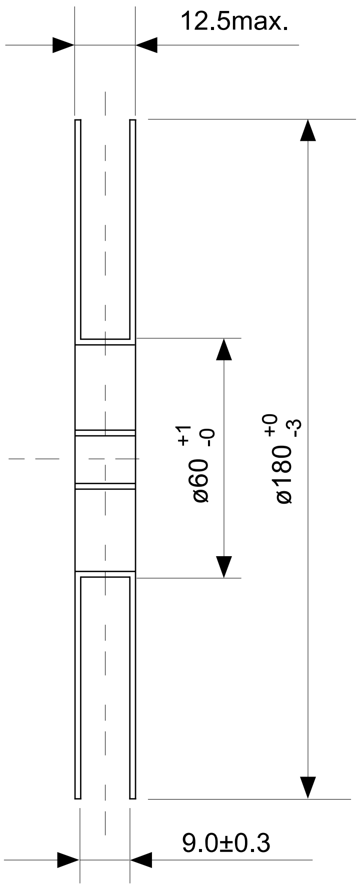


No. MP005-A-C-SD-2.1

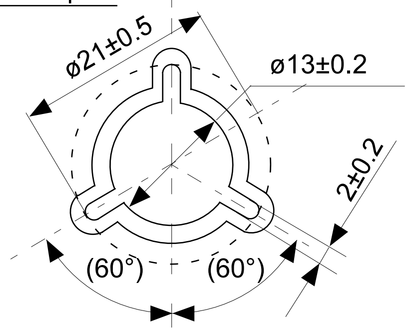
TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
SCALE	
UNIT	mm

Seiko Instruments Inc.





Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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