S-19192 Series

AUTOMOTIVE, 105°C OPERATION, BATTERY MONITORING IC FOR 3-SERIAL TO 6-SERIAL CELL PACK

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Rev.1.0_00

The S-19192 Series is a monitoring IC for automotive rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. Switching control for 3-serial to 6-serial cell is possible by inputting voltage to the SEL1 pin and the SEL2 pin.
In addition, the S-19192 Series can perform a self-test to confirm overcharge and overdischarge detection operations.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.

■ Features

- High-accuracy voltage detection circuit for each cell
  Overcharge detection voltage n (n = 1 to 6): 2.500 V to 4.500 V (25 mV step) Accuracy ±20 mV (Ta = +25°C)
  Accuracy ±30 mV (Ta = –5°C to +55°C)
  Overcharge release voltage n (n = 1 to 6): 2.300 V to 4.500 V (50 mV step)[*1] Accuracy ±50 mV
  Overdischarge detection voltage n (n = 1 to 6): 1.500 V to 3.000 V (100 mV step)[*2, *3] Accuracy ±80 mV
  Overdischarge release voltage n (n = 1 to 6): 1.500 V to 3.300 V (100 mV step)[*4] Accuracy ±100 mV
- Self-test function to confirm overcharge and overdischarge detection operations is available.
  Delay time shortening function during self-test is selectable from "available" / "unavailable".
- Each delay time is settable by an internal circuit only (External capacitors are not necessary).
  Detection delay time is selectable: 32 ms, 64 ms, 128 ms, 256 ms
  Release delay time is selectable: 2.0 ms, 4.0 ms, 8.0 ms, 16.0 ms
- Switching control for 3-serial to 6-serial cell is possible by inputting voltage to the SEL1 pin and the SEL2 pin.
- Two output pins: OUT1 pin: Overcharge and overdischarge detection results
  OUT2 pin: Self-test results
- Output form is selectable: CMOS output, Nch open-drain output
- Output logic is selectable: Active "H", active "L"
- High-withstand voltage: Absolute maximum rating 28 V
- Wide operation voltage range: 6 V to 28 V
- Wide operation temperature range: Ta = –40°C to +105°C
- Low current consumption
  During operation: 18 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 in process[*5]
- The following documents are available when customers perform verifications for "Hardware Component Qualification" in order to meet "Functional Safety Requirements".[*5, *6]
  "Hardware Safety Analysis Report"
  "Hardware Integration and Testing Report"
  "Qualification Kit"

***1.** Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage n (n = 1 to 6) is selectable from 0 V to 400 mV in 50 mV step.)
***2.** Set the voltage difference between the overcharge detection voltage and overdischarge detection voltage to 2.5 V or lower.
***3** When the S-19192 Series is used for monitoring a 3-serial-cell battery, set the overdischarge detection voltage n (n = 1 to 6) to 2.0 V or higher.
***4.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage n (n = 1 to 6) is selectable from 0 V to 0.7 V in 100 mV step.)
***5.** Contact our sales office for details.
***6.** The Non Disclosure Agreement is necessary when providing the documents.

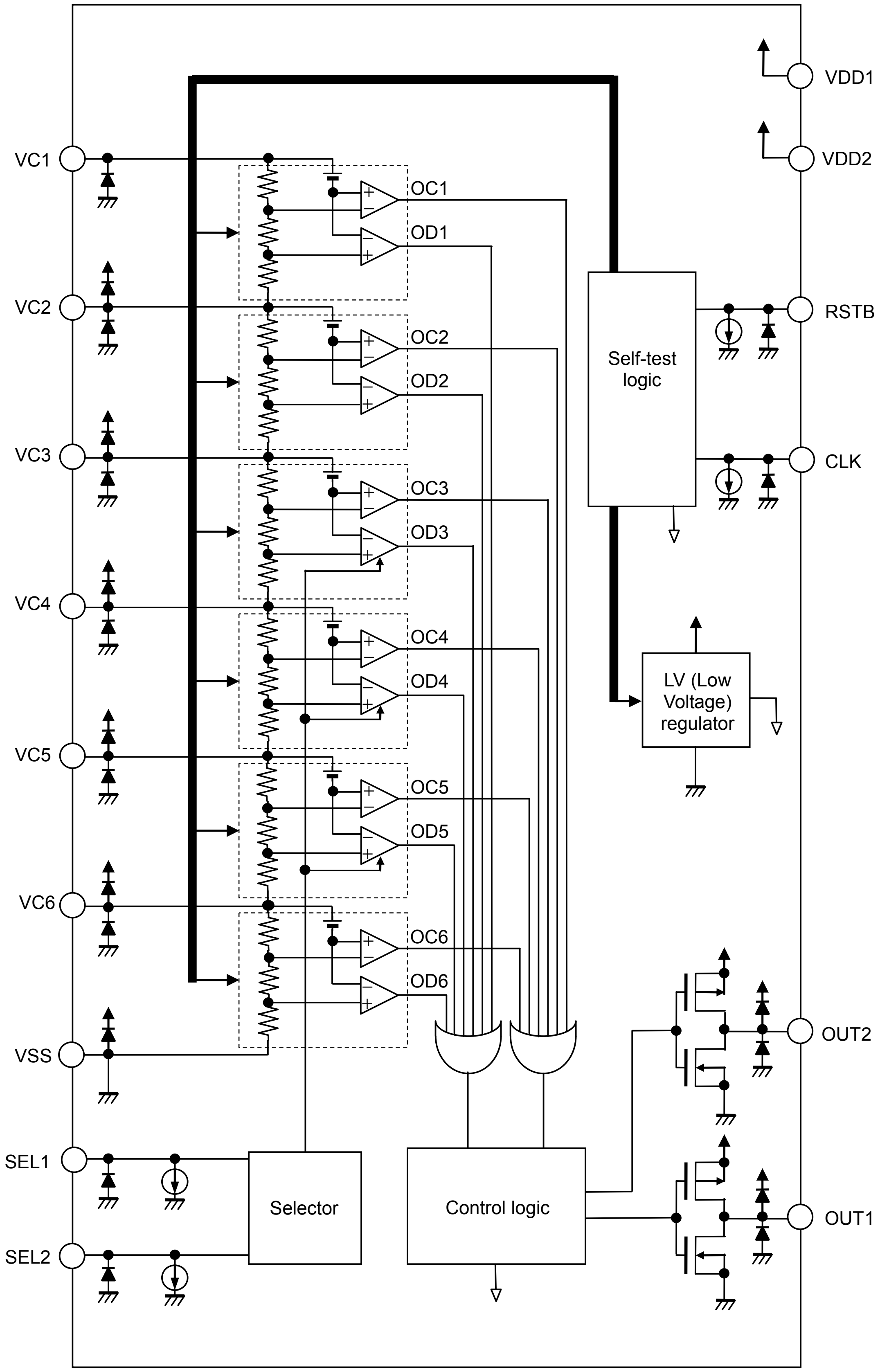
■ Application

- Automotive rechargeable battery pack (EV, HEV, PHEV)

■ Package

- HTSSOP-16

■ Block Diagram



Remark The diodes in the figure are parasitic diodes.

Figure 1

■ AEC-Q100 in Process

Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name

S-19192 xxx H - BCT1 U

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications[*1]
BCT1: HTSSOP-16, Tape

Operation temperature
H: Ta = –40°C to +105°C

Serial code[*2]
Sequentially set from AAA to ZZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
HTSSOP-16	FR016-A-P-SD	FR016-A-C-SD	FR016-A-R-SD	FR016-A-L-SD

3. Product name list

Table 2 (1 / 2)

Product Name	Overcharge Detection Voltage $[V_{CU}]$	Overcharge Release Voltage $[V_{CL}]$	Overdischarge Detection Voltage $[V_{DL}]$	Overdischarge Release Voltage $[V_{DU}]$	Detection Delay Time[*1] $[t_{DET}]$	Release Delay Time[*2] $[t_{REL}]$
S-19192AAAH-BCT1U	4.350 V	4.100 V	2.000 V	2.400 V	128 ms	2.0 ms

Table 2 (2 / 2)

Product Name	Delay Time Shortening during Self-test[*3]	OUT1 Pin		OUT2 Pin	
		Output Form	Output Logic	Output Form	Output Logic
S-19192AAAH-BCT1U	Unavailable	CMOS output	Active "H"	CMOS output	Active "H"

***1.** Detection delay time is selectable from 32 ms, 64 ms, 128 ms, 256 ms.
***2.** Release delay time is selectable from 2.0 ms, 4.0 ms, 8.0 ms, 16.0 ms.
***3.** Refer to "**■ Self-test Function**" for details.

Remark Please contact our sales office for products other than those specified above.

■ Pin Configuration

1. HTSSOP-16

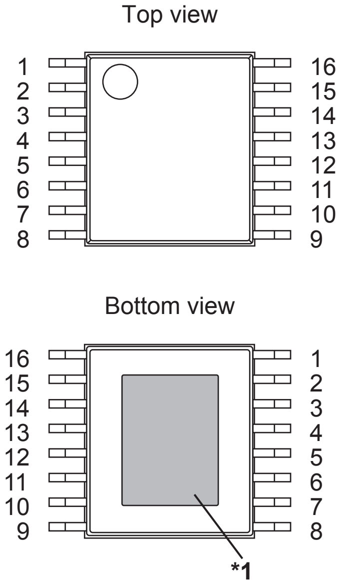


Figure 2

Table 3

Pin No.	Symbol	Description
1	VDD1[*2]	Input pin for positive power supply, connection pin for positive voltage of battery 1
2	VC1	Connection pin for positive voltage of battery 1
3	VC2	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
4	VC3	Connection pin for negative voltage of battery 2, connection pin for positive voltage of battery 3
5	VC4	Connection pin for negative voltage of battery 3, connection pin for positive voltage of battery 4
6	VC5	Connection pin for negative voltage of battery 4, connection pin for positive voltage of battery 5
7	VC6	Connection pin for negative voltage of battery 5, connection pin for positive voltage of battery 6
8	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 6
9	NC[*3]	No connection
10	OUT2	Output pin 2 (Refer to "■ **Self-test Function**")
11	OUT1	Output pin 1 (Refer to "■ **Operation**" and "■ **Self-test Function**")
12	SEL2	Switching pins for number of serial cells [SEL1, SEL2] = ["L", "L"] : 6-serial cell [SEL1, SEL2] = ["L", "H"] : 5-serial cell [SEL1, SEL2] = ["H", "L"] : 4-serial cell [SEL1, SEL2] = ["H", "H"] : 3-serial cell
13	SEL1	
14	CLK	Input pin for clock signal
15	RSTB	Input pin for reset signal
16	VDD2[*2]	Input pin for positive power supply, connection pin for positive voltage of battery 1

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential open.
However, do not use it as the function of electrode.

***2.** Be sure to connect both the VDD1 pin and the VDD2 pin to the positive power supply.

***3.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD1, VDD2	$V_{SS} - 0.3$ to $V_{SS} + 28$	V
Input pin voltage	V_{IN}	VC1, VC2, VC3, VC4, VC5, VC6, SEL1, SEL2, RSTB, CLK	$V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 28$	V
Output pin voltage	V_{OUT}	OUT1, OUT2	$V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 28$	V
Operation ambient temperature	T_{opr}	–	–40 to +105	°C
Storage temperature	T_{stg}	–	–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance[*1]	θ_{JA}	HTSSOP-16	Board A	–	91	–	°C/W
			Board B	–	65	–	°C/W
			Board C	–	34	–	°C/W
			Board D	–	32	–	°C/W
			Board E	–	26	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 6 (1 / 2)

(V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection Voltage						
Overcharge detection voltage n (n = 1 to 6)	V_{CUn}	–	V_{CUn} – 0.020	V_{CUn}	V_{CUn} + 0.020	V
		Ta = –5°C to +55°C[*1]	V_{CUn} – 0.030	V_{CUn}	V_{CUn} + 0.030	V
Overdischarge detection voltage n (n = 1 to 6)	V_{DLn}	–	V_{DLn} – 0.080	V_{DLn}	V_{DLn} + 0.080	V
Release Voltage		–				
Overcharge release voltage n (n = 1 to 6)	V_{CLn}	–	V_{CLn} – 0.050	V_{CLn}	V_{CLn} + 0.050	V
Overdischarge release voltage n (n = 1 to 6)	V_{DUn}	–	V_{DUn} – 0.100	V_{DUn}	V_{DUn} + 0.100	V
Input Voltage						
Operation voltage between VDD pin and VSS pin	V_{DSOP}	–	6	–	28	V
SEL1 pin voltage "H"	V_{SEL1H}	–	V_{DS} – 0.5	–	–	V
SEL1 pin voltage "L"	V_{SEL1L}	–	–	–	0.5	V
SEL2 pin voltage "H"	V_{SEL2H}	–	V_{DS} – 0.5	–	–	V
SEL2 pin voltage "L"	V_{SEL2L}	–	–	–	0.5	V
RSTB pin voltage "H"	V_{RSTBH}	–	1.6	–	–	V
RSTB pin voltage "L"	V_{RSTBL}	–	–	–	0.5	V
CLK pin voltage "H"	V_{CLKH}	–	1.6	–	–	V
CLK pin voltage "L"	V_{CLKL}	–	–	–	0.5	V

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

Table 6 (2 / 2)

(V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Current						
Current consumption during operation	I_{OPE}	–	–	10	18	μA
Current consumption during overcharge	I_{OPEC}	V1 = V2 = V3 = V4 = V5 = V6 = V_{CU} + 0.1 V	–	–	18	μA
Current consumption during overdischarge	I_{OPED}	V1 = V2 = V3 = V4 = V5 = V6 = V_{DL} – 0.1 V	–	–	18	μA
VC1 pin current	I_{VC1}	–	–	1.5	2.0	μA
VC2 pin current	I_{VC2}	–	–0.1	0.0	0.1	μA
VC3 pin current	I_{VC3}	–	–0.1	0.0	0.1	μA
VC4 pin current	I_{VC4}	–	–0.1	0.0	0.1	μA
VC5 pin current	I_{VC5}	–	–0.1	0.0	0.1	μA
VC6 pin current	I_{VC6}	–	–0.1	0.0	0.1	μA
SEL1 pin sink current	I_{SEL1H}	$V_{SEL1} = V_{DS}$	–	1.0	4.0	μA
SEL1 pin leakage current	I_{SEL1L}	V_{SEL1} = 0 V	–0.1	–	0.1	μA
SEL2 pin sink current	I_{SEL2H}	$V_{SEL2} = V_{DS}$	–	1.0	4.0	μA
SEL2 pin leakage current	I_{SEL2L}	V_{SEL2} = 0 V	–0.1	–	0.1	μA
RSTB pin sink current	I_{RSTBH}	$V_{RSTB} = V_{DS}$	–	1.0	4.0	μA
RSTB pin leakage current	I_{RSTBL}	V_{RSTB} = 0 V	–0.1	–	0.1	μA
CLK pin sink current	I_{CLKH}	$V_{CLK} = V_{DS}$	–	1.0	4.0	μA
CLK pin leakage current	I_{CLKL}	V_{CLK} = 0 V	–0.1	–	0.1	μA
Output Current						
OUT1, OUT2 pin output current (output form: CMOS output)						
OUT1 pin source current	I_{OUT1H}	–	–	–	–300	μA
OUT1 pin sink current	I_{OUT1L}	–	300	–	–	μA
OUT2 pin source current	I_{OUT2H}	–	–	–	–300	μA
OUT2 pin sink current	I_{OUT2L}	–	300	–	–	μA
OUT1, OUT2 pin output current (output form: Nch open-drain output)						
OUT1 pin sink current	I_{OUT1L}	–	300	–	–	μA
OUT1 pin leakage current	I_{OUT1HL}	–	–	–	0.1	μA
OUT2 pin sink current	I_{OUT2L}	–	300	–	–	μA
OUT2 pin leakage current	I_{OUT2HL}	–	–	–	0.1	μA
Delay Time						
Detection delay time	t_{DET}	–	$t_{DET} \times 0.8$	t_{DET}	$t_{DET} \times 1.2$	ms
Release delay time	t_{REL}	–	$t_{REL} \times 0.8$	t_{REL}	$t_{REL} \times 1.2$	ms
Delay Time during Self-test						
Overcharge detection delay time	t_{DETDC}	–	$t_{DET} \times 0.7$	t_{DET}	$t_{DET} \times 1.3$	ms
Overdischarge detection delay time	t_{DETDD}	–	$t_{DET} \times 0.7$	t_{DET}	$t_{DET} \times 1.3$	ms
Overcharge release delay time	t_{RELDC}	–	$t_{REL} \times 0.7$	t_{REL}	$t_{REL} \times 1.3$	ms
Overdischarge release delay time	t_{RELDD}	–	$t_{REL} \times 0.7$	t_{REL}	$t_{REL} \times 1.3$	ms

■ Test Circuit

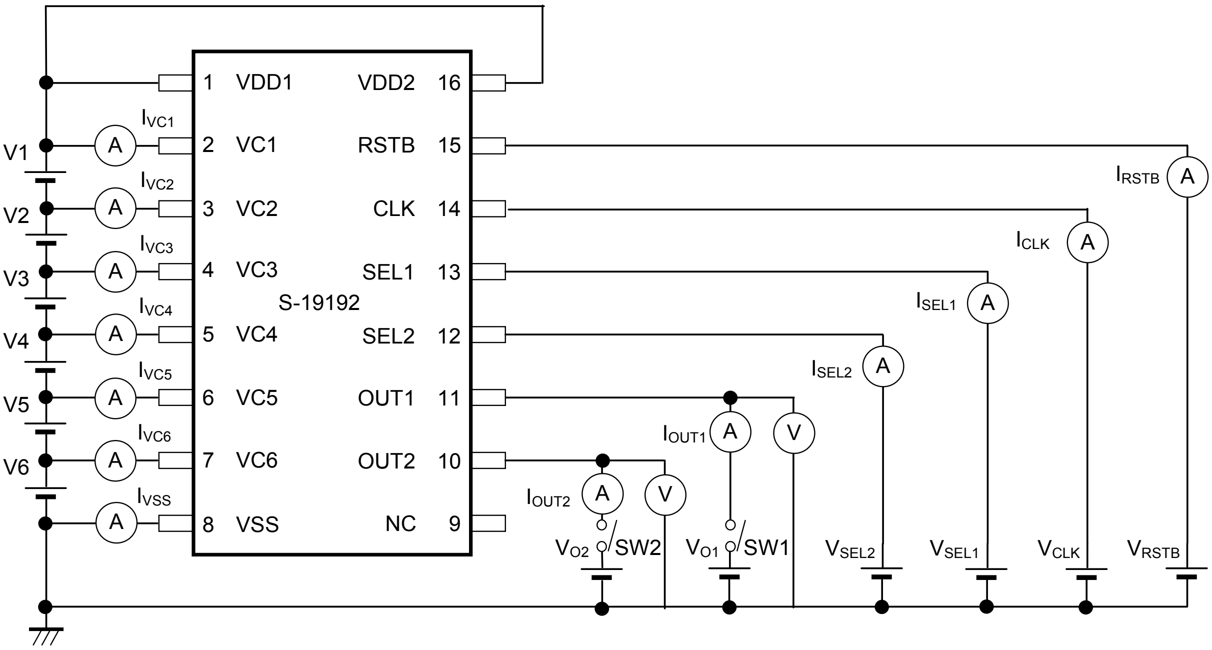


Figure 3

Remark Set SW1 and SW2 to OFF unless otherwise specified.

1. Overcharge detection voltage n (V_{CUn}), overcharge release voltage n (V_{CLn})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V and V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, the voltage V1 is gradually increased. When the OUT1 pin output switches to the detection status, the voltage V1 is defined as V_{CU1}. The voltage V1 is then gradually decreased. When the OUT1 pin output switches to the release status, the voltage V1 is defined as V_{CL1}. Similarly, V_{CUn} and V_{CLn} can be defined by changing Vn (n = 2 to 6).

2. Overdischarge detection voltage n (V_{DLn}), overdischarge release voltage n (V_{DUn})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V and V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, the voltage V1 is gradually decreased. When the OUT1 pin output switches to the detection status, V1 is defined as V_{DL1}. The voltage V1 is then gradually increased. When the OUT1 pin output switches to the release status, the voltage V1 is defined as V_{DU1}. Similarly, V_{DLn} and V_{DUn} can be defined by changing Vn (n = 2 to 6).

3. SEL1 pin voltage "H" (V_{SEL1H}), SEL1 pin voltage "L" (V_{SEL1L}), SEL2 pin voltage "H" (V_{SEL2H}), SEL2 pin voltage "L" (V_{SEL2L})

After setting V1 = V2 = V3 = V4 = V6 = V_{DU} + 0.1 V, V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, and V5 = V_{DL} − 0.1 V, the voltage V_{SEL1} is gradually increased. When the OUT1 pin output switches to the release status, the voltage V_{SEL1} is defined as V_{SEL1H}. The voltage V_{SEL1} is then gradually decreased. When the OUT1 pin output switches to the detection status, the voltage V_{SEL1} is defined as V_{SEL1L}. Similarly, V_{SEL2H} and V_{SEL2L} can be defined by changing V_{SEL2}.

4. RSTB pin voltage "H" (V_{RSTBH}), RSTB pin voltage "L" (V_{RSTBL}), CLK pin voltage "H" (V_{CLKH}), CLK pin voltage "L" (V_{CLKL})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, and V_{RSTB} = V_{DS}, the voltage V1 is increased to V_{CU} + 0.1 V. OUT1 pin output and OUT2 pin output then switch to the detection status, and after that, the voltage V_{RSTB} is gradually decreased. When the OUT2 pin output switches to the release status, the voltage V_{RSTB} is defined as V_{RSTBL}. Following the above, V_{RSTB} is gradually increased. When the OUT2 pin output switches to the detection status, the voltage V_{RSTB} is defined as V_{RSTBH}.

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, and V_{RSTB} = V_{DS}, the voltage V_{CLK} is gradually increased. When the OUT1 pin output and OUT2 pin output switch to the detection status, the voltage V_{CLK} is defined as V_{CLKH}. After that, V_{CLK} is gradually decreased. When the OUT1 pin output and OUT2 pin output switch to the release status, V_{CLK} is defined as V_{CLKL}.

5. Current consumption during operation (I_{OPE}), current consumption during overcharge (I_{OPEC}), current consumption during overdischarge (I_{OPED})

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V and V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, the VSS pin current is defined as I_{OPE}.

When V1 = V2 = V3 = V4 = V5 = V6 = V_{CU} + 0.1 V and V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, the VSS pin current is defined as I_{OPEC}.

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DL} − 0.1 V and V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, the VSS pin current is defined as I_{OPED}.

6. VCn pin current (I_{VCn}) (n = 1 to 6)

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V and V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, the VCn pin current is defined as I_{VCn}.

7. SEL1 pin sink current (I_{SEL1H}), SEL1 pin leakage current (I_{SEL1L}), SEL2 pin sink current (I_{SEL2H}), SEL2 pin leakage current (I_{SEL2L})

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V and V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, the SEL1 pin current and SEL2 pin current are defined as I_{SEL1L} and I_{SEL2L}, respectively.

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTB} = V_{CLK} = V_{SEL2} = 0 V, and V_{SEL1} = V_{DS}, the SEL1 pin current is defined as I_{SEL1H}.

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTB} = V_{CLK} = V_{SEL1} = 0 V, and V_{SEL2} = V_{DS}, the SEL2 pin current is defined as I_{SEL2H}.

8. RSTB pin sink current (I_{RSTBH}), RSTB pin leakage current (I_{RSTBL}), CLK pin sink current (I_{CLKH}), CLK pin leakage current (I_{CLKL})

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V and V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, the RSTB pin current and CLK pin current are defined as I_{RSTBL} and I_{CLKL}, respectively.

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, and V_{RSTB} = V_{DS}, the RSTB pin current is defined as I_{RSTBH}.

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTB} = V_{SEL1} = V_{SEL2} = 0 V, and V_{CLK} = V_{DS}, the CLK pin current is defined as I_{CLKH}.

9. OUT1 pin source current (I_{OUT1H}), OUT1 pin sink current (I_{OUT1L}), OUT1 pin leakage current (I_{OUT1HL}), OUT2 pin source current (I_{OUT2H}), OUT2 pin sink current (I_{OUT2L}), OUT2 pin leakage current (I_{OUT2HL})

9. 1 CMOS output, active "H"

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, V_{O1} = V_{O2} = 0.5 V, and SW1 = ON, the OUT1 pin current is I_{OUT1L}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2L}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{CU} + 0.1 V, V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, V_{RSTB} = V_{DS}, V_{O1} = V_{O2} = V_{DS} − 0.5 V, and SW1 = ON, the OUT1 pin current is I_{OUT1H}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2H}.

9. 2 CMOS output, active "L"

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, V_{O1} = V_{O2} = V_{DS} − 0.5 V, and SW1 = ON, the OUT1 pin current is I_{OUT1H}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2H}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{CU} + 0.1 V, V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, V_{RSTB} = V_{DS}, V_{O1} = V_{O2} = 0.5 V, and SW1 = ON, the OUT1 pin current is I_{OUT1L}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2L}.

9. 3 Nch open-drain output, active "H"

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, V_{O1} = V_{O2} = 0.5 V, and SW1 = ON, the OUT1 pin current is I_{OUT1L}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2L}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{CU} + 0.1 V, V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, V_{RSTB} = V_{DS}, V_{O1} = V_{O2} = V_{DS}, and SW1 = ON, the OUT1 pin current is I_{OUT1HL}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2HL}.

9. 4 Nch open-drain output, active "L"

When V1 = V2 = V3 = V4 = V5 = V6 = V_{CU} + 0.1 V, V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, V_{RSTB} = V_{DS}, V_{O1} = V_{O2} = 0.5 V, and SW1 = ON, the OUT1 pin current is I_{OUT1L}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2L}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, V_{O1} = V_{O2} = V_{DS}, and SW1 = ON, the OUT1 pin current is I_{OUT1HL}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2HL}.

10. Detection delay time (t_{DET}), release delay time (t_{REL})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTB} = V_{CLK} = V_{SEL1} = V_{SEL2} = 0 V, the voltage V4 is changed from V_{DU} + 0.1 V to V_{CU} + 1.0 V. The time interval from the V4 change until OUT1 pin output switches to the detection status is t_{DET}.
The voltage V4 is then changed from V_{CU} + 1.0 V to V_{DL} + 0.1 V. The time interval from the V4 change until OUT1 pin output switches to the release status is t_{REL}.
Subsequently, the voltage V4 is changed from V_{DL} + 0.1 V to V_{DL} − 1.0 V. The time interval from the V4 change until OUT1 pin output switches to the detection status is t_{DET}.
The voltage V4 is then changed from V_{DL} − 1.0 V to V_{CU} − 0.1 V. The time interval from the V4 change until OUT1 pin output switches to the release status is t_{REL}.

■ Standard Circuits

Connect the S-19192 Series according to the number of serial cells as shown below.

1. 6-serial cell (SEL1 = "L", SEL2 = "L")

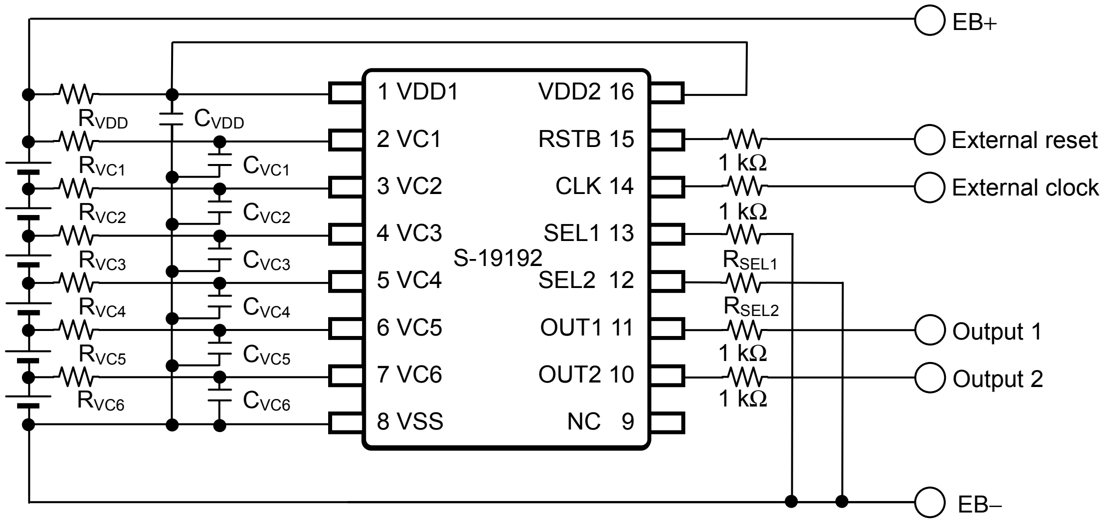


Figure 4

2. 5-serial cell (SEL1 = "L", SEL2 = "H")

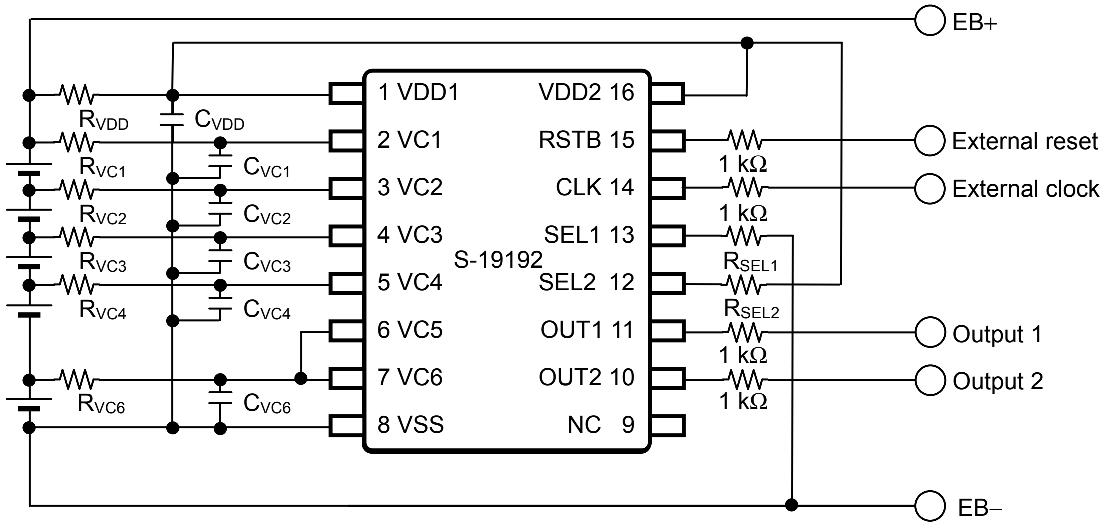


Figure 5

3. 4-serial cell (SEL1 = "H", SEL2 = "L")

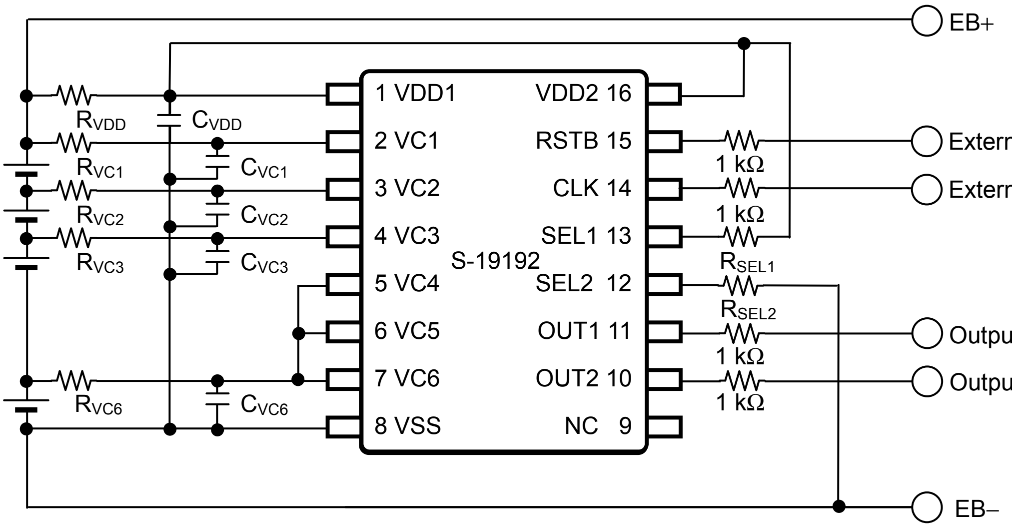


Figure 6

4. 3-serial cell (SEL1 = "H", SEL2 = "H")

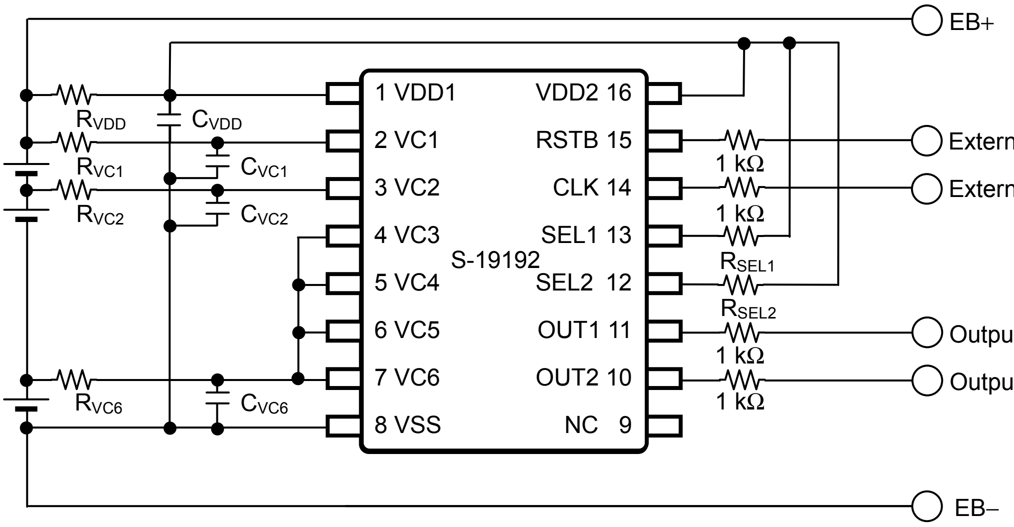


Figure 7

Table 7 Constants for External Components

Symbol	Min.	Typ.	Max.	Unit
R_{VDD}	0.5	1.0	1.0	kΩ
R_{VCn}	0.5	1.2	1.2	kΩ
R_{SEL1}, R_{SEL2}	0.5	1.0	–	kΩ
C_{VDD}	0.075	0.100	1.000	μF
C_{VCn}	0.075	0.100	1.000	μF

Caution 1. The above constants may be changed without notice.
2. The connection examples and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

Remark n = 1 to 6

■ Operation

1. Normal status

When the voltage of each of the batteries is in the range from the overcharge detection voltage n (V_{CUn}) to the overdischarge detection voltage n (V_{DLn}), and additionally, the RSTB pin input voltage (V_{RSTB}) and the CLK pin input voltage (V_{CLK}) are lower than the RSTB pin voltage "L" (V_{RSTBL}) and the CLK pin voltage "L" (V_{CLKL}), respectively, the OUT1 pin and OUT2 pin output the release signal. This is the normal status.

Remark When the OUT2 pin output is in the detection status following the initial connection with batteries, input "H" to the RSTB pin and return the input voltage to "L". S-19192 Series then returns to the normal status.

2. Overcharge status

When the voltage of any of the batteries exceeds V_{CUn} and the status continues for the detection delay time (t_{DET}) or longer, the OUT1 pin output inverts and switches to the detection status (Refer to **Figure 9**). This is the overcharge status.
When the voltage of each of the batteries falls below the overcharge release voltage n (V_{CLn}) and the status continues for the release delay time (t_{REL}) or longer, the overcharge status is released and the S-19192 Series returns to the normal status.

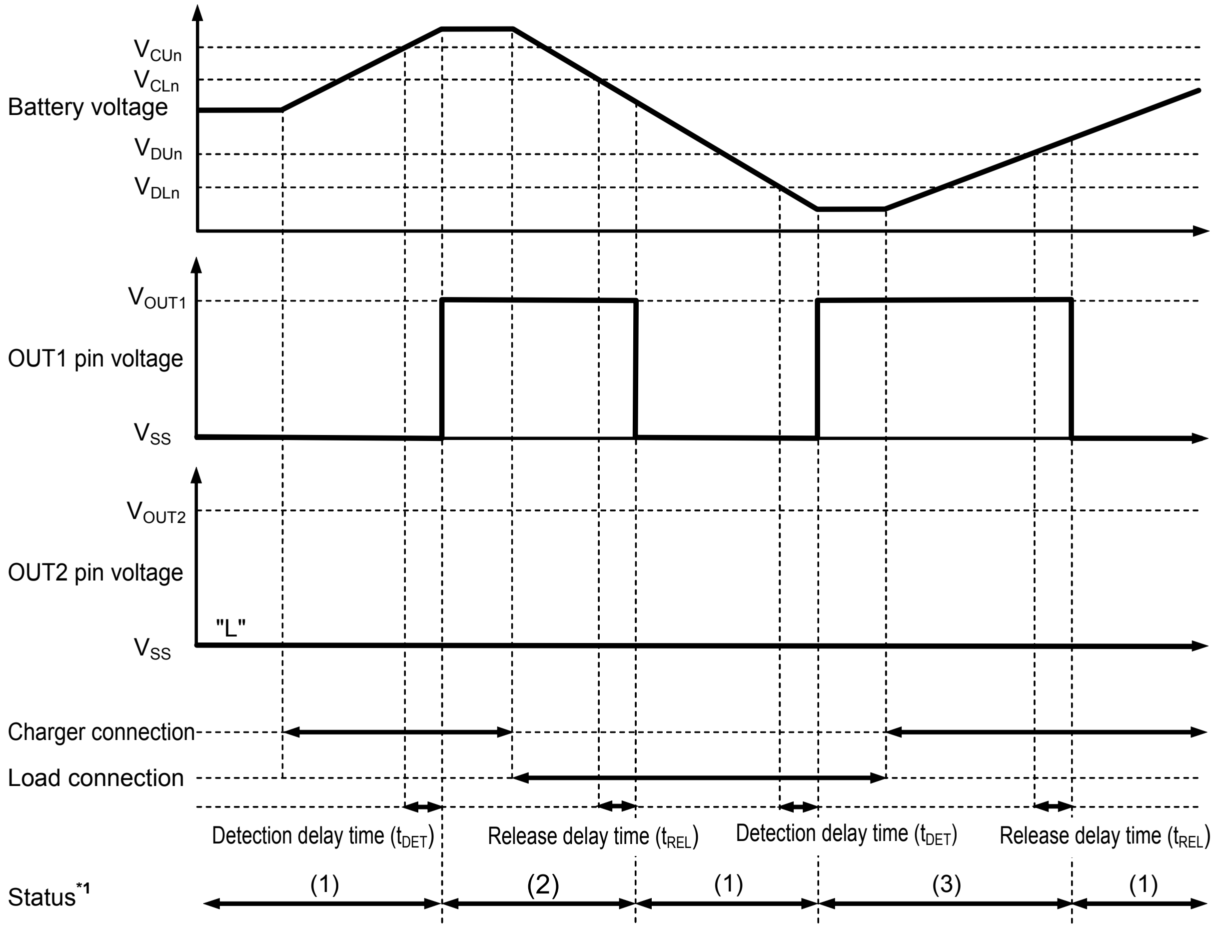
3. Overdischarge status

When the voltage of any of the batteries falls below V_{DLn} and the status continues for the detection delay time (t_{DET}) or longer, the OUT1 pin output inverts and switches to the detection status (**Refer to Figure 10**). This is the overdischarge status.
When the voltage of each of the batteries exceeds the overdischarge release voltage n (V_{DUn}) and the status continues for the release delay time (t_{REL}) or longer, the overdischarge status is released and the S-19192 Series returns to the normal status.

Remark 1. Use the S-19192 Series within the range where the power supply voltage is 6 V or more and the voltage of each of the batteries is not lower than 1 V.
2. n = 1 to 6

■ Timing Charts

1. Overcharge detection and overdischarge detection

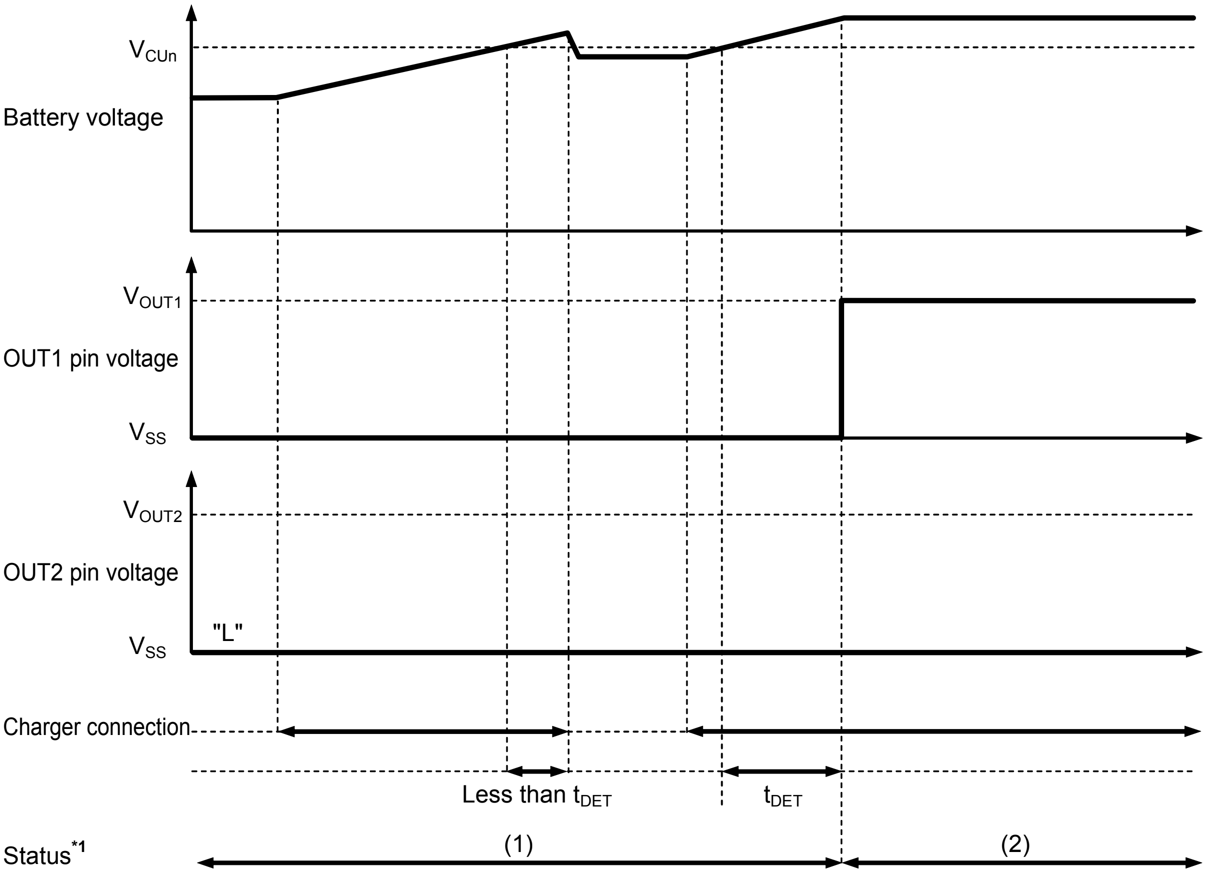


***1.** (1) : Normal status
(2) : Overcharge status
(3) : Overdischarge status

Remark 1. Refer to "■ **Self-test function**" for details of the OUT2 pin.
2. n = 1 to 6

Figure 8

2. Overcharge detection delay

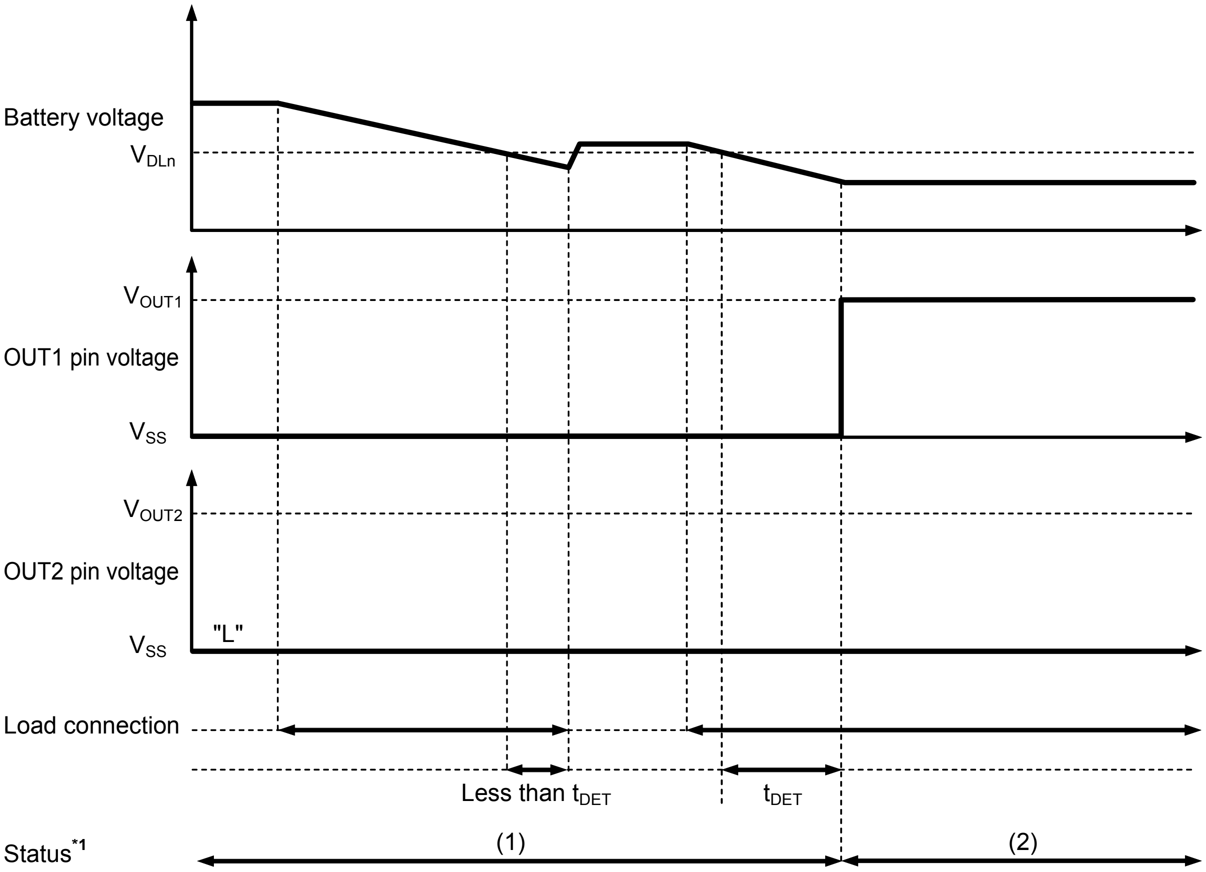


***1.** (1) : Normal status
(2) : Overcharge status

Remark 1. Refer to "■ **Self-test function**" for details of the OUT2 pin.
2. n = 1 to 6

Figure 9

3. Overdischarge detection delay



***1.** (1) : Normal status
(2) : Overdischarge status

Remark 1. Refer to "■ **Self-test function**" for details of the OUT2 pin.
2. n = 1 to 6

Figure 10

■ Self-test Function

The S-19192 Series has a self-test function to confirm overcharge and overdischarge detection operations. Due to the self-test function, a current flows in internal voltage-dividing resistors, comparator input voltage changes, and then the S-19192 Series spuriously switches to the overcharge or overdischarge status. It is possible to confirm whether the S-19192 Series normally detects the overcharge and overdischarge or not by monitoring the OUT1 pin and OUT2 pin output signals.

1. When delay time shortening function during self-test is "available"

Delay time during the self-test can be shortened by selecting a product with the delay time shortening function during the self-test. In this case, each delay time is specified as follows.

- Overcharge detection delay time (t_{DETDC}) : Approximately 1/64
- Overdischarge detection delay time (t_{DETDD}) : Approximately 1/64
- Overcharge release delay time (t_{RELDC}) : t_{REL}
- Overdischarge release delay time (t_{RELDD}) : Fixed to 4 ms

The self-test is not normally performed under the following conditions.
- When the S-19192 Series is in the overcharge or overdischarge status
- When the power supply voltage is 6 V or lower

Remark When the OUT2 pin output is in the detection status following the initial connection with batteries, input "H" to the RSTB pin and return the input voltage to "L". The S-19192 Series then returns to the normal status. In order to initialize it hereafter, input voltages to the RSTB pin by the same procedure.

2. Description of pins

2. 1 RSTB pin

When "H" is input to the RSTB pin, the self-test starts. When "L" is input, the S-19192 Series returns to the normal operation.

2. 2 CLK pin

When "H" is input to the RSTB pin and clock signals are input to the CLK pin, the following diagnostics are performed.

1st clock : Performs overcharge comparator 1 (OC1) diagnostics
2nd clock : Performs overdischarge comparator 1 (OD1) diagnostics
3rd to 12th clocks : Performs overcharge comparator n (OCn) diagnostics at the 2n – 1th clock for the clock signal input to the CLK pin (Refer to **Figure 12** and **Figure 13**)
Performs overdischarge comparator n (ODn) diagnostics at the 2nth clock for the clock signal input to the CLK pin (Refer to **Figure 14** and **Figure 15**)
13th clock : Does not perform any diagnostics, which makes it possible to determine at which clock diagnostics are being performed.
14th and 15th clocks : Performs abnormal high voltage and low voltage diagnostics for the LV regulator (Refer to **Figure 11**)

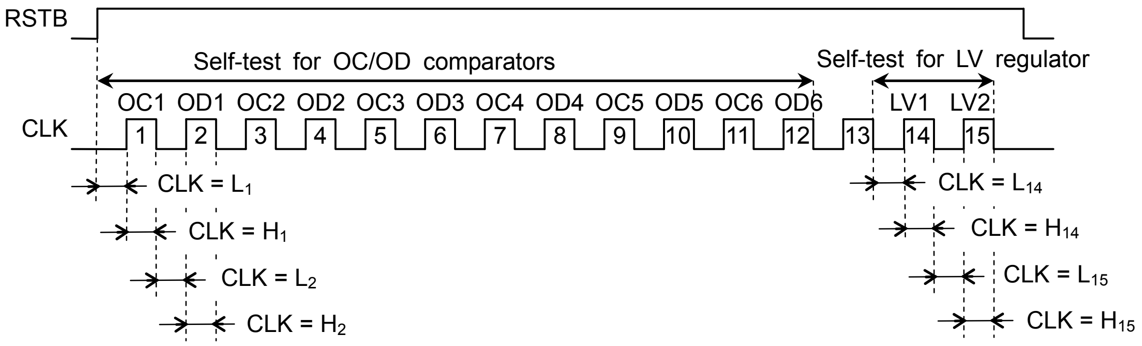


Figure 11

Remark n = 1 to 6

2. 3 OUT1 pin

When "H" is input to the RSTB pin and clock signals are input to the CLK pin, the OUT1 pin output is as follows.

1st clock : Switches to the detection status once the self-test overcharge detection delay time (t_{DETDC}) elapses after a clock signal rises
Switches to the release status once the self-test overcharge release delay time (t_{RELDC}) elapses after a clock signal falls
2nd clock : Switches to the detection status once the self-test overdischarge detection delay time (t_{DETDD}) elapses after a clock signal rises
Switches to the release status once the self-test overdischarge release delay time (t_{RELDD}) elapses after a clock signal falls
3rd to 12th clocks : Repeat the same operations as the 1st and 2nd clocks (Refer to **Figure 17**)
13th and successive clocks : Maintains the release status

2. 4 OUT2 pin

2. 4. 1 Operation when there is no failure

When clock signals are input to the CLK pin after "H" is input to the RSTB pin, the OUT2 pin output operates the same as the OUT1 pin output for the 1st to 13th clocks. The OUT2 pin output switches to the release status when "L" is input to the CLK pin for the 14th and 15th clocks. Alternatively, the OUT2 pin output switches to the detection status when "H" is input to the CLK pin (Refer to **Figure 17**).

2. 4. 2 Operation when there is an overcharge comparator n (OCn) or overdischarge comparator n (ODn) failure

When a comparator failure is detected, the OUT2 pin output switches to the detection status after a clock signal falls. The detection status continues until "L" is input to the RSTB pin and "H" is input again (Refer to **Figure 18**, **Figure 21**, and **Figure 23**).

Remark n = 1 to 6

2. 4. 3 Operation when there is an LV regulator failure

When an LV regulator failure is detected, the OUT2 pin output switches to the detection status after the 13th clock signal falls. The detection status continues until "L" is input to the RSTB pin and H" is input again (Refer to **Figure 19**).

3. Block diagrams of self-test function

3. 1 Self-test performed for overcharge comparators (Overcharge detection function)

(1) When overcharge is not detected

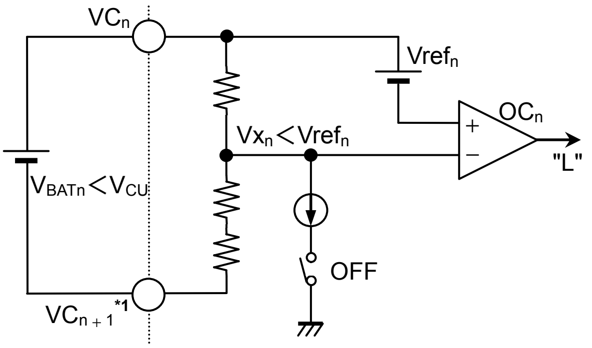


Figure 12 When self-test is not performed (RSTB = "L", CLK = "L")

(2) When overcharge is detected during self-test

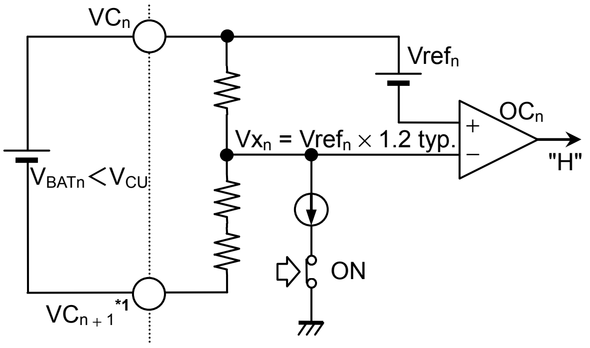


Figure 13 When self-test is performed (RSTB = "H", CLK = "H_{2n-1}")

3. 2 Self-test performed for overdischarge comparators (overdischarge detection function)

(1) When overdischarge is not detected

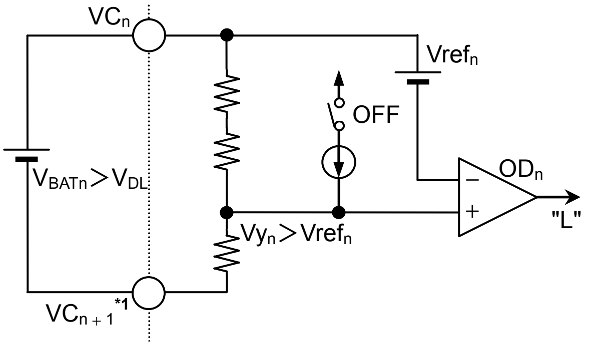


Figure 14 When self-test is not performed (RSTB = "L", CLK = "L")

(2) When overdischarge is detected during self-test

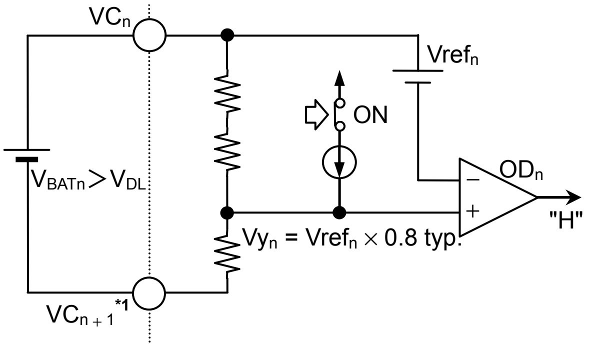
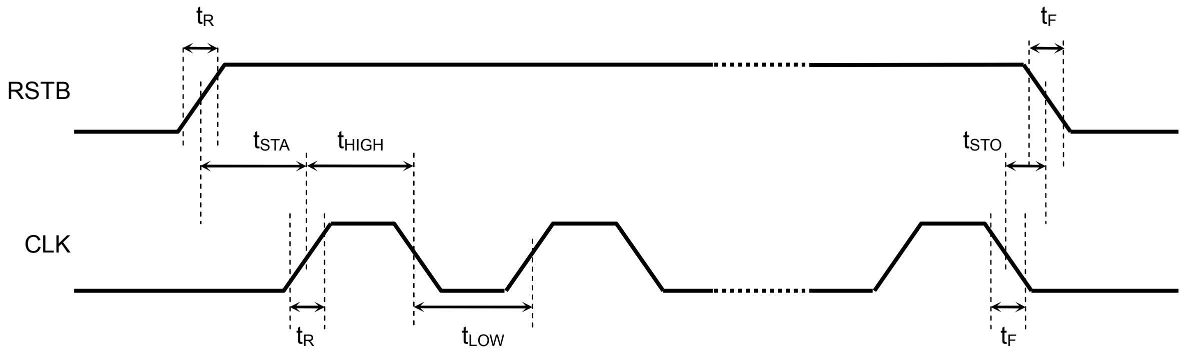


Figure 15 When self-test is performed (RSTB = "H", CLK = "H_{2n}")

***1.** When n = 6, it is VSS pin.

Remark n = 1 to 6

4. Timing charts during self-test



Remark f_{CLK} = 2.5 Hz max. ($t_{CLK} = t_{HIGH} + t_{LOW}$)
t_{LOW}, t_{HIGH}, t_{STA}, t_{STO} = 200 ms min.
t_R, t_F = 300 ns max.

Figure 16

5. Example of self-test operation

5. 1 6-serial cell

5. 1. 1 When there is no failure

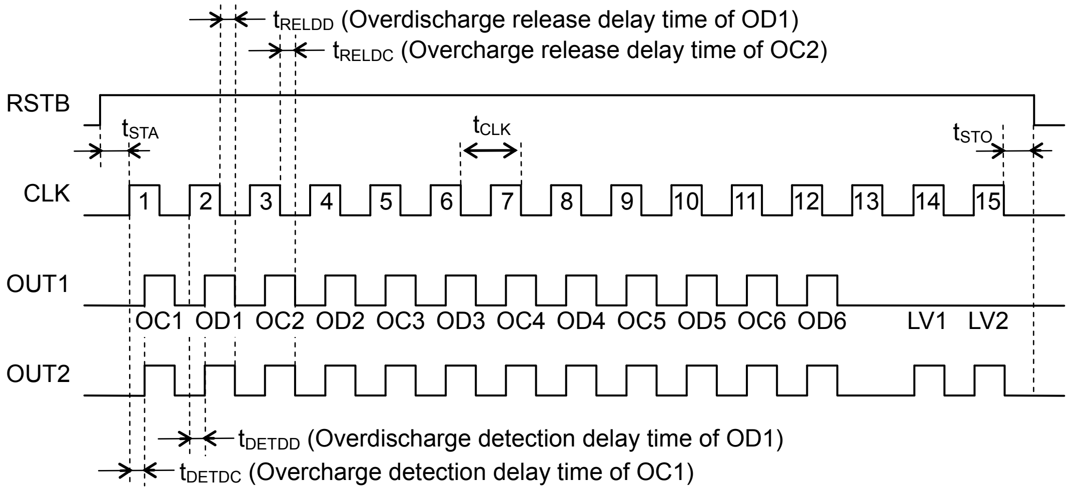


Figure 17

5. 1. 2 When there is an overcharge comparator failure (OC3)

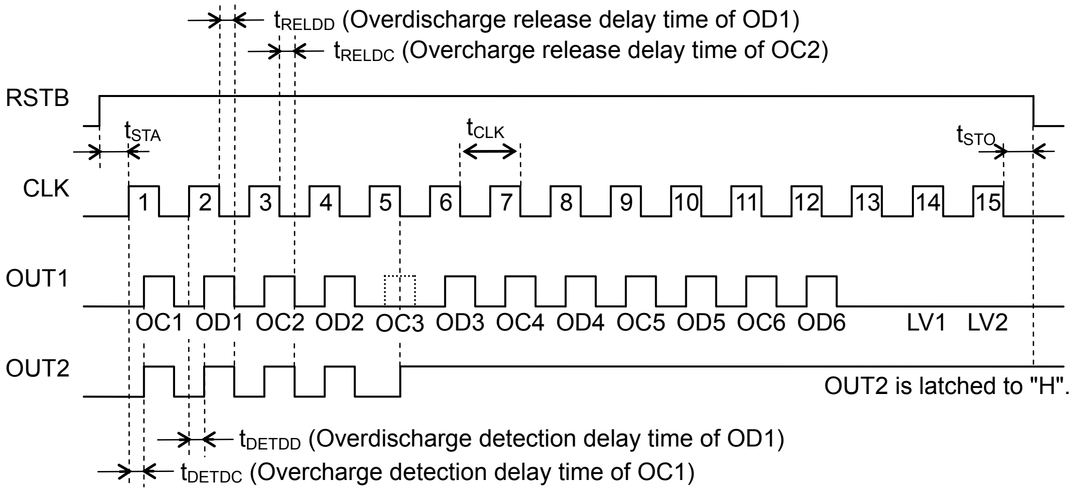


Figure 18

5. 1. 3 When there is an LV regulator failure

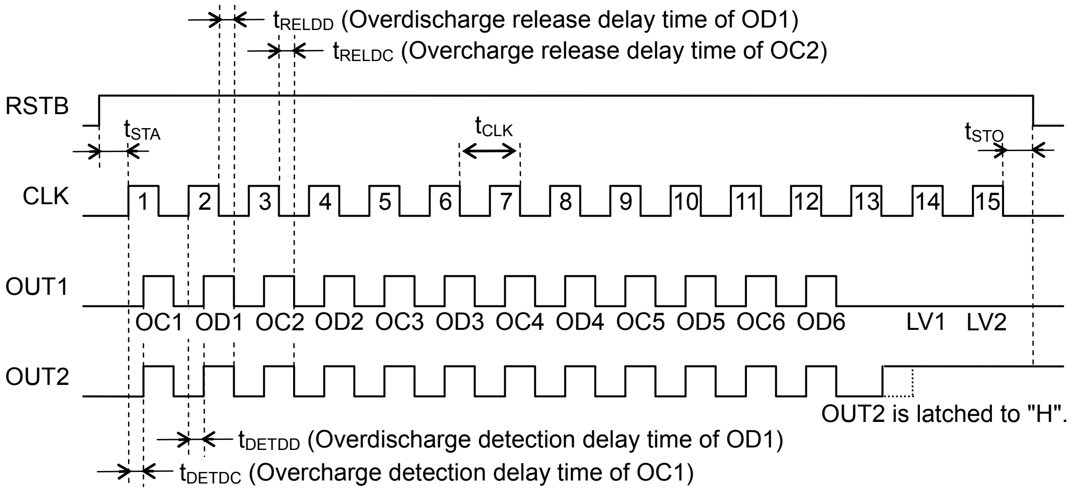


Figure 19

5. 2 3-serial cell

5. 2. 1 When there is no failure

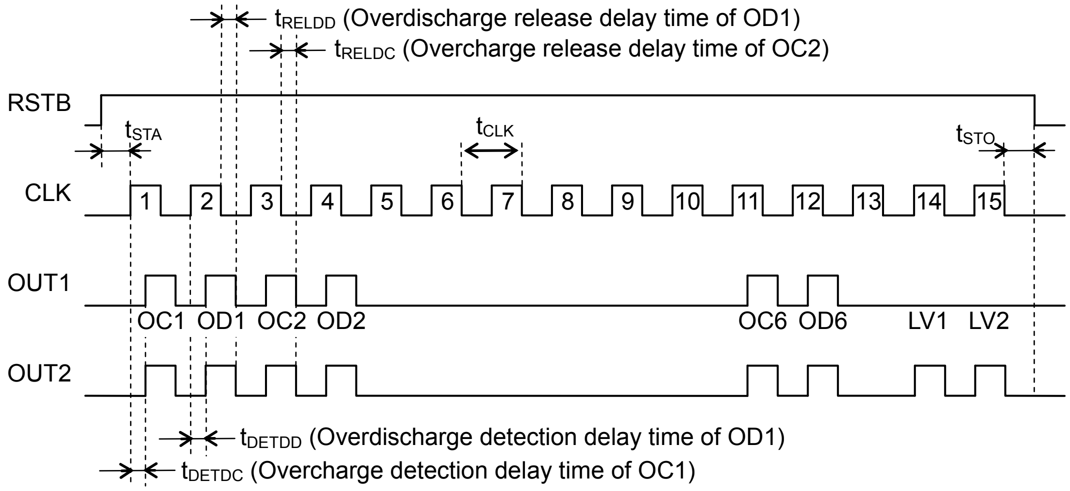


Figure 20

5. 2. 2 When there is an overdischarge comparator failure (OD2)

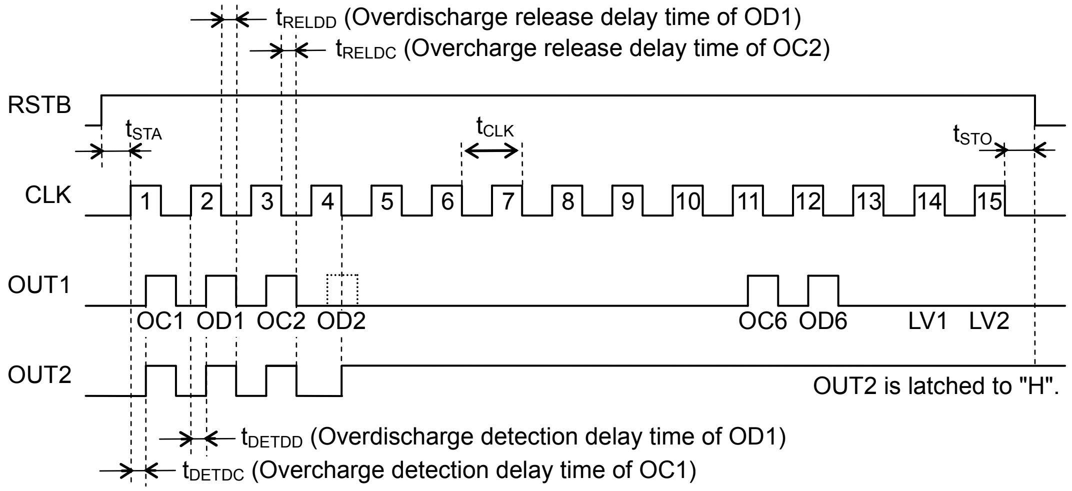


Figure 21

5. 3 6-serial cell (Self-test interruption)

5. 3. 1 When there is no failure

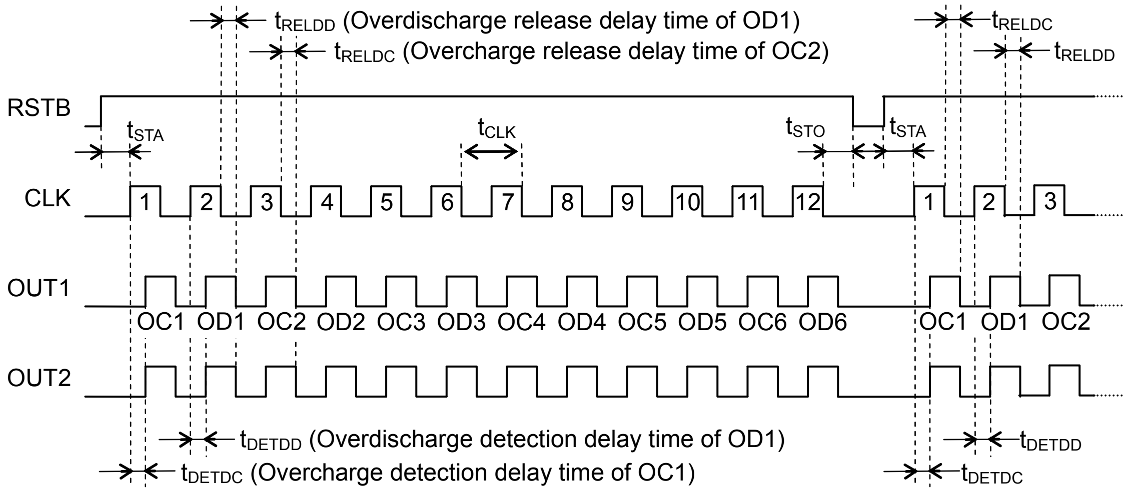


Figure 22

5. 3. 2 When there is an overcharge comparator failure (OC3)

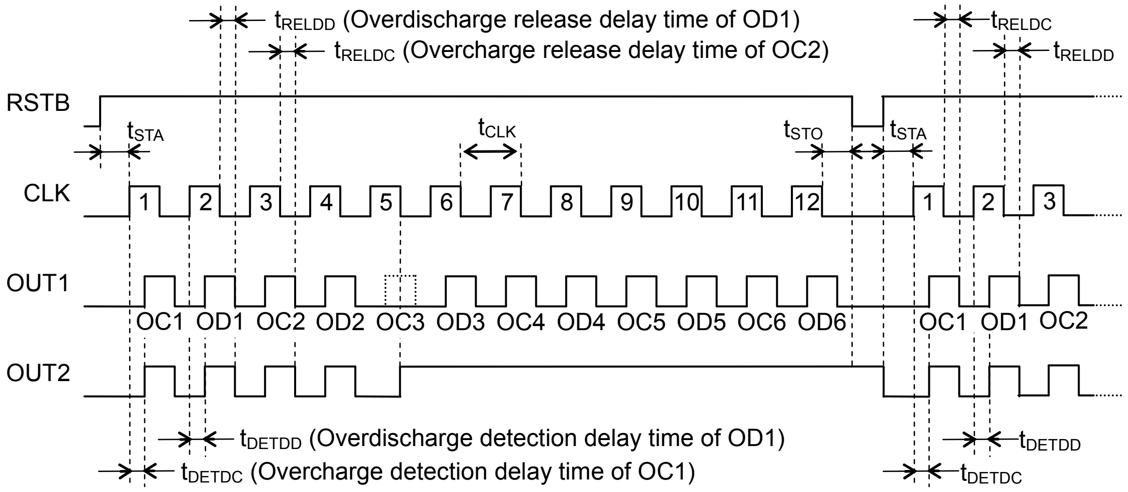


Figure 23

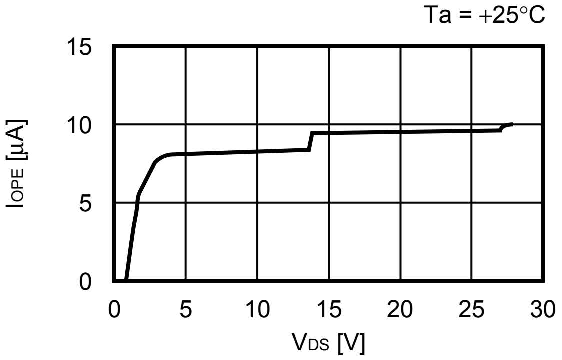
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Batteries can be connected in any order; however, there may be cases when the OUT2 pin output is in the detection status after batteries are connected. In this case, the S-19192 Series returns to the normal status when inputting "H" to the RSTB pin and returning the input voltage to "L".
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

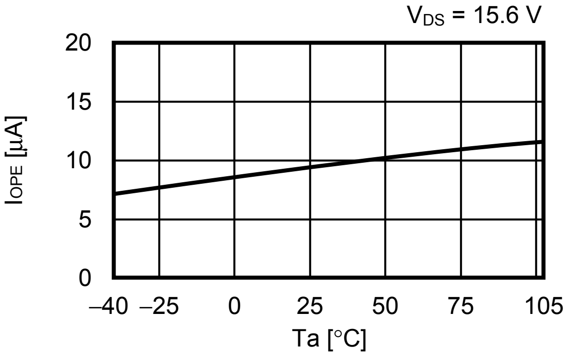
■ Characteristics (Typical Data)

1. Current consumption

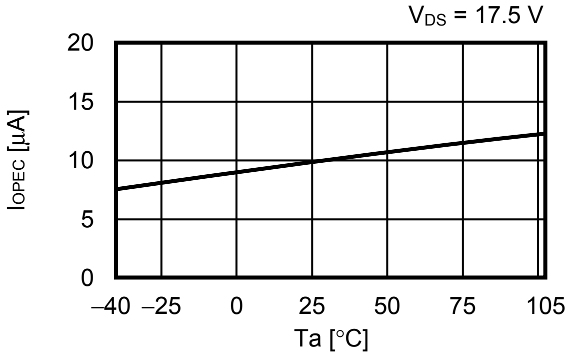
1. 1 I_{OPE} vs. V_{DS}



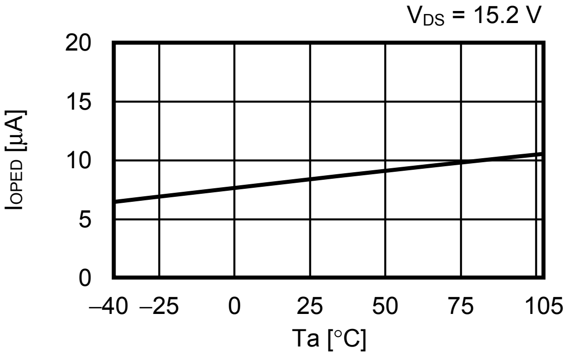
1. 2 I_{OPE} vs. Ta



1. 3 I_{OPEC} vs. Ta

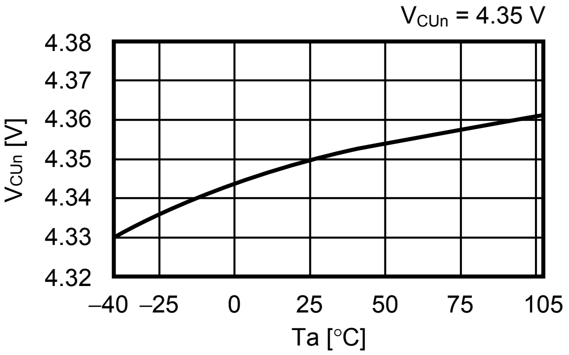


1. 4 I_{OPED} vs. Ta

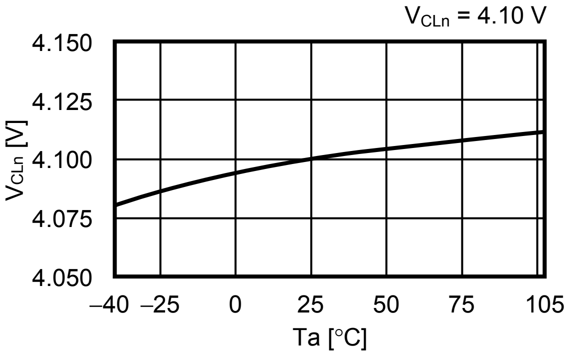


2. Detection voltage, release voltage

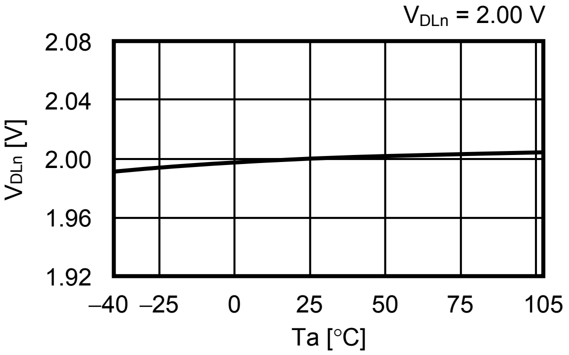
2. 1 V_{CUn} vs. Ta



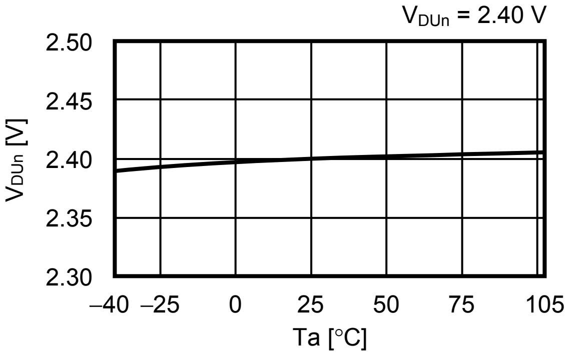
2. 2 V_{CLn} vs. Ta



2. 3 V_{DLn} vs. Ta

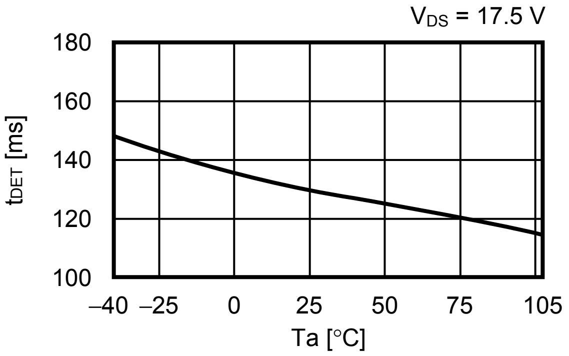


2. 4 V_{DUn} vs. Ta

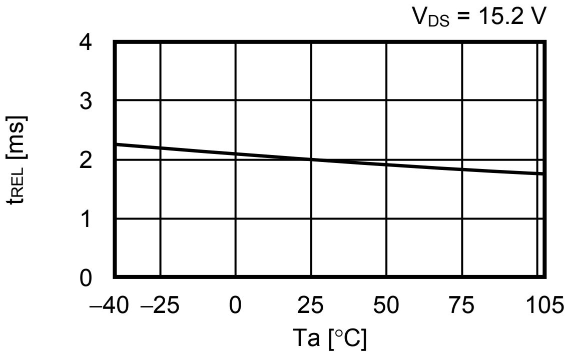


3. Delay time

3. 1 t_{DET} vs. Ta



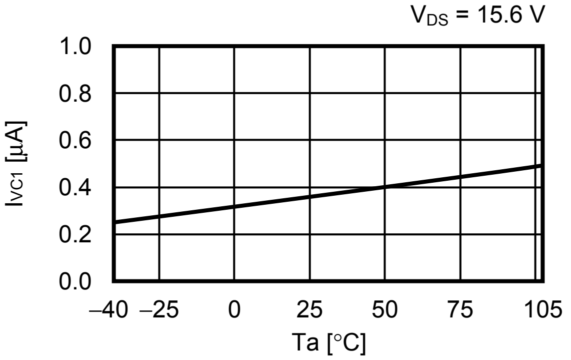
3. 2 t_{REL} vs. Ta



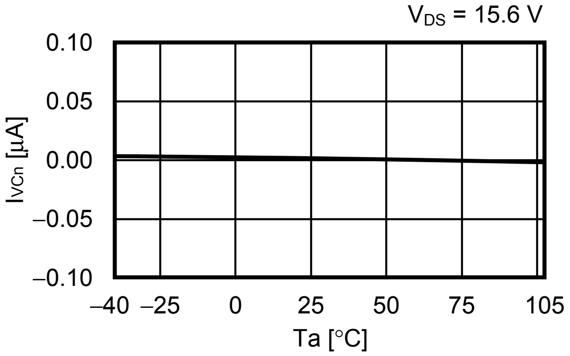
Remark n = 1 to 6

4. Input current

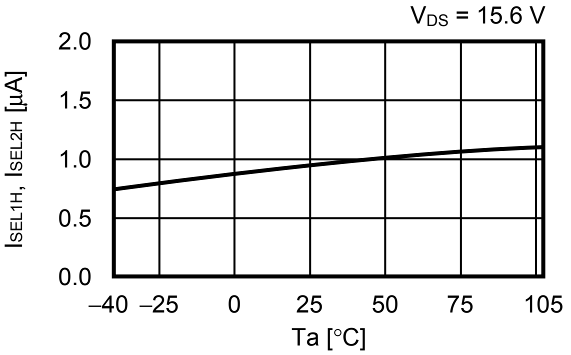
4. 1 I_{VC1} vs. Ta



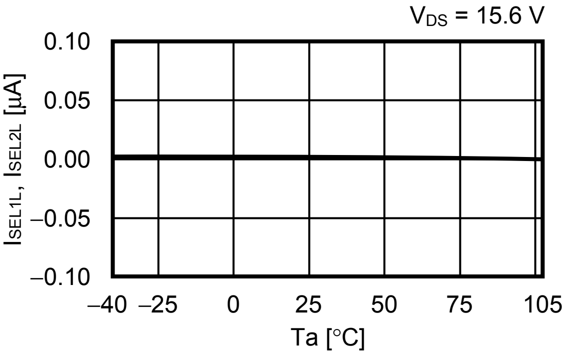
4. 2 I_{VCn} vs. Ta



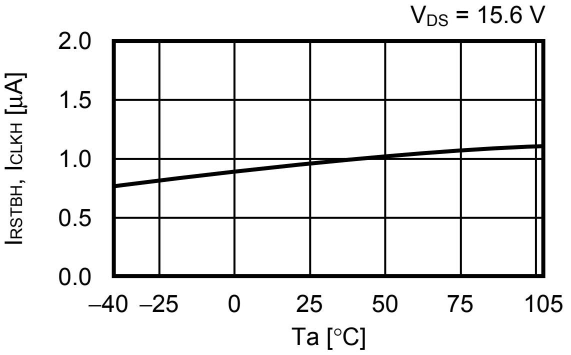
4. 3 I_{SEL1H}, I_{SEL2H} vs. Ta



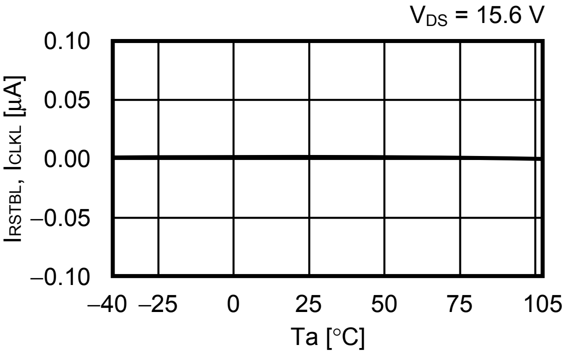
4. 4 I_{SEL1L}, I_{SEL2L} vs. Ta



4. 5 I_{RSTBH}, I_{CLKH} vs. Ta



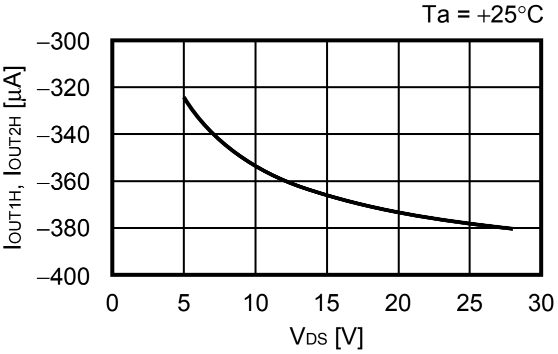
4. 6 I_{RSTBL}, I_{CLKL} vs. Ta



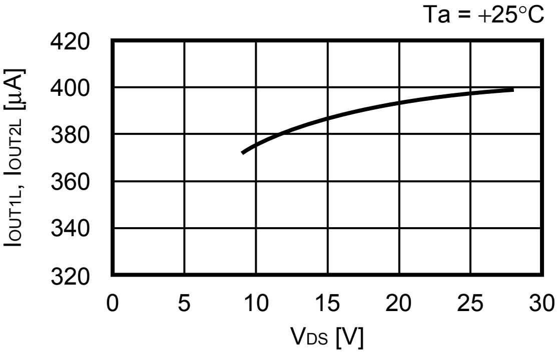
Remark n = 2 to 6

5. Output current

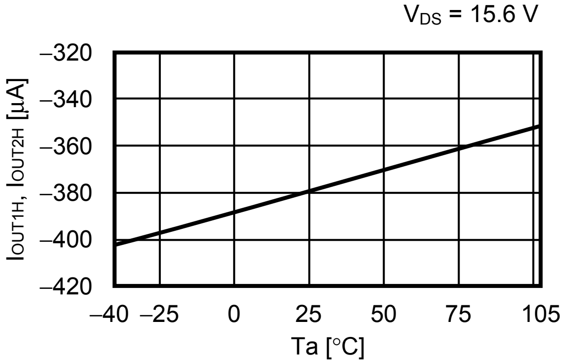
5. 1 I_{OUT1H}, I_{OUT2H} vs. V_{DS}



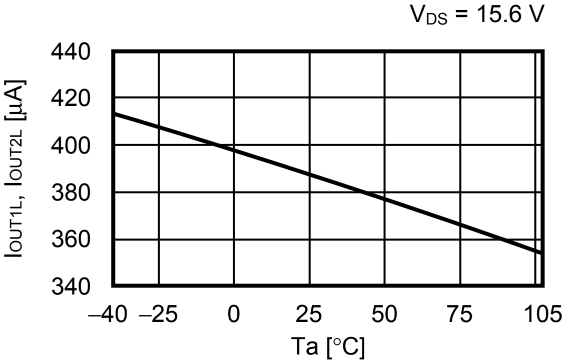
5. 2 I_{OUT1L}, I_{OUT2L} vs. V_{DS}



5. 3 I_{OUT1H}, I_{OUT2H} vs. Ta

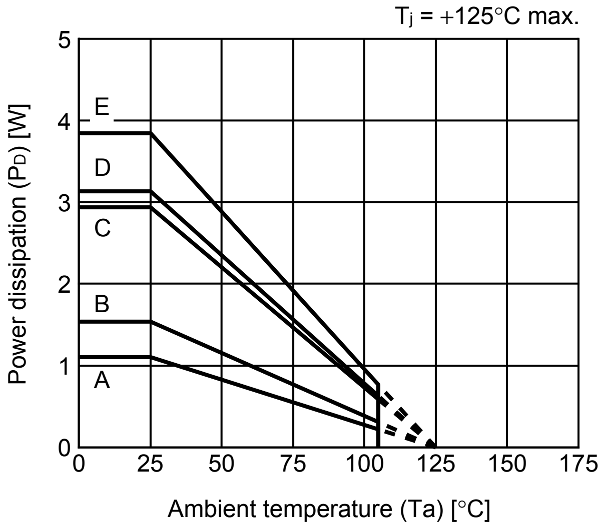


5. 4 I_{OUT1L}, I_{OUT2L} vs. Ta



■ Power Dissipation

HTSSOP-16

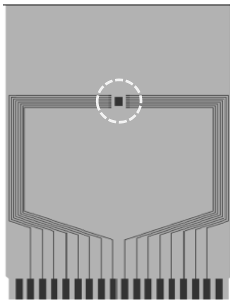


Board	Power Dissipation (P_D)
A	1.10 W
B	1.54 W
C	2.94 W
D	3.13 W
E	3.85 W

HTSSOP-16 Test Board

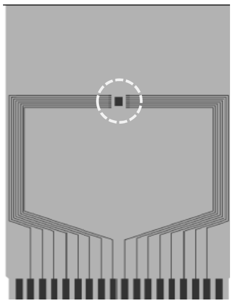
◌ IC Mount Area

(1) Board A



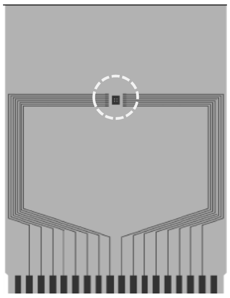
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B

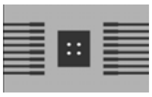


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



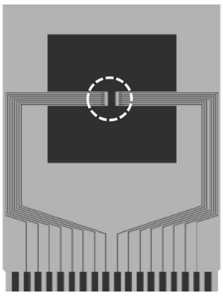
enlarged view

No. HTSSOP16-A-Board-SD-1.0

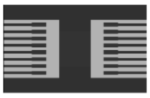
HTSSOP-16 Test Board

◌ IC Mount Area

(4) Board D

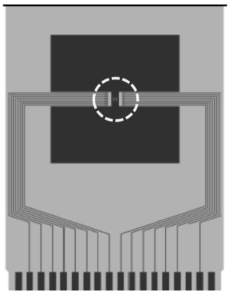


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

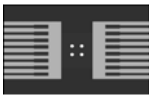


enlarged view

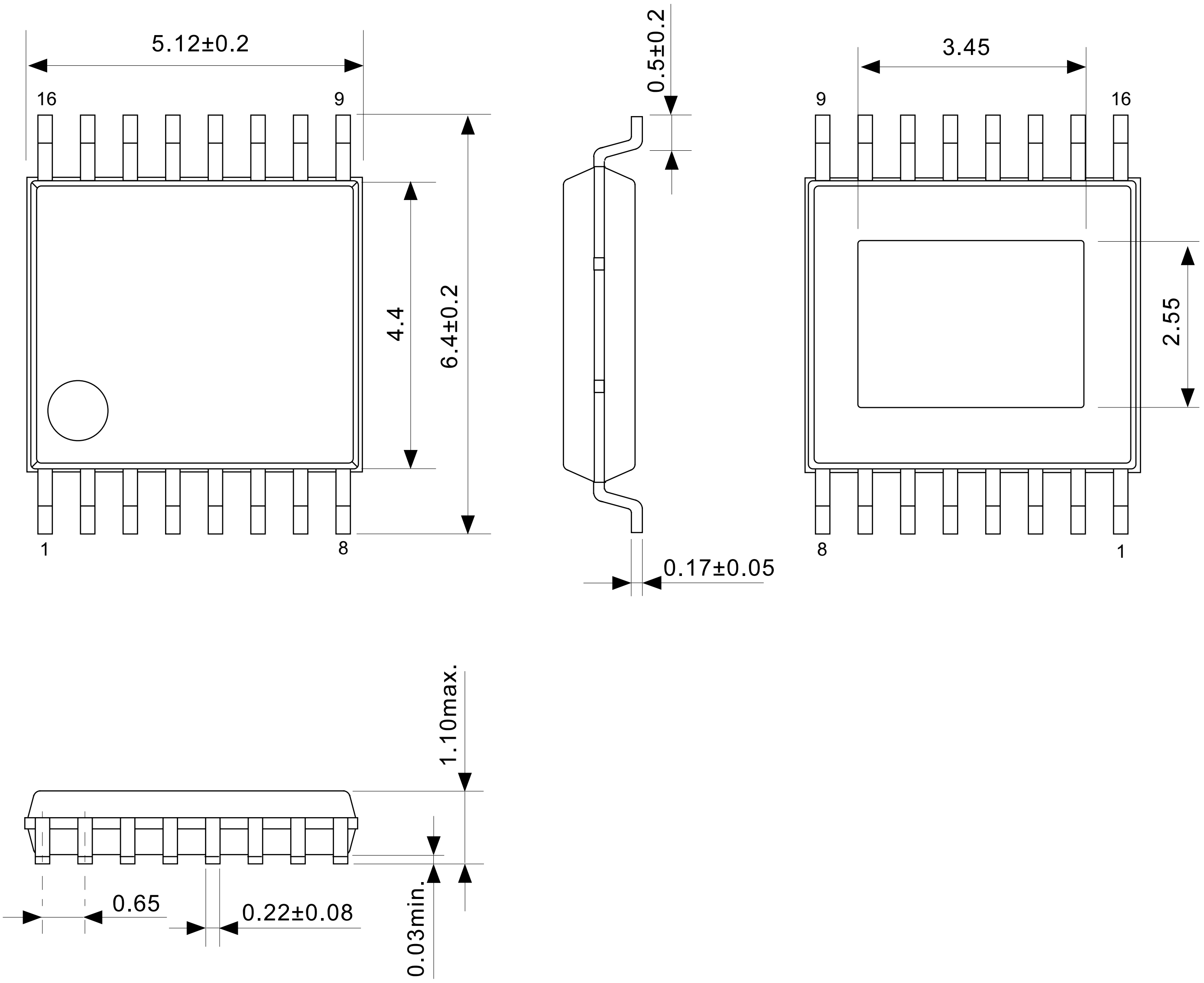
(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



enlarged view



No. FR016-A-P-SD-1.0

TITLE	HTSSOP16-A-PKG Dimensions
No.	FR016-A-P-SD-1.0
ANGLE	
UNIT	mm

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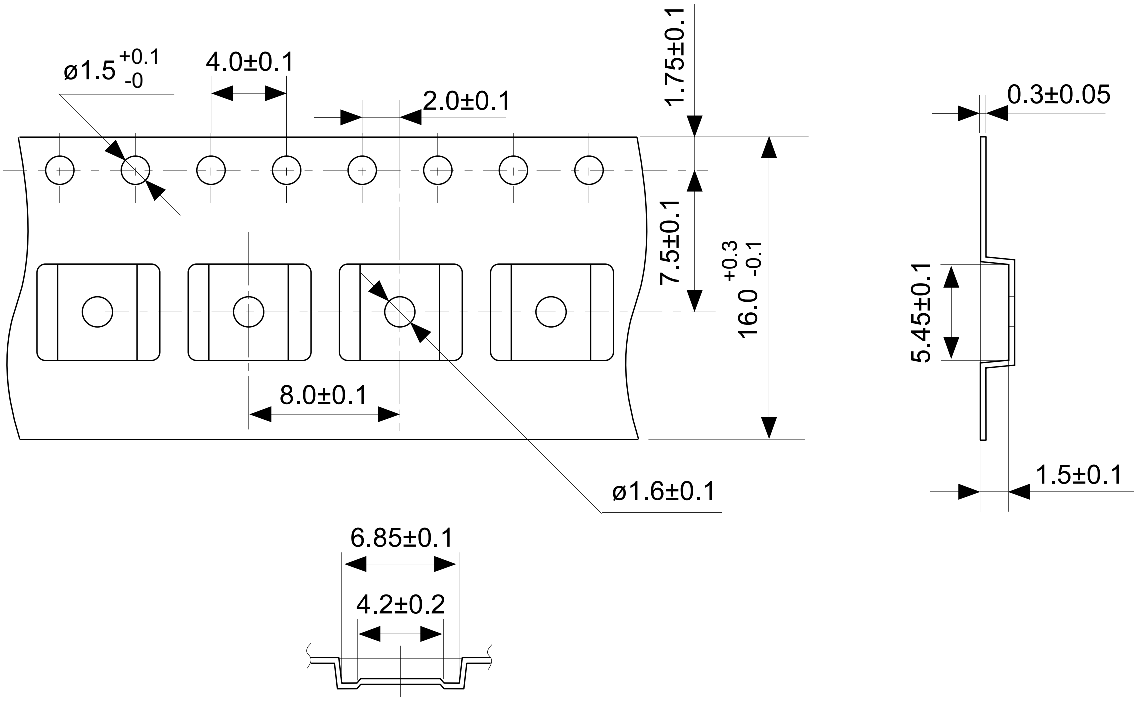

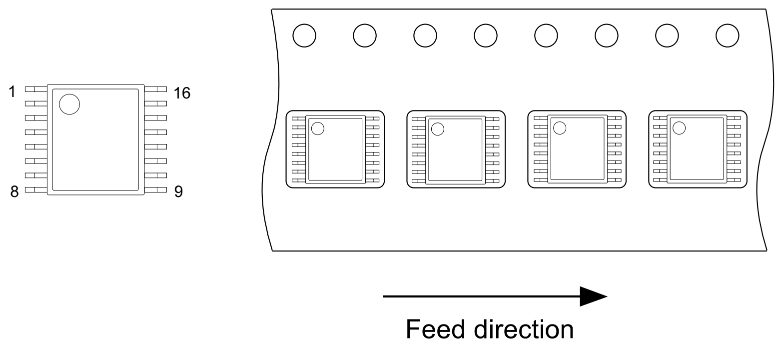

No. FR016-A-C-SD-1.0

TITLE	HTSSOP16-A-Carrier Tape
No.	FR016-A-C-SD-1.0
ANGLE	
UNIT	mm

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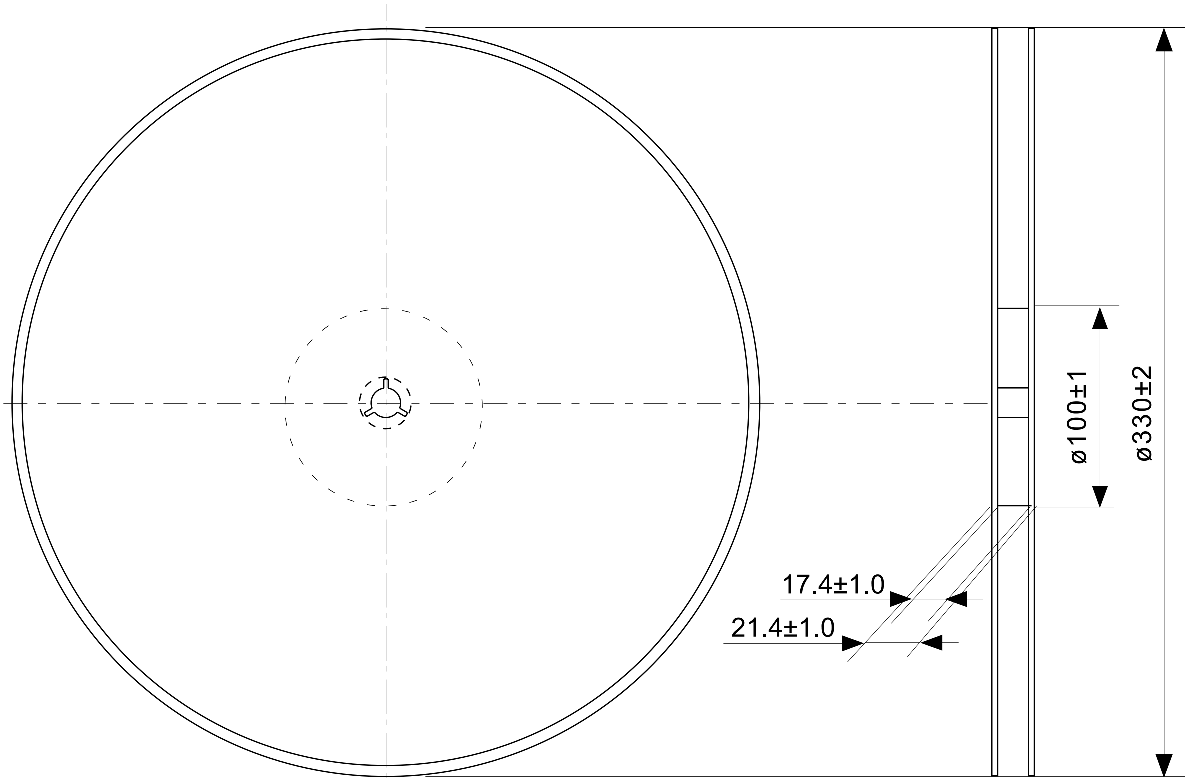
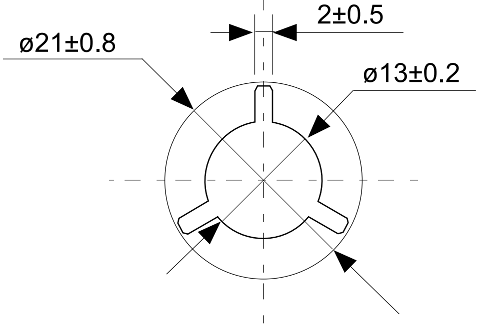


Enlarged drawing in the central part



No. FR016-A-R-SD-1.0

TITLE	HTSSOP16-A- Reel		
No.	FR016-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		

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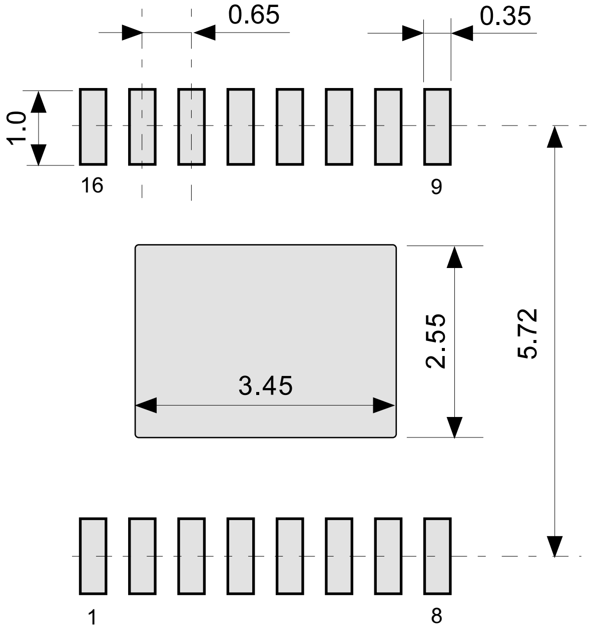

No. FR016-A-L-SD-1.0

TITLE	HTSSOP16-A -Land Recommendation
No.	FR016-A-L-SD-1.0
ANGLE	
UNIT	mm

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