S-19312 Series

AUTOMOTIVE, 125°C OPERATION, 36 V INPUT, 400 mA VOLTAGE REGULATOR WITH RESET FUNCTION

www.ablicinc.com

Rev.1.0_01

The S-19312 Series, developed by using high-withstand voltage CMOS technology, is a positive voltage regulator with the reset function, which has high-withstand voltage and high-accuracy output voltage. This IC has a built-in low on-resistance output transistor which provides a small dropout voltage and a large output current. Also, a built-in overcurrent protection circuit to limit overcurrent of the output transistor and a built-in thermal shutdown circuit to limit heat are included.
High heat radiation TO-252-5S(A) and HSOP-8A packages enable high-density mounting.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.**

■ Features

Regulator block

- Output voltage: 3.0 V to 5.3 V, selectable in 0.1 V step
- Input voltage: 4.0 V to 36.0 V
- Output voltage accuracy: ±2.0% (T_j = −40°C to +150°C)
- Dropout voltage: 120 mV typ. (5.0 V output product, I_{OUT} = 100 mA)
- Output current: Possible to output 400 mA (V_{IN} = $V_{OUT(S)}$ + 1.0 V)*1
- Input and output capacitors: A ceramic capacitor of 2.2 μF or more can be used.
- Ripple rejection: 70 dB typ. (f = 100 Hz)
- Built-in overcurrent protection circuit: Limits overcurrent of output transistor.
- Built-in thermal shutdown circuit: Detection temperature 170°C typ.

Detector block

- Detection voltage: 2.6 V to 5.0 V, selectable in 0.1 V step
- Detection voltage accuracy: ±100 mV (T_j = −40°C to +150°C)
- Hysteresis width: 0.12 V min.
- Release delay time: 18 ms typ. (C_{DLY} = 47 nF)
- Output form: Nch open-drain output (Built-in pull-up resistor)

Overall

- Current consumption: During operation: 60 μA typ., 95 μA max. (T_j = −40°C to +150°C)
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*2

***1.** Please make sure that the loss of the IC will not exceed the power dissipation when the output current is large.
***2.** Contact our sales office for details.

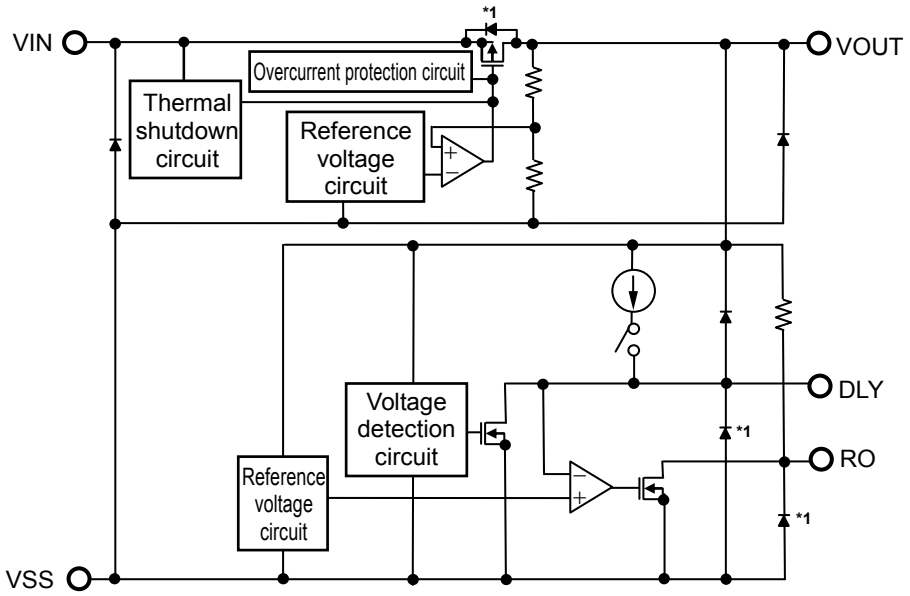
■ Applications

- Constant-voltage power supply and reset circuit for automotive electric component
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

■ Packages

- TO-252-5S(A)
- HSOP-8A

■ Block Diagram



***1.** Parasitic diode

Figure 1

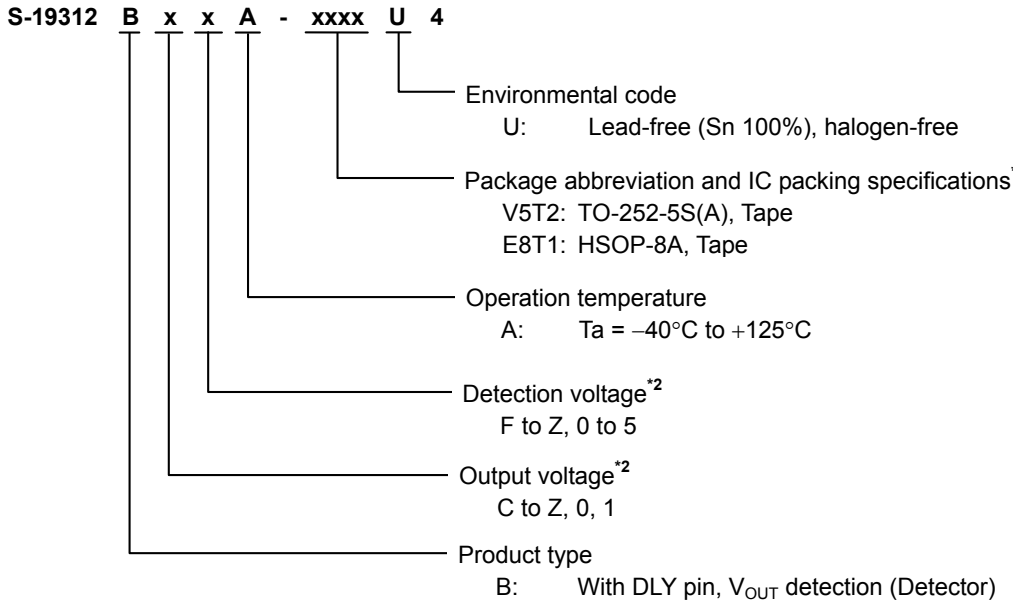
■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

Users can select the output voltage and detection voltage for the S-19312 Series. Refer to "**1. Product name**" regarding the contents of product name, "**3. Packages**" regarding the package drawings and "**4. Product name list**" for details of product names.

1. Product name



***1.** Refer to the tape drawing.
***2.** Refer to "**2. Product option list**".

2. Product option list

2. 1 Output voltage

Set Output Voltage	Symbol
5.3 V	C
5.2 V	D
5.1 V	E
5.0 V	F
4.9 V	G
4.8 V	H
4.7 V	J
4.6 V	K
4.5 V	L
4.4 V	M
4.3 V	N
4.2 V	P

Set Output Voltage	Symbol
4.1 V	Q
4.0 V	R
3.9 V	S
3.8 V	T
3.7 V	U
3.6 V	V
3.5 V	W
3.4 V	X
3.3 V	Y
3.2 V	Z
3.1 V	0
3.0 V	1

2. 2 Detection voltage

Set Detection Voltage	Symbol
5.0 V	F
4.9 V	G
4.8 V	H
4.7 V	J
4.6 V	K
4.5 V	L
4.4 V	M
4.3 V	N
4.2 V	P
4.1 V	Q
4.0 V	R
3.9 V	S
3.8 V	T

Set Detection Voltage	Symbol
3.7 V	U
3.6 V	V
3.5 V	W
3.4 V	X
3.3 V	Y
3.2 V	Z
3.1 V	0
3.0 V	1
2.9 V	2
2.8 V	3
2.7 V	4
2.6 V	5

Remark Set output voltage ≥ Set detection voltage + 0.3 V

3. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TO-252-5S(A)	VA005-A-P-SD	VA005-A-C-SD	VA005-A-R-SD	VA005-A-L-SD
HSOP-8A	FH008-A-P-SD	FH008-A-C-SD	FH008-A-R-SD	FH008-A-L-SD

4. Product name list

Table 2

Output Voltage	Detection Voltage	TO-252-5S(A)	HSOP-8A
3.3 V ± 2.0%	2.9 V ± 0.1 V	S-19312BY2A-V5T2U4	S-19312BY2A-E8T1U4
5.0 V ± 2.0%	2.9 V ± 0.1 V	S-19312BF2A-V5T2U4	S-19312BF2A-E8T1U4
5.0 V ± 2.0%	4.2 V ± 0.1 V	S-19312BFPA-V5T2U4	S-19312BFPA-E8T1U4
5.0 V ± 2.0%	4.6 V ± 0.1 V	S-19312BFKA-V5T2U4	S-19312BFKA-E8T1U4

Remark Please contact our sales office for products with specifications other than the above.

■ Pin Configurations

1. TO-252-5S(A)

Top view

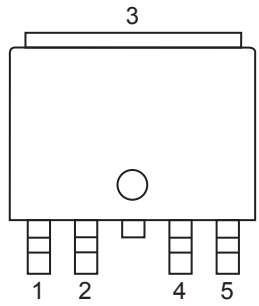


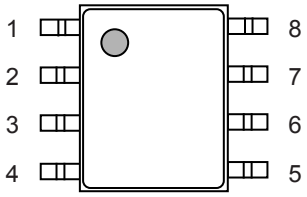
Figure 2

Table 3

Pin No.	Symbol	Description
1	VOUT	Voltage output pin (Regulator block)
2	DLY	Connection pin for delay time adjustment capacitor
3	VSS	GND pin
4	RO	Reset output pin
5	VIN	Voltage input pin (Regulator block)

2. HSOP-8A

Top view



Bottom view

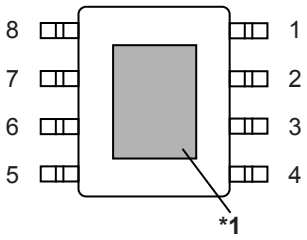


Figure 3

Table 4

Pin No.	Symbol	Description
1	VOUT	Voltage output pin (Regulator block)
2	NC*2	No connection
3	VSS	GND pin
4	DLY	Connection pin for delay time adjustment capacitor
5	RO	Reset output pin
6	NC*2	No connection
7	NC*2	No connection
8	VIN	Voltage input pin (Regulator block)

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.

***2.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 5

(T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
VIN pin voltage	V_{IN}	V_{SS} − 0.3 to V_{SS} + 45.0	V
VOUT pin voltage	V_{OUT}	V_{SS} − 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 7.0	V
DLY pin voltage	V_{DLY}	V_{SS} − 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
RO pin voltage	V_{RO}	V_{SS} − 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
Output current	I_{OUT}	520	mA
Junction temperature	T_j	−40 to +150	°C
Operation ambient temperature	T_{opr}	−40 to +125	°C
Storage temperature	T_{stg}	−40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TO-252-5S(A)	Board A	–	86	–	°C/W
			Board B	–	60	–	°C/W
			Board C	–	38	–	°C/W
			Board D	–	31	–	°C/W
			Board E	–	28	–	°C/W
		HSOP-8A	Board A	–	104	–	°C/W
			Board B	–	74	–	°C/W
			Board C	–	39	–	°C/W
			Board D	–	37	–	°C/W
			Board E	–	31	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Regulator block

Table 7

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Output voltage*1	$V_{OUT(E)}$	V_{IN} = 13.5 V, I_{OUT} = 30 mA	$V_{OUT(S)}$ × 0.98	$V_{OUT(S)}$	$V_{OUT(S)}$ × 1.02	V	1
Output current*2	I_{OUT}	$V_{IN} \geq V_{OUT(S)}$ + 1.0 V	400*4	–	–	mA	2
Dropout voltage*3	V_{drop}	I_{OUT} = 100 mA, Ta = +25°C, $V_{OUT(S)}$ = 3.0 V to 5.3 V	–	120	200	mV	1
		I_{OUT} = 200 mA, Ta = +25°C, $V_{OUT(S)}$ = 3.0 V to 5.3 V	–	240	400	mV	1
Line regulation	$\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}$	$V_{OUT(S)}$ + 1.0 V ≤ V_{IN} ≤ 36.0 V, I_{OUT} = 30 mA, Ta = +25°C	–	0.02	0.10	%/V	1
Load regulation	ΔV_{OUT2}	V_{IN} = 13.5 V, 100 μA ≤ I_{OUT} ≤ 100 mA, Ta = +25°C	–	20	40	mV	1
Input voltage	V_{IN}	–	4.0	–	36.0	V	–
Ripple rejection	|RR|	V_{IN} = 13.5 V, I_{OUT} = 30 mA, f = 100 Hz, ΔV_{rip} = 1.0 V_{p-p}	–	70	–	dB	3
Short-circuit current	I_{short}	V_{IN} = 13.5 V, V_{OUT} = 0 V, Ta = +25°C	–	105	–	mA	2
Thermal shutdown detection temperature	T_{SD}	Junction temperature	–	170	–	°C	–
Thermal shutdown release temperature	T_{SR}	Junction temperature	–	135	–	°C	–

***1.** $V_{OUT(S)}$: Set output voltage
$V_{OUT(E)}$: Actual output voltage
Output voltage when fixing I_{OUT} (= 30 mA) and inputting 13.5 V

***2.** The output current at which the output voltage becomes 95% of $V_{OUT(E)}$ after gradually increasing the output current.

***3.** $V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$
V_{OUT3} is the output voltage when $V_{IN} = V_{OUT(S)}$ + 1.0 V.
V_{IN1} is the input voltage at which the output voltage becomes 98% of V_{OUT3} after gradually decreasing the input voltage.

***4.** The output current can be at least this value.
Due to limitation of the power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation when the output current is large.
This specification is guaranteed by design.

2. Detector block

Table 8

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	−	$-V_{DET(S)}$ − 0.1	$-V_{DET(S)}$	$-V_{DET(S)}$ + 0.1	V	4
Hysteresis width	V_{HYS}	−	120	150	−	mV	4
Reset output voltage "H"	V_{ROH}	−	$V_{OUT(S)}$ × 0.9	−	−	V	4
Reset output voltage "L"	V_{ROL}	$V_{OUT} \geq$ 1.0 V, $R_{ext} \geq$ 3 kΩ, Connect to VOUT pin	−	0.2	0.4	V	4
Reset pull-up resistance	R_{RO}	VOUT pin internal resistance	20	30	45	kΩ	−
Reset output current	I_{RO}	V_{RO} = 0.4 V, $V_{OUT} = -V_{DET(S)} - 0.1$ V	3.0	−	−	mA	5
Lower reset timing threshold voltage	V_{DRL}	−	0.2	0.3	0.4	V	6
Upper timing threshold voltage	V_{DU}	−	1.5	1.9	2.3	V	6
Charge current	$I_{D,cha}$	V_{DLY} = 1.0 V	2.0	5.0	8.0	μA	6
Release delay time*2	t_{rd}	C_{DLY} = 47 nF	11	18	25	ms	4
Reset reaction time*3	t_{rr}	C_{DLY} = 47 nF	−	−	50	μs	4

***1.** $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Set detection voltage

***2.** The time period from when V_{OUT} changes to $-V_{DET(S)} - 0.15$ V → $V_{OUT(S)}$ to when V_{RO} reaches V_{OUT} / 2.

***3.** The time period from when V_{OUT} changes to $V_{OUT(S)} \rightarrow -V_{DET(S)} - 0.15$ V to when V_{RO} reaches V_{OUT} / 2.

3. Overall

Table 9

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption during operation	I_{SS1}	V_{IN} = 13.5 V, I_{OUT} = 0 mA	−	60	95	μA	7

■ Test Circuits

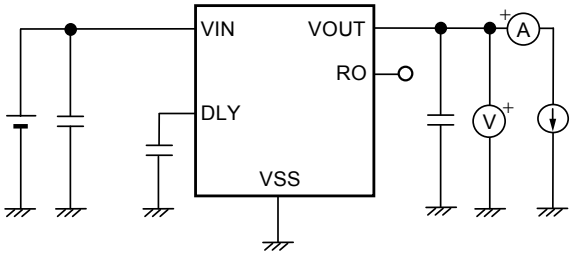


Figure 4 Test Circuit 1

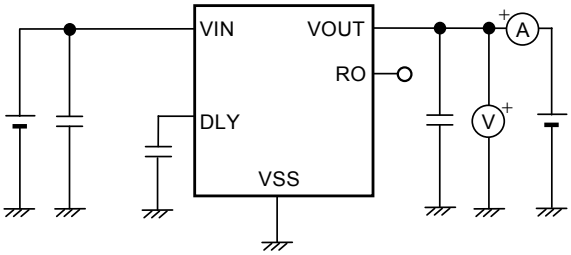


Figure 5 Test Circuit 2

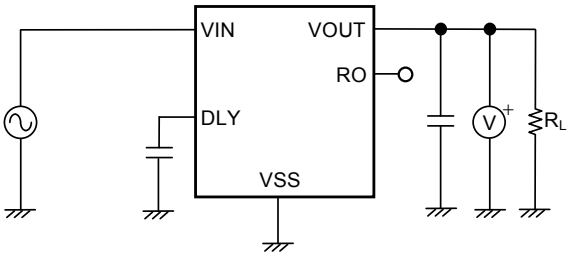


Figure 6 Test Circuit 3

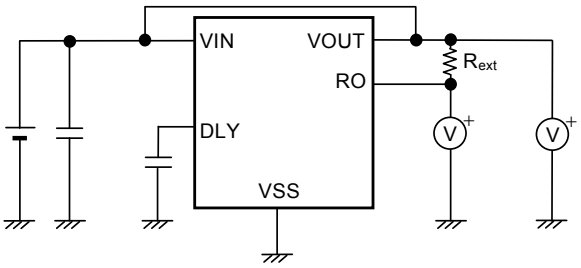


Figure 7 Test Circuit 4

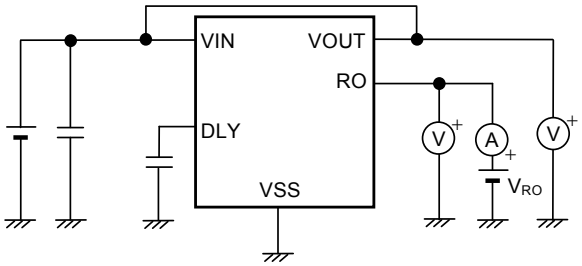


Figure 8 Test Circuit 5

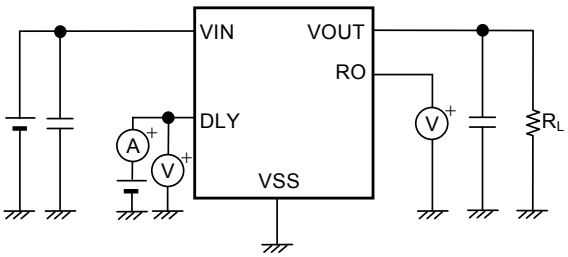


Figure 9 Test Circuit 6

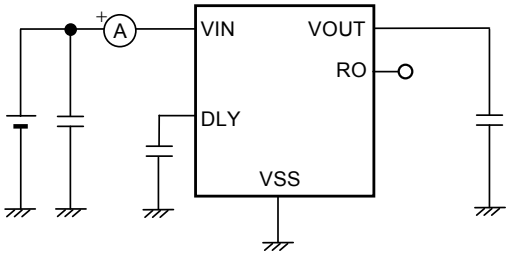


Figure 10 Test Circuit 7

■ Timing Chart

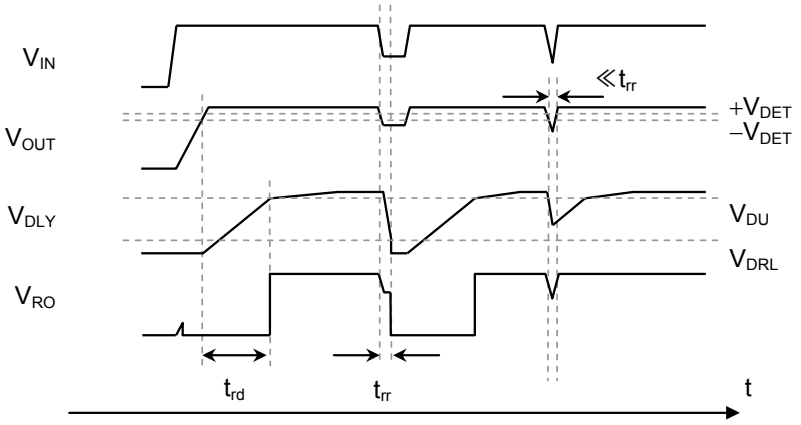


Figure 11 Example of Detector Operation

■ Standard Circuit

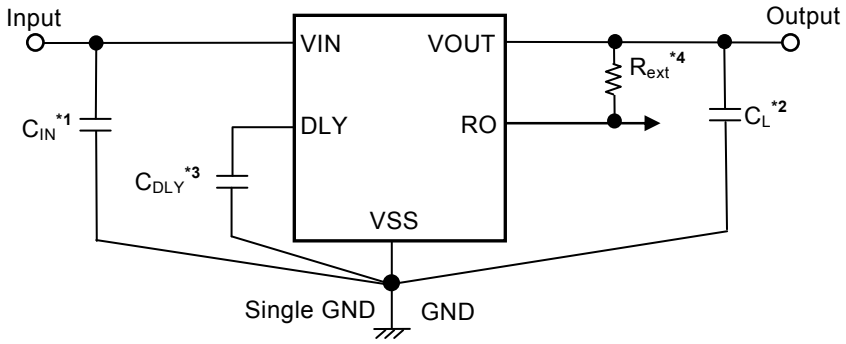


Figure 12

***1.** C_{IN} is a capacitor for stabilizing the input.

***2.** C_L is a capacitor for stabilizing the output. A ceramic capacitor of 2.2 μF or more can be used.

***3.** C_{DLY} is the delay time adjustment capacitor.

***4.** R_{ext} is the external pull-up resistor for the reset output pin.
Connection of the external pull-up resistor is not absolutely essential since the S-19312 Series has a built-in pull-up resistor.

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.

■ Condition of Application

Input capacitor (C_{IN})	: 2.2 μF or more
Output capacitor (C_L)	: 2.2 μF or more
ESR of output capacitor	: 50 Ω or less
Delay time adjustment capacitor (C_{DLY})	: 1.0 nF or more
External pull-up resistor (R_{ext})	: 3 kΩ or more

Caution Generally a series regulator may cause oscillation, depending on the selection of external parts. Confirm that no oscillation occurs in the application for which the above capacitors are used.

■ Selection of Input and Output Capacitors (C_{IN}, C_L)

The S-19312 Series requires C_L between the VOUT pin and the VSS pin for phase compensation. Operation is stabilized by a ceramic capacitor with an output capacitance of 2.2 μF or more over the entire temperature range. When using an OS capacitor, a tantalum capacitor, or an aluminum electrolytic capacitor, the capacitance must be 2.2 μF or more, and the ESR must be 50 Ω or less.
The values of output overshoot and undershoot, which are transient response characteristics, vary depending on the value of the output capacitor.
The required value of capacitance for the input capacitor differs depending on the application.

Caution Define the capacitance of C_{IN} and C_L by sufficient evaluation including the temperature characteristics under the actual usage conditions.

■ Selection of Delay Time Adjustment Capacitor (C_{DLY})

In the S-19312 Series, the delay time adjustment capacitor (C_{DLY}) is necessary between the DLY pin and the VSS pin to adjust the release delay time (t_{rd}) of the detector.
The set release delay time ($t_{rd(S)}$), is calculated by using following equation.
The release delay time (t_{rd}) at the time of the condition of C_{DLY} = 47 nF is shown in "**■ Electrical Characteristics**".

$$t_{rd(S)}\ [\text{ms}] = t_{rd}\ [\text{ms}] \times \frac{C_{DLY}\ [\text{nF}]}{47\ [\text{nF}]}$$

Caution 1. The above equation will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics using an actual application to set the constants.

2. Mounted board layout should be made in such a way that no current flows into or flows from the DLY pin since the impedance of the DLY pin is high, otherwise correct delay time may not be provided.

3. Select C_{DLY} whose leakage current can be ignored against the built-in constant current. The leakage current may cause deviation in delay time and monitoring time. When the leakage current is larger than the built-in constant current, no release takes place.

■ Explanation of Terms

1. Regulator block

1. 1 Low dropout voltage regulator

This voltage regulator has the low dropout voltage due to its built-in low on-resistance transistor.

1. 2 Output voltage (V_{OUT})

The accuracy of the output voltage is ensured at ±2.0% under specified conditions of fixed input voltage[*1], fixed output current, and fixed temperature.

***1.** Differs depending on the product.

Caution If the above conditions change, the output voltage value may vary and exceed the accuracy range of the output voltage. Refer to "1. Regulator block" in "■ Electrical Characteristics" and "1. Regulator block" in "■ Characteristics (Typical Data)" for details.

1. 3 Line regulation $\left(\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}\right)$

Indicates the dependency of the output voltage against the input voltage. That is, the value shows how much the output voltage changes due to a change in the input voltage after fixing output current constant.

1. 4 Load regulation (ΔV_{OUT2})

Indicates the dependency of the output voltage against the output current. That is, the value shows how much the output voltage changes due to a change in the output current after fixing input voltage constant.

1. 5 Dropout voltage (V_{drop})

Indicates the difference between input voltage (V_{IN1}) and the output voltage when; decreasing input voltage (V_{IN}) gradually until the output voltage has dropped out to the value of 98% of output voltage (V_{OUT3}), which is at V_{IN} = $V_{OUT(S)}$ + 1.0 V.

$V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$

2. Detector block

2. 1 Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output of the RO pin turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (Refer to **Figure 13**).

2. 2 Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output of the RO pin turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (Refer to **Figure 14**). This value is calculated from the actual detection voltage ($-V_{DET}$) of a product and the hysteresis width (V_{HYS}), and is $+V_{DET} = -V_{DET} + V_{HYS}$.

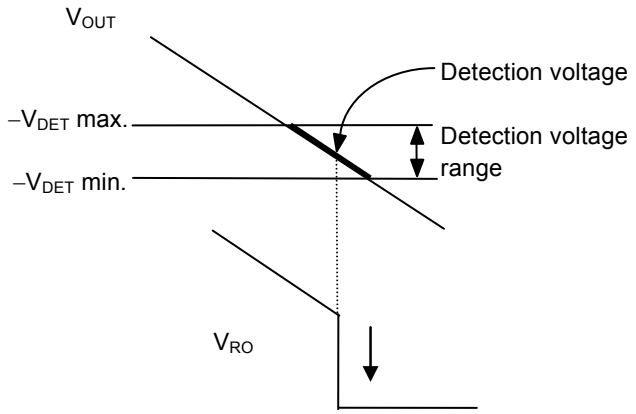


Figure 13 Detection Voltage

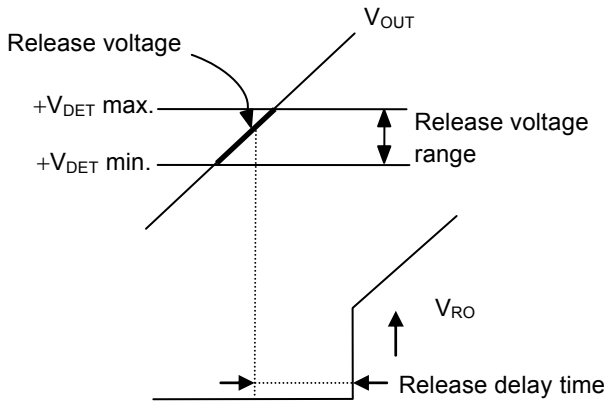


Figure 14 Release Voltage

2. 3 Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage. Setting the hysteresis width between the detection voltage and the release voltage prevents malfunction caused by noise on the VOUT pin voltage (V_{OUT}).

2. 4 Release delay time (t_{rd})

The release delay time is the time period from when V_{OUT} exceeds the release voltage ($+V_{DET}$) to when the RO pin output inverts (Refer to **Figure 15**), and this value changes according to the delay time adjustment capacitor (C_{DLY}). t_{rd} is determined by a built-in constant current which charges C_{DLY}, the charge detection threshold of the DLY pin, and the capacitance of C_{DLY}. It is calculated by using the following equation.

$$t_{rd} = C_{DLY} \times \frac{V_{DU}}{I_{D,cha}}$$

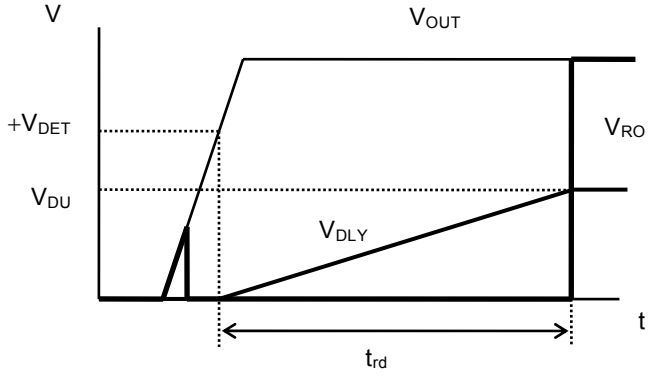


Figure 15 Release Delay Time

2. 5 Reset reaction time (t_{rr})

The reset reaction time is the time period from when V_{OUT} falls below the detection voltage ($-V_{DET}$) to when the RO pin output inverts (Refer to **Figure 16**). Since t_{rr} depends on the reaction time of internal circuit and the discharge time of C_{DLY}, it becomes longer if the capacitance of C_{DLY} becomes larger. Refer to "**2. 9 Reset reaction time vs. Capacitance for delay time adjustment capacitor**" in "**■ Characteristics (Typical Data)**".

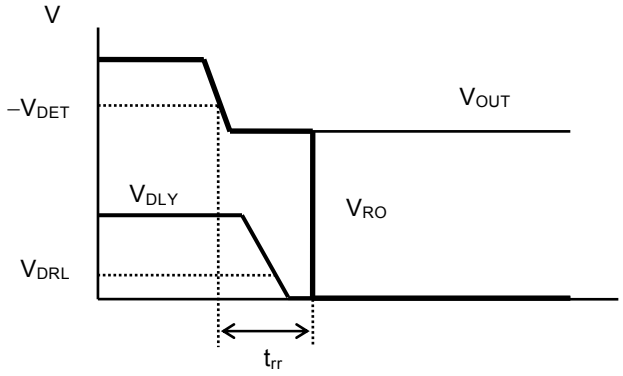


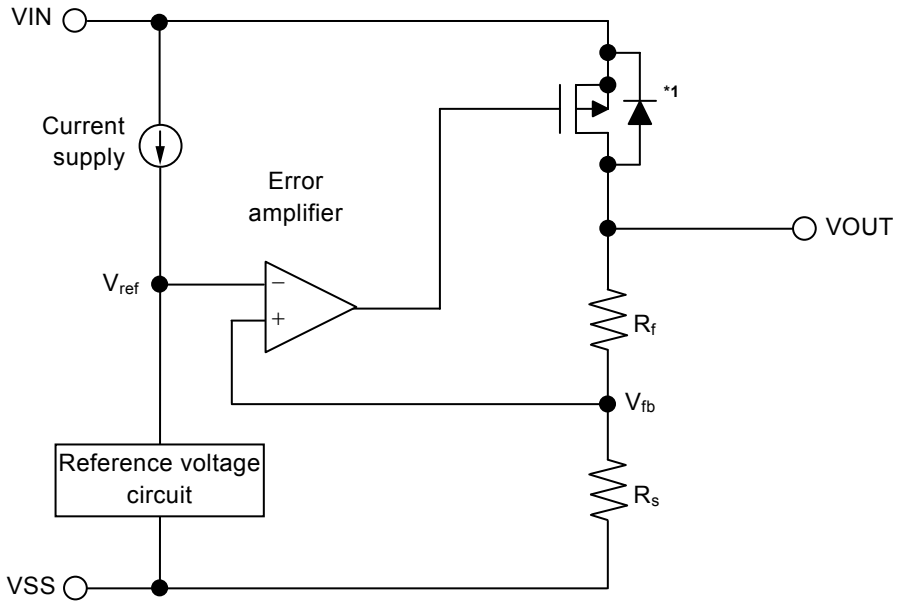
Figure 16 Reset Reaction Time

■ Operation

1. Regulator block

1. 1 Basic operation

Figure 17 shows the block diagram of the regulator in the S-19312 Series.
The error amplifier compares the reference voltage (V_{ref}) with feedback voltage (V_{fb}), which is the output voltage resistance-divided by feedback resistors (R_s and R_f). It supplies the gate voltage necessary to maintain the constant output voltage which is not influenced by the input voltage and temperature change, to the output transistor.



***1.** Parasitic diode

Figure 17

1. 2 Output transistor

In the S-19312 Series, a low on-resistance P-channel MOS FET is used as the output transistor.
Be sure that V_{OUT} does not exceed $V_{IN} + 0.3$ V to prevent the voltage regulator from being damaged due to reverse current flowing from the VOUT pin through a parasitic diode to the VIN pin, when the potential of V_{OUT} became higher than V_{IN}.

1. 3 Overcurrent protection circuit

The S-19312 Series includes an overcurrent protection circuit which having the characteristics shown in "**1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)"** of "**1. Regulator block**" in "**■ Characteristics (Typical Data)**", in order to limit an excessive output current and overcurrent of the output transistor due to short-circuiting between the VOUT pin and the VSS pin. The current when the output pin is short-circuited (I_{short}) is internally set at approx. 105 mA typ., and the load current when short-circuiting is limited based on this value. The output voltage restarts regulating if the output transistor is released from overcurrent status.

Caution This overcurrent protection circuit does not work as for thermal protection. If this IC long keeps short circuiting, pay attention to the conditions of input voltage and load current so that, under the usage conditions including short circuit, the loss of the IC will not exceed power dissipation.

1. 4 Thermal shutdown circuit

The S-19312 Series has a thermal shutdown circuit to limit self-heating. When the junction temperature rises to 170°C typ., the thermal shutdown circuit operates to stop regulating. After that, when the junction temperature drops to 135°C typ., the thermal shutdown circuit is released to restart regulating.
Due to self-heating of the S-19312 Series, if the thermal shutdown circuit starts operating, it stops regulating so that the output voltage drops. For this reason, self-heating is limited and the IC's temperature drops.
When the temperature drops, the thermal shutdown circuit is released to restart regulating, thus self-heating is generated again due to rising of the output voltage. Repeating this procedure makes the waveform of the VOUT pin output into a pulse-like form. This phenomenon continues unless decreasing either or both of the input voltage and the output current in order to reduce the internal power consumption, or decreasing the ambient temperature. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously.

Table 10

Thermal Shutdown Circuit	VOUT Pin Voltage
Detect: 170°C typ.*1	V_{SS} level
Release: 135°C typ.*1	Set value

***1.** Junction temperature

2. Detector block

2. 1 Basic operation

(1) When the output voltage (V_{OUT}) of the regulator is release voltage ($+V_{DET}$) of the detector or higher, the Nch transistor (N1 and N2) are turned off and "H" is output to the RO pin. Since the Pch transistor (P1) is turned on, the input voltage to the comparator (C1) is $\frac{R_B \bullet V_{OUT}}{R_A + R_B}$.

(2) Even if V_{OUT} decreases to $+V_{DET}$ or lower, "H" is output to the RO pin when V_{OUT} is the detection voltage ($-V_{DET}$) or higher. When V_{OUT} decreases to $-V_{DET}$ (point A in **Figure 19**) or lower, N1 which is controlled by C1 is turned on, and C_{DLY} is discharged. If the DLY pin voltage (V_{DLY}) decreases to the lower reset timing threshold voltage (V_{DRL}) or lower, N2 of output stage of C2 is turned on, and then "L" is output to the RO pin. At this time, P1 is turned off, and the input voltage to C1 is $\frac{R_B \bullet V_{OUT}}{R_A + R_B + R_C}$.

(3) If V_{OUT} further decreases to the IC's minimum operation voltage or lower, the RO pin output is "H".

(4) When V_{OUT} increases to the IC's minimum operation voltage or higher, "L" is output to the RO pin. Moreover, even if V_{OUT} exceeds $-V_{DET}$, the output is "L" when V_{OUT} is lower than $+V_{DET}$.

(5) When V_{OUT} increases to $+V_{DET}$ (point B in **Figure 19**) or higher, N1 is turned off and C_{DLY} is charged. N2 is turned off if V_{DLY} increases to the upper timing threshold voltage (V_{DU}) or higher, and "H" is output to the RO pin.

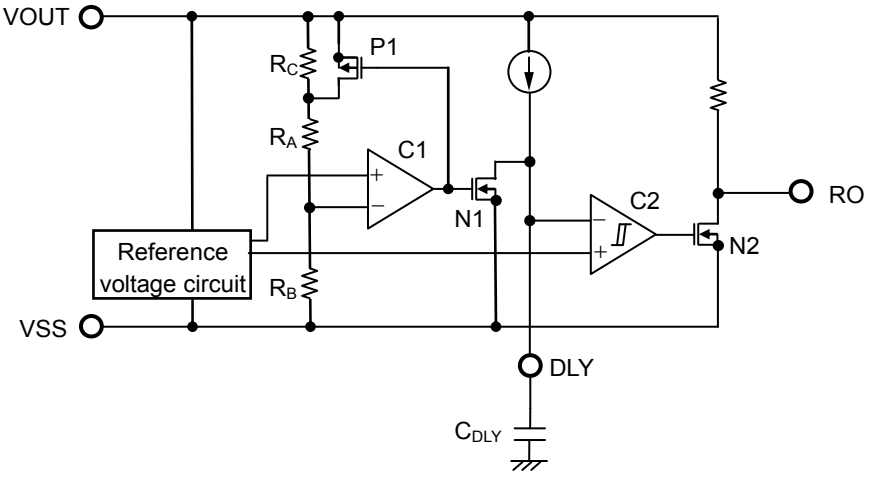


Figure 18 Operation of Detector Block

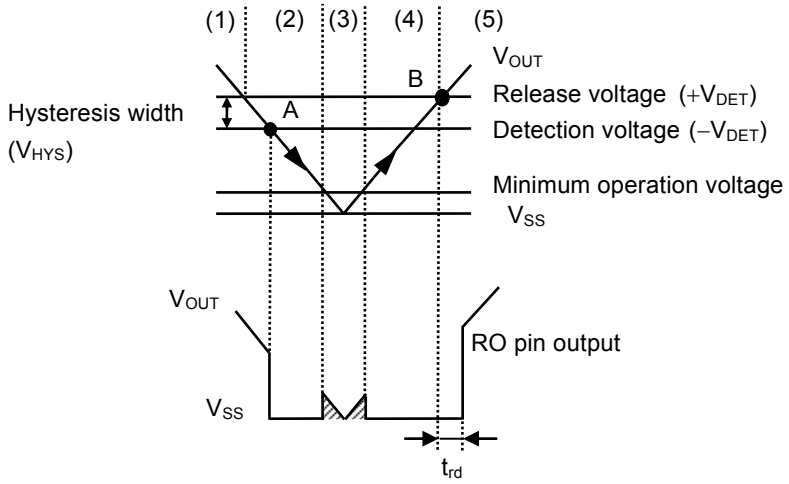


Figure 19 Timing Chart of Detector Block

2. 2 Delay circuit

When the output voltage (V_{OUT}) of the regulator rises under the status that "L" is output to the RO pin, the reset release signal is output to the RO pin later than when V_{OUT} becomes $+V_{DET}$. The release delay time (t_{rd}) changes according to C_{DLY}. Refer to "■ **Selection of Delay Time Adjustment Capacitor (C_{DLY})**" for details.
Moreover, when V_{OUT} decreases to $-V_{DET}$ or lower, the delay time of the same time length as the reset reaction time (t_{rr}) occurs in the output to the RO pin. Refer to "**2. Detector block**" in "■ **Explanation of Terms**" for details.
If the time period from when V_{OUT} decreases to $-V_{DET}$ or lower to when V_{OUT} increases to $+V_{DET}$ or higher is significantly shorter compared to the length of t_{rr}, V_{DLY} may not decrease to V_{DRL} or lower. In that case, "H" output remains in the RO pin.

Caution Since t_{rd} depends on the charge time of C_{DLY}, t_{rd} may be shorter than the set value if the charge operation is initiated under the condition that a residual electric charge is left in C_{DLY}.

2. 3 Output circuit

The output form of the RO pin is Nch open-drain. The RO pin can output a signal without an external pull-up resistor since it has a built-in resistor to pull up to the VOUT pin internally.
Do not connect to the pin other than VOUT pin when connecting an external pull-up resistor to the RO pin.

Caution Define the external pull-up resistance by sufficient evaluation including the temperature characteristics under the actual usage conditions.

■ Precautions

- Wiring patterns for the VIN pin, the VOUT pin and GND should be designed so that the impedance is low. When mounting an output capacitor between the VOUT pin and the VSS pin (C_L) and an input capacitor between the VIN pin and the VSS pin (C_{IN}), the distance from the capacitors to these pins should be as short as possible.
- Note that generally the output voltage may increase when a series regulator is used at low load current (0.1 mA or less).
- Note that generally the output voltage may increase due to the leakage current from an output transistor when a series regulator is used at high temperature.
- Generally a series regulator may cause oscillation, depending on the selection of external parts. The following conditions are recommended for the S-19312 Series. However, be sure to perform sufficient evaluation under the actual usage conditions for selection, including evaluation of temperature characteristics. Refer to "**4. Example of equivalent series resistance vs. Output current characteristics (Ta = +25°C)**" in "**■ Reference Data**" for the equivalent series resistance (R_{ESR}) of the output capacitor.

  Input capacitor (C_{IN}): 2.2 μF or more
  Output capacitor (C_L): 2.2 μF or more

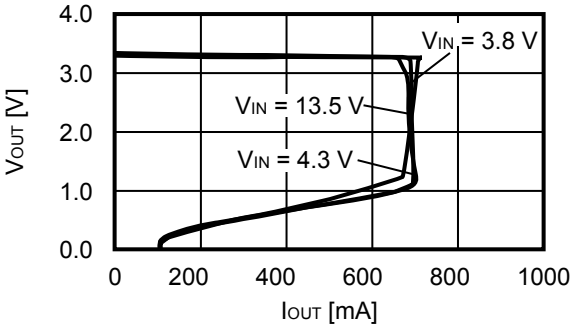
- In a series regulator, generally the values of overshoot and undershoot in the output voltage vary depending on the variation factors of power-on, power supply fluctuation and load fluctuation, or output capacitance.
  Determine the conditions of the output capacitor after sufficiently evaluating the temperature characteristics of overshoot or undershoot in the output voltage with the actual device.
- The voltage regulator may oscillate when the impedance of the power supply is high and the input capacitance is small or an input capacitor is not connected.
- Overshoot may occur in the output voltage momentarily if the voltage is rapidly raised at power-on or when the power supply fluctuates. Sufficiently evaluate the output voltage at that time with the actual device.
- If the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur to the VOUT pin due to resonance of the wiring inductance and the output capacitance in the application. The negative voltage can be limited by inserting a protection diode between the VOUT pin and the VSS pin or inserting a series resistor to the output capacitor.
- The application conditions for the input voltage, the output voltage, and the load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In determining the output current, attention should be paid to the output current value specified in **Table 7** in "**■ Electrical Characteristics**" and footnote ***4** of the table.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

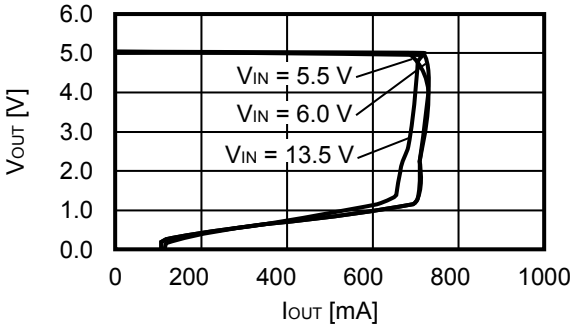
1. Regulator block

1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)

1. 1. 1 V_{OUT} = 3.3 V

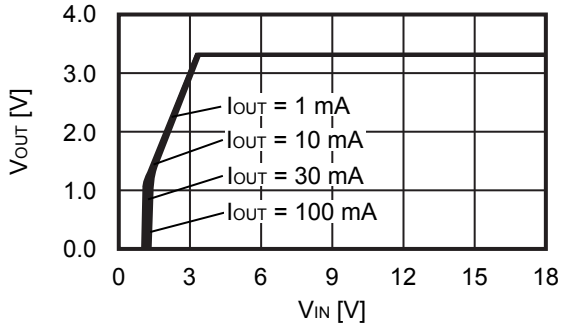


1. 1. 2 V_{OUT} = 5.0 V

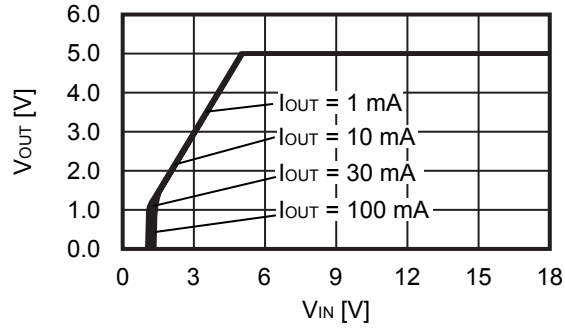


1. 2 Output voltage vs. Input voltage (Ta = +25°C)

1. 2. 1 V_{OUT} = 3.3 V

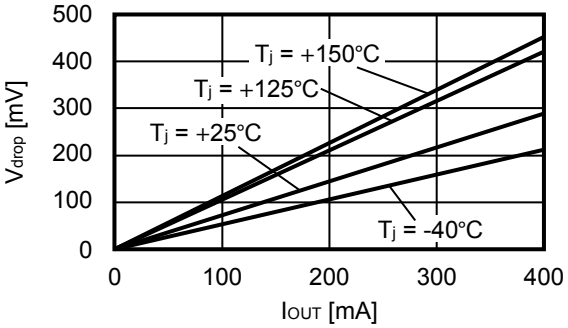


1. 2. 2 V_{OUT} = 5.0 V

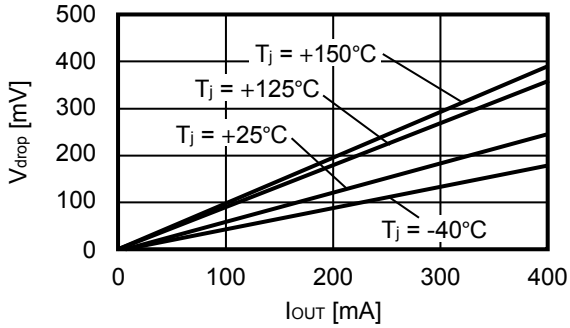


1. 3 Dropout voltage vs. Output current

1. 3. 1 V_{OUT} = 3.3 V

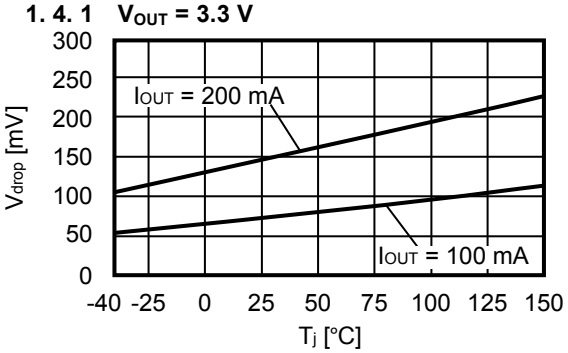


1. 3. 2 V_{OUT} = 5.0 V

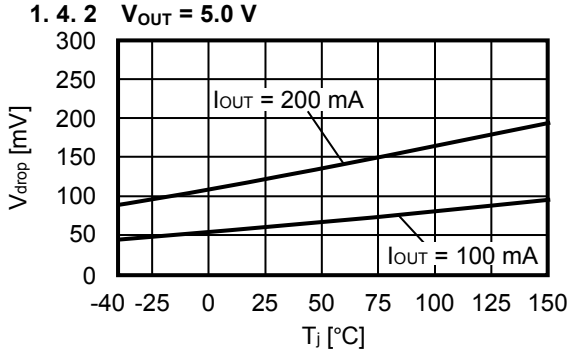


1. 4 Dropout voltage vs. Junction temperature

1. 4. 1 V_{OUT} = 3.3 V

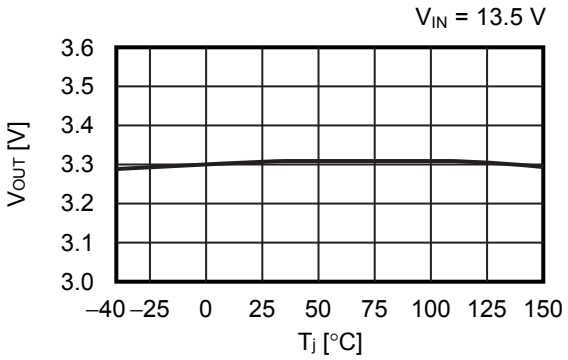


1. 4. 2 V_{OUT} = 5.0 V

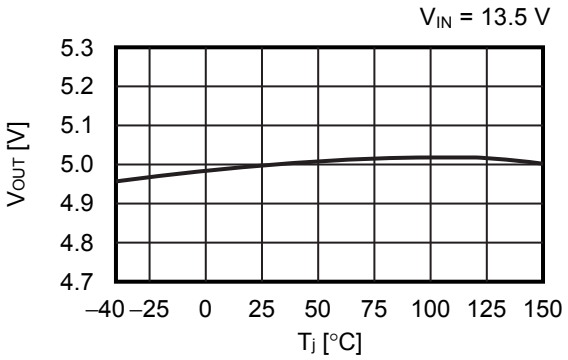


1. 5 Output voltage vs. Junction temperature

1. 5. 1 V_{OUT} = 3.3 V

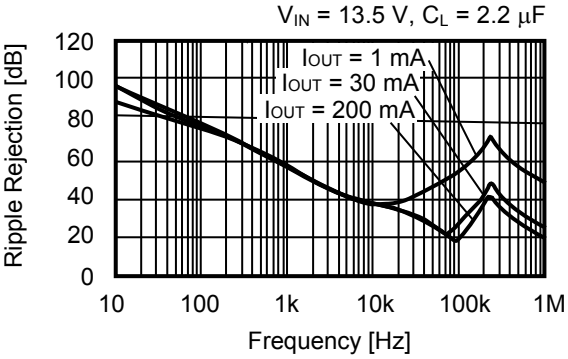


1. 5. 2 V_{OUT} = 5.0 V

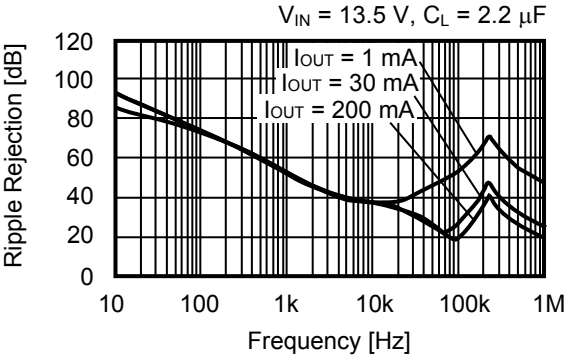


1. 6 Ripple rejection (Ta = +25°C)

1. 6. 1 V_{OUT} = 3.3 V



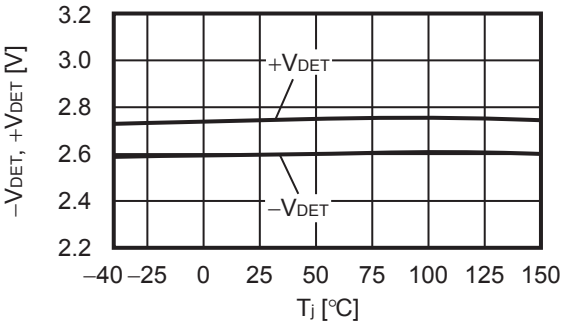
1. 6. 2 V_{OUT} = 5.0 V



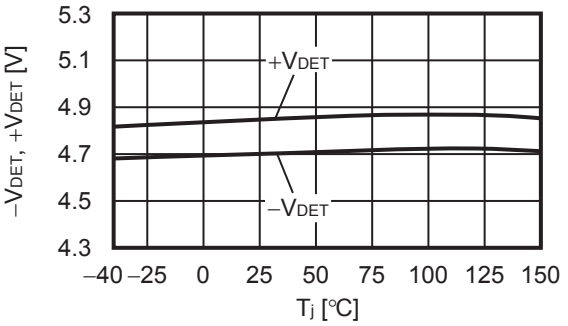
2. Detector block

2. 1 Detection voltage, Release voltage vs. Junction temperature

2. 1. 1 $-V_{DET}$ = 2.6 V

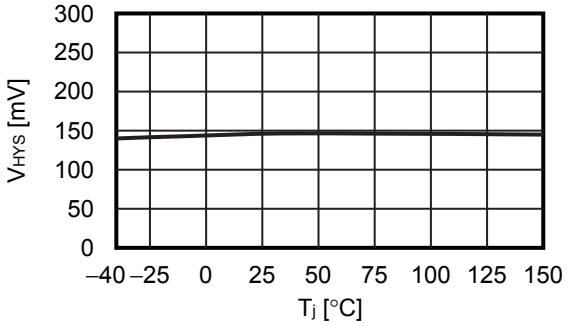


2. 1. 2 $-V_{DET}$ = 4.7 V

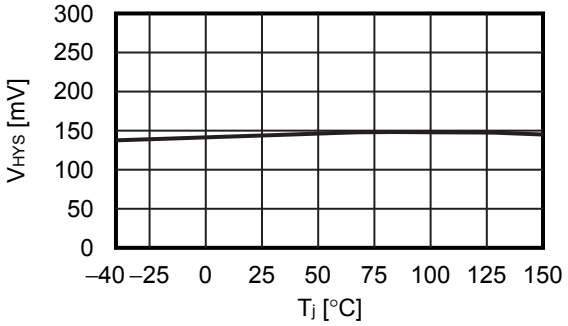


2. 2 Hysteresis width vs. Junction temperature

2. 2. 1 $-V_{DET}$ = 2.6 V

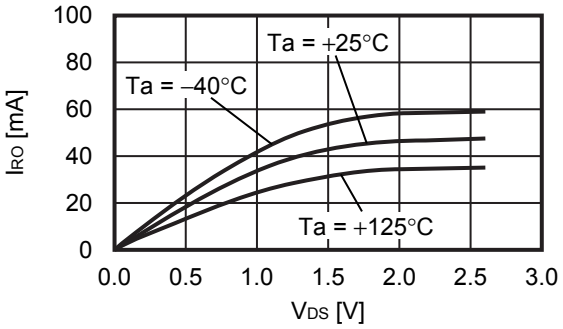


2. 2. 2 $-V_{DET}$ = 4.7 V

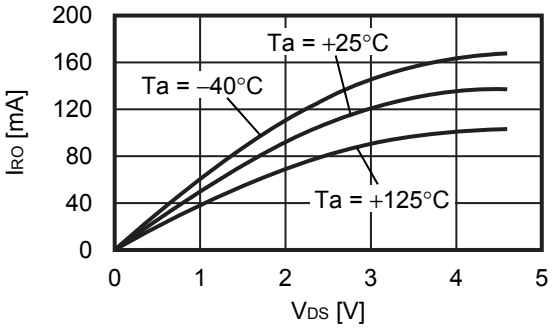


2. 3 Nch transistor output current vs. V_{DS}

2. 3. 1 $-V_{DET}$ = 2.6 V

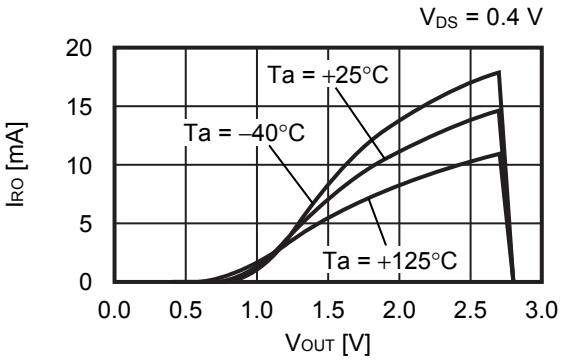


2. 3. 2 $-V_{DET}$ = 4.7 V

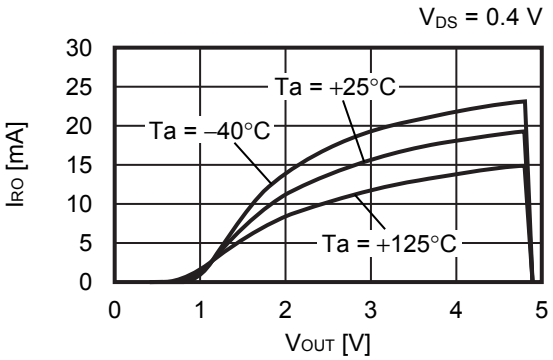


2. 4 Nch transistor output current vs. Output voltage

2. 4. 1 $-V_{DET}$ = 2.6 V

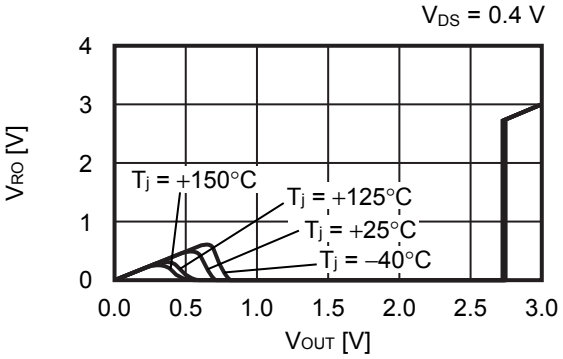


2. 4. 2 $-V_{DET}$ = 4.7 V

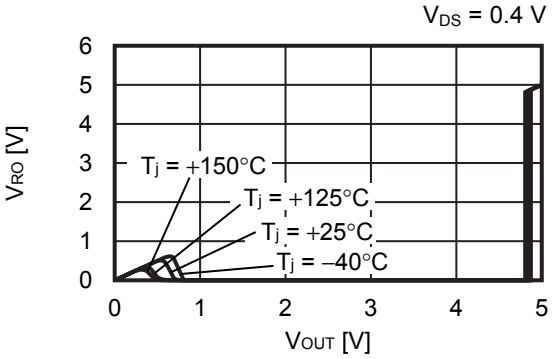


2. 5 Nch transistor output voltage vs. Output voltage

2. 5. 1 $-V_{DET}$ = 2.6 V



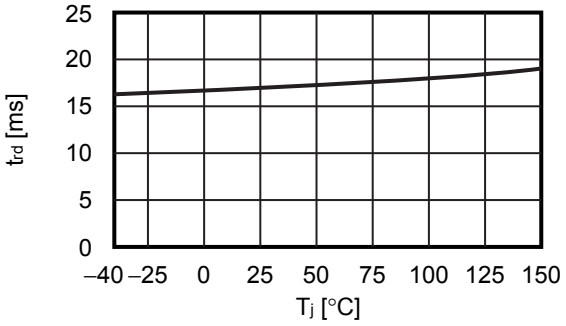
2. 5. 2 $-V_{DET}$ = 4.7 V



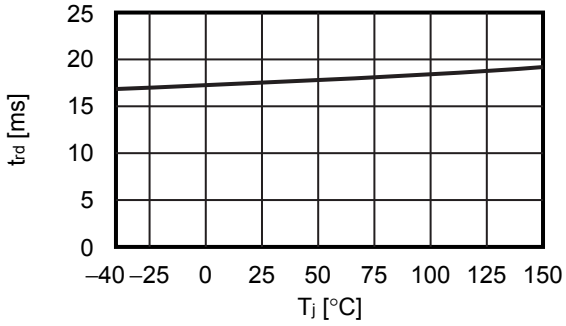
Remark V_{DS}: Drain-to-source voltage of the output transistor

2. 6 Release delay time vs. Junction temperature

2. 6. 1 $-V_{DET}$ = 2.6 V

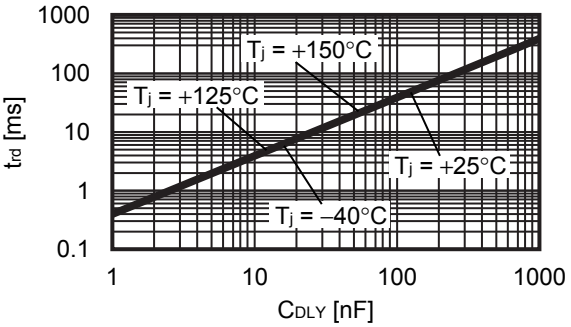


2. 6. 2 $-V_{DET}$ = 4.7 V

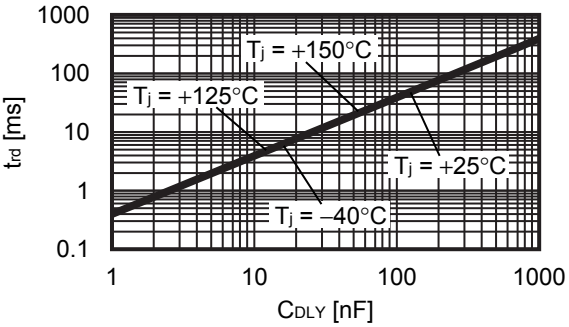


2. 7 Release delay time vs. Capacitance for delay time adjustment capacitor

2. 7. 1 $-V_{DET}$ = 2.6 V

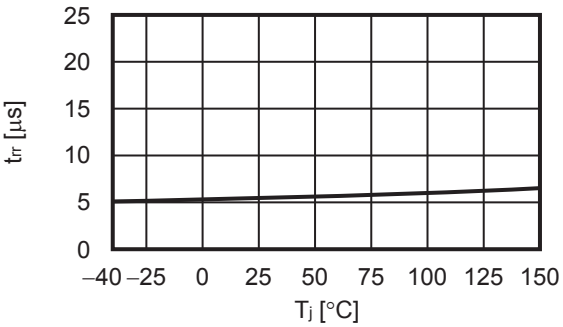


2. 7. 2 $-V_{DET}$ = 4.7 V

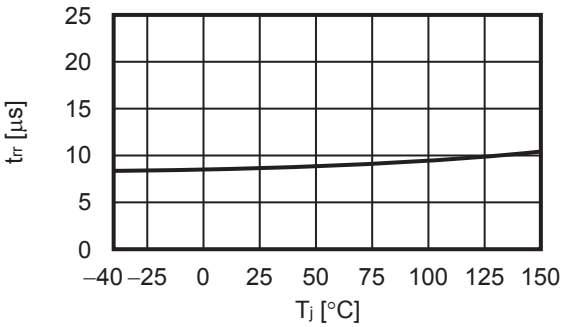


2. 8 Reset reaction time vs. Junction temperature

2. 8. 1 $-V_{DET}$ = 2.6 V

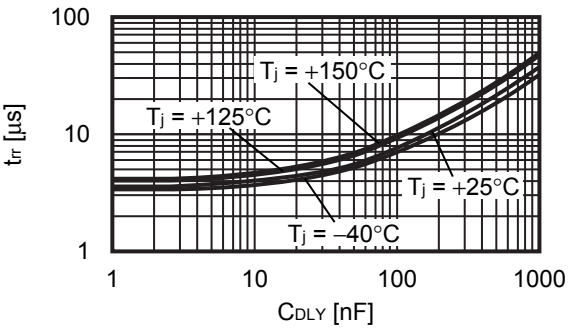


2. 8. 2 $-V_{DET}$ = 4.7 V

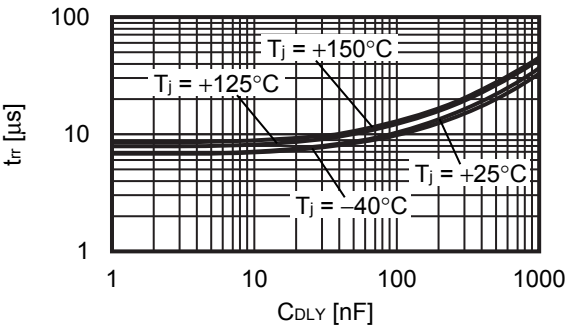


2. 9 Reset reaction time vs. Capacitance for delay time adjustment capacitor

2. 9. 1 $-V_{DET}$ = 2.6 V



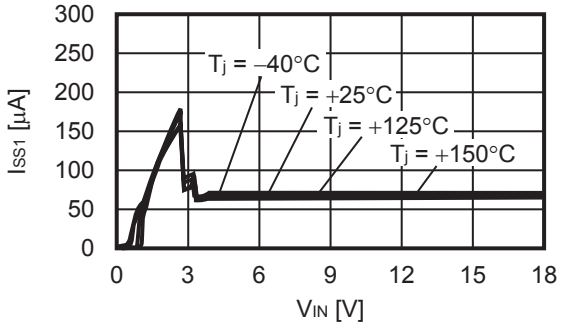
2. 9. 2 $-V_{DET}$ = 4.7 V



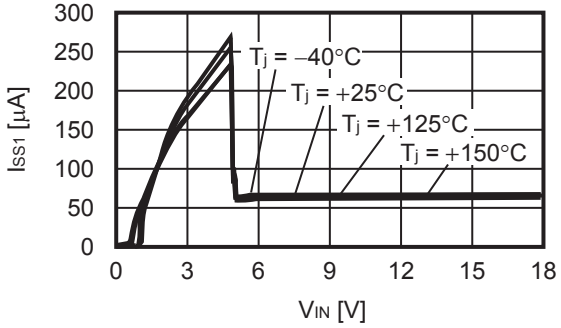
3. Overall

3. 1 Current consumption during operation vs. input voltage

3. 1. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

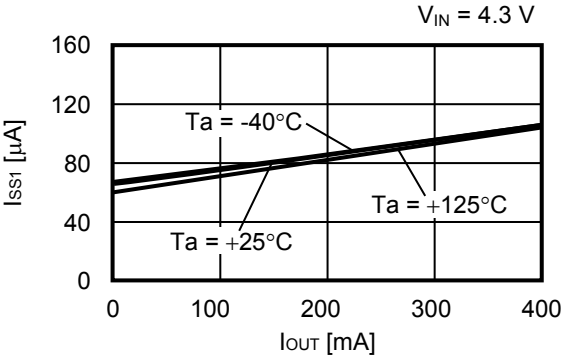


3. 1. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

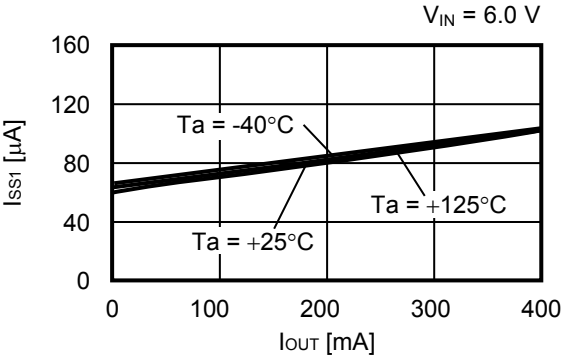


3. 2 Current consumption during operation vs. Output current

3. 2. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

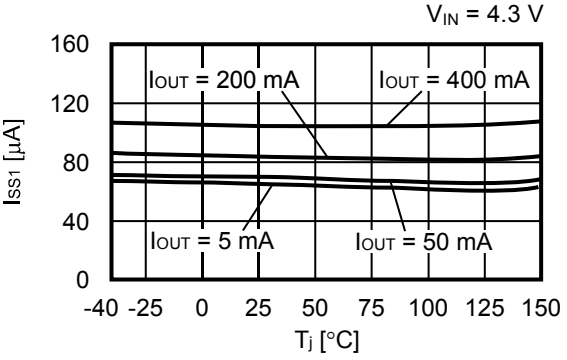


3. 2. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

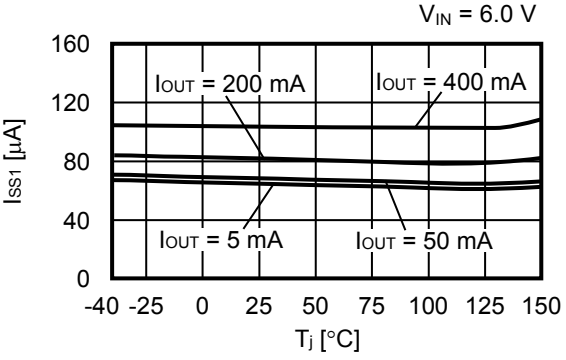


3. 3 Current consumption during operation vs. Junction temperature

3. 3. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V



3. 3. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

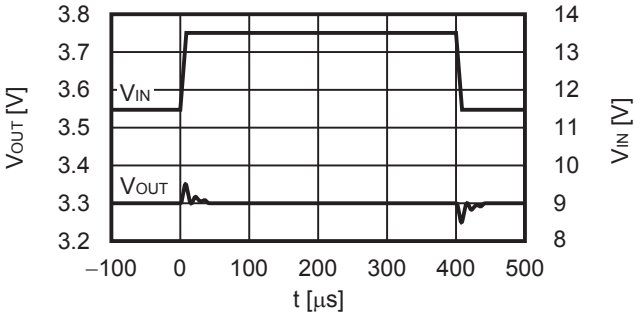


■ Reference Data

1. Transient response characteristics when input (Ta = +25°C)

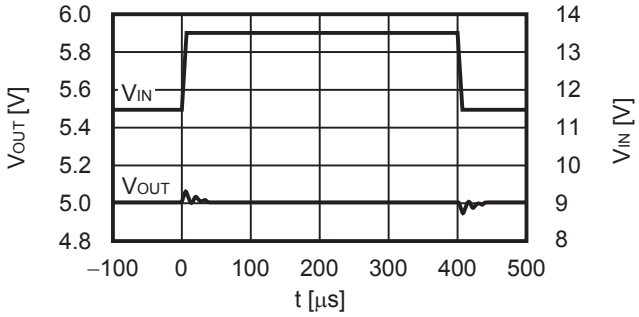
1. 1 V_{OUT} = 3.3 V

I_{OUT} = 30 mA, C_L = 2.2 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



1. 2 V_{OUT} = 5.0 V

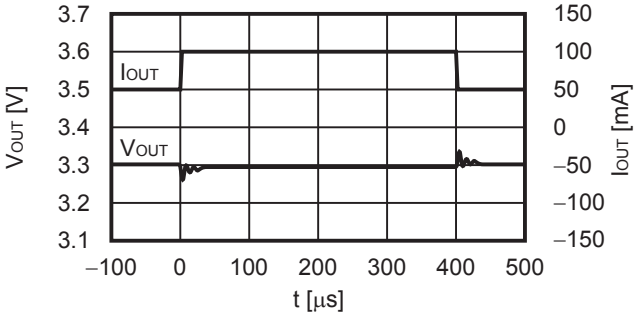
I_{OUT} = 30 mA, C_L = 2.2 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



2. Transient response characteristics of load (Ta = +25°C)

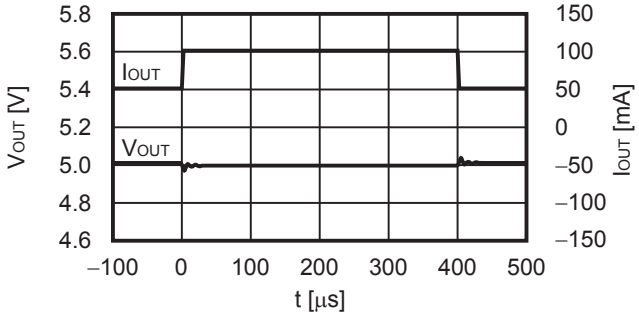
2. 1 V_{OUT} = 3.3 V

V_{IN} = 13.5 V, C_L = 2.2 µF, I_{OUT} = 50 mA ↔ 100 mA



2. 2 V_{OUT} = 5.0 V

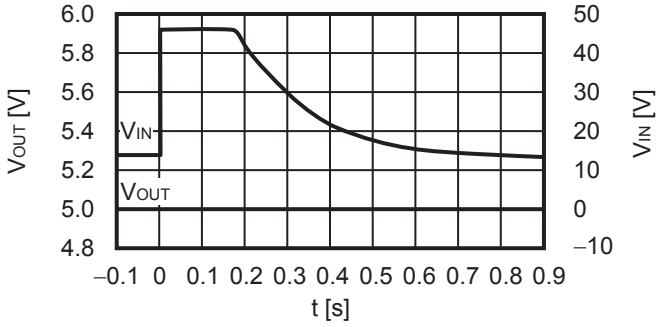
V_{IN} = 13.5 V, C_L = 2.2 µF, I_{OUT} = 50 mA ↔ 100 mA



3. Load dump characteristics (Ta = +25°C)

3. 1 V_{OUT} = 5.0 V

I_{OUT} = 0.1 mA, V_{IN} = 13.5 V ↔ 45.0 V, C_{IN} = C_L = 2.2 µF



4. Example of equivalent series resistance vs. Output current characteristics (Ta = +25°C)

C_{IN} = C_L = 2.2 µF, C_{DLY} = 47 nF

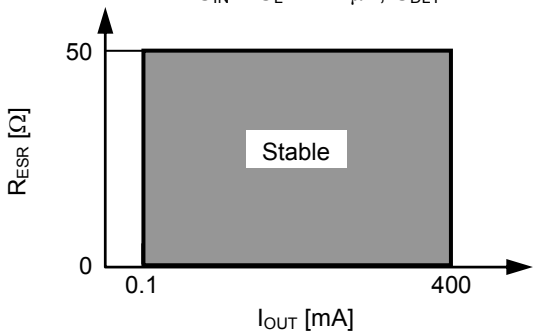
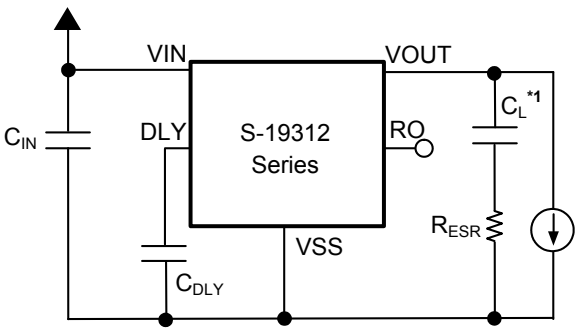


Figure 20

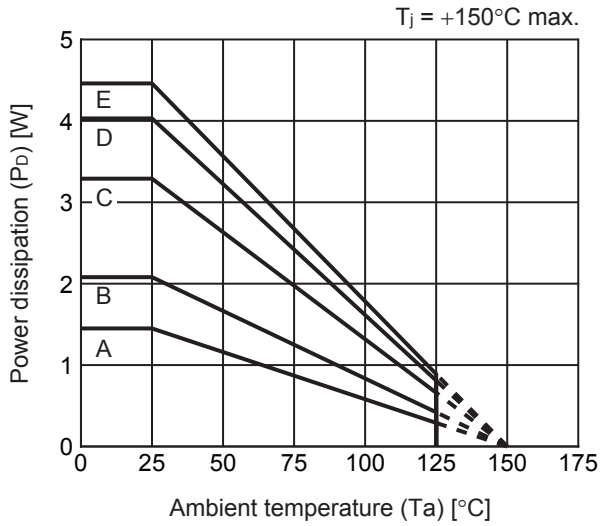


***1.** C_L: Murata Manufacturing Co., Ltd.
GCM31CR71H225K (2.2 µF)

Figure 21

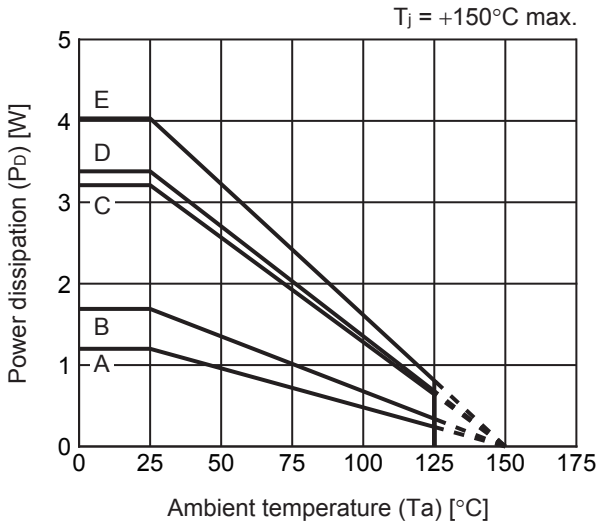
■ Power Dissipation

TO-252-5S(A)



Board	Power Dissipation (P_D)
A	1.45 W
B	2.08 W
C	3.29 W
D	4.03 W
E	4.46 W

HSOP-8A

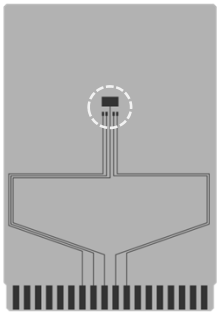


Board	Power Dissipation (P_D)
A	1.20 W
B	1.69 W
C	3.21 W
D	3.38 W
E	4.03 W

TO-252-5S Test Board

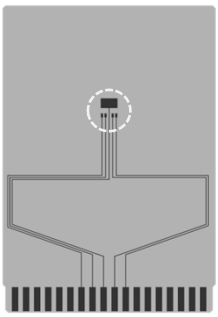
(1) Board A

IC Mount Area



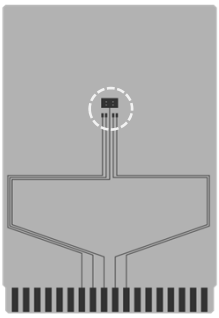
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B

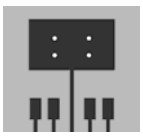


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



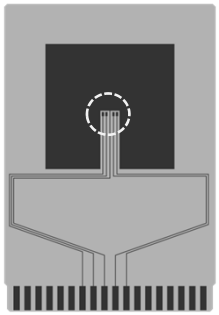
enlarged view

No. TO252-5S-A-Board-SD-1.0

TO-252-5S Test Board

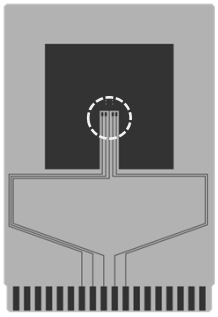
(4) Board D

IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

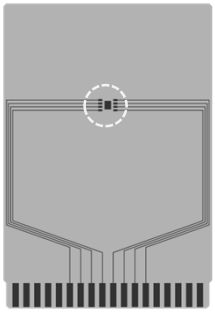
enlarged view

No. TO252-5S-A-Board-SD-1.0

HSOP-8A Test Board

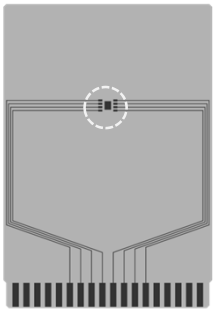
(1) Board A

IC Mount Area



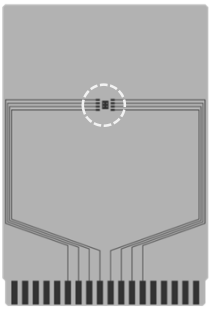
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B

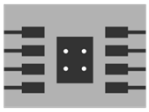


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



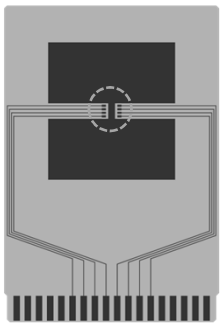
enlarged view

No. HSOP8A-A-Board-SD-1.0

HSOP-8A Test Board

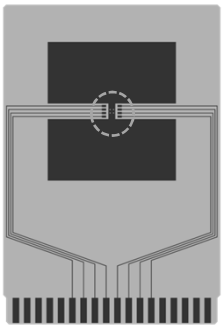
(4) Board D

IC Mount Area

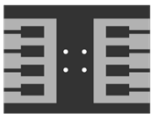


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E

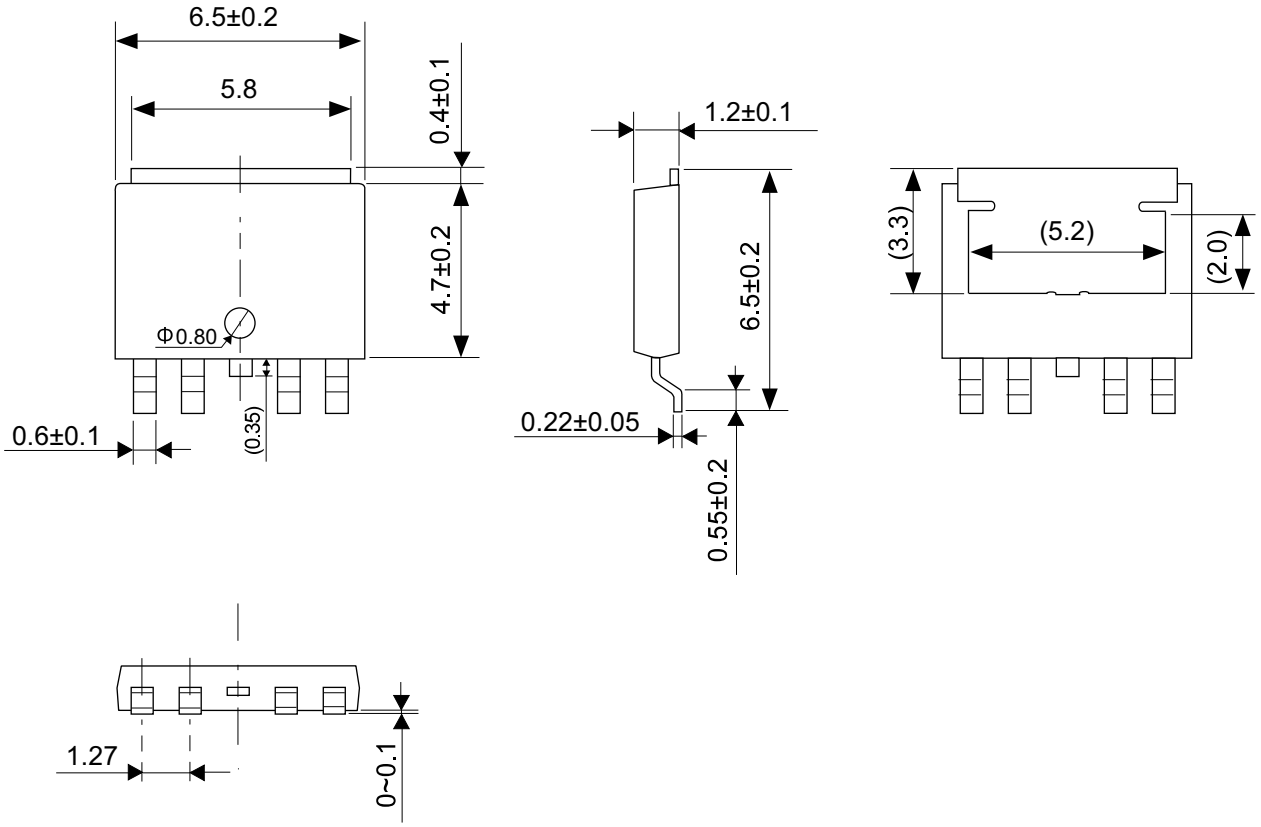


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



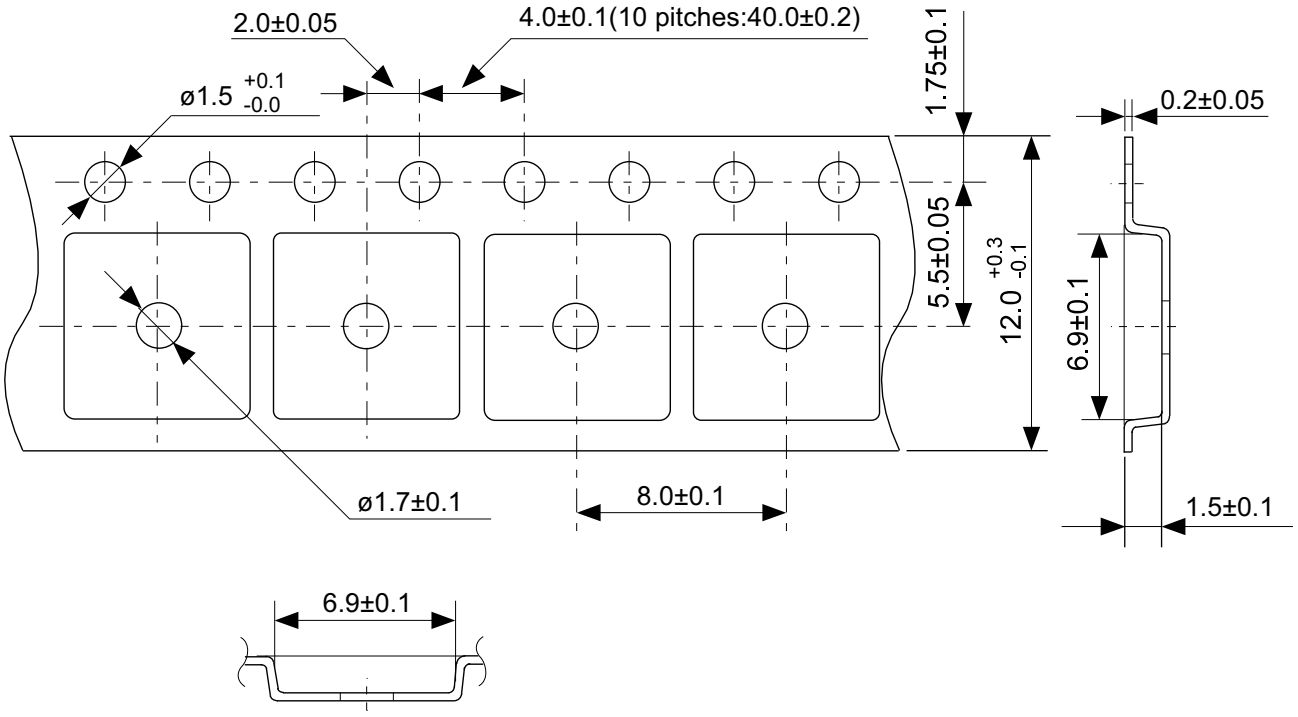
enlarged view

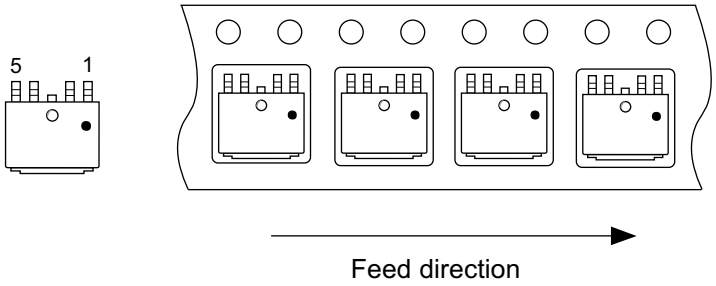
No. HSOP8A-A-Board-SD-1.0



No. VA005-A-P-SD-2.0

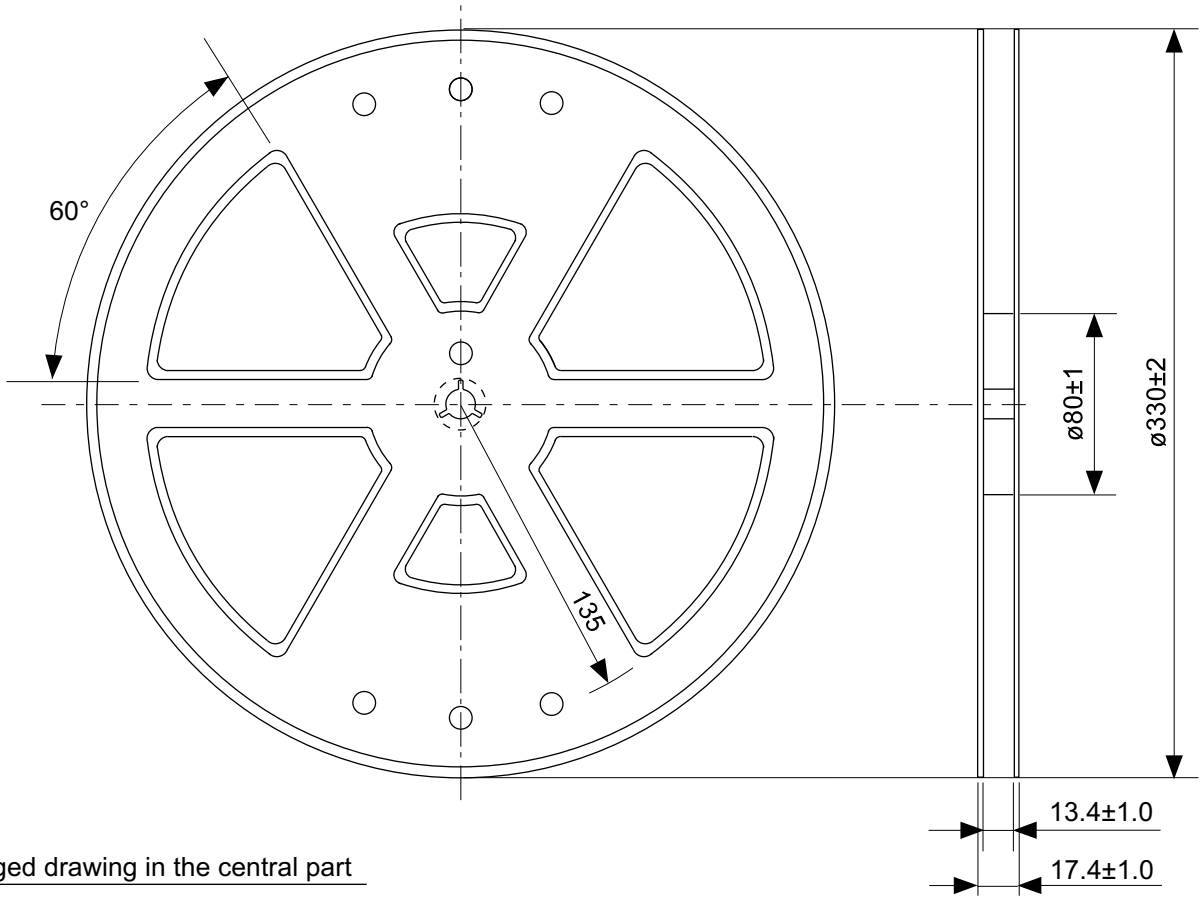
TITLE	TO-252-5S-A-PKG Dimensions
No.	VA005-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



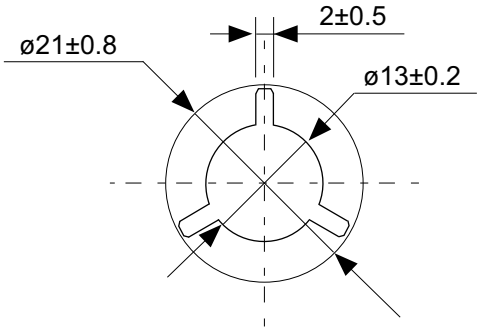


No. VA005-A-C-SD-1.0

TITLE	TO-252-5S-A-Carrier Tape
No.	VA005-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

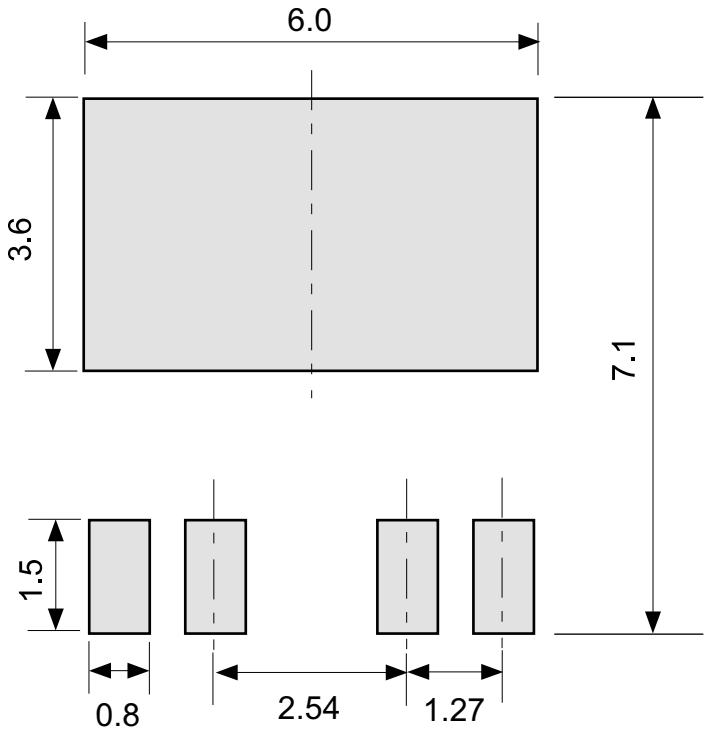


Enlarged drawing in the central part



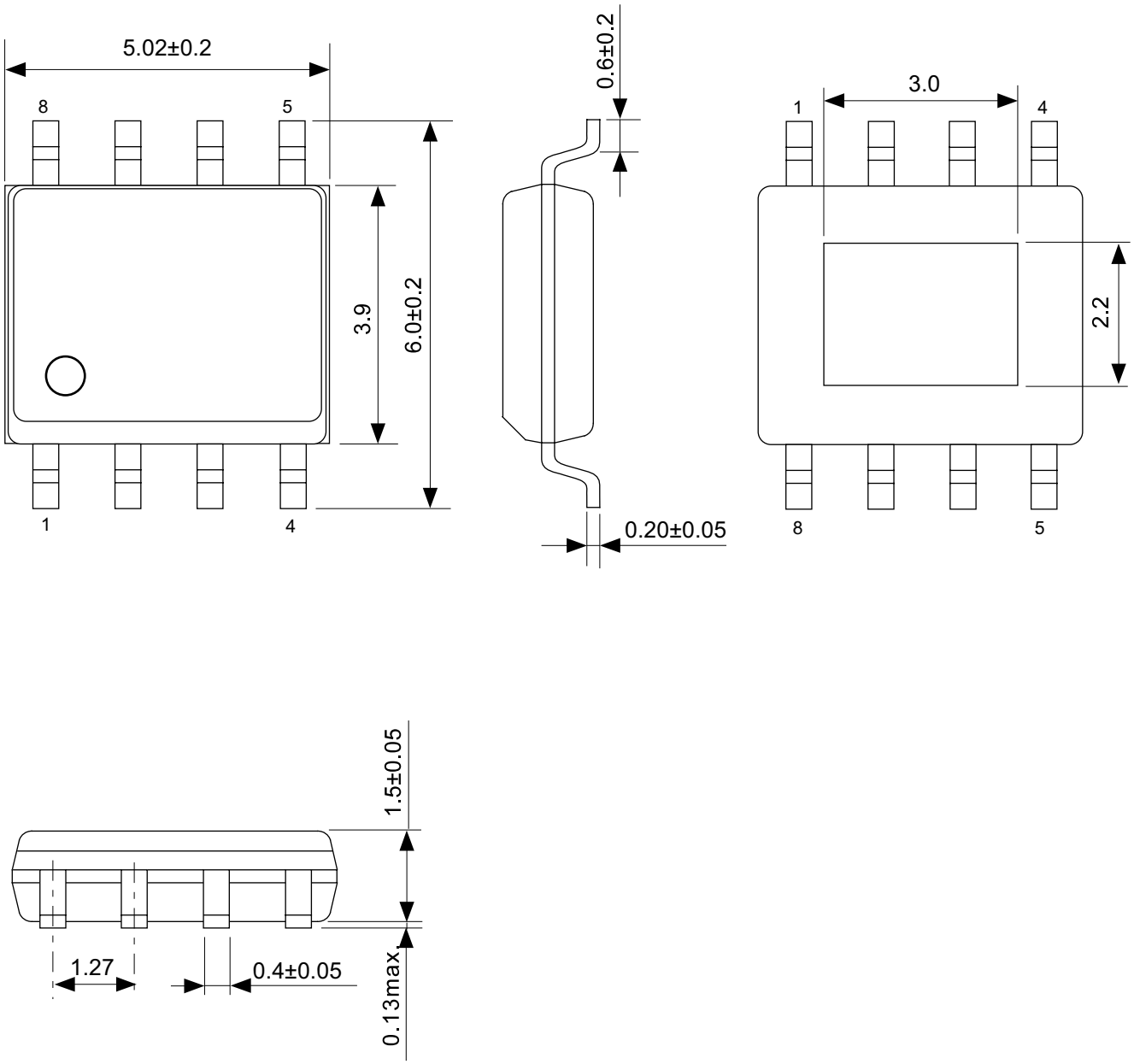
No. VA005-A-R-SD-1.0

TITLE	TO-252-5S-A-Reel		
No.	VA005-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



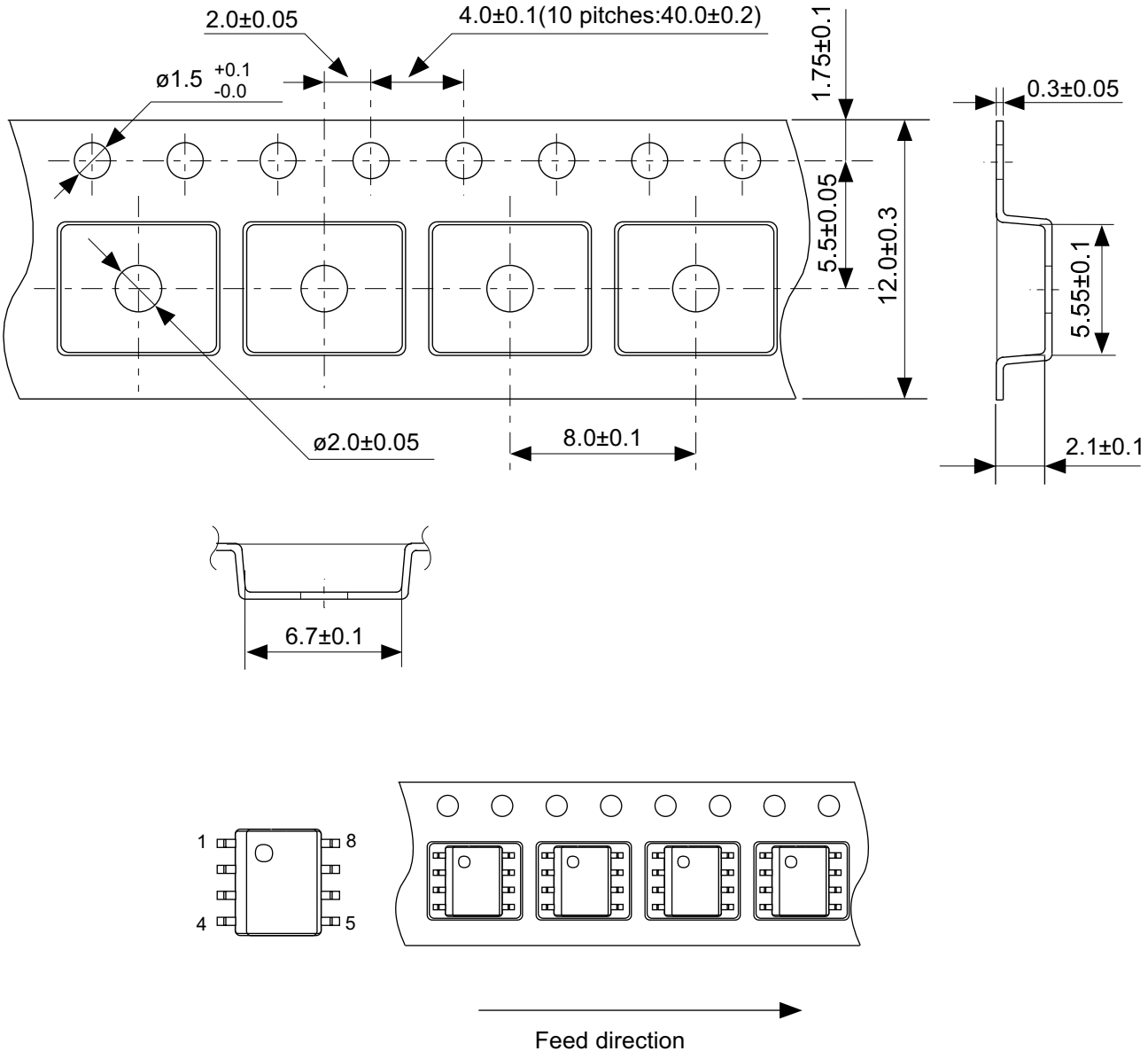
No. VA005-A-L-SD-1.0

TITLE	TO-252-5S-A -Land Recommendation
No.	VA005-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



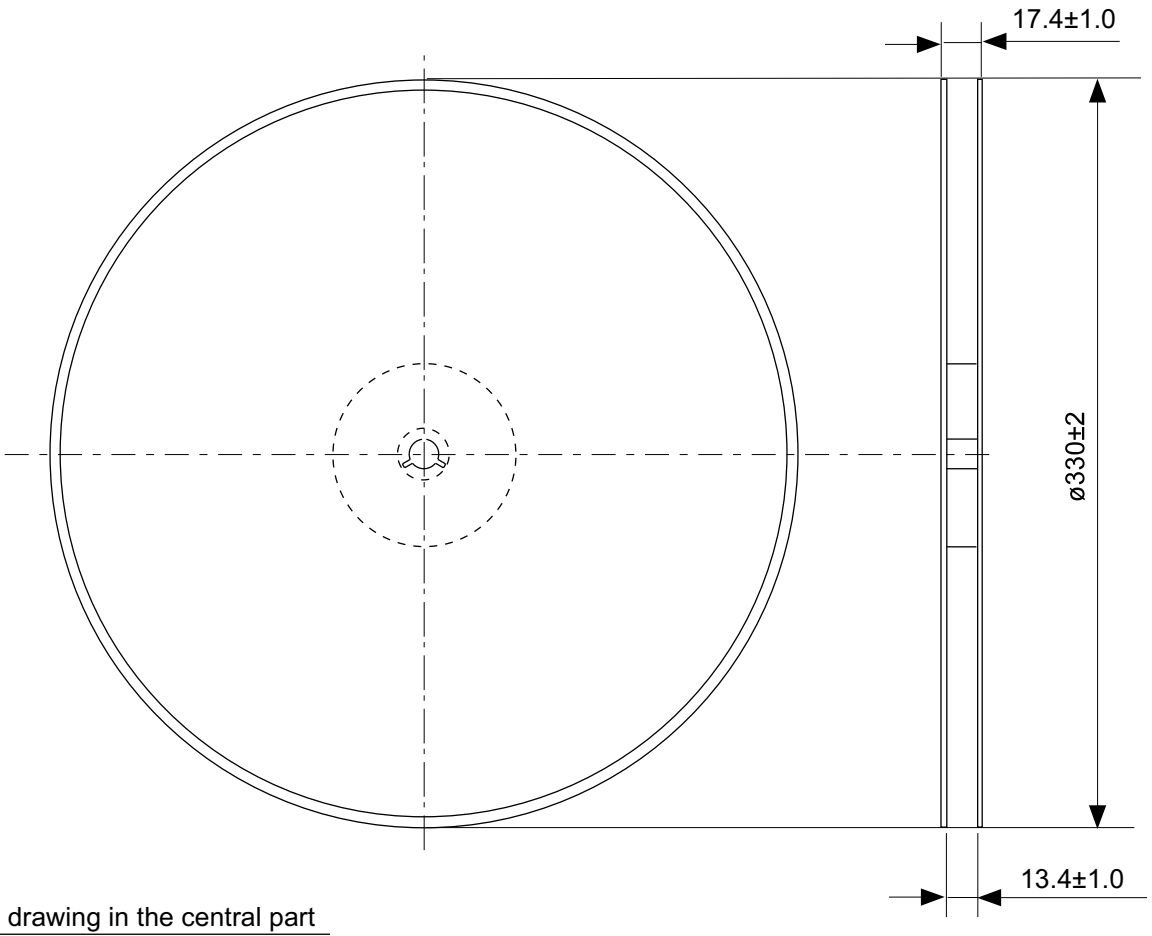
No. FH008-A-P-SD-2.0

TITLE	HSOP8A-A-PKG Dimensions
No.	FH008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

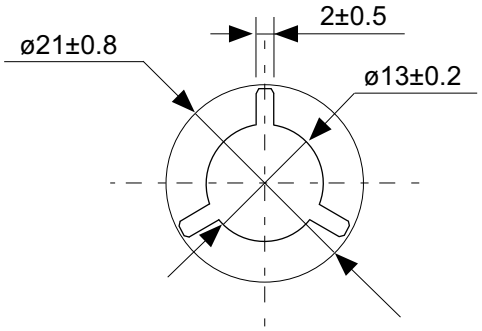


No. FH008-A-C-SD-1.0

TITLE	HSOP8A-A-Carrier Tape
No.	FH008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

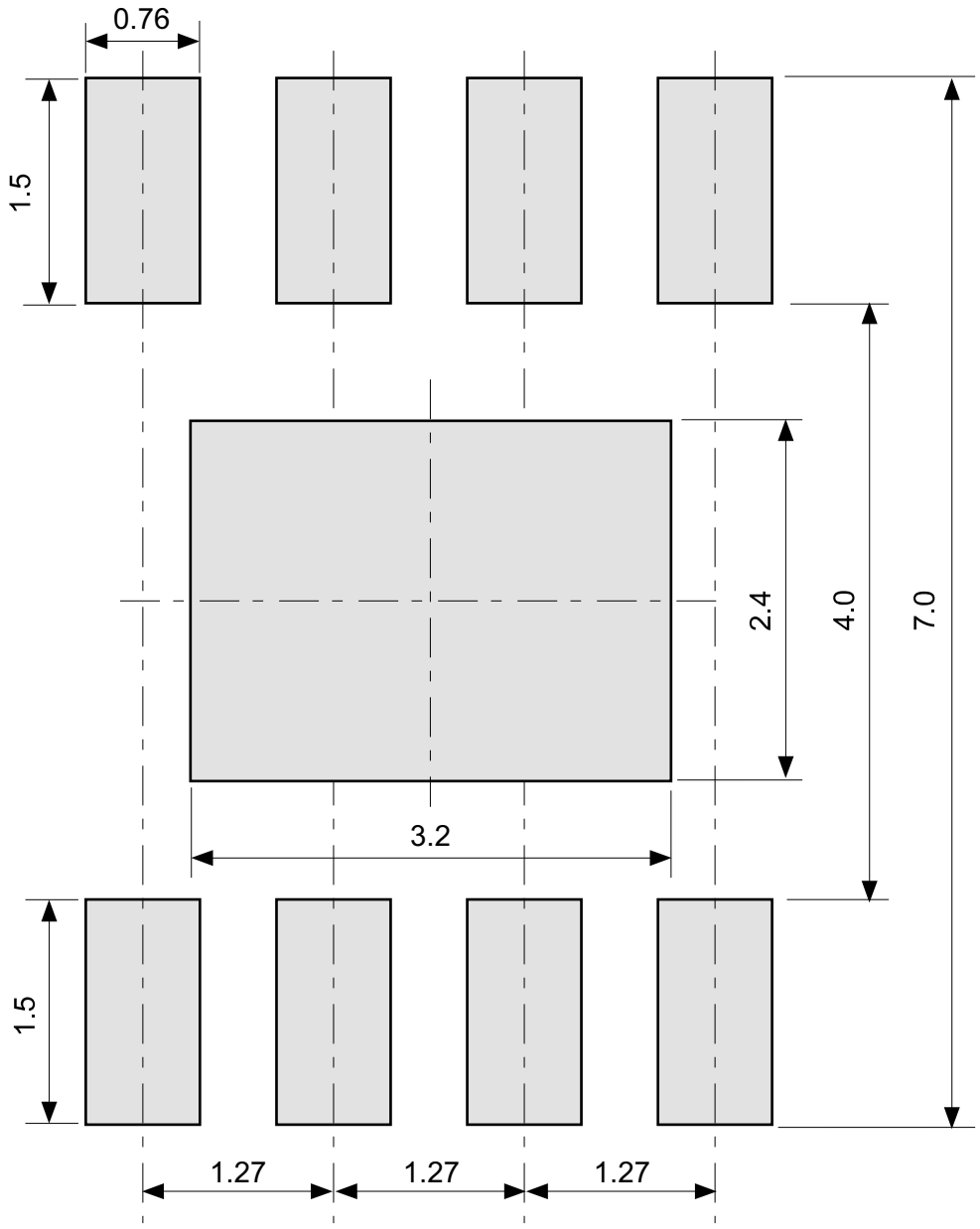


Enlarged drawing in the central part



No. FH008-A-R-SD-1.0

TITLE	HSOP8A-A-Reel		
No.	FH008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



No. FH008-A-L-SD-1.0

TITLE	HSOP8A-A -Land Recommendation
No.	FH008-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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