S-19502/19503 Series

AUTOMOTIVE, 125°C OPERATION, 36 V INPUT, 400 mA, BUILT-IN WATCHDOG TIMER CIRCUIT VOLTAGE REGULATOR WITH RESET FUNCTION

www.ablicinc.com

Rev.1.0_01

The S-19502/19503 Series, developed by using high-withstand voltage CMOS technology, is a low dropout positive voltage regulator with the watchdog timer and the reset function, which has high-withstand voltage. The monitoring time of watchdog timer can be adjusted by an external capacitor. Moreover, a voltage detection circuit which monitors the output voltage is also prepared.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.**

■ Features

Regulator block

- Output voltage: 3.0 V to 5.3 V, selectable in 0.1 V step
- Input voltage: 4.0 V to 36.0 V
- Output voltage accuracy: ±2.0% (T_j = −40°C to +150°C)
- Dropout voltage: 120 mV typ. (5.0 V output product, I_{OUT} = 100 mA)
- Output current: Possible to output 400 mA (V_{IN} = $V_{OUT(S)}$ + 1.0 V)*1
- Input and output capacitors: A ceramic capacitor of 2.2 μF or more can be used.
- Ripple rejection: 70 dB typ. (f = 100 Hz)
- Built-in overcurrent protection circuit: Limits overcurrent of output transistor.
- Built-in thermal shutdown circuit: Detection temperature 170°C typ.

Detector block

- Detection voltage: 2.6 V to 5.0 V, selectable in 0.1 V step
- Detection voltage accuracy: ±100 mV (T_j = −40°C to +150°C)
- Hysteresis width: 0.12 V min.
- Release delay time: 18 ms typ. (C_{DLY} = 47 nF)
- Output form: Nch open-drain output (Built-in pull-up resistor)

Watchdog timer block

- Autonomous watchdog operation function: The watchdog timer operates due to detection of load current.
- Watchdog activation current is adjustable: 1.5 mA typ. (WADJ pin is open)
- Product type is selectable: S-19502 Series (Product with watchdog enable function) S-19503 Series (Product without watchdog enable function)
- Watchdog trigger time is adjustable: 43 ms typ. (C_{DLY} = 47 nF)
- Output form: Nch open-drain output (Built-in pull-up resistor)

Overall

- Current consumption: 60 μA typ. (I_{OUT} = 0 mA, When the watchdog timer is deactivated.) 75 μA typ. (I_{OUT} ≤ 5 mA, When the watchdog timer is activated.)
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*2 HSOP-8A package product

***1.** Please make sure that the loss of the IC will not exceed the power dissipation when the output current is large.
***2.** TO-252-9S package product is in the process of AEC-Q100.
Contact our sales office for details.

■ Applications

- Constant-voltage power supply for automotive electric component, monitoring of microcotroller

■ Packages

- TO-252-9S
- HSOP-8A

■ Block Diagrams

1. S-19502 Series (Product with watchdog enable function)

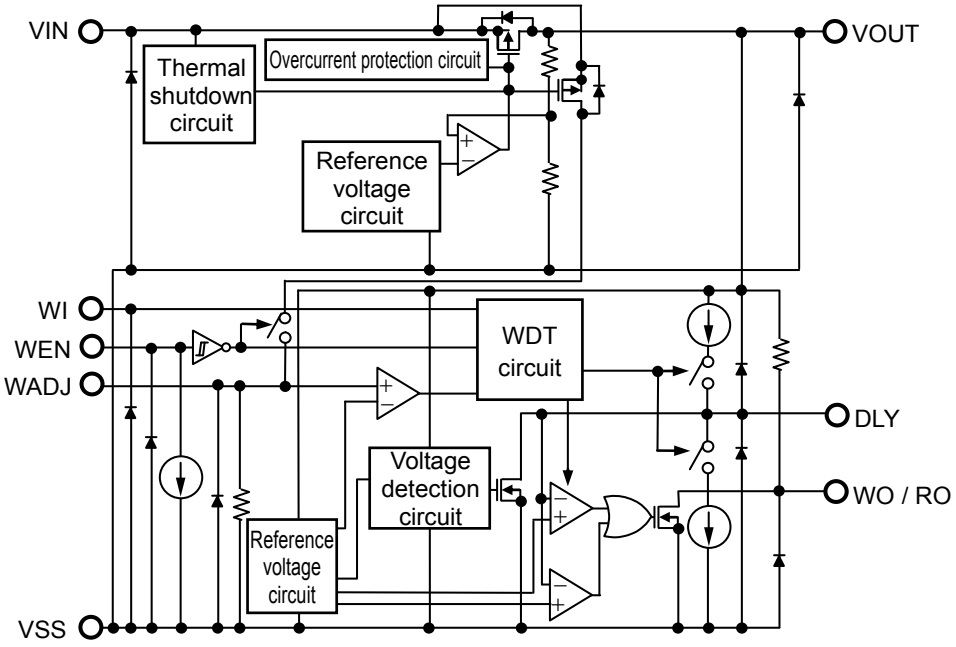


Figure 1

2. S-19503 Series (Product without watchdog enable function)

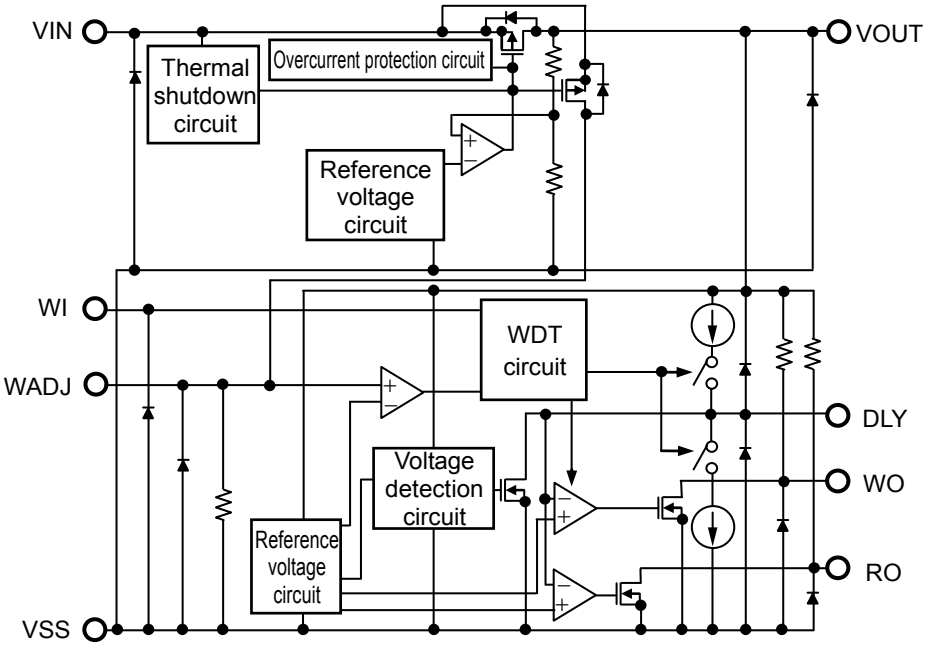


Figure 2

■ AEC-Q100 Qualified*1

This IC supports AEC-Q100 for the operation temperature grade 1.
Contact our sales office for details of AEC-Q100 reliability specification.

***1.** TO-252-9S package product is in the process of AEC-Q100.
Contact our sales office for details.

■ Product Name Structure

Users can select the product type, output voltage and detection voltage for the S-19502/19503 Series. Refer to "**1. Product name**" regarding the contents of product name, "**3. Packages**" regarding the package drawings and "**4. Product name list**" for details of product names.

1. Product name

S-1950 x A x x A - xxxx U 4

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - V9T1: TO-252-9S, Tape
  - E8T1: HSOP-8A, Tape
- Operation temperature
  - A: Ta = −40°C to +125°C
- Detection voltage*2
  - F to Z, 0 to 5
- Output voltage*2
  - C to Z, 0, 1
- Product type 1
  - A: WEN pin positive logic type
- Product type 2
  - 2: S-19502 Series (Product with watchdog enable function)
  - 3: S-19503 Series (Product without watchdog enable function)

***1.** Refer to the tape drawing.
***2.** Refer to "**2. Product option list**".

2. Product option list

2. 1 Output voltage

Set Output Voltage	Symbol
5.3 V	C
5.2 V	D
5.1 V	E
5.0 V	F
4.9 V	G
4.8 V	H
4.7 V	J
4.6 V	K
4.5 V	L
4.4 V	M
4.3 V	N
4.2 V	P

Set Output Voltage	Symbol
4.1 V	Q
4.0 V	R
3.9 V	S
3.8 V	T
3.7 V	U
3.6 V	V
3.5 V	W
3.4 V	X
3.3 V	Y
3.2 V	Z
3.1 V	0
3.0 V	1

2. 2 Detection voltage

Set Detection Voltage	Symbol
5.0 V	F
4.9 V	G
4.8 V	H
4.7 V	J
4.6 V	K
4.5 V	L
4.4 V	M
4.3 V	N
4.2 V	P
4.1 V	Q
4.0 V	R
3.9 V	S
3.8 V	T

Set Detection Voltage	Symbol
3.7 V	U
3.6 V	V
3.5 V	W
3.4 V	X
3.3 V	Y
3.2 V	Z
3.1 V	0
3.0 V	1
2.9 V	2
2.8 V	3
2.7 V	4
2.6 V	5

Remark Set output voltage ≥ Set detection voltage + 0.3 V

3. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TO-252-9S	VA009-A-P-SD	VA009-A-C-SD	VA009-A-R-SD	VA009-A-L-SD
HSOP-8A	FH008-A-P-SD	FH008-A-C-SD	FH008-A-R-SD	FH008-A-L-SD

4. Product name list

4. 1 S-19502 Series (Product with watchdog enable function)

Table 2

Output Voltage	Detection Voltage	TO-252-9S	HSOP-8A
3.3 V ± 2.0%	2.8 V ± 0.1 V	S-19502AY3A-V9T1U4	–
3.3 V ± 2.0%	2.9 V ± 0.1 V	S-19502AY2A-V9T1U4	S-19502AY2A-E8T1U4
5.0 V ± 2.0%	4.6 V ± 0.1 V	S-19502AFKA-V9T1U4	S-19502AFKA-E8T1U4
5.0 V ± 2.0%	4.7 V ± 0.1 V	S-19502AFJA-V9T1U4	–

Remark Please contact our sales office for products with specifications other than the above.

4. 2 S-19503 Series (Product without watchdog enable function)

Table 3

Output Voltage	Detection Voltage	TO-252-9S	HSOP-8A
3.3 V ± 2.0%	2.8 V ± 0.1 V	S-19503AY3A-V9T1U4	–
3.3 V ± 2.0%	2.9 V ± 0.1 V	S-19503AY2A-V9T1U4	S-19503AY2A-E8T1U4
5.0 V ± 2.0%	4.6 V ± 0.1 V	S-19503AFKA-V9T1U4	S-19503AFKA-E8T1U4
5.0 V ± 2.0%	4.7 V ± 0.1 V	S-19503AFJA-V9T1U4	–

Remark Please contact our sales office for products with specifications other than the above.

■ Pin Configurations

1. TO-252-9S

Top view

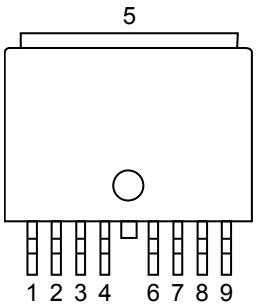


Figure 3

Table 4 S-19502 Series (Product with Watchdog Enable Function)

Pin No.	Symbol	Description	
1	VOUT	Voltage output pin (Regulator block)	
2	WADJ	Connection pin for watchdog activation threshold current adjustment resistor	
3	DLY	Connection pin for delay time adjustment capacitor	
4	NC*1	No connection	
5	VSS	GND pin	
6	WO / RO*2	WO	Watchdog output pin
		RO	Reset output pin
7	WEN	Watchdog enable pin	
8	WI	Watchdog input pin	
9	VIN	Voltage input pin (Regulator block)	

Table 5 S-19503 Series (Product without Watchdog Enable Function)

Pin No.	Symbol	Description
1	VOUT	Voltage output pin (Regulator block)
2	WADJ	Connection pin for watchdog activation threshold current adjustment resistor
3	DLY	Connection pin for delay time adjustment capacitor
4	NC*1	No connection
5	VSS	GND pin
6	RO	Reset output pin
7	WO	Watchdog output pin
8	WI	Watchdog input pin
9	VIN	Voltage input pin (Regulator block)

***1.** The NC pin is electrically open.
The NC pin can be connected to the VIN pin or the VSS pin.
***2.** The WO / RO pin combines the watchdog output pin and the reset output pin.

2. HSOP-8A

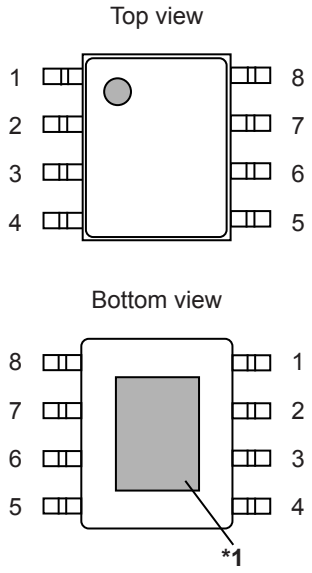


Figure 4

Table 6 S-19502 Series (Product with Watchdog Enable Function)

Pin No.	Symbol	Description	
1	VOUT	Voltage output pin (Regulator block)	
2	WADJ	Connection pin for watchdog activation threshold current adjustment resistor	
3	VSS	GND pin	
4	DLY	Connection pin for delay time adjustment capacitor	
5	WO / RO*2	WO	Watchdog output pin
		RO	Reset output pin
6	WEN	Watchdog enable pin	
7	WI	Watchdog input pin	
8	VIN	Voltage input pin (Regulator block)	

Table 7 S-19503 Series (Product without Watchdog Enable Function)

Pin No.	Symbol	Description
1	VOUT	Voltage output pin (Regulator block)
2	WADJ	Connection pin for watchdog activation threshold current adjustment resistor
3	VSS	GND pin
4	DLY	Connection pin for delay time adjustment capacitor
5	RO	Reset output pin
6	WO	Watchdog output pin
7	WI	Watchdog input pin
8	VIN	Voltage input pin (Regulator block)

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.

***2.** The WO / RO pin combines the watchdog output pin and the reset output pin.

■ Pin Functions

1. WADJ pin

This is a pin to connect an external resistor in order to adjust watchdog activation threshold current ($I_{O,WDact}$). **Table 8** shows the connection of the WADJ pin depending on the usage of the watchdog timer.
In the S-19502 Series, the watchdog timer is deactivated regardless of the connection of the WADJ pin if the watchdog timer is set to Disable by the WEN pin.

Table 8

Usage of Watchdog Timer	Connection of WADJ Pin
Watchdog timer is not in use	Connect to the VSS pin
Watchdog timer is always activated	Connect to the VOUT pin via a resistor of 270 kΩ
Watchdog timer turns on and off autonomously depending on the load current (Autonomous watchdog operation function[*1])	Open, or connect to the VSS pin via an external resistor[*2]

***1.** Refer to "**3. Watchdog timer block**" in "**■ Operation**" for details.
***2.** Refer to "**■ Selection of Watchdog Activation Threshold Current Adjustment Resistor ($R_{WADJ,ext}$)**" for details.

2. DLY pin

This is a pin to connect an external capacitor in order to adjust the release delay time (t_{rd}) of the detector and monitoring time of the watchdog timer. Refer to "**■ Selection of Delay Time Adjustment Capacitor (C_{DLY})**" for the selection of an external capacitor.

3. WO / RO pin (S-19502 Series only)

This is an output pin for the detector and the watchdog timer. The output level is AND logic of the detector and the watchdog timer. (For example, the WO / RO pin is "L" when the WO pin is "L" and the RO pin is "H".)

4. WO pin (S-19503 Series only)

This is an output pin for the watchdog timer. It outputs "H" when the watchdog timer stops or if the DLY pin voltage (V_{DLY}) exceeds the upper timing threshold voltage (V_{DU}) when the watchdog timer operates. It outputs "L" if V_{DLY} falls below the lower watchdog timing threshold voltage (V_{DWL}) when the watchdog timer operates.

5. RO pin (S-19503 Series only)

This is an output pin for the detector. It outputs "H" when V_{DLY} exceeds V_{DU}, and outputs "L" when V_{DLY} falls below the lower reset timing threshold voltage (V_{DRL}).

6. WEN pin (S-19502 Series only)

This is a pin to switch Enable / Disable of the watchdog timer.
The watchdog timer becomes Enable if the input is "H", and becomes Disable when the input is "L". Since the WEN pin has a built-in pull-down current source, the input becomes "L" when using it in open.

7. WI pin

This is an input pin to recieve a trigger signal from the monitored object by the watchdog timer. By being input a rising edge at an appropriate timing, the WI pin confirms the normal operation of the monitored object. Refer to "**3. Watchdog timer block**" in "**■ Operation**".

■ Absolute Maximum Ratings

Table 9

(T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
VIN pin voltage	V_{IN}	V_{SS} − 0.3 to V_{SS} + 45.0	V
VOUT pin voltage	V_{OUT}	V_{SS} − 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 7.0	V
DLY pin voltage	V_{DLY}	V_{SS} − 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
RO pin voltage	V_{RO}	V_{SS} − 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
WADJ pin voltage	V_{WADJ}	V_{SS} − 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 7.0	V
WEN pin voltage	V_{WEN}	V_{SS} − 0.3 to V_{SS} + 7.0	V
WI pin voltage	V_{WI}	V_{SS} − 0.3 to V_{SS} + 7.0	V
WO pin voltage	V_{WO}	V_{SS} − 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
WO / RO pin voltage	$V_{WO\,/\,RO}$	V_{SS} − 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
Output current	I_{OUT}	520	mA
Junction temperature	T_j	−40 to +150	°C
Operation ambient temperature	T_{opr}	−40 to +125	°C
Storage temperature	T_{stg}	−40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 10

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TO-252-9S	Board A	–	88	–	°C/W
			Board B	–	63	–	°C/W
			Board C	–	37	–	°C/W
			Board D	–	31	–	°C/W
			Board E	–	28	–	°C/W
		HSOP-8A	Board A	–	104	–	°C/W
			Board B	–	74	–	°C/W
			Board C	–	39	–	°C/W
			Board D	–	37	–	°C/W
			Board E	–	31	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Recommended Operation Conditions

Table 11

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VIN pin voltage	V_{IN}	–	4.0	–	36.0	V
		When using autonomous watchdog operation function*1	$V_{OUT(S)}$ + 1.0	–	36.0	V
VOUT pin voltage	V_{OUT}	Detector block	1.0	–	–	V
		Watchdog timer block	$+V_{DET}$	–	–	V
Watchdog input voltage "H"*2	V_{WIH}	–	2	–	–	V
Watchdog input voltage "L"*2	V_{WIL}	–	–	–	0.8	V
Watchdog input "H" time*2	t_{high}	$V_{WI} \geq V_{WIH}$	5.0	–	–	μs
Watchdog input "L" time*2	t_{low}	$V_{WI} \leq V_{WIL}$	5.0	–	–	μs
Slew rate*2	$\frac{dV_{WI}}{dt}$	$V_{WI} = V_{WIL} + (V_{WIH} - V_{WIL}) \times 0.1$ to $V_{WIL} + (V_{WIH} - V_{WIL}) \times 0.9$	1	–	–	V/μs
Watchdog input frequency	f_{WI}	Duty ratio 50%	–	–	0.2	MHz
WEN pin input voltage "H"	V_{WENH}	–	2.0	–	$V_{OUT(S)}$	V
WEN pin input voltage "L"	V_{WENL}	–	0	–	0.8	V

***1.** Refer to "**3. Watchdog timer block**" in "**■ Operation**" for the autonomous watchdog operation function.

***2.** When inputting a rising edge that satisfies the condition of **Figure 5** to the WI pin, the watchdog timer detects a trigger.
The signal input from the monitored object by the watchdog timer should satisfy the condition of **Figure 5**.

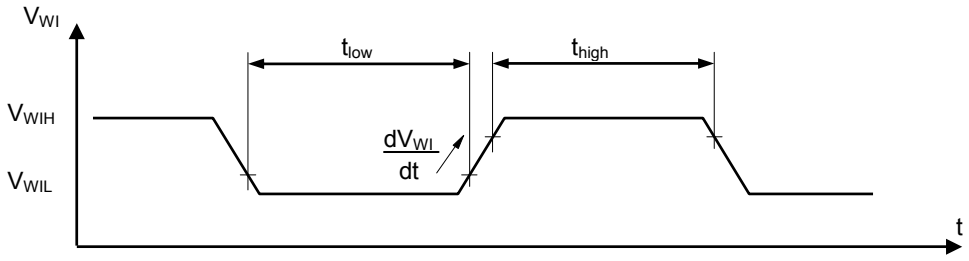


Figure 5

■ Electrical Characteristics

1. Regulator block

Table 12

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Output voltage*1	$V_{OUT(E)}$	V_{IN} = 13.5 V, I_{OUT} = 30 mA	$V_{OUT(S)}$ × 0.98	$V_{OUT(S)}$	$V_{OUT(S)}$ × 1.02	V	1
Output current*2	I_{OUT}	$V_{IN} \geq V_{OUT(S)}$ + 1.0 V	400*4	–	–	mA	2
Dropout voltage*3	V_{drop}	I_{OUT} = 100 mA, Ta = +25°C, $V_{OUT(S)}$ = 3.0 V to 5.3 V	–	120	200	mV	1
		I_{OUT} = 200 mA, Ta = +25°C, $V_{OUT(S)}$ = 3.0 V to 5.3 V	–	240	400	mV	1
Line regulation	$\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}$	$V_{OUT(S)}$ + 1.0 V ≤ V_{IN} ≤ 36.0 V, I_{OUT} = 30 mA, Ta = +25°C	–	0.02	0.10	%/V	1
Load regulation	ΔV_{OUT2}	V_{IN} = 13.5 V, 100 μA ≤ I_{OUT} ≤ 100 mA, Ta = +25°C	–	20	40	mV	1
Input voltage	V_{IN}	–	4.0	–	36.0	V	–
Ripple rejection	|RR|	V_{IN} = 13.5 V, I_{OUT} = 30 mA, f = 100 Hz, ΔV_{rip} = 1.0 V_{p-p}	–	70	–	dB	3
Short-circuit current	I_{short}	V_{IN} = 13.5 V, V_{OUT} = 0 V, Ta = +25°C	–	105	–	mA	2
Thermal shutdown detection temperature	T_{SD}	Junction temperature	–	170	–	°C	–
Thermal shutdown release temperature	T_{SR}	Junction temperature	–	135	–	°C	–

***1.** $V_{OUT(S)}$: Set output voltage
$V_{OUT(E)}$: Actual output voltage
Output voltage when fixing I_{OUT} (= 30 mA) and inputting 13.5 V

***2.** The output current at which the output voltage becomes 95% of $V_{OUT(E)}$ after gradually increasing the output current.

***3.** $V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$
V_{OUT3} is the output voltage when $V_{IN} = V_{OUT(S)}$ + 1.0 V.
V_{IN1} is the input voltage at which the output voltage becomes 98% of V_{OUT3} after gradually decreasing the input voltage.

***4.** The output current can be at least this value.
Due to limitation of the power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation when the output current is large.
This specification is guaranteed by design.

2. Detector block

Table 13

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	−	$-V_{DET(S)}$ − 0.1	$-V_{DET(S)}$	$-V_{DET(S)}$ + 0.1	V	4
Hysteresis width	V_{HYS}	−	120	150	−	mV	4
Reset output voltage "H"	V_{ROH}	−	$V_{OUT(S)}$ × 0.9	−	−	V	4
Reset output voltage "L"	V_{ROL}	$V_{OUT} \geq$ 1.0 V, $R_{extR} \geq$ 3 kΩ, Connect to VOUT pin	−	0.2	0.4	V	4
Reset pull-up resistance	R_{RO}	VOUT pin internal resistance	20	30	45	kΩ	−
Reset output current	I_{RO}	V_{RO} = 0.4 V, $V_{OUT} = -V_{DET(S)} - 0.1$ V	3.0	−	−	mA	5
Lower reset timing threshold voltage	V_{DRL}	−	0.2	0.3	0.4	V	6
Upper timing threshold voltage	V_{DU}	−	1.5	1.9	2.3	V	6
Charge current	$I_{D,cha}$	V_{DLY} = 1.0 V	2.0	5.0	8.0	μA	6
Release delay time*2	t_{rd}	C_{DLY} = 47 nF	11	18	25	ms	4
Reset reaction time*3	t_{rr}	C_{DLY} = 47 nF	−	−	50	μs	4

***1.** $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Set detection voltage

***2.** The time period from when V_{OUT} changes to $-V_{DET(S)} - 0.15$ V → $V_{OUT(S)}$ to when V_{RO} reaches V_{OUT} / 2.

***3.** The time period from when V_{OUT} changes to $V_{OUT(S)} \rightarrow -V_{DET(S)} - 0.15$ V to when V_{RO} reaches V_{OUT} / 2.

3. Watchdog timer block

3. 1 S-19502 Series (Product with watchdog enable function)

Table 14

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Watchdog activation threshold current	$I_{O,WDact}$	WADJ pin is open	1.1	1.5	1.9	mA	7
Watchdog deactivation threshold current	$I_{O,WDdeact}$	WADJ pin is open	−	1.3	−	mA	7
Watchdog activation hysteresis current	$I_{O,WDhys}$	WADJ pin is open	0.1	0.2	−	mA	7
Watchdog activation threshold voltage	$V_{WADJ,th}$	−	1.28	1.35	1.45	V	8
WADJ pin current ratio	$\frac{I_{OUT}}{I_{WADJ}}$	V_{WADJ} = 0 V, I_{OUT} = 10 mA	−	750	−	−	8
WADJ pin internal resistance	$R_{WADJ,int}$	−	490	650	845	kΩ	−
Charge curernt	$I_{D,cha}$	V_{DLY} = 1.0 V	2	5	8	μA	9
Discharge current	$I_{D,dcha}$	V_{DLY} = 1.0 V	0.6	1.3	2.0	μA	9
Upper timing threshold voltage	V_{DU}	−	1.5	1.9	2.3	V	9
Lower watchdog timing threshold voltage	V_{DWL}	−	0.5	0.7	0.9	V	9
Watchdog output pulse period	$t_{WD,p}$	C_{DLY} = 47 nF	38	54	72	ms	7
Watchdog output "L" time	$t_{WD,l}$	$V_{OUT} > -V_{DET}$, C_{DLY} = 47 nF Watchdog timer is activated	6	11	16	ms	7
Watchdog trigger time	$t_{WI,tr}$	C_{DLY} = 47 nF	32	43	56	ms	7
WEN pin input voltage "H"	V_{SH}	−	2	−	−	V	10
WEN pin input voltage "L"	V_{SL}	−	−	−	0.8	V	10
WEN pin input current "H"	I_{SH}	V_{WEN} = $V_{OUT(S)}$	−	−	1	μA	10
WEN pin input current "L"	I_{SL}	V_{WEN} = 0 V	−	−	0.1	μA	10

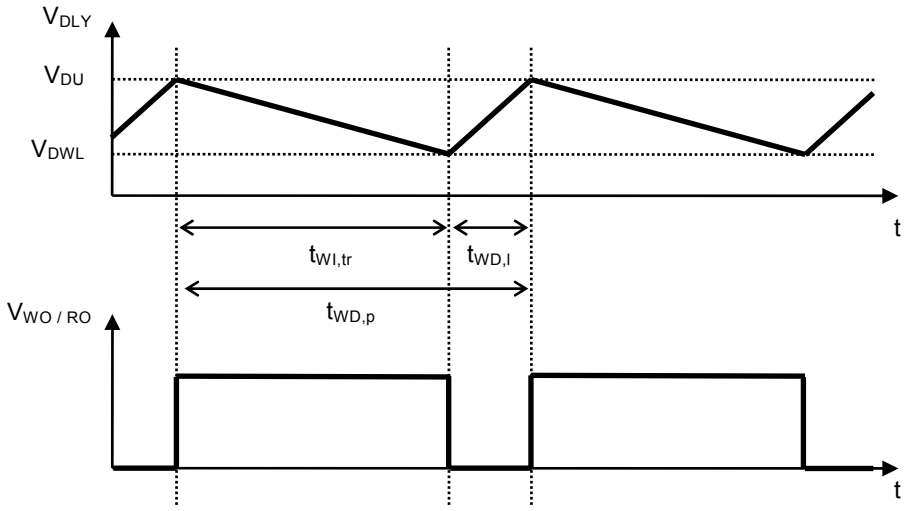


Figure 6

3. 2 S-19503 Series (Product without watchdog enable function)

Table 15

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Watchdog activation threshold current	$I_{O,WDact}$	WADJ pin is open	1.1	1.5	1.9	mA	7
Watchdog deactivation threshold current	$I_{O,WDdeact}$	WADJ pin is open	–	1.3	–	mA	7
Watchdog activation hysteresis current	$I_{O,WDhys}$	WADJ pin is open	0.1	0.2	–	mA	7
Watchdog activation threshold voltage	$V_{WADJ,th}$	–	1.28	1.35	1.45	V	8
WADJ pin current ratio	$\frac{I_{OUT}}{I_{WADJ}}$	V_{WADJ} = 0 V, I_{OUT} = 10 mA	–	750	–	–	8
WADJ pin internal resistance	$R_{WADJ,int}$	–	490	650	845	kΩ	–
Watchdog output voltage "H"	V_{WOH}	–	$V_{OUT(S)}$ × 0.9	–	–	V	13
Watchdog output voltage "L"	V_{WOL}	R_{extW} ≥ 3 kΩ, Connect to VOUT pin	–	0.2	0.4	V	13
Watchdog pull-up resistance	R_{WO}	VOUT pin internal resistance	20	30	45	kΩ	–
Watchdog output current	I_{WO}	V_{WO} = 0.4 V, V_{OUT} = $-V_{DET(S)}$ − 0.1 V	3.0	–	–	mA	14
Charge current	$I_{D,cha}$	V_{DLY} = 1.0 V	2	5	8	μA	9
Discharge current	$I_{D,dcha}$	V_{DLY} = 1.0 V	0.6	1.3	2.0	μA	9
Upper timing threshold voltage	V_{DU}	–	1.5	1.9	2.3	V	9
Lower watchdog timing threshold voltage	V_{DWL}	–	0.5	0.7	0.9	V	9
Watchdog output pulse period	$t_{WD,p}$	C_{DLY} = 47 nF	38	54	72	ms	7
Watchdog output "L" time	$t_{WD,l}$	V_{OUT} > $-V_{DET}$, C_{DLY} = 47 nF Watchdog timer is activated	6	11	16	ms	7
Watchdog trigger time	$t_{WI,tr}$	C_{DLY} = 47 nF	32	43	56	ms	7

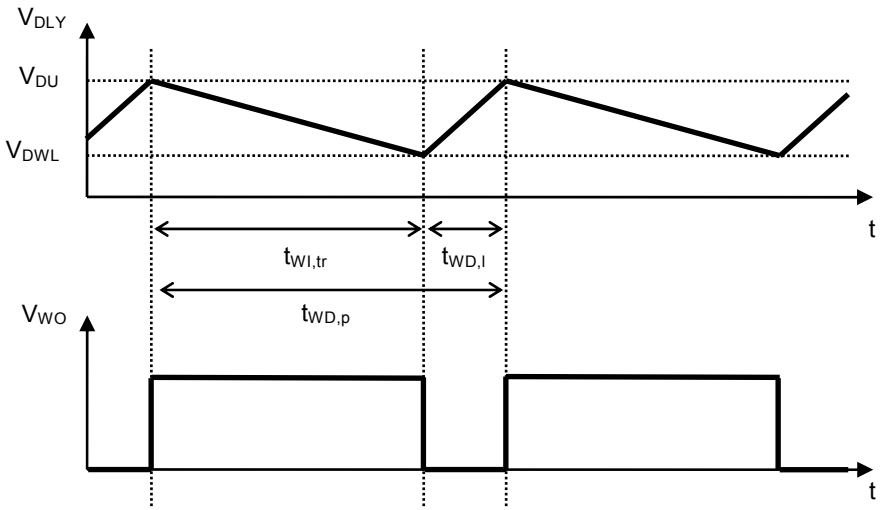


Figure 7

4. Overall

Table 16

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption during operation	I_{SS1}	$I_{OUT} \leq$ 5 mA, WADJ pin is open, Watchdog timer is activated, WO pin = "H"	−	75	115	μA	11
		I_{OUT} = 50 mA, WADJ pin is open, Watchdog timer is activated, WO pin = "H"	−	80	125	μA	11
		I_{OUT} = 200 mA, WADJ pin is open, Watchdog timer is activated, WO pin = "H"	−	100	150	μA	11
Current consumption when watchdog timer is deactivated	I_{SS2}	I_{OUT} = 0 mA, Watchdog timer is deactivated	−	60	95	μA	12

■ Test Circuits

1. S-19502 Series (Product with watchdog enable function)

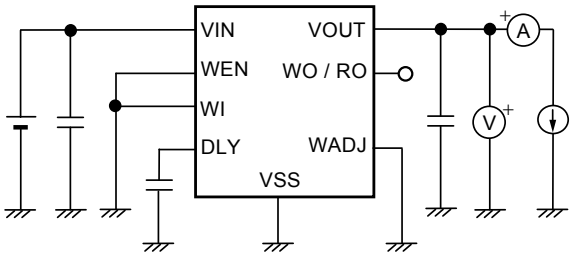


Figure 8 Test Circuit 1

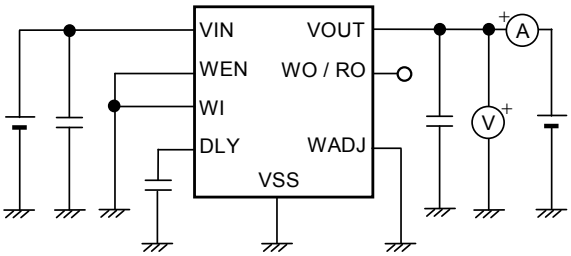


Figure 9 Test Circuit 2

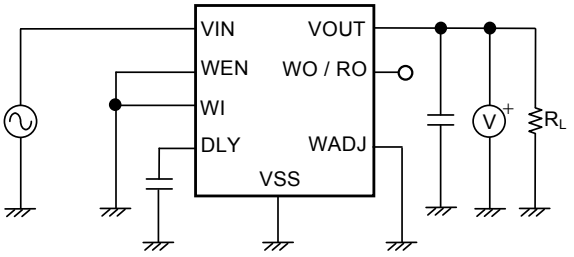


Figure 10 Test Circuit 3

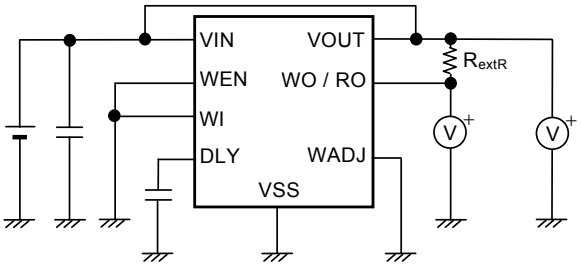


Figure 11 Test Circuit 4

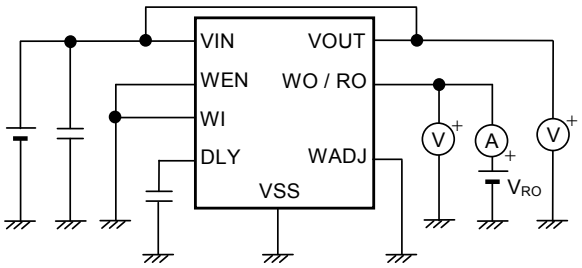


Figure 12 Test Circuit 5

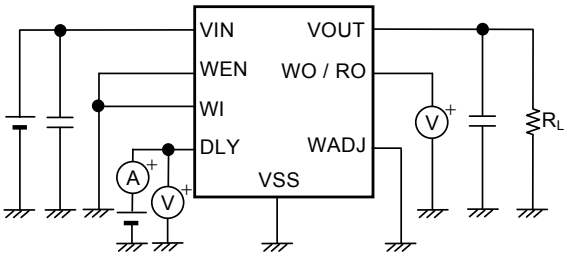


Figure 13 Test Circuit 6

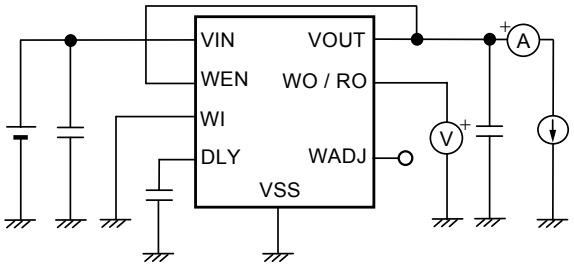


Figure 14 Test Circuit 7

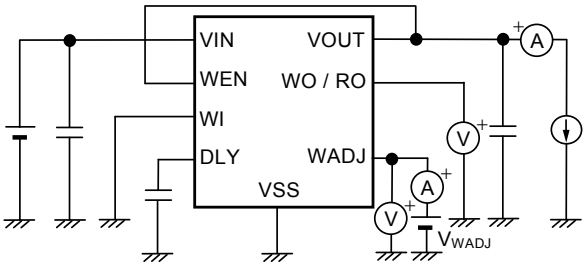
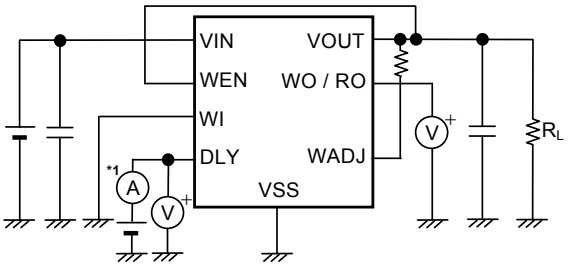


Figure 15 Test Circuit 8



***1.** Charge current: the direction of the current which flows out of the IC is positive
Discharge current: the direction of the current which flows into the IC is positive

Figure 16 Test Circuit 9

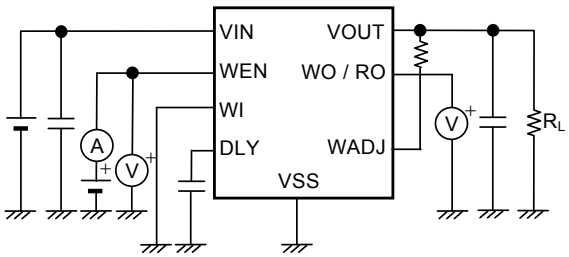


Figure 17 Test Circuit 10

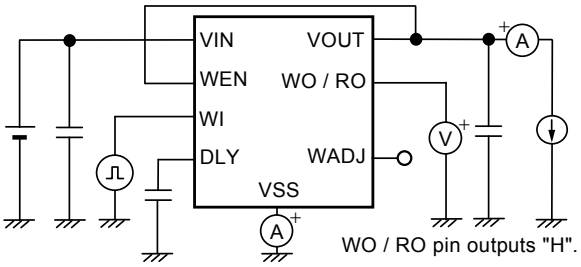


Figure 18 Test Circuit 11

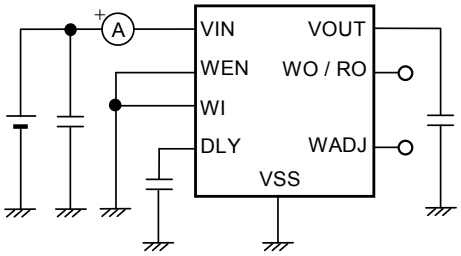


Figure 19 Test Circuit 12

2. S-19503 Series (Product without watchdog enable function)

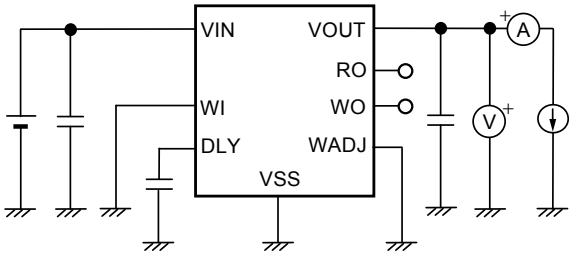


Figure 20 Test Circuit 1

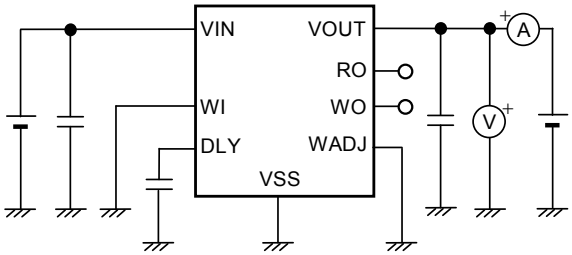


Figure 21 Test Circuit 2

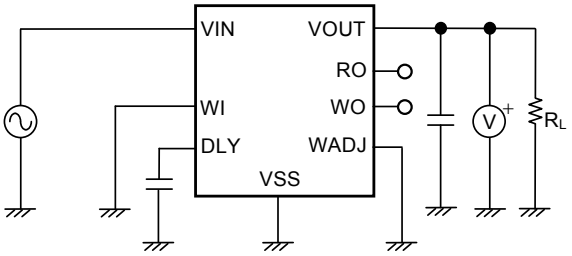


Figure 22 Test Circuit 3

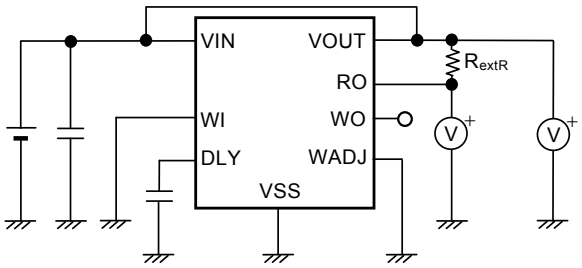


Figure 23 Test Circuit 4

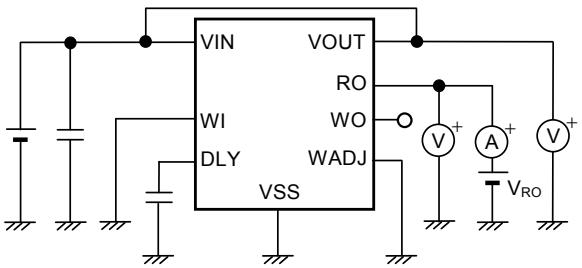


Figure 24 Test Circuit 5

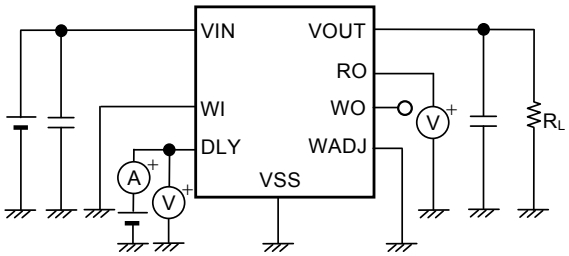


Figure 25 Test Circuit 6

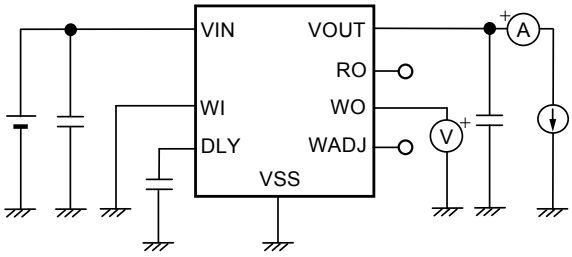


Figure 26 Test Circuit 7

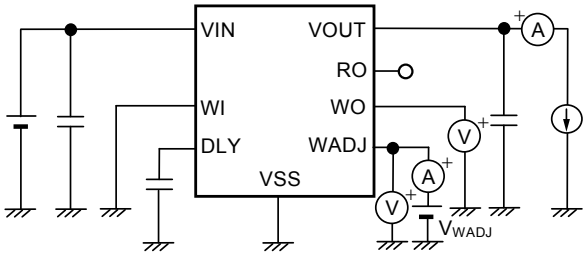
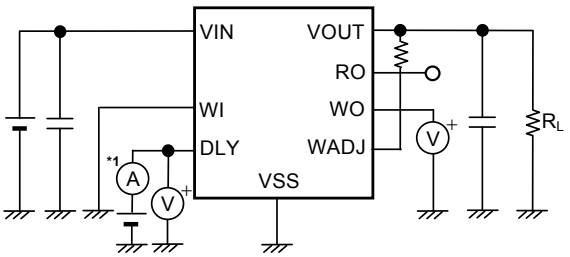


Figure 27 Test Circuit 8



***1.** Charge current: the direction of the current which flows out of the IC is positive
Discharge current: the direction of the current which flows into the IC is positive

Figure 28 Test Circuit 9

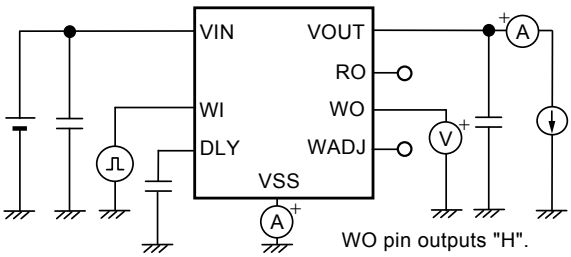


Figure 29 Test Circuit 11

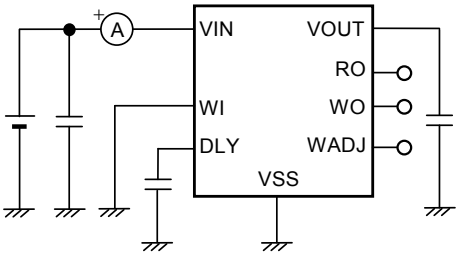


Figure 30 Test Circuit 12

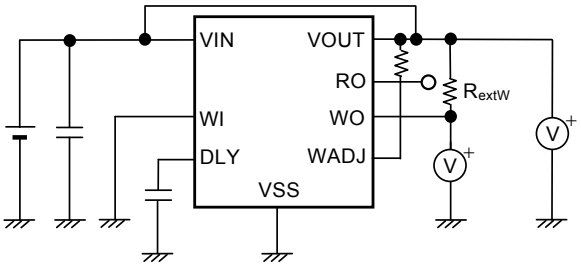


Figure 31 Test Circuit 13

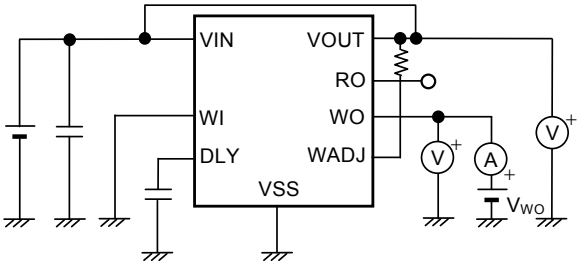


Figure 32 Test Circuit 14

■ Standard Circuits

1. S-19502 Series (Product with watchdog enable function)

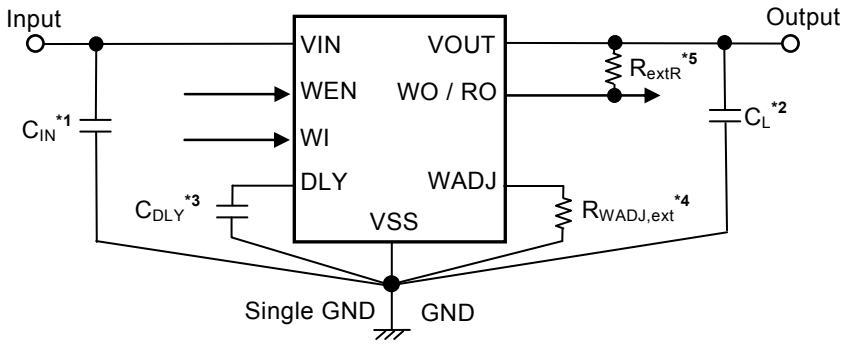


Figure 33

2. S-19503 Series (Product without watchdog enable function)

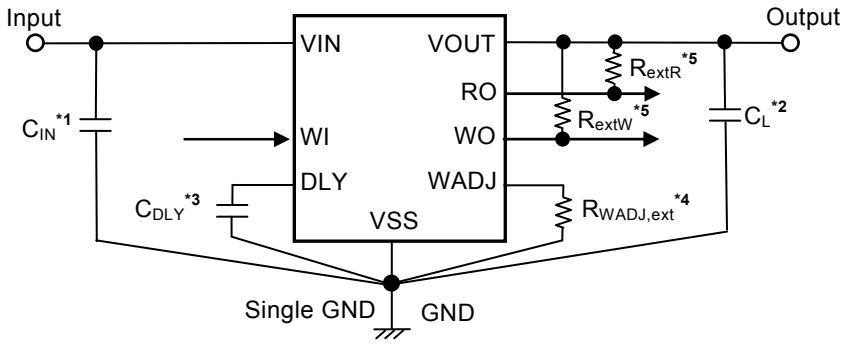


Figure 34

***1.** C_{IN} is a capacitor for stabilizing the input.

***2.** C_L is a capacitor for stabilizing the output. A ceramic capacitor of 2.2 μF or more can be used.

***3.** C_{DLY} is the delay time adjustment capacitor.

***4.** $R_{WADJ,ext}$ is the watchdog activation threshold current adjustment resistor.

***5.** R_{extR} and R_{extW} are the external pull-up resistors for the reset output pin and the watchdog output pin, respectively. Connection of the external pull-up resistor is not absolutely essential since the S-19502/19503 Series has a built-in pull-up resistor.

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.

■ Condition of Application

Input capacitor (C_{IN})	: 2.2 μF or more
Output capacitor (C_L)	: 2.2 μF or more
ESR of output capacitor	: 50 Ω or less
Delay time adjustment capacitor (C_{DLY})	: 1.0 nF or more
Watchdog activation threshold current adjustment resistor ($R_{WADJ,ext}$)	: 10 kΩ or more
External pull-up resistors (R_{extR}, R_{extW})	: 3 kΩ or more

Caution Generally a series regulator may cause oscillation, depending on the selection of external parts. Confirm that no oscillation occurs in the application for which the above capacitors are used.

■ Selection of Input and Output Capacitors (C_{IN}, C_L)

The S-19502/19503 Series requires C_L between the VOUT pin and the VSS pin for phase compensation. Operation is stabilized by a ceramic capacitor with an output capacitance of 2.2 μF or more over the entire temperature range. When using an OS capacitor, a tantalum capacitor, or an aluminum electrolytic capacitor, the capacitance must be 2.2 μF or more, and the ESR must be 50 Ω or less.
The values of output overshoot and undershoot, which are transient response characteristics, vary depending on the value of the output capacitor.
The required value of capacitance for the input capacitor differs depending on the application.

Caution Define the capacitance of C_{IN} and C_L by sufficient evaluation including the temperature characteristics under the actual usage conditions.

■ Selection of Delay Time Adjustment Capacitor (C_{DLY})

In the S-19502/19503 Series, the delay time adjustment capacitor (C_{DLY}) is necessary between the DLY pin and the VSS pin to adjust the release delay time (t_{rd}) of the detector and the monitoring time of the watchdog timer.
The set release delay time ($t_{rd(S)}$), the set watchdog trigger time ($t_{WI,tr(S)}$), the set watchdog output "L" time ($t_{WD,l(S)}$) and the set watchdog output pulse period ($t_{WD,p(S)}$) are calculated by using following equations, respectively.
The release delay time (t_{rd}), the watchdog trigger time ($t_{WI,tr}$), the watchdog output "L" time ($t_{WD,l}$) and the watchdog output pulse period ($t_{WD,p}$) at the time of the condition of C_{DLY} = 47 nF are shown in "■ **Electrical Characteristics**".

$$t_{rd(S)}\ [\text{ms}] = t_{rd}\ [\text{ms}] \times \frac{C_{DLY}\ [\text{nF}]}{47\ [\text{nF}]}$$

$$t_{WI,tr(S)}\ [\text{ms}] = t_{WI,tr}\ [\text{ms}] \times \frac{C_{DLY}\ [\text{nF}]}{47\ [\text{nF}]}$$

$$t_{WD,l(S)}\ [\text{ms}] = t_{WD,l}\ [\text{ms}] \times \frac{C_{DLY}\ [\text{nF}]}{47\ [\text{nF}]}$$

$$t_{WD,p(S)}\ [\text{ms}] = t_{WI,tr(S)}\ [\text{ms}] + t_{WD,l(S)}\ [\text{ms}]$$

Caution 1. The above equations will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics using an actual application to set the constants.

2. Mounted board layout should be made in such a way that no current flows into or flows from the DLY pin since the impedance of the DLY pin is high, otherwise correct delay time and monitoring time may not be provided.

3. Select C_{DLY} whose leakage current can be ignored against the built-in constant current. The leakage current may cause deviation in delay time and monitoring time. When the leakage current is larger than the built-in constant current, no release takes place.

■ Selection of Watchdog Activation Threshold Current Adjustment Resistor ($R_{WADJ,ext}$)

In the S-19502/19503 Series, the watchdog activation threshold current adjustment resistor ($R_{WADJ,ext}$) can be connected between the WADJ pin and the VSS pin to adjust the watchdog timer activation threshold current.
The set watchdog activation threshold current ($I_{O,WDact(S)}$), the set watchdog deactivation threshold current ($I_{O,WDdeact(S)}$) and the set watchdog activation hysteresis current ($I_{O,WDhys(s)}$) are calculated by using following equations, respectively.
The watchdog activation threshold current ($I_{O,WDact}$), the watchdog deactivation threshold current ($I_{O,WDdeact}$) and the watchdog activation hysteresis current ($I_{O,WDhys}$) when the WADJ pin is open are shown in "**■ Electrical Characteristics**".

$$I_{O,WDact(S)}\ [mA] = I_{O,WDact}\ [mA] \times \left(1 + \frac{R_{WADJ,int}\ [k\Omega]}{R_{WADJ,ext}\ [k\Omega]}\right)$$

$$I_{O,WDdeact(S)}\ [mA] = I_{O,WDdeact}\ [mA] \times \left(1 + \frac{R_{WADJ,int}\ [k\Omega]}{R_{WADJ,ext}\ [k\Omega]}\right)$$

$$I_{O,WDhys(S)}\ [mA] = I_{O,WDact(S)}\ [mA] - I_{O,WDdeact(S)}\ [mA]$$

Caution 1. The above equations will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics using an actual application to set the constants.

2. Mounted board layout should be made in such a way that no current flows into or flows from the WADJ pin since the impedance of the WADJ pin is high, otherwise correct $I_{O,WDact}$ and $I_{O,WDdeact}$ may not be provided.

■ Explanation of Terms

1. Regulator block

1. 1 Low dropout voltage regulator

This voltage regulator has the low dropout voltage due to its built-in low on-resistance transistor.

1. 2 Output voltage (V_{OUT})

The accuracy of the output voltage is ensured at ±2.0% under specified conditions of fixed input voltage[*1], fixed output current, and fixed temperature.

***1.** Differs depending on the product.

Caution If the above conditions change, the output voltage value may vary and exceed the accuracy range of the output voltage. Refer to "1. Regulator block" in "■ Electrical Characteristics" and "1. Regulator block" in "■ Characteristics (Typical Data)" for details.

1. 3 Line regulation $\left(\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}\right)$

Indicates the dependency of the output voltage against the input voltage. That is, the value shows how much the output voltage changes due to a change in the input voltage after fixing output current constant.

1. 4 Load regulation (ΔV_{OUT2})

Indicates the dependency of the output voltage against the output current. That is, the value shows how much the output voltage changes due to a change in the output current after fixing input voltage constant.

1. 5 Dropout voltage (V_{drop})

Indicates the difference between input voltage (V_{IN1}) and the output voltage when; decreasing input voltage (V_{IN}) gradually until the output voltage has dropped out to the value of 98% of output voltage (V_{OUT3}), which is at V_{IN} = $V_{OUT(S)}$ + 1.0 V.

$V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$

2. Detector block

2. 1 Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output of the RO pin turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (Refer to **Figure 35**).

2. 2 Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output of the RO pin turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (Refer to **Figure 36**). This value is calculated from the actual detection voltage ($-V_{DET}$) of a product and the hysteresis width (V_{HYS}), and is $+V_{DET} = -V_{DET} + V_{HYS}$.

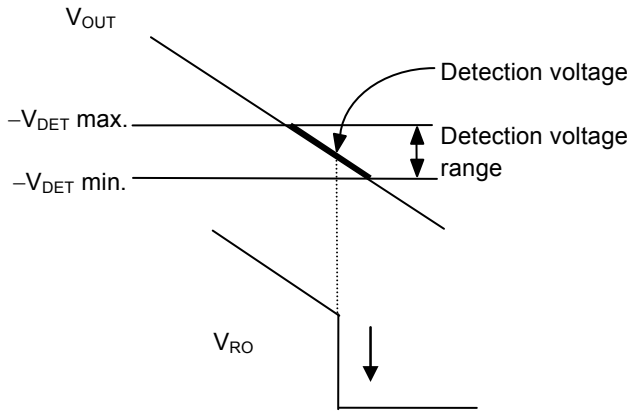


Figure 35 Detection Voltage

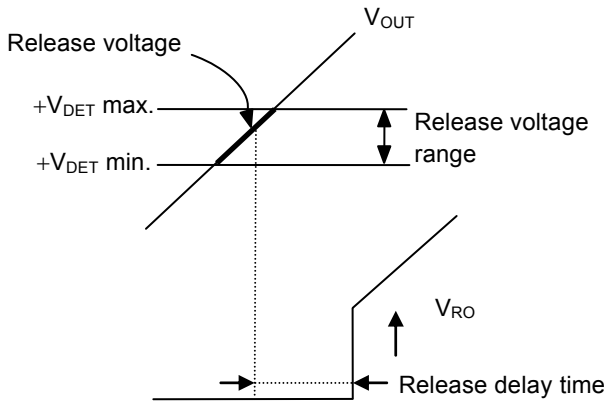


Figure 36 Release Voltage

2. 3 Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage. Setting the hysteresis width between the detection voltage and the release voltage prevents malfunction caused by noise on the VOUT pin voltage (V_{OUT}).

2. 4 Release delay time (t_{rd})

The release delay time is the time period from when V_{OUT} exceeds the release voltage ($+V_{DET}$) to when the RO pin output inverts (Refer to **Figure 37**), and this value changes according to the delay time adjustment capacitor (C_{DLY}). t_{rd} is determined by a built-in constant current which charges C_{DLY}, the charge detection threshold of the DLY pin, and the capacitance of C_{DLY}. It is calculated by using the following equation.

$$t_{rd} = C_{DLY} \times \frac{V_{DU}}{I_{D,cha}}$$

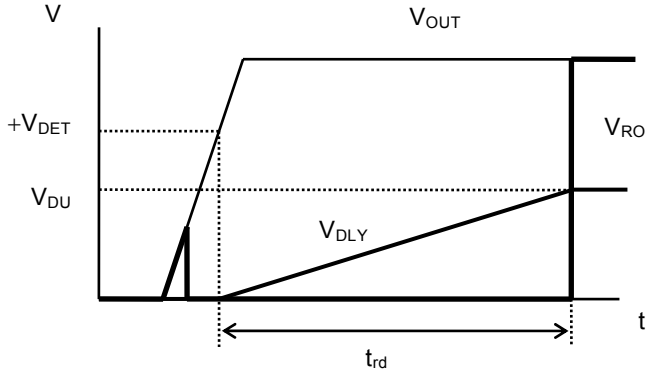


Figure 37 Release Delay Time

2. 5 Reset reaction time (t_{rr})

The reset reaction time is the time period from when V_{OUT} falls below the detection voltage ($-V_{DET}$) to when the RO pin output inverts (Refer to **Figure 38**). Since t_{rr} depends on the reaction time of internal circuit and the discharge time of C_{DLY}, it becomes longer if the capacitance of C_{DLY} becomes larger. Refer to "**2. 9 Reset reaction time vs. Capacitance for delay time adjustment capacitor**" in "**■ Characteristics (Typical Data)**".

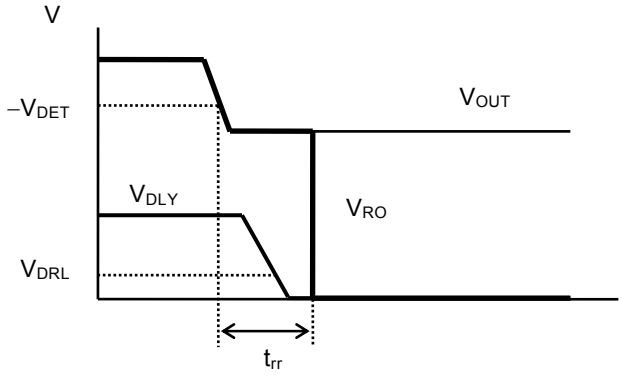


Figure 38 Reset Reaction Time

Caution Values shown in "2. Detector block" in "■ Electrical Characteristics" are values when watchdog timer stops. t_{rr} may shorten since the discharge operation of C_{DLY} may be performed while the watchdog timer operates.

3. Watchdog timer block

3. 1 Watchdog trigger time ($t_{WI,tr}$)

The watchdog trigger time is the time period from when the watchdog timer initiates the detection of a trigger signal to when a time-out is detected and the WO pin output changes to "L" (Refer to **Figure 39**). This value changes according to C_{DLY}. $t_{WI,tr}$ is determined by a built-in constant current which charges C_{DLY}, the charge detection threshold of the DLY pin, and the capacitance of C_{DLY}. It is calculated by using the following equation.

$$t_{WI,tr} = C_{DLY} \times \frac{(V_{DU} - V_{DWL})}{I_{D,dcha}}$$

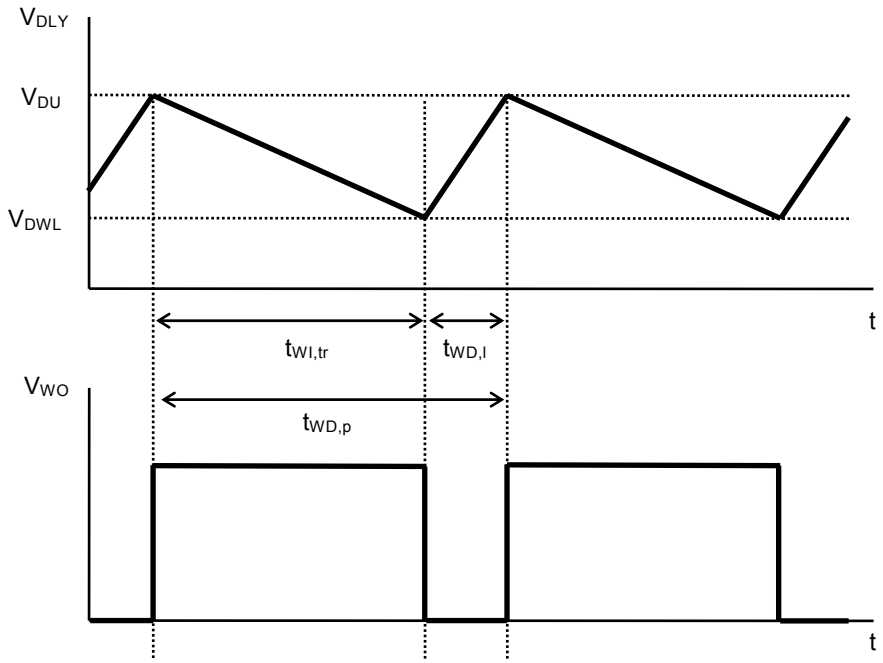


Figure 39 Watchdog Trigger Time

3. 2 Watchdog output "L" time ($t_{WD,I}$)

The watchdog output "L" time is the time period when the WO pin continues "L" after the watchdog timer detects a time-out. This value changes according to C_{DLY}, and is calculated by using the following equation.

$$t_{WD,I} = C_{DLY} \times \frac{(V_{DU} - V_{DWL})}{I_{D,dcha}}$$

3. 3 Watchdog output pulse period ($t_{WD,p}$)

The watchdog output pulse period is the period of the continuous rectangular wave that appears in the WO pin when the watchdog timer repeats the detection of a time-out. It is calculated by using the following equation.

$$t_{WD,p} = t_{WI,tr} + t_{WD,I}$$

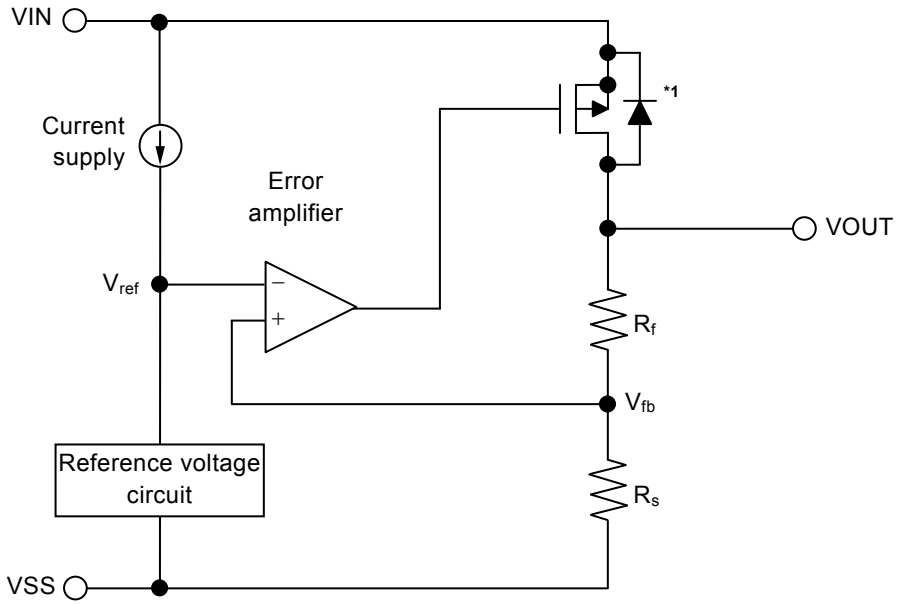
Caution Values shown in "3. Watchdog timer block" in "■ Electrical Characteristics" and "■ Characteristics (Typical Data)" are values when V_{OUT} decreases to $-V_{DET}$ or lower and the discharge operation of C_{DLY} due to the detector operation is not performed.
The discharge operation of C_{DLY} could be performed when V_{OUT} decreases to $-V_{DET}$ or lower, at that time, $t_{WI,tr}$, $t_{WD,I}$ and $t_{WD,p}$ may be changed.

■ Operation

1. Regulator block

1. 1 Basic operation

Figure 40 shows the block diagram of the regulator in the S-19502/19503 Series.
The error amplifier compares the reference voltage (V_{ref}) with feedback voltage (V_{fb}), which is the output voltage resistance-divided by feedback resistors (R_s and R_f). It supplies the gate voltage necessary to maintain the constant output voltage which is not influenced by the input voltage and temperature change, to the output transistor.



***1.** Parasitic diode

Figure 40

1. 2 Output transistor

In the S-19502/19503 Series, a low on-resistance P-channel MOS FET is used as the output transistor.
Be sure that V_{OUT} does not exceed $V_{IN} + 0.3$ V to prevent the voltage regulator from being damaged due to reverse current flowing from the VOUT pin through a parasitic diode to the VIN pin, when the potential of V_{OUT} became higher than V_{IN}.

1. 3 Overcurrent protection circuit

The S-19502/19503 Series includes an overcurrent protection circuit which having the characteristics shown in "**1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)"** of "**1. Regulator block**" in "**■ Characteristics (Typical Data)**", in order to limit an excessive output current and overcurrent of the output transistor due to short-circuiting between the VOUT pin and the VSS pin. The current when the output pin is short-circuited (I_{short}) is internally set at approx. 105 mA typ., and the load current when short-circuiting is limited based on this value. The output voltage restarts regulating if the output transistor is released from overcurrent status.

Caution This overcurrent protection circuit does not work as for thermal protection. If this IC long keeps short circuiting, pay attention to the conditions of input voltage and load current so that, under the usage conditions including short circuit, the loss of the IC will not exceed power dissipation.

1. 4 Thermal shutdown circuit

The S-19502/19503 Series has a thermal shutdown circuit to limit self-heating. When the junction temperature rises to 170°C typ., the thermal shutdown circuit operates to stop regulating. After that, when the junction temperature drops to 135°C typ., the thermal shutdown circuit is released to restart regulating.
Due to self-heating of the S-19502/19503 Series, if the thermal shutdown circuit starts operating, it stops regulating so that the output voltage drops. For this reason, self-heating is limited and the IC's temperature drops. When the temperature drops, the thermal shutdown circuit is released to restart regulating, thus self-heating is generated again due to rising of the output voltage. Repeating this procedure makes the waveform of the VOUT pin output into a pulse-like form. This phenomenon continues unless decreasing either or both of the input voltage and the output current in order to reduce the internal power consumption, or decreasing the ambient temperature. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously.

Table 17

Thermal Shutdown Circuit	VOUT Pin Voltage
Detect: 170°C typ.*1	V_{SS} level
Release: 135°C typ.*1	Set value

***1.** Junction temperature

2. Detector block

2. 1 Basic operation

(1) When the output voltage (V_{OUT}) of the regulator is release voltage ($+V_{DET}$) of the detector or higher, the Nch transistor (N1 and N2) are turned off and "H" is output to the RO pin. Since the Pch transistor (P1) is turned on, the input voltage to the comparator (C1) is $\frac{R_B \bullet V_{OUT}}{R_A + R_B}$.

(2) Even if V_{OUT} decreases to $+V_{DET}$ or lower, "H" is output to the RO pin when V_{OUT} is the detection voltage ($-V_{DET}$) or higher. When V_{OUT} decreases to $-V_{DET}$ (point A in **Figure 42**) or lower, N1 which is controlled by C1 is turned on, and C_{DLY} is discharged. If the DLY pin voltage (V_{DLY}) decreases to the lower reset timing threshold voltage (V_{DRL}) or lower, N2 of output stage of C2 is turned on, and then "L" is output to the RO pin. At this time, P1 is turned off, and the input voltage to C1 is $\frac{R_B \bullet V_{OUT}}{R_A + R_B + R_C}$.

(3) If V_{OUT} further decreases to the IC's minimum operation voltage or lower, the RO pin output is "H".

(4) When V_{OUT} increases to the IC's minimum operation voltage or higher, "L" is output to the RO pin. Moreover, even if V_{OUT} exceeds $-V_{DET}$, the output is "L" when V_{OUT} is lower than $+V_{DET}$.

(5) When V_{OUT} increases to $+V_{DET}$ (point B in **Figure 42**) or higher, N1 is turned off and C_{DLY} is charged. N2 is turned off if V_{DLY} increases to the upper timing threshold voltage (V_{DU}) or higher, and "H" is output to the RO pin.

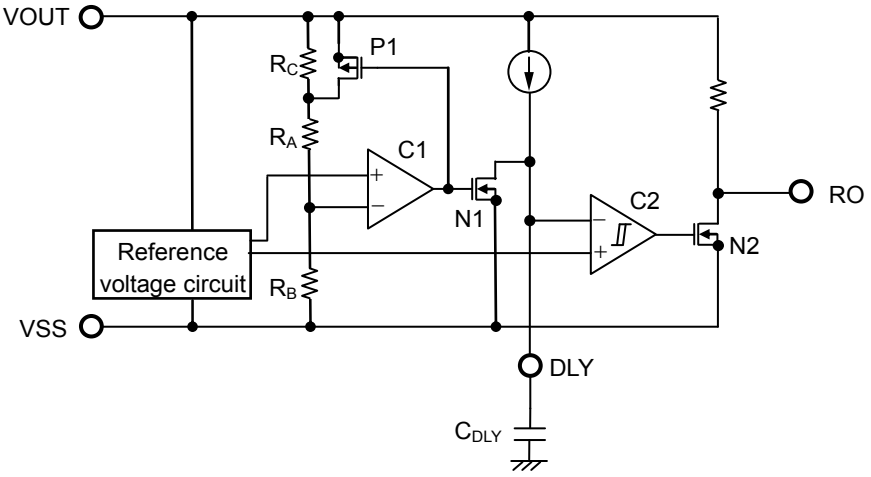


Figure 41 Operation of Detector Block

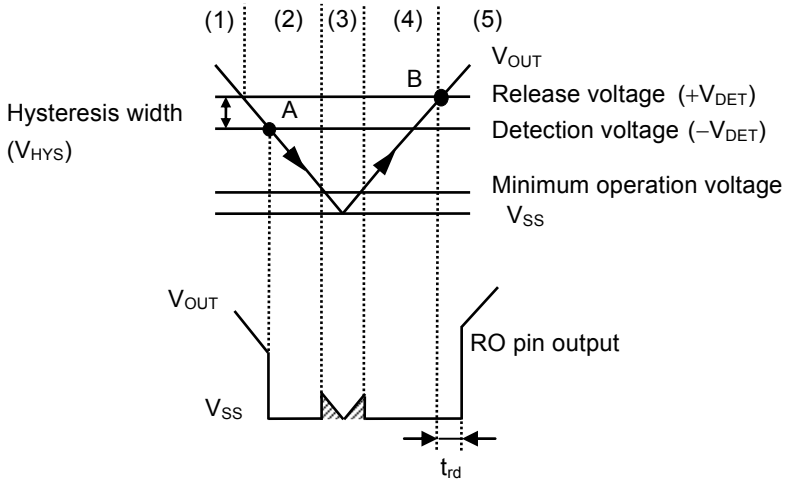


Figure 42 Timing Chart of Detector Block

2. 2 Delay circuit

When the output voltage (V_{OUT}) of the regulator rises under the status that "L" is output to the RO pin, the reset release signal is output to the RO pin later than when V_{OUT} becomes $+V_{DET}$. The release delay time (t_{rd}) changes according to C_{DLY}. Refer to "■ **Selection of Delay Time Adjustment Capacitor (C_{DLY})**" for details.
Moreover, when V_{OUT} decreases to $-V_{DET}$ or lower, the delay time of the same time length as the reset reaction time (t_{rr}) occurs in the output to the RO pin. Refer to "**2. Detector block**" in "■ **Explanation of Terms**" for details.
If the time period from when V_{OUT} decreases to $-V_{DET}$ or lower to when V_{OUT} increases to $+V_{DET}$ or higher is significantly shorter compared to the length of t_{rr}, V_{DLY} may not decrease to V_{DRL} or lower. In that case, "H" output remains in the RO pin.

Caution Since t_{rd} depends on the charge time of C_{DLY}, t_{rd} may be shorter than the set value if the charge operation is initiated under the condition that a residual electric charge is left in C_{DLY}.

2. 3 Output circuit

The output form of the RO pin is Nch open-drain. The RO pin can output a signal without an external pull-up resistor since it has a built-in resistor to pull up to the VOUT pin internally.
Do not connect to the pin other than VOUT pin when connecting an external pull-up resistor to the RO pin.
In the S-19502 Series, the reset output pin is prepared as the WO / RO pin.

Caution Define the external pull-up resistance by sufficient evaluation including the temperature characteristics under the actual usage conditions.

3. Watchdog timer block

3. 1 Basic operation

The watchdog timer operates as follows during monitoring operation.

(1) When the WO pin outputs "H", C_{DLY} is discharged by an internal constant current source, and the DLY pin voltage (V_{DLY}) decreases. The watchdog timer detects a trigger and the C_{DLY} is charged by an internal constant current source if a rising edge is input to the WI pin from a monitored object by the watchdog timer, and then V_{DLY} rises. The discharge operation is restarted if V_{DLY} reaches the upper timing threshold voltage (V_{DU}), and V_{DLY} decreases again. By inputting a rising edge to the WI pin again during the discharge operation, the similar operation is repeated. At this time, the WO pin outputs "H" continuously.
(2) The watchdog timer does not detect a trigger if the rising edge is not input to the WI pin from a monitored object by the watchdog timer when the C_{DLY} is discharged and V_{DLY} decreases. The WO pin outputs "L" if the discharge operation continues not detecting a trigger when V_{DLY} reaches the lower watchdog timing threshold voltage (V_{DWL}). This operation is called the time-out detection.
(3) After the time-out detection, C_{DLY} is charged while the WO pin outputs "L", and V_{DLY} increases. The WO pin outputs "H" and restarts the discharge operation if V_{DLY} reaches V_{DU}.
(4) By the operation of (3), a monitored object by the watchdog timer is reset. If a rising edge is input to the WI pin again, the operation similar to (1) is continued since the watchdog timer detects a trigger.
(5) After the operation of (3), if the status in which a rising edge is not input to the WI pin continues, the watchdog timer repeats the operation of (5) → (3) → (5) →...

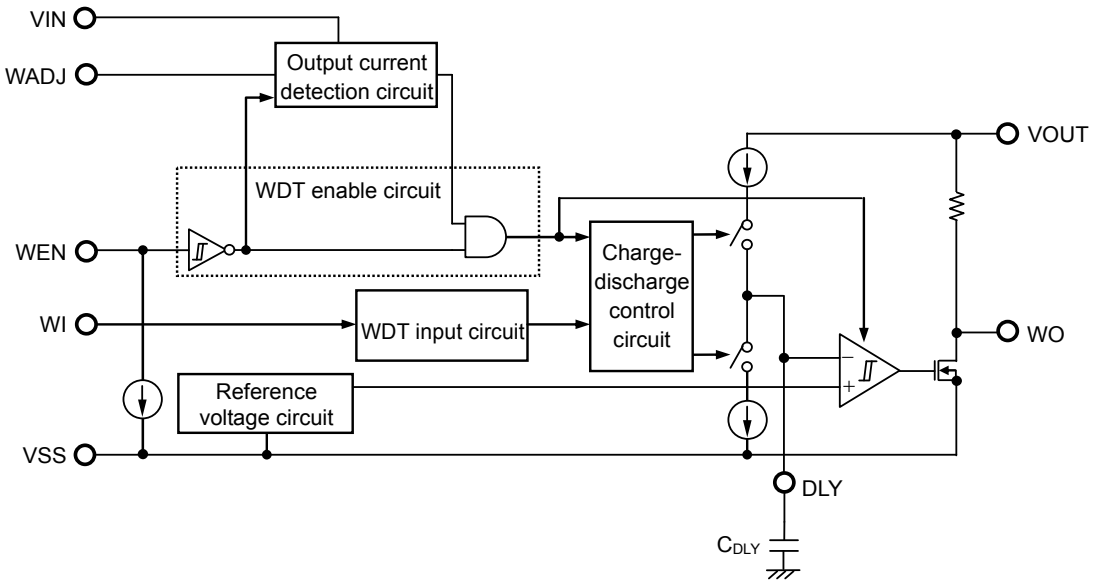


Figure 43

The time period from when the watchdog timer detects a trigger to when it detects a time-out ($t_{WD,TO}$) is indicated as the following expression. **Figure 44** shows a timing chart of the watchdog timer.

$$t_{WI,tr} \leq t_{WD,TO} \leq t_{WD,p}$$

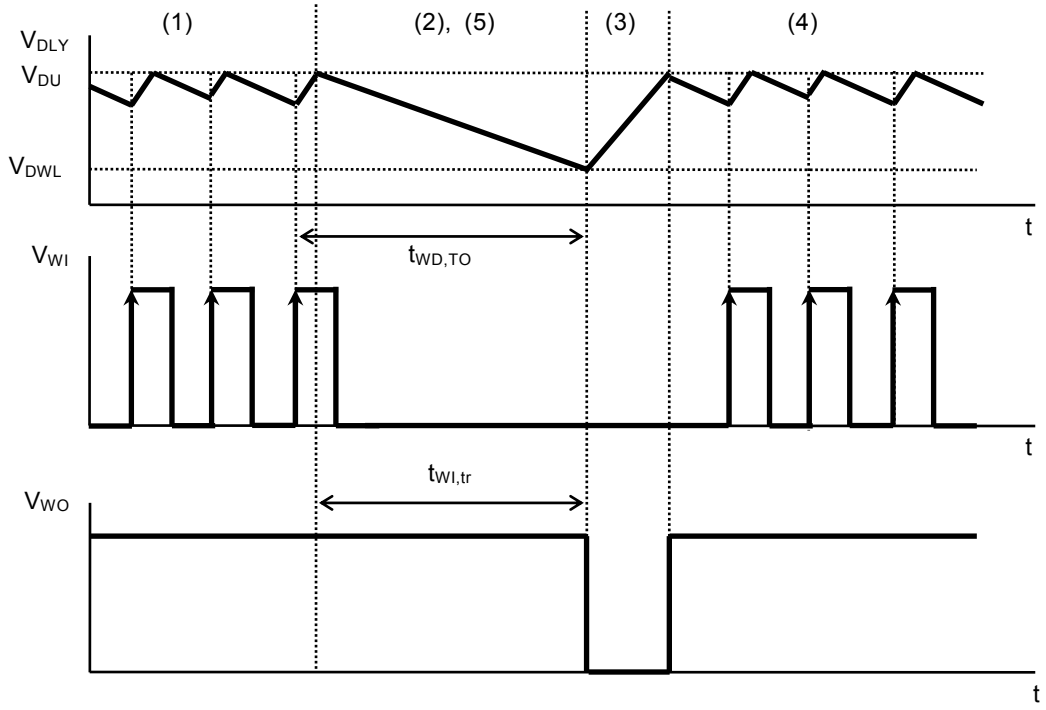


Figure 44

Regardless of the status of the watchdog timer, the capacitance of C_{DLY} could be discharged by the detector operation. Even if watchdog timer detects a trigger of signal input to the WI pin, the WO pin outputs "L" when V_{DLY} reaches V_{DWL}. After that, the watchdog timer restarts the monitoring operation if the WO pin outputs "H" when V_{DLY} reaches V_{DU}.

3. 2 Output current detection circuit

Since the S-19502/19503 Series has a built-in output current detection circuit, the watchdog timer operates autonomously. When using the autonomous watchdog operation function, the current flows in the load is detected by the output current of the regulator, the watchdog timer initiates the activation when the output current is the watchdog activation threshold current ($I_{O,WDact}$) or more, the watchdog timer is deactivated when the output current is the watchdog deactivation threshold current ($I_{O,WDdeact}$) or less
When not using the autonomous watchdog operation function, select a connection of the WADJ pin from **Table 8** in "**■ Pin Functions** ".

Depending on the output current (I_{OUT}) of the regulator, the watchdog timer monitoring activation is as follows.

(1) When I_{OUT} of the regulator is the watchdog activation threshold current ($I_{O,WDact}$) or more, the WADJ pin voltage (V_{WADJ}) is higher than the reference voltage (V_{ref}), and the output of the comparator (C1) is "H". At this time, the watchdog timer initiates the monitoring activation.
(2) When I_{OUT} decreases to the watchdog deactivation threshold current ($I_{O,WDdeact}$) (point A in **Figure 46**) or less, V_{WADJ} decreases to V_{ref} or less and the output of C1 is "L". At this time, the watchdog timer deactivates the monitoring. Even if I_{OUT} increases, the watchdog timer continues the monitoring deactivation when I_{OUT} is within less than $I_{O,WDact}$
(3) If I_{OUT} further increases to $I_{O,WDact}$ (point B in **Figure 46**) or more, V_{WADJ} increases to V_{ref} or higher and the output of C1 is "H". And then, the watchdog timer initiates the monitoring activation.

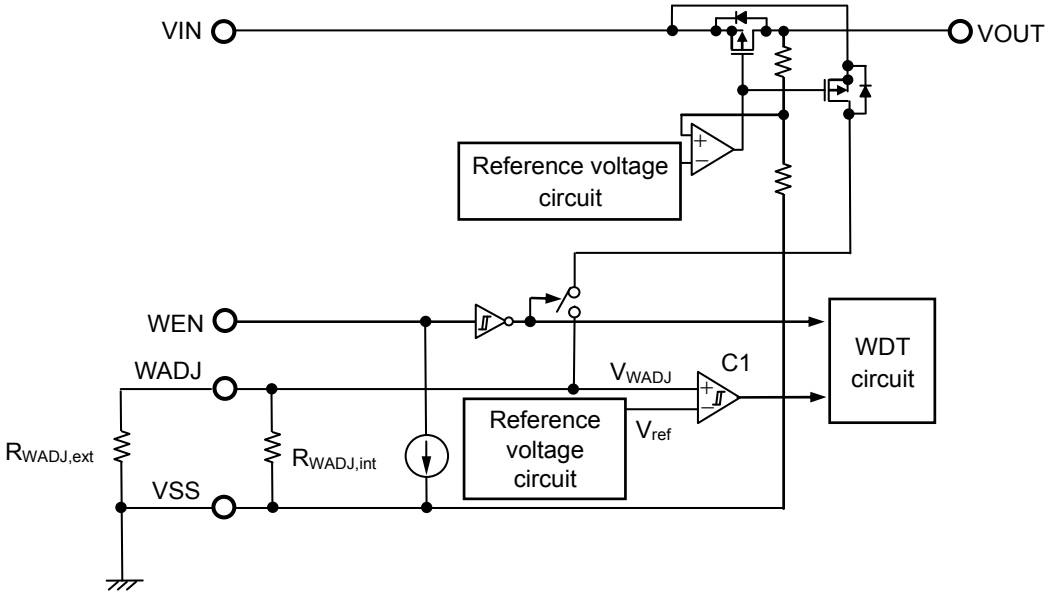


Figure 45 Operation of Output Current Detection Circuit

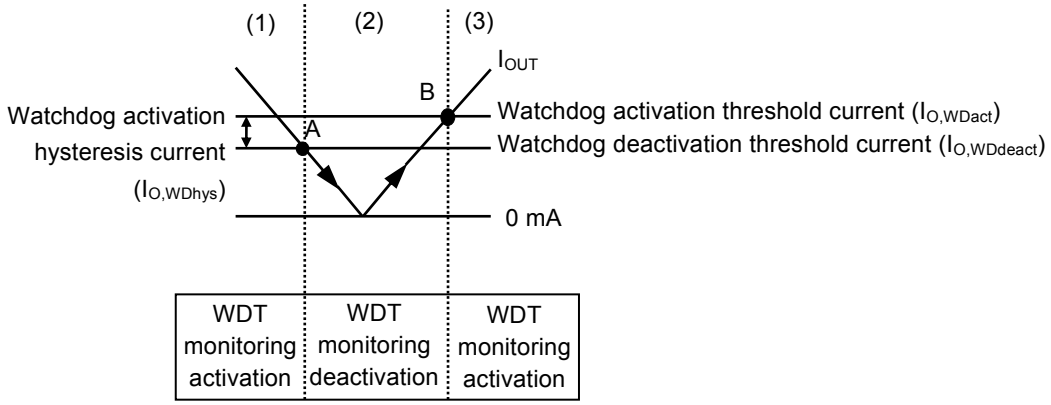


Figure 46 Autonomous Watchdog Operation Function

Caution **Due to detecting I_{OUT} of the regulator, current flows through the registors connected to the WADJ pin ($R_{WADJ,ext}$ and $R_{WADJ,int}$). Therefore, the WADJ pin voltage (V_{WADJ}) may fluctuate since the current flowing through $R_{WADJ,ext}$ and $R_{WADJ,int}$ also changes in the same way if the output current changes transiently. V_{WADJ} at that time should be evaluated with the actual device**.

Remark $I_{O,WDact}$, $I_{O,WDdeact}$ and $I_{O,WDhys}$ can be adjusted by connecting $R_{WADJ,ext}$ to the WADJ pin. Refer to "**■ Selection of Watchdog Activation Threshold Current Adjustment Resistor ($R_{WADJ,ext}$)**" for the detail.

3. 3 Watchdog enable circuit

S-19502 Series has a built-in watchdog Enable circuit that switches Enable or Disable of the watchdog timer due to input to the WEN pin. When inputting "L" to the WEN pin, the watchdog timer becomes Disable and stops the output current detection operation and monitoring activation. When inputting "H" to the WEN pin, the watchdog timer becomes Enable. The watchdog timer monitoring activation is performed depending on the connection of the WADJ pin.
The internal equivalent circuit of the WEN pin is configured as shown in **Figure 47**, and is pulled down internally by the constant current source. For this reason, the WEN pin is set to "L" when using the WEN pin in the floating status, and the watchdog timer becomes Disable. However, in order that the watchdog timer become Disable certainly, connect the WEN pin to GND so that "L" is input to the WEN pin certainly, since the impedance of the WEN pin is high when using the WEN pin in the floating status.
In order to fix the watchdog timer to Enable, connect the WEN pin to the VOUT pin so that "H" is input to the WEN pin.

Table 18 shows the relation between status of each pins and the watchdog timer.

Table 18

WEN Pin Input Logic	WADJ Pin Connection*1	Output Current*2	Output Current Detection Circuit	Watchdog Timer Monitoring Activation	WO Pin Input Logic
"H"	Open, or connect to VSS pin via external resistor*3	"H"	Operate	Activate	"H" or "L"
"H"	Open, or connect to VSS pin via external resistor*3	"L"	Operate	Deactivate	"H"
"H"	Connect to VOUT pin via resistor of 270 kΩ	Don't care	Stop	Activate	"H" or "L"
"H"	Connect to VSS pin	Don't care	Stop	Deactivate	"H"
"L"	Don't care	Don't care	Stop	Deactivate	"H"

***1.** Refer to "**1. WADJ pin**" in "**■ Pin Functions**".

***2.** Output current "H": $I_{OUT} > I_{O,WDact}$
Output current "L": $I_{OUT} < I_{O,WDdeact}$

***3.** Refer to "**■ Selection of Watchdog Activation Threshold Current Adjustment Resistor ($R_{WADJ,ext}$)**".

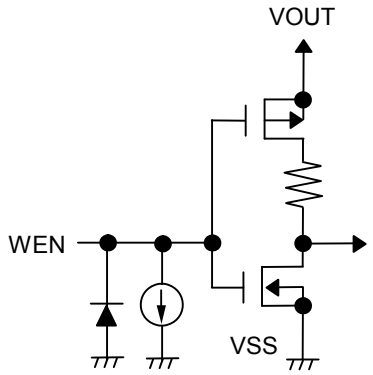


Figure 47

3. 4 Watchdog input circuit

By inputting a rising edge to the WI pin, the watchdog timer detects a trigger. The S-19502/19503 Series has a built-in watchdog input circuit which contains a band pass filter in the WI pin, and detects a rising edge which satisfies an input condition as a trigger signal. Refer to ***2** and **Figure 5** in "**■ Recommended Operation Conditions**".

During the operation of the watchdog timer, a trigger is detected only when the DLY pin voltage is in V_{DU} to V_{DWL} and while the discharge operation of C_{DLY} is being performed. Refer to "**3. Watchdog timer block**" in "**■ Operation**" for details. The signal input from a monitored object by the watchdog timer to the watchdog timer should be input with a time interval which is sufficiently shorter than the watchdog trigger time ($t_{WI,tr}$).

Caution Under a noisy environment, the watchdog input circuit may detect the noise as a trigger signal. Sufficiently evaluate with the actual application to confirm that a trigger is detected only in the intended signal.

3. 5 Watchdog output circuit

The output form of the WO pin is Nch open-drain. The WO pin can output a signal without an external pull-up resistor since it has a built-in resistor to pull up to the VOUT pin internally.

Do not connect to the pin other than VOUT pin when connecting an external pull-up resistor to the WO pin.

In the S-19502 Series, the watchdog output pin is prepared as the WO / RO pin.

Caution Define the external pull-up resistance by sufficient evaluation including the temperature characteristics under the actual usage conditions.

■ Timing Charts

1. S-19502 Series (Product with watchdog enable function)

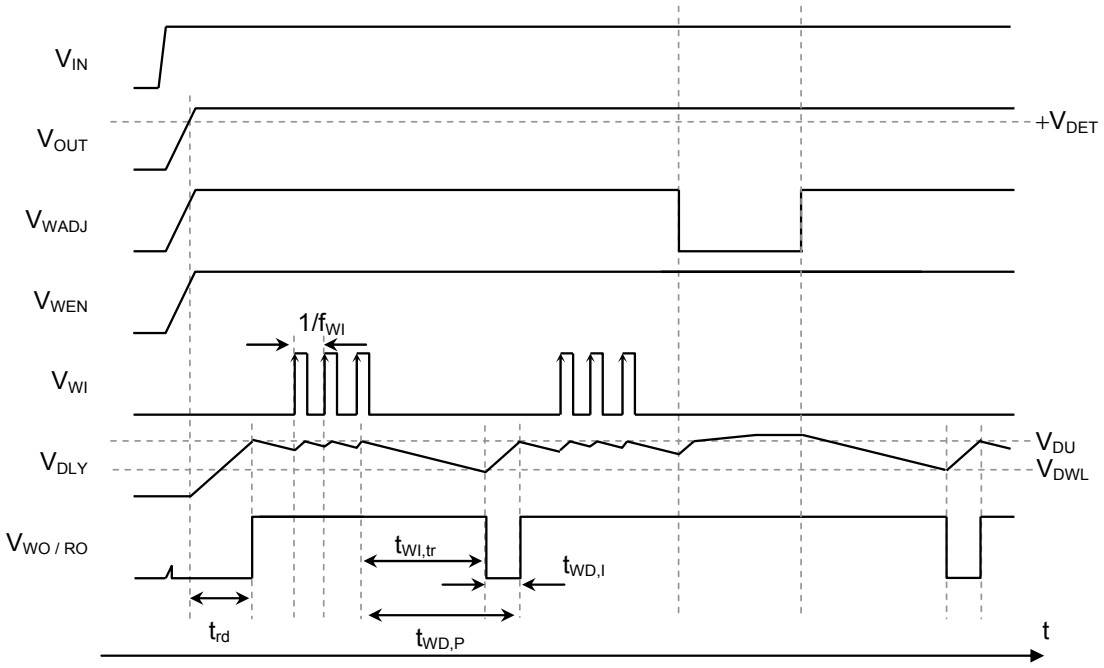


Figure 48 Example of Watchdog Timer Monitoring Operation

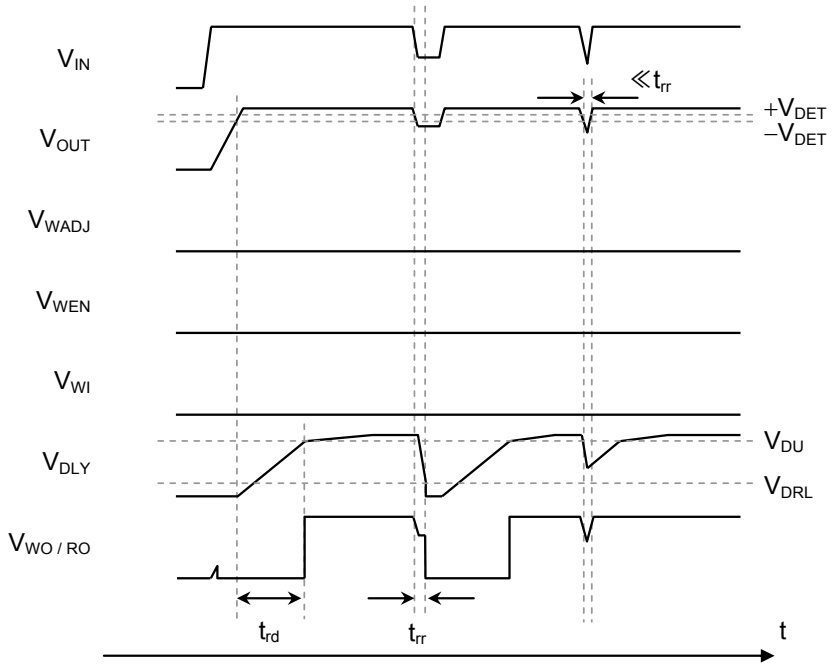


Figure 49 Example of Detector Operation

2. S-19503 Series (Product without watchdog enable function)

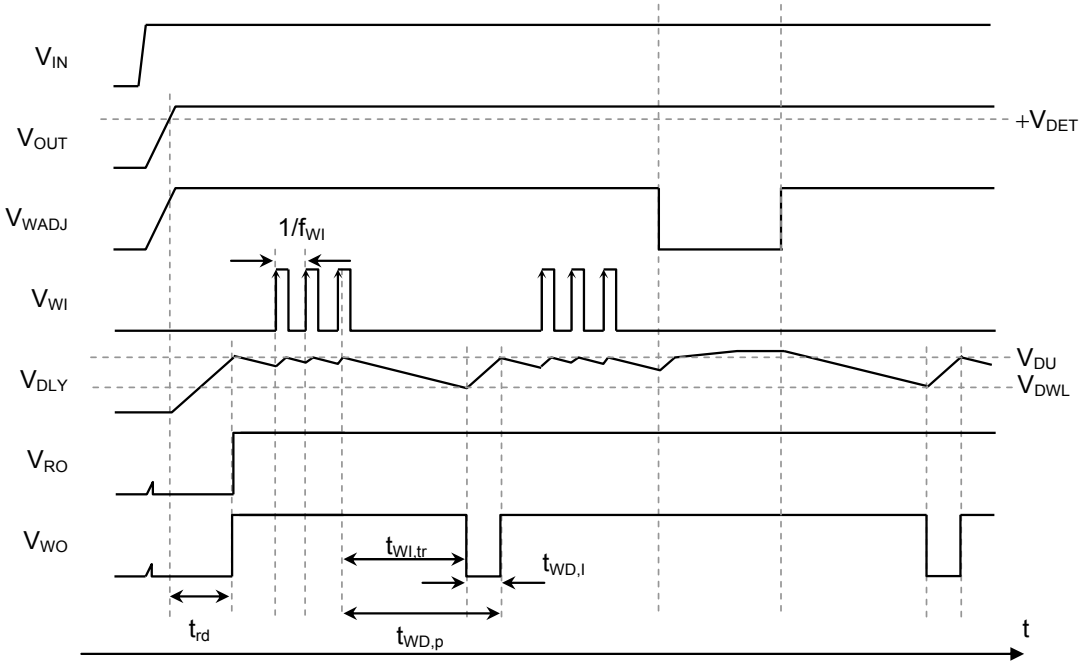


Figure 50 Example of Watchdog Timer Monitoring Operation

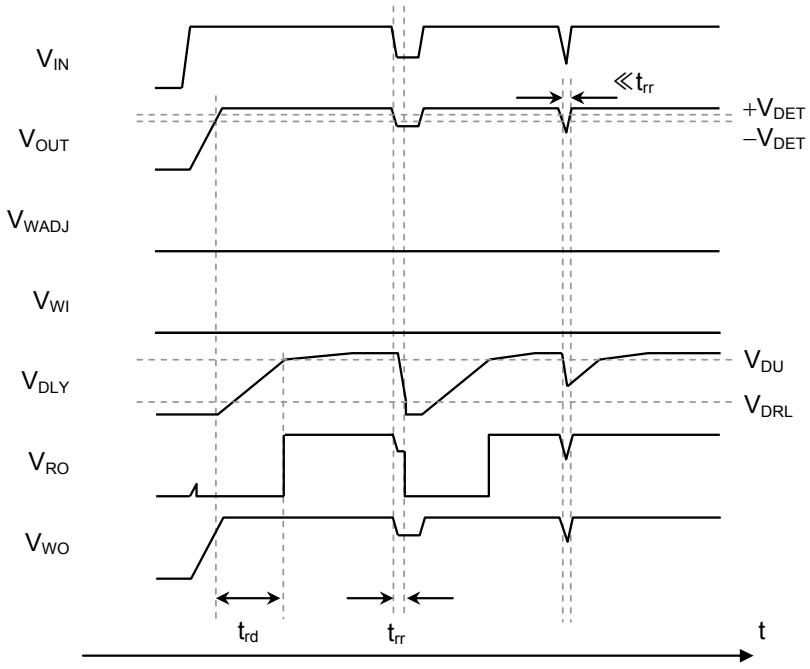


Figure 51 Example of Detector Operation

■ Precautions

- Wiring patterns for the VIN pin, the VOUT pin and GND should be designed so that the impedance is low. When mounting an output capacitor between the VOUT pin and the VSS pin (C_L) and an input capacitor between the VIN pin and the VSS pin (C_{IN}), the distance from the capacitors to these pins should be as short as possible.
- Note that generally the output voltage may increase when a series regulator is used at low load current (0.1 mA or less).
- Note that generally the output voltage may increase due to the leakage current from an output transistor when a series regulator is used at high temperature.
- Generally a series regulator may cause oscillation, depending on the selection of external parts. The following conditions are recommended for the S-19502/19503 Series. However, be sure to perform sufficient evaluation under the actual usage conditions for selection, including evaluation of temperature characteristics. Refer to "**4. Equivalent series resistance vs. Output current characteristics (Ta = +25°C)**" in "**■ Reference Data**" for the equivalent series resistance (R_{ESR}) of the output capacitor.

  Input capacitor (C_{IN}): 2.2 μF or more
  Output capacitor (C_L): 2.2 μF or more

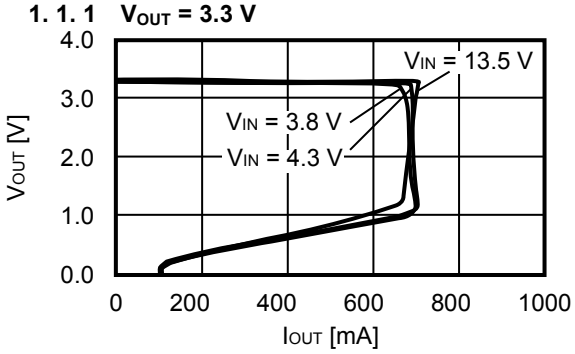
- In a series regulator, generally the values of overshoot and undershoot in the output voltage vary depending on the variation factors of power-on, power supply fluctuation and load fluctuation, or output capacitance.
  Determine the conditions of the output capacitor after sufficiently evaluating the temperature characteristics of overshoot or undershoot in the output voltage with the actual device.
- The voltage regulator may oscillate when the impedance of the power supply is high and the input capacitance is small or an input capacitor is not connected.
- Overshoot may occur in the output voltage momentarily if the voltage is rapidly raised at power-on or when the power supply fluctuates. Sufficiently evaluate the output voltage at that time with the actual device.
- If the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur to the VOUT pin due to resonance of the wiring inductance and the output capacitance in the application. The negative voltage can be limited by inserting a protection diode between the VOUT pin and the VSS pin or inserting a series resistor to the output capacitor.
- The application conditions for the input voltage, the output voltage, and the load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In determining the output current, attention should be paid to the output current value specified in **Table 12** in "**■ Electrical Characteristics**" and footnote ***4** of the table.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

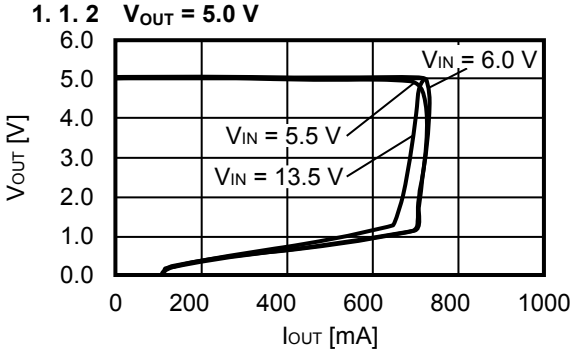
1. Regulator block

1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)

1. 1. 1 V_{OUT} = 3.3 V

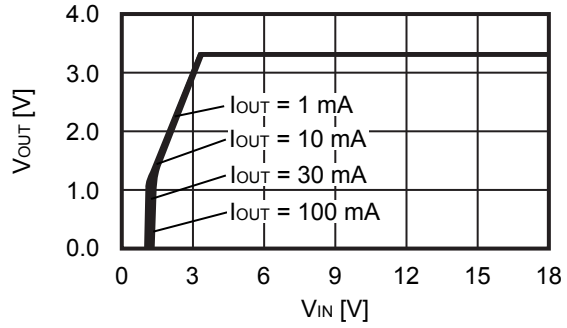


1. 1. 2 V_{OUT} = 5.0 V

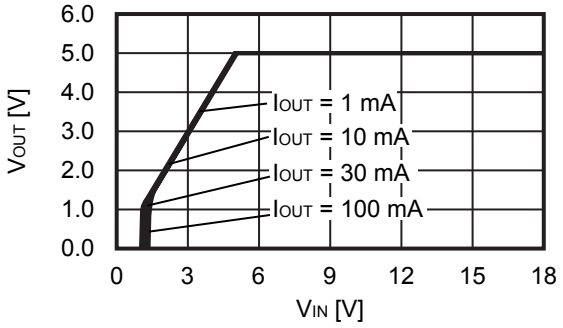


1. 2 Output voltage vs. Input voltage (Ta = +25°C)

1. 2. 1 V_{OUT} = 3.3 V

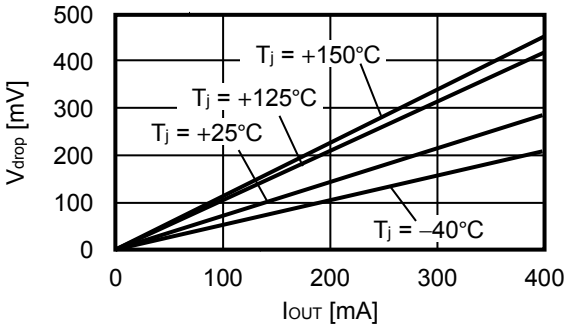


1. 2. 2 V_{OUT} = 5.0 V

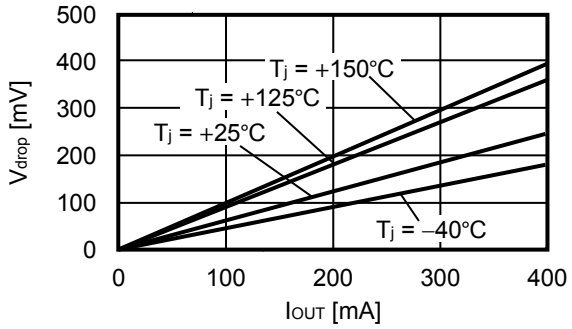


1. 3 Dropout voltage vs. Output current

1. 3. 1 V_{OUT} = 3.3 V

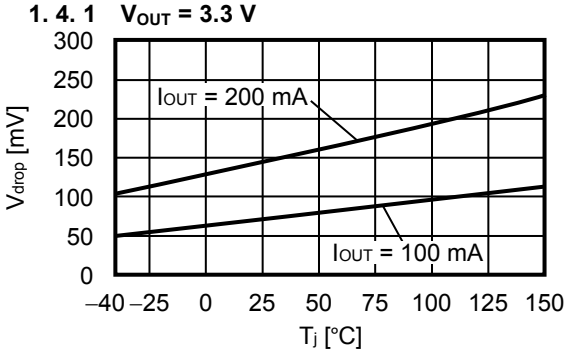


1. 3. 2 V_{OUT} = 5.0 V

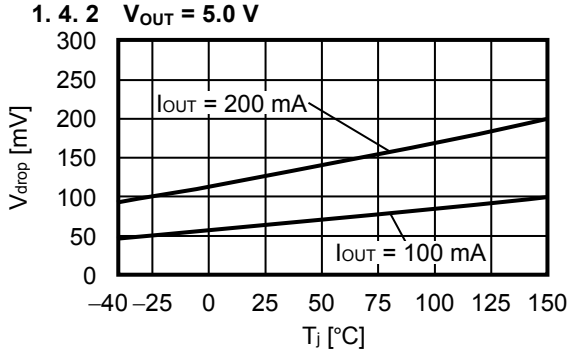


1. 4 Dropout voltage vs. Junction temperature

1. 4. 1 V_{OUT} = 3.3 V

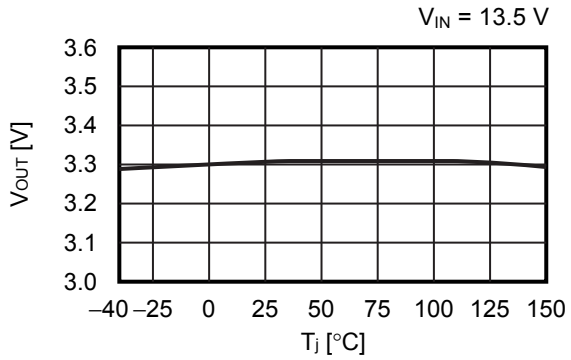


1. 4. 2 V_{OUT} = 5.0 V

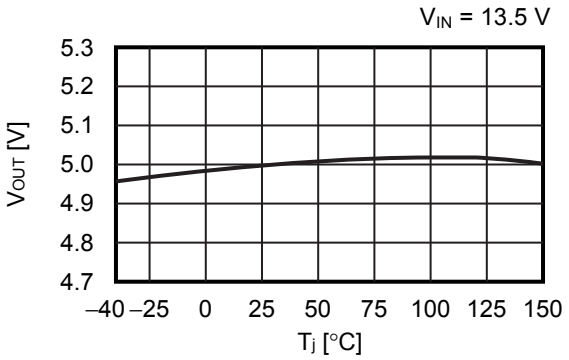


1. 5 Output voltage vs. Junction temperature

1. 5. 1 V_{OUT} = 3.3 V

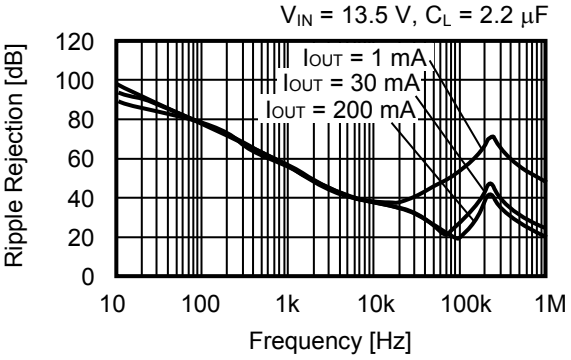


1. 5. 2 V_{OUT} = 5.0 V

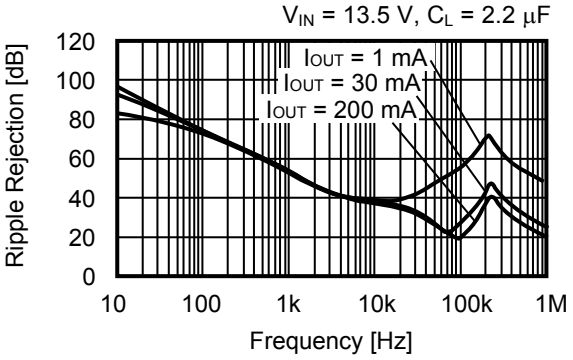


1. 6 Ripple rejection (Ta = +25°C)

1. 6. 1 V_{OUT} = 3.3 V



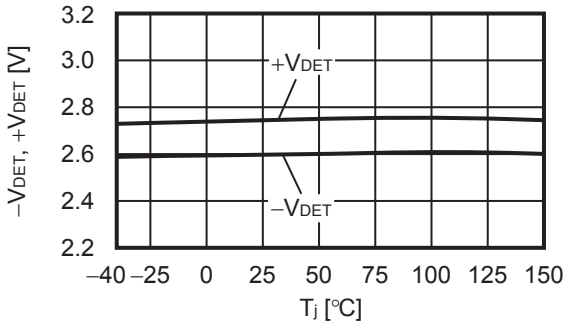
1. 6. 2 V_{OUT} = 5.0 V



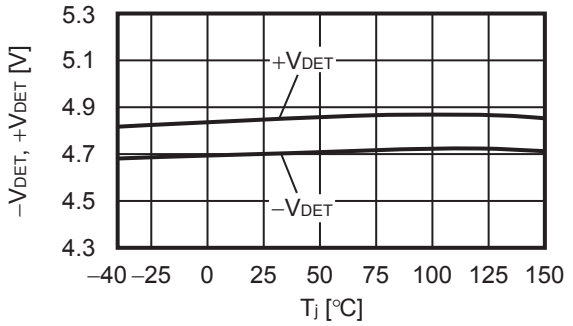
2. Detector block

2. 1 Detection voltage, Release voltage vs. Junction temperature

2. 1. 1 $-V_{DET}$ = 2.6 V

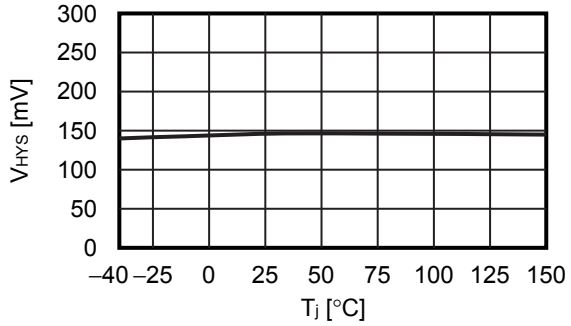


2. 1. 2 $-V_{DET}$ = 4.7 V

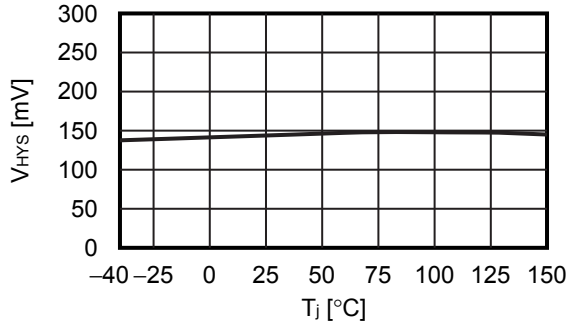


2. 2 Hysteresis width vs. Junction temperature

2. 2. 1 $-V_{DET}$ = 2.6 V

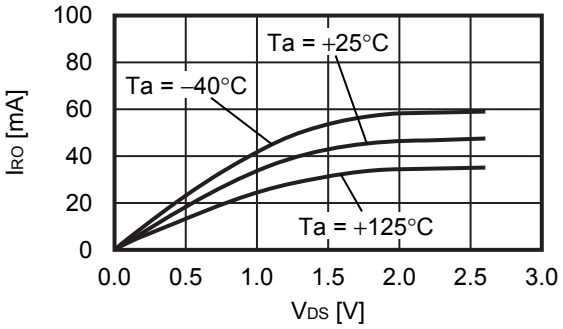


2. 2. 2 $-V_{DET}$ = 4.7 V

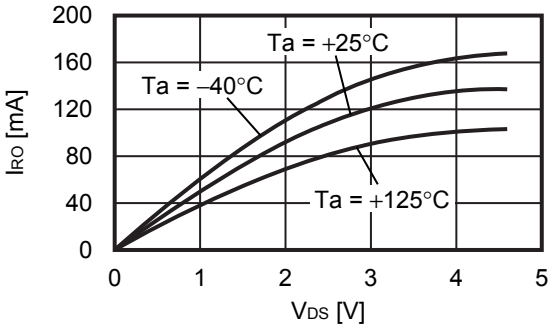


2. 3 Nch transistor output current vs. V_{DS}

2. 3. 1 $-V_{DET}$ = 2.6 V

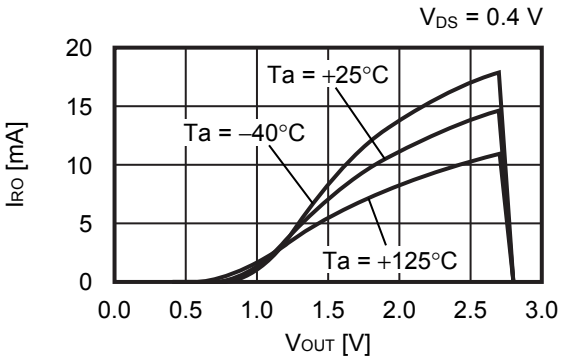


2. 3. 2 $-V_{DET}$ = 4.7 V

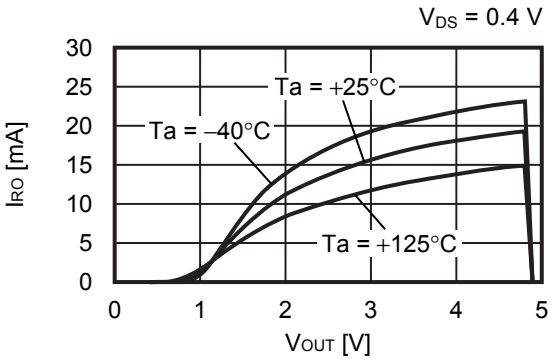


2. 4 Nch transistor output current vs. Output voltage

2. 4. 1 $-V_{DET}$ = 2.6 V

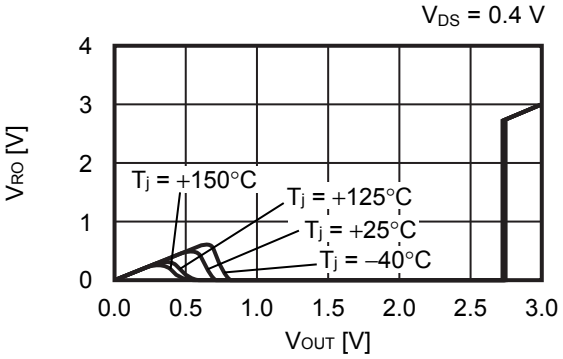


2. 4. 2 $-V_{DET}$ = 4.7 V

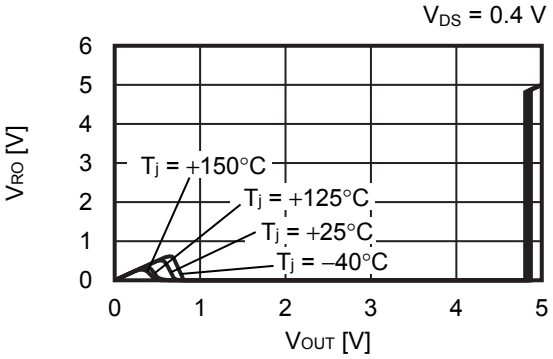


2. 5 Nch transistor output voltage vs. Output voltage

2. 5. 1 $-V_{DET}$ = 2.6 V



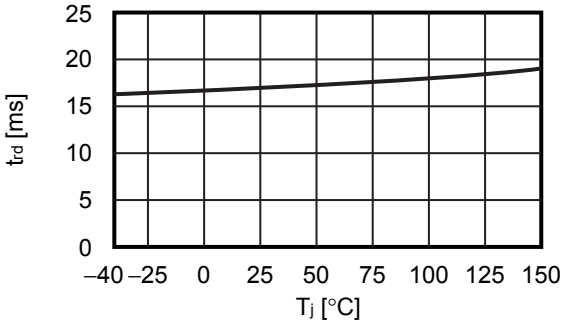
2. 5. 2 $-V_{DET}$ = 4.7 V



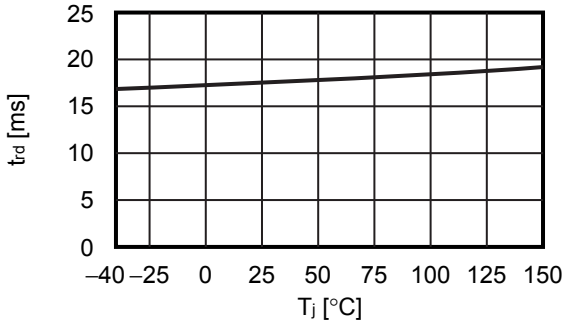
Remark V_{DS}: Drain-to-source voltage of the output transistor

2. 6 Release delay time vs. Junction temperature

2. 6. 1 $-V_{DET}$ = 2.6 V

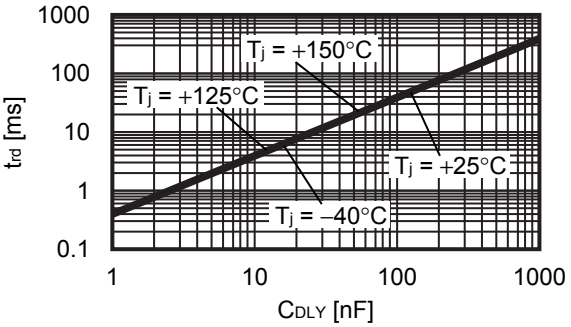


2. 6. 2 $-V_{DET}$ = 4.7 V

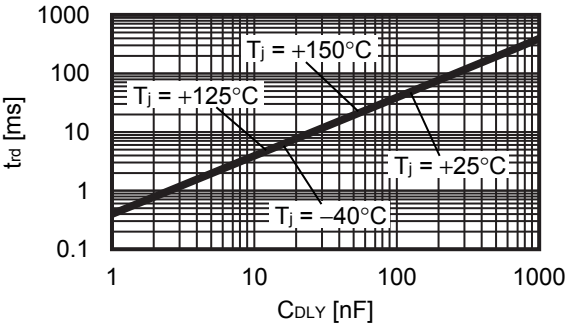


2. 7 Release delay time vs. Capacitance for delay time adjustment capacitor

2. 7. 1 $-V_{DET}$ = 2.6 V

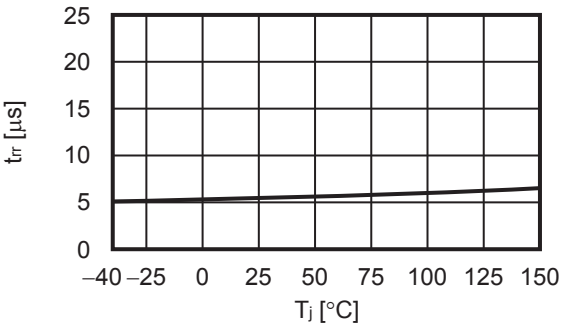


2. 7. 2 $-V_{DET}$ = 4.7 V

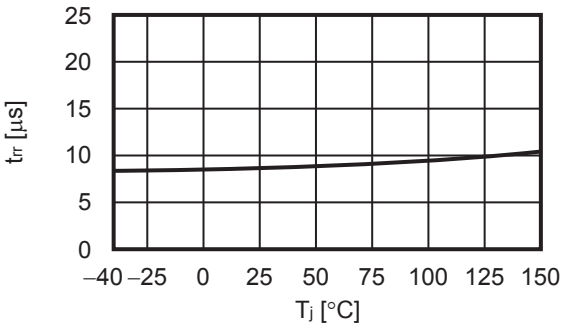


2. 8 Reset reaction time vs. Junction temperature

2. 8. 1 $-V_{DET}$ = 2.6 V

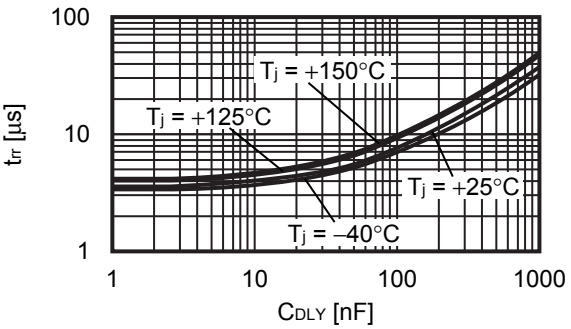


2. 8. 2 $-V_{DET}$ = 4.7 V

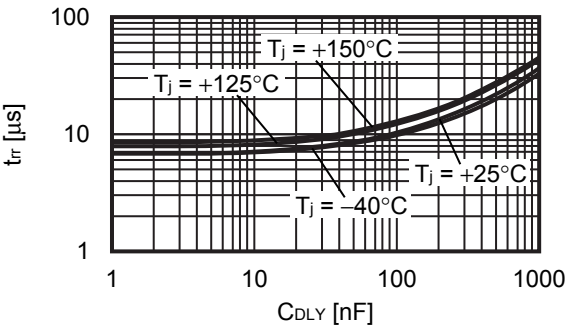


2. 9 Reset reaction time vs. Capacitance for delay time adjustment capacitor

2. 9. 1 $-V_{DET}$ = 2.6 V



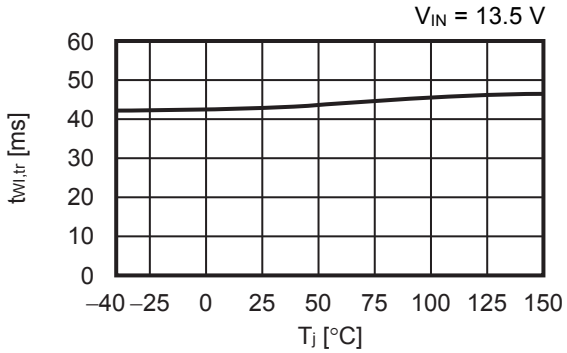
2. 9. 2 $-V_{DET}$ = 4.7 V



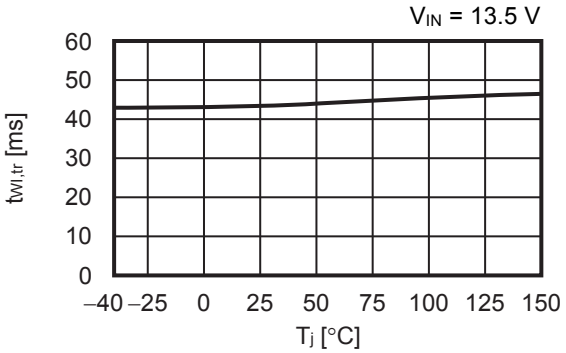
3. Watchdog timer block

3. 1 Watchdog trigger time vs. Junction temperature

3. 1. 1 V_{OUT} = 3.3 V

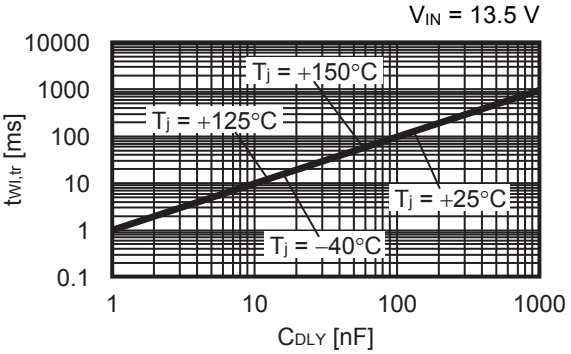


3. 1. 2 V_{OUT} = 5.0 V

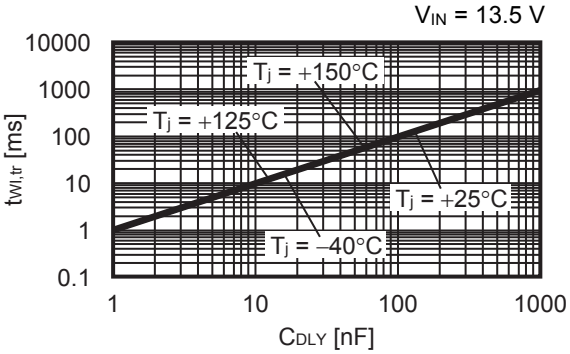


3. 2 Watchdog trigger time vs. Capacitance for delay time adjustment capacitor

3. 2. 1 V_{OUT} = 3.3 V

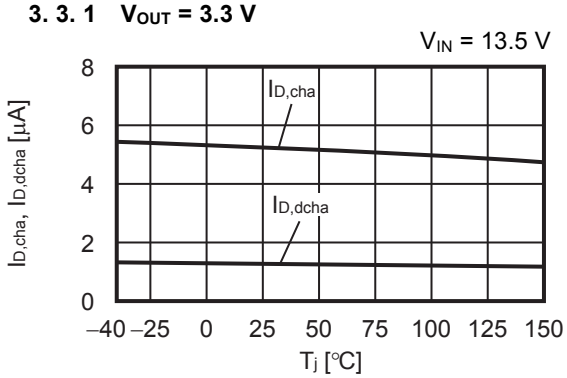


3. 2. 2 V_{OUT} = 5.0 V

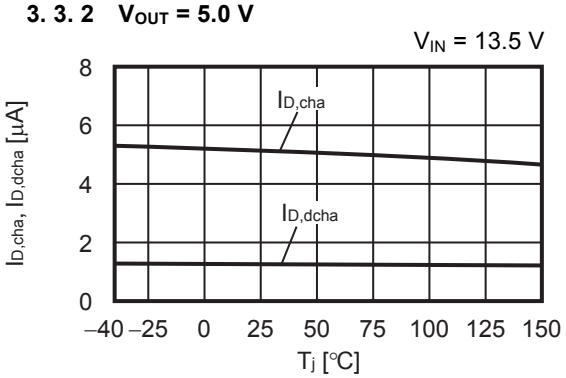


3. 3 Charge current, discharge current vs. Junction temperature

3. 3. 1 V_{OUT} = 3.3 V

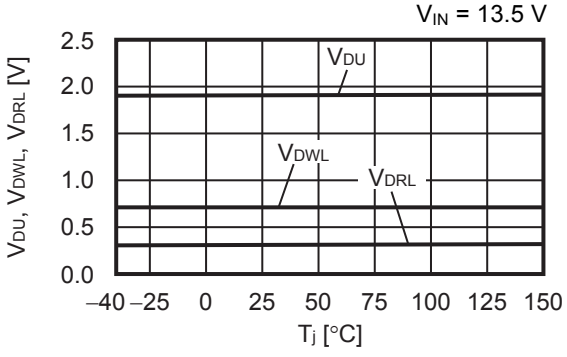


3. 3. 2 V_{OUT} = 5.0 V

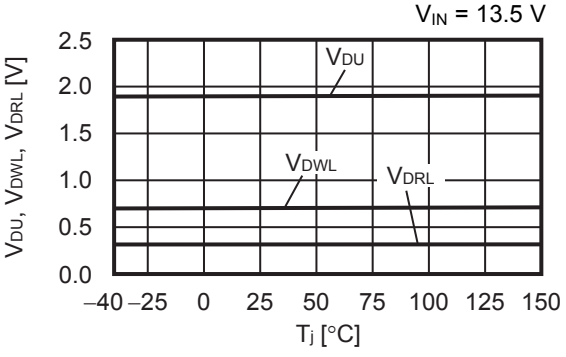


3. 4 Upper timing threshold voltage, lower watchdog timing threshold voltage, lower reset timing threshold voltage vs. Junction temperature

3. 4. 1 V_{OUT} = 3.3 V

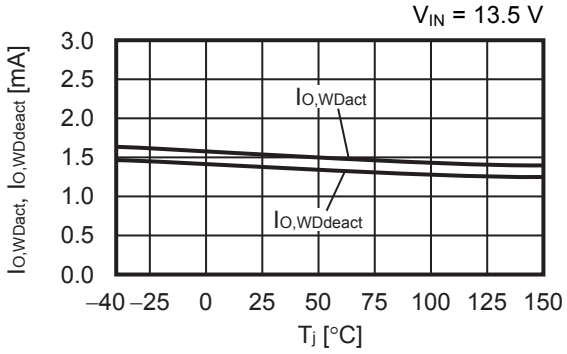


3. 4. 2 V_{OUT} = 5.0 V

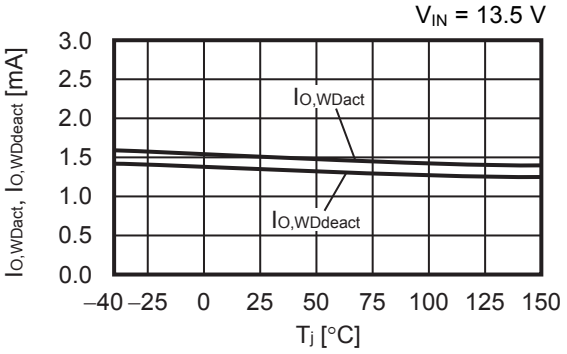


3. 5 Watchdog activation current, watchdog deactivation current vs. Junction temperature

3. 5. 1 V_{OUT} = 3.3 V

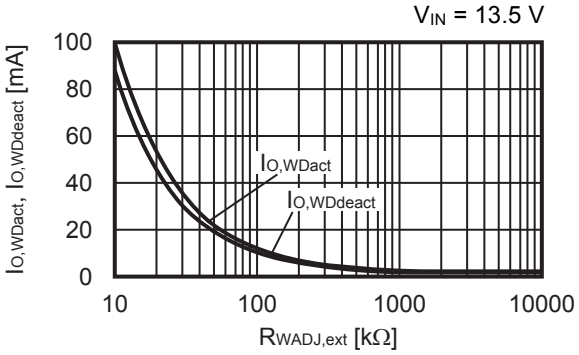


3. 5. 2 V_{OUT} = 5.0 V

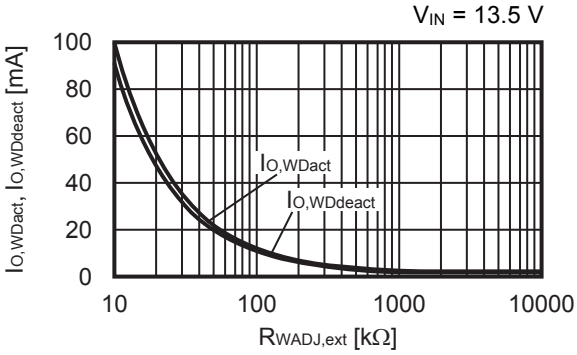


3. 6 Watchdog activation current, Watchdog deactivation current vs. Watchdog activation threshold current adjustment resistor (Ta = +25°C)

3. 6. 1 V_{OUT} = 3.3 V



3. 6. 2 V_{OUT} = 5.0 V

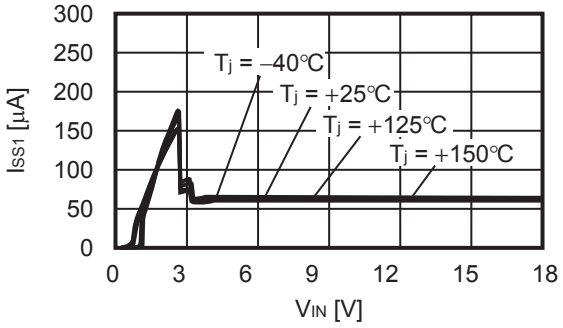


4. Overall

4. 1 Current consumption during operation vs. input voltage

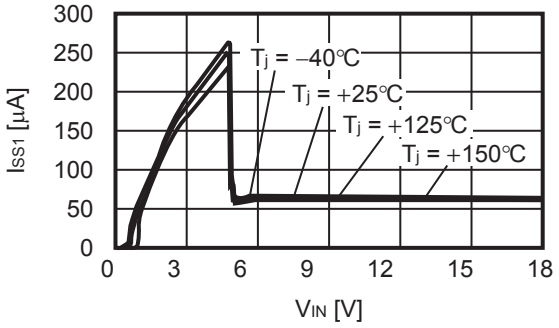
4. 1. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

When watchdog timer is deactivated



4. 1. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

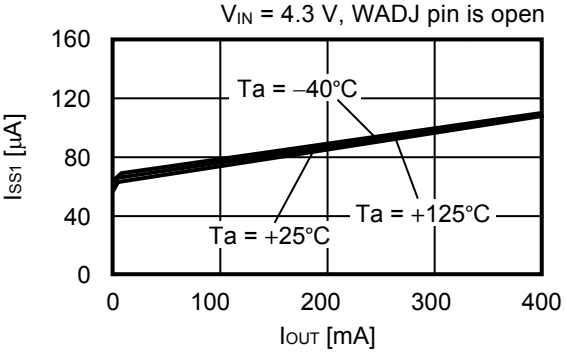
When watchdog timer is deactivated



4. 2 Current consumption during operation vs. Output current

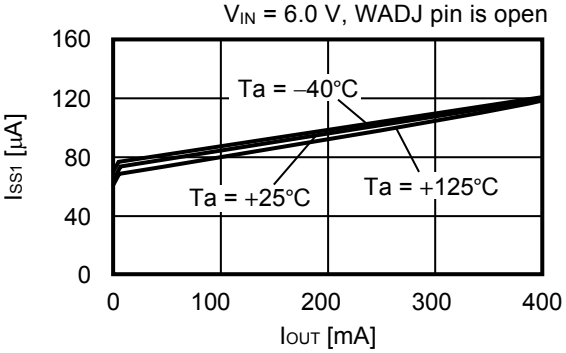
4. 2. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

V_{IN} = 4.3 V, WADJ pin is open



4. 2. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

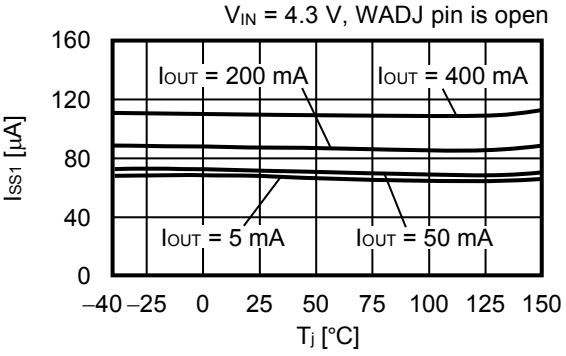
V_{IN} = 6.0 V, WADJ pin is open



4. 3 Current consumption during operation vs. Junction temperature

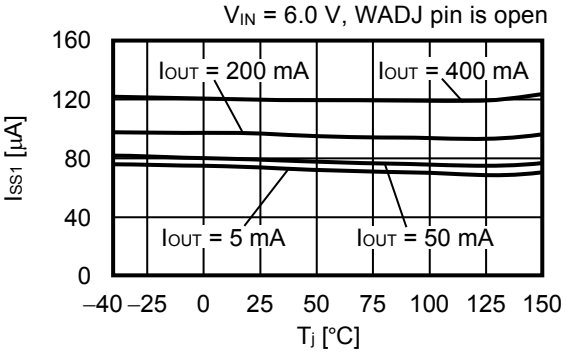
4. 3. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

V_{IN} = 4.3 V, WADJ pin is open



4. 3. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

V_{IN} = 6.0 V, WADJ pin is open

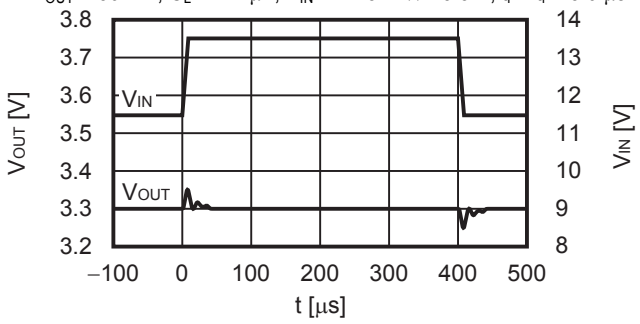


■ Reference Data

1. Transient response characteristics when input (Ta = +25°C)

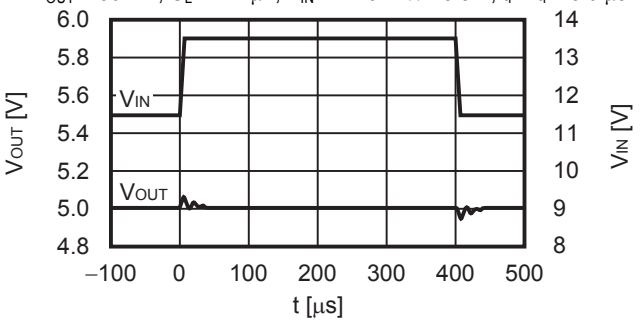
1. 1 V_{OUT} = 3.3 V

I_{OUT} = 30 mA, C_L = 2.2 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



1. 2 V_{OUT} = 5.0 V

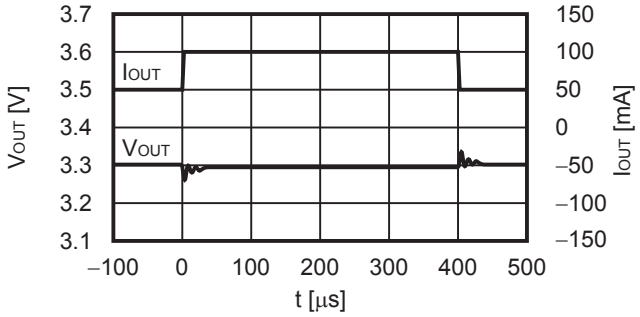
I_{OUT} = 30 mA, C_L = 2.2 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



2. Transient response characteristics of load (Ta = +25°C)

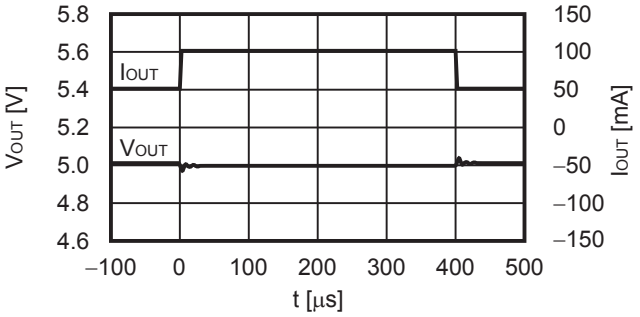
2. 1 V_{OUT} = 3.3 V

V_{IN} = 13.5 V, C_L = 2.2 µF, I_{OUT} = 50 mA ↔ 100 mA



2. 2 V_{OUT} = 5.0 V

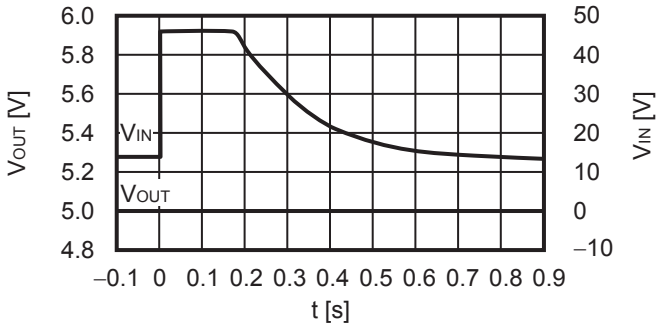
V_{IN} = 13.5 V, C_L = 2.2 µF, I_{OUT} = 50 mA ↔ 100 mA



3. Load dump characteristics (Ta = +25°C)

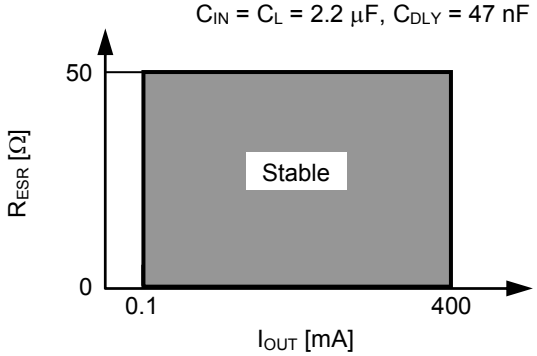
3. 1 V_{OUT} = 5.0 V

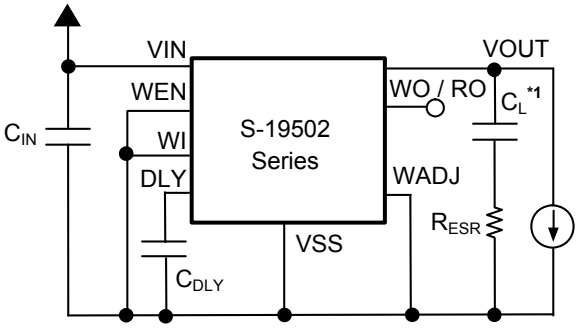
I_{OUT} = 0.1 mA, V_{IN} = 13.5 V ↔ 45.0 V, C_{IN} = C_L = 2.2 µF



4. Example of equivalent series resistance vs. Output current characteristics (Ta = +25°C)

C_{IN} = C_L = 2.2 µF, C_{DLY} = 47 nF

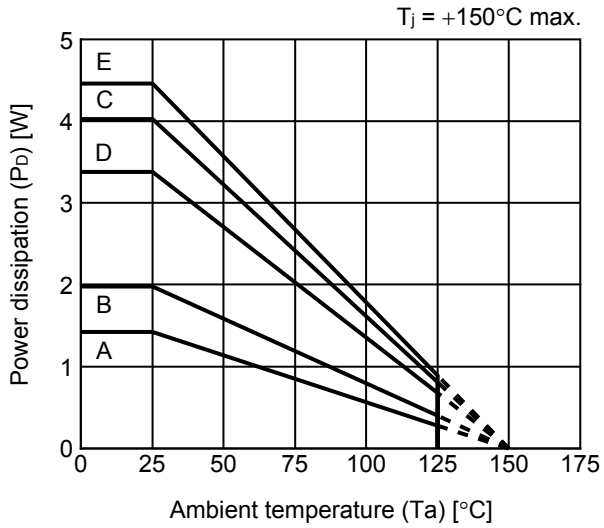




***1.** C_L: Murata Manufacturing Co., Ltd.
GCM31CR71H225K (2.2 µF)

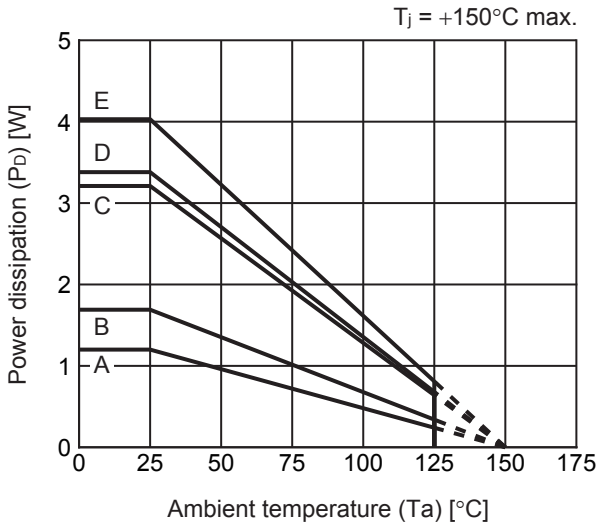
■ Power Dissipation

TO-252-9S



Board	Power Dissipation (P_D)
A	1.42 W
B	1.98 W
C	3.38 W
D	4.03 W
E	4.46 W

HSOP-8A

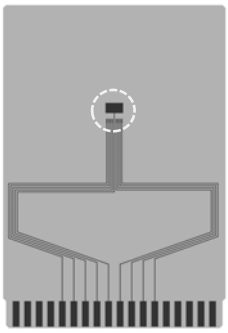


Board	Power Dissipation (P_D)
A	1.20 W
B	1.69 W
C	3.21 W
D	3.38 W
E	4.03 W

TO-252-9S Test Board

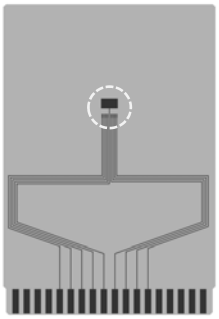
(1) Board A

IC Mount Area



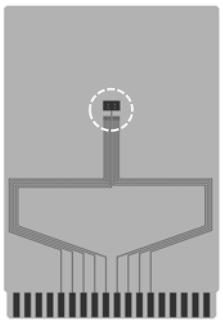
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

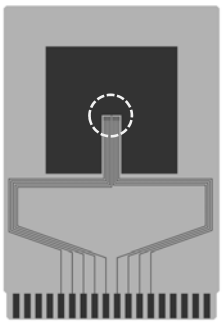
enlarged view

No. TO252-9S-A-Board-SD-1.0

TO-252-9S Test Board

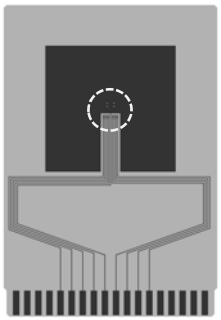
(4) Board D

IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

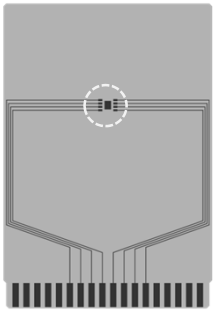
enlarged view

No. TO252-9S-A-Board-SD-1.0

HSOP-8A Test Board

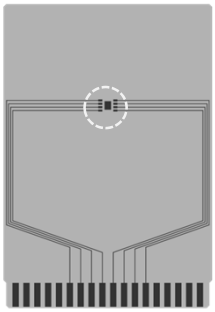
(1) Board A

IC Mount Area



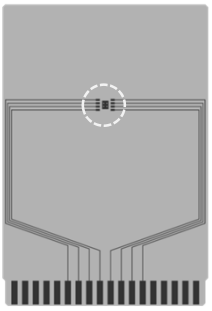
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B

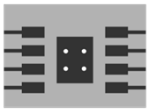


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



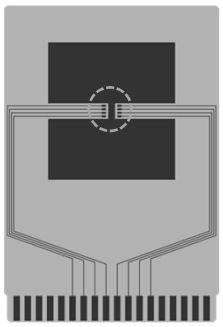
enlarged view

No. HSOP8A-A-Board-SD-1.0

HSOP-8A Test Board

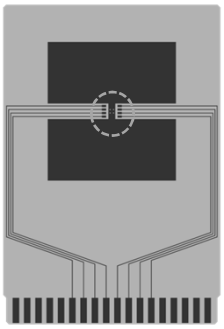
(4) Board D

IC Mount Area

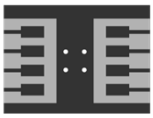


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E

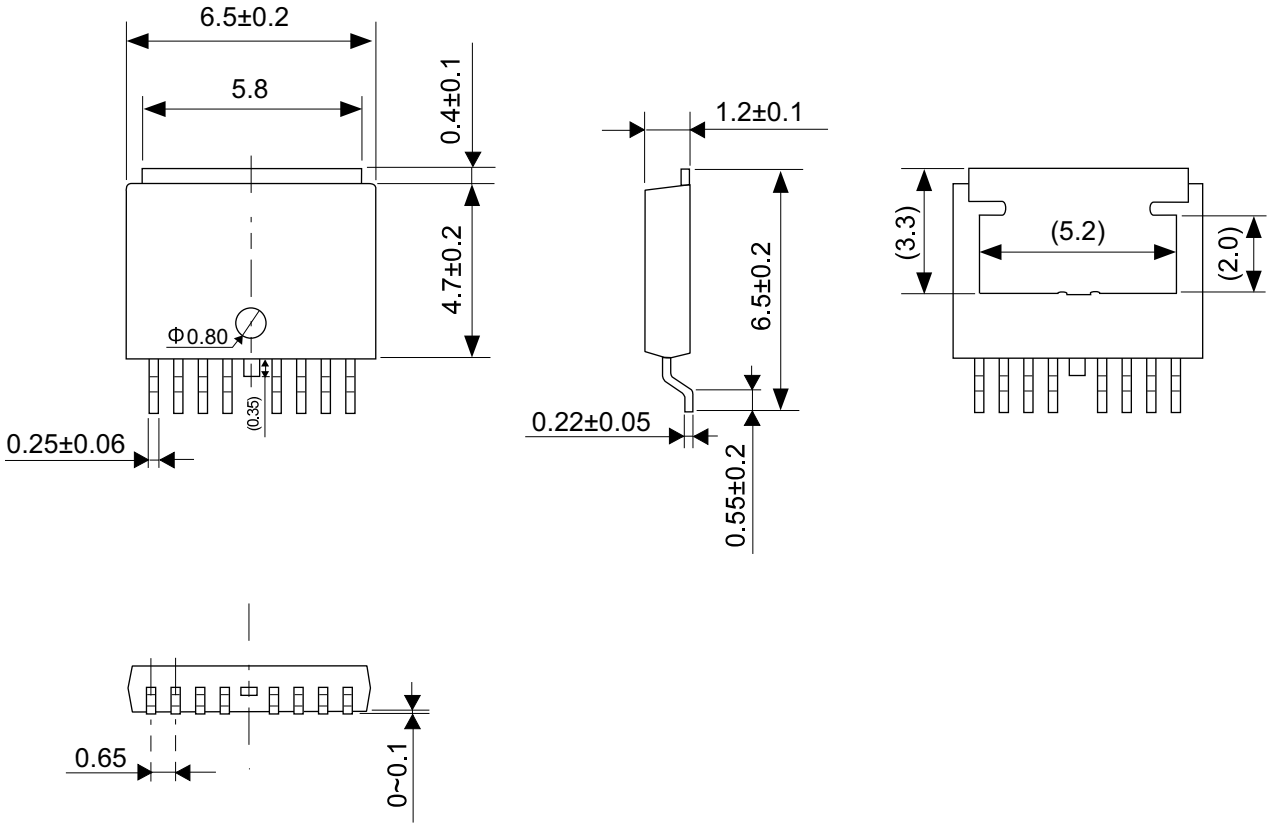


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



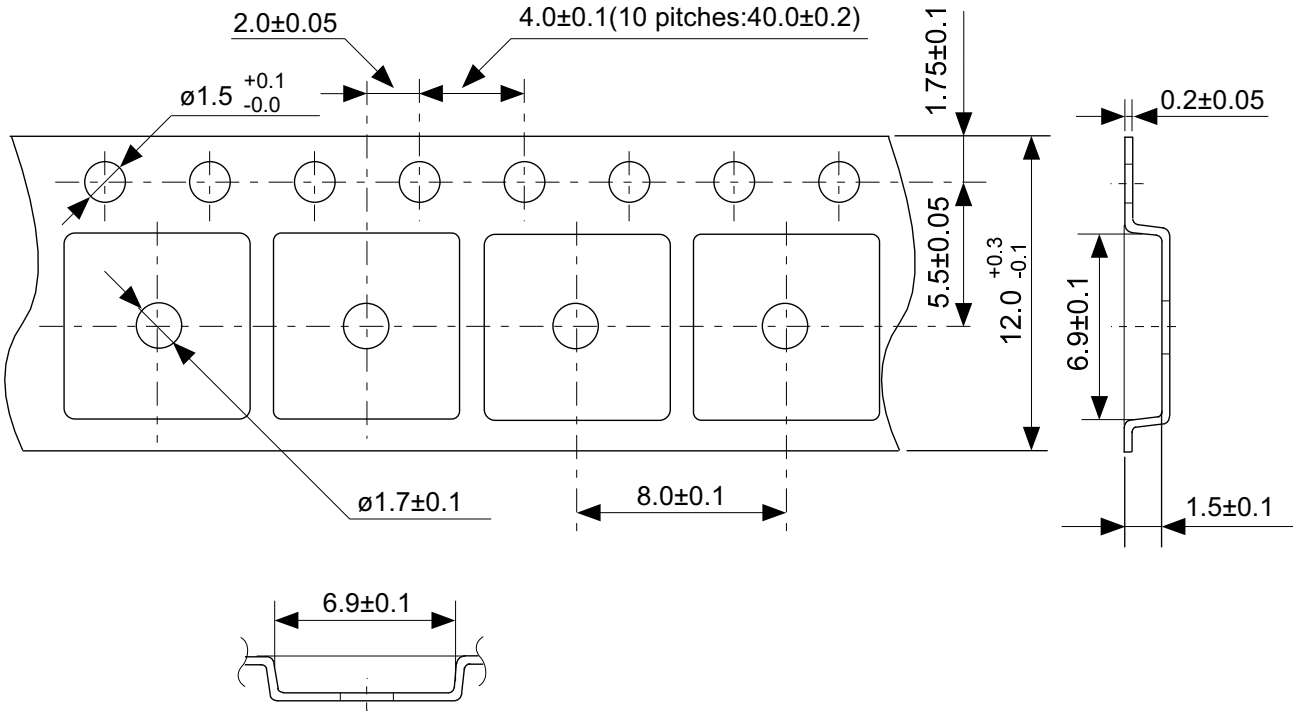
enlarged view

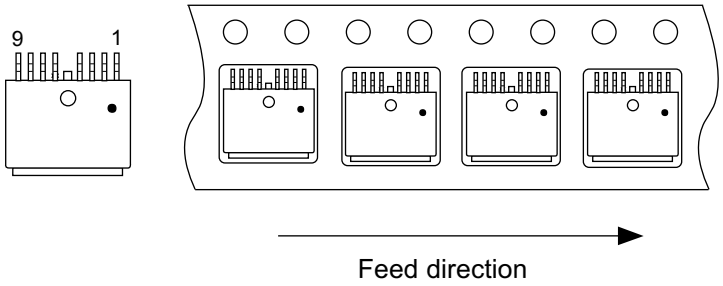
No. HSOP8A-A-Board-SD-1.0



No. VA009-A-P-SD-2.0

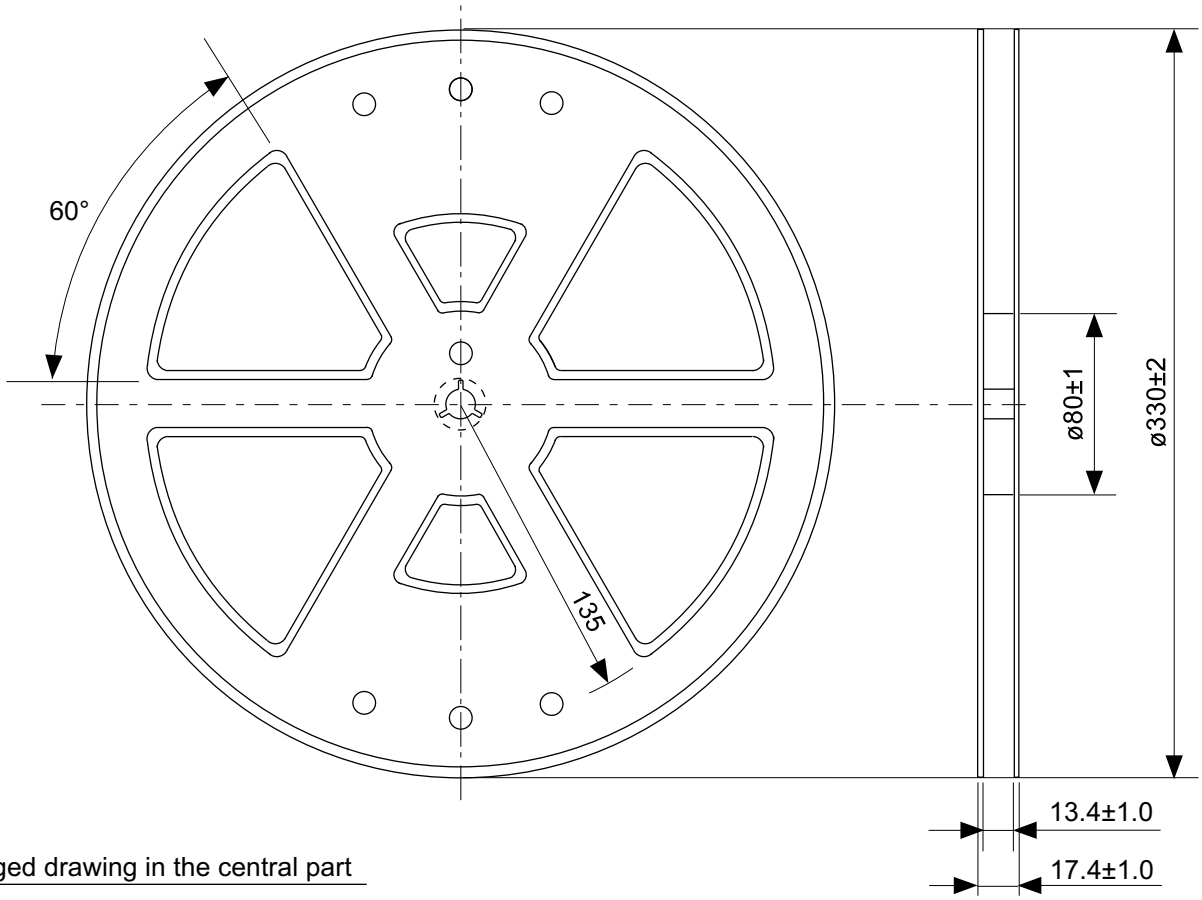
TITLE	TO252-9S-A-PKG Dimensions
No.	VA009-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



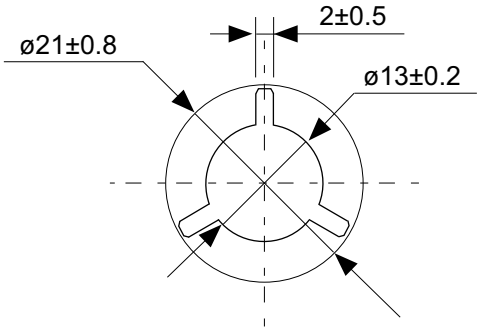


No. VA009-A-C-SD-1.0

TITLE	TO252-9S-A-Carrier Tape
No.	VA009-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

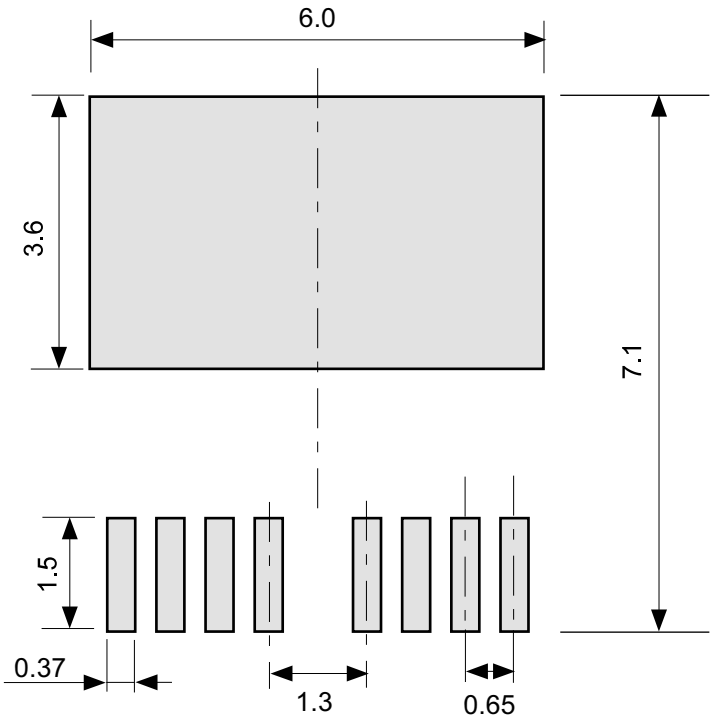


Enlarged drawing in the central part



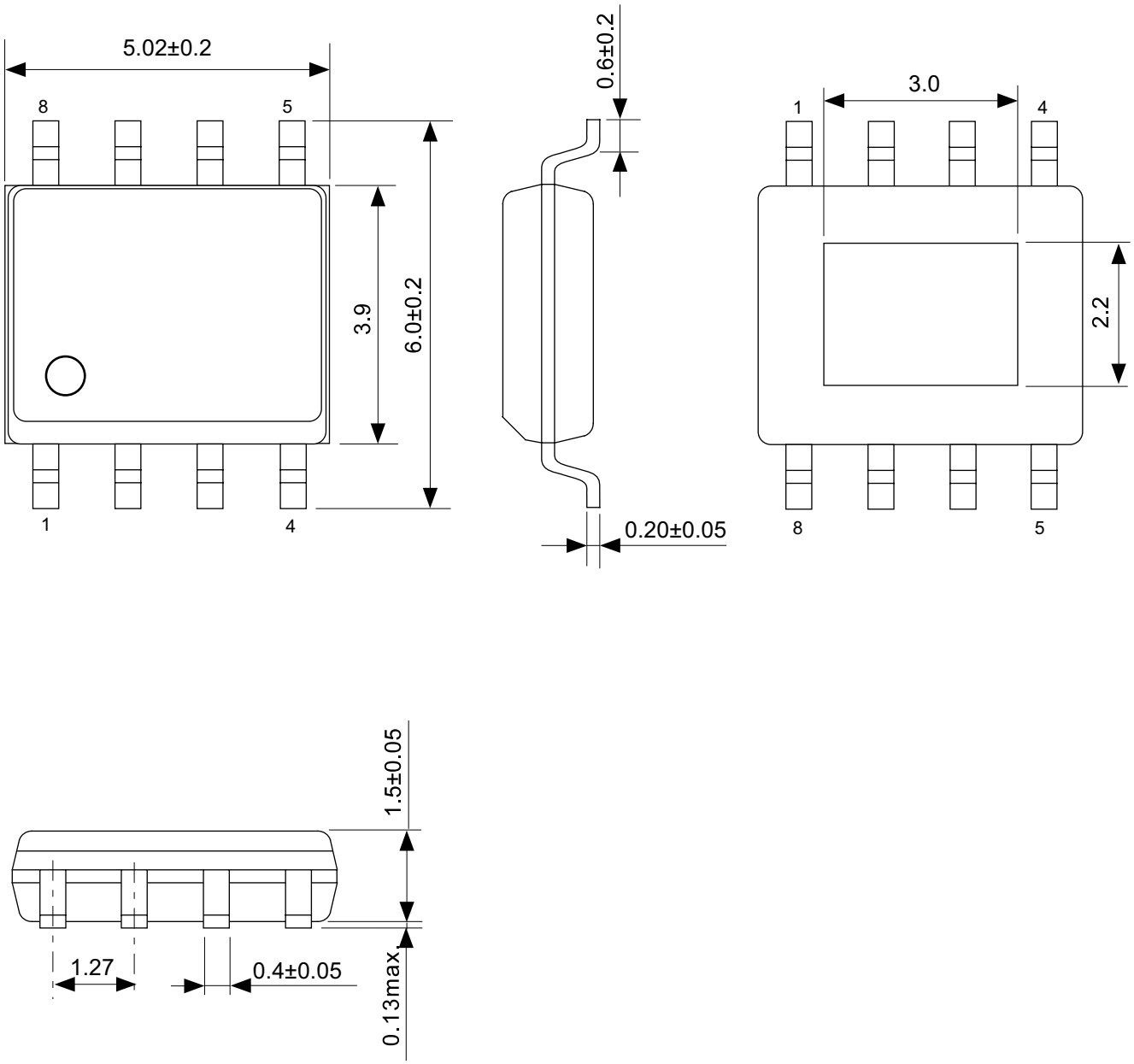
No. VA009-A-R-SD-1.0

TITLE	TO252-9S-A-Reel		
No.	VA009-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



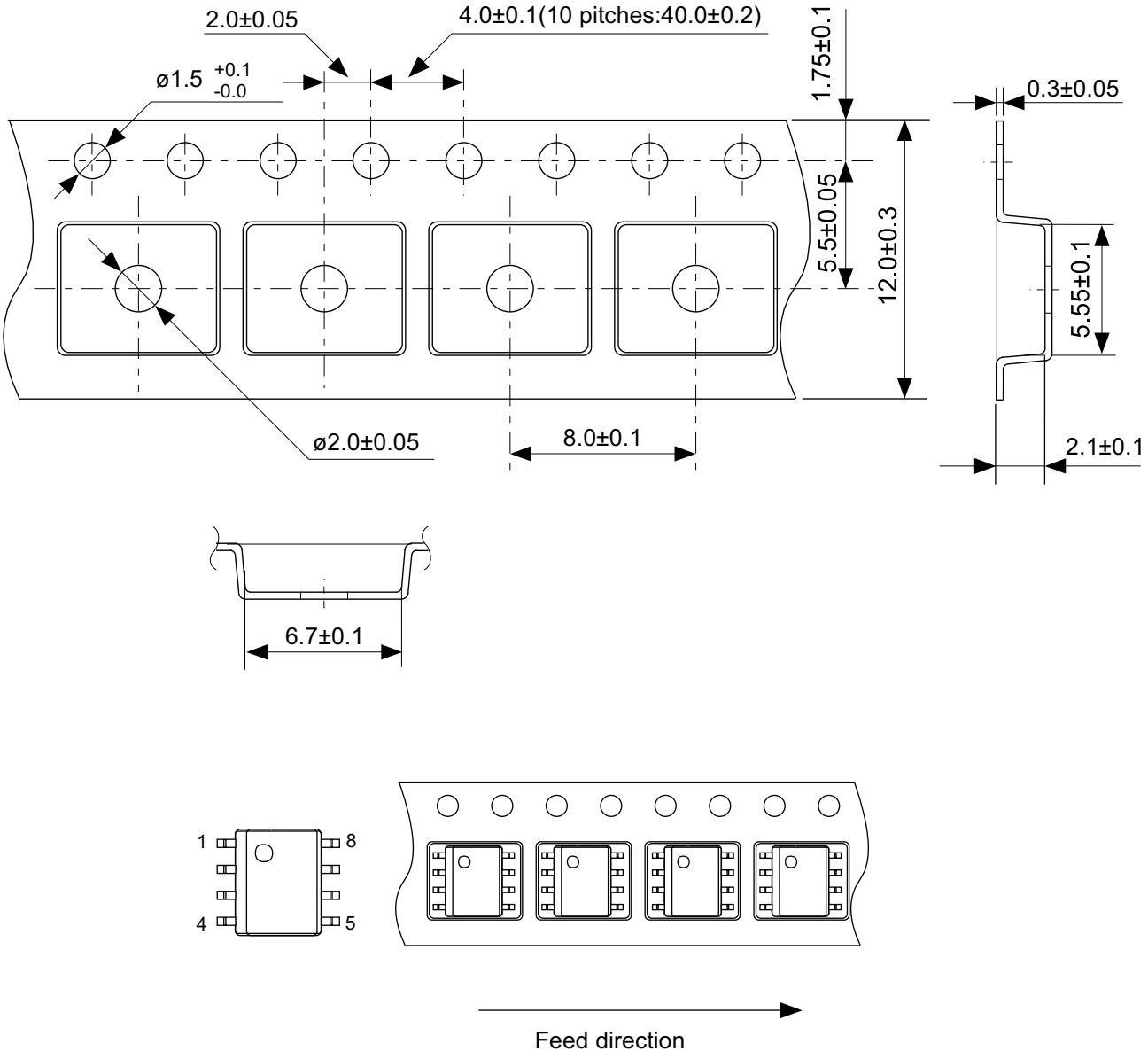
No. VA009-A-L-SD-1.0

TITLE	TO252-9S-A -Land Recommendation
No.	VA009-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



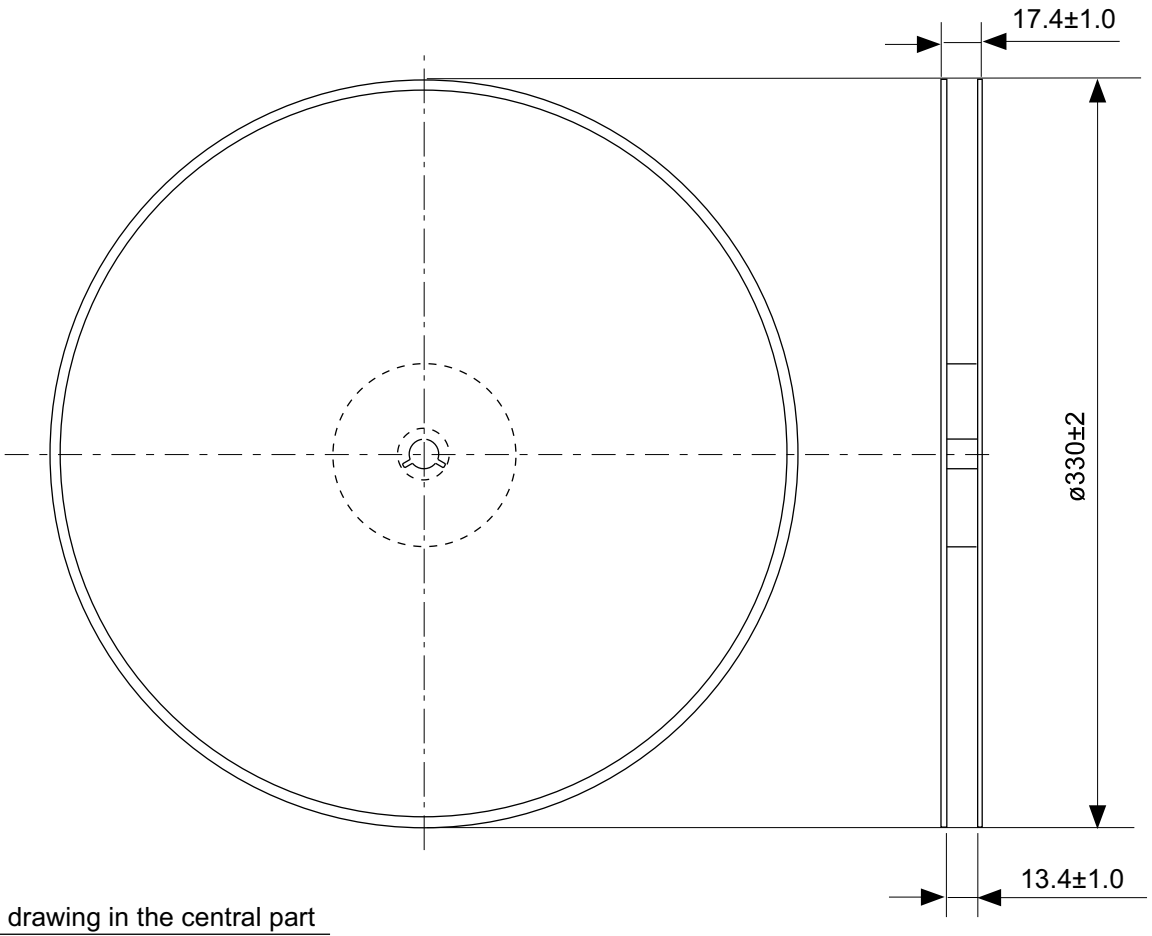
No. FH008-A-P-SD-2.0

TITLE	HSOP8A-A-PKG Dimensions
No.	FH008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

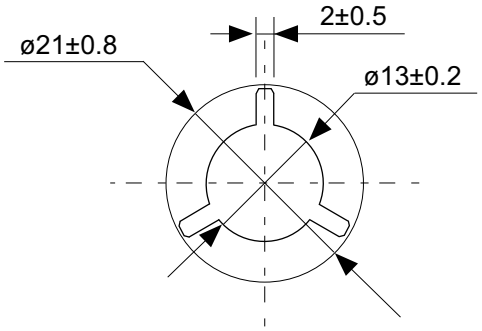


No. FH008-A-C-SD-1.0

TITLE	HSOP8A-A-Carrier Tape
No.	FH008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

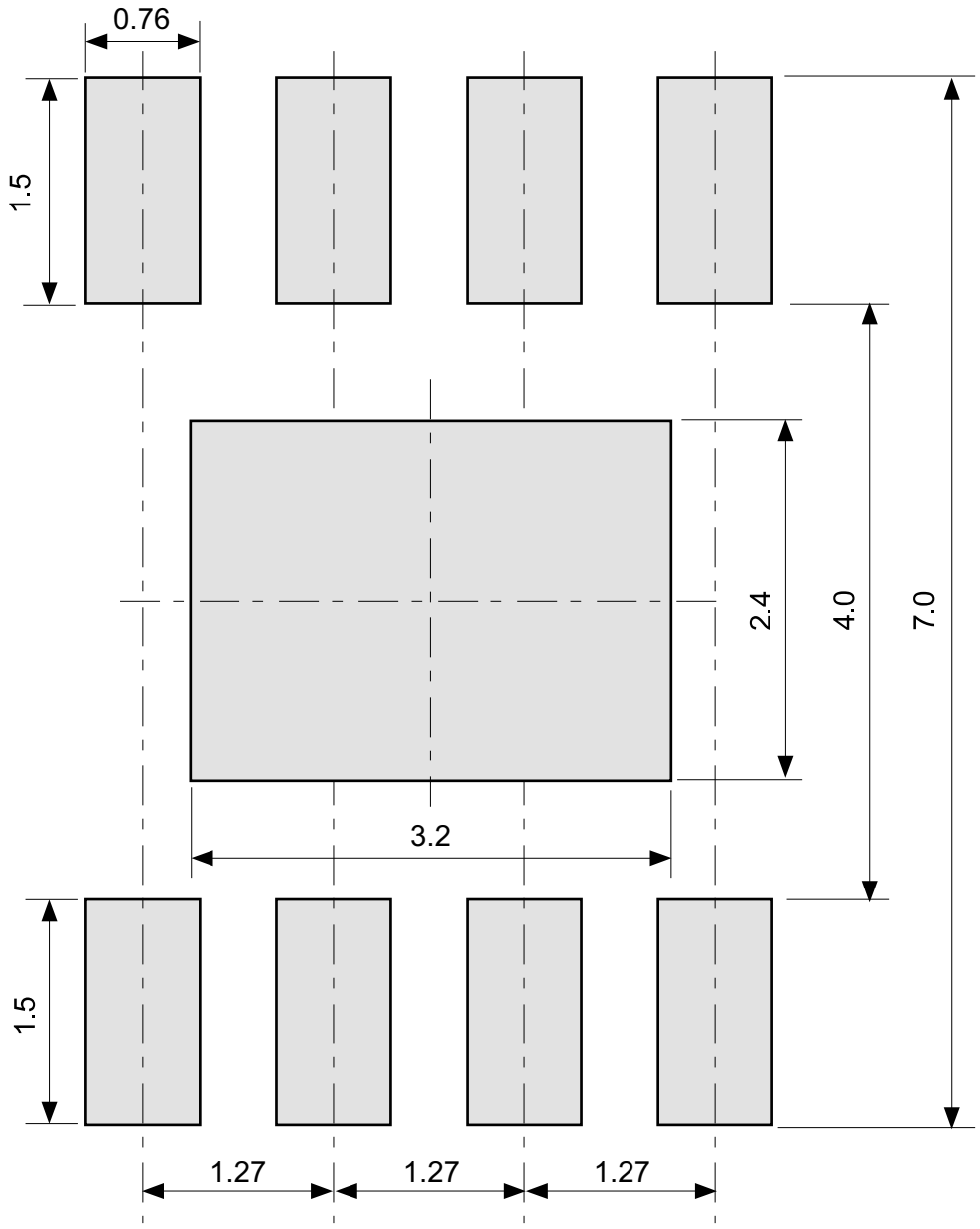


Enlarged drawing in the central part



No. FH008-A-R-SD-1.0

TITLE	HSOP8A-A-Reel		
No.	FH008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



No. FH008-A-L-SD-1.0

TITLE	HSOP8A-A -Land Recommendation
No.	FH008-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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