CMOS 1K-bit serial E²PROM
Easy interface with serial port
With memory protection

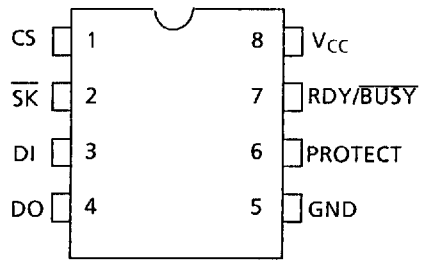
The S-2918I is a high speed, low power 1K-bit E²PROM that uses the CMOS floating-gate process. The organization is 128-word × 8-bit, and it is read or written serially. The memory array is composed of two banks, one of which has a memory protect function.

■ Features

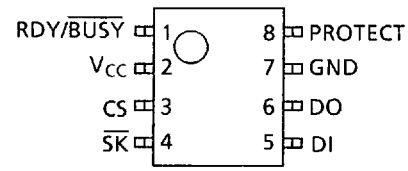
- Low power consumption
  Operating: 4.0 mA max.
  Standby: 100 µA max.
- 5-V single power supply
- Write operation with built-in timer
- Chip erase operation
- Continuous instructions are available (except READ)
- Memory protection
- Easy interface with serial port
- Rewritings: 104 or 105 times
- Data retention: 10 years

■ Pin Assignment

8-pin DIP
Top view



8-pin SOP
Top view



CS	Chip select
SK	Serial clock
DI	Serial data input
DO	Serial data output
GND	Ground(0 V)
RDY/BUSY	Status output

V_{CC}	Power supply voltage (+ 5V)
PROTECT	Memory protection control* Connected to Vcc or open: Protection valid Connected to GND: Protection invalid

*Memory protection

This function protects memory contents from erroneous writing when the CPU malfunctions. When the PROTECT pin is connected to VCC or is open, write to BANK1 (addresses 0 to 31) of the memory array is inhibited. When it becomes low, write operation can start.

Figure 1

■ Block Diagram

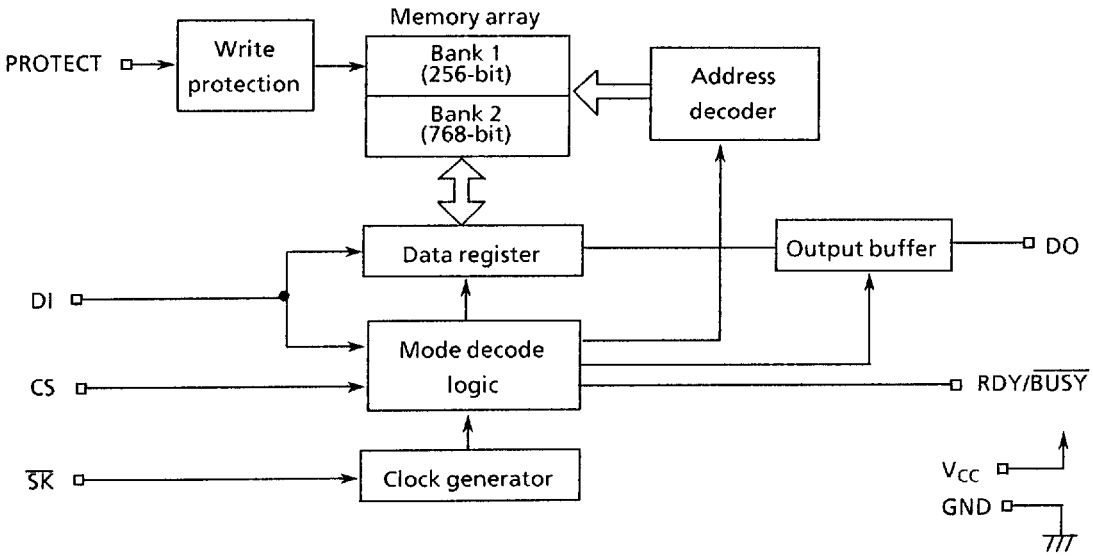


Figure 2

■ Instruction Set

Table 1

Instruction		Start bit	Op code	Address	Data
READ	(Read data)	1	1000xxx	A_6 to A_0x	D_7 to D_0
PROGRAM	(Program)	1	x100xxx	A_6 to A_0x	D_7 to D_0
WRAL	(Write all)	1	0001xxx	00000000	D_7 to D_0
ERAL	(Erase all)	1	0010xxx	00000000	—
PEN	(Program enable)	1	0011xxx	—	—
PDS	(Program disable)	1	0000xxx	—	—

x: Don't care

■ Absolute Maximum Ratings

Table 2

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to +95	°C
Storage temperature	T_{stg}	-65 to +150	°C

■ Recommended Operating Conditions

Table 3

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
High level input voltage	V_{IH}	2.0	—	V_{CC}	V
Low level input voltage	V_{IL}	−0.1	—	0.8	V
Operating temperature	T_{opr}	−40	—	+85	°C

■ DC Electrical Characteristics

Table 4

(Ta = -40°C to 85°C, V_{CC} = +5 V ± 10%)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption (READ, PEN, PDS)	I_{CC1}	V_{IN} = GND to V_{CC} DO = open	—	—	1.0	mA
Current consumption (PROGRAM, ERAL, WRAL)	I_{CC2}	V_{IN} = GND to V_{CC}	—	—	4.0	mA
Standby current consumption	I_{SB}	$\overline{CS}$ = GND $\overline{SK}$ = DI = GND or V_{CC}	—	—	100	µA
Input leakage current	I_{LI}	V_{IN} = V_{CC}, GND	—	0.1	10	µA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}, CS = GND	—	0.1	10	µA
Low level output voltage	V_{OL}	CMOS I_{OL} = 100 µA	—	—	0.1	V
		TTL I_{OL} = 2.1 mA	—	—	0.4	V
High level output voltage	V_{OH}	CMOS I_{OH} = -100 µA	V_{CC} - 0.3	—	—	V
		TTL I_{OH} = -400 µA	2.4	—	—	V
Write inhibit voltage	V_{WI}		—	—	3.7	V
Pull-up current for PROTECT control pin	I_{PU}	PROTECT pin = GND, V_{CC} = 5.5 V	—	—	10	µA

■ Rewriting Times

Table 5

(Ta = -40°C to 85°C, V_{CC} = +5 V ± 10%)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rewriting times	N_W	S-2918I01	10^4	—	—	times/word
		S-2918I10	10^5	—	—	times/word

■ Pin Capacitance

Table 6

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

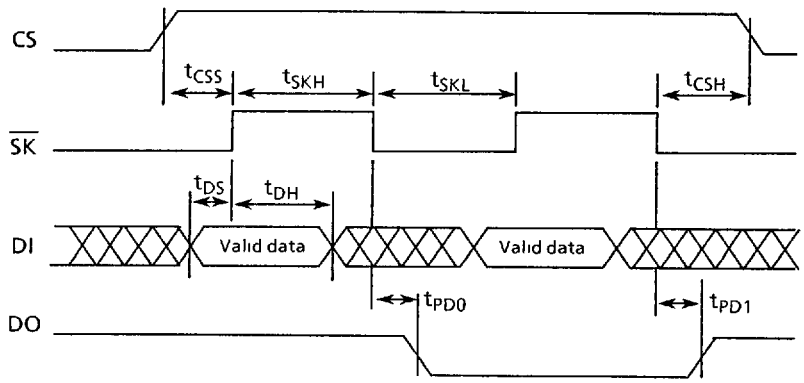
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V	—	—	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V	—	—	10	pF

■ AC Electrical Characteristics

Table 7

(Ta = -40°C to 85°C, V_{CC} = + 5 V ± 10%)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CS setup time	t_{CSS}	V_{IL} = 0.45 V V_{IH} = 2.40 V CL = 100 pF V_{OL} = 0.80 V V_{OH} = 2.0V	0.2	—	—	µs
CS hold time	t_{CSH}		0.1	—	—	µs
CS setup time (CPU)	$t_{CSS(CPU)}$		0.0	—	—	µs
CS hold time (CPU)	$t_{CSH(CPU)}$		1.0	—	—	µs
Data setup time	t_{DS}		0.2	—	—	µs
Data hold time	t_{DH}		0.2	—	—	µs
1 data output delay	t_{PD1}		0.0	—	0.4	µs
0 data output delay	t_{PD0}		0.0	—	0.4	µs
Clock frequency	f_{SK}		0	—	500	kHz
Clock pulse width	t_{SKH}, t_{SKL}		1.0	—	—	µs
Program time	t_{PR}		—	—	10	ms



Input data is fetched on the rising edge of $\overline{SK}$.
Output data is triggered at the fall of $\overline{SK}$.

Figure 3 Timing chart

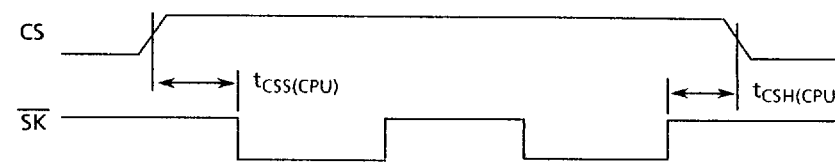


Figure 4 Timing chart of $t_{CSS(CPU)}$ and $t_{CSH(CPU)}$ when connecting to CPU

■ Operation

Each of op code with a start bit, address and data is composed of eight bits, and the S-2918I is easily interfaced with a CPU serial I/O port. A start bit is recognized when high of DI is fetched at the rise of the $\overline{SK}$ clock after rising of CS, and operation starts.

Note

- DI must be "L" during verify operation.

(1) Read mode

This mode reads data from a specified address. By the READ instruction, data is triggered at the fall of $\overline{SK}$, and output serially to DO pin.

The READ instruction is executed for all memory array bits regardless of the state of the PROTECT pin, program enable/disable mode.

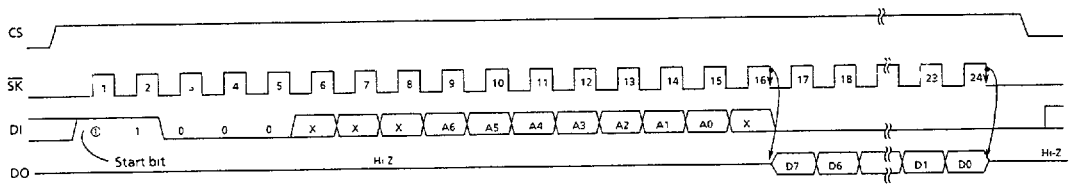


Figure 5 Read mode timing

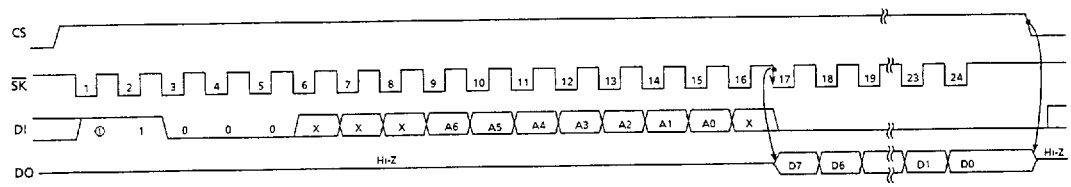


Figure 6 Read mode timing when connected to the CPU

(2) Program mode

The PROGRAM instruction, in program enable mode, writes data into the specified address.

When the last data (D0) is fetched in the data register, the data in the specified address is erased and new data is written. This operation is performed by the internal auto-timing generation circuit. During operation, the RDY/$\overline{\text{BUSY}}$ pin goes low, and other instructions cannot be accepted. When the next instruction follows, start that instruction by fetching the start bit after RDY/$\overline{\text{BUSY}}$ goes high.

Note: When the PROTECT pin is connected to V_{CC} or is open, the PROGRAM instruction to BANK1 is invalid and data cannot be written into BANK1. However the internal auto-timing generation circuit operates and the RDY/$\overline{\text{BUSY}}$ pin goes low.

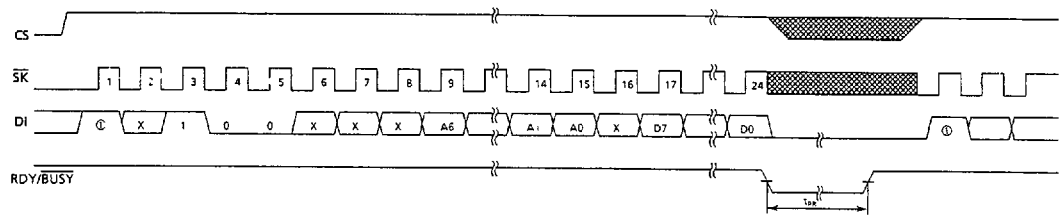


Figure 7 Program mode timing

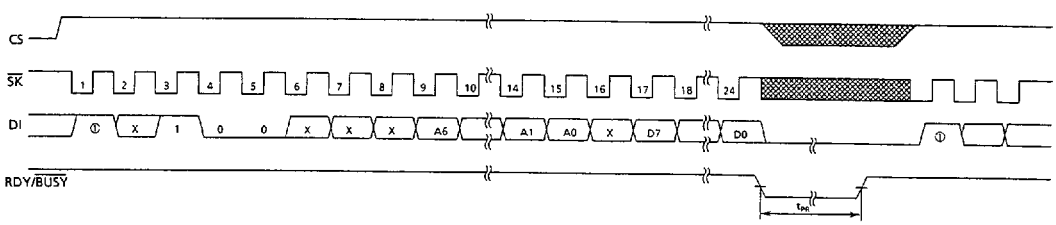


Figure 8 Program mode timing when connected to the CPU

(3) Write all (WRAL) mode

In the program enable mode, the WRAL instruction puts the S-2918I into write all mode. When the last data (D0) is fetched into the data register, the same data is written into all the addresses of the memory array. This operation is performed by the internal auto-timing generation circuit. During operation, the RDY/$\overline{\text{BUSY}}$ pin goes low, and other instructions cannot be accepted. When the next instruction follows, start that instruction by fetching the start bit after RDY/$\overline{\text{BUSY}}$ goes high.

Note:
- When the PROTECT pin is connected to V_{CC} or is open, the WRAL instruction to BANK1 is invalid and data cannot be written into BANK1.
- Before executing a WRAL instruction, set all memory array bits to 1. When the PROTECT pin is connected to V_{CC} or is open, set all bits of BANK2 to 1.

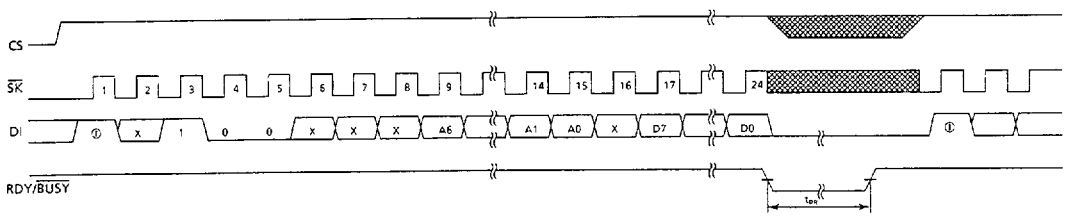


Figure 9 WRAL mode timing

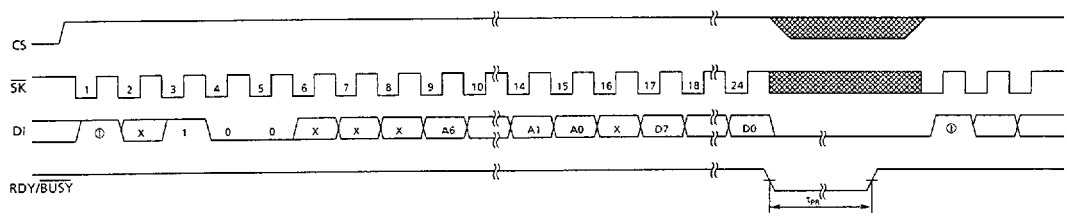


Figure 10 WRAL mode timing when connected to the CPU

(4) Erase all (ERAL) mode

In program enable mode, the ERAL instruction erases the whole of the chip's memory (all memory array bits are set to 1). This operation is performed by the internal auto-timing generation circuit. During operation, the RDY/$\overline{\text{BUSY}}$ pin goes low, and other instructions cannot be accepted. When the next instruction follows, start that instruction by fetching the start bit after RDY/$\overline{\text{BUSY}}$ goes high.

Note: When the PROTECT pin is connected to V_{CC} or is open, the ERAL instruction to BANK1 is invalid and data in BANK1 cannot be erased.

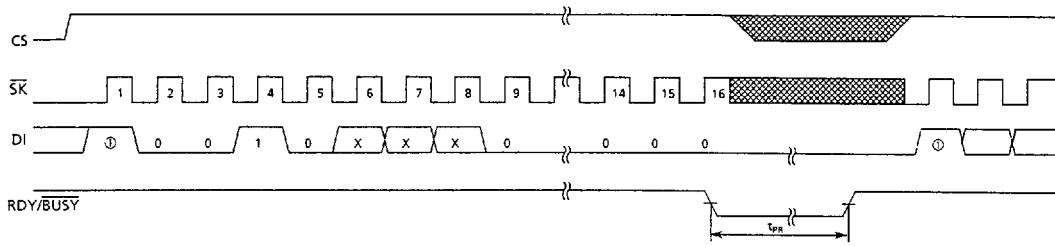


Figure 11 ERAL mode timing

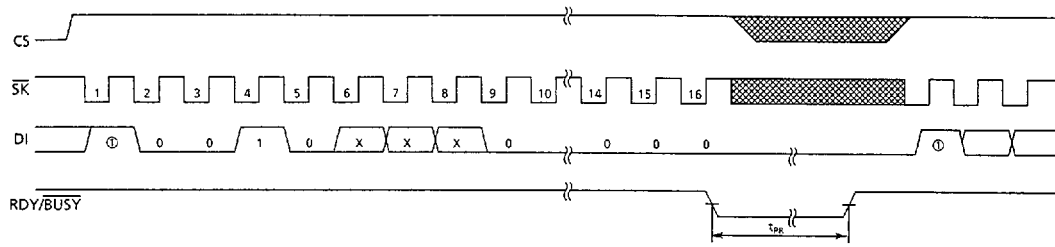


Figure 12 ERAL mode timing when connected to the CPU

(5) Program enable (PEN) and program disable (PDS) modes

The PEN instruction puts the S-2918I into program enable (PEN) mode. In this mode, PROGRAM, WRAL and ERAL instructions are enabled. The S-2918I remains in PEN mode until a PDS instruction is executed. The PDS instruction puts the S-2918I into program disable (PDS) mode. The PROGRAM, WRAL and ERAL instructions are ignored in the PDS mode; this mode is used to protect data against accidental programming.

Note: When power is applied, or the power supply voltage falls below the write inhibit voltage V_{WI}, an internal error protection circuit operates and puts the S-2918I into PDS mode.

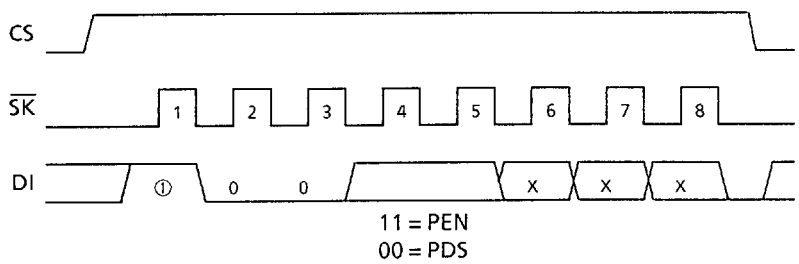


Figure 13 PEN/PDS mode timing

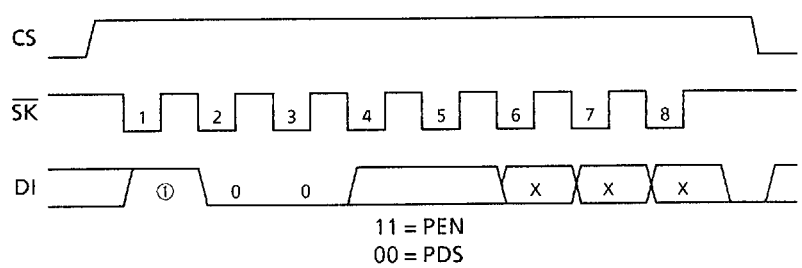


Figure 14 PEN/PDS mode timing when connected to the CPU

(6) Continuous execution

While CS is high, instructions can be continuously executed. An instruction is executed by 8 (including a start bit) × n (n = 1,2,3 ···) $\overline{SK}$. Fetching of the next instruction starts by fetching high of DI (when a start bit is recognized).
READ instruction cannot be executed continuously.

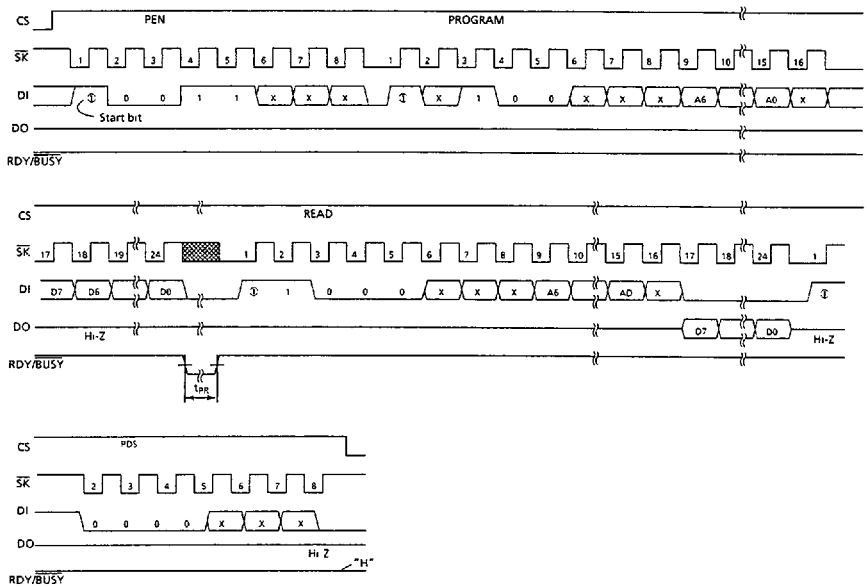


Figure 15 Continuous execution timing

■ Interface with CPU Serial Port

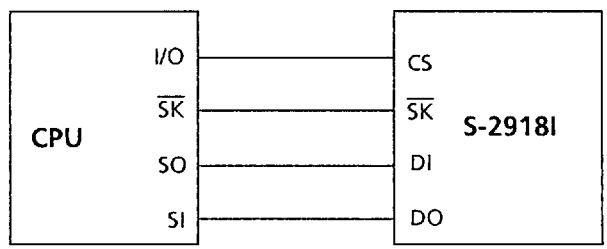


Figure 16 Circuit example

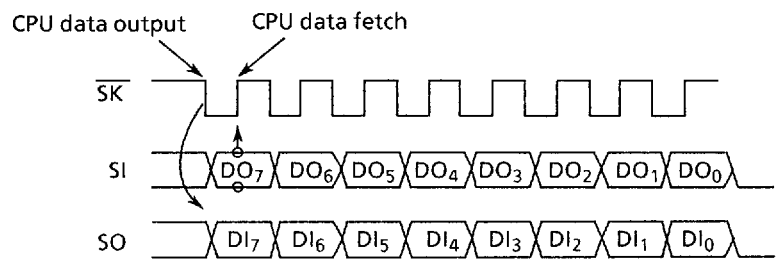


Figure 17 Serial shift timing

■ Dimensions (Unit:mm)

1. S-2918I (8-pin DIP)

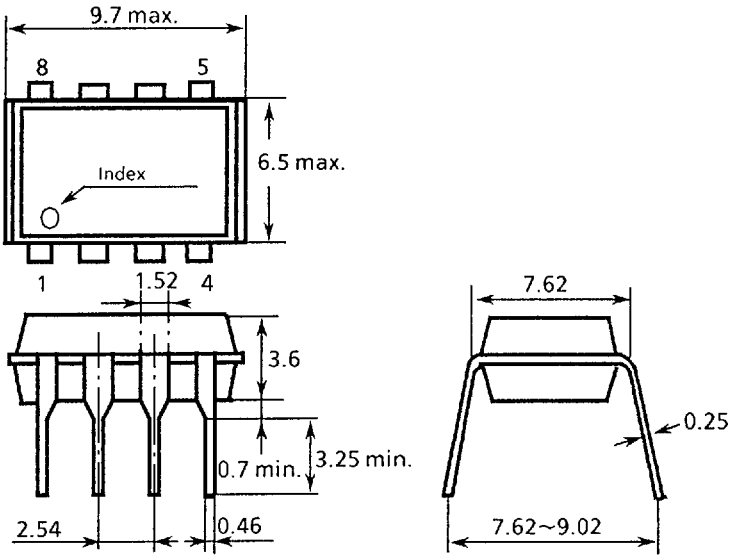


Figure 18

2. S-2918IF (8-pin SOP)

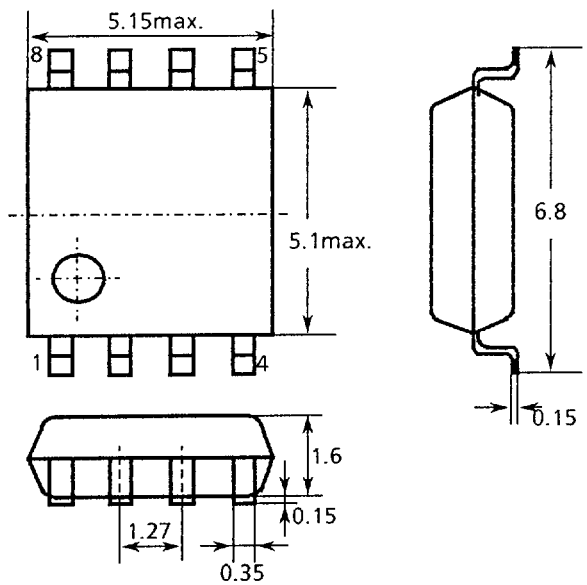


Figure 19

■ Ordering Information

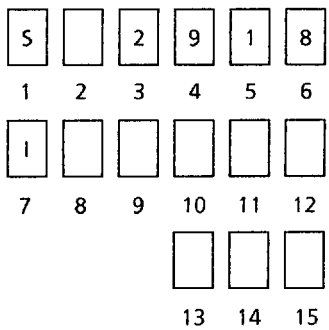
Table 8

Product name	Rewritings / word	Temperature	Package
S-2918I01	10^4	-40°C to 85°C	DIP plastic
S-2918IF01	10^4	-40°C to 85°C	SOP plastic
S-2918I10	10^5	-40°C to 85°C	DIP plastic
S-2918IF10	10^5	-40°C to 85°C	SOP plastic

Note : Each bit is set to 1 before delivery.

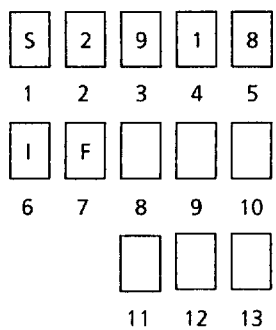
■ Markings

1. S-2918I (8-pin DIP)



1 : S
2 : Blank
3 to 6 : Product name
7 : Temperature range: I = -40 to 85°C
8 to 9 : Minimum rewritings: 01 = 104, 10 = 105
10 to 12 : Lot No.
13 : Assembly mark
14 : Last column of year
15 : Month of manufacturing: January = 1, February = 2, March = 3, April = 4, May = 5, June = 6, July = 7, August = 8, September = 9, October = X, November = Y, December = Z

2. S-2918IF (8-pin SOP)



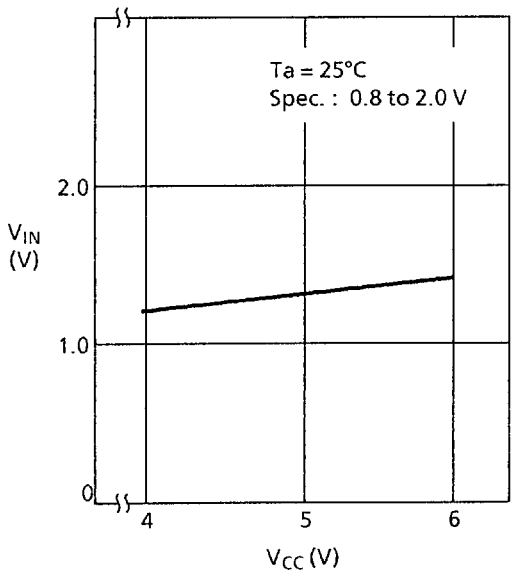
1 to 5 : Product name
6 : Temperature range: I = -40 to 85°C
7 : Package: F = SOP
8 to 9 : Minimum rewritings: 01 = 104, 10 = 105
10 : Assembly mark
11 : Month of manufacturing: January = 1, February = 2, March = 3, April = 4, May = 5, June = 6, July = 7, August = 8, September = 9, October = X, November = Y, December = Z
12 to 13 : Lot No.

■ Characteristics

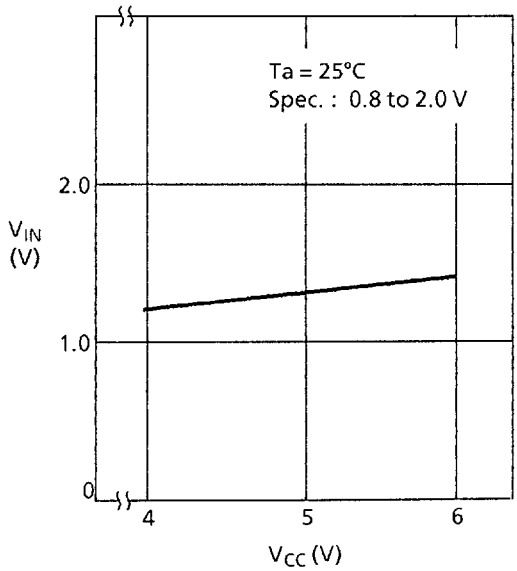
1. DC characteristics

1.1 Input voltage (V_{IN})

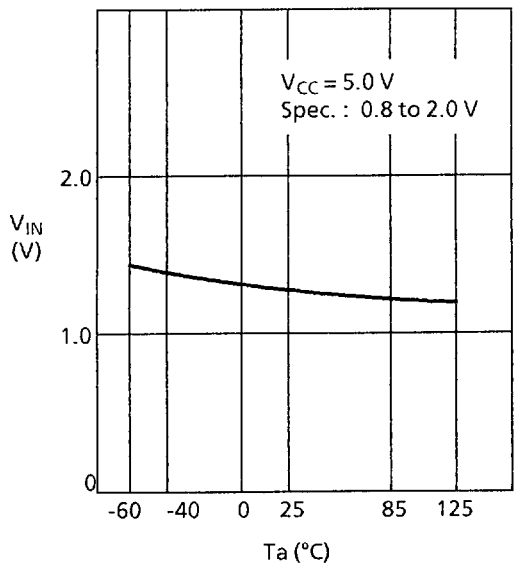
(1) Power supply voltage (V_{CC}) : CS pin



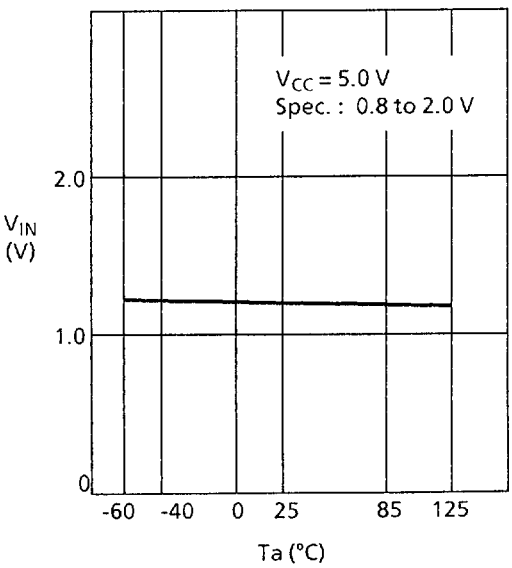
: $\overline{SK}$ pin



(2) Temperature (Ta) : CS pin

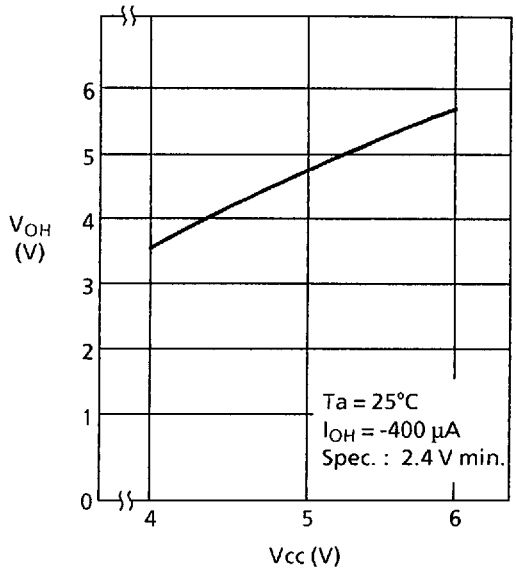


: $\overline{SK}$ pin

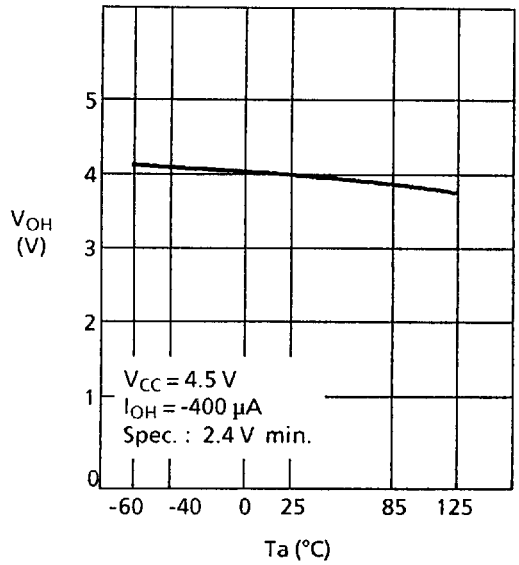


1.2 High level output voltage (V_{OH})

(1) Power supply voltage (V_{CC})

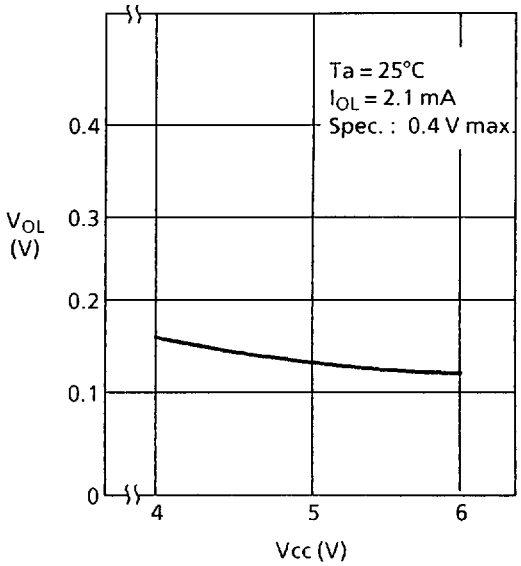


(2) Temperature (Ta)

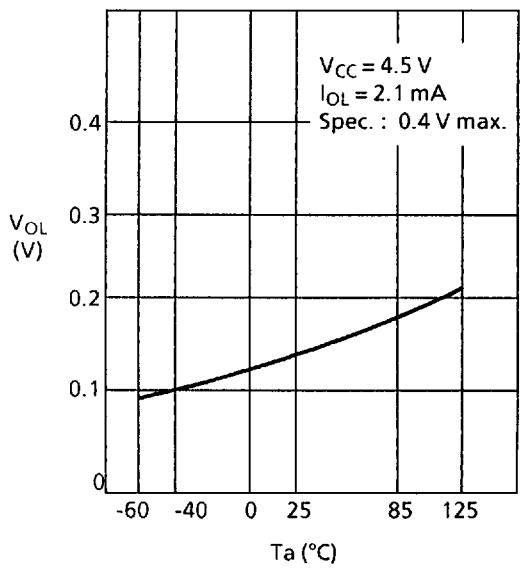


1.3 Low level output voltage (V_{OL})

(1) Power supply voltage (V_{CC})

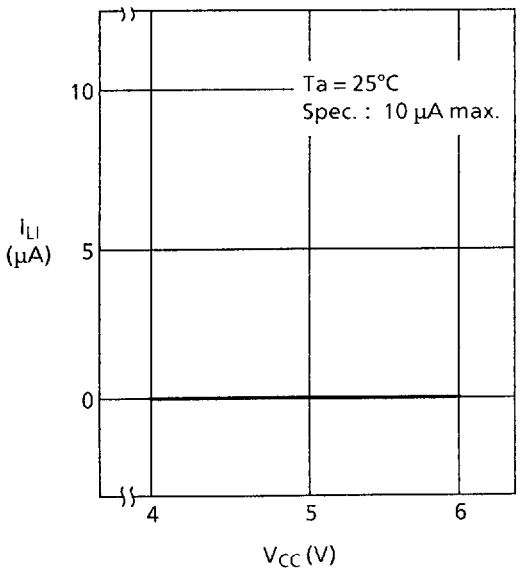


(2) Temperature (Ta)

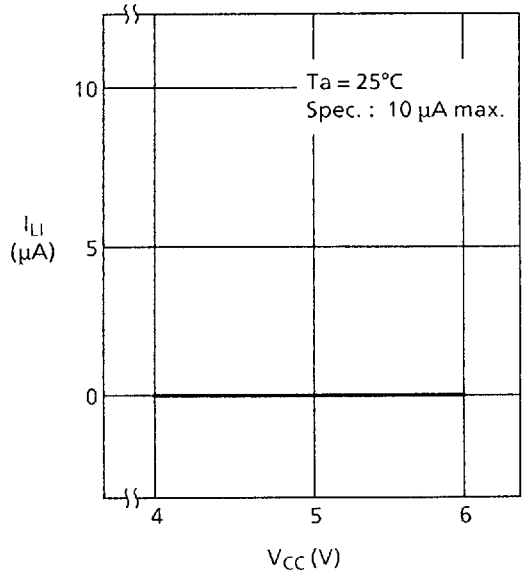


1.4 Input leakage current (I_{LI})

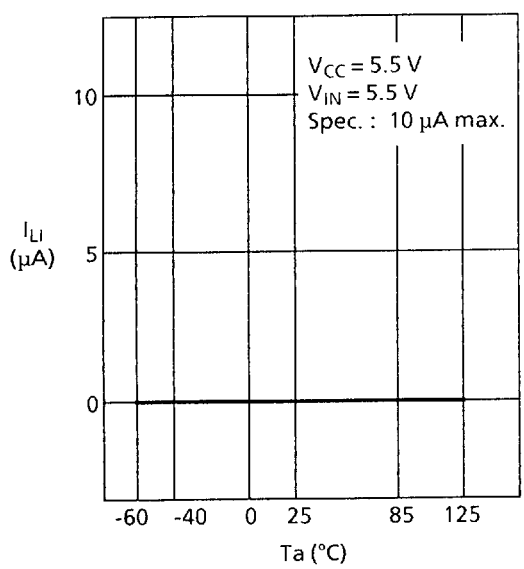
(1) Power supply voltage (V_{CC}) : CS pin



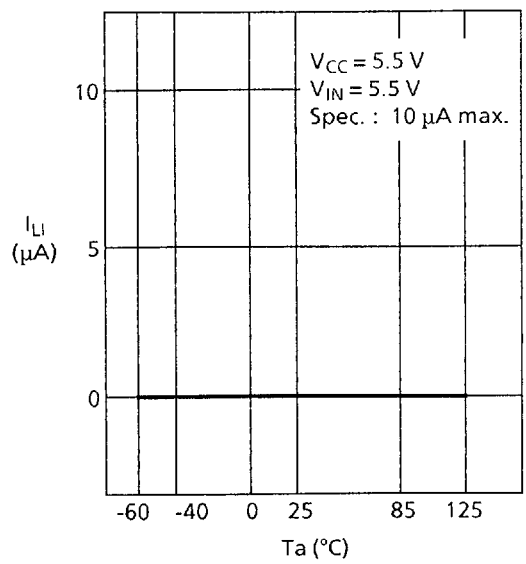
: $\overline{SK}$ and DI pins



(2) Temperature (Ta) : CS pin

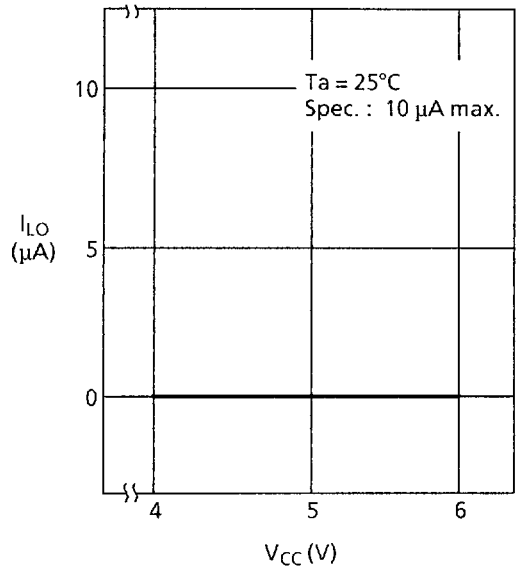


: $\overline{SK}$ and DI pins

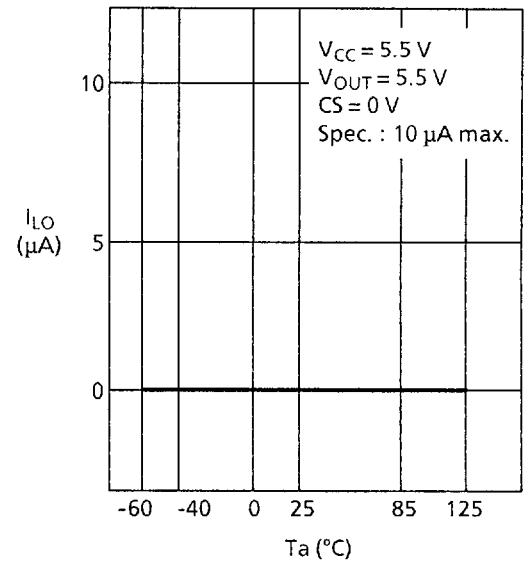


1.5 Output leakage current (I_{LO})

(1) Power supply voltage (V_{CC})

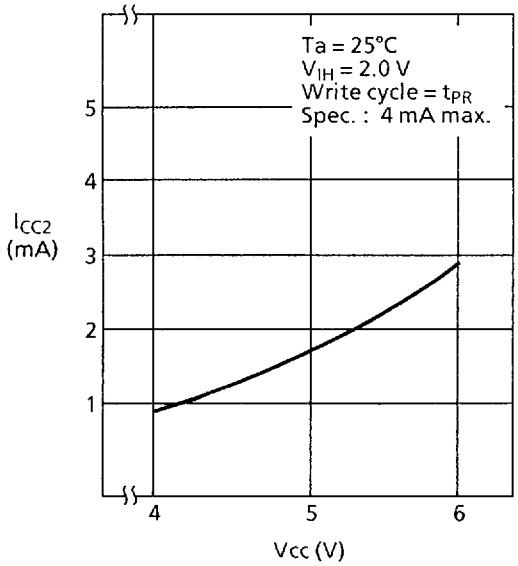


(2) Temperature (Ta) : DO pin

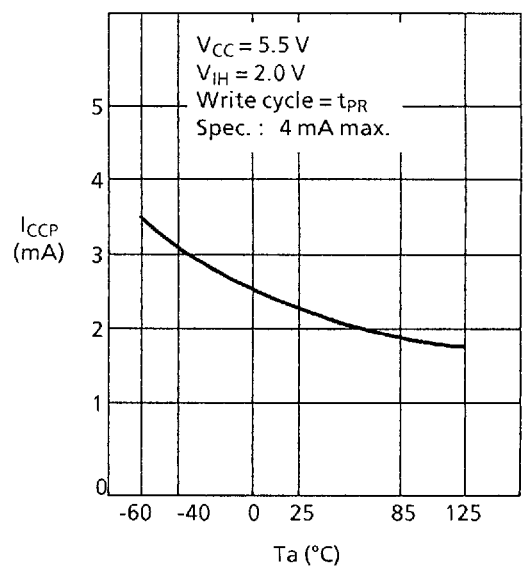


1.6 Writing current consumption (I_{CC2})

(1) Power supply voltage (V_{CC})

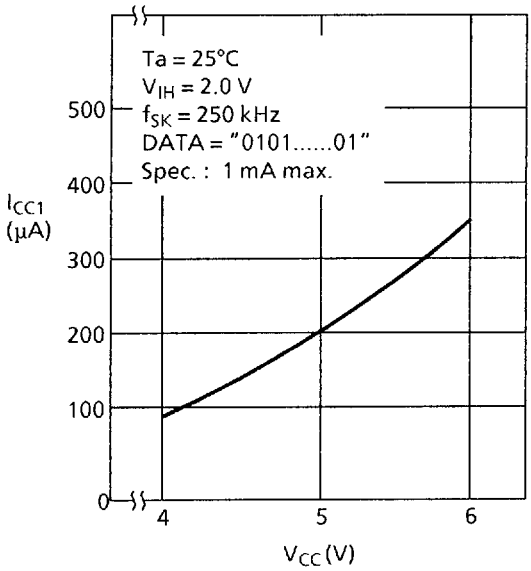


(2) Temperature (Ta)

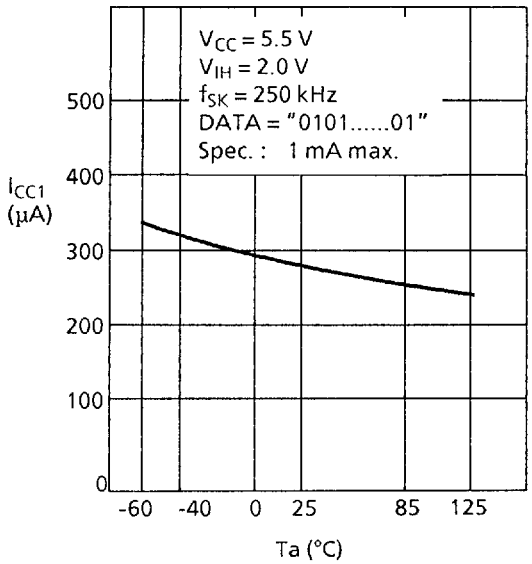


1.7 Reading current consumption (I_{CC1})

(1) Power supply voltage (V_{CC})

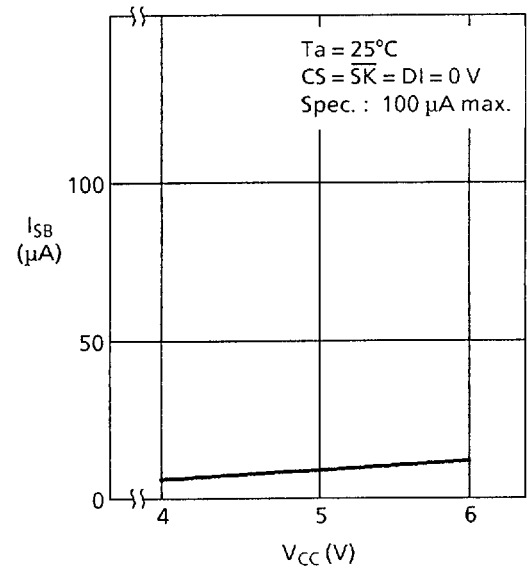


(2) Temperature (Ta)

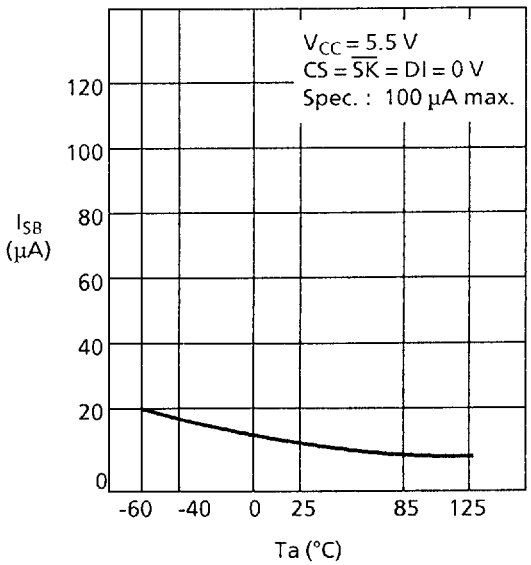


1.8 Standby current consumption (I_{SB})

(1) Power supply voltage (V_{CC})



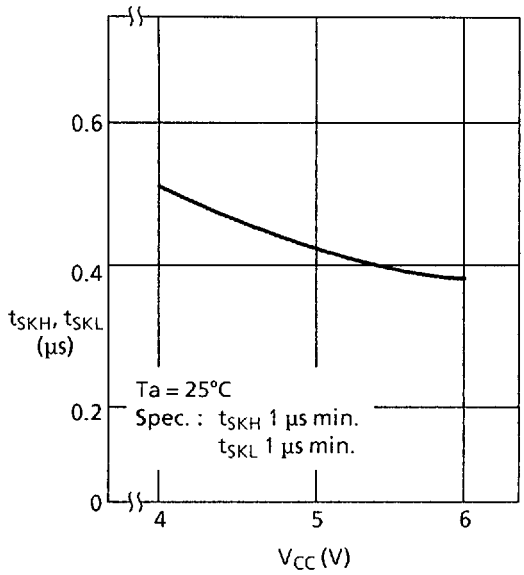
(2) Temperature (Ta)



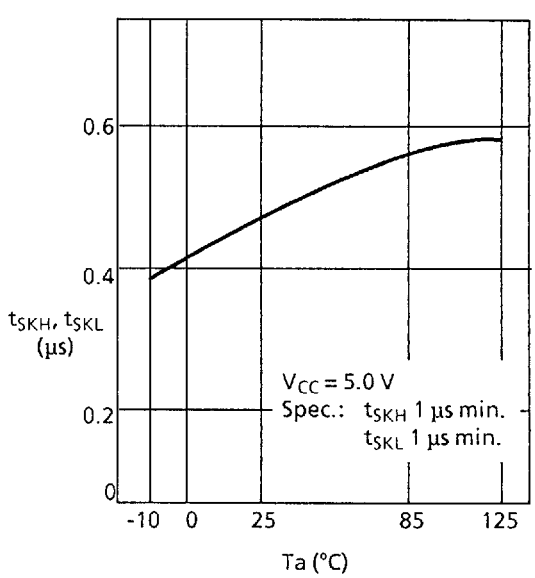
2. AC characteristics

2.1 Clock pulse width (t_{SKH} or t_{SKL})

(1) Power supply voltage (V_{CC})

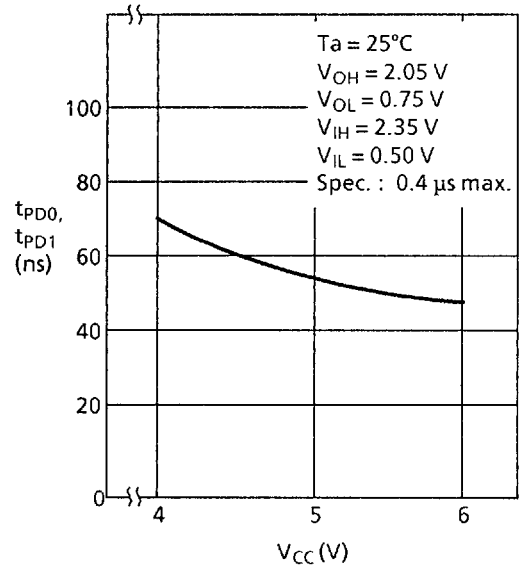


(2) Temperature (Ta)

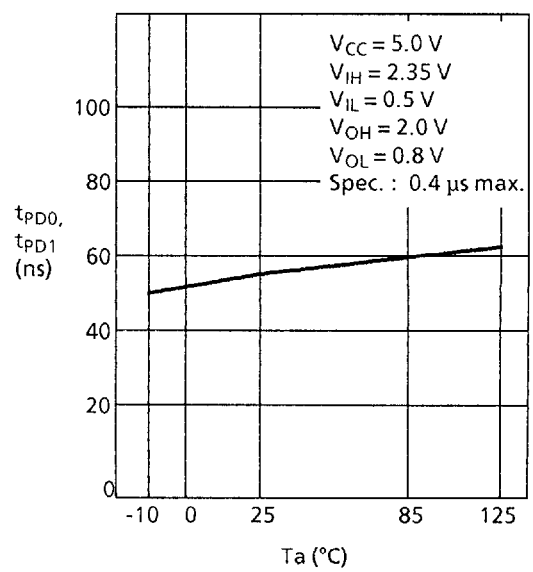


2.2 Data output delay (t_{PD0} or t_{PD1})

(1) Power supply voltage (V_{CC})

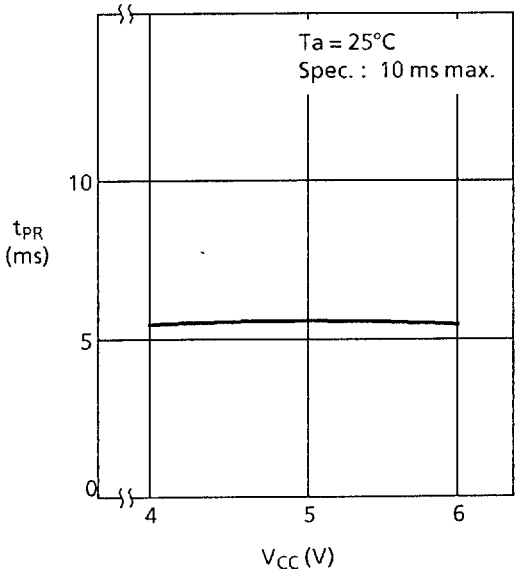


(2) Temperature (Ta)



2.3 Program time (t_{PR})

(1) Power supply voltage (V_{CC})



(2) Temperature (Ta)