## Contents

PARALLEL NON-VOLATILE RAM

# S-22 Series

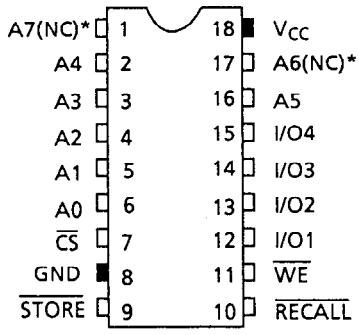
The S-22 Series is a non-volatile CMOS RAM, composed of a CMOS static RAM and a non-volatile electrically erasable and programmable memory ($E^2$PROM) to backup the SRAM. The organization is 256-word × 4-bit (total 1K bits) for the S-22H12 and the S-22S12, and 64-word × 4-bit (total 256 bits) for the S-22H10 and the S-22S10.

## ■ Features

- 1K bits
  S-22H12: TTL input, compatible with the X2212 of Xicor
  S-22S12: Schmitt input for $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins
- 256 bits
  S-22H10: TTL input, compatible with the X2210 of Xicor
  S-22S10: Schmitt input for $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins
- Erroneous store protection : ≈ 3.5 V
- + 5-V single power supply ( + 5 V ± 10%)
- Low current consumption
  Operating: 10 mA typ.
  Standby : 1 μA max.
- Access time: 200 ns max.
- $E^2$PROM store cycles : $10^5$ times
- $E^2$PROM data retention: 10 years
- 18-pin DIP/SOP package

## ■ Pin Assignment

18-pin DIP/SOP
Top view

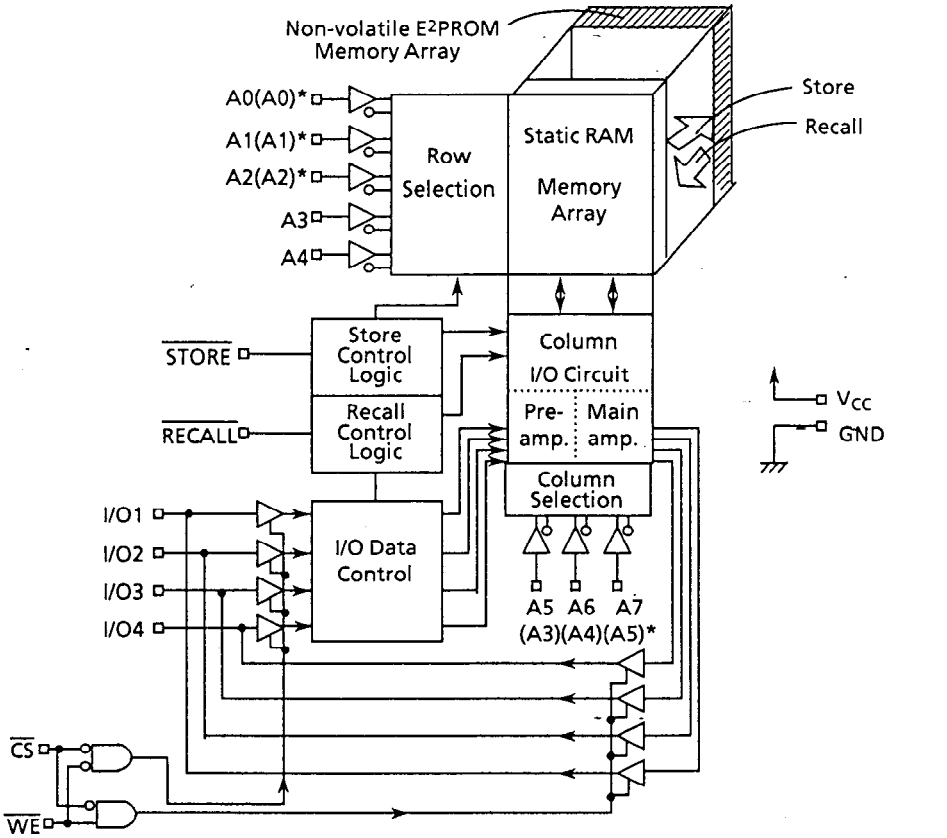



| | |
|---|---|
| A0 to A7(A5)* | Address input |
| I/O1 to I/O4 | Data input/output |
| $\overline{\text{WE}}$ | Write enable |
| $\overline{\text{CS}}$ | Chip select |
| $\overline{\text{RECALL}}$ | Recall |
| $\overline{\text{STORE}}$ | Store |
| GND | Ground |
| $V_{CC}$ | Power supply voltage ( + 5 V) |

*( ) is for the S-22H10 and S-22S10.

Figure 1

## ■ Block Diagram




*( ) is for the S-22H10 and S-22S10.

Figure 2

## ■ Absolute Maximum Ratings

Table 1

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | -0.3 to +6.0 | V |
| Input voltage | $V_{IN}$ | -0.3 to $V_{CC}$ + 0.3 | V |
| Output voltage | $V_{OUT}$ | 0.0 to $V_{CC}$ | V |
| Storage temperature under bias | $T_{bias}$ | -50 to +95 | °C |
| Storage temperature | $T_{stg}$ | -65 to +150 | °C |

## ■ Recommended Operating Conditions

Table 2

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V |
| High level input voltage 1 | $V_{IH}$ | S-22H Series : All inputs<br>S-22S Series : $\overline{CS}$, $\overline{WE}$, I/O and address | 2.0 | — | $V_{CC}$ | V |
| High level input voltage 2 | $V_{IHS}$ | S-22S Series : $\overline{STORE}$ and $\overline{RECALL}$ | 3.4 | — | $V_{CC}$ | V |
| Low level input voltage 1 | $V_{IL}$ | S-22H Series : All inputs<br>S-22S Series : $\overline{CS}$, $\overline{WE}$, I/O and address | 0.0 | — | 0.8 | V |
| Low level input voltage 2 | $V_{ILS}$ | S-22S Series : $\overline{STORE}$ and $\overline{RECALL}$ | 0.0 | — | 0.8 | V |
| Operating temperature | $T_{opr}$ | | -40 | — | +85 | °C |

## ■ Pin Capacitance

Table 3

(Ta = 25°C, f = 1.0 MHz, $V_{CC}$ = 5 V)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V | — | — | 6 | pF |
| Output capacitance (I/O pins) | $C_{I/O}$ | $V_{I/O}$ = 0 V | — | — | 10 | pF |

## ■ DC Electrical Characteristics

Table 4

(Ta = -40°C to 85°C, $V_{CC}$ = + 5 V ± 10%)

| Parameter | Symbol | Conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Operating current consumption | $I_{CC}$ | | — | 10 | 30 | mA |
| Standby current | $I_{SB}$ | All inputs are $V_{CC}$ | — | — | 1 | μA |
| Input leakage current | $I_{LI}$ | $V_{IN}$ = GND to $V_{CC}$ | — | 0.1 | 1 | μA |
| Output leakage current | $I_{LO}$ | $V_{OUT}$ = GND to $V_{CC}$ | — | 0.1 | 1 | μA |
| Low level output voltage | $V_{OL}$ | CMOS : $I_{OL}$ = 100 μA | — | — | 0.1 | V |
| | | TTL : $I_{OL}$ = 4.2 mA | — | — | 0.4 | V |
| High level output voltage | $V_{OH}$ | CMOS : $I_{OH}$ = − 100 μA | $V_{CC}$-0.7 | — | — | V |
| | | TTL : $I_{OH}$ = − 2 mA | 2.4 | — | — | V |
| Store inhibition voltage | $V_{WI}$ | | — | 3.5 | 4.1 | V |
| Schmitt width | $V_{WD}$ | S-22S Series : $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ | 0.4 | — | — | V |

## ■ Data Hold Characteristics

Table 5

| Parameter | Symbol | Conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Data hold voltage | $V_{DH}$ | $\overline{CS} \geq V_{CC}$-0.2V, $\overline{RECALL} \geq V_{CC}$-0.2V | 1.5 | — | 5.5 | V |
| Data hold setup time | $t_{CDH}$ | | 50 | — | — | ns |
| Recovery time | $t_R$ | | 300 | — | — | ns |

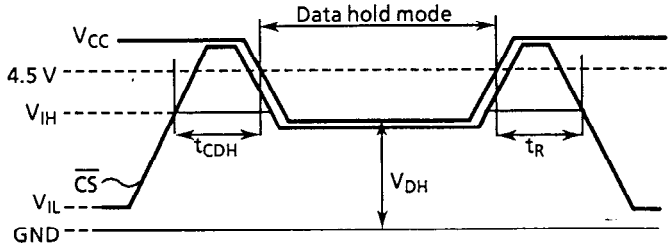



Figure 3 Data hold timing chart

## ■ AC Electrical Chracteristics

Table 6 Measuring conditions

| Parameter | Conditions | |
|---|---|---|
| Input pulse voltage | S-22H Series : All inputs<br>S-22S Series : $\overline{CS}$, $\overline{WE}$, I/O and address | 0.0 to 3.0 V |
| | S-22S Series : $\overline{STORE}$ and $\overline{RECALL}$ | 0.0 to 4.0 V |
| Input pulse rise/fall time | | 10 ns |
| I/O reference voltage | | 1.5 V |
| Output load | | 1TTL + 100pF |

1. Read cycle

Table 7

| Parameter | Symbol | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Read cycle time | $t_{RC}$ | 200 | — | — | ns |
| Address access time | $t_{AA}$ | — | — | 200 | ns |
| $\overline{CS}$ access time | $t_{CS}$ | — | — | 200 | ns |
| Output data hold time | $t_{OH}$ | 20 | — | — | ns |
| Output enable time ($\overline{CS}$) | $t_{CLZ}$ | 10 | — | — | ns |
| Output disable time ($\overline{CS}$) | $t_{CHZ}$ | 10 | — | 70 | ns |

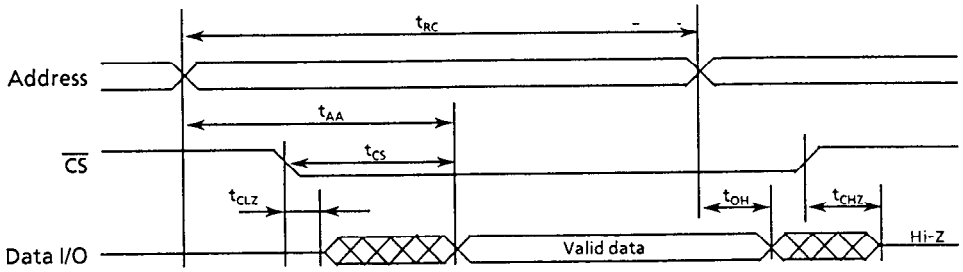



Figure 4

2. Write Cycle

Table 8

| Parameter | Symbol | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Write cycle time | $t_{WC}$ | 200 | — | — | ns |
| $\overline{CS}$ pulse width | $t_{CW}$ | 120 | — | — | ns |
| Address setup time | $t_{AS}$ | 20 | — | — | ns |
| $\overline{WE}$ pulse width | $t_{WP}$ | 120 | — | — | ns |
| Write reset time | $t_{WR}$ | 25 | — | — | ns |
| Input data setup time | $t_{DW}$ | 50 | — | — | ns |
| Input data hold time | $t_{DH}$ | 20 | — | — | ns |
| Output disable time ($\overline{WE}$) | $t_{WHZ}$ | 10 | — | 70 | ns |
| Output enable time ($\overline{WE}$) | $t_{WLZ}$ | 10 | — | — | ns |

· Write cycle 1 : $\overline{WE}$ control

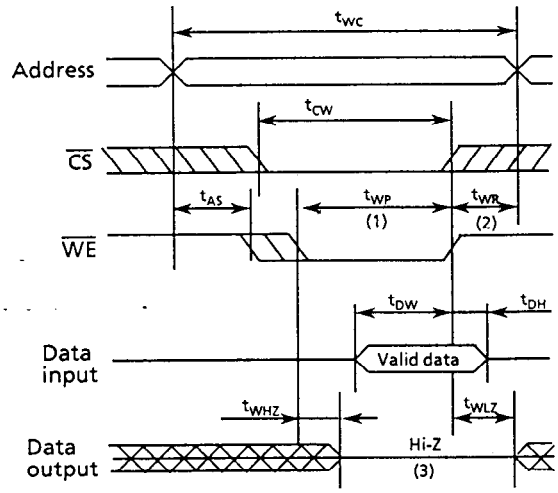



Figure 5

· Write cycle 2 : $\overline{CS}$ control

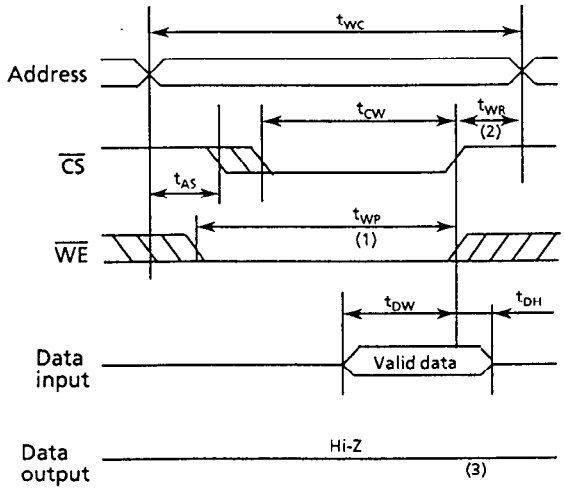



Figure 6

(1) The write cycle starts when both $\overline{CS}$ and $\overline{WE}$ are low.

(2) $t_{WR}$ is the period of time from the rise of $\overline{CS}$ or $\overline{WE}$ whichever is the first to the end of write cycle.

(3) Output remains in high-impedance state when $\overline{CS}$ falls simultaneously with or after the fall of $\overline{WE}$.

3. Store Cycle

Table 9

| Parameter | Symbol | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Store time | $t_{ST}$ | — | — | 10 | ms |
| Store pulse width | $t_{STP}$ | 200 | — | — | ns |
| Store disable time | $t_{STZ}$ | — | — | 100 | ns |
| Store enable time | $t_{OST}$ | 10 | — | — | ns |

Store operation starts at the falling of $\overline{STORE}$.

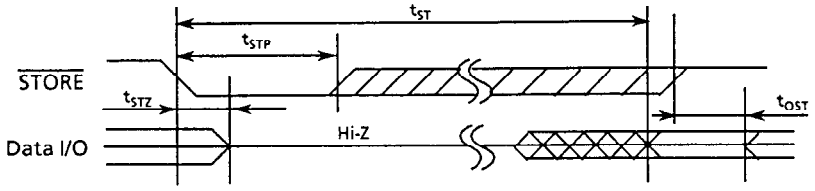



Figure 7

4. Recall cycle

Table 10

| Parameter | Symbol | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Recall cycle time | $t_{RCC}$ | 1300 | — | — | ns |
| Recall pulse width | $t_{RCP}$ | 200 | — | — | ns |
| Recall disable time | $t_{RCZ}$ | — | — | 100 | ns |
| Recall enable time | $t_{ORC}$ | 10 | — | — | ns |
| Recall data access time | $t_{ARC}$ | — | — | 1100 | ns |

Recall operation starts at the rise of $\overline{\text{RECALL}}$. It can be repeated without limitation.

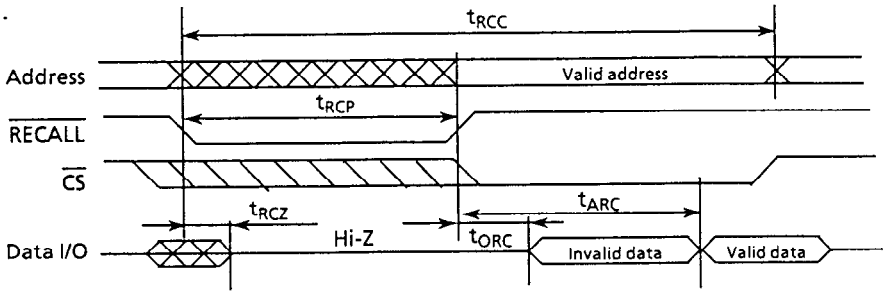



Figure 8

## ■ Operation Mode

Table 11

| Mode | Input | | | | Input/output |
|---|---|---|---|---|---|
| | $\overline{CS}$ | $\overline{WE}$ | $\overline{RECALL}$ | $\overline{STORE}$ | |
| Standby mode | H | X | H | H | Output is high impedance |
| Read mode | L | H | H | H | Output data |
| Write mode | L | L | H | H | Input data |
| Recall mode | X<br>H | H<br>X | L<br>L | H<br>H | Output is high impedance |
| Store mode | X<br>H | H<br>X | H<br>H | L<br>L | Output is high impedance |

X : Don't care

Notes · When $\overline{\text{RECALL}}$ and $\overline{\text{STORE}}$ are simultaneously input, $\overline{\text{RECALL}}$ is valid.
· When $\overline{\text{RECALL}}$ is low, $\overline{\text{STORE}}$ cannot be received.
· When power supply voltage ($V_{CC}$) is below store inhibition voltage $V_{WI}$, the store operation is inhibited.

## ■ Operation

1. Standby mode

When $\overline{CS}$ goes high, the S-22 Series enters into the standby mode: power consumption becomes lowest, and I/O1 to I/O4 are high impedance.

2. SRAM modes

2.1 Read mode

When $\overline{CS}$ is low and $\overline{WE}$ is high, the S-22 Series enters into the read mode: the SRAM data is output to I/O1 to I/O4.

2.2 Write mode

When $\overline{CS}$ and $\overline{WE}$ are low, the S-22 Series enters into the write mode: the data input in I/O1 to I/O4 is written to the SRAM.

3. SRAM⇆E²PROM mode

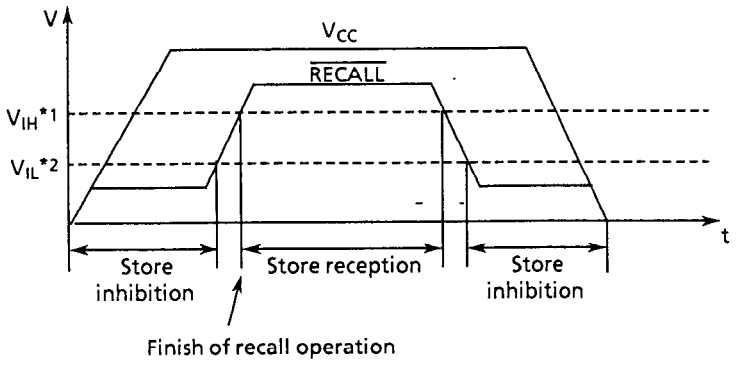
3.1 Store mode

When $\overline{\text{STORE}}$ goes $V_{IL}(V_{ILS})$, the S-22 Series enters into the store mode: the SRAM data is copied to the E²PROM. The original data in the SRAM is effective. Since the copied data in the E²PROM is non-volatile, they are retained even if power turns off. When $\overline{\text{STORE}}$ falls, the store operation starts and finishes automatically. When store operation starts, I/O1 to I/O4 go to high impedance and other operations are inhibited until store operation is finished and $\overline{\text{STORE}}$ goes to high. During store operation, the CPU can access other instructions.

The store operation is inhibited if power supply voltage ($V_{CC}$) is under $V_{WI}$ ($\simeq$ 3.5 V).

The following two methods prevent erroneous store, caused by noise when power turns on or off:

- $\overline{\text{RECALL}}$ goes $V_{IL}(V_{ILS})$ when power turns on or off (see Figure 9).
- $\overline{\text{STORE}}$ connects to $V_{CC}$ with pull-up resistor.




*1 $V_{IHS}$ for the S-22S Series
*2 $V_{ILS}$ for the S-22S Series

**Figure 9 STORE inhibition period and reception period at power ON and OFF**

3.2 Recall mode

When $\overline{\text{RECALL}}$ goes $V_{IL}(V_{ILS})$, the S-22 Series enters into the recall mode: the data copied into the E²PROM is recopied to the SRAM. The recopied data can be read or written as SRAM data. Even if the data is copied repeatedly, the data in the E²PROM does not change. Other operations are inhibited during its operation.

## ■ Dimensions (Unit:mm)

1. 18-pin DIP

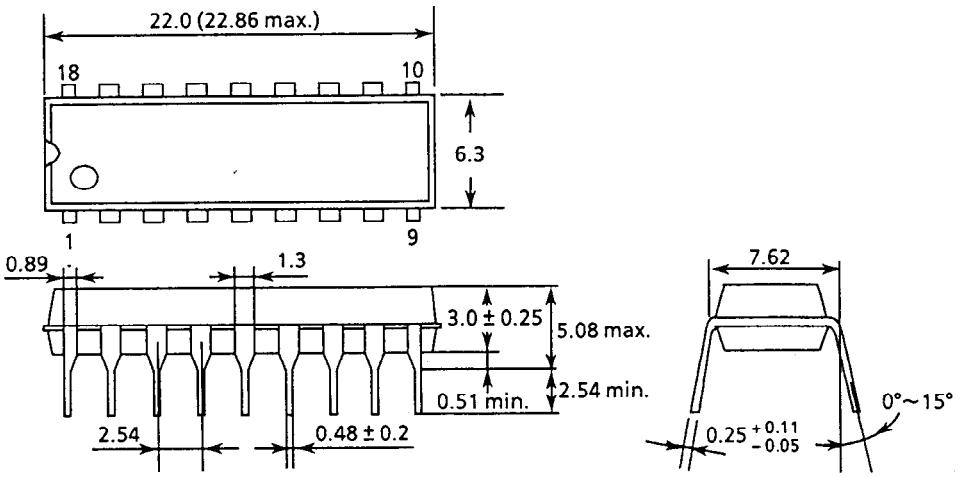



Figure 10

2. 18-pin SOP

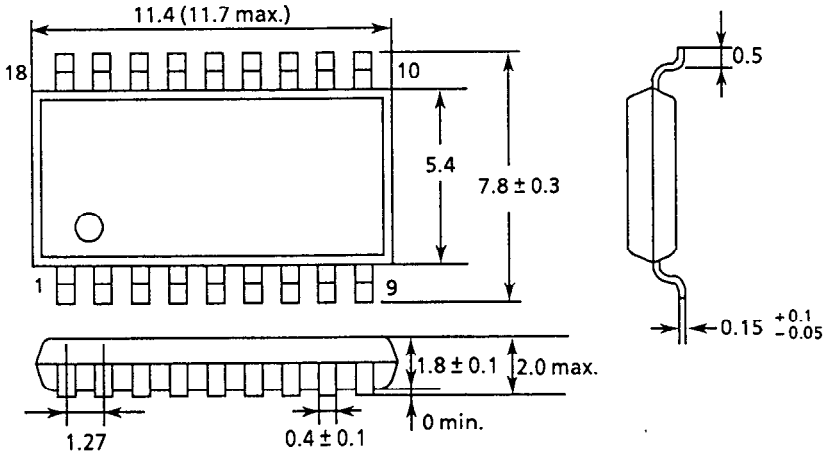



Figure 11

## ■ Ordering Information

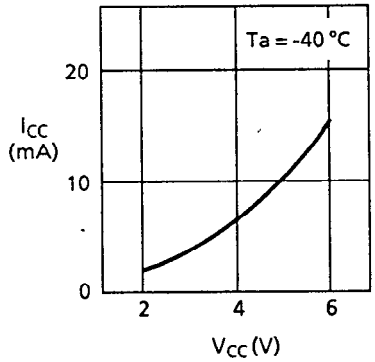
S-22X XX X X XX

| | | |
|---|---|---|
| Rewriting times | 10 | : $10^5$ times |
| Package | Blank: | DIP |
| | F | : SOP |
| Temperature | I | : −40°C to 85°C |
| Memory size | 10 | : 256-bit |
| | 12 | : 1K-bit |
| Input level | H | : All pins TTL compatible |
| | S | : Schmitt input for $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ |

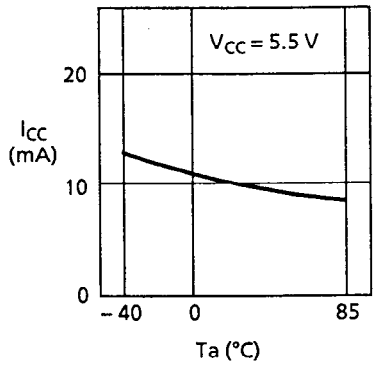
## ■ Characteristics

1. DC Characteristics

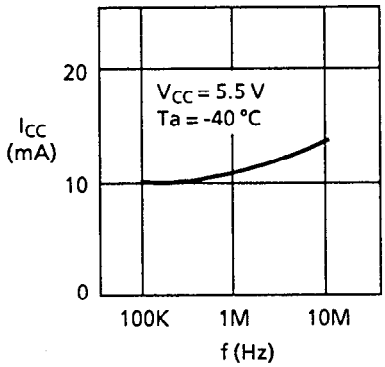
1.1 Operating current consumption $I_{CC}$
— Power supply voltage $V_{CC}$



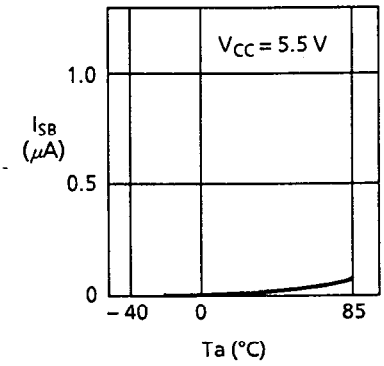

1.2 Operating current consumption $I_{CC}$
— Ambient temperature Ta



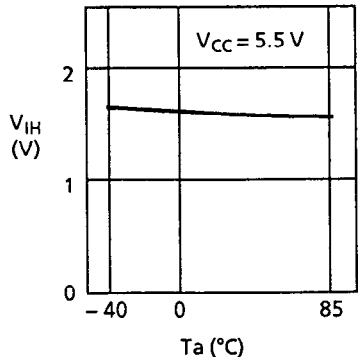

1.3 Operating current consumption $I_{CC}$
— Reading frequency



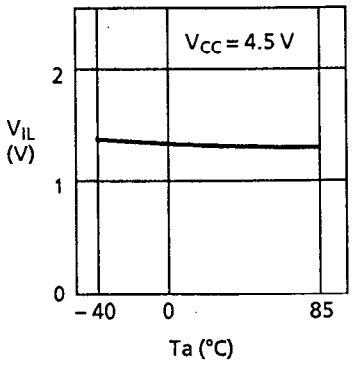

1.4 Standby current consumption $I_{SB}$
— Ambient temperature Ta



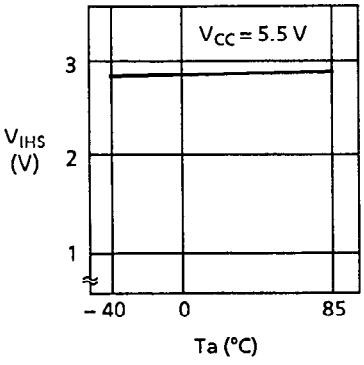

1.5 High level input voltabe $V_{IH}$
—Ambient temperature Ta
S-22H Series : All inputs
S-22S Series : $\overline{CS}$, $\overline{WE}$, I/O and address



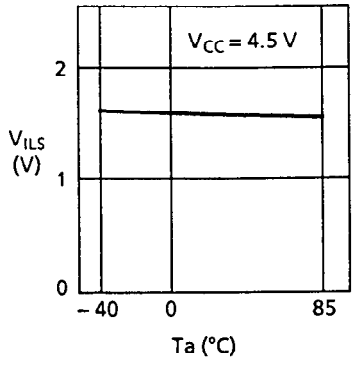

1.6 Low level input voltage $V_{IL}$
—Ambient temperature Ta
S-22H Series : All inputs
S-22S Series : $\overline{CS}$, $\overline{WE}$, I/O and address




1.7 High level input voltabe $V_{IHS}$
—Ambient temperature Ta
S-22S Series : $\overline{STORE}$ and $\overline{RECALL}$

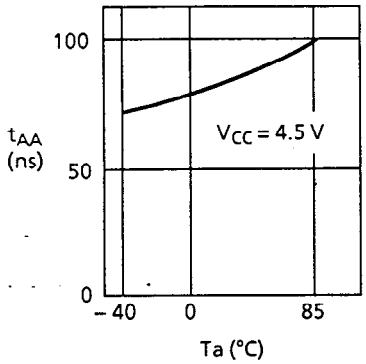



1.8 Low level input voltage $V_{ILS}$
—Ambient temperature Ta
S-22S Series : $\overline{STORE}$ and $\overline{RECALL}$

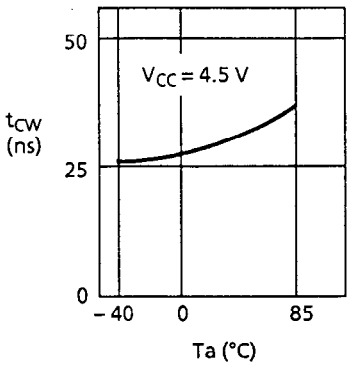


2. AC Characteristics

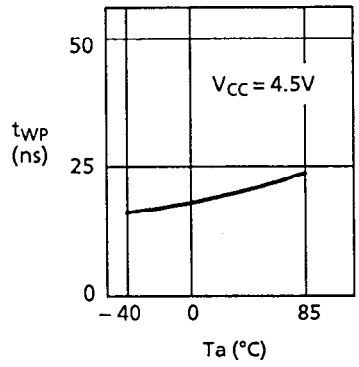
2.1 Address access time $t_{AA}$
—Ambient temperature Ta



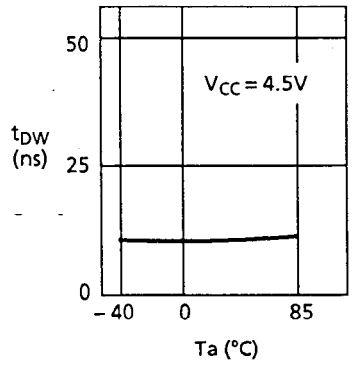

2.2 $\overline{CS}$ pulse width $t_{CW}$
— Ambient temperature Ta



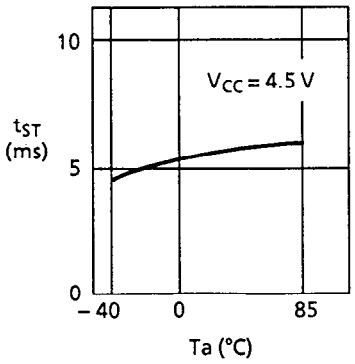

2.3 $\overline{WE}$ pulse width $t_{WP}$
— Ambient temperature Ta



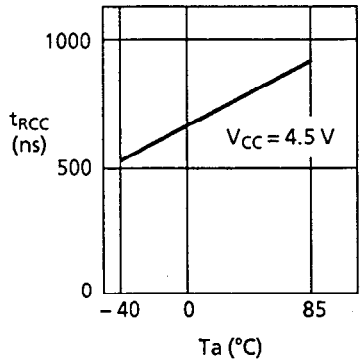

2.4 Input data setup time $t_{DW}$
— Ambient temperature Ta



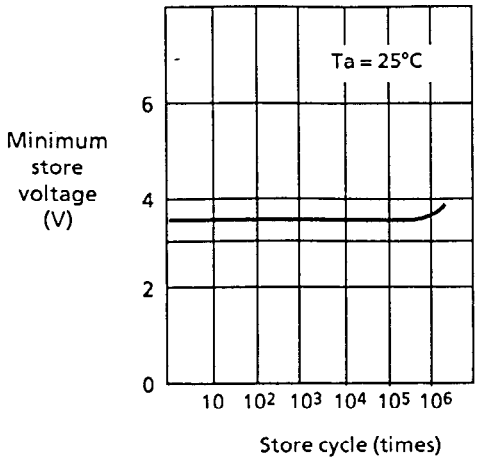

2.5 Store time $t_{ST}$
—Ambient temperature Ta




2.6 Recall cycle time $t_{RCC}$
—Ambient temperature Ta




3. Rewriting Characteristics



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