Contents

CMOS SERIAL E^2PROM

S-29XX1A Series

The S-29XX1A Series is high speed, low power 1K/2K/4K-bit E2PROM with a wide operating voltage range. They are organized as 64-word × 16-bit, 128-word × 16-bit and 256-word × 16-bit, respectively. Each is capable of sequential read, at which time addresses are automatically incremented in 16-bit blocks. The instruction code is compatible with the NM93CSXX Series.
The S-29XX1A Series is capable of protecting the memory, 50% of which can be protected starting from address 00.

■ Features

- Low power consumption
  Standby : 1.0 μA Max. (VCC = 6.5 V)
  Operating : 0.8 mA Max. (VCC = 5.5 V)
  : 0.4 mA Max. (VCC = 2.5 V)
- Wide operating voltage range
  Write : 2.5 to 6.5 V
  Read : 1.8 to 6.5 V
- Memory Protection
- Endurance : 10^5 cycles/word
- Data retention : 10 years
- S-29131A : 1K bits NM93CS46 instruction code compatible
- S-29221A : 2K bits NM93CS56 instruction code compatible
- S-29231A : 2K bits CAT35C102 instruction code compatible
- S-29331A : 4K bits NM93CS66 instruction code compatible

■ Pin Assignment

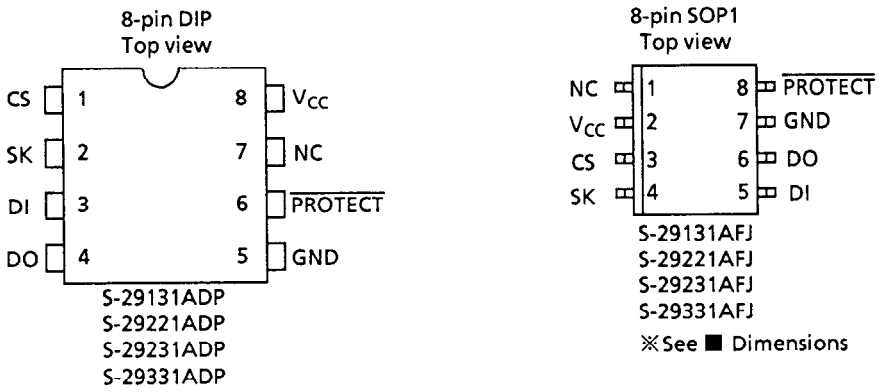


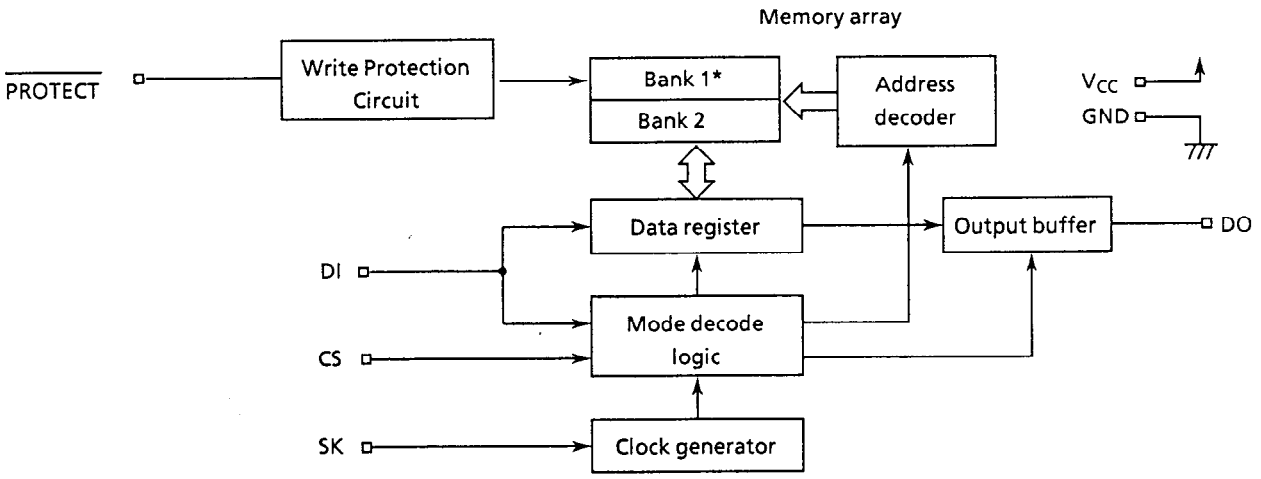
Figure 1

■ Pin Functions

Table 1

Name	Pin Number		Function
	DIP	SOP1	
CS	1	3	Chip select input
SK	2	4	Serial clock input
DI	3	5	Serial data input
DO	4	6	Serial data output
GND	5	7	Ground
$\overline{\text{PROTECT}}$	6	8	Memory Protection Control Input Connected to GND or Open : Protection Valid Connected to Vcc : Protection Invalid
NC	7	1	No Connection
V_{CC}	8	2	Power supply

■ Block Diagram



* 50% of the memory can be protected starting from address 00

Figure 2

■ Instruction Set

Table 2

Instruction	Start Bit	Op code	Address				Data
			S-29131A	S-29231A	S-29221A	S-29331A	
READ (Read data)	1	10	A_5 to A_0	A_6 to A_0	XA_6 to A_0	A_7 to A_0	D_{15} to D_0 Output*
WRITE (Write data)	1	01	A_5 to A_0	A_6 to A_0	XA_6 to A_0	A_7 to A_0	D_{15} to D_0 Input
ERASE (Erase data)	1	11	A_5 to A_0	A_6 to A_0	XA_6 to A_0	A_7 to A_0	—
WRAL (Write all)	1	00	01xxxx	01xxxxx	01xxxxxx	01xxxxxx	D_{15} to D_0 Input
ERAL (Erase all)	1	00	10xxxx	10xxxxx	10xxxxxx	10xxxxxx	—
EWEN (Program enable)	1	00	11xxxx	11xxxxx	11xxxxxx	11xxxxxx	—
EWDS (Program disable)	1	00	00xxxx	00xxxxx	00xxxxxx	00xxxxxx	—

x : Doesn't matter.
* : Addresses are continuously incremented.

■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to +95	°C
Storage temperature	T_{stg}	-65 to +150	°C

■ Recommended Operating Conditions

Table 4

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation Write Enable/Disable	1.8	—	6.5	V
		Write Operation	2.5	—	6.5	V
High level input voltage	V_{IH}	V_{CC} = 5.5 to 6.5 V	0.8 × Vcc	—	Vcc	V
		V_{CC} = 4.5 to 5.5 V	2.0	—	Vcc	V
		V_{CC} = 2.7 to 4.5 V	0.8 × Vcc	—	Vcc	V
		V_{CC} = 1.8 to 2.7 V	0.8 × Vcc	—	Vcc	V
Low level input voltage	V_{IL}	V_{CC} = 5.5 to 6.5 V	0.0	—	0.2 × Vcc	V
		V_{CC} = 4.5 to 5.5 V	0.0	—	0.8	V
		V_{CC} = 2.7 to 4.5 V	0.0	—	0.2 × Vcc	V
		V_{CC} = 1.8 to 2.7 V	0.0	—	0.15 × Vcc	V
Operating temperature	T_{opr}		-40	—	+ 85	°C

■ Pin Capacitance

Table 5

(T_a = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	—	—	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	—	—	10	pF

■ Endurance

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^5	—	—	cycles/word

■ DC Electrical Characteristics

Table 7

Parameter	Smbl	Conditions	V_{CC} = 5.5 V to 6.5 V			V_{CC} = 4.5 V to 5.5 V			V_{CC} = 2.5 to 4.5 V			VCC = 1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	DO unloaded	—	—	1.0	—	—	0.8	—	—	0.6	—	—	0.4	mA
Current consumption (PROGRAM)	I_{CC2}	DO unloaded	—	—	2.5	—	—	2.0	—	—	1.5				mA

Table 8

Parameter	Smbl	Conditions	V_{CC} = 4.5 V to 6.5 V			V_{CC} = 2.5 to 4.5 V			V_{CC} = 1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	CS = GND DO = Open Connected to V_{CC} or GND	—	—	1.0	—	—	0.6	—	—	0.4	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	0.45							V
		I_{OL} = 100 μA	—	—	0.1	—	—	0.1	—	—	0.1	V
High level output voltage	V_{OH}	I_{OH} = -400 μA	2.4	—	—							V
		I_{OH} = -100 μA	V_{CC}-0.7	—	—	V_{CC}-0.7	—	—				V
		I_{OH} = -10 μA	V_{CC}-0.7	—	—	V_{CC}-0.7	—	—	V_{CC}-0.3	—	—	V
Write enable latch data hold voltage	V_{DH}	Only when write disable mode	1.5	—	—	1.5	—	—	1.5	—	—	V
Pull-Down Current	I_{PD}	$\overline{\text{PROTECT}}$ Terminal = V_{CC}	15	—	100	3	—	50	1	—	10	μA

■ AC Electrical Characteristics

Table 9

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100pF

Table 10

Parameter	Smbl	V_{CC} = 4.5 to 6.5V			V_{CC} = 2.5 to 4.5 V			V_{CC} = 1.8 to 2.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS setup time	t_{CSS}	0.2	—	—	0.4	—	—	1.0	—	—	μs
CS hold time	t_{CSH}	0.2	—	—	0.4	—	—	1.0	—	—	μs
CS deselect time	t_{CDS}	0.2	—	—	0.2	—	—	0.4	—	—	μs
Data setup time	t_{DS}	0.2	—	—	0.4	—	—	0.8	—	—	μs
Data hold time	t_{DH}	0.2	—	—	0.4	—	—	0.8	—	—	μs
Output delay	t_{PD}	—	—	0.4	—	—	1.0	—	—	2.0	μs
Clock frequency	f_{SK}	0	—	2.0	0	—	0.5	—	—	0.25	MHz
Clock pulse width	t_{SKH}, t_{SKL}	0.25	—	—	1.0	—	—	2.0	—	—	μs
Output disable time	t_{HZ1}, t_{HZ2}	0	—	0.15	0	—	0.5	0	—	1.0	μs
Output enable time	t_{SV}	0	—	0.15	0	—	0.5	0	—	1.0	μs
Programming time	t_{PR}	—	4.0	10.0	—	4.0	10.0				ms

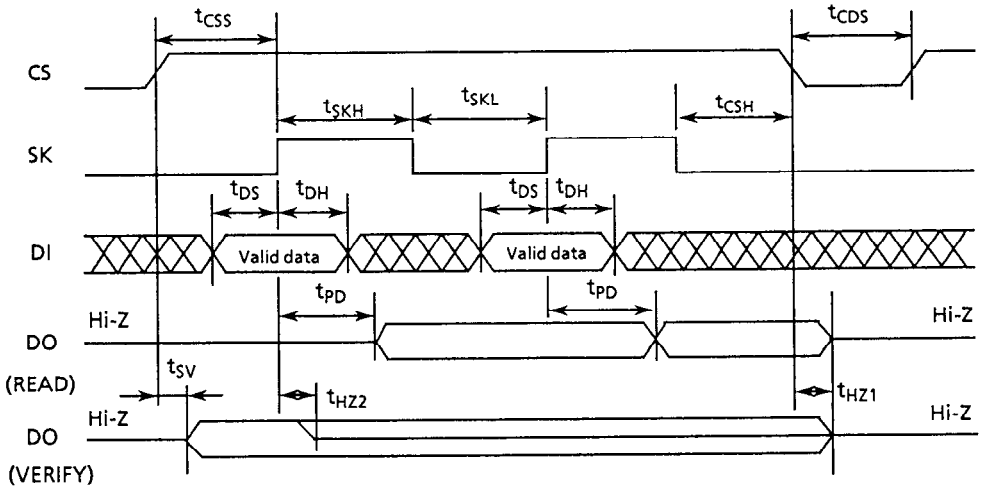


Figure 3 Timing Chart

■ Operation

Instructions (in the order of start-bit, instruction, address, and data) are latched to DI in synchronization with the rising edge of SK after CS goes high. A start-bit can only be recognized when the high of DI is latched to the rising edge of SK when CS goes from low to high, it is impossible for it to be recognized as long as DI is low, even if there are SK pulses after CS goes high. Any SK pulses input while DI is low are called "dummy clocks." Dummy clocks can be used to adjust the number of clock cycles needed by the serial IC to match those sent out by the CPU. Instruction input finishes when CS goes low, where it must be between commands during t_{CDS}.

All input, including DI and SK signals, is ignored while CS is low, which is stand-by mode.

1. Read

The READ instruction reads data from a specified address. After A0 is latched at the rising edge of SK, DO output changes from a high-impedance state (Hi-Z) to low level output. Data is continuously output in synchronization with the rise of SK.

When all of the data (D0) in the specified address has been read, the data in the next address can be read with the input of another SK clock. Thus, it is possible for all of the data addresses to be read through the continuous input of SK clocks as long as CS is high.

The last address (An ··· A1 A0 = 1 ··· 11) rolls over to the top address (An ··· A0 = 0 ··· 00).

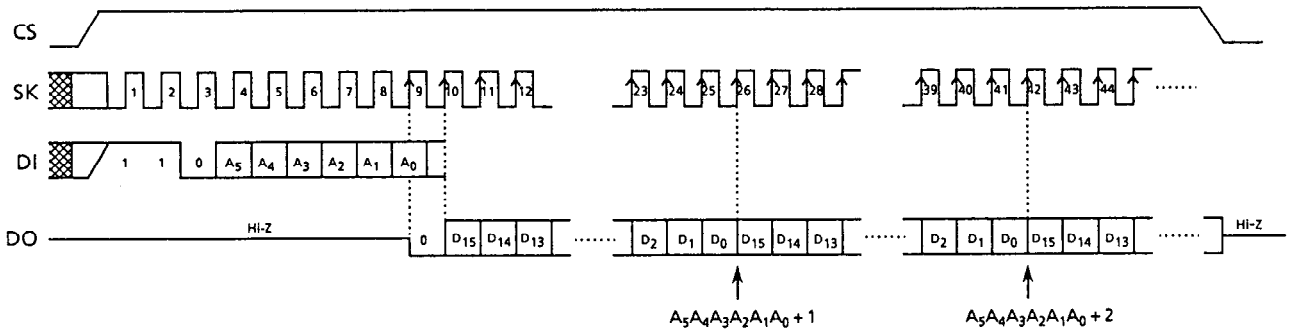


Figure 4 Read Timing (S-29131A)

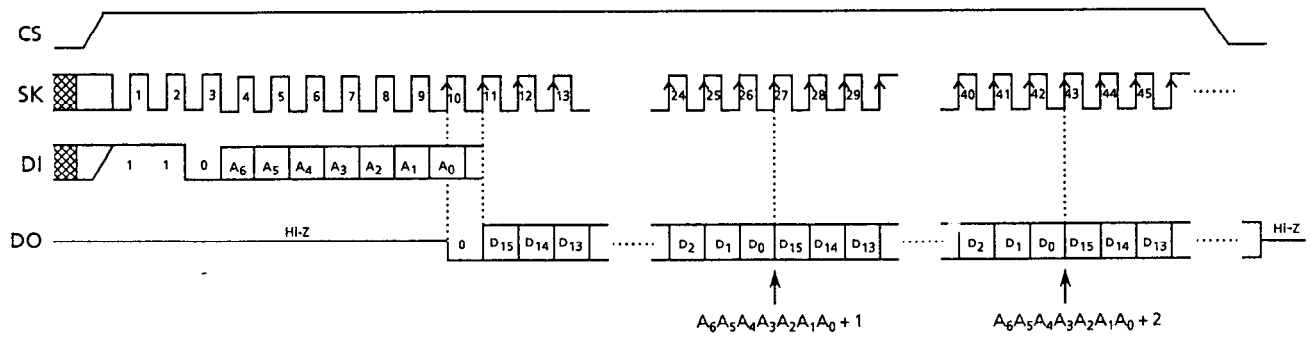


Figure 5 Read Timing (S-29231A)

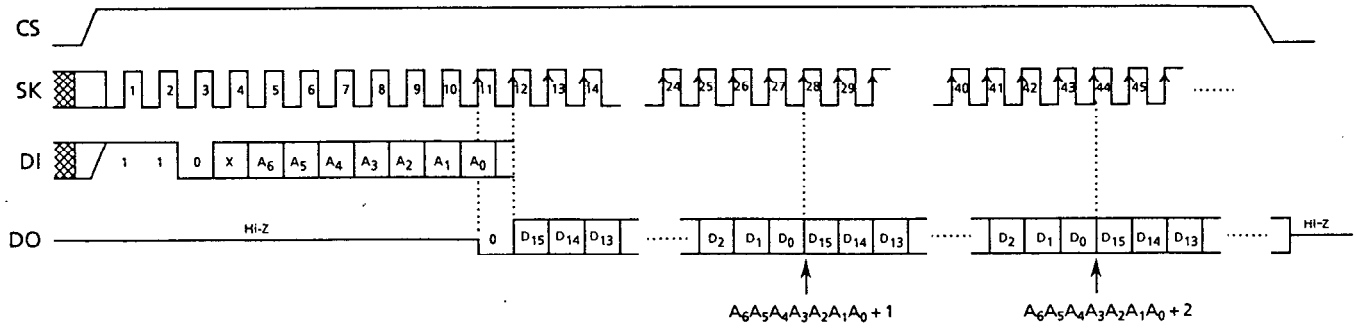


Figure 6 Read Timing (S-29221A)

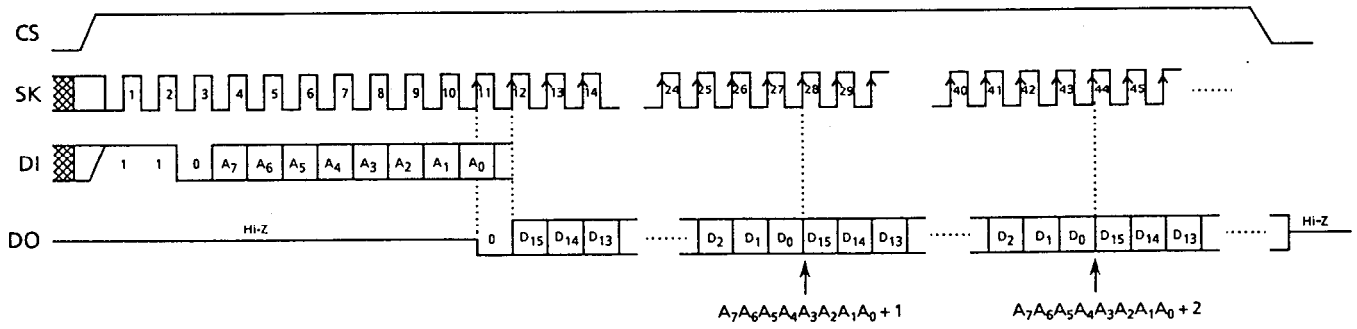


Figure 7 Read Timing (S-29331A)

2. WRITE (WRITE, ERASE, WRAL, ERAL)

There are four write instructions, WRITE, ERASE, WRAL, and ERAL. Each automatically begins writing to the non-volatile memory when CS goes low at the completion of the specified clock input.

The write operation is completed in 10 ms (t_{PR} Max.), and the typical write period is less than 5 ms. In the S-29XX1A Series, it is easy to VERIFY the completion of the write operation in order to minimize the write cycle by setting CS to high and checking the DO pin, which is low during the write operation and high after its completion. This VERIFY procedure can be executed over and over again.

Because all SK and DI inputs are ignored during the write operation, any input of instruction will also be disregarded. When DO outputs high after completion of the write operation or if it is in the high-impedence state (Hi-Z), the input of instructions is available. Even if the DO pin remains high, it will enter the high-impedence state upon the recognition of a high of DI (start-bit) attached to the rising edge of an SK pulse. (see Figure 3).

DI input should be low during the VERIFY procedure.

2.1 WRITE

This instruction writes 16-bit data to a specified address.
After changing CS to high, input a start-bit, op-code (WRITE), address, and 16-bit data. If there is a data overflow of more than 16 bits, only the last 16-bits of the data is considered valid. Changing CS to low will start the WRITE operation. It is not necessary to make the data "1" before initiating the WRITE operation.

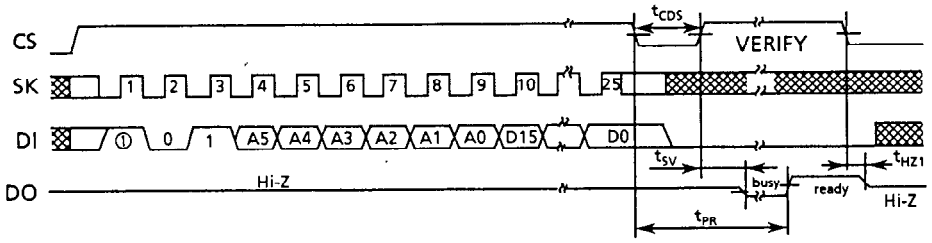


Figure 8 WRITE Timing (S-29131A)

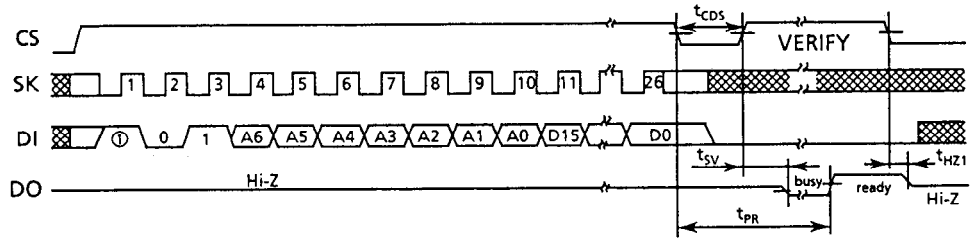


Figure 9 WRITE Timing (S-29231A)

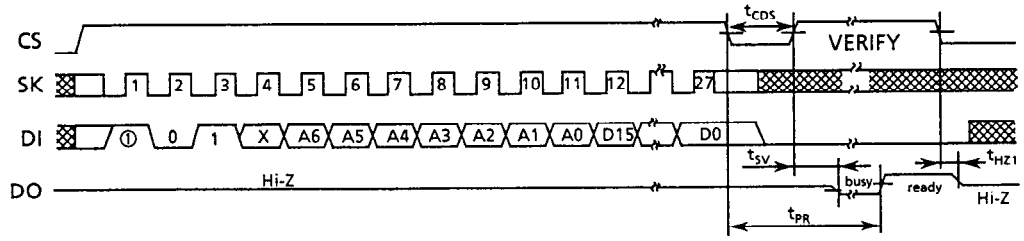


Figure 10 WRITE Timing (S-29221A)

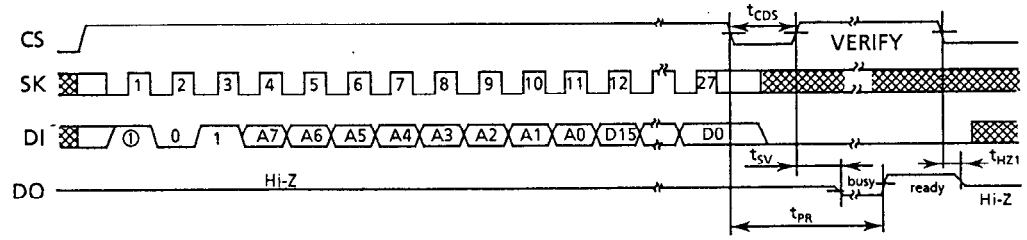


Figure 11 WRITE Timing (S-29331A)

2.2 ERASE

This command erases 16-bit data in a specified address.
After changing CS to high, input a start-bit, op-code (ERASE), and address. It is not necessary to input data.
Changing CS to low will start the ERASE operation, which changes every bit of the 16 bit data to "1."

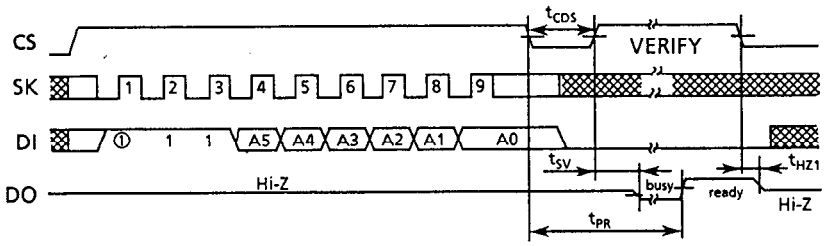


Figure 12 ERASE Timing (S-29131A)

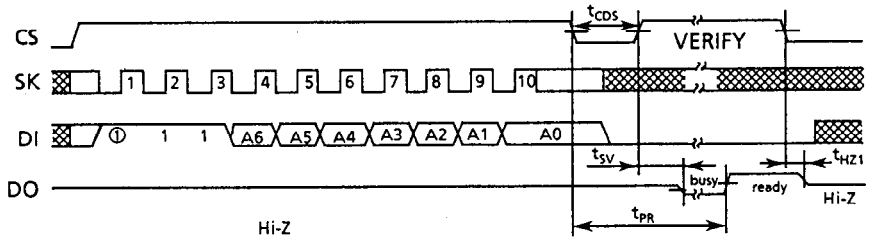


Figure 13 ERASE Timing (S-29231A)

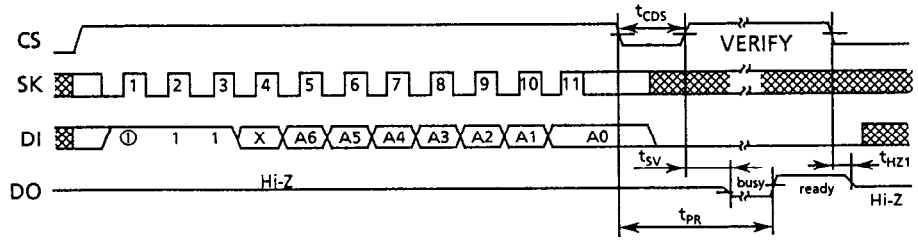


Figure 14 ERASE Timing (S-29221A)

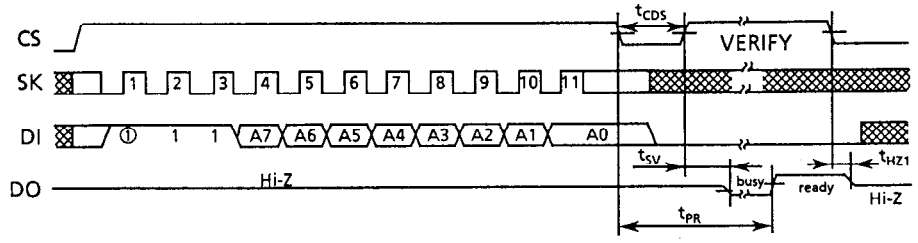


Figure 15 ERASE Timing (S-29331A)

2.3 WRAL

This instruction writes the same 16-bit data into every address.

After changing CS to high, input a start-bit, op-code (WRAL), address (optional), and 16-bit data. If there is a data overflow of more than 16 bits, only the last 16-bits of the data is considered valid. Changing CS to low will start the WRAL operation. It is not necessary to make the data "1" before initiating the WRAL operation.

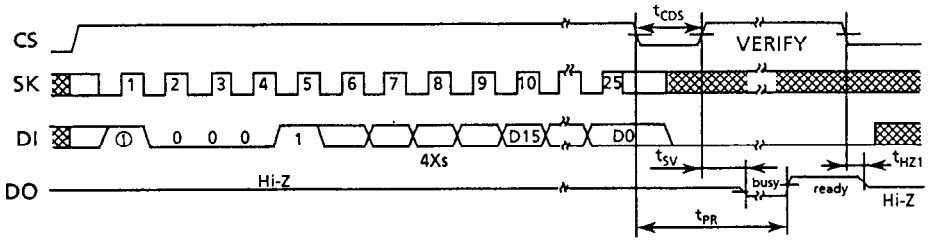


Figure 16 WRAL Timing (S-29131A)

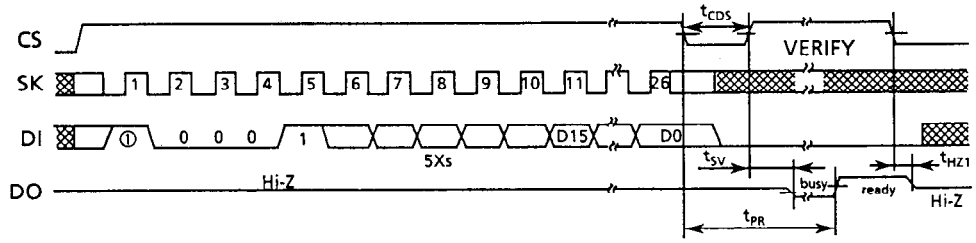


Figure 17 WRAL Timing (S-29231A)

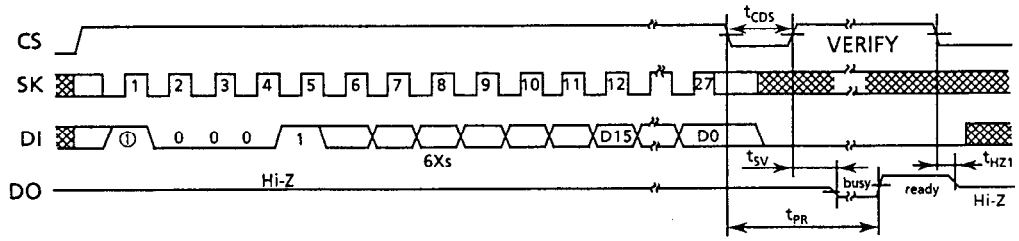


Figure 18 WRAL Timing (S-29221A)

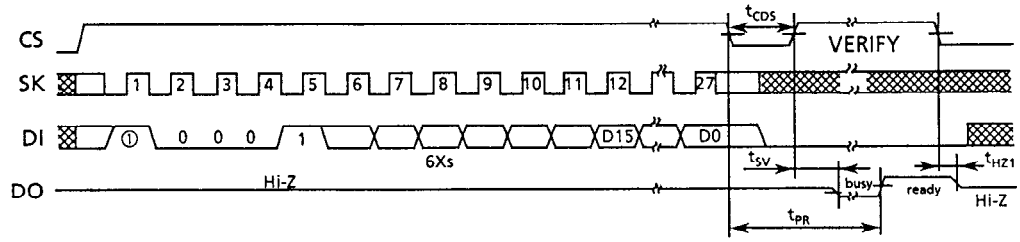


Figure 19 WRAL Timing (S-29331A)

2.4 ERAL

This instruction erases the data in every address.
After changing CS to high, input a start-bit, op-code (ERAL), and address (optional). It is not necessary to input data. Changing CS to low will start the ERAL operation, which changes every bit of data to "1."

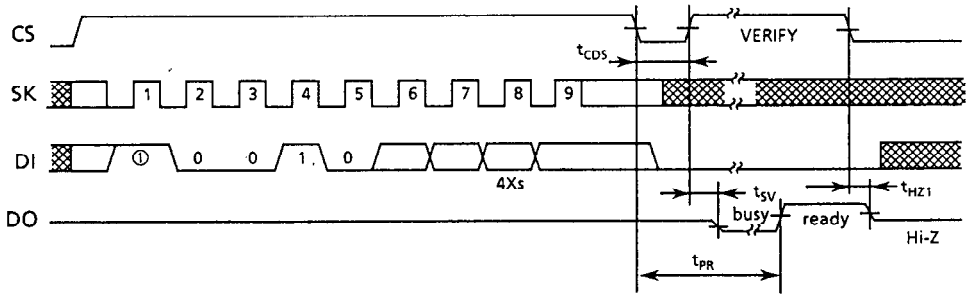


Figure 20 ERAL Timing (S-29131A)

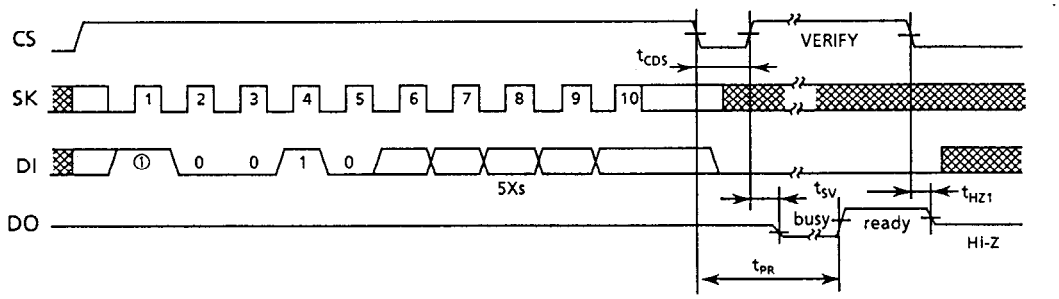


Figure 21 ERAL Timing (S-29231A)

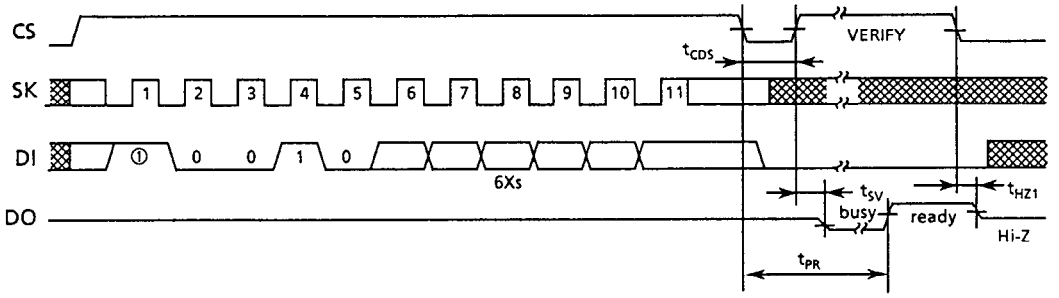


Figure 22 ERAL Timing (S-29221A)

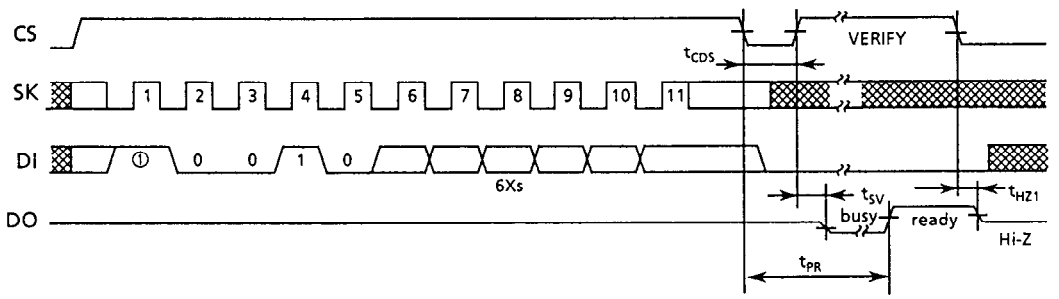


Figure 23 ERAL Timing (S-29331A)

3. Write enable (EWEN) and Write disable (EWDS)

The EWEN instruction puts the S-29XX1A Series into write enable mode, which accepts WRITE, ERASE, WRAL, and ERAL instructions. The EWDS instruction puts the S-29XX1A Series into write disable mode, which refuses WRITE, ERASE, WRAL, and ERAL instructions.

The S-29XX1A Series powers on in write disable mode, which protects data against unexpected, erroneous write operations caused by noise and/or CPU malfunctions. It should be kept in write disable mode except when performing write operations.

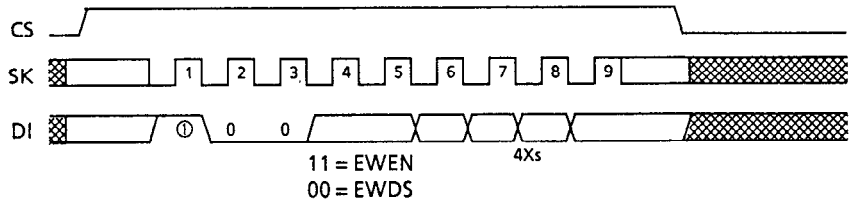


Figure 24 EWEN/EWDS Timing (S-29131A)

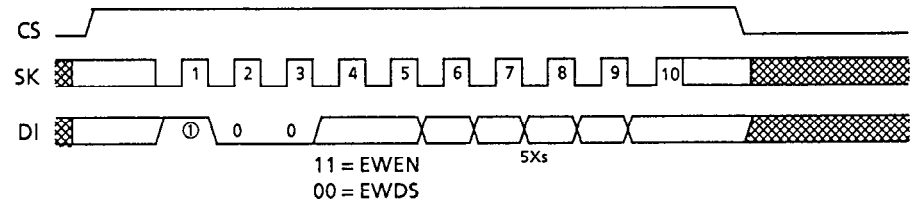


Figure 25 EWEN/EWDS Timing (S-29231A)

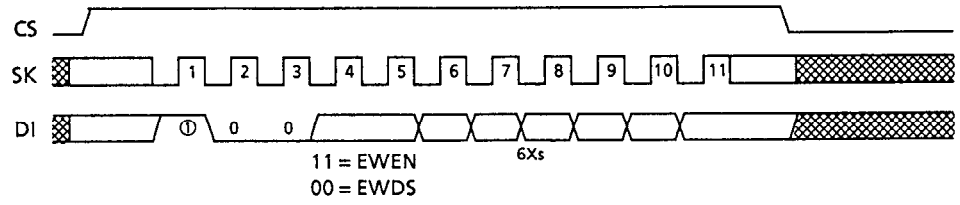


Figure 26 EWEN/EWDS Timing (S-29221A)

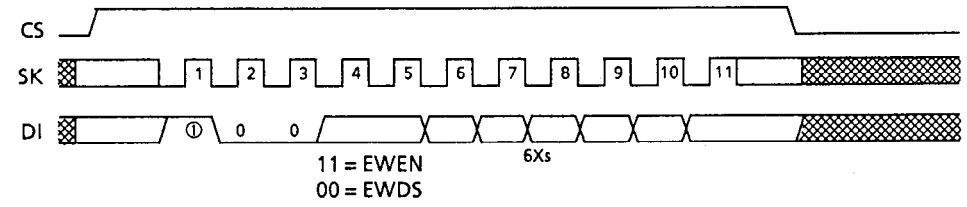


Figure 27 EWEN/EWDS Timing (S-29331A)

■ Receiving a Start-Bit

Both the recognition of a start-bit and the VERIFY procedure occur when CS is "high." Therefore, only after a write operation, in order to accept the next command by having CS go high, will the DO pin switch from a state of high-impedence to a state of data output; but if it recognizes a start-bit, the DO pin returns to a state of high-impedence.

■ Three-wire Interface (DI-DO direct connection)

Although the normal configuration of a serial interface is a 4-wire interface to CS, SK, DI, and DO, a 3-wire interface is also a possibility by connecting DI and DO. However, since there is a possibility that the DO output from the serial memory IC will interfere with the data output from the CPU with a 3-wire interface, install a resistor between DI and DO in order to give preference to data output from the CPU to DI(See Figure 28).

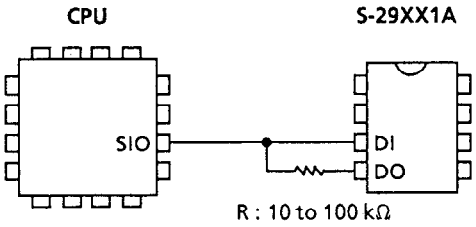


Figure 28

■ Memory Protection

The S-29XX1A Series is capable of protecting the memory. So, the contents of the memory will not be miswritten due to error run or malfunction of the CPU. When the $\overline{\text{PROTECT}}$ terminal is connected to GND or OPEN, write to Bank 1 in the memory array is prohibited (50% of the memory can be protected starting from address 00). Because the pull-down resistance is connected to the $\overline{\text{PROTECT}}$ terminal internally, the memory can be automatically protected when the $\overline{\text{PROTECT}}$ terminal is OPEN. When the protection is valid, the data in the memory of Bank 1 will not be rewritten. However, because the write control circuit inside the IC functions, the next instruction cannot be executed during the time period of writing (t_{PR}). While write instruction is being input and write is being executed, always connect the $\overline{\text{PROTECT}}$ terminal to "H," "L" or OPEN, and leave the input signal unchanged (see Figure 29).

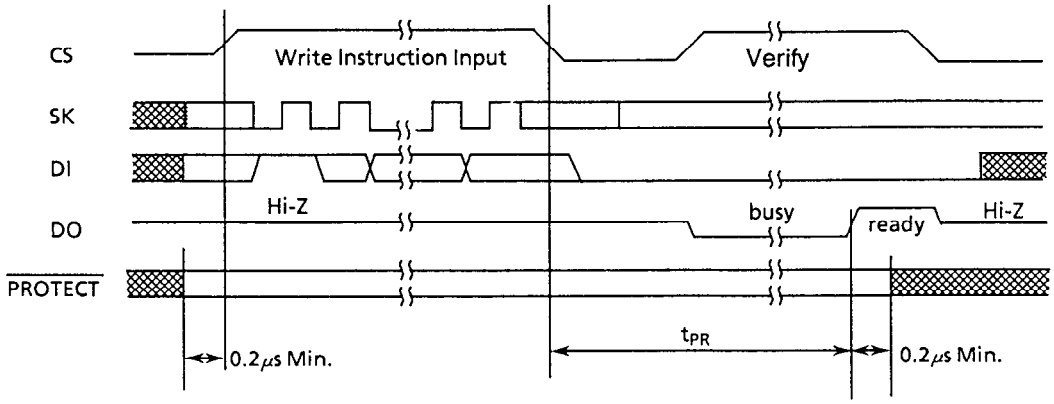


Figure 29 PROTECT Terminal Input Signal Timing

■ Dimensions (Unit : mm)

1. 8-pin DIP

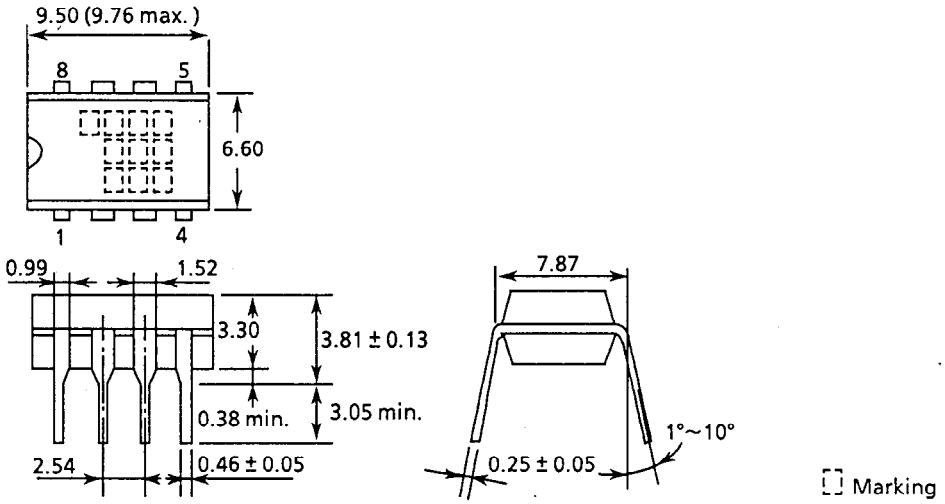


Figure 30

2. 8-pin SOP

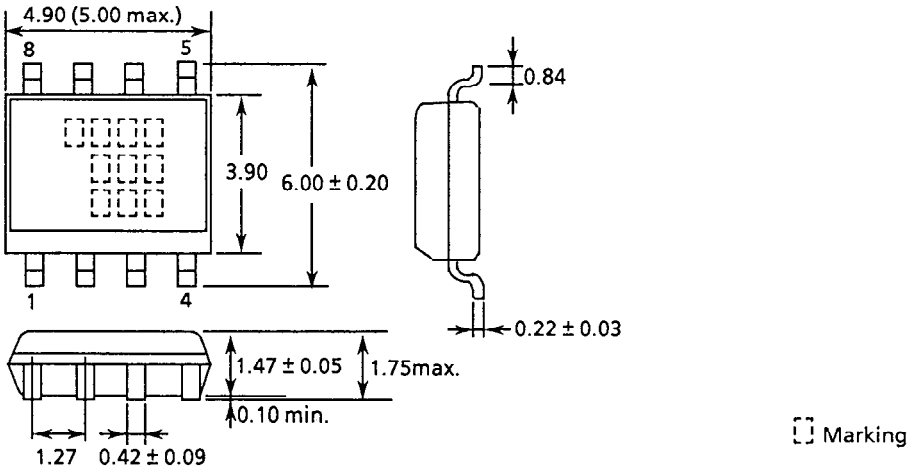


Figure 31

■ Ordering Information

S-29XX1A XXX

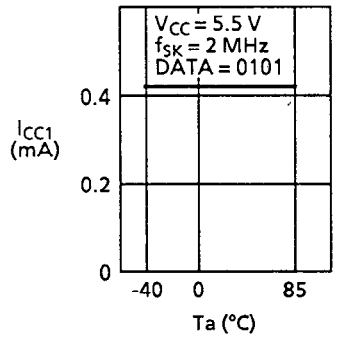
Package DP : DIP
FJ : SOP1

Product name S-29131A : 1K-bit
S-29221A : 2K-bit
S-29231A : 2K-bit
S-29331A : 4K-bit

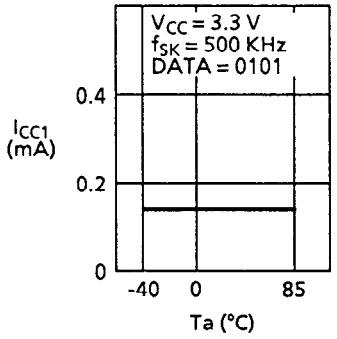
■ Characteristics

1. DC Characteristics

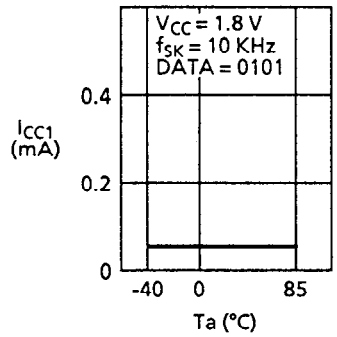
1.1 Current consumption (READ) I_{CC1} — Ambient temperature Ta



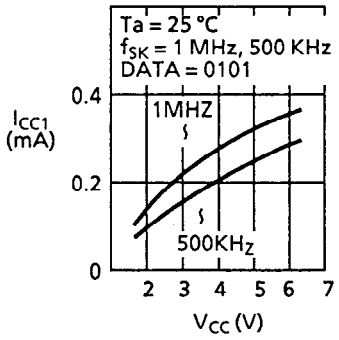
1.2 Current consumption (READ) I_{CC1} — Ambient temperature Ta



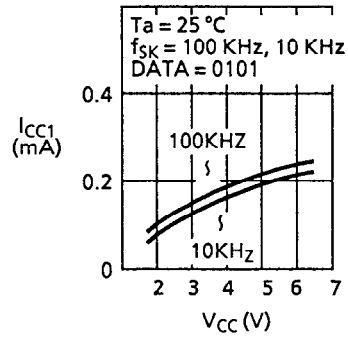
1.3 Current consumption (READ) I_{CC1} — Ambient temperature Ta



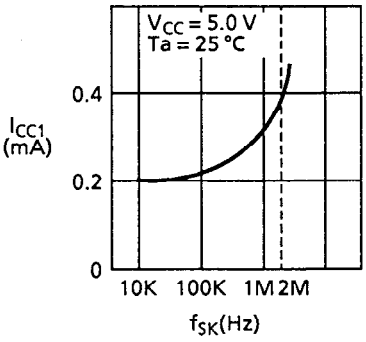
1.4 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



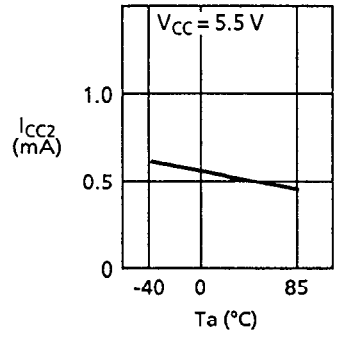
1.5 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



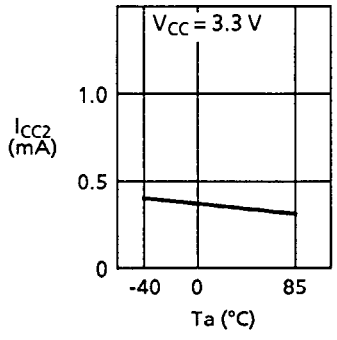
1.6 Current consumption (READ) I_{CC1} — Clock frequency f_{SK}



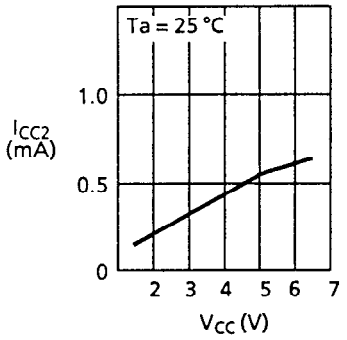
1.7 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



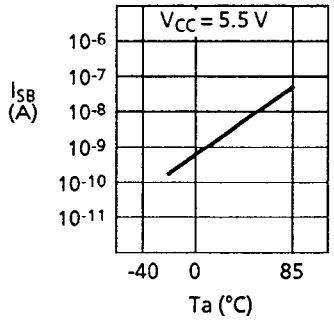
1.8 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



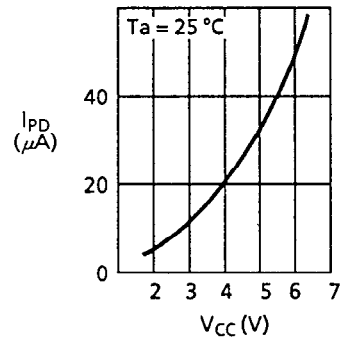
1.9 Current consumption (PROGRAM) I_{CC2} – Power supply voltage V_{CC}



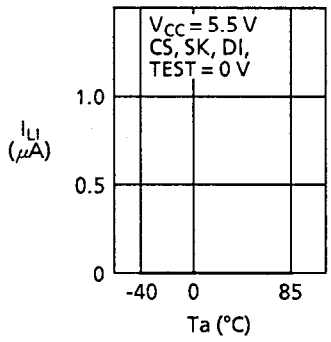
1.10 Standby current consumption I_{SB} — Ambient temperature Ta



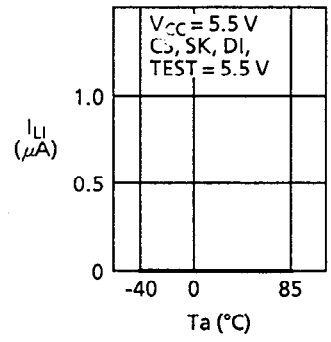
1.11 Pull-Down current I_{PD} — Power supply voltageV_{CC}



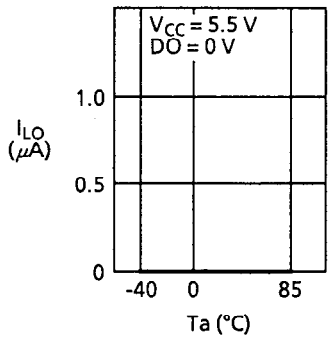
1.12 Input leakage current I_{LI} – Ambient temperature Ta



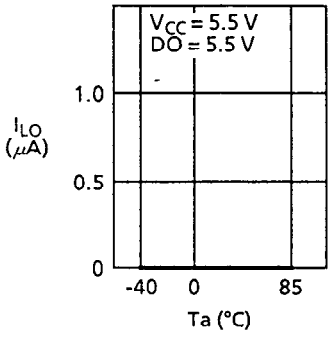
1.13 Input leakage current I_{LI} – Ambient temperature Ta



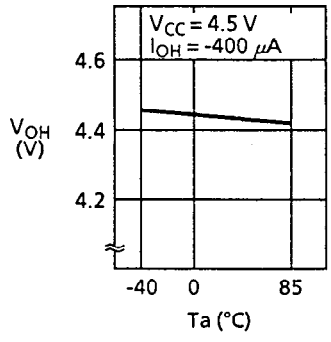
1.14 Output leakage current I_{LO} – Ambient temperature Ta



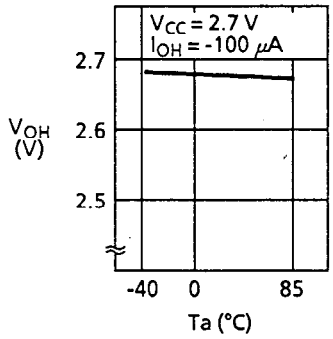
1.15 Output leakage current I_{LO} – Ambient temperature Ta



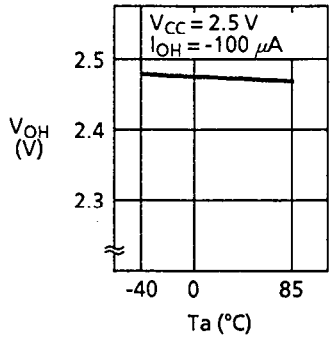
1.16 High level output voltage V_{OH} – Ambient temperature Ta



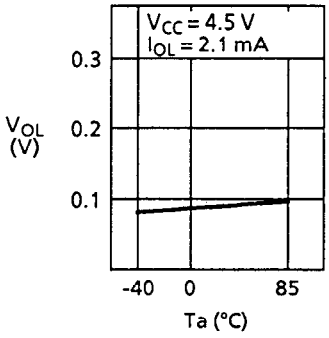
1.17 High level output voltage V_{OH} – Ambient temperature Ta



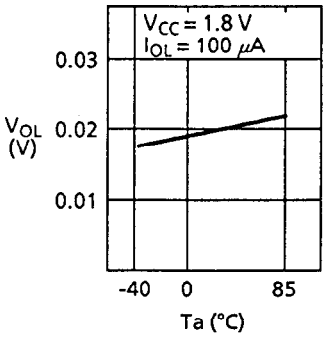
1.18 High level output voltage V_{OH} – Ambient temperature Ta



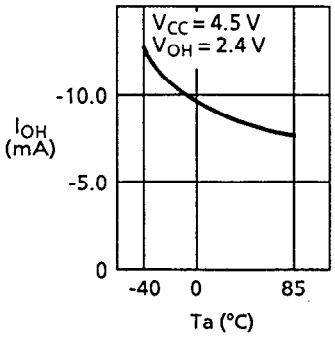
1.19 Low level output voltage V_{OL} – Ambient temperature Ta



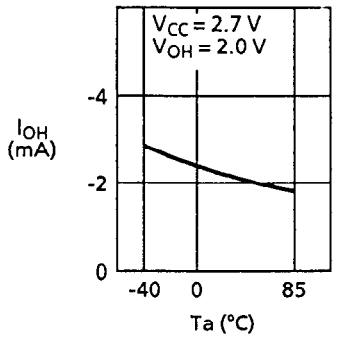
1.20 Low level output voltage V_{OL} – Ambient temperature Ta



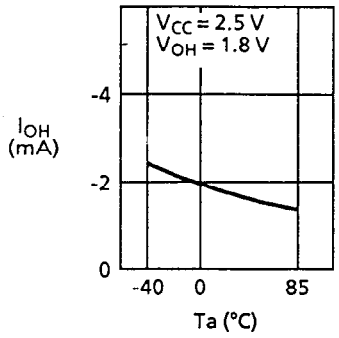
1.21 High level output current I_{OH} – Ambient temperature Ta



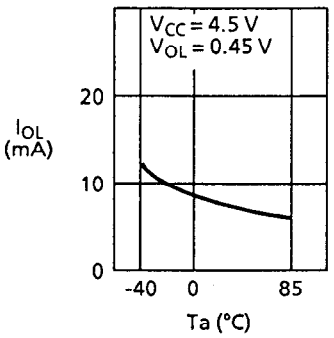
1.22 High level output current I_{OH} – Ambient temperature Ta



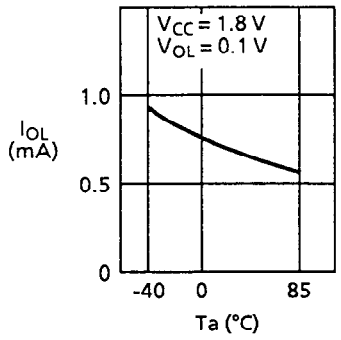
1.23 High level output current I_{OH} – Ambient temperature Ta



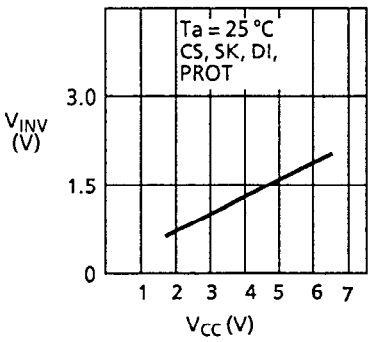
1.24 Low level output current I_{OL} – Ambient temperature Ta



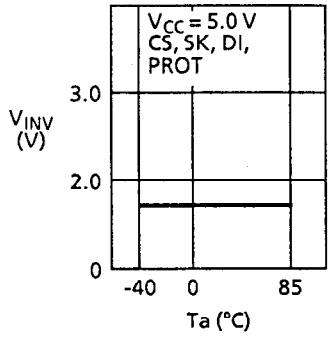
1.25 Low level output current I_{OL} – Ambient temperature Ta



1.26 Input voltage V_{IN} (V_{IL}, V_{IH}) – Power supply voltage V_{CC}

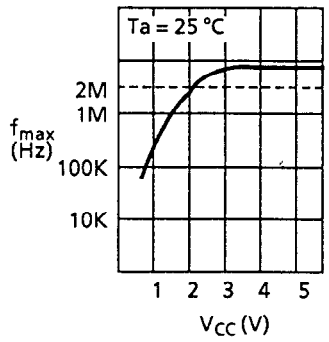


1.27 Input voltage V_{IN} (V_{IL}, V_{IH}) – Ambient temperature Ta

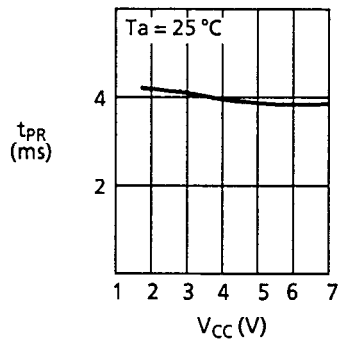


2. AC Characteristics

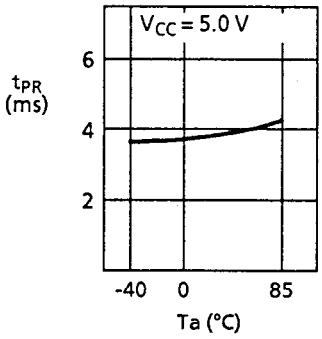
2.1 Maximum operating frequency fmax – Power supply voltage V_{CC}



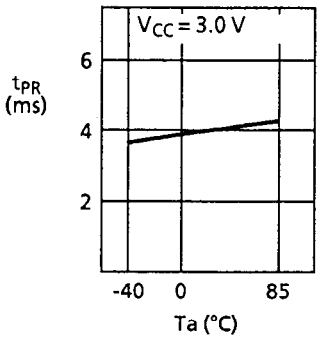
2.2 Program time t_{PR} – Power supply voltage V_{CC}



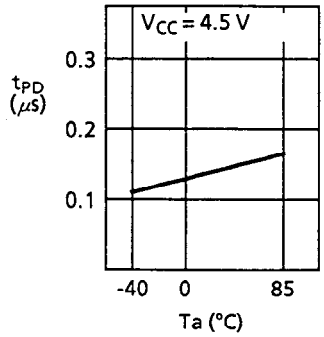
2.3 Program time t_{PR} – Ambient temperature Ta



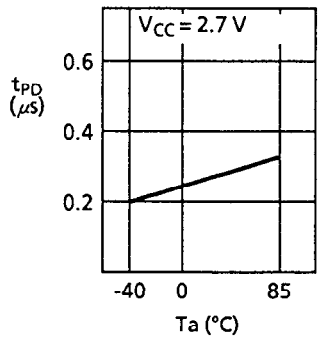
2.4 Program time t_{PR} – Ambient temperature Ta



2.5 Data output delay time t_{PD} – Ambient temperature Ta



2.6 Data output delay time t_{PD} – Ambient temperature Ta



2.7 Data output delay time t_{PD} – Ambient temperature Ta