2-WIRE CMOS SERIAL E^{2}PROM FOR DIMM SERIAL PRESENCE DETECT

S-34C02A

S-34C02A is a 2-wired serial E^{2}PROM for DIMM Serial Presence Detect which operates with low current consumption and the wide range operation. The S-34C02A has the capacity of 2K-bit and the organization of 256 words × 8-bit, is able to Page Write and Sequential Read.
S-34C02A has Hardware Protect and Software Protect. Hardware Protect inhibits Write to all memory area by connecting the WP pin to V_{CC}. Software Protect inhibits Write in 50% of the lower address (the address 00h to 7Fh) in all memory area by inputting command when the WP pin is connected to GND or left open.

■ Features

- Operating voltage range — Read: 1.6 to 5.5 V; Write: 1.7 to 5.5 V
- Page write: 16 bytes / page
- Sequential read
- Operation frequency: 400 kHz (V_{CC} = 2.5 to 5.5 V)
- Noise filtering: Schmitt trigger and noise filter on bus input pins (SCL, SDA)
- Write protect function during low power supply
- Endurance: 10^6 cycles / word*1 (at +25°C)
  ***1.** For each address (Word: 8 bits)
- Data retention: 100 years (at +25°C)
- Memory size: 2K-bit
- Write Protect: Hardware Protect 100% (addresses 00h to FFh)
  Software Protect for the lower address of 50% (addresses 00h to 7Fh)
- Lead-free product

■ Package

Package name	Drawing code		
	Package	Tape	Reel
8-Pin TSSOP	FT008-A	FT008-E	FT008-E

Caution This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to SII is indispensable.

■ Pin Configuration

8-Pin TSSOP
Top view

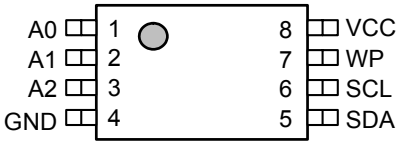


Figure 1

S-34C02A0I-T8T1G

Table 1

Pin No.	Symbol	Description
1	A0	Address input
2	A1	Address input
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

Remark See Dimensions for details of the package drawings.

■ Block Diagram

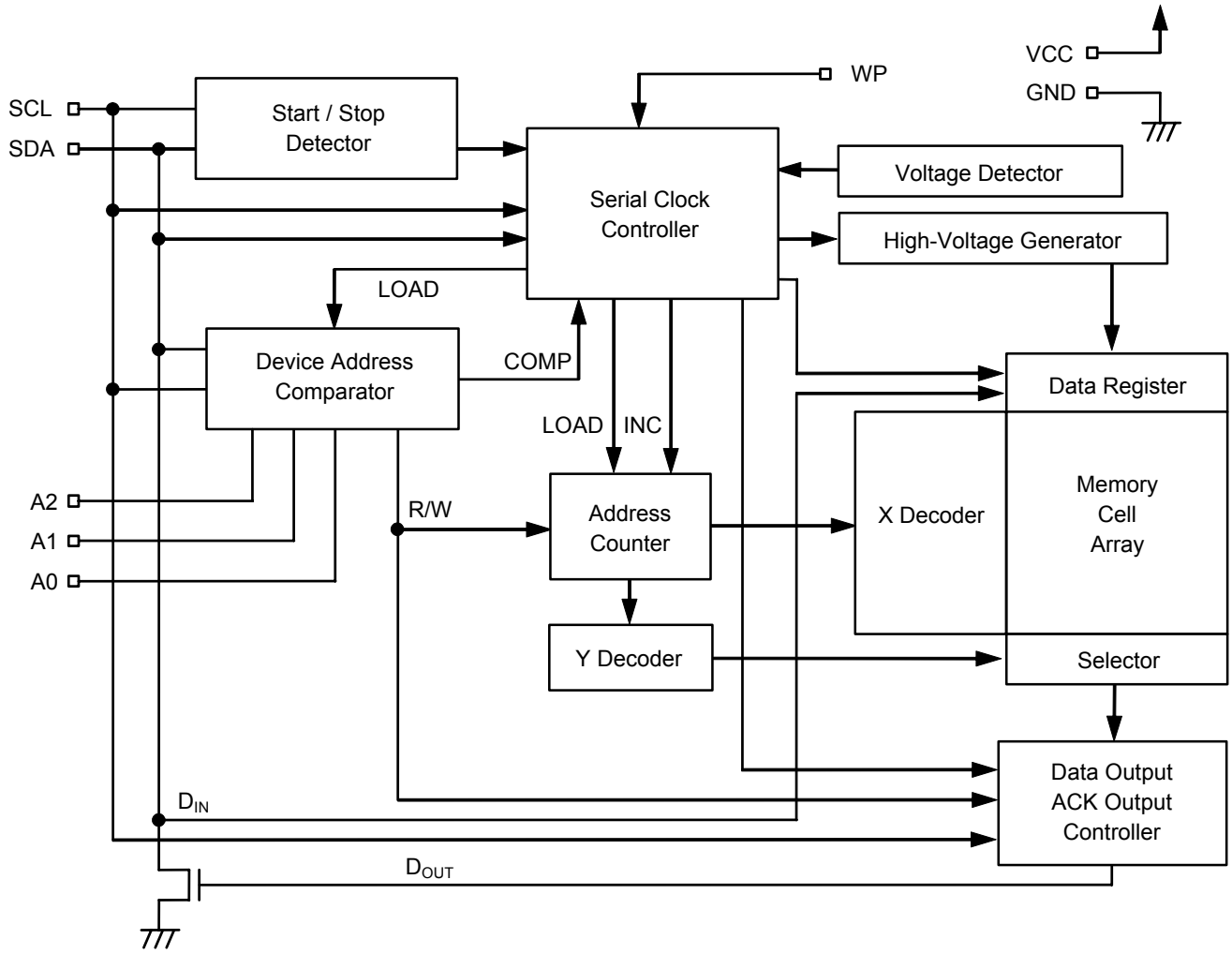


Figure 2

■ Absolute Maximum Ratings

Table 2

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to +7.0	V
A0 High level Input voltage	V_{HV}	−0.3 to +10.0	V
Output voltage	V_{OUT}	−0.3 to V_{CC}+0.3	V
Operation ambient temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 3

Item	Symbol	Condition	Min.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation	1.6	5.5	V
		Write Operation	1.7	5.5	V
High level input voltage	V_{IH}	V_{CC} = 1.6 to 5.5 V	0.7 × V_{CC}	V_{CC}	V
Low level input voltage	V_{IL}	V_{CC} = 1.6 to 5.5 V	0.0	0.3 × V_{CC}	V
A0 High level input voltage	V_{HV}	V_{HV} − V_{CC} > 4.8 V	7.0	10.0	V

■ Pin Capacitance

Table 4

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V (SCL, A0, A1, A2, WP)	−	10	pF
Input / output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V (SDA)	−	10	pF

■ Endurance

Table 5

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	+25°C	10^6	−	cycles / word*1

***1.** For each address (Word: 8 bits)

■ Data Retention

Table 6

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data retention	−	+25°C	100	−	year

■ DC Electrical Characteristics

Table 7

Item	Symbol	Condition	V_{CC} = 2.5 to 5.5 V f = 400 kHz		V_{CC} = 1.6 to 2.5 V f = 100 kHz		V_{CC} = 1.7 to 2.5 V f = 100 kHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	–	–	0.8	–	0.2	–	0.2	mA
Current consumption (WRITE)	I_{CC2}	–	–	4.0	–	–	–	1.5	mA

Table 8

Item	Symbol	Condition	V_{CC} = 2.5 to 5.5 V		V_{CC} = 1.6 to 2.5 V		Unit
			Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	V_{IN} = V_{CC} or GND	–	1.5	–	1.5	μA
Input leakage current	I_{LI}	SCL, SDA V_{IN} = GND to V_{CC}	–	1.0	–	1.0	μA
Output leakage current	I_{LO}	SDA V_{OUT} = GND to V_{CC}	–	1.0	–	1.0	μA
Input current 1	I_{IL}	A0, A1, A2, WP $V_{IN} < 0.3 \times V_{CC}$	–	50.0	–	50.0	μA
Input current 2	I_{IH}	A0, A1, A2, WP $V_{IN} > 0.7 \times V_{CC}$	–	2.0	–	2.0	μA
Input Impedance 1	Z_{IL}	A0, A1, A2, WP $V_{IN} = 0.3 \times V_{CC}$	30	–	30	–	KΩ
Input Impedance 2	Z_{IH}	A0, A1, A2, WP $V_{IN} = 0.7 \times V_{CC}$	800	–	800	–	KΩ
Low level output voltage	V_{OL}	I_{OL} = 3.2 mA	–	0.4	–	0.4	V
Current address hold voltage	V_{AH}	–	1.5	5.5	1.5	2.5	V

■ AC Electrical Characteristics

Table 9 Measurement Conditions

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Input pulse rising / falling time	20 ns
Output determination voltage	$0.5 \times V_{CC}$
Output load	100 pF+Pull-up resistor 1.0 kΩ

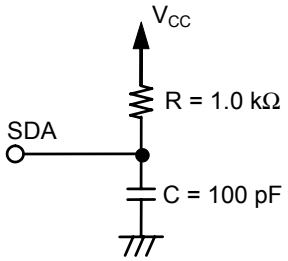


Figure 3 Output Load Circuit

Table 10

Item	Symbol	V_{CC} = 2.5 to 5.5 V		V_{CC} = 1.6 to 2.5 V		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	400	0	100	kHz
SCL clock time "L"	t_{LOW}	1.3	–	4.7	–	µs
SCL clock time "H"	t_{HIGH}	0.6	–	4.0	–	µs
SDA output delay time	t_{AA}	0.1	0.9	0.1	3.5	µs
SDA output hold time	t_{DH}	50	–	100	–	ns
Start condition setup time	$t_{SU.STA}$	0.6	–	4.7	–	µs
Start condition hold time	$t_{HD.STA}$	0.6	–	4.0	–	µs
Data input setup time	$t_{SU.DAT}$	100	–	200	–	ns
Data input hold time	$t_{HD.DAT}$	0	–	0	–	ns
Stop condition setup time	$t_{SU.STO}$	0.6	–	4.0	–	µs
SCL • SDA rising time	t_R	–	0.3	–	1.0	µs
SCL • SDA falling time	t_F	–	0.3	–	0.3	µs
WP setup time	t_{WS1}	0	–	0	–	µs
WP hold time	t_{WH1}	0	–	0	–	µs
WP release setup time	t_{WS2}	0	–	0	–	µs
WP release hold time	t_{WH2}	0	–	0	–	µs
Bus release time	t_{BUF}	1.3	–	4.7	–	µs
Noise suppression time	t_I	–	50	–	100	ns

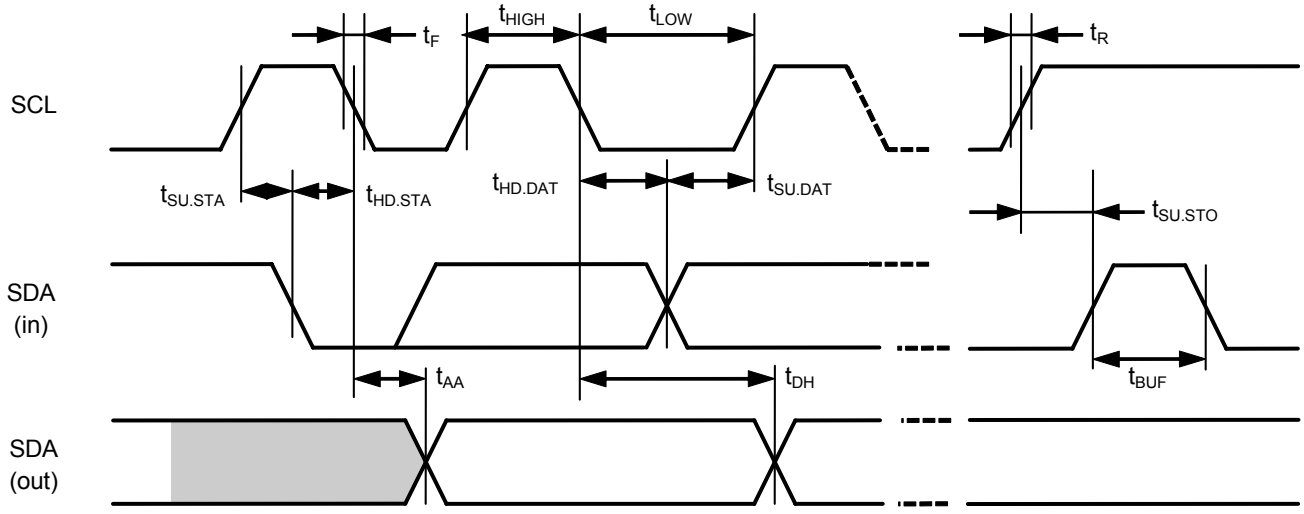


Figure 4 Bus Timing

Table 11

Item	Symbol	V_{CC} = 1.7 to 5.5 V		Unit
		Min.	Max.	
Write time	t_{WR}	–	4.0	ms

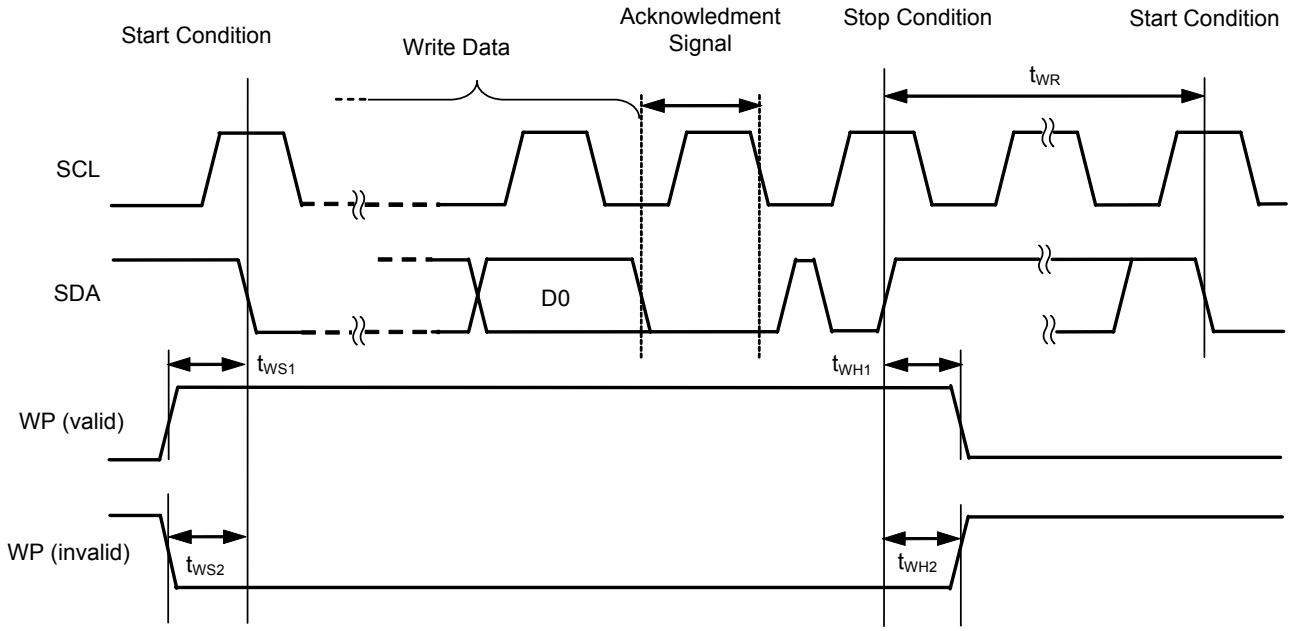


Figure 5 Write Cycle Timing

■ Pin Functions

1. A0, A1 and A2 (Address Input) Pins

In the S-34C02A, to set the slave address, connect each pin of A0, A1, A2 to GND or V_{CC}. Therefore the users can set 8 types of slave address by a combination of A0, A1, A2 pins.

Comparing the slave address transmitted from the master device and one that you set, makes possible to select the S-34C02A from other devices connected onto the bus.

Be sure to connect to fix the address input pin to GND or V_{CC}.

2. SDA (Serial Data Input / Output) Pin

The SDA pin is used for the bi-directional transmision of serial data. It consists of a signal input pin and an Nch open drain output pin.

In use, generally, connect the SDA line to any other device which has the open-drain or open-collector output with Wired-OR connection by pulling up to V_{CC} by a resistor.

3. SCL (Serial Clock Input) Pin

The SCL pin is used for the serial clock input. Since the signals are processed at a rising or falling edge of the SCL clock, pay the attention to the rising and falling time and comply with the specification.

4. WP (Write Protect) Pin

The Write protect function is to inhibit Write in all memory area or in the protect register while this pin is being connected to V_{CC}. While the WP pin is being connected to GND or left open, this pin inhibits Write in the first half of memory (addresses 00h to 7Fh) according to the status of the protect register.

■ Operation

1. Start Condition

A start condition starts by changing the SDA line from “H” to “L” while the SCL line is “H”.
All operations start with a start condition.

2. Stop Condition

A stop condition starts by changing the SDA line from “L” to “H” while the SCL line is “H”.
During Read sequence if the S-34C02A receives a stop condition, its Read operation is interrupted so that the S-34C02A goes in the standby mode.
During Write sequence if the S-34C02A receives a stop condition, the S-34C02A finishes installing Write data so that the Write operation starts.

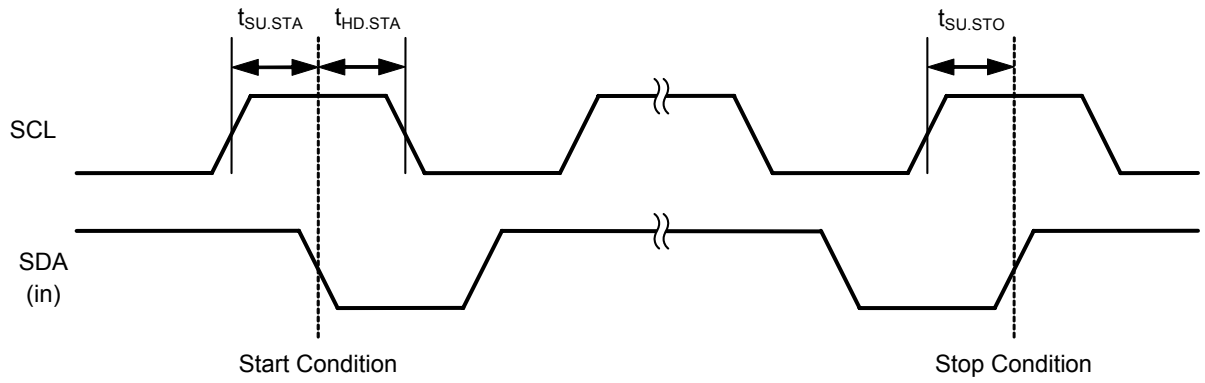


Figure 6 Start / Stop Conditions

3. Data Transmission

Data is transmitted by changing the SDA line while the SCL line is “L”.
If the SDA line changes while the SCL line is “H”, the S-34C02A goes in the start or stop condition status.

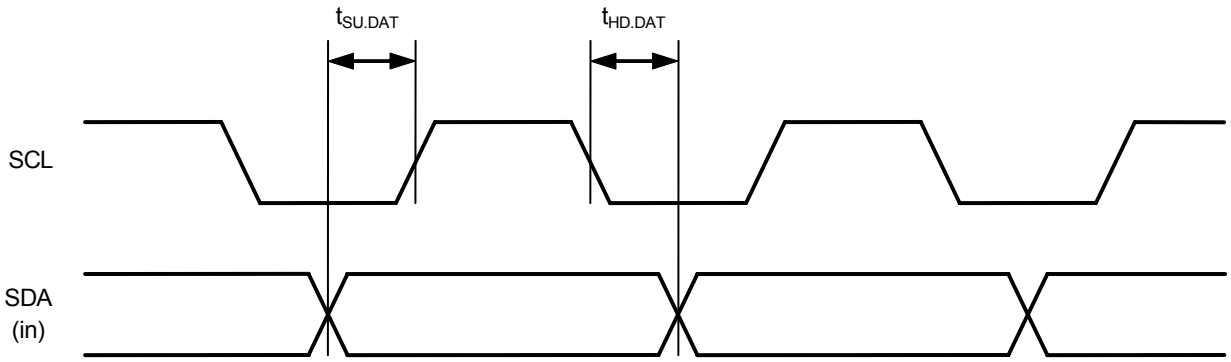


Figure 7 Data Transmission Timing

4. Acknowledgment

Data is transmitted sequentially in 8-bit. Changing the SDA line to “L” indicates that the devices on the system bus have received data, thus the devices send an acknowledgment signal back during the 9th clock of cycle.
The S-34C02A does not send an acknowledgment signal back during the Write operation.

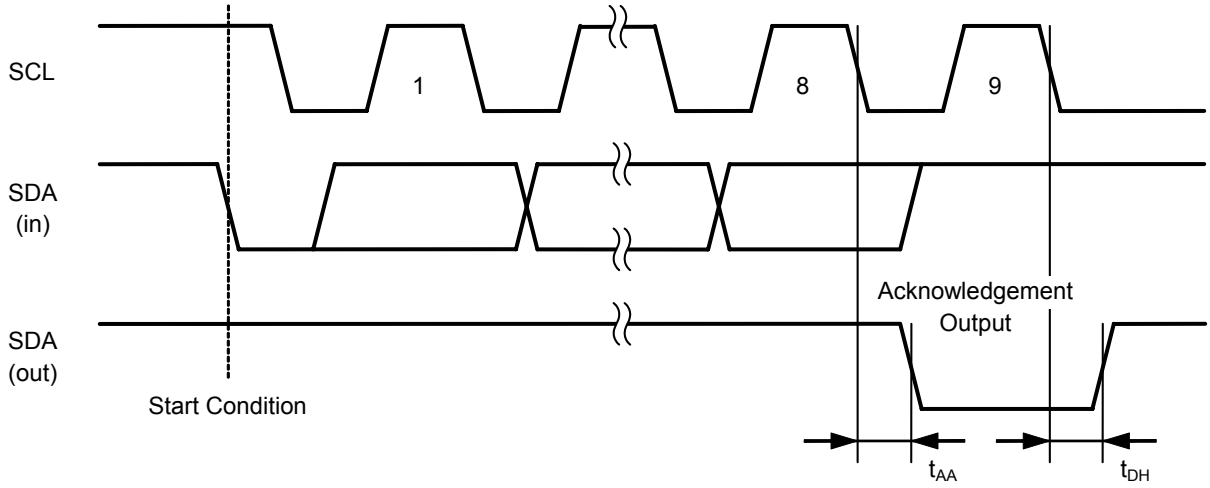


Figure 8 Acknowledgment Output Timing

5. Device Addressing

To start the transmission, the master device on the system generates a start condition for the slave address. After that, the master device transmits the 7-bit device address and the 1-bit Read/Write instruction code to the SDA bus.
In the S-34C02A, the higher 4 bits of the device address are device cord, and are fixed at “1010”.
The next 3 bits of the device address are slave address. This address is used to select the devices on the system bus, and is compared with the address value which is set beforehand by the address input pins (A0, A1, A2). If the comparison result matches, the slave address sends an acknowledgment signal back at the 9th clock of cycle.

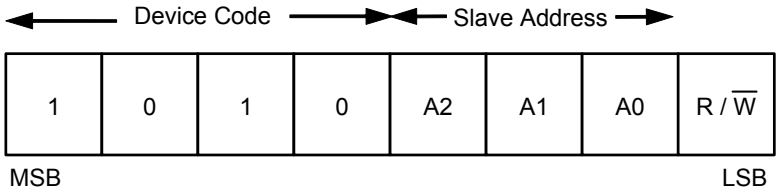


Figure 9 Device Address

6. Write Operation

6. 1 Byte Write

When the S-34C02A receives the 7-bit device address and the Read/Write instruction cord “0” after receiving a start condition, it generates an acknowledgment signal.
Next, it receives the 8-bit word address, and generates an acknowledgment signal. After that, it receives 8-bit Write data and generates an acknowledgment signal, it receives a stop condition so that the Write operation to the specified memory address starts.
During the Write operation to the S-34C02A, all operations are inhibited to be performed and S-34C02A does not send back an acknowledgment signal.

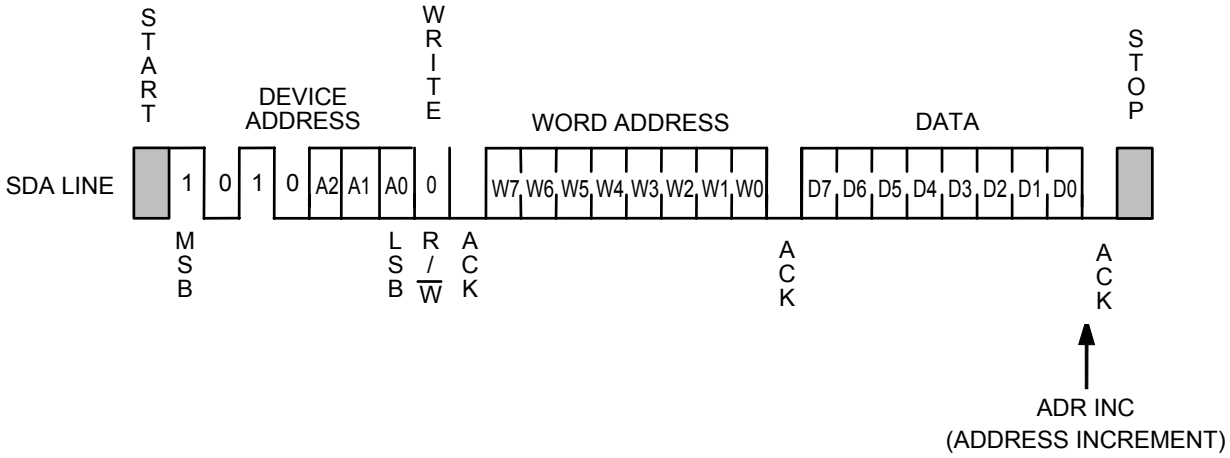


Figure 10 Byte Write

6. 2 Page Write

The S-34C02A is able to Page Write of 16-bit.
Its basic process to transmit data is as same as Byte Write, but it operates Page Write by sequentially receiving 8-bit Write data as much data as the page size has.
When the S-34C02A receives the 7-bit device address and Read/Write instruction code “0” after receiving a start condition, it generates an acknowledgment signal. Next, by receiving the 8-bit word address, it generates an acknowledgment signal. After the S-34C02A generated an acknowledgment signal by receiving 8-bit Write data, the S-34C02A receives 8-bit Write data equivalent to the next word address so that it generates an acknowledgment signal. Receiving 8-bit Write data and generating an acknowledgment signal are sequentially repeated, so that S-34C02A can receive Write data which has the largest page size.
By receiving a stop condition, the Write operation in an address area equivalent to the received page size starts.

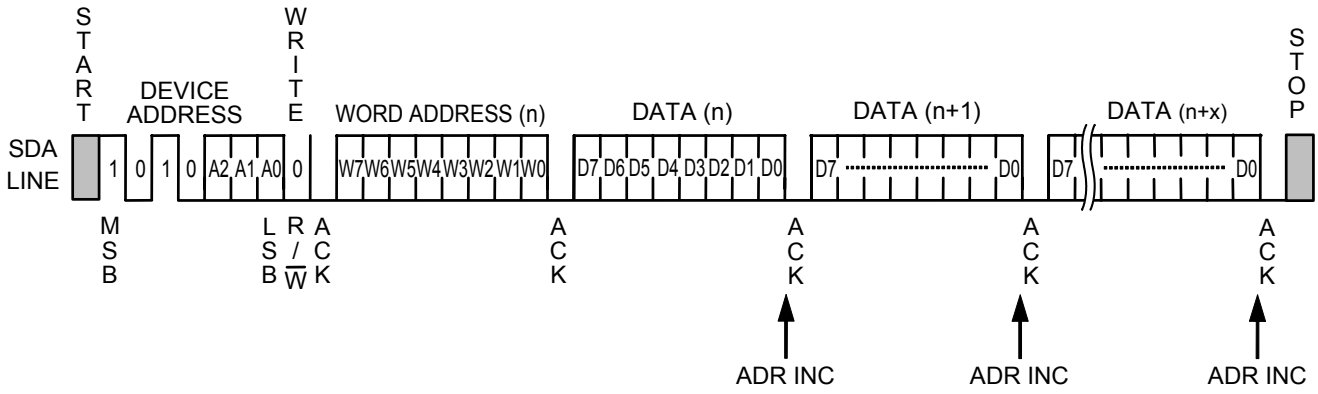


Figure 11 Page Write

In the S-34C02A, the lower 4 bits of the word address are automatically incremented every time when the S-34C02A receives 8-bit write data. If the size of Write data exceeds 16-byte, the higher 4-bit of the word address remain unchanged, and the lower 4 bits are rolled over and previously received data will be overwritten.

6. 3 Hardware Write Protect

Write protect is available in the S-34C02A.
When the WP pin is connected to V_{CC}, the Write operation in all memory area is inhibited.
Fix the WP pin during the period from the start condition to the stop condition in the Write operation (Byte Write and Page Write). Written data in the address is not assurable if the condition of the WP pin is changed during this period. Refer to **Figure 5** regarding the timing of Hardware Write Protect.
Be sure to connect the WP pin to GND when you don't use Hardware Write Protect. Hardware Write Protect is valid in the range of power supply voltage. If setting Hardware Write Protect valid, the S-34C02A does not generate an acknowledgment signal.
In this case, the users cannot perform the SWP (Set RSWP), CWP (Clear RSWP), PSWP (Set PSWP) instructions.

6. 4 Software Write Protect

The S-34C02A has Permanent Software Write Protect (PSWP) and Reversible Software Write Protect (RSWP).

(1) PSWP

If the software protect has been set with the PSWP instruction, 50% of the lower address (addresses 00h to 7Fh) in all memory is permanently Write-protected. This Write protect cannot be cleared by any instruction, or by power-cycling the device, and regardless the state of WP pin. Also, once the PSWP instruction has been successfully excuted, the S-34C02A no longer acknowledges any instruction (device code of "0110") to access the Write protect setting.

(2) RSWP

If the software protect has been set with the SWP (Set RSWP) instruction, 50% of the lower address (addresses 00h to 7Fh) in all memory is Write-protected. This write protect can be cleared with the CWP (Clear RSWP) instruction.
These two instructions have the same format as a Byte Write instruction, but have a different device code. Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents can be set in all "Don't Care". In the instructions of SWP and CWP, be sure to apply the high voltage of V_{HV} to the A0 pin, and input "H" or "L" to the A1 and A2 pins.

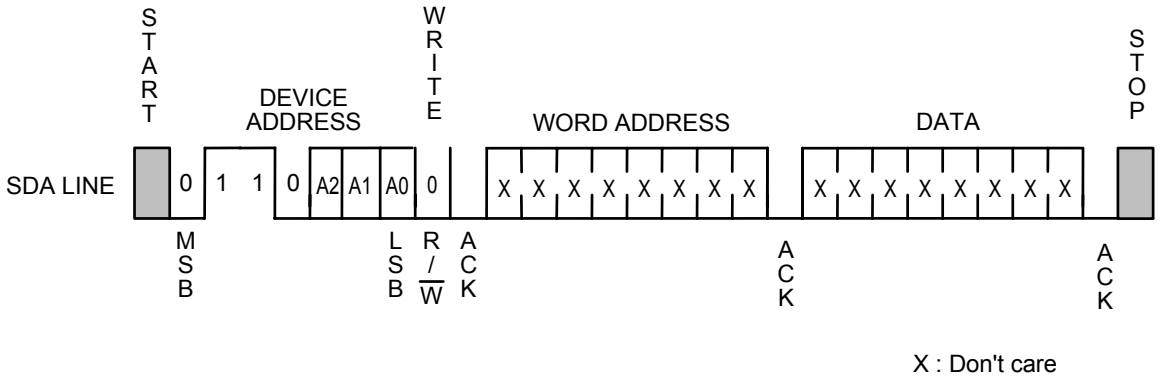


Figure 12 Software Write Protect

Table 12 Device Select Code

Instruction	Device code				Slave address			R/$\overline{W}$	Pin condition		
	B7	B6	B5	B4	B3	B2	B1	B0	A2	A1	A0
Memory Area Select *1	1	0	1	0	A2	A1	A0	R/$\overline{W}$	A2	A1	A0
Set RSWP (SWP)	0	1	1	0	0	0	1	0	V_{SS}	V_{SS}	V_{HV}
Clear RSWP (CWP)	0	1	1	0	0	1	1	0	V_{SS}	V_{CC}	V_{HV}
Set PSWP (PSWP)*1	0	1	1	0	A2	A1	A0	0	A2	A1	A0
Read SWP	0	1	1	0	0	0	1	1	V_{SS}	V_{SS}	V_{HV}
Read CWP	0	1	1	0	0	1	1	1	V_{SS}	V_{CC}	V_{HV}
Read PSWP*1	0	1	1	0	A2	A1	A0	1	A2	A1	A0

***1.** Slave addresses A2, A1, A0 are compared by the address input pins (A0, A1, A2) of a memory device with the address value which is set beforehand.

Table 13 Acknowledgment for WRITE Instruction(R / $\overline{W}$ bit = 0)

Status	WP	Instruction	ACK output	Word Address	ACK output	DATA	ACK output	Write
Permanent Software Write Protect (PSWP)	X	SWP, CWP or PSWP	No	Don't care	No	Don't care	No	No
		Page or Byte Write in Lower 128 bytes	Yes	Address	Yes	DATA	No	No
Reversible Software Write Protect (RSWP)	0	SWP	No	Don't care	No	Don't care	No	No
		CWP	Yes	Don't care	Yes	Don't care	Yes	Yes
		PSWP	Yes	Don't care	Yes	Don't care	Yes	Yes
		Page or Byte Write in Lower 128 bytes	Yes	Address	Yes	DATA	No	No
	1	SWP	No	Don't care	No	Don't care	No	No
		CWP	Yes	Don't care	Yes	Don't care	No	No
		PSWP	Yes	Don't care	Yes	Don't care	No	No
		Page or Byte Write	Yes	Address	Yes	DATA	No	No
No software protect	0	SWP, CWP or PSWP	Yes	Don't care	Yes	Don't care	Yes	Yes
		Page or Byte Write	Yes	Address	Yes	DATA	Yes	Yes
	1	SWP, CWP or PSWP	Yes	Don't care	Yes	Don't care	No	No
		Page or Byte Write	Yes	Address	Yes	DATA	No	No

Table 14 Acknowledgment for READ Instruction(R / $\overline{W}$ bit = 1)

Status	Instruction	ACK output	Word Address	ACK output	DATA	ACK output
Permanent Software Write Protect (PSWP)	SWP, CWP or PSWP	No	Don't care	No	Don't care	No
Reversible Software Write Protect (RSWP)	SWP	No	Don't care	No	Don't care	No
	CWP	Yes	Don't care	No	Don't care	No
	PSWP	Yes	Don't care	No	Don't care	No
No software protect	SWP, CWP or PSWP	Yes	Don't care	No	Don't care	No

6. 5 Acknowledge Polling

Acknowledge polling is used to find when the Write operation has completed. After receiving a stop condition the Write operation has once started, all operations are inhibited to be performed so that the S-34C02A cannot respond to the signals transmitted from the master device. The master device sends a start condition, the device address and Read/Write instruction code to the S-34C02A (slave address), and detects the response from the slave address. It is possible to find when the Write operation has completed. Thus if the slave device does not send an acknowledgment signal back, the Write operation is in progress. If it sends an acknowledgment signal back, the Write operation has completed. Fix the WP pin until an acknowledgment is confirmed. It is recommended to use the Read instruction “1” for the Read/Write instruction code transmitted by the master device during acknowledgment polling.

7. Read

7. 1 Current Address Read

Both in the Write and Read operation, the S-34C02A maintains the memory address that is one the S-34C02A received when it has accessed last time. The memory address is maintained unless the power supply voltage is equal to the current address hold voltage V_{AH} or less. Therefore as long as the master device acknowledges the position where the address pointer is, data can be read by the memory address of an address pointer without specifying the word address. This is the current address Read.
The following is about the case that an address counter in the S-34C02A is in "n".
When the S-34C02A receives the 7-bit device address and the Read/Write instruction code "1" after receiving a start condition, it generates an acknowledgment signal.
Next, 8-bit data at address n is input from the S-34C02A synchronizing with a SCL clock. At the same time an address counter is incremented at a falling edge of SCL clock right after the output of 8th bit data, so that address n+1 is contained in an address counter. The Read operation ends when the master device outputs a stop condition, not an acknowledgment signal.

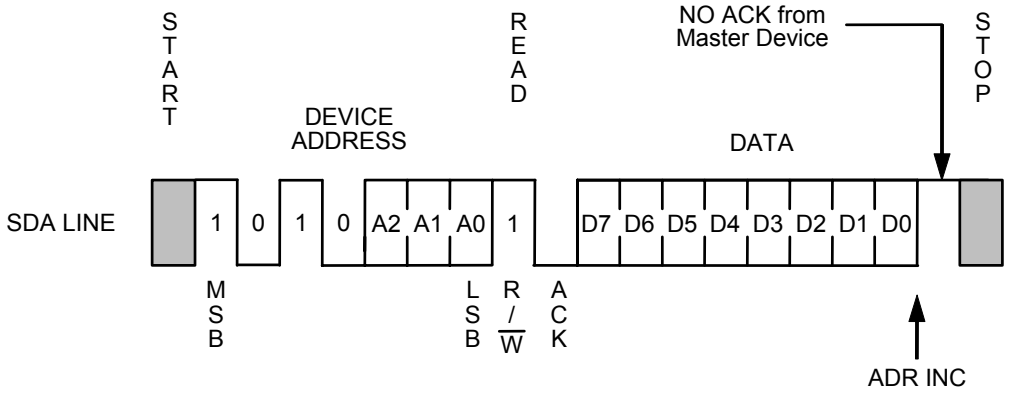


Figure 13 Current Address Read

Regarding the recognition of address pointer, pay the attention to the following;
In the Read operation, a memory address counter in the S-34C02A is automatically incremented every time at a falling edge of the SCL clock right after the output of 8th bit data. However, in the Write operation, a memory address counter is not be incremented because the higher 4 bits of the memory address (the higher 4 bits of the word address) are fixed every time at a falling edge of the SCL clock right after the receipt of 8th bit data.

7. 2 Random Read

Random Read is used to read data at an arbitrary memory address.
To load the memory address into an address counter in the S-34C02A, perform Dummy Write with the process below.
When the S-34C02A receives the 7-bit device address and the Read/Write instruction code “0” after receiving a start condition, it generates an acknowledgment signal. After that, it generates an acknowledgment signal by receiving the 8-bit word address. By these operations, the memory address is loaded into the address counter in the S-34C02A.
After this, in Byte Write and Page Write, the S-34C02A receives Write data, but in Dummy Write, the S-34C02A does not receive data.
Since the memory address has been loaded into the memory address counter by Dummy Write, the master device sends a start condition newly and performs the same operation as current Read. The users can read data which starts from the arbitrary memory address.
Thus, the S-34C02A receives the 7-bit device address and the Read/Write instruction cord “1” after receiving a start condition, it generates an acknowledgment signal.
And 8-bit data is output from the S-34C02A synchronizing with the SCL clock. After that, the Read operation ends when the master device transmits a stop condition, not an acknowledgment signal.

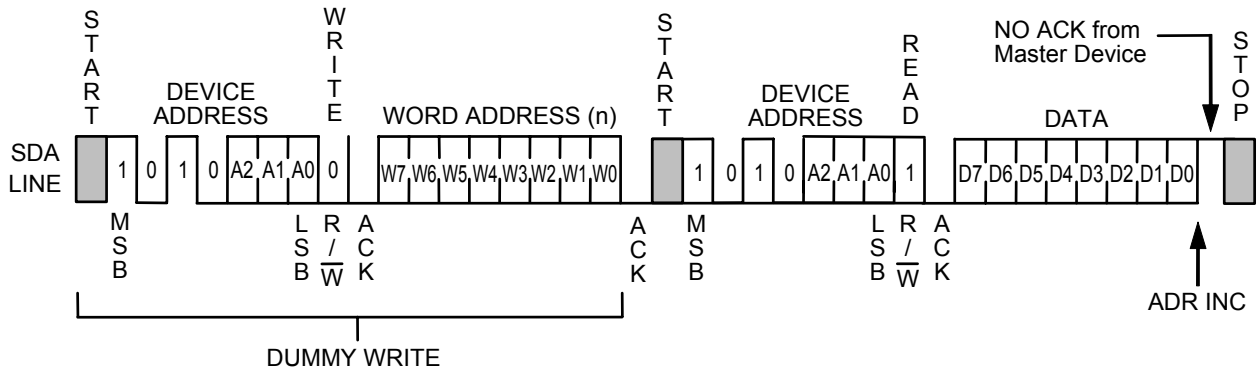


Figure 14 Random Read

7. 3 Sequential Read

Both in current Read and random Read, when the S-34C02A receives the 7-bit device address and Read/Write instruction code “1” after receiving a start condition, it generates an acknowledgment signal.
When 8-bit data is output from the S-34C02A synchronizing with the SCL clock, an memory address counter in the S-34C02A is automatically incremented at a falling edge of SCL clock right after the output of 8th bit data.
After that, the master device transmits an acknowledgment signal, the next data in the memory data address is output. A memory address counter in the S-34C02A is incremented because the master device transmits an acknowledge signal, so that S-34C02A keeps reading data sequentially. This is sequential read.
The Write operation ends when the master device transmits a stop condition, not an acknowledgment signal.
Although S-34C02A can read data sequentially in this sequential read, if a memory address counter reaches the last word address, it rolls over to the first memory address.

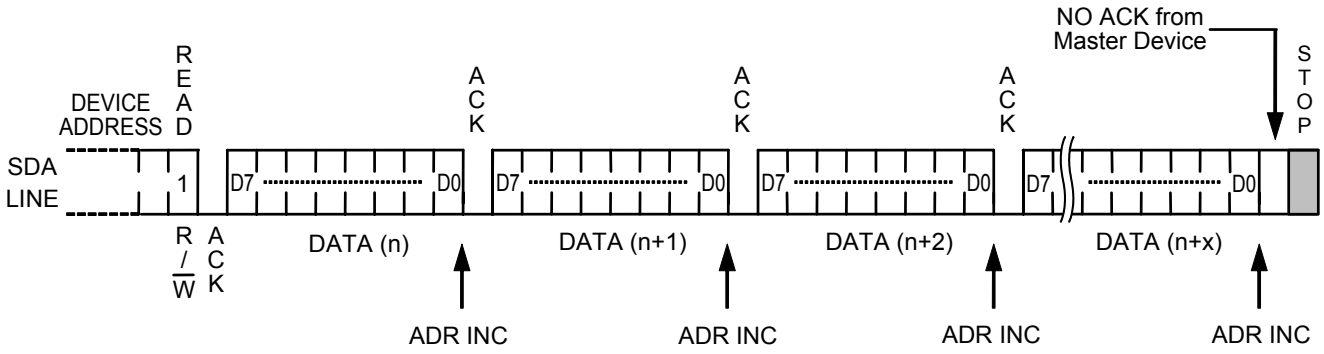


Figure 15 Sequential Read

8. Address Increment Timing

In the Read operation, the timing when a memory address counter is automatically incremented is at a falling edge of the SCL clock right after the output of 8th bit.
In the Write operation, that timing is at a falling edge of the SCL clock when installing the 8th bit data.

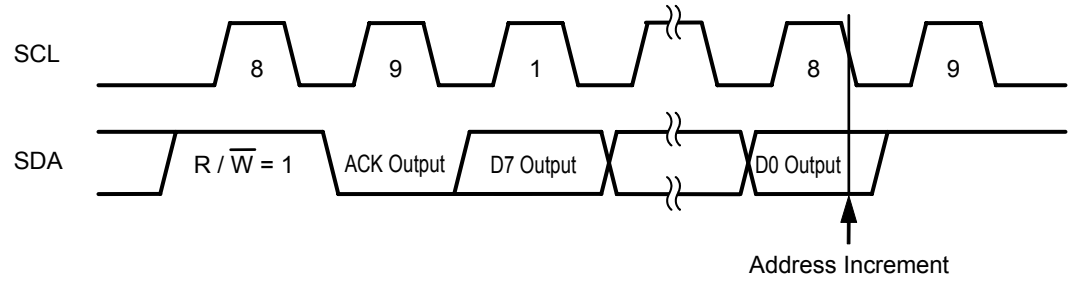


Figure 16 Address Increment Timing in Reading

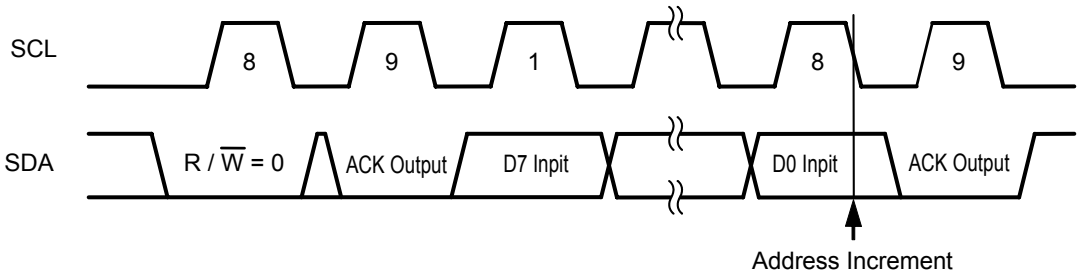


Figure 17 Address Increment Timing in Writing

■ Write Inhibition Function at Low Power Voltage

The S-34C02A has a built-in detection circuit which operates with the low power supply voltage, cancels Write when the power supply voltage drops and power-on. Its detection and release voltages are 1.20 V typ. (Refer to **Figure 18**).
The S-34C02A cancels Write by detecting a low power supply voltage when it receives a stop condition.
In the data trasmission and the Write operation, data in the address written during the low power supply voltage is not assurable.

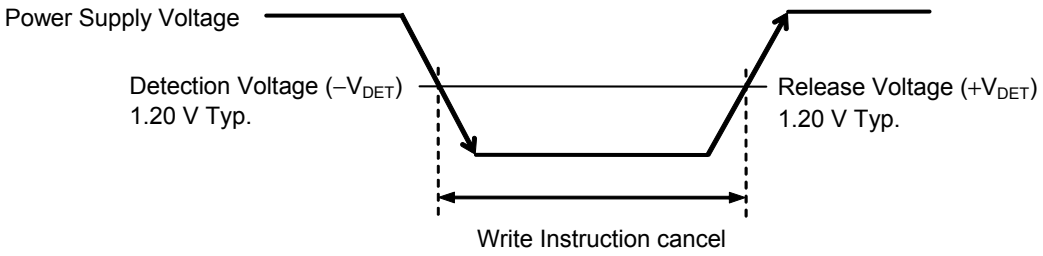


Figure 18 Operation at Low Power Voltage

■ Using S-34C02A

1. SDA I/O pin and SCL input pin

In consideration of I^2C-bus protocol function, the SDA I/O and SCL input pins*1 should be connected with a pull-up resister of 1 to 5 kΩ.
The S-34C02A cannot transmit normally without using a pull-up resistor.

***1.** In the case that the SCL input pin of the S-34C02A is connected to the tri-state output pin in the master device, connect the SCL pin with a pull-up resistor as well in order not to set the SCL input pin in high impedance. This prevents the S-34C02A from error caused by an uncertain output (high impedance) from the tri-state pin when resetting the master device during the voltage drop.

2. Equivalent circuit of I/O pin

Each input pin (A0, A1, A2, WP) of the S-34C02A has a built-in pull-down register. The SDA line has an open-drain output. The followings are equivalent circuits of the pins.

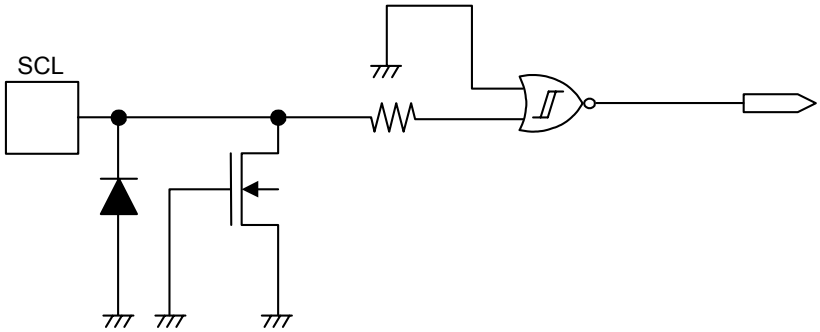


Figure 19 SCL Pin

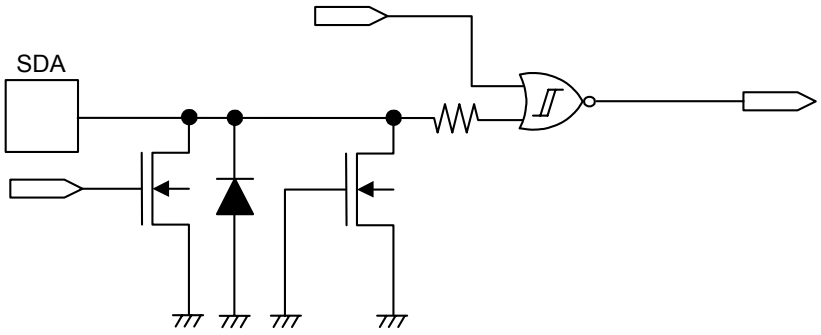


Figure 20 SDA Pin

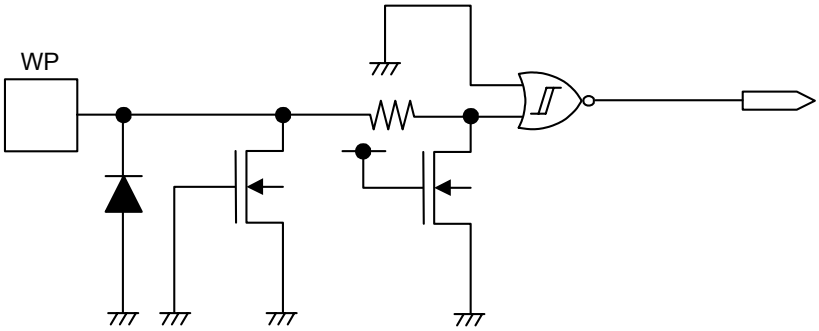


Figure 21 WP Pin

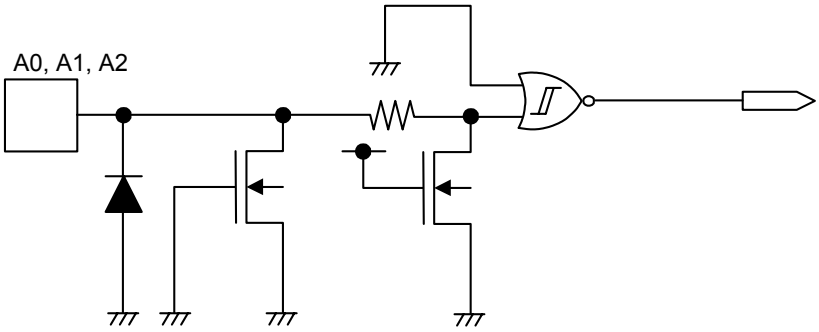


Figure 22 A0, A1, A2 Pin

3. Phase adjustment during S-34C02A access

The S-34C02A does not have a pin to reset (the internal circuit). The users cannot forcibly reset it externally. If the communication to the S-34C02A interrupted, the users need to handle it as you do for software.
Although the reset signal is input to the master device, the S-34C02A's internal circuit does not go in reset, but it does by inputting a stop condition to the S-34C02A. The S-34C02A keeps the same status thus cannot do the next operation. Especially, this case is correspond to that only the master device is reset when the power supply voltage drops.
If the power supply voltage restored in this status, input the instruction after resetting (adjusting the phase with the master device) the S-34C02A. How to reset is shown below.

[How to reset S-34C02A]

The S-34C02A is able to be reset by a start and stop instructions. When the S-34C02A is reading data "0" or is outputting the acknowledgment signal, outputs "0" to the SDA line. In this status, the master device cannot output an instruction to the SDA line. In this case, terminate the acknowledgment output operation or the Read operation, and then input a start instruction. **Figure 23** shows this procedure.
First, input a start condition. Then transmit 9 clocks (dummy clock) of SCL. During this time, the master device sets the SDA line to "H". By this operation, the S-34C02A interrupts the acknowledgment output operation or data output, so input a start condition*1. When a start condition is input, the S-34C02A is reset. To make doubly sure, input the stop condition to the S-34C02A. The normal operation is then possible.

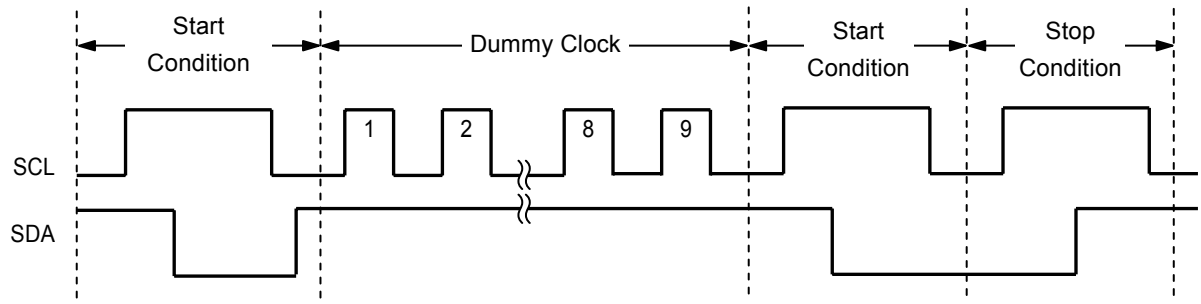


Figure 23 Resetting S-34C02A

***1.** After 9 clocks (dummy clock), if the SCL clock contuniues to being output without inputting a start condition, S-34C02A may go in the Write operation when it receives a stop condition. To prevent this, input a start condition after 9 clock (dummy clock).

Remark Regarding this reset procedure with dummy clock, it is recommended to perform at the system initialization after applying the power supply voltage.

4. Acknowledge check

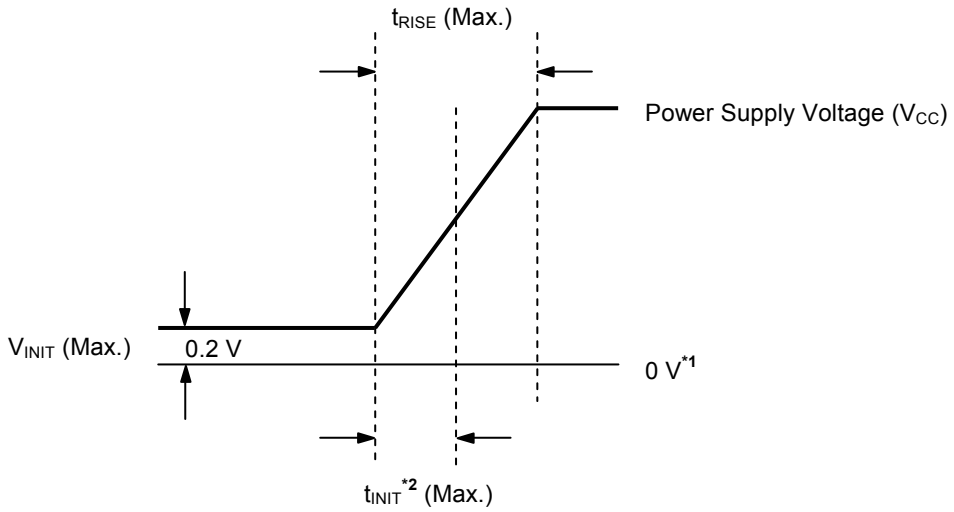
The I^{2}C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the master device and S-34C02A. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check with the master device.

5. Built-in power-on-clear circuit

The S-34C02A has a built-in power-on-clear circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-clear circuit normally, the following conditions must be satisfied to raise the power supply voltage.

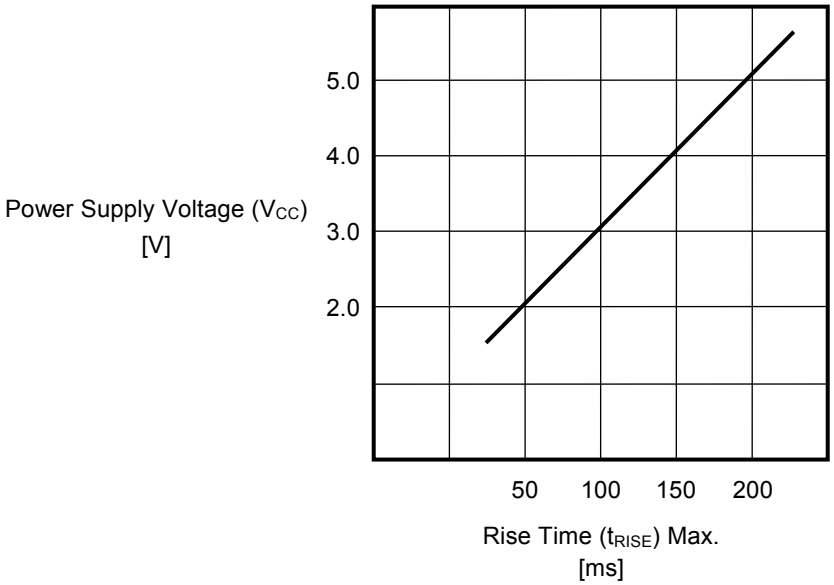
5. 1 Raising power supply voltage

Shown in **Figure 24**, raise the power supply voltage from 0.2 V max., within the time defined as t_{RISE} which is the time required to reach the power supply voltage to be set.
For example, if the power supply voltage is 5.0 V, t_{RISE} = 200 ms seen in **Figure 25**. The power supply voltage must be raised within 200 ms.



***1.** 0 V means there is no difference in potential between the V_{CC} pin and the GND pin of the S-34C02A.
***2.** t_{INIT} is the time required to initialize the S-34C02A. No instructions are accepted during this time.

Figure 24 Raising Power Supply Voltage



For example: If the supply voltage = 5.0 V, raise the power supply voltage to 5.0 V within 200 ms.

Figure 25 Rise Time of Power Supply Voltage

When initialization is successfully completed by the power-on-clear circuit, the S-34C02A enters the standby status. If the power-on-clear circuit does not operate, the followings are the possible causes.

(1) Because the S-34C02A has not completed initialization, an instruction previously input is still valid or an instruction may be inappropriately recognized. In this case, S-34C02A may perform the Write operation.
(2) The voltage drops due to power off while the S-34C02A is being accessed. Even if the master device is reset due to the low power voltage, the S-34C02A may malfunction unless the power-on-clear operation conditions of S-34C02A are satisfied. For the power-on-clear operation conditions of the S-34C02A, refer to **5.1 Raising power supply voltage**.

If the power-on-clear circuit does not operate, match the phase (reset) so that the S-34C02A's internal circuit is normally reset. The statuses of the S-34C02A immediately after the power-on-clear circuit operation and when phase is matched (reset) are the same.

5. 2 Initialization time

The S-34C02A initializes at the same time when the power supply voltage is raised. Input instructions to the S-34C02A after initialization. S-34C02A does not accept any instruction during initialization.
Figure 26 shows the initialization time of the S-34C02A.

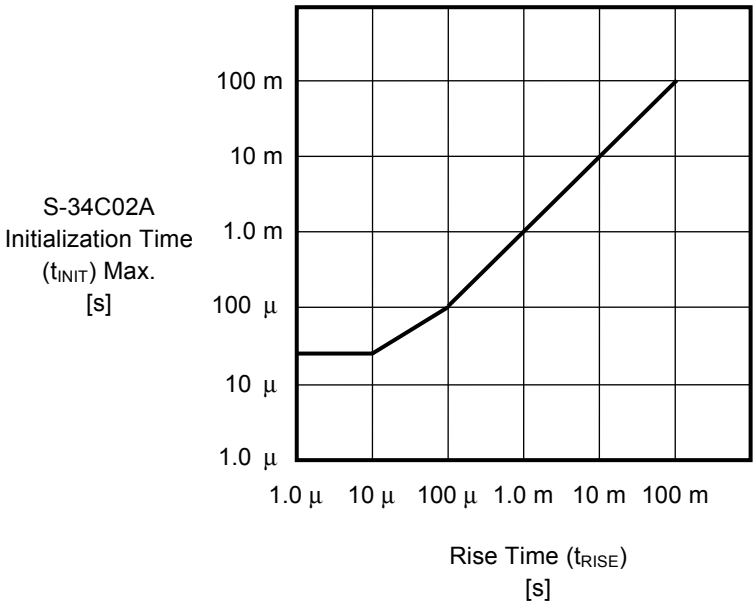


Figure 26 Initialization Time of S-34C02A

6. Data hold time ($t_{HD.DAT}$ = 0 ns)

If SCL and SDA of the S-34C02A are changed at the same time, it is necessary to prevent a start/stop condition from being mistakenly recognized due to the effect of noise. If a start/stop condition is mistakenly recognized during communication, the S-34C02A enters the standby status.
In the S-34C02A, it is recommended to set the delay time of 0.3 µs minimum from a falling edge of SCL for the SDA. This is to prevent S-34C02A from going in a stop/start condition due to the time lag caused by the load of the bus line.

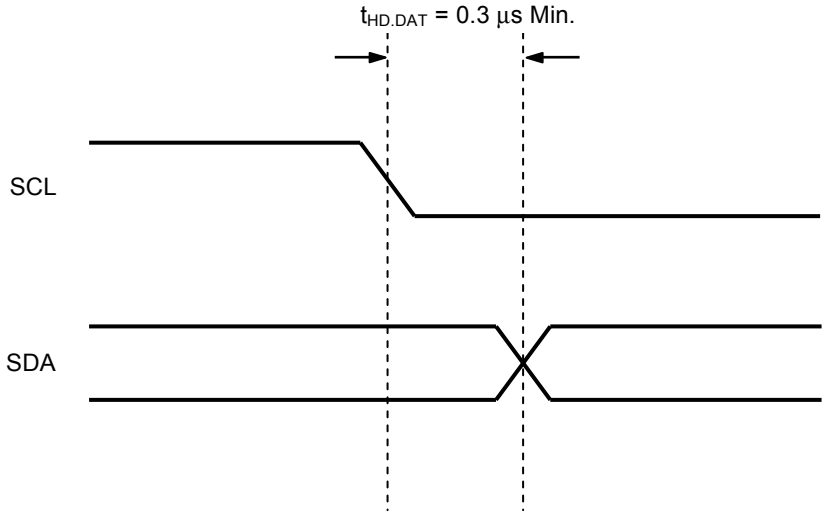


Figure 27 S-34C02A Data Hold Time

7. SDA pin and SCL pin noise suppression time

The S-34C02A includes a built-in low-pass filter at the SDA and SCL pins to suppress noise. This means that if the power supply voltage is 5.0 V, noise with a pulse width of 160 ns or less can be suppressed.
For details of the assurable value, refer to noise suppression time (t_I) in **Table 10**.

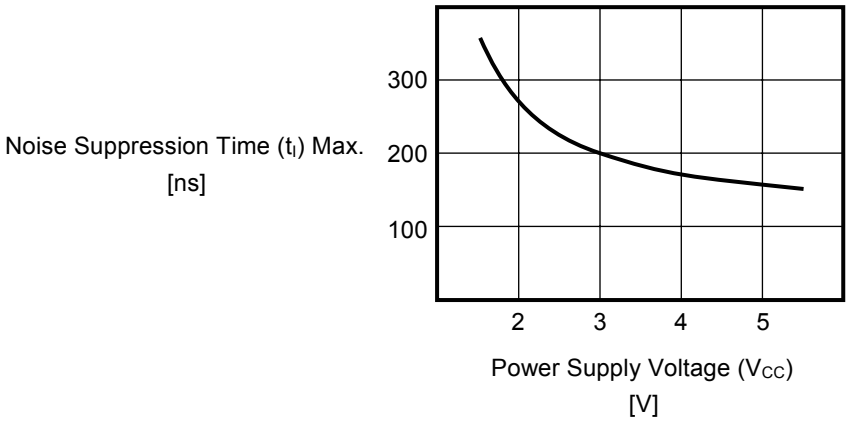


Figure 28 Noise Suppression Time for SDA and SCL Pins

8. S-34C02A Operation when inputting a stop condition with the clock less than the defined data length (less than 8-bit) to the SCL pin inputting Write data

If S-34C02A forcibly recieves a stop condition while it is receiving Write data of 1-byte, it does not perform the Write operation.
To operate Page Write, if S-34C02A recieves a stop condition after receiving data of 1-byte or more, S-34C02A operates Write only in the address equivalent to the byte of which S-34C02A normally received 8-bit data before a stop condition.

9. S-34C02A Operation and data if inputting Write data more than the defined Page Size during Page Write

The S-34C02A is able to Page Write of 16-byte, but in case if it receives data of 17-byte, 8-bit data of the 17th byte is overwritten in the first byte in the same page because the S-34C02A cannot Write data across the page address.

10. Precaution for use

Absolute maximum ratings: Do not operate these ICs in excess of the absolute maximum ratings (as listed on the data sheet). Exceeding the supply voltage rating can cause latch-up.

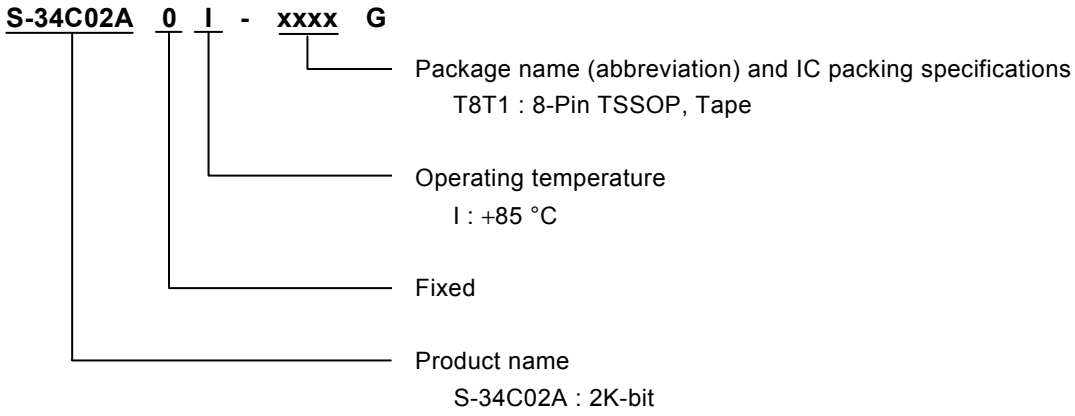
Operations with moisture on the E^2PROM pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the E^2PROM up from low temperature tank during the evaluation. Be sure that not remain frost on the E^2PROM pin to prevent malfunction by short-circuit.
Also attention should be paid in using on environment, which is easy to dew for the same reason.

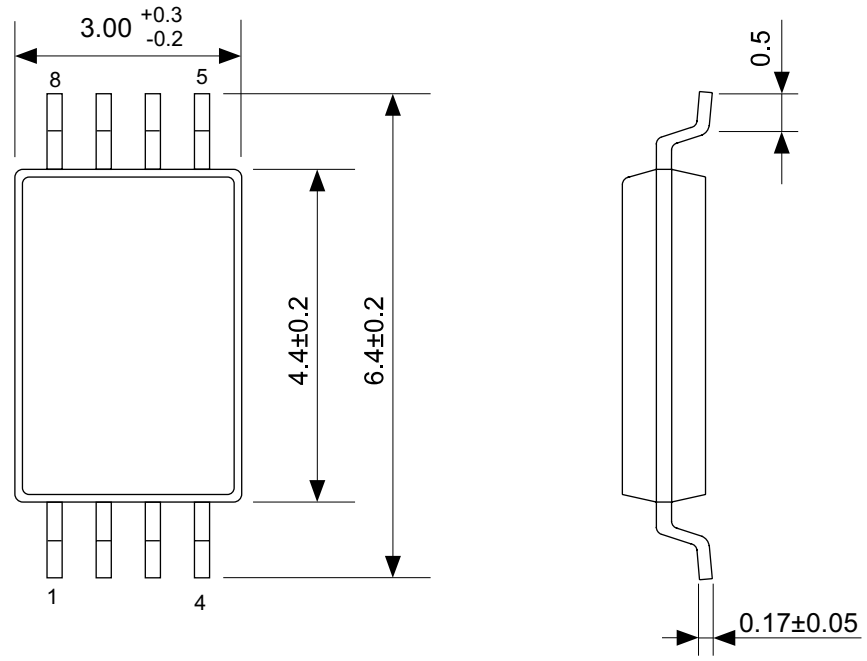
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

■ Product Name Structure

1. 8-Pin TSSOP Package





No. FT008-A-P-SD-1.1

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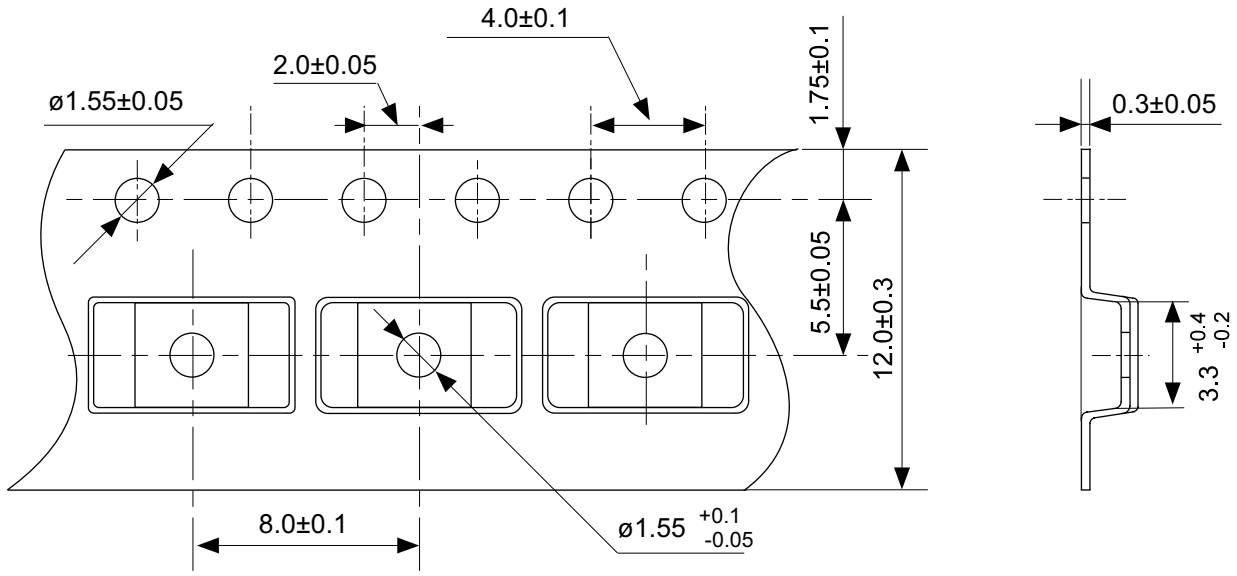
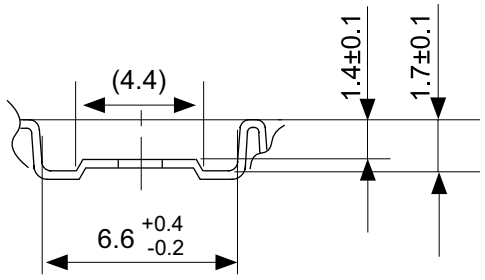
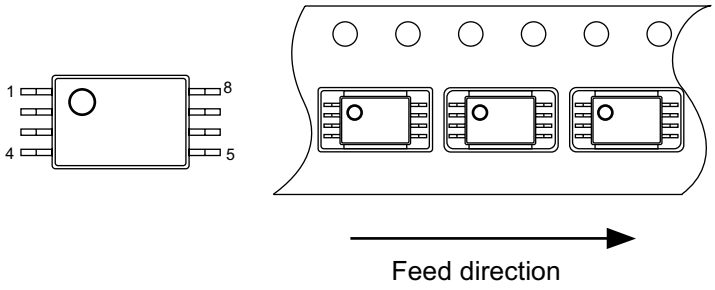
UNIT	mm
Seiko Instruments Inc.	







No. FT008-E-C-SD-1.0

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No.	FT008-E-C-SD-1.0
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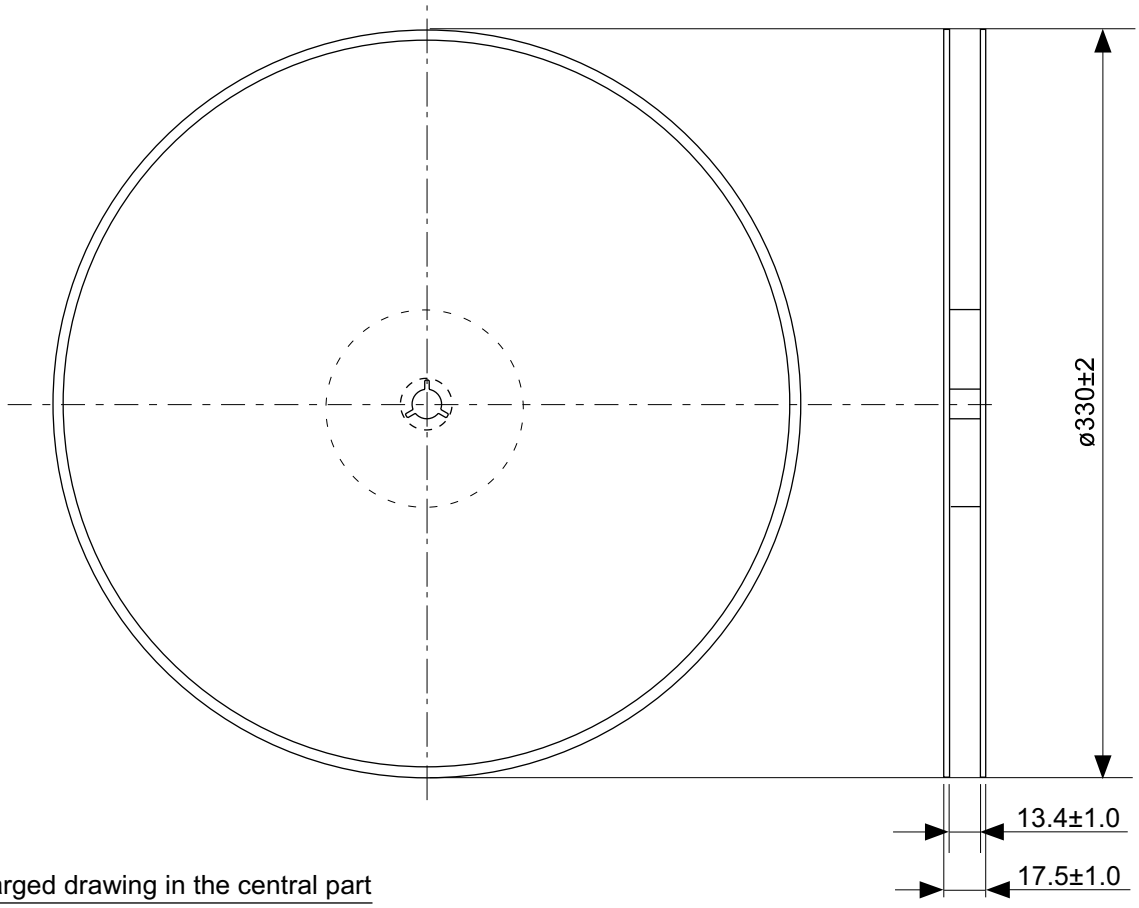
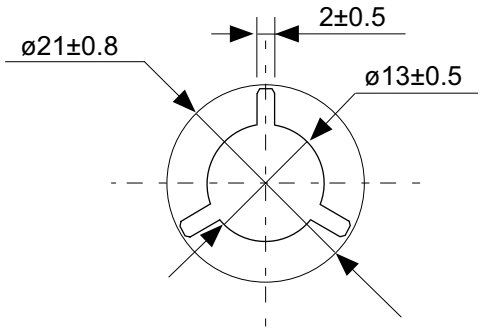
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
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UNIT	mm		
Seiko Instruments Inc.			

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