S-34C04A

2-WIRE SERIAL E^2PROM FOR DIMM SERIAL PRESENCE DETECT

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Rev.1.0_02_U

This IC is a 2-wire serial E^2PROM for DIMM serial presence detect which operates in 1.7 V to 3.6 V voltage ranges. This IC has the capacity of 4 K-bit and the organization of 2 pages × 256-word × 8-bit. Page write and sequential read are available. This IC operates with the I^2C-bus at 1.0 MHz maximum.

Caution **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

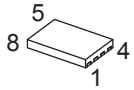
■ Features

- Page write: 16 bytes / page
- Sequential read
- Write protect function during low power supply voltage
- Write protect:
  Individual software data protection for each of four 128-byte blocks
- Endurance: 10^6 cycle / word*1 (Ta = +25°C)
- Data retention: 100 years (Ta = +25°C)
- Memory capacity: 4 K-bit
- Initial delivery state: FFh
- JEDEC standard compliant: EE1004-1
- Current consumption:
  Standby mode: 3.0 μA max.
  Read operation mode: 0.4 mA max.
  Write operation mode: 2.0 mA max.
- Operation voltage range: 1.7 V to 3.6 V
- Operation frequency: 1.0 MHz max. (V_{DD} = 2.2 V to 3.6 V)
  400 kHz max. (V_{DD} = 1.7 V to 3.6 V)
- Noise suppression: Schmitt trigger and noise filter on input pins (SCL, SDA)
- Operation temperature range: Ta = −20°C to +125°C
- Lead-free (Sn 100%), halogen-free

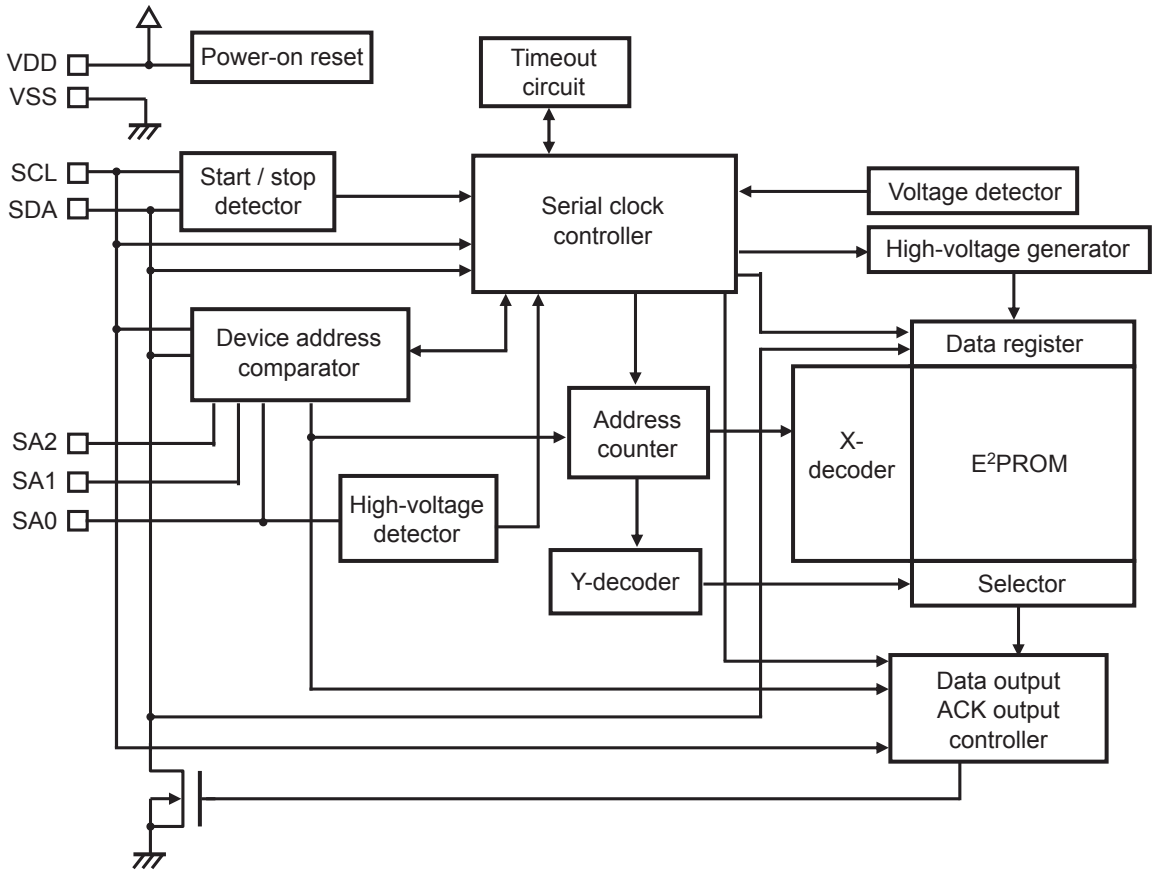
***1.** For each address (Word: 8-bit)

■ Package

- DFN-8(2030)



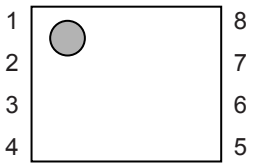
■ Block Diagram



■ Pin Configuration

1. DFN-8(2030)

Top view



Pin No.	Symbol	Description
1	SA0	Select address input
2	SA1	Select address input
3	SA2	Select address input
4	VSS	Ground
5	SDA*1	Serial data I/O
6	SCL*1	Serial clock input
7	NC*2	No connection
8	VDD	Power supply

***1.** Do not use it in "High-Z".
***2.** The NC pin is electrically open.
Therefore, leave it open or connect it to VDD pin or VSS pin.

Remark For DFN-8(2030) package, connect the heatsink of back side to the board, and set electric potential open or V_{SS}.
However, do not use it as the function of electrode.

■ Absolute Maximum Ratings

Table 1

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	−0.3 to +4.3	V
Input voltage (SCL, SA1, SA2)	V_{IN}	−0.3 to +4.3	V
SA0 high level input voltage	V_{HV}	−0.3 to +10.0	V
I/O voltage (SDA)	V_{IO}	−0.3 to +4.3	V
Operation ambient temperature	T_{opr}	−20 to +125	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operation Conditions

Table 2

Item	Symbol	Condition	Min.	Max.	Unit
Power supply voltage	V_{DD}	EE1004-1 compliant	1.7	3.6	V
Operation ambient temperature	T_{opr}	−	−20	+125	°C
High level input voltage	V_{IH}	−	$0.7 \times V_{DD}$	$V_{DD} + 0.5$	V
Low level input voltage	V_{IL}	−	−0.3	$0.3 \times V_{DD}$	V
SA0 high level input voltage	V_{HV}	$V_{HV} - V_{DD} \geq 4.8$ V	7.0	10.0	V

■ Pin Capacitance

Table 3

(Ta = +25°C, f = 1.0 MHz, V_{DD} = 2.5 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V (SCL, SA0, SA1, SA2)	−	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V (SDA)	−	8	pF

■ Endurance

Table 4

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	Ta = +25°C	10^6	−	cycle / word*1

***1.** For each address (Word: 8-bit)

■ Data Retention

Table 5

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data retention	−	Ta = +25°C	100	−	year

■ DC Electrical Characteristics

Table 6

Item	Symbol	Condition	Ta = −20°C to +125°C, V_{DD} = 1.7 V to 3.6 V		Unit
			Min.	Max.	
Standby current consumption	I_{DD1}	$V_{IN} = V_{SS}$ or V_{DD}	−	3.0	μA
Current consumption (READ)	I_{DDR}	f = 1.0 MHz (V_{DD} = 2.2 V to 3.6 V) f = 400 kHz (V_{DD} = 1.7 V to 3.6 V)	−	0.4	mA
Current consumption (WRITE)	I_{DDW}	f = 1.0 MHz (V_{DD} = 2.2 V to 3.6 V) f = 400 kHz (V_{DD} = 1.7 V to 3.6 V)	−	2.0	mA
Input leakage current	I_{LI}	SCL, SDA $V_{IN} = V_{SS}$ to V_{DD}	−	1.0	μA
Output leakage current	I_{LO}	SDA $V_{OUT} = V_{SS}$ to V_{DD}	−	1.0	μA
Input current 1	I_{IL}	SA0, SA1, SA2 $V_{IN} < 0.3 \times V_{DD}$	−	50.0	μA
Input current 2	I_{IH}	SA0, SA1, SA2 $V_{IN} > 0.7 \times V_{DD}$	−	2.0	μA
Input impedance 1	Z_{IL}	SA0, SA1, SA2 $V_{IN} = 0.3 \times V_{DD}$	30	−	kΩ
Input impedance 2	Z_{IH}	SA0, SA1, SA2 $V_{IN} = 0.7 \times V_{DD}$	800	−	kΩ
Low level output voltage 1	V_{OL1}	SDA I_{OL} = 3.0 mA, $V_{DD} > 2.0$ V	−	0.4	V
Low level output voltage 2	V_{OL2}	SDA I_{OL} = 2.0 mA, $V_{DD} \leq 2.0$ V	−	$0.2 \times V_{DD}$	V
Low level output current 1	I_{OL1}	SDA V_{OL} = 0.4 V, $V_{DD} \geq 2.2$ V	20	−	mA
Low level output current 2	I_{OL2}	SDA V_{OL} = 0.6 V, f ≤ 400 kHz	6	−	mA
Power-on reset threshold voltage	V_{PON}	−	1.6	−	V
Power-off threshold voltage	V_{POFF}	−	−	0.9	V

■ AC Electrical Characteristics

Table 7 Measurement Conditions

Input pulse voltage	$0.2 \times V_{DD}$ to $0.8 \times V_{DD}$
Input pulse rising / falling time	20 ns or less
Output reference voltage	$0.3 \times V_{DD}$ to $0.7 \times V_{DD}$
Output load	100 pF

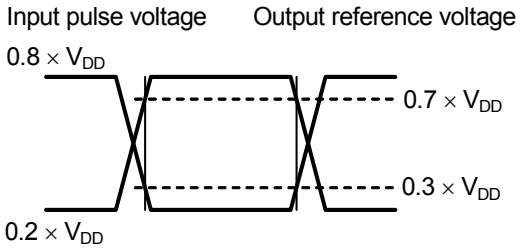


Figure 1 Input / Output Waveform during AC Measurement

Table 8

Item	Symbol	Ta = −20°C to +125°C				Unit
		V_{DD} = 1.7 V to 3.6 V		V_{DD} = 2.2 V to 3.6 V		
		400 kHz		1000 kHz		
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	10	400	10	1000	kHz
SCL clock time "L"	t_{LOW}	1.3	–	0.5	–	µs
SCL clock time "H"	t_{HIGH}	0.6	–	0.26	–	µs
SCL clock "L" timeout	$t_{TIMEOUT}$	25	35	25	35	ms
SCL, SDA rising time	t_R	0.02	0.3	–	0.12	µs
SCL, SDA falling time	t_F	0.02	0.3	–	0.12	µs
Data input setup time	$t_{SU.DAT}$	100	–	50	–	ns
Data input hold time	$t_{HD.DI}$	0	–	0	–	ns
Data output hold time	$t_{HD.DAT}$	200	900	0	350	ns
Start condition setup time	$t_{SU.STA}$	0.6	–	0.26	–	µs
Start condition hold time	$t_{HD.STA}$	0.6	–	0.26	–	µs
Stop condition setup time	$t_{SU.STO}$	0.6	–	0.26	–	µs
Bus release time	t_{BUF}	1.3	–	0.5	–	µs
Noise suppression time	t_I	–	50	–	50	ns
Power-off time	t_{POFF}	1	–	1	–	ms
Initialize time	t_{INIT}	0.2	–	0.2	–	ms

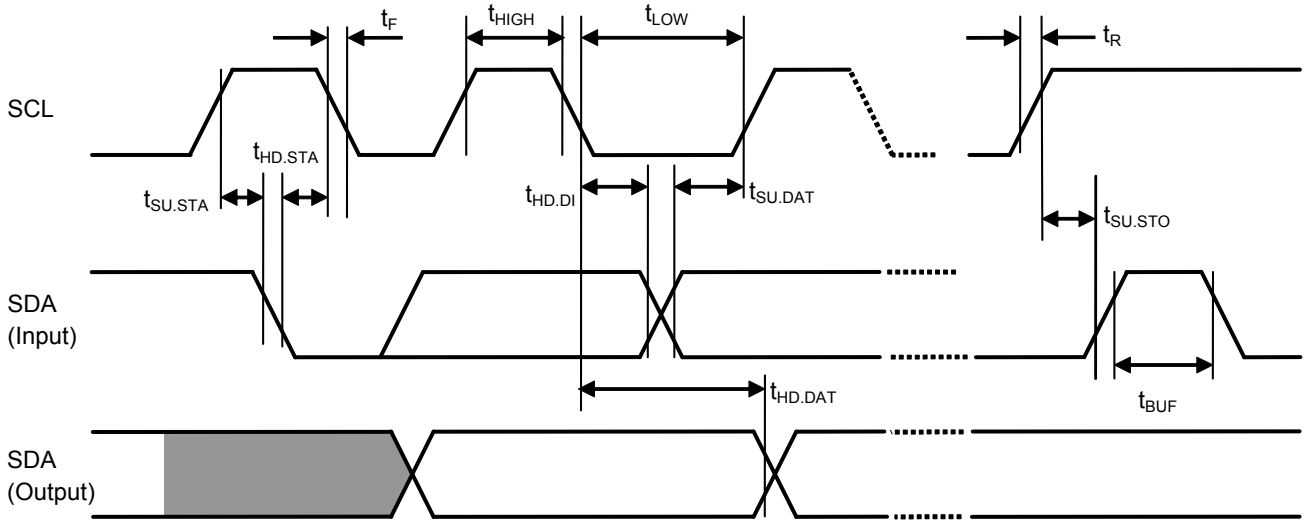


Figure 2 Bus Timing

Table 9

Item	Symbol	Ta = −20°C to +125°C V_{DD} = 1.7 V to 3.6 V		Unit
		Min.	Max.	
Write time	t_{WR}	−	5.0	ms

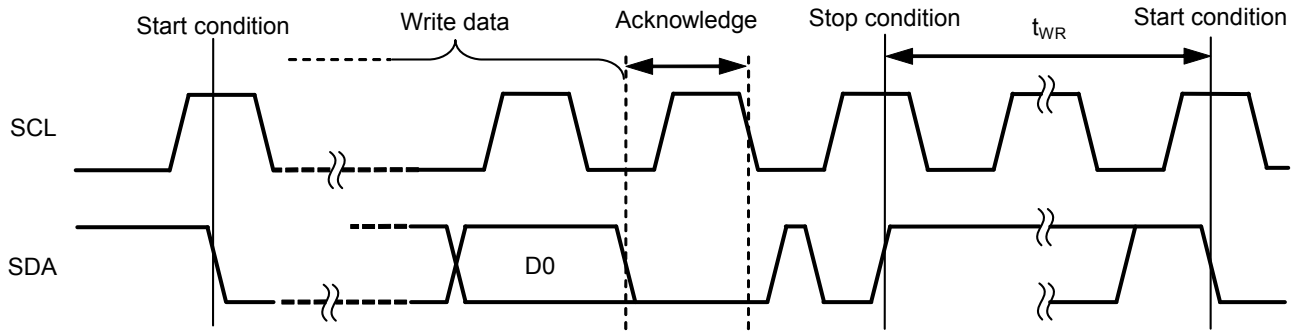


Figure 3 Write Cycle Timing

■ Pin Functions

1. VDD (Power supply) pin

The VDD pin is used to apply positive supply voltage. Regarding the applied voltage value, refer to "■ **Recommended Operation Conditions**". Set a bypass capacitor of about 0.1 μF between the VDD pin and the VSS pin for stabilization as close to IC as possible.

2. SA0, SA1 and SA2 (Select address input) pins

In this IC, to set the slave address, connect each of the SA0 pin, SA1 pin and SA2 pin to the VSS pin or the VDD pin. Therefore the users can set 8 types of slave address by a combination of the SA0 pin, SA1 pin, SA2 pin.
Comparing the slave address transmitted from the master device and one that you set, makes possible to select one slave address from other devices connected onto the bus.
Each of the SA0 pin, SA1 pin and SA2 pin has a built-in pull-down resistor. In open, the pin is set to the same status as it connected to the VSS pin.
The SA0 pin is used to detect the V_{HV} voltage, when decoding an SWPn or CWP instruction. Refer to **Table 10** for pin setting and device select code.

3. SDA (Serial data I/O) pin

The SDA pin is used for the bi-directional transmission of serial data. This pin is a signal input pin, and an Nch open-drain output pin.
In use, generally, connect the SDA line to any other device which has the open-drain or open-collector output with Wired-OR connection by pulling up to V_{DD} by a resistor.

4. SCL (Serial clock input) pin

The SCL pin is used for the serial clock input. Since the signals are processed at a rising or falling edge of the SCL clock, pay attention to the rising and falling time and comply with the specification.

■ Initial Delivery State

Initial delivery state of all address is "FFh". All write protects are cleared.

■ Operation

This IC behaves as a slave device in the 2-wire I^{2}C-bus protocol.
All operations are synchronized by the serial clock. Read and write operations are initiated by a start condition, generated by the master device. The start condition is followed by a device select code and read / write bit, and this IC generates an acknowledge bit.
The 7-bit device select code is constructed of 4-bit device type identifier code (DTIC) and 3-bit code which shows the state of the SA0 pin, SA1 pin, and SA2 pin. DTIC is a code to define functions.
When writing data to this IC, this IC generates an acknowledge bit during the 9th bit time, following the master device's 8-bit transmission. When data is read by the master device, the master device acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a master device which generates stop condition after an acknowledge for write, and after no acknowledge for read.
This IC has the timeout function. This IC shall not initiate clock stretching, which is an optional I^{2}C-bus feature.

1. Selecting function

This IC has a 4 K-bit E²PROM array. The E²PROM array is devided into two pages consisting of a lower 256-byte page and an upper 256-byte page, which change over by the set E²PROM page address order. Each page has two 128-byte blocks. Each block can be set to write-protected by software write protect function. Page write operation up to 16 bytes and sequential read operation are available.
Operation function is identified by DTIC. There are two types of DTIC. The E²PROM memory may be accessed using a DTIC of "1010b", and to perform the software write protection or the page address operations a DTIC of "0110b" is required.
All operations are inhibited to be performed during write time.
For more detail, refer to "■ **E²PROM Operation**".

2. Initialization operation after power-on

By a power-on-reset circuit, this IC initializes the internal circuit at the time of power-on. Perform the beginning (start condition) of the instruction transmission to this IC after the initialization by the power-on-reset circuit. Regarding the datails of power-on-reset, refer to "■ **Reset and Initialization**".

3. Start condition

Start is identified by a "H" to "L" transition of the SDA line while the SCL line is stable at "H".
Every operation begins from a start condition.

4. Stop condition

Stop is identified by a "L" to "H" transition of the SDA line while the SCL line is stable at "H".
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and this IC initiates a write cycle.

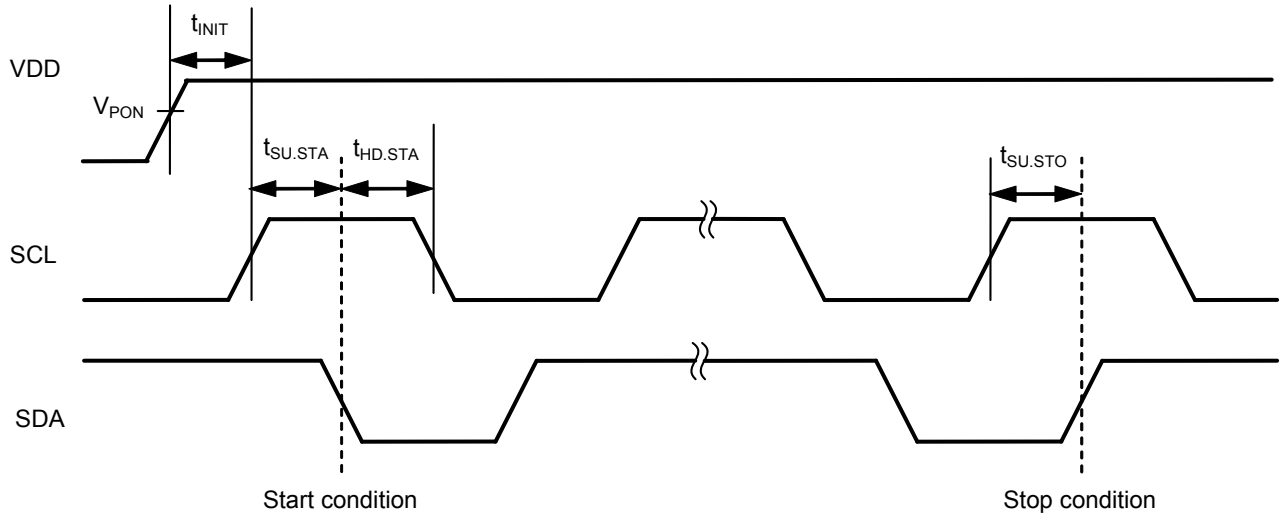


Figure 4 Start / Stop Conditions after Power-on

5. Data transmission

Changing the SDA line while the SCL line is "L", data is transmitted.
Changing the SDA line while the SCL line is "H", a start or stop condition is recognized.

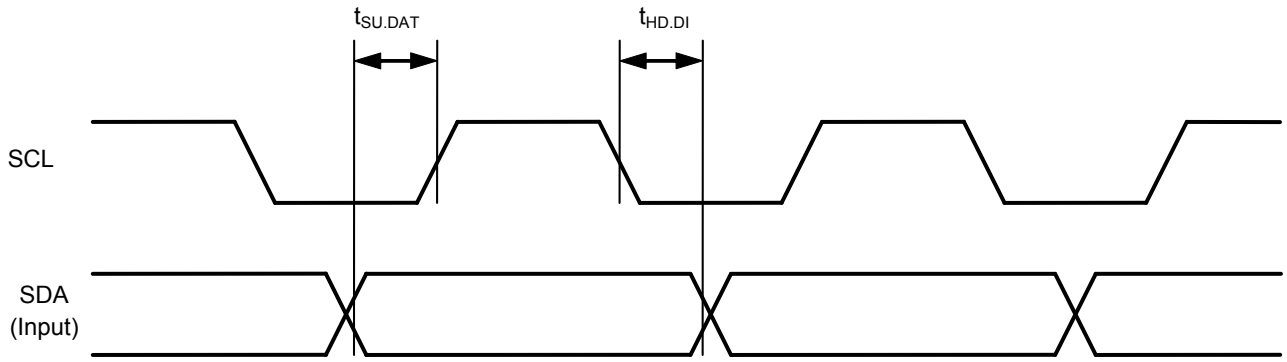


Figure 5 Data Transmission Timing

6. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When a write cycle is in progress, this IC does not generate an acknowledge.

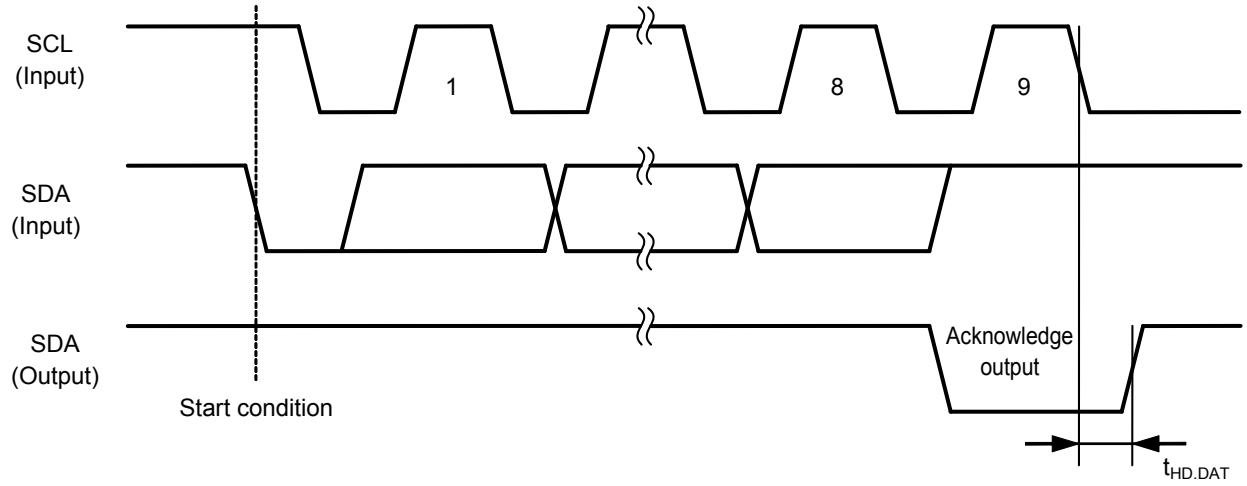


Figure 6 Acknowledge Output Timing

7. Device addressing

To start communication, the master device on the system generates a start condition to the slave device. Following this, the master device sends the device select code.

Table 10 Device Select Code

Instruction	Device Type Identifier				Select Address Signal			R/$\overline{W}$	SA Pin		
	B7	B6	B5	B4	B3	B2	B1	B0	SA2	SA1	SA0
Read/write E²PROM*1	1	0	1	0	SA2	SA1	SA0	R/$\overline{W}$	SA2	SA1	SA0
Set write protection, block 0 (SWP0)	0	1	1	0	0	0	1	0	–*2	–*2	V_{HV}
Set write protection, block 1 (SWP1)	0	1	1	0	1	0	0	0	–*2	–*2	V_{HV}
Set write protection, block 2 (SWP2)	0	1	1	0	1	0	1	0	–*2	–*2	V_{HV}
Set write protection, block 3 (SWP3)	0	1	1	0	0	0	0	0	–*2	–*2	V_{HV}
Clear all write protection (CWP)	0	1	1	0	0	1	1	0	–*2	–*2	V_{HV}
Read SWP0 status (RPS0)	0	1	1	0	0	0	1	1	–*2	–*2	–*2
Read SWP1 status (RPS1)	0	1	1	0	1	0	0	1	–*2	–*2	–*2
Read SWP2 status (RPS2)	0	1	1	0	1	0	1	1	–*2	–*2	–*2
Read SWP3 status (RPS3)	0	1	1	0	0	0	0	1	–*2	–*2	–*2
Set page address to 0 (SPA0)	0	1	1	0	1	1	0	0	–*2	–*2	–*2
Set page address to 1 (SPA1)	0	1	1	0	1	1	1	0	–*2	–*2	–*2
Read page address (RPA)	0	1	1	0	1	1	0	1	–*2	–*2	–*2

***1.** Slave addresses (SA2, SA1, SA0) are compared by the select address input pins (SA2, SA1, SA0) of a memory device with the address value which is set beforehand.

***2.** Connected to the VSS pin or VDD pin.

The device select code consists of a 4-bit device type identifier, and 3-bit select signals (SA2 pin, SA1 pin, SA0 pin). To address the memory array, the 4-bit device type identifier is "1010b"; to access the write-protection settings and the page address settings, it is "0110b".

Up to eight devices can be connected on a single I²C-bus. Address select signals (SA2 pin, SA1 pin, SA0 pin) should be set on each device, respectively. The device continues the operation only when the received device select code matches the address select signal.

The SWPn, CWP, RPSn write protect commands and SPAn, RPA page address commands do not use the select address, therefore all devices on the I²C-bus will act on these commands simultaneously.

The 8th bit is the read / write bit (R/$\overline{W}$). This bit is set to "1" for read and "0" for write operations. If a match occurs on the device select code, the corresponding device gives an acknowledge on serial data (SDA) during the 9th bit time. If the device does not match the device select code, This IC goes into standby mode automatically.

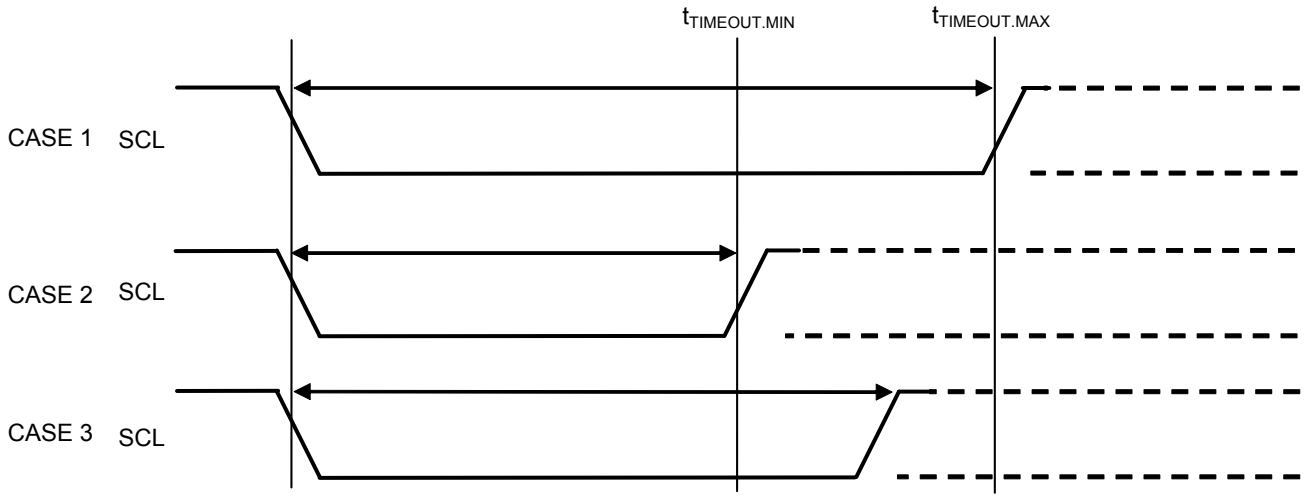
Table 11 Operating Modes

Mode	R/$\overline{W}$	Byte	I/O Sequence
Current address read	1	1	Start, device select, R/$\overline{W}$ = 1, data, stop
Random read	0	1	Start, device select, R/$\overline{W}$ = 0, address
	1		Restart, device select, R/$\overline{W}$ = 1, data, stop
Sequencial read	1	≥ 1	Similar to current address read or random read
Byte write	0	1	Start, device select, R/$\overline{W}$ = 0, address, data, stop
Page write	0	≤ 16	Start, device select, R/$\overline{W}$ = 0, address, data, stop
SWPn and CWP	0	2	Start, device select, R/$\overline{W}$ = 0, X*1, X*1, stop
Set page address	0	2	Start, device select, R/$\overline{W}$ = 0, X*1, X*1, stop
Read page address	1	2	Start, device select, R/$\overline{W}$ = 1, X*1, X*1, stop

***1.** X: Don't care

8. Timeout

This IC has the timeout function. If the SCL stays "L" for the time $t_{TIMEOUT}$ or more, this IC resets the serial interface and returns to standby mode. If the SCL stays "L" for less than the $t_{TIMEOUT}$, this IC does not reset the serial interface. The $t_{TIMEOUT}$ is 30 ms typ.



CASE1: SCL clock time "L" ≥ $t_{TIMEOUT.MAX}$, this IC will reset the bus communication and return to standby mode.
CASE2: SCL clock time "L" < $t_{TIMEOUT.MIN}$, this IC will not reset the bus communication.
CASE3: $t_{TIMEOUT.MIN}$ ≤ SCL clock time "L" < $t_{TIMEOUT.MAX}$, this IC may or may not reset the bus communication.

Figure 7 The Examples of the Timeout Timing

When this IC is not in the range of the clock frequency specified by AC characteristics, it may not perform communication normally.

■ E²PROM Operation

1. Write

1. 1 Byte write

When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, this IC generates an acknowledge.
This IC then receives an 8-bit word address and responds with an acknowledge. After this IC receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.
When the certain word address is protected by the write instruction, this IC does not generate an acknowledge after data byte coding, and write operation is not performed.
During the write operation to this IC, all operations are inhibited to be performed and does not send back an acknowledge.

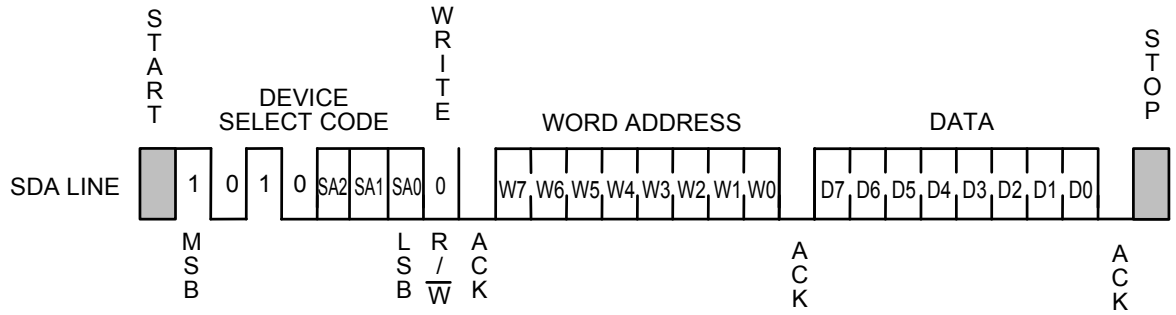


Figure 8 Byte Write

1. 2 Page write

The page write mode allows up to 16 bytes to be written in a single write operation in this IC.
Its basic process to transmit data is as same as byte write, but it operates page write by sequentially receiving 8-bit write data as much data as the page size has.
When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, it generates an acknowledge. Then this IC receives an 8-bit word address, and responds with an acknowledge. After this IC receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. This IC repeats reception of 8-bit write data and generation of acknowledge in succession. This IC can receive as many write data as the maximum page size.
Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.

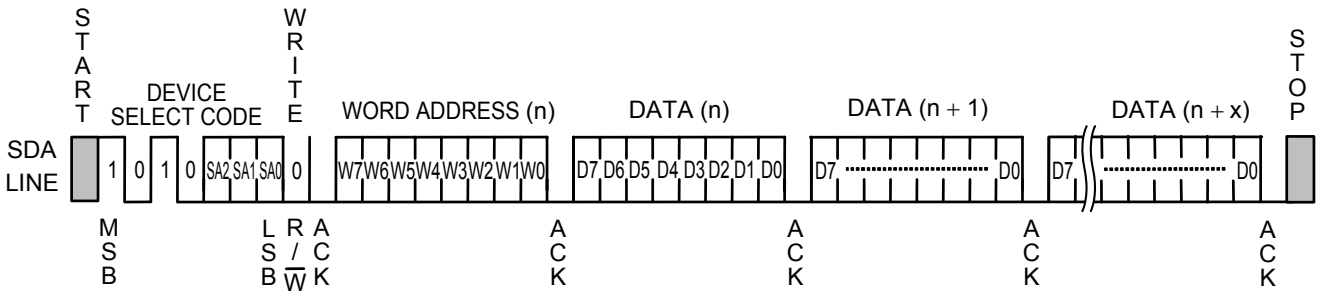


Figure 9 Page Write

The lower 4 bits of the word address are automatically incremented every time when it receives 8-bit write data. If the size of the write data exceeds 16 bytes, the higher 4 bits (W7 to W4) of the word address remain unchanged, and the lower 4 bits are rolled over and the last 16-byte data that this IC received will be overwritten.

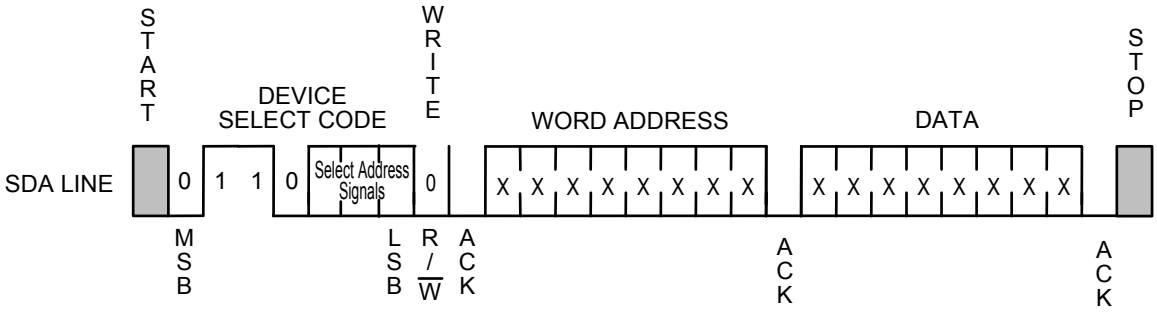
1. 3 Software write protect

This IC has set write protection for block n (SWPn), clear write protection for all blocks (CWP) and read protection status for block n (RPSn).
There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = word addresses 00h to 7Fh, page address = 0
- Block 1 = word addresses 80h to FFh, page address = 0
- Block 2 = word addresses 00h to 7Fh, page address = 1
- Block 3 = word addresses 80h to FFh, page address = 1

1. 3. 1 Set write protect (SWPn) and clear write protect (CWP)

If the software write protect has been set with the SWPn instruction, the block n in memory is write-protected.
The four independent blocks are protected by SWPn instructions. The write-protected block can be cleared with the CWP instruction.
The CWP instruction clears write-protection for all blocks, therefore the CWP instruction can not clear write-protection for each block.
The SWPn and CWP instructions have the same format as a byte write instruction, but have a different device select code. Like the byte write instruction, it is followed by an address byte and a data byte, but in this case the contents can be set in all "Don't care". In the instructions of SWPn and CWP, be sure to apply the high voltage of V_{HV} to the SA0 pin, and input "H" or "L" to the SA1 pin and SA2 pin.
The device select code for each block is shown in **Table 10**.



Remark X: Don't care

Figure 10 Software Write Protect

1. 3. 2 Read protection status (RPSn)

The RPSn are the instructions to find the write protection status in block n. If the block is not protected by SWPn instruction, this IC generates an acknowledge after the device receives the device select code of the block. If a certain block is protected by SWPn instruction, this IC does not generate an acknowledge after the device receives the device select code of the block.

1. 3. 3 Set page address (SPAn)

The SPAn are the instructions to select the lower 256-byte page (SPA0) or the higher 256-byte page (SPA1). The page address selects the lower 256 bytes (SPA0) after power-on reset.

1. 3. 4 Read page address (RPA)

The RPA are the instructions to find the current page address status. If the current page address is "0", this IC generates an acknowledge after the device receives the device select code. If the current page address is "1", this IC does not generate an acknowledge.

Table 12 Acknowledge for Write Instruction (R/$\overline{W}$ bit = 0)

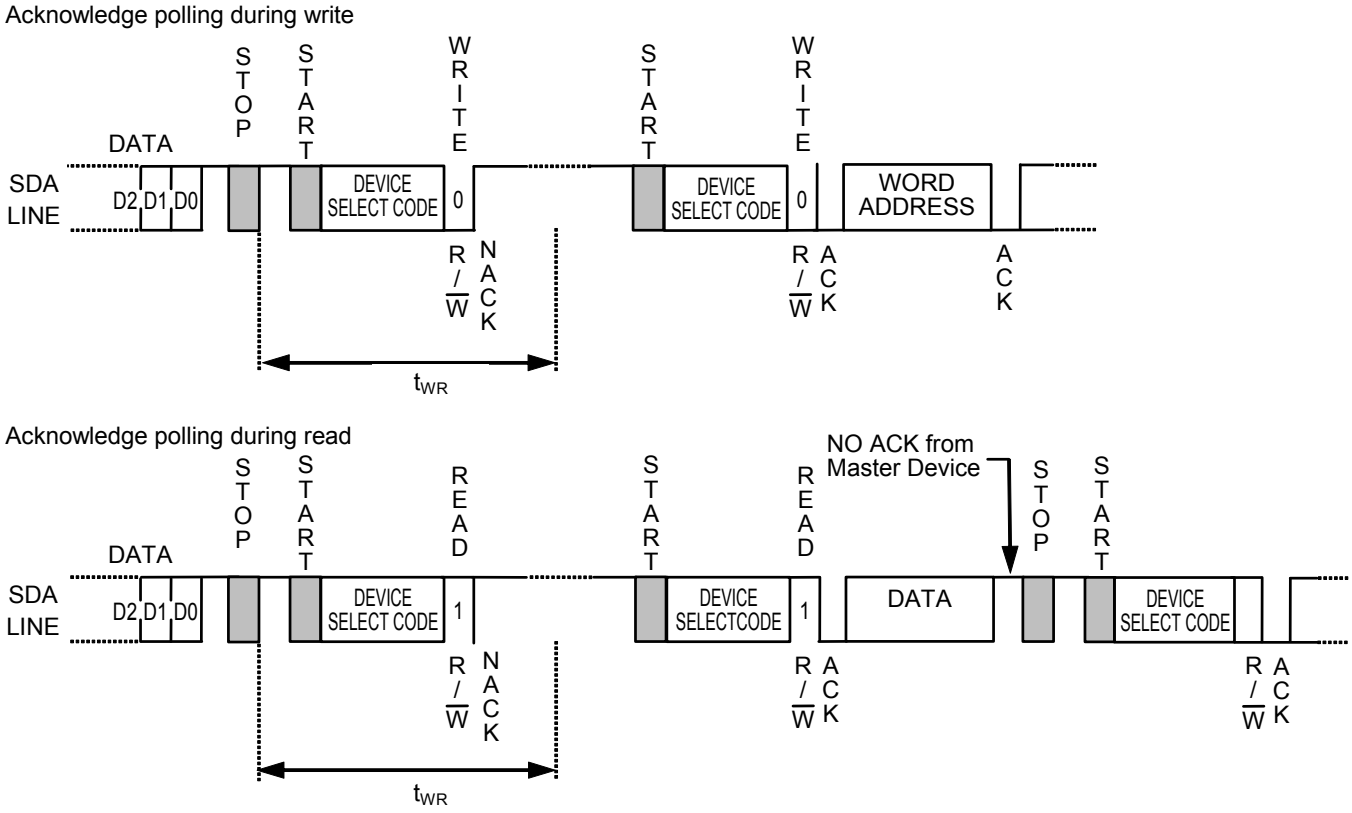
Status	Instruction	ACK Output	Word Address	ACK Output	Data	ACK Output	Write
Software Write Protect (SWPn)	SWPn in protected block	No	Don't care	No	Don't care	No	No
	SWPn in no protected block	Yes	Don't care	Yes	Don't care	Yes	Yes
	CWP	Yes	Don't care	Yes	Don't care	Yes	Yes
	Page write or byte write in protected block	Yes	Word address	Yes	Don't care	No	No
	Page write or byte write in no protected block	Yes	Word address	Yes	Data	Yes	Yes
No Software Write Protect	SWPn or CWP	Yes	Don't care	Yes	Don't care	Yes	Yes
	Page write or byte write	Yes	Word address	Yes	Data	Yes	Yes

Table 13 Acknowledge for Read Instruction (R/$\overline{W}$ bit = 1)

Status	Instruction	ACK Output	Word Address	ACK Output	Data	ACK Output
Software Write Protect (SWPn)	RPSn	No	Don't care	No	Don't care	No
No Software Write Protect	RPSn	Yes	Don't care	No	Don't care	No

1. 4 Acknowledge polling

Acknowledge polling is used to know the completion of the write cycle in this IC.
After this IC receives a stop condition and once starts the write cycle, all operations are forbidden and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in this IC by detecting a response from the slave device after transmitting the start condition, the device address and the read / write instruction code to this IC, namely to the slave devices.
That is, if this IC does not generate an acknowledge, the write cycle is in progress and if this IC generates an acknowledge, the write cycle has been completed.
It is recommended to use the read instruction "1" as the read / write instruction code transmitted by the master device.



Remark Users are able to input data after acknowledge output in acknowledge polling during write.
Users are able to read data after acknowledge output in acknowledge polling during read.
However, after that users input the write instruction, a start condition may not be input during data output. Input a stop condition and the next instruction after acknowledge output and data output.

Figure 11 Usage Example of Acknowledge Polling

2. Read

2. 1 Current address read

Either in writing or in reading this IC holds the last accessed memory address. The memory address is maintained when the instruction transmission is not interrupted, and the memory address is maintained as long as the power voltage does not decrease less than the power-on reset threshold voltage (V_{PON}).
The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in this IC. This is called "current address read".
In the following the address counter in this IC is assumed to be "n".
When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition, it responds with an acknowledge.
Next an 8-bit data at the address "n" is sent from this IC synchronous to the SCL clock. The address counter is incremented and the content of the address counter becomes n + 1. The master device outputs stop condition not an acknowledge, the reading of this IC is ended.

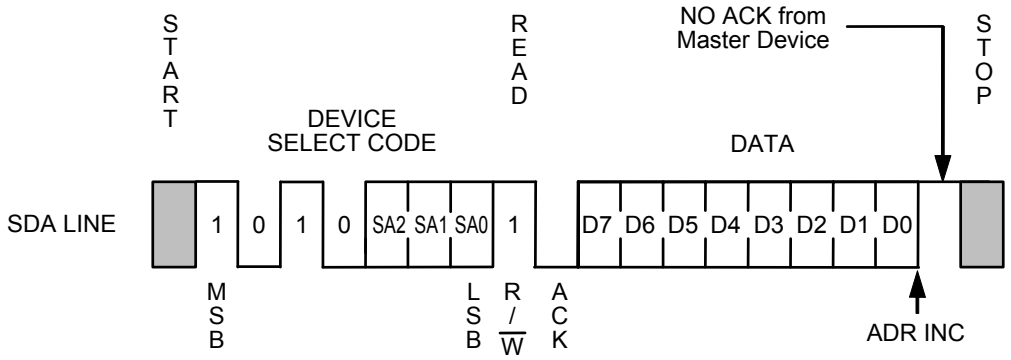


Figure 12 Current Address Read

Attention should be paid to the following point on the recognition of the address pointer in this IC.
In read, the memory address counter in this IC is automatically incremented after output of the 8th bit of the data. In write, on the other hand, the higher bits of the memory address (the higher 4 bits of the word address) are left unchanged and are not incremented.

2. 2 Random read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the memory address into the address counter.
When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "0" following a start condition, it responds with an acknowledge.
This IC then receives an 8-bit word address and responds with an acknowledge. The memory address is loaded to the address counter in this IC by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in byte write and in page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1", following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from this IC synchronously with the SCL clock. The master device outputs stop condition not an acknowledge, the reading of this IC is ended.

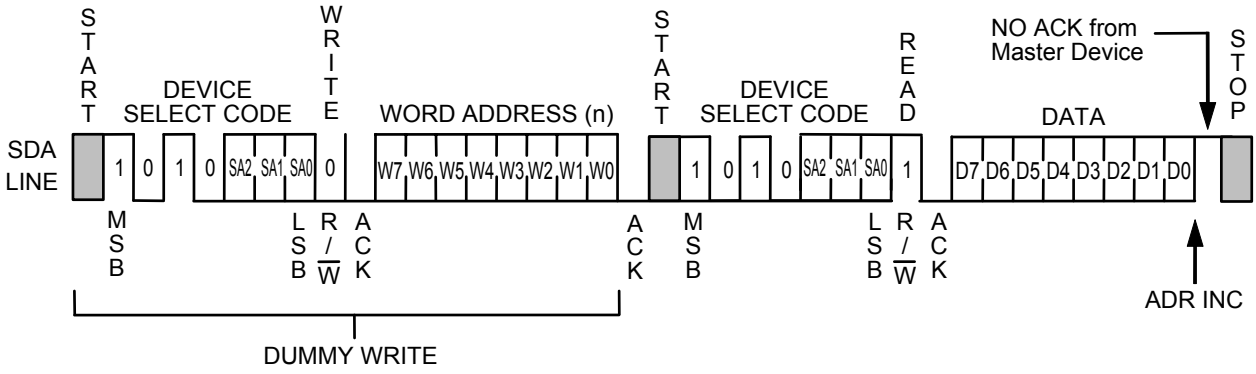


Figure 13 Random Read

2. 3 Sequential read

When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition both in current address read and random read, it responds with an acknowledge.
When an 8-bit data is output from this IC synchronously with the SCL clock, the address counter is automatically incremented.
When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in this IC incremented and makes it possible to read data in succession. This is called sequential read.
The master device outputs stop condition not an acknowledge, the reading of this IC is ended.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first word address of same page address.

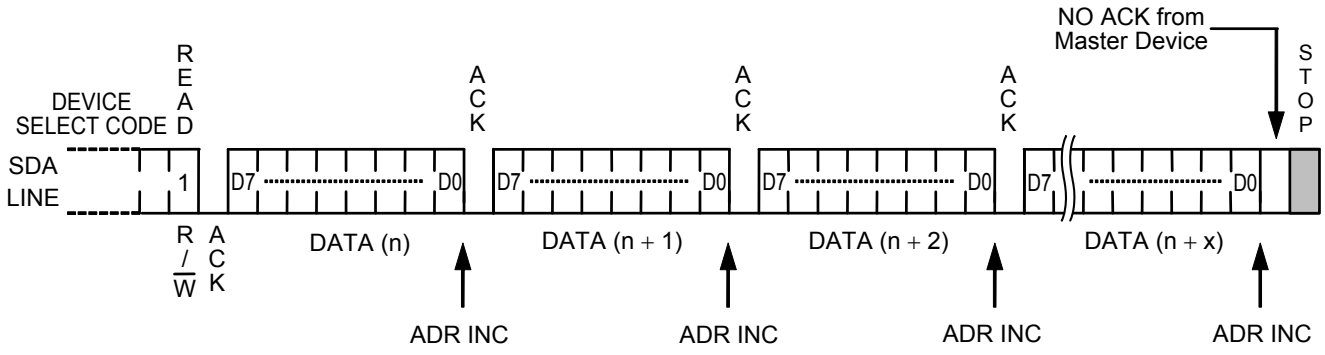


Figure 14 Sequential Read

■ Reset and Initialization

This IC has a power-on reset circuit which prevents malfunction, cancels write at power-on.
At power-on status, the master device should not transfer the data from the time that the power supply voltage reaches V_{DD} min. to t_{INIT}. And at power-down, all registers are reset when the power supply voltage drops below V_{POFF}. Therefore if the power supply voltage remains below V_{POFF} for t_{POFF}, all operations of this IC are reset.
Operating this IC will be required to apply the stable power supply voltage (V_{DD}). The power supply voltage must remain stable until the end of the transmission of the data and, for a write instruction.

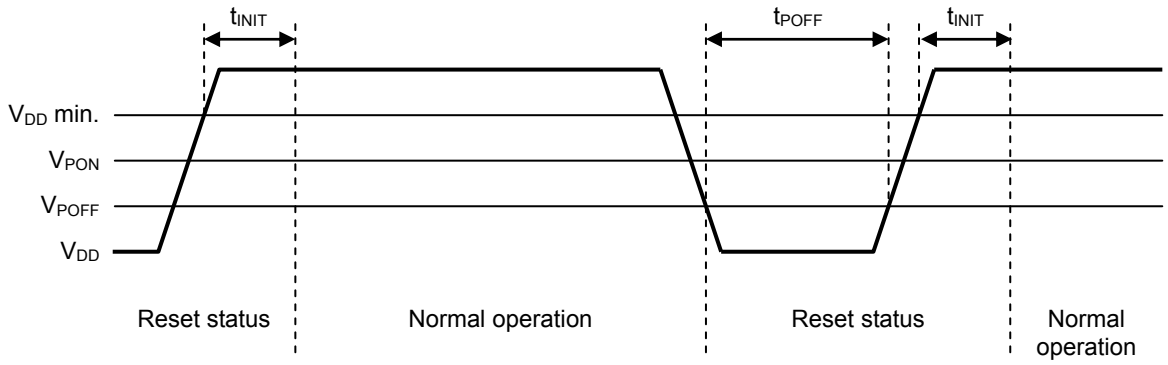


Figure 15 Operation when Power Supply Voltage Drops and Power-on

■ Usage

1. A pull-up resistor to SDA I/O pin and SCL input pin

In consideration of I^{2}C-bus protocol function, the SDA I/O pin and SCL input pin should be connected with a pull-up resistor. This IC cannot transmit normally without using a pull-up resistor.

In case that the SCL input pin of this IC is connected to the Nch open-drain output pin of the master device, connect the SCL pin with a pull-up resistor. As well, in case the SCL input pin of this IC is connected to the tri-state output pin of the master device, connect the SCL pin with a pull-up resistor in order not to set it in "High-Z". This prevents this IC from error caused by an uncertain output (High-Z) from the tri-state pin when resetting the master device during the voltage drop.

2. Equivalent circuits of input pin and I/O pin

The SCL pin and the SDA pin of this IC do not have a built-in pull-down or pull-up resistor. Each of the SA0 pin, SA1 pin and SA2 pin has a built-in pull-down resistor. The SDA pin is an open-drain output. The followings are equivalent circuits of the pins.

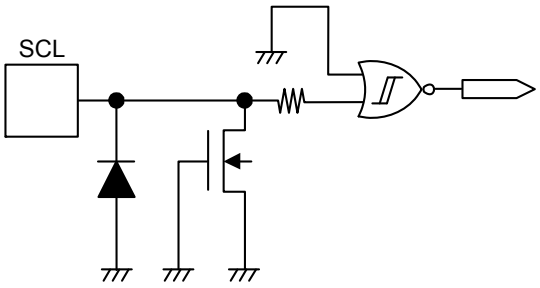


Figure 16 SCL Pin

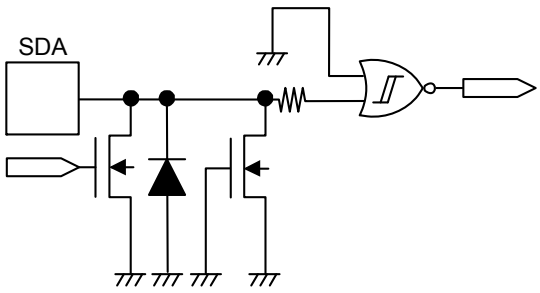


Figure 17 SDA Pin

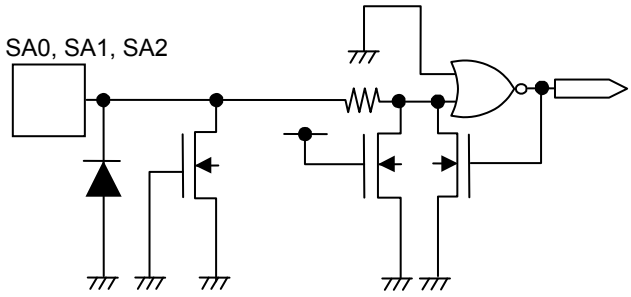


Figure 18 SA0, SA1, SA2 Pin

3. Acknowledge check

The I^{2}C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the master device and this IC. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check with the master device.

4. SDA pin and SCL pin noise suppression time

This IC includes a built-in low-pass filter at the SDA pin and the SCL pin to suppress noise. If the power supply voltage is 2.2 V, noise with a pulse width of 75 ns or less can be suppressed.
For details of the assurable value, refer to noise suppression time (t_I) in **Table 8** in "**■ AC Electrical Characteristics**".

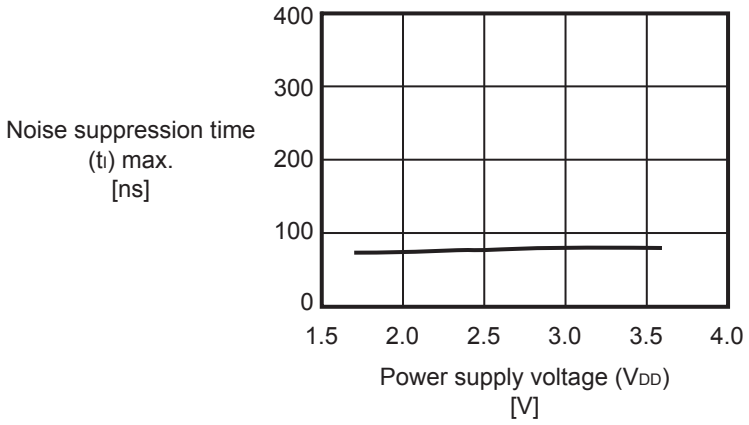


Figure 19 Noise Suppression Time for SDA Pin and SCL Pin

5. Operation when inputting stop condition during write

This IC does write operation only when it receives data of 1 byte or more and receives a stop condition immediately after an acknowledge output.
Refer to **Figure 20** for details.

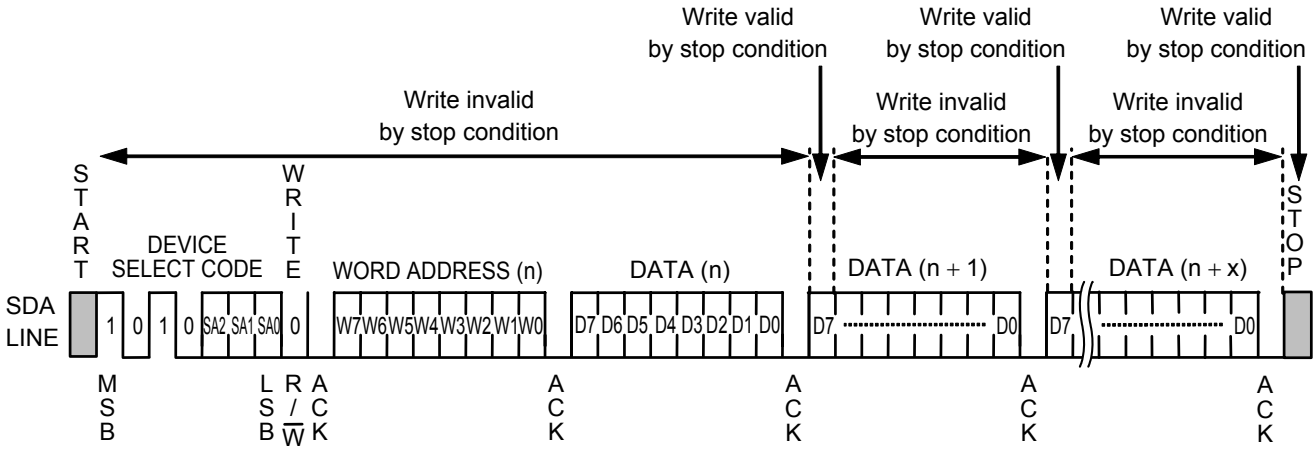


Figure 20 Write Operation by Inputting Stop Condition during Write

6. Command cancel by start condition

By a start condition, users are able to cancel command which is being input. However, users are not able to input a start condition when this IC is outputting "L". When users cancel the command, there may be a case that the address will not be identified. Use random read for the read operation, not current address read.

■ Precautions

- Do not operate these ICs in excess of the absolute maximum ratings. Attention should be paid to the power supply voltage, especially. The surge voltage which exceeds the absolute maximum ratings can cause latch-up and malfunction. Perform operations after confirming the detailed operation condition in the data sheet.

- Operations with moisture on this IC's pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking this IC up from low temperature tank during the evaluation. Be sure that not remain frost on this IC's pin to prevent malfunction by short-circuit.
  Also attention should be paid in using on environment, which is easy to dew for the same reason.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

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