REAL-TIME CLOCK S-3510 Series

The S-3510 is a series of CMOS real-time clock ICs that inputs/outputs serial clock or calendar data into/from the CPU.

■ Features

- Operating power supply: 1.7 V to 5.5 V
- Low current consumption: 1.2 µA typ. at 3.0 V
  (S-3510AFFJA: 2.0 µA typ. at 3.0 V)
- BCD output of second, minute, hour, day, date, month and year
- Easy serial interface to CPU with 3 lines (SIO, SCK, and CS)
- Built-in automatic calendar, automatic leap-year calculation up to 2099.
- Built-in voltage detector
- Built-in constant voltage circuit
- Built-in 32 kHz oscillation circuit (Built-in Cg/Cd, or Cd only)

■ Applications

- Video cameras
- FAXes
- Cellular phones
- Printers

■ Package

- 8-Pin SOP (Pin pitch : 1.27 mm) (Package drawing code: FJ008-D)

■ Block Diagram

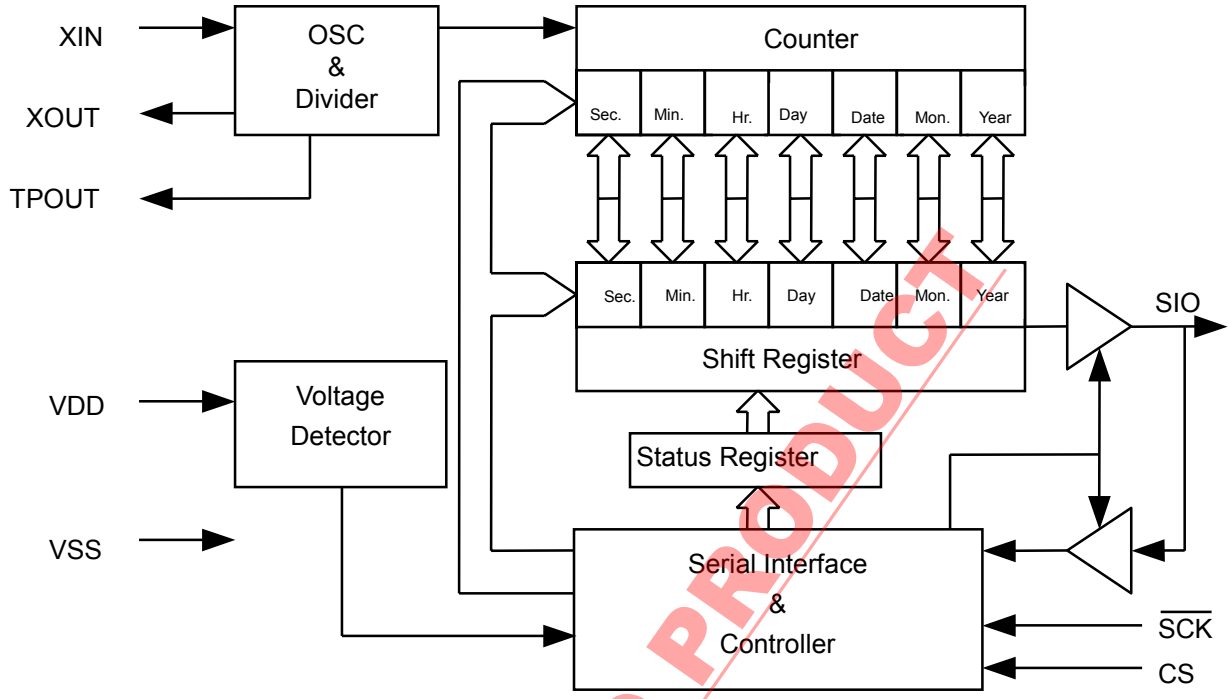


Figure 1

■ Pin Assignment

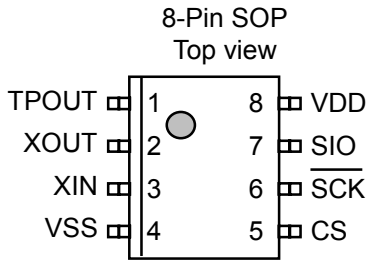


Figure 2

■ Pin Function

Table 1

No.	Name	Function
1	TPOUT	Standard signal output (Nch open-drain output or CMOS output)
2	XOUT	Connects to the X'ftal resonator (f=32,768 Hz) Built-in Cg/Cd, or Cd only
3	XIN	
4	VSS	Power supply (GND)
5	CS	Chip select input (Built-in pull-down resistance) : "H": The SIO pin is capable of inputting/outputting data. The SCK pin is capable of accepting the input. "L": The SIO pin is at Hi-Z. The SCK pin is not capable of accepting the input.
6	$\overline{\text{SCK}}$	Clock input : Inputs and outputs data from the SIO pin in synchronization with the clock. The clock cannot be accepted when the CS pin is "L".
7	SIO	Serial data input/output : When the CS is "L", the SIO pin is at "Hi-Z". When the CS pin changes from "L" to "H", it serves as the input pin. The SIO pin is assigned to the input or output pin according to the next command data. The type of output is either Nch open-drain or CMOS depending upon the model of the IC you use.
8	VDD	Positive power supply

■ Command Configuration

Table 2

Command	Code	Note
READ 1(Data Read)	1 1 1 0 × × × ×	Output from the year data
READ 2(Data Read)	1 1 1 1 × × × ×	Output from the day data
WRITE 1(Data Write)	1 0 0 1 × × × ×	Input from the year data
WRITE 2(Data Write)	1 0 0 0 × × × ×	Input from the day data
STATUS WRITE	1 0 1 1 D3 D2 D1 D0	Status write
RESET	1 0 1 0 1 0 1 0	Initialization
TEST START	1 1 0 1 0 1 0 1	Test mode start
TEST END	1 1 0 1 1 0 1 0	Test mode end

■ Data Configuration

The S-3510 series is provided with a timer data BCD (Binary Coded Decimal) display*1 device and an automatic calendar. A set of flags are configured as follows:

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Year data (0 to 99)
0	0	0	M4	M3	M2	M1	M0	Month data (1 to 12)
0	0	D5	D4	D3	D2	D1	D0	Date data (1 to 31)
$\overline{12/24}$	$\overline{TPEN}$	TPF	FRE	TEST	W2	W1	W0	Status and day data (1 to 7)
$\overline{AM/PM}$	0	H5	H4	H3	H2	H1	H0	Hour data (0 to 23 or 0 to 11) and flags
POW	m6	m5	m4	m3	m2	m1	m0	Minute data (0 to 59) and flags
BLD	S6	S5	S4	S3	S2	S1	S0	Second data (0 to 59) and flags

***1.** $\overline{AM}$/PM Flag : When writing in 12-hour display mode, always input 0 for AM and 1 for PM. In 24-hour display mode, it is unnecessary as both 1 and 0 are ignorged. However, when reading the time in either display mode 0 is read as AM 1 as PM.

BLD Flag : When a decrease in the voltage is detected, it is set to 1. This is valid during reading and is invalid during writing.

POW Flag : 1 is set at the power on, and cleared through the RESET command. This flag is ingored during writing.

TEST Flag When the test mode is set, it is set to 1. When the bit is 1, always use the TEST END or RESET command to set to 0. This bit is valid for reading and ignored during writing.

■ Ordering Information

Table 3

Model No.	SIO output	TPOUT output	TPOUT output form	Oscillation circuit capacity
S-3510ANFJA	Nch open-drain	Selection of 1 H_Z / 32,768 H_Z by command	Nch open-drain	Internal Cg, Cd
S-3510ACFJA	CMOS	Selection of 1 H_Z / 32,768 H_Z by command	Nch open-drain	Internal Cg, Cd
S-3510ADFJ	CMOS	32,768 H_Z	Nch open-drain	External Cg, Internal Cd
S-3510AEFJ	Nch open-drain	32,768 H_Z	Nch open-drain	Internal Cg, Cd
S-3510AFFJ	CMOS	32,768 H_Z	CMOS	External Cg, Internal Cd

■ Absolute Maximum Ratings

Table 4

(Unless otherwise specified : Ta=25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	–	V_{SS}–0.3 to V_{SS}+7.0	V
Input Voltage	V_{IN1}	$\overline{SCK}$, CS, SIO	V_{SS}–0.3 to V_{SS}+7.0	V
	V_{IN2}	SIO (CMOS output)	V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	TPOUT, SIO	V_{SS}–0.3 to V_{SS}+7.0	V
Operating temperature	T_{opr}	V_{DD}=3.0 V	–30 to +80	°C
Storage temperature	T_{stg}	–	–55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 5

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	1.7	3.0	5.5	V
Operating temperature	T_{opr}	–20	–	+70	°C

■ Oscillation Characteristics

Table 6

(Unless otherwise specified : Ta=25°C, V_{DD}=3.0 V, Xtal resonator: SII Quartz Techno Ltd., DS-VT-200 (R_1=30 kΩ, C_L*1=6 pF, 32,768 Hz))

Parameter	Symbol	Conditions	Standard			Unit
			Min.	Typ.	Max.	
Oscillation start voltage	V_{STA}	Within 10 s	1.7	–	5.5	V
Oscillation start time	T_{STA}	–	–	–	3.0	s
Frequency deviation between ICs	δIC	–	–10	–	+10	ppm
Frequency voltage deviation	δV	V_{DD}=1.7 V to 5.5 V	–3	–	+3	ppm/V
Input capacitance	C_{IN1}*2	Applied to X_{IN}	–	12	–	pF
	C_{IN2}*3	Applied to X_{IN}	–	8	–	pF
Output capacitance	C_{OUT}*4	Applied to X_{OUT}	–	12	–	pF

***1.** The load capacitance (C_L) changes depending upon the capacitance of the PCB mounted onto the IC. Adjust the load capacitance.
***2** Applied to S-3510ANFJx, S-3510ACFJx, S-3510AEFJA (Internal)
***3** Applied to S-3510ADFJA, S-3510AFFJA (External)
***4** Applied to S-3510ANFJx, S-3510ACFJx, S-3510AEFJA, S-3510ADFJA, S-3510AFFJA (Internal)

■ DC Characteristics

Table 7

Unless otherwise specified: Ta=25 °C, V_{DD}=3.0 V, X'tal resonator: SII Quartz Techno Ltd., DS-VT-200 (R_1=30 kΩ, C_L=6 pF, 32,768 Hz)

Parameter	Symbol	Applicable pin	Conditions	Standard			Unit
				Min.	Typ.	Max.	
Operating voltage range	V_{DD}	–	Ta=–20°C to +70°C, Communications when SCK=100 kHz	1.7	3.0	5.5	V
Power current consumption	I_{DD1}	–	CS=0 V. No output load. Communication inhibit*1	–	1.2	2.0	µA
		–	CS=0 V. No output load. Communication inhibit*2	–	2.0	3.5	µA
	I_{DD2}	–	The current which flows through the CS is not included. No output load. Communications when SCK=100 kHz*3	–	10	30	µA
		–	The current which flows through the CS is not included. No output load. Communications when SCK=100 kHz*4	–	30	60	µA
Input leak current	I_{IHL1}	SIO, SCK	V_{IN}=5.5 V*5	–0.5	–	0.5	µA
	I_{IHL2}	SIO, SCK	V_{IN}=V_{DD}*6	–0.5	–	0.5	µA
	I_{ILL}	SIO, SCK, CS	V_{IN}=0 V	–0.5	–	0.5	µA
Input current	I_{IH2}	CS	V_{IN}=5.5 V	–	10	30	µA
	I_{IH3}	CS	V_{IN}=0.4 V	30	100	300	µA
Input voltage	V_{IH}	–	–	0.8 ×V_{DD}	–	–	V
	V_{IL}	–	–	–	–	0.2 ×V_{DD}	V
Output current	I_{OL1}	TPOUT	V_{IN}=0.4 V	200	–	–	µA
	I_{OL2}	SIO	V_{IN}=0.4 V	500	–	–	µA
	I_{OH1}	TPOUT	V_{IN}=2.6 V*7	–	–	–200	µA
	I_{OH2}	SIO	V_{IN}=2.6 V*8	–	–	–500	µA
Voltage detection voltage	V_{DET}	–	Ta=25°C	1.8	2.0	2.2	V
		–	Ta=–20°C to +70°C	1.72	–	2.3	V
BLD current consumption	I_{BLD}	–	Ta=–20°C to +70°C	–	0.3	1.0	µA

***1.** Applied to the products except S-3510AFFJA
***2.** Applied to S-3510AFFJA
***3.** Applied to 3510ANFJx, S-3510ADFJA, S-3510AFFJA
***4.** Applied to S-3510ACFJx, S-3510ADFJA, S-3510AFFJA
***5.** Applied to S-3510ANJFx, S-3510AEFJA
***6.** Applied to S-3510ACFJx, S-3510ADFJA, S-3510AFFJA
***7.** Applied to S-3510AFFJA
***8.** Applied to S-3510ACFJx, S-3510ADFJA, S-3510AFFJA

■ AC Characteristics 1 (S-3510ANFJx, S-3510AEFJA, R_{L1}=30 kΩ, C_{L1}=50 pF)

Conditions: V_{DD}=1.7 V to 5.5 V, Ta=−20°C to 70°C, Interface voltage Vcc=5.0 V
Input: V_{IH}=0.8×V_{DD}, V_{IL}=0.2×V_{DD}, Output: V_{OH}=0.8×V_{CC}, V_{OL}=0.2×V_{CC}

Table 8

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse width	t_{SCK}	5	–	250000	µs
Setup time prior to the rising of the CS	t_{DS}	1	–	–	µs
Hold time after the rising of the CS	t_{CSH}	1	–	–	µs
Input data setup time	t_{ISU}	1	–	–	µs
Input data hold time	t_{IHO}	1	–	–	µs
Output data determination time	t_{ACC}	–	–	3.5	µs
Setup time prior to the falling of the CS	t_{CSS}	1	–	–	µs
Hold time after the falling of the CS	t_{DH}	1	–	–	µs
Input rising/falling time	t_R, t_F	–	–	0.1	µs

■ AC Characteristics 2 (S-3510ACFJx, S-3510ADFJA, S-3510AFFJA, C_{L1}=50 pF)

Conditions : V_{DD}=5.0±0.5 V, Ta=−20°C to 70°C
Input: V_{IH}=0.8×V_{DD}, V_{IL}=0.2×V_{DD}, Output: V_{OH}=0.8×V_{DD}, V_{OL}=0.2×V_{DD}

Table 9

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse width	t_{SCK}	0.5	–	250000	µs
Setup time prior to the rising of the CS	t_{DS}	0.1	–	–	µs
Hold time after the rising of the CS	t_{CSH}	0.1	–	–	µs
Input data setup time	t_{ISU}	0.1	–	–	µs
Input data hold time	t_{IHO}	0.1	–	–	µs
Output data determination time	t_{ACC}	–	–	0.3	µs
Setup time prior to the falling of the CS	t_{CSS}	0.1	–	–	µs
Hold time after the falling of the CS	t_{DH}	0.1	–	–	µs
Input rising/falling time	t_R, t_F	–	–	0.05	µs

■ AC Characteristics 3 (S-3510ACFJx, S-3510ADFJA, S-3510AFFJA, C_{L1}=50 pF)

Conditions : V_{DD}=3.0±0.6 V, Ta=−20°C to 70°C
Input: V_{IH}=0.8×V_{DD}, V_{IL}=0.2×V_{DD}, Output: V_{OH}=0.8×V_{DD}, V_{OL}=0.2×V_{DD}

Table 10

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse width	t_{SCK}	1.0	–	250000	µs
Setup time prior to the rising of the CS	t_{DS}	0.2	–	–	µs
Hold time after the rising of the CS	t_{CSH}	0.2	–	–	µs
Input data setup time	t_{ISU}	0.2	–	–	µs
Input data hold time	t_{IHO}	0.2	–	–	µs
Output data determination time	t_{ACC}	–	–	0.6	µs
Setup time prior to the falling of the CS	t_{CSS}	0.2	–	–	µs
Hold time after the falling of the CS	t_{DH}	0.2	–	–	µs
Input rising/falling time	t_R, t_F	–	–	0.05	µs

■ Timing Charts

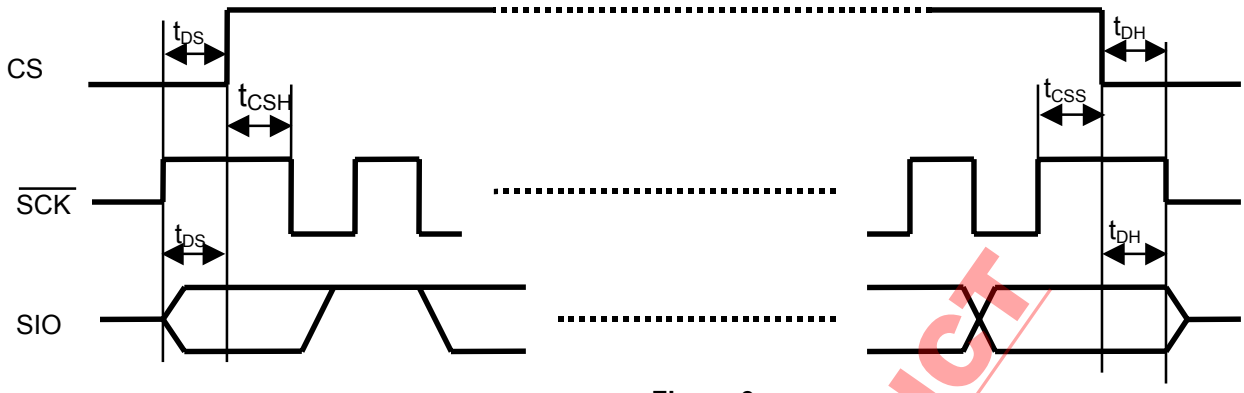


Figure 3

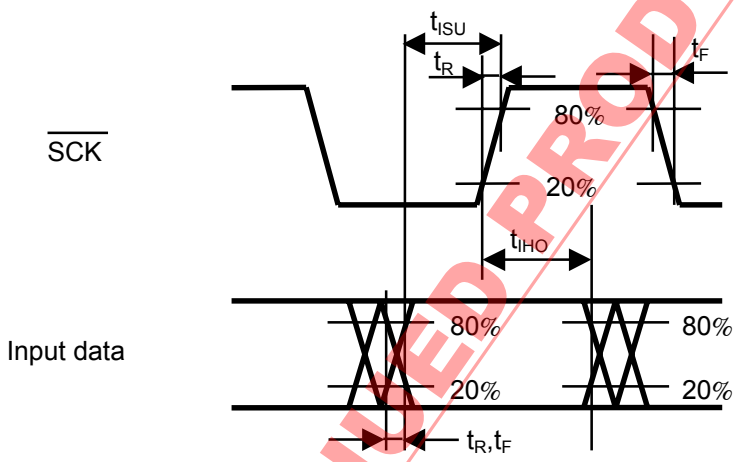


Figure 4

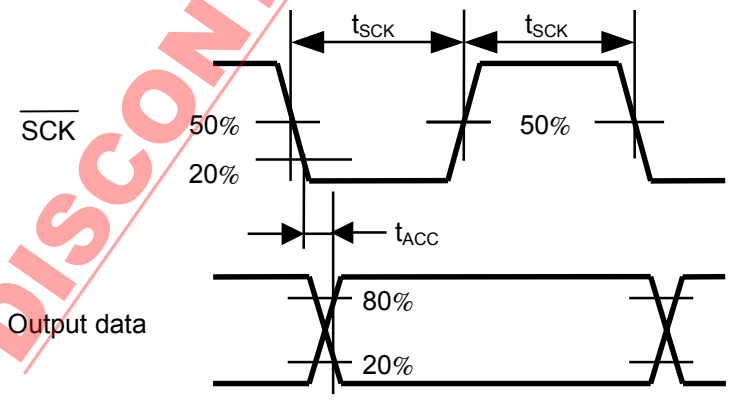


Figure 5

■ Operation

(1) Initialization

When the power is switched on, the POW flag is assigned via the power-on detector. Always turn the CS to"L". Regardless of the logic of the POW flag, initialization must be executed, therefore always send the RESET command (10101010) from the CPU.

This allows the divider, counter and status register of the S-3510 series to be reset. Namely, the second, minute, hour, day, date, month, and year (00 s, 00 min., 00 hr., Sunday (1), January (01), 00 year) are set, and the counter starts to operate upon the falling edge of the CS.

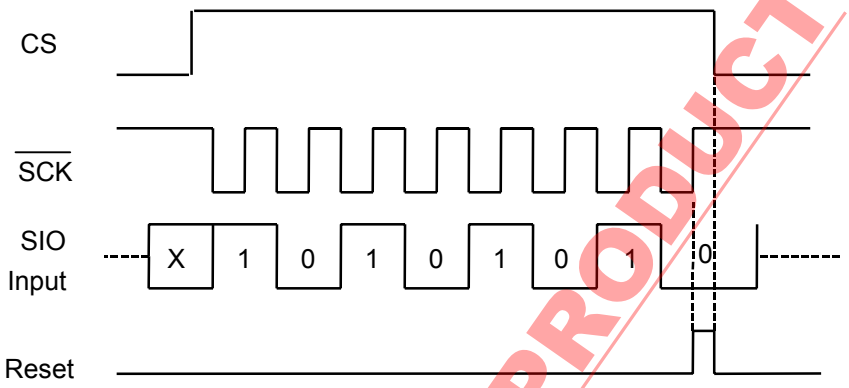
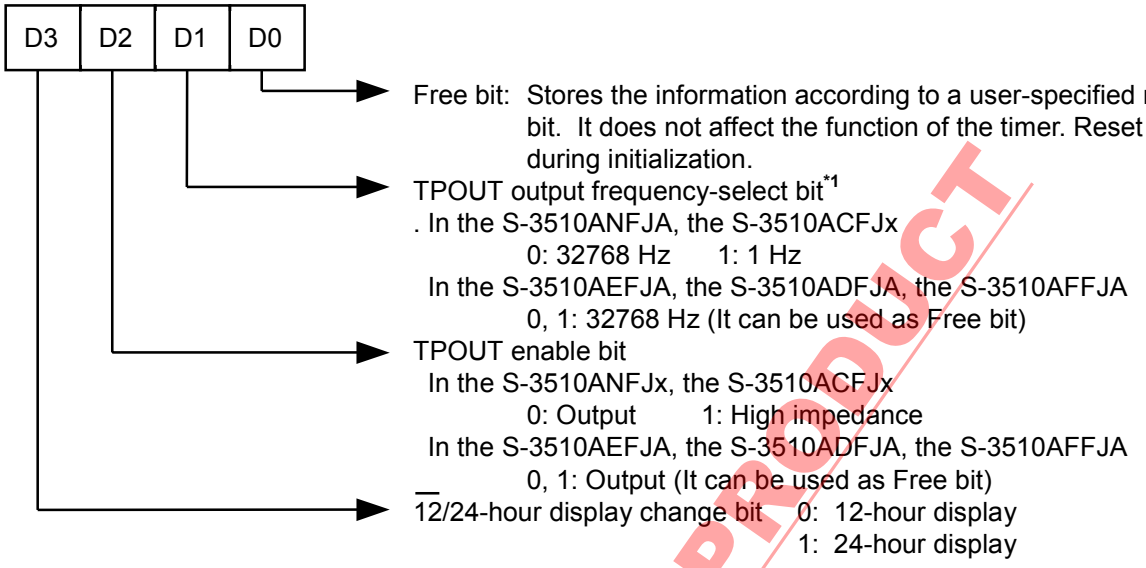


Figure 6

(2) Write to the Status Register

The S-3510 series is provided with a 4-bit status register. To write the data in the register, send the STATUS WRITE command (1011D3D2D1D0). This data is retrieved in synchronization with the falling edge of the CS.



***1.** When the frequency-select bit is rewritten during operation, the first pulse generated immediately after the CS is turned to "L" cannot be output at the correct frequency

Upon initialization, (D3, D2, D1, D0) is set to (1, 0, 1, 0). In other words,

(a) In the S-3510ANFJx, the S-3510ACFJA, 1 Hz is output from TPOUT , and the status is set to the 24-hour display mode.

(b) In the S-3510AEFJx, the S-3510ADFJA, the S-3510AFFJA, 32768 Hz is output from TPOUT , and the status is set to the 24-hour display mode.

When initialization is not executed, the data of the status register is not specified. Always execute initialization when switching on the power.

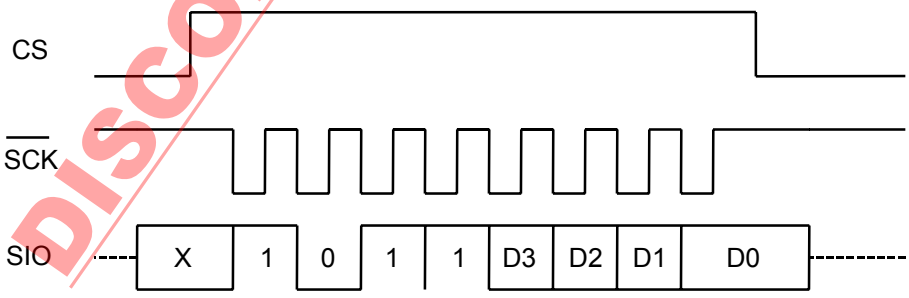


Figure 7

(3) Data Read

The time data can be read by sending the READ command after the CS goes “H”. The data is output in order of the LSB of the day or year.

After the READ command is interpreted, the time data is transmitted from the counter to the shift register. In synchronization with the falling edge of the 9th clock, the SIO status changes from input to output, and the LSB of the timer register is output. After then, in synchronization with the falling edge of the clock, the time data is output from the shift register.

If the power supply voltage detector activates, the MSB (BLD bit) is set to”1”, which allows the power supply voltage to be monitored. For more details, refer to the **“(6) Voltage Detector**”.

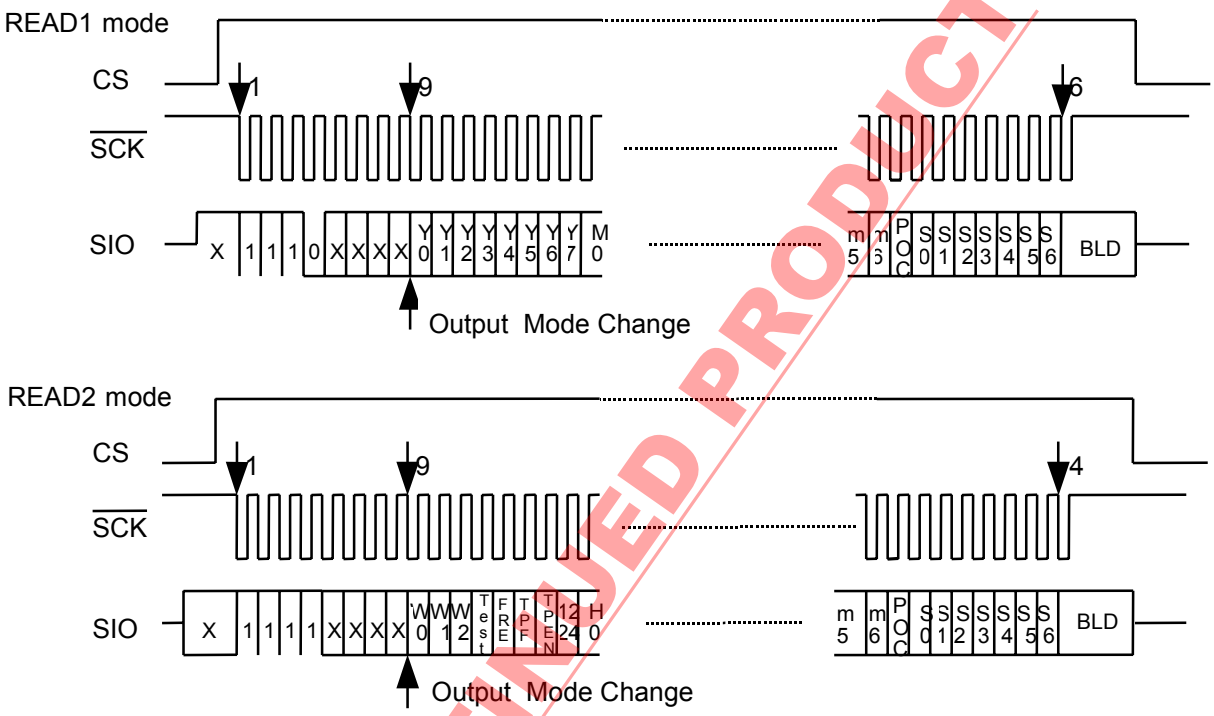
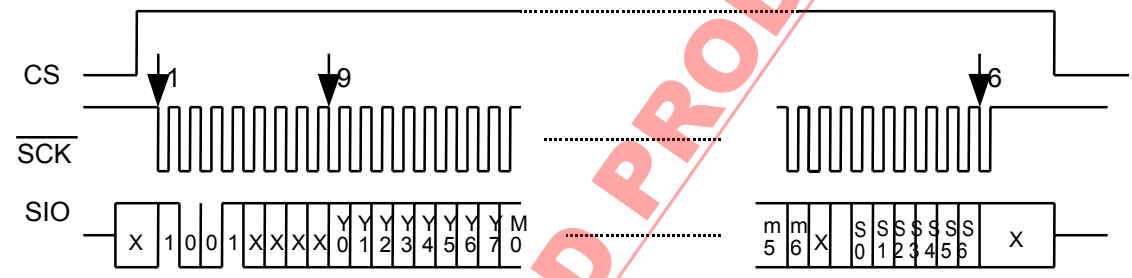


Figure 8

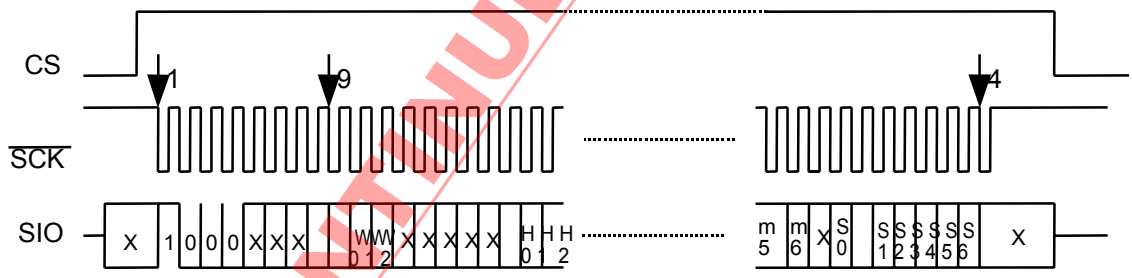
(4) Data Write

Sending the WRITE command after the CS changes from “L” to”H” halts the update operation and resets the frequency divider. This allows the time data to be written. The data is input in order of the LSB of the day or year. The time data transmitted from the SIO is written in the shift register in synchronization with the rising edge of the clock. After transmission of the minute data has been completed, the currently-stored data is transmitted to the counter during the period of the transmission of the second data, and the month-end correction is executed. The second data is transmitted from the shift register to the second counter in synchronization with the point where the CS changes from “H” to”L”. Accordingly, the second data error processing is not performed. Turning the CS to “L” allows the divider to run and update operation to start. One second after, the carry-up signal is transmitted to the second counter. If non-existent data is written in the second counter, the second counter is set to “00”, and the carry-up signal is transmitted to the minute counter.

WRITE1 mode

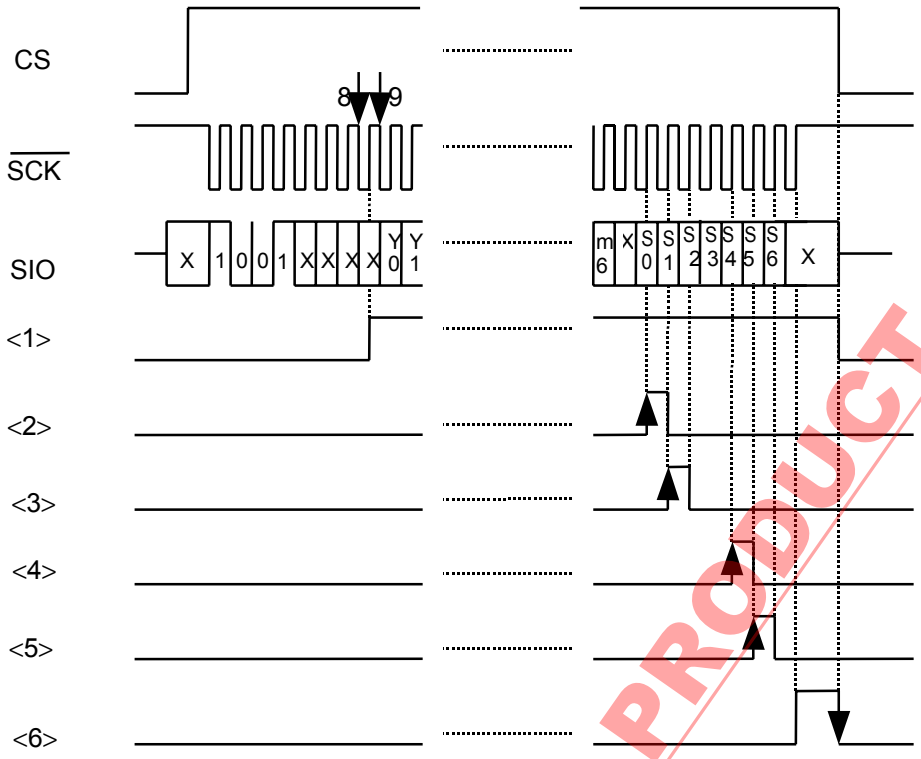


WRITE 2 mode



Caution When the CS is turned to “L”, correct data cannot be written. Never turn the CS to “L” before WRITE is completed. Refer to the timing chart shown below.

Figure 9



<1> Dividing steps are reset at “H”.
<2> All bits of the minute, hour and day (date, month, and year) counter are zero cleared at “H”.
<3> With respect to the bit where the data written in the minute, hour and day (date, month, and year) counter is 1, 1 is set at “H”.
<4> Invalid data processing is performed at “H”.
<5> Month-end processing is performed at “H”.
<6> The second data is written at “H”.

Figure 10

(5) Month-End Correction

When the time data is written in the counter, its validity is checked and either invalid data or month-end processing is performed.

[Data Processing]

Table 11

	Normal data	Error data	Result
Year data	00 to 99	XA to XF, AX to FX	00
Month data	01 to 12	00, 13 to 19, XAto XF	01
Day data	1 to 7	0	1
Date data	01 to 31	00, 32 to 39, XA to XF	01
Hour data (24-hour)*1	0 to 23	24 to 29, 3X, XA to XF	00
(12-hour)	0 to 11	12 to 19, XA to XF	00
Minute data	00 to 59	60 to 79, XA to XF	00
Second data*2	00 to 59	60 to 79, XA to XF	00

***1.** Invalid data processing for the second data is performed through the carry pulse 1 second after the completion of writing. The carry pulse is sent to the minute counter.

***2.** Write 0 or 1 into the AM/PM flag using the 12-hour display.
For the 24-hour display, 0 or 1 is neglected when writing into the AM/PM flag. When reading, however, 0 is read during 0 to 11 o'clock, and 1 is read during 12 to 23 o'clock.

[Month-End Processing]

Non-existent days at the end of the month are automatically processed as the 1st day of the following month. For example, April 31 is automatically set to May 1. Leap years are allso adjusted.

(6) Voltage Detector

The S-3510 series incorporates a voltage detector that performs sampling once a second for 62.5 ms.
When the supply voltage goes below the detection voltage, the BLD latch-up circuit latches "H", and stops sampling.
When the CS is turned to "H", the output of the latch-up circuit is transmitted to the shift register only when the subsequent command is the READ command.
Reading the BLD bit allows the decrease in the voltage to be monitored.
If the CS is turned to "L" after completing the read, sampling restarts. That is, once a decrease in the voltage is detected, detection is not performed and the status is kept "H" as long as an initialization is not performed or a READ command is not sent.

Caution The BLD flag can read 1 when the supply voltage increases and the first read is executed. After that, however, sampling is permitted. Therefore, when the next read is performed after sampling of the detector, the BLD flag is reset. Refer to the timing charts shown next:

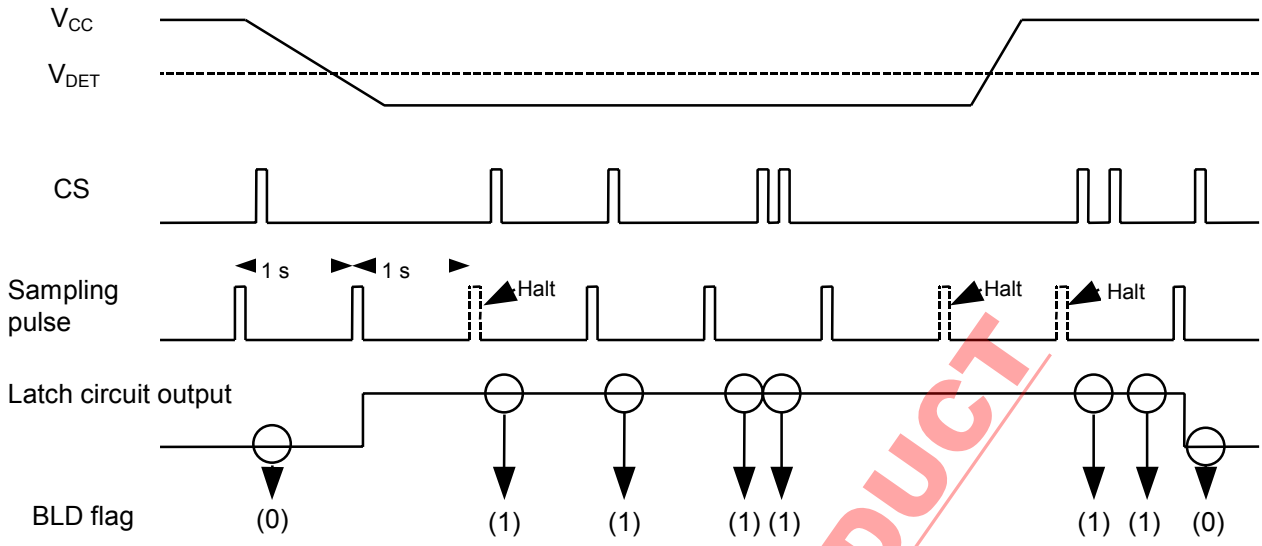


Figure 11

[Timing of Sampling Pulse]

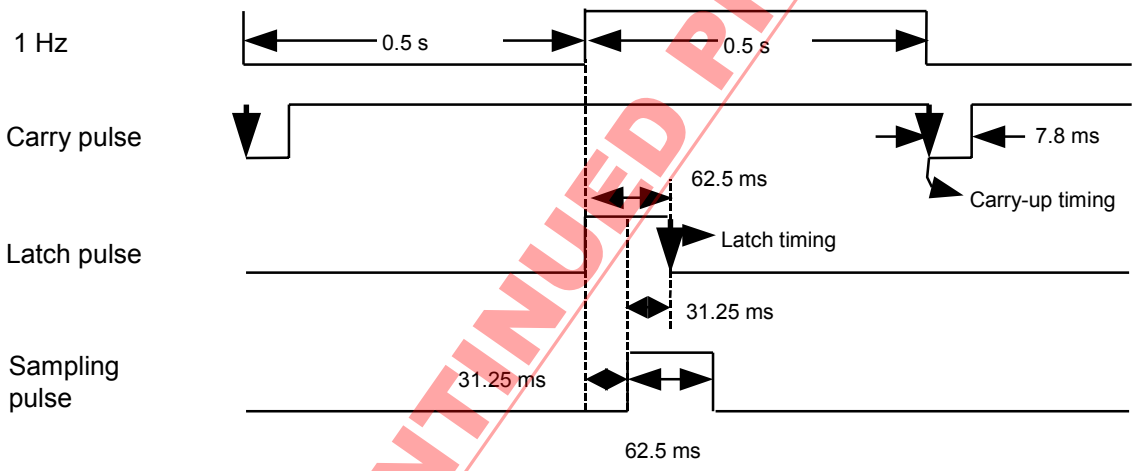


Figure 12

■ Application Circuit Examples

(1) S-3510ANFJx, S-3510AEFJx (Nch open-drain output)

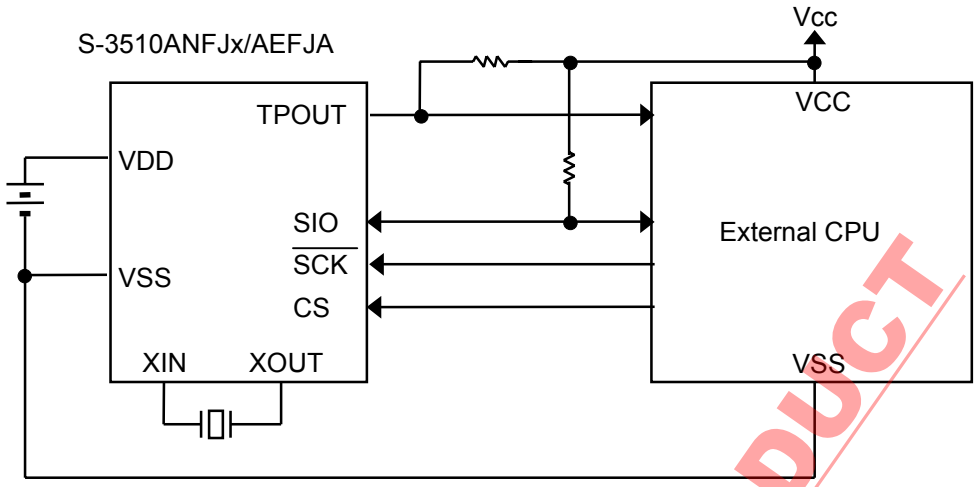


Figure 13

(2) S-3510ACFJx, S-3510ADFJx (CMOS output)

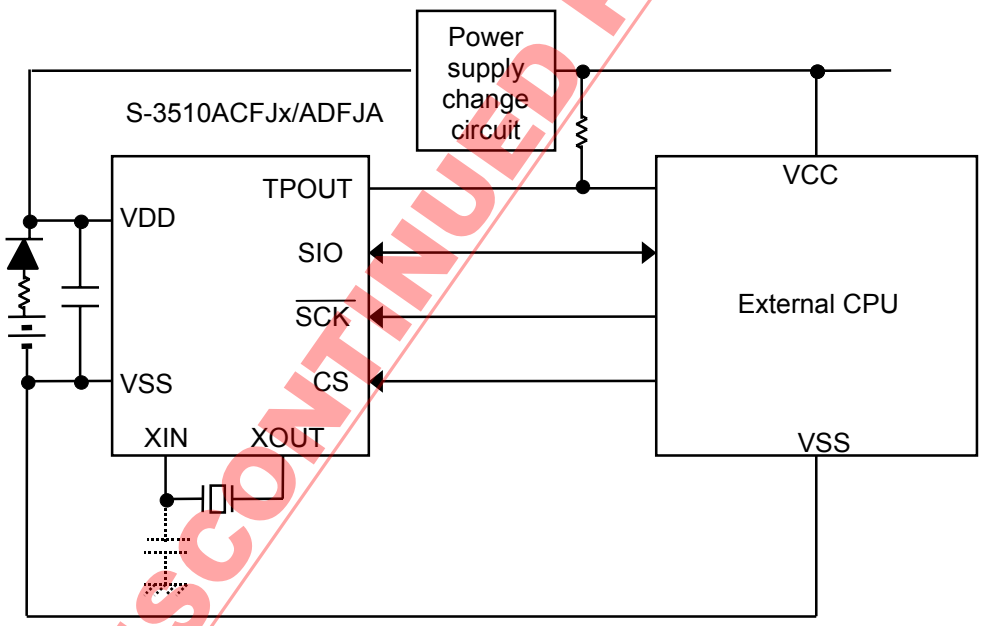


Figure 14

Caution In the case of (2) or (3), the voltage of more than V_{DD} cannot be applied to the SIO,CS,SCK. For communication purpose, switch the system power supply (V_{CC}) on, and turn the CS to "H" after the system power supply stabilizes. Always turn the CS to "L" and switch the system power supply off.

(3) S-3510AFFJ (SIO:CMOS output, TPout:CMOS output)

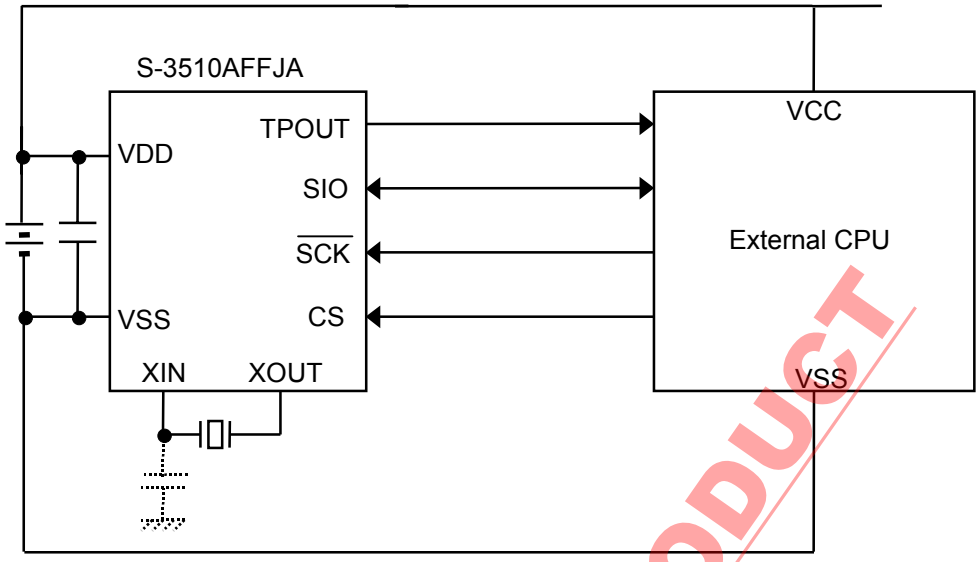


Figure 15

Caution In the case of (2) or (3), the voltage of more than V_{DD} cannot be applied to the SIO,CS,SCK. For communication purpose, switch the system power supply (V_{CC}) on, and turn the CS to "H" after the system power supply stabilizes. Always turn the CS to "L" and switch the system power supply off.

When $V_{DD}<V_{CC}$, the SCK and CS terminals can be directly connected to the CPU because there is no flow of current from the CPU.

■ Precautions

- The oscillation which uses a quartz crystal resonator is sensitive to external noise which may have an effect on the accuracy of the watch. Make sure to design your oscillation circuit with this in mind.
  A) Configure the quartz crystal resonator as close to the IC as possible.
  B) Take measures for sufficient insulation between pins XIN and XOUT.
  C) Do not design a circuit where signal lines or the power lines pass close to the oscillation circuit.

- When using other resonators, not specified herein or other than the DS-VT-200, always check the accuracy and stability of the oscillation by changing conditions such as the power supply voltage and temperature on the actual PCB you use.

- The load capacitance (C_L) of the quartz crystal resonator visibly changes depending upon the capacitance of the PCB mounted onto the IC. Adjust the load capacitance.

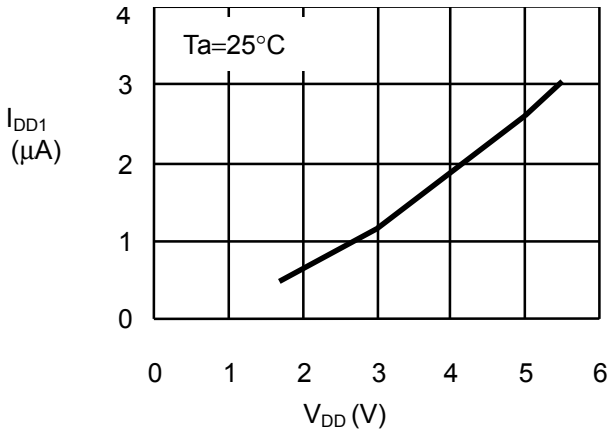
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

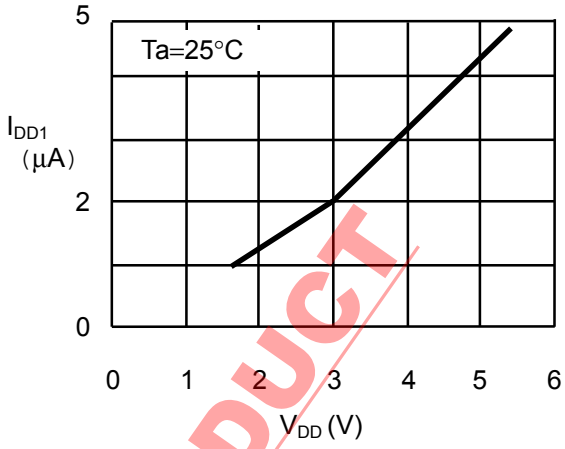
■ Characteristics

1.1 I_{DD1} - V_{DD}

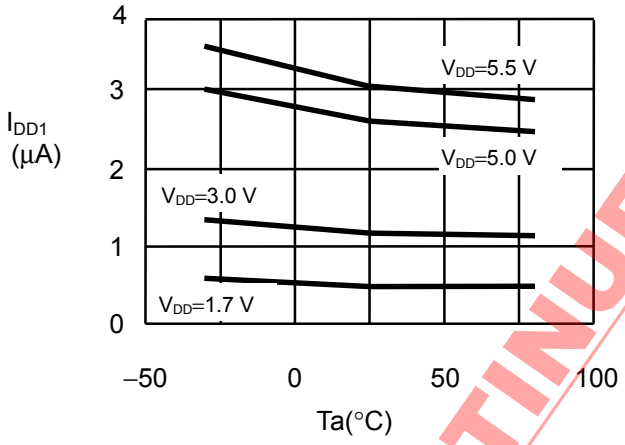
(The products except S-3510AFFJA)



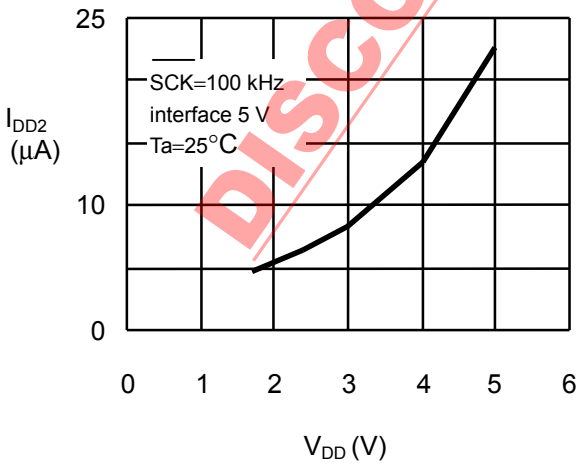
(S-3510AFFJA)



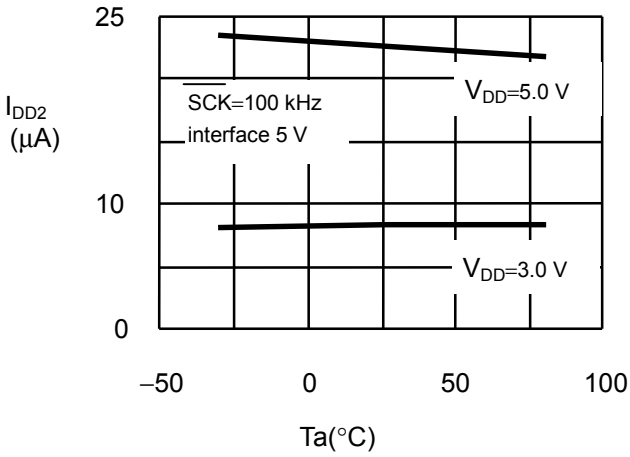
1.2 I_{DD1} - Ta



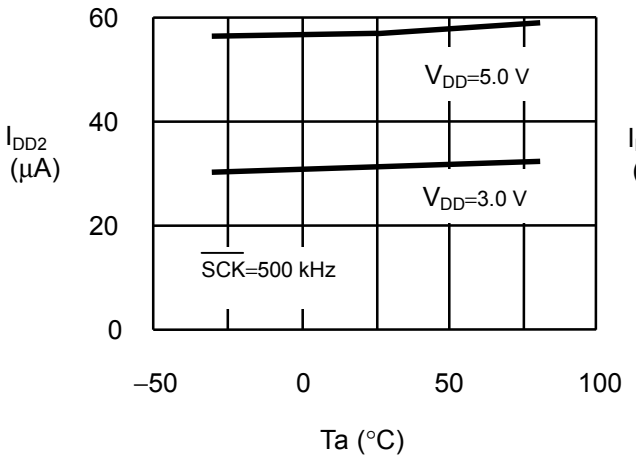
2.1 I_{DD2} - V_{DD} (S-3510ANFJx,S-3510AEFJA)



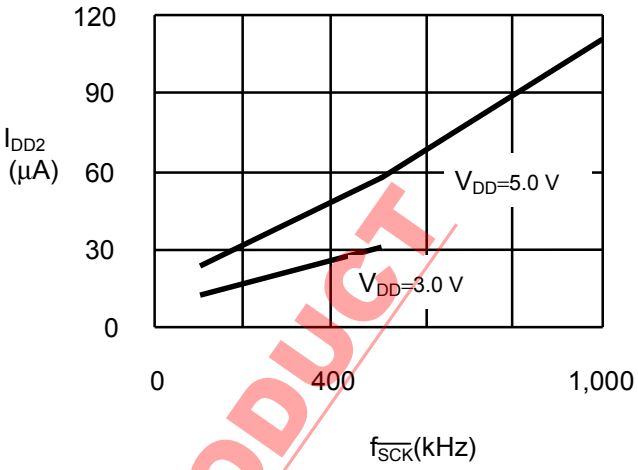
2.2 I_{DD2} - Ta (S-3510ANFJx,S-3510AEFJA)



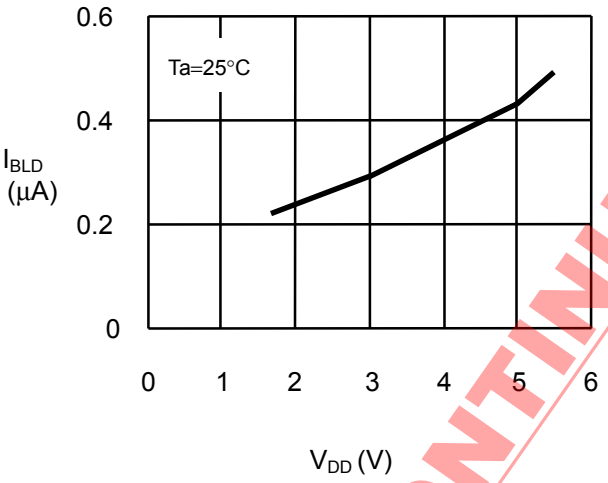
2.3 I_{DD2} - Ta
(S-3510ACFJx,S-3510ADFJA,S-3510AFFJA)



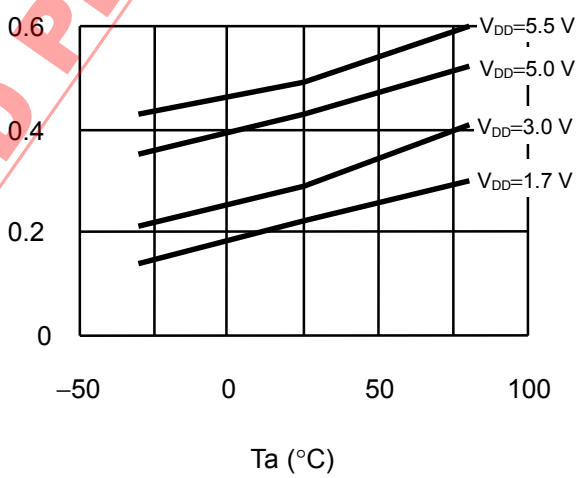
2.4 I_{DD2} - $f_{\overline{SCK}}$
(S-3510ACFJx,S-3510ADFJA,S3510AFFJA)



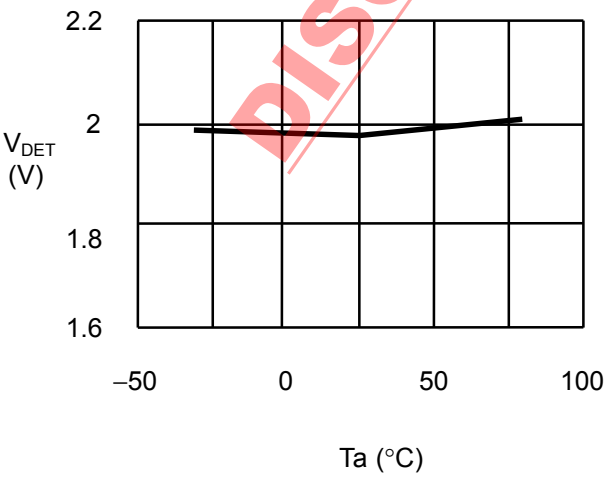
3.1 I_{BLD} - V_{DD}



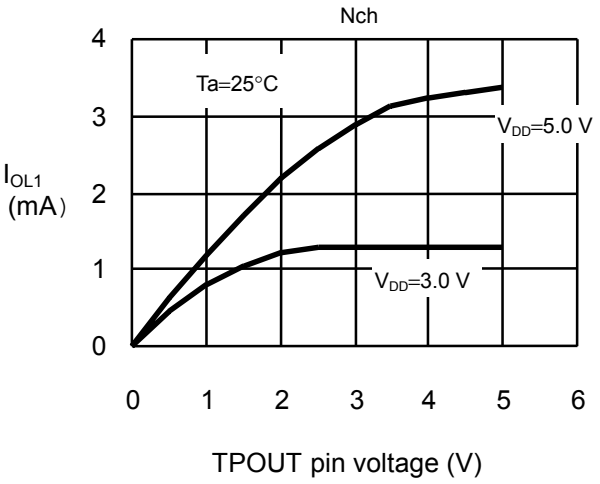
3.2 I_{BLD} - Ta



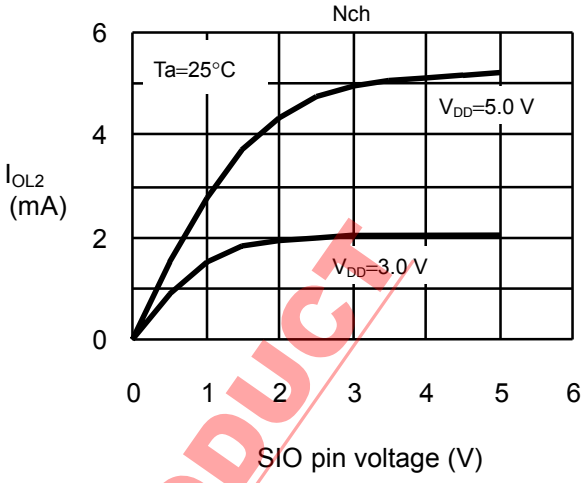
3.3 BLD detection voltage temperature characteristics



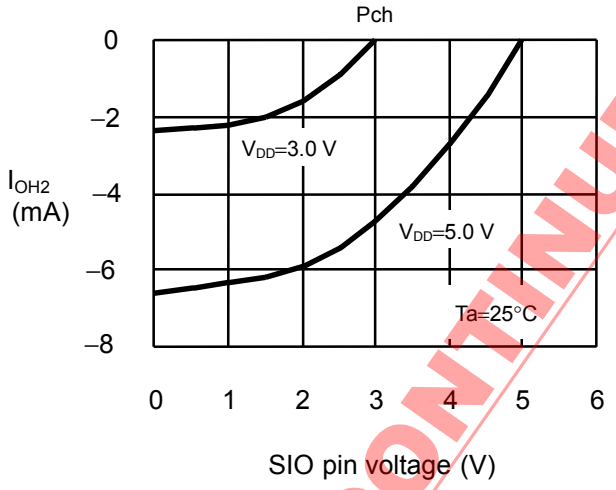
4.1 TPOUT pin output transistor characteristics



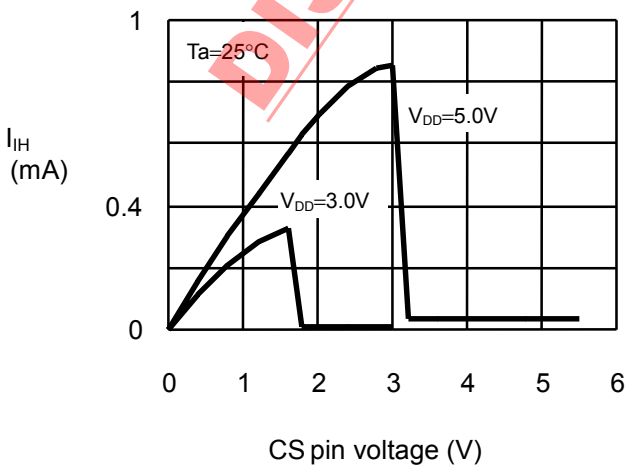
4.2 SIO pin output transistor characteristics



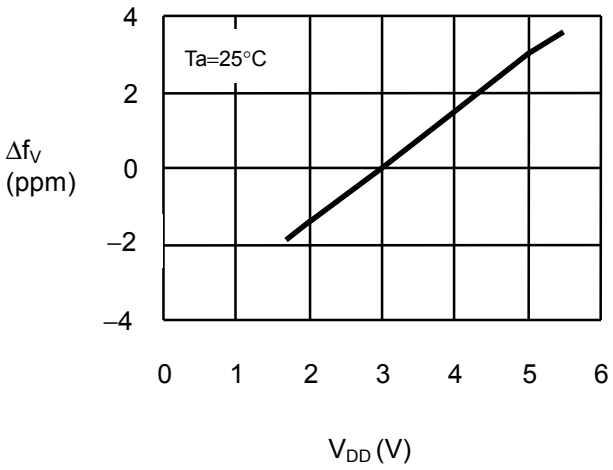
4.3 SIO pin output transistor characteristics



5.1 CS pin input current characteristics

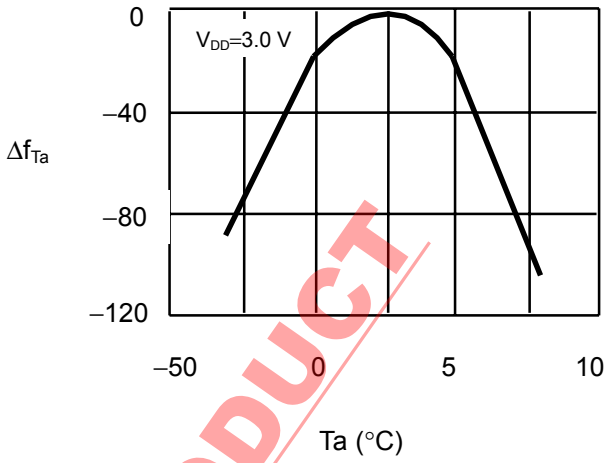


6.1 Oscillation frequency deviation



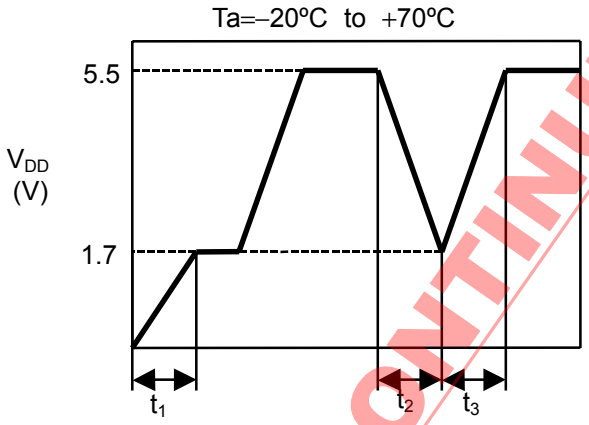
$$\Delta f_V = \frac{f(V_{DD}) - f(3V)}{f(3V)} \times 10^6 (ppm)$$

6.2 Oscillation frequeny temperature deviation

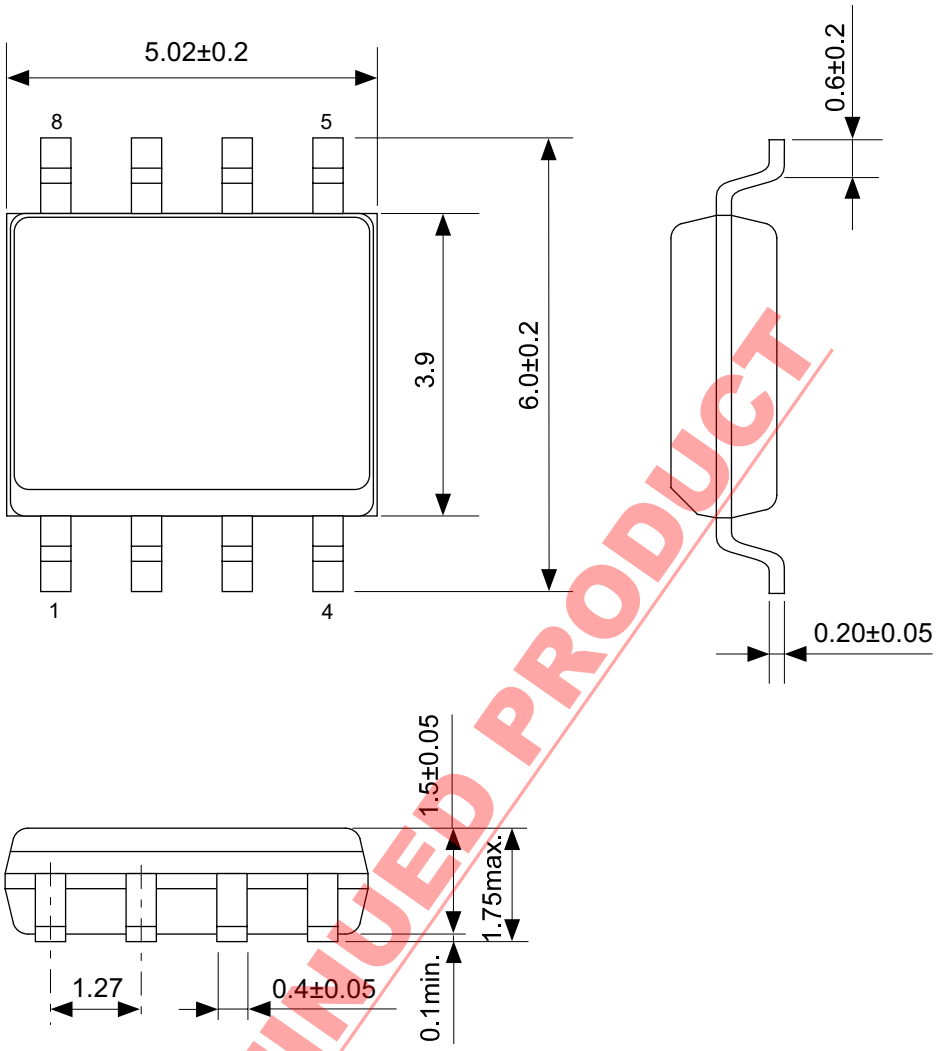


$$\Delta f_{Ta} = \frac{f(Ta) - f(25°C)}{f(25°C)} \times 10^6 (ppm)$$

7.1 Power-on detector characteristics

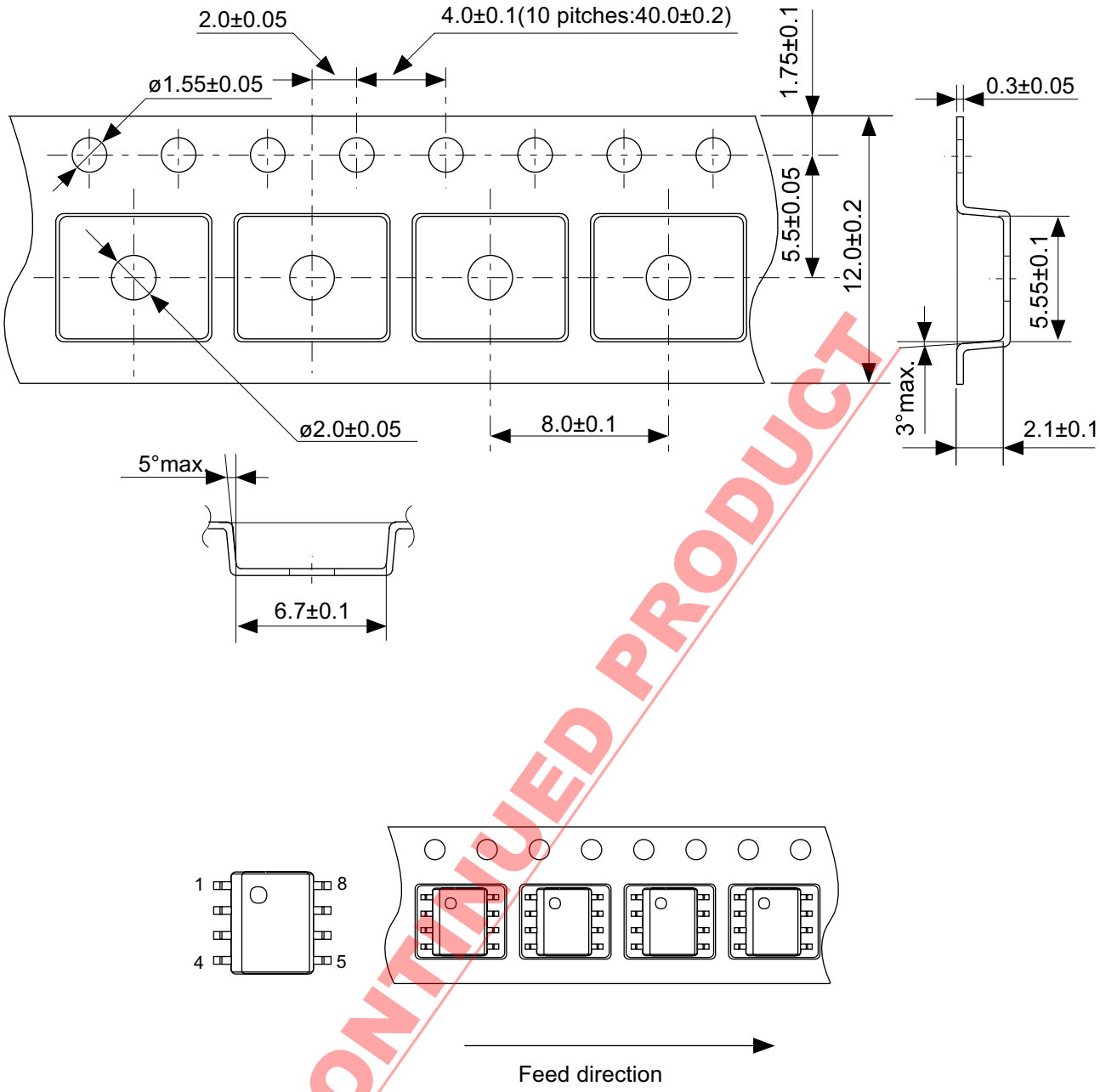


t_1=Condition where power-on is detected:
$t_2 \leq 1$ ms.
t_2=Condition where the data is retained and the IC functions normally when the power supply voltage falls:
$t_2 \geq 1$ ms.
t_3=Condition where the data is retained and the IC functions normally when the power supply voltage rises:
$t_3 \geq 1$ ms.



No. FJ008-A-P-SD-2.1

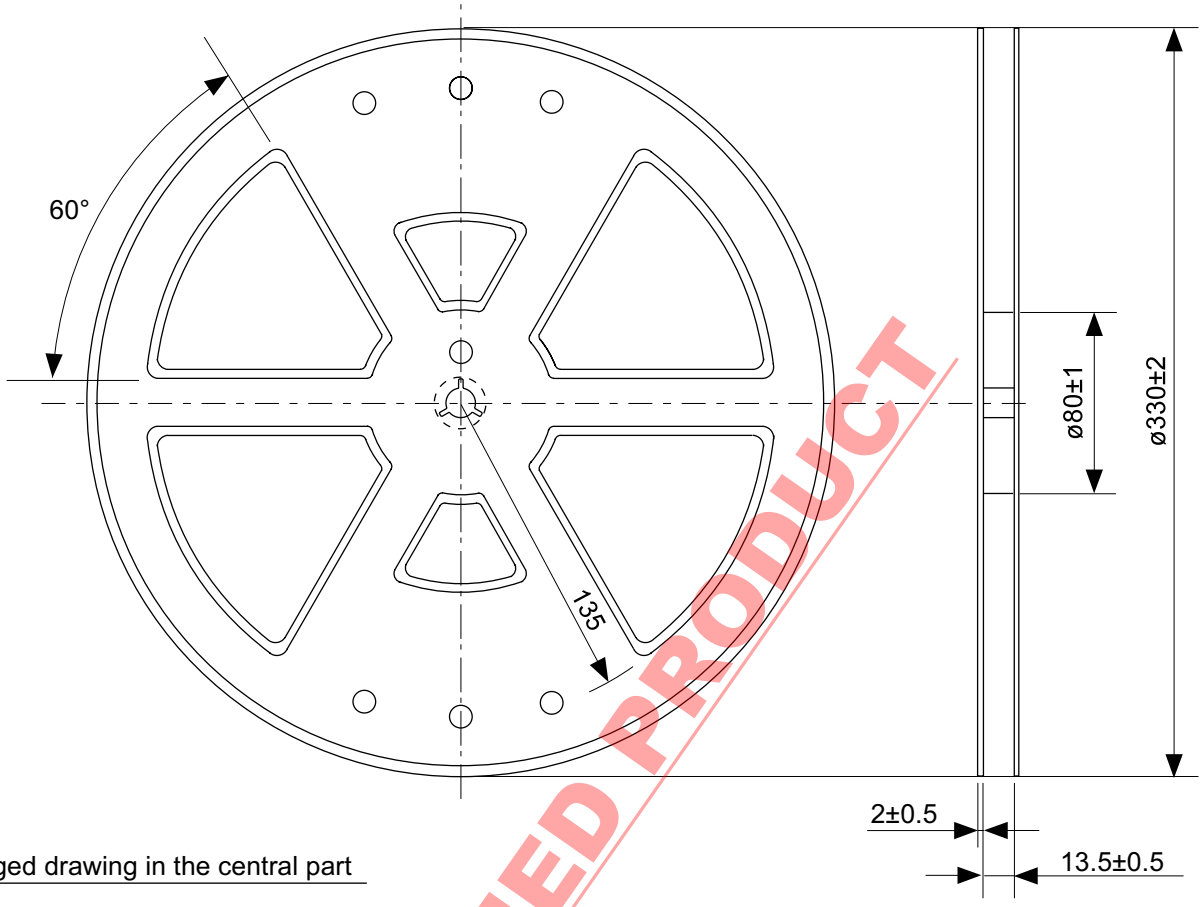
TITLE	SOP8J-A-PKG Dimensions
No.	FJ008-A-P-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



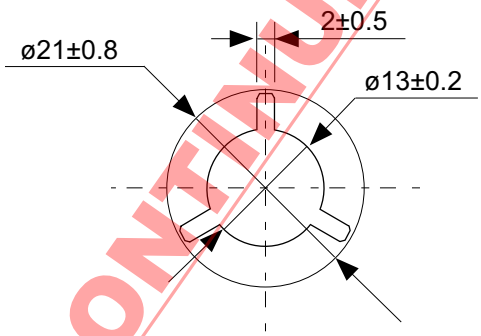
No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm

Seiko Instruments Inc.



Enlarged drawing in the central part



No. FJ008-D-R-SD-1.1

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			