S-35710 A Series

CONVENIENCE TIMER

AUTOMOTIVE, 125°C OPERATION, 2-WIRE TIMER

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The convenience timer is a CMOS timer IC which operates with low current consumption, and is suitable for the time management of the relative time.
The S-35710 Series compares the timer value and the value written to the internal register, and outputs an interrupt signal when the values match each other.
The timer of the S-35710 Series is a 24-bit binary-up counter.
The internal register data can be set freely by users via a 2-wire serial interface. Consequently, the time before the occurrence of an interrupt signal can be set freely.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.**

■ Features

- Alarm interrupt function: Settable on the second time scale from 1 second to 194 days (Approximately half a year)
- Low current consumption: 0.2 μA typ. (Quartz crystal: C_L = 6.0 pF, V_{DD} = 3.0 V, Ta = +25°C)
- Wide range of operation voltage: 1.8 V to 5.5 V
- 2-wire (I^2C-bus) CPU interface
- Built-in 32.768 kHz crystal oscillation circuit
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*1

*1. Contact our sales office for details.

■ Application

- Time management of various systems during the sleep period

■ Package

- TMSOP-8

■ Block Diagram

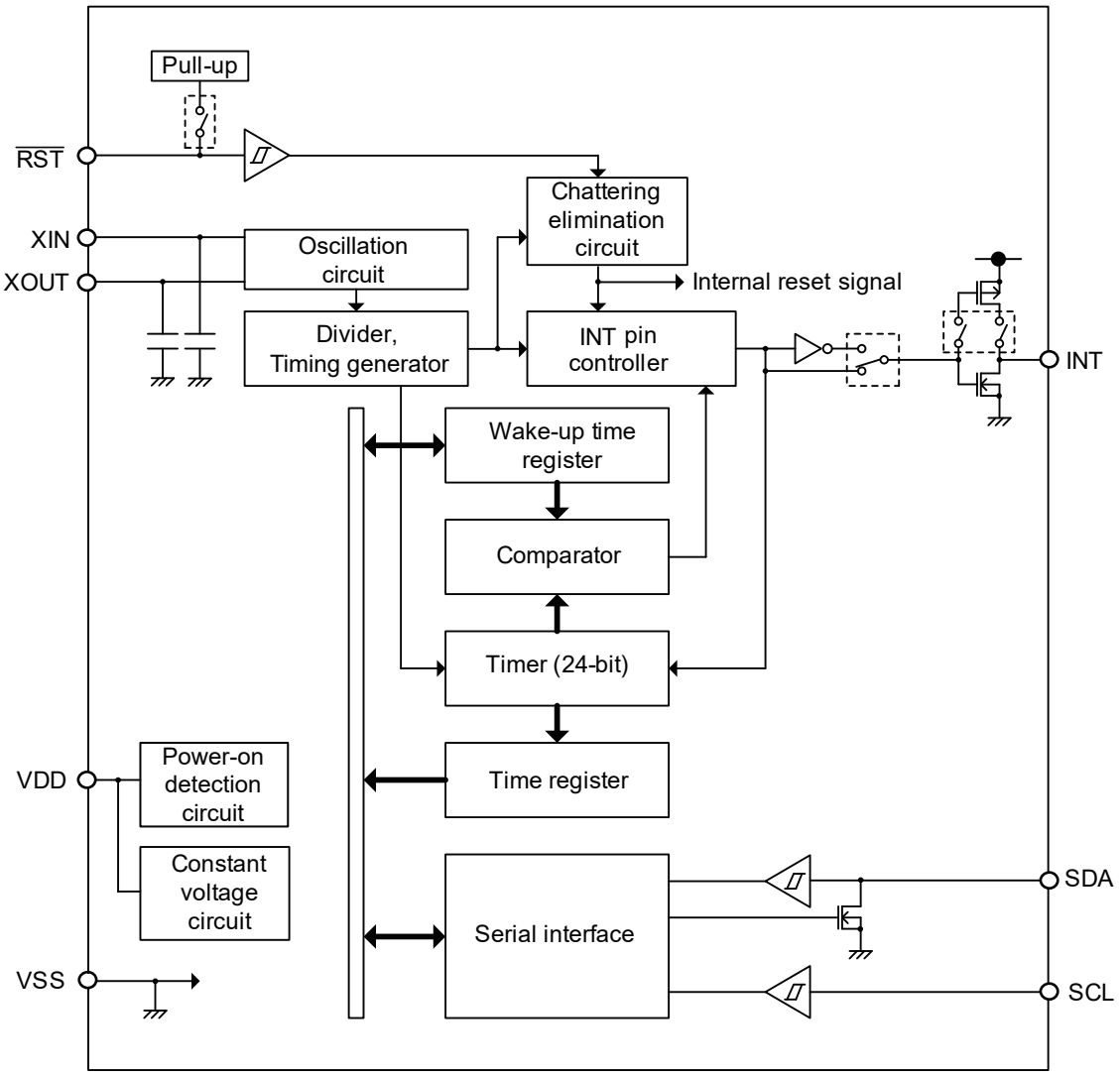


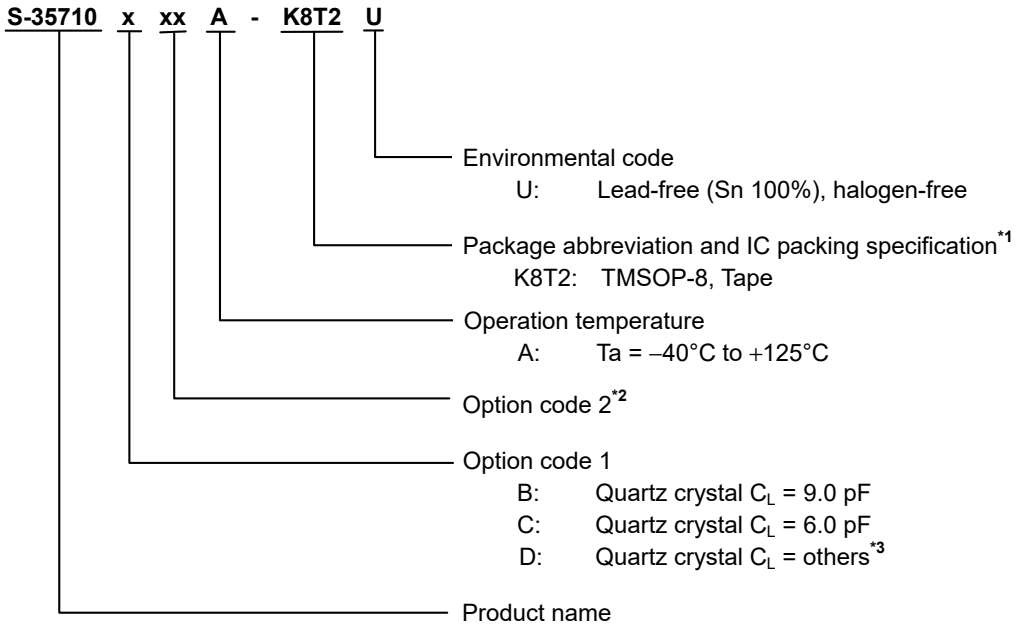
Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** A sequence number added by the optional function that is user-selected.
***3.** Contact our sales office for details.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	$\overline{\text{RST}}$ Pin*1	INT Pin Output Form*2	Time-out Type*3
S-35710B01A-K8T2U	With pull-up resistor	CMOS output	Handshake time-out
S-35710C01A-K8T2U	Without pull-up resistor	Nch open-drain output	Handshake time-out

***1.** The pin with / without pull-up resistor is selectable. Refer to "■ **Pin Functions**".
***2.** The pin of Nch open-drain output / CMOS output is selectable. Refer to "■ **Pin Functions**".
***3.** The type of one-shot loop time-out / handshake time-out is selectable. Refer to "■ **INT Pin Interrupt Signal Output"**.

Remark Please contact our sales office for products with specifications other than the above.

■ Pin Configuration

1. TMSOP-8

Top view

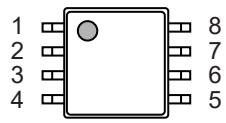


Figure 2

Table 3 List of Pins

Pin No.	Symbol	Description	I/O	Configuration
1	$\overline{RST}$	Input pin for reset signal	Input	CMOS input (With / without pull-up resistor is selectable)
2	XOUT	Connection pins for quartz crystal	–	–
3	XIN			
4	VSS	GND pin	–	–
5	INT	Output pin for interrupt signal	Output	Nch open-drain output / CMOS output is selectable
6	SDA	I/O pin for serial data	Bi-directional	Nch open-drain output, CMOS input
7	SCL	Input pin for serial clock	Input	CMOS input
8	VDD	Pin for positive power supply	–	–

■ Pin Functions

1. SDA (I/O for serial data) pin

This is a data input / output pin for I²C-bus interface. The SDA pin inputs / outputs data by synchronizing with a clock pulse from the SCL pin. This pin has CMOS input and Nch open-drain output. Generally in use, the SDA pin is pulled up to V_{DD} potential via a resistor, and is used with wired-OR connection of other device of Nch open-drain output or open collector output.

2. SCL (Input for serial clock) pin

This is a clock input pin for I²C-bus interface. The SDA pin inputs / outputs data by synchronizing with this clock.

3. $\overline{\text{RST}}$ (Input for reset signal) pin

This pin inputs the reset signal. The timer is reset when inputting "L" to the $\overline{\text{RST}}$ pin. The INT pin is set to "H" when inputting "H" to the $\overline{\text{RST}}$ pin, and the timer starts the operation. The $\overline{\text{RST}}$ pin has a built-in chattering elimination circuit. Regarding the chattering elimination circuit, refer to "■ **$\overline{\text{RST}}$ Pin**".
Also, the $\overline{\text{RST}}$ pin with / without a pull-up resistor can be selected.

4. INT (Output for interrupt signal) pin

This pin outputs an interrupt signal. The interrupt signal is output when the time written to the wake-up time register comes. The interrupt signal output (time-out type) of one-shot loop time-out / handshake time-out can be selected as the option. Regarding the operation of the interrupt signal output, refer to "■ **INT Pin Interrupt Signal Output**".
Also, the INT pin output form of Nch open-drain output / CMOS output can be selected.

5. XIN, XOUT (Connection for quartz crystal) pins

Connect a quartz crystal between the XIN pin and the XOUT pin.

6. VDD (Positive power supply) pin

Connect this pin with a positive power supply. Regarding the values of voltage to be applied, refer to "■ **Recommended Operation Conditions**".

7. VSS pin

Connect this pin to GND.

■ Equivalent Circuits of Pins

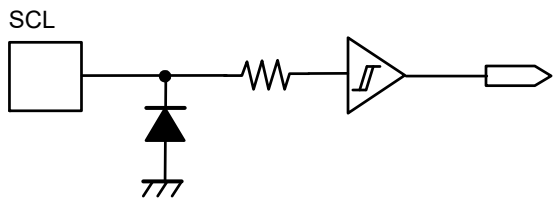


Figure 3 SCL Pin

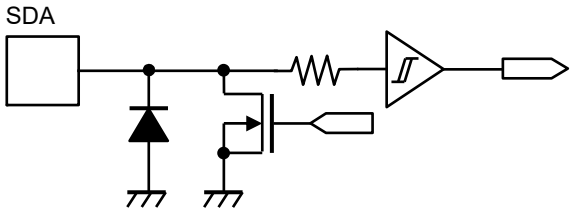


Figure 4 SDA Pin

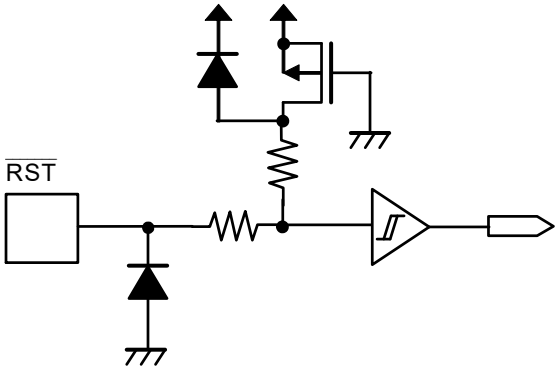


Figure 5 $\overline{\text{RST}}$ Pin (With Pull-up Resistor)

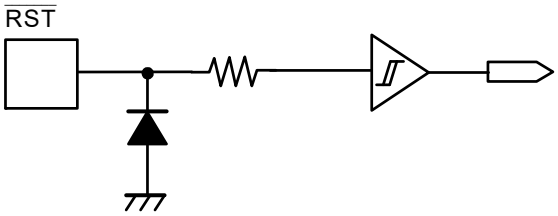


Figure 6 $\overline{\text{RST}}$ Pin (Without Pull-up Resistor)

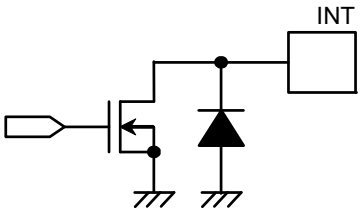


Figure 7 INT Pin (Nch Open-drain Output)

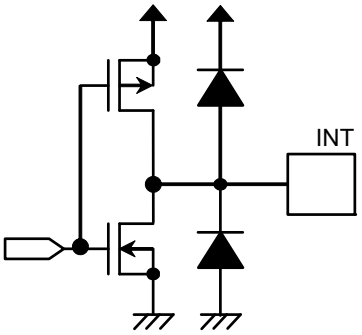


Figure 8 INT Pin (CMOS Output)

■ Absolute Maximum Ratings

Table 4

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	–	V_{SS} – 0.3 to V_{SS} + 6.5	V
Input voltage	V_{IN}	SDA, SCL, $\overline{RST}$*1	V_{SS} – 0.3 to V_{SS} + 6.5	V
		$\overline{RST}$*2	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 6.5	V
Output voltage	V_{OUT}	SDA, INT*3	V_{SS} – 0.3 to V_{SS} + 6.5	V
		INT*4	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 6.5	V
Operation ambient temperature*5	T_{opr}	–	–40 to +125	°C
Storage temperature	T_{stg}	–	–55 to +150	°C

***1.** When a product without a pull-up resistor is selected.
***2.** When a product with a pull-up resistor is selected.
***3.** When an Nch open-drain output product is selected.
***4.** When a CMOS output product is selected.
***5.** Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operation Conditions

Table 5

(V_{SS} = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operation power supply voltage	V_{DD}	Ta = –40°C to +125°C	1.8	–	5.5	V

■ Oscillation Characteristics

Table 6

(Ta = +25°C, V_{DD} = 3.0 V, V_{SS} = 0 V unless otherwise specified)
(Quartz crystal (NX3215SD, C_L = 6.0 pF / 9.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within 10 seconds	1.8	–	5.5	V
Oscillation start time	t_{STA}	–	–	–	1	s
IC-to-IC frequency deviation*1	δIC	C_L = 6.0 pF	–20	–	+20	ppm
		C_L = 9.0 pF	–25	–	+25	ppm

***1.** Reference value

■ DC Electrical Characteristics

Table 7

(Ta = –40°C to +125°C, V_{SS} = 0 V unless otherwise specified)
(Quartz crystal (NX3215SD, C_L = 6.0 pF / 9.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	V_{DD} = 3.0 V, Ta = –40°C to +85°C, Out of communication, $\overline{RST}$ pin = V_{DD}, INT pin = no load, C_L = 6.0 pF	–	0.2	0.35	µA
			V_{DD} = 3.0 V, Ta = –40°C to +85°C, Out of communication, $\overline{RST}$ pin = V_{DD}, INT pin = no load, C_L = 9.0 pF	–	0.26	0.5	µA
			V_{DD} = 3.0 V, Ta = +125°C, Out of communication, $\overline{RST}$ pin = V_{DD}, INT pin = no load, C_L = 6.0 pF	–	0.7	0.95	µA
			V_{DD} = 3.0 V, Ta = +125°C, Out of communication, $\overline{RST}$ pin = V_{DD}, INT pin = no load, C_L = 9.0 pF	–	0.8	1.25	µA
Current consumption 2	I_{DD2}	–	V_{DD} = 3.0 V, f_{SCL} = 1 MHz, During communication, $\overline{RST}$ pin = V_{DD}, INT pin = no load	–	170	300	µA
High level input leakage current	I_{IZH}	SDA, SCL, $\overline{RST}$	V_{IN} = V_{DD}	–0.5	–	0.5	µA
Low level input leakage current	I_{IZL}	SDA, SCL, $\overline{RST}$*1	V_{IN} = V_{SS}	–0.5	–	0.5	µA
High level output leakage current	I_{OZH}	SDA, INT*2	V_{OUT} = V_{DD}	–0.5	–	0.5	µA
Low level output leakage current	I_{OZL}	SDA, INT*2	V_{OUT} = V_{SS}	–0.5	–	0.5	µA
High level input voltage	V_{IH}	SDA, SCL, $\overline{RST}$	–	0.7 × V_{DD}	–	V_{SS} + 5.5	V
Low level input voltage	V_{IL}	SDA, SCL, $\overline{RST}$	–	V_{SS} – 0.3	–	0.3 × V_{DD}	V
High level output voltage*3	V_{OH}	INT	I_{OH} = –0.4 mA	0.8 × V_{DD}	–	–	V
Low level output voltage	V_{OL}	SDA, INT	I_{OL} = 2.0 mA	–	–	0.4	V
Low level input current*4	I_{IL}	$\overline{RST}$	V_{DD} = 3.0 V, V_{IN} = V_{SS}	–100	–30	–5	µA

***1.** When a product without a pull-up resistor is selected.
***2.** When an Nch open-drain output product is selected.
***3.** When a CMOS output product is selected.
***4.** When a product with a pull-up resistor is selected.

■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	$V_{IH} = 0.8 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$
Input pulse rise / fall time	20 ns
Output reference voltage	$V_{OH} = 0.7 \times V_{DD}$, $V_{OL} = 0.3 \times V_{DD}$
Output load	100 pF

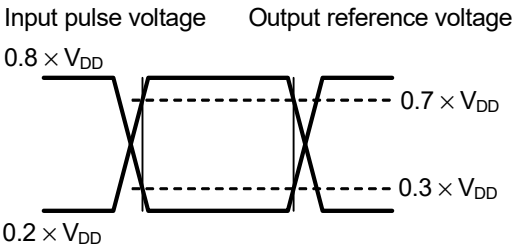


Figure 9 Input / Output Waveform during AC Measurement

Table 9 AC Electrical Characteristics

(Ta = −40°C to +125°C)

Item	Symbol	V_{DD} = 1.8 V to 2.5 V		V_{DD} = 2.5 V to 5.5 V		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	400	0	1000	kHz
SCL clock "L" time	t_{LOW}	1.3	–	0.4	–	µs
SCL clock "H" time	t_{HIGH}	0.6	–	0.3	–	µs
SDA output delay time*1	t_{AA}	–	0.9	–	0.5	µs
Start condition set-up time	$t_{SU.STA}$	0.6	–	0.25	–	µs
Start condition hold time	$t_{HD.STA}$	0.6	–	0.25	–	µs
Data input set-up time	$t_{SU.DAT}$	100	–	80	–	ns
Data input hold time	$t_{HD.DAT}$	0	–	0	–	ns
Stop condition set-up time	$t_{SU.STO}$	0.6	–	0.25	–	µs
SCL, SDA rise time	t_R	–	0.3	–	0.3	µs
SCL, SDA fall time	t_F	–	0.3	–	0.3	µs
Bus release time	t_{BUF}	1.3	–	0.5	–	µs
Noise suppression time	t_I	–	50	–	50	ns

*1. Since the output form of the SDA pin is Nch open-drain output, the SDA output delay time is determined by the values of the load resistance and load capacitance outside the IC. **Figure 11** shows the relationship between the output load values.

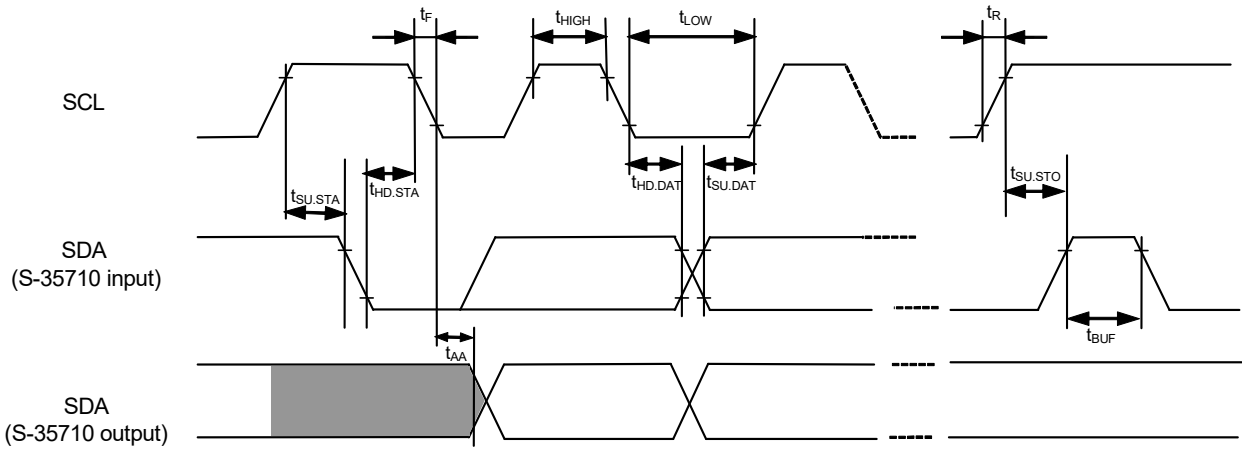


Figure 10 Bus Timing

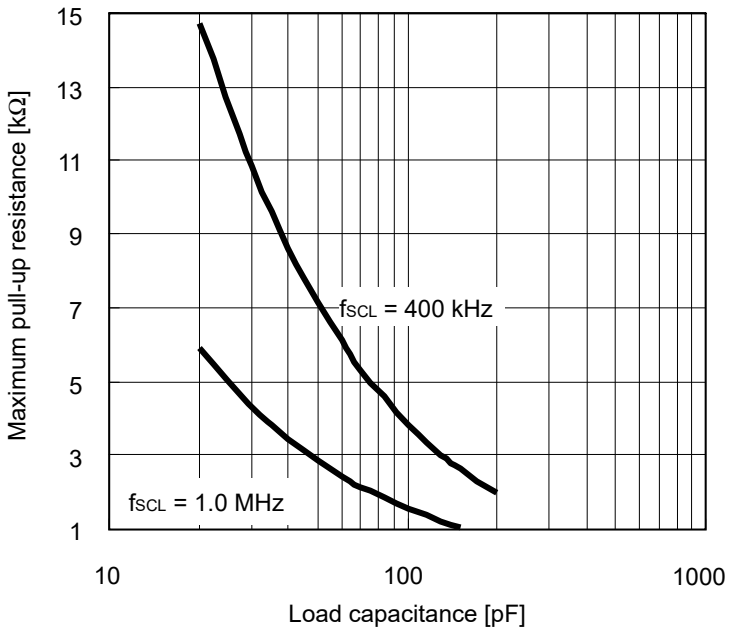


Figure 11 Output Load

■ INT Pin Interrupt Signal Output

The INT pin interrupt signal output (time-out type) can be selected from either of the following:

- One-shot loop time-out
- Handshake time-out

1. One-shot loop time-out

One-shot loop time-out is a type to output "L" pulse interrupt signal repeatedly from the INT pin.
After the $\overline{RST}$ pin changes from "L" to "H", the timer starts the operation. Then, the INT pin outputs "L" pulse when the timer value matches the value written to the wake-up time register. After that, the S-35710 Series resets the timer automatically, and restarts a count-up action.

Remark The above description is the example of an Nch open-drain output product.
In a CMOS output product, the INT pin output is the inverse logic of the Nch open-drain output product.

1. 1 Write mode

If write operation is performed to the wake-up time register during the count-up action, the action will be restarted after resetting the timer. This operation is called "write mode".
If "L" is input to the $\overline{RST}$ pin before the timer value matches the value written to the wake-up time register, the timer and the wake-up time register are reset.

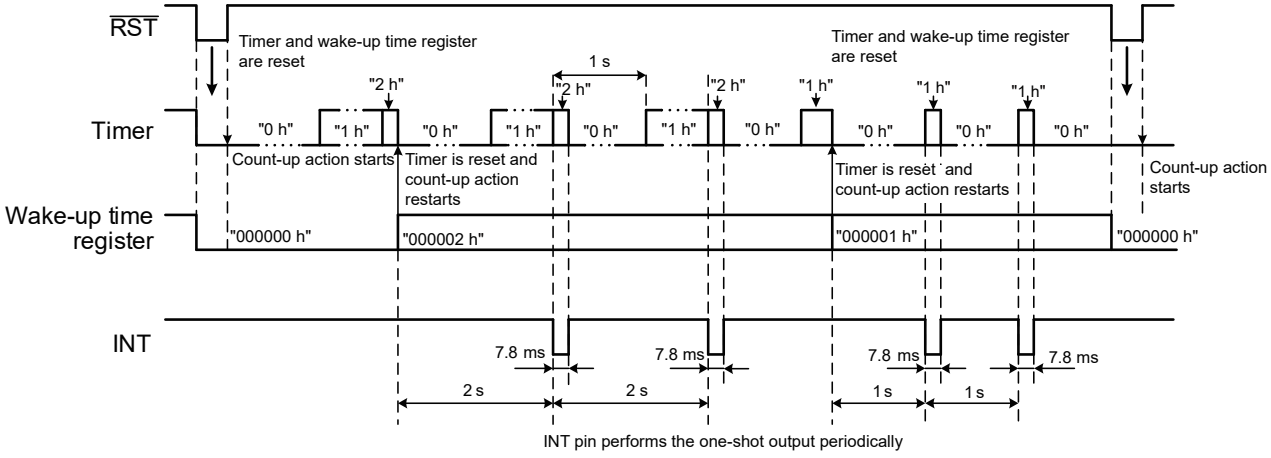


Figure 12 Output Timing of One-shot Loop Time-out (Nch Open-drain Output)

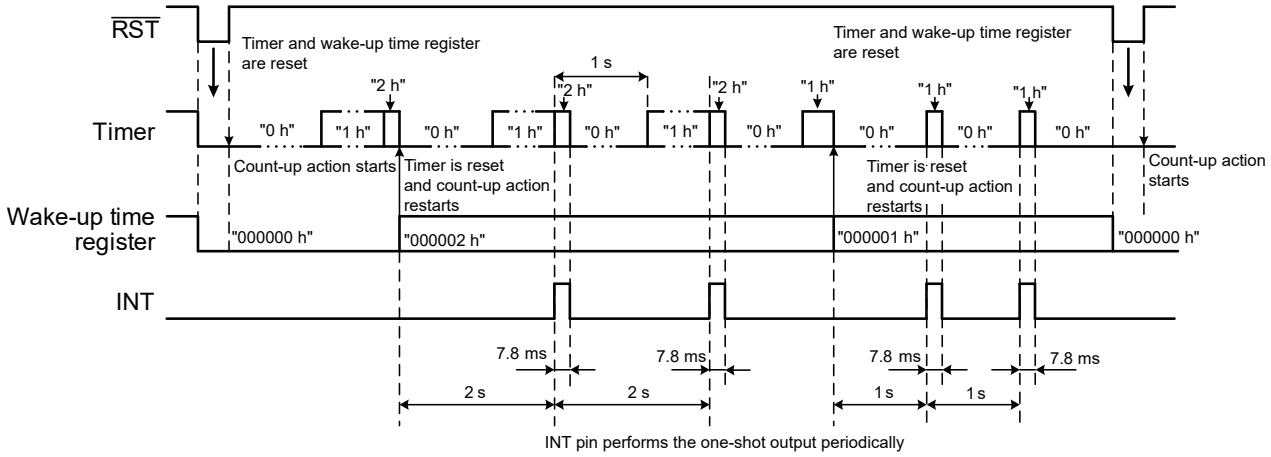


Figure 13 Output Timing of One-shot Loop Time-out (CMOS Output)

1. 2 Read mode

If write operation is not performed to the wake-up time register after the timer starts the operation, the interrupt signal is not output from the INT pin. The timer stops at "FFFFFF h". The timer value during timing can be confirmed by reading the time register. This operation is called "read mode".
In order for the timer to operate again, set the $\overline{RST}$ pin from "L" to "H" or perform write operation to the wake-up time register.

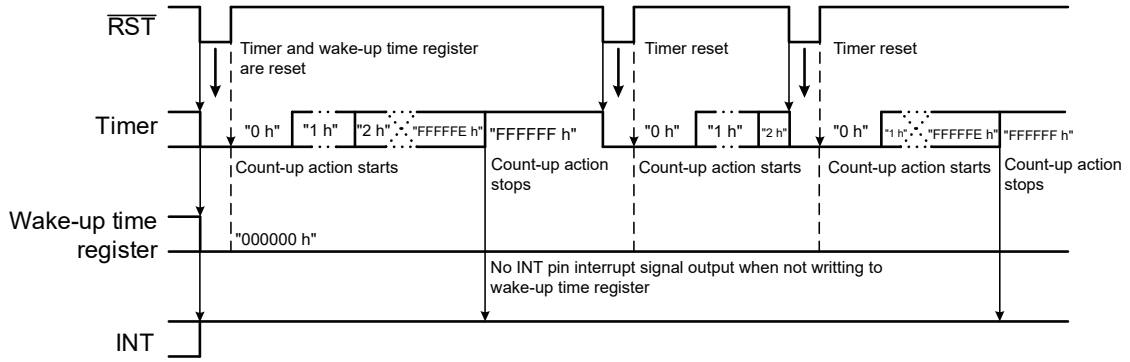


Figure 14 When Write Operation is not Performed to the Wake-up Time Register (Nch Open-drain Output)

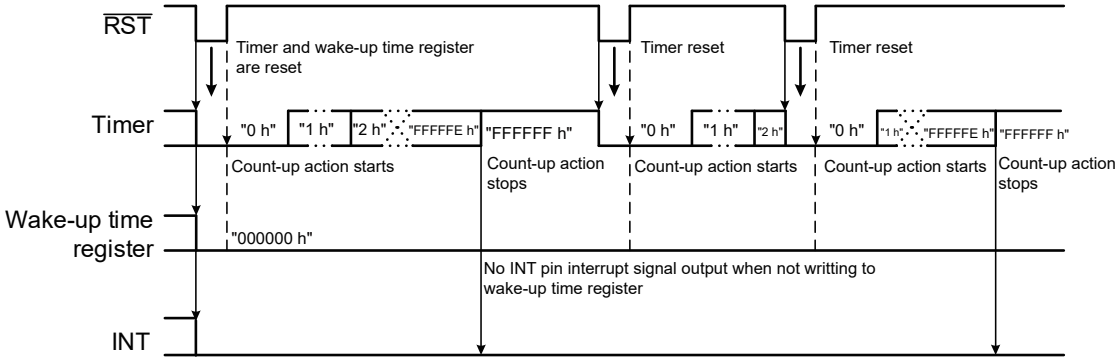


Figure 15 When Write Operation is not Performed to the Wake-up Time Register (CMOS Output)

Figure 16 and **Figure 17** show the status transition diagrams about the one-shot loop time-out operation.

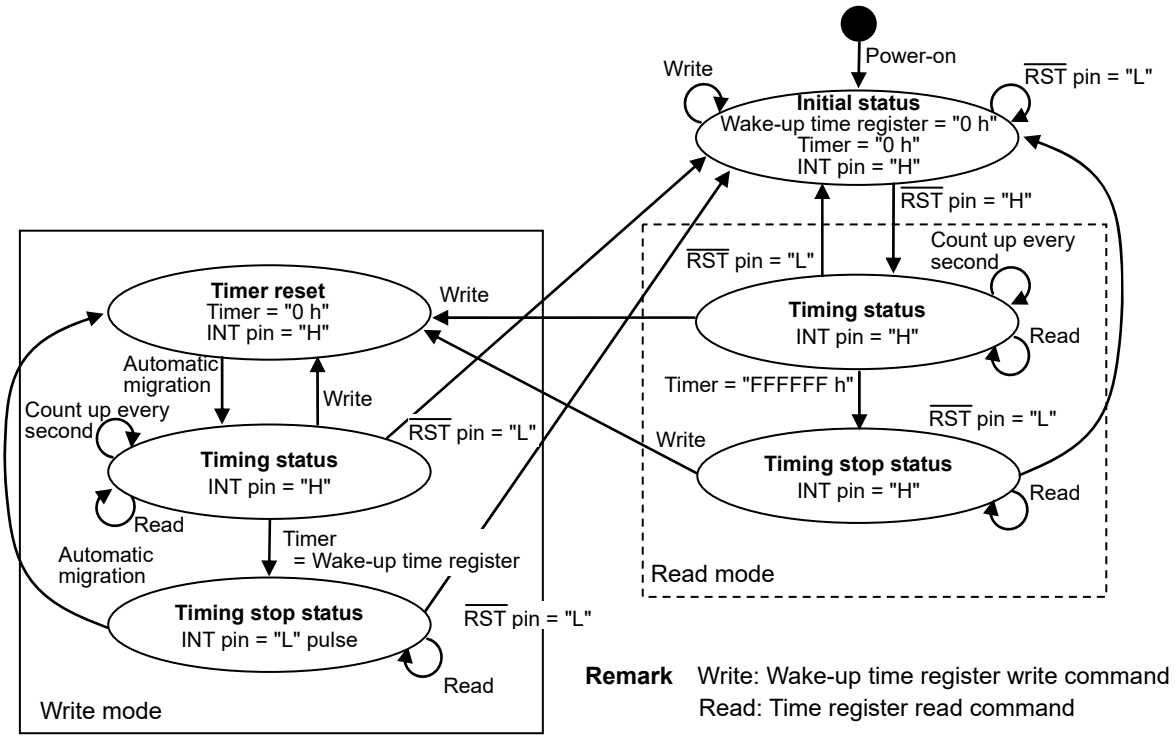


Figure 16 Status Transition Diagram of One-shot Loop Time-out (Nch Open-drain Output)

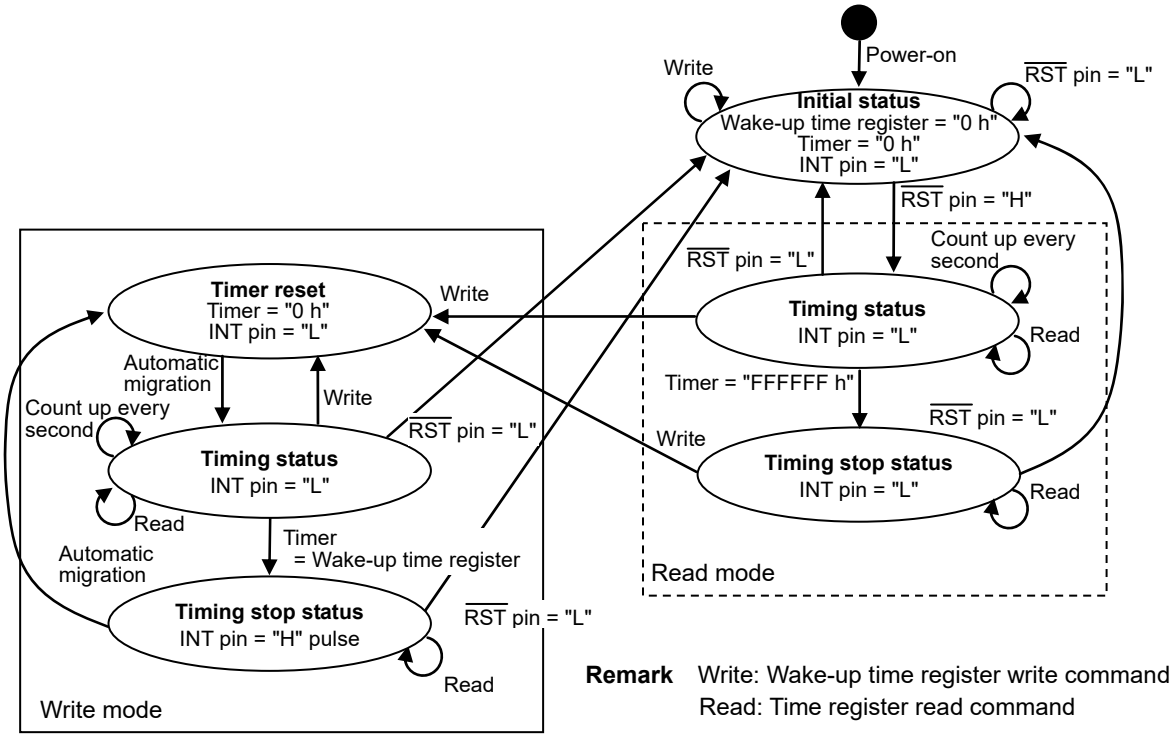


Figure 17 Status Transition Diagram of One-shot Loop Time-out (CMOS Output)

2. Handshake time-out

Handshake time-out is a type to output "L" level interrupt signal from the INT pin.
After the $\overline{RST}$ pin changes from "L" to "H", the timer starts the operation. Then, the INT pin outputs "L" level when the timer value matches the value written to the wake-up time register. When the INT pin outputs "L" level, the timer stops and maintains the timer value.
The timer is reset by inputting "L" to the $\overline{RST}$ pin. After that, if "H" is input to the $\overline{RST}$ pin, the INT pin is set to "H" and the timer restarts the count-up action.

Remark The above description is the example of an Nch open-drain output product.
In a CMOS output product, the INT pin output is the inverse logic of the Nch open-drain output product.

2. 1 Write mode

If write operation is performed to the wake-up time register during the count-up action, the action will be restarted after resetting the timer. This operation is called "write mode".
Before the timer value matches the value written to the wake-up time register, if "L" is input to the $\overline{RST}$ pin, the timer is reset.

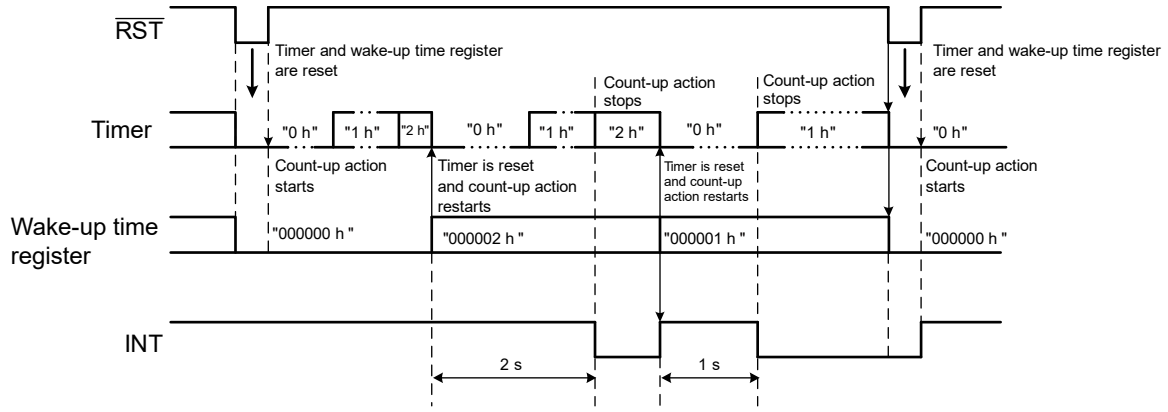


Figure 18 Output Timing of Handshake Time-out (Nch Open-drain Output)

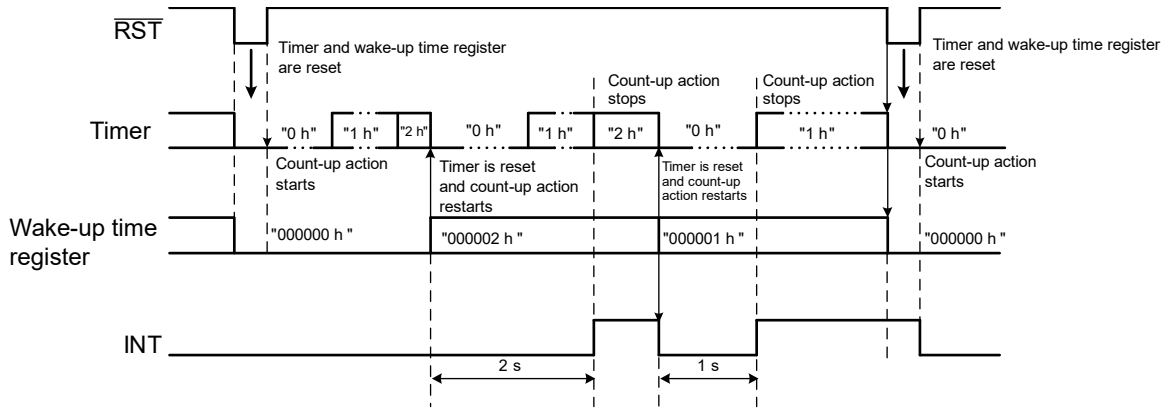
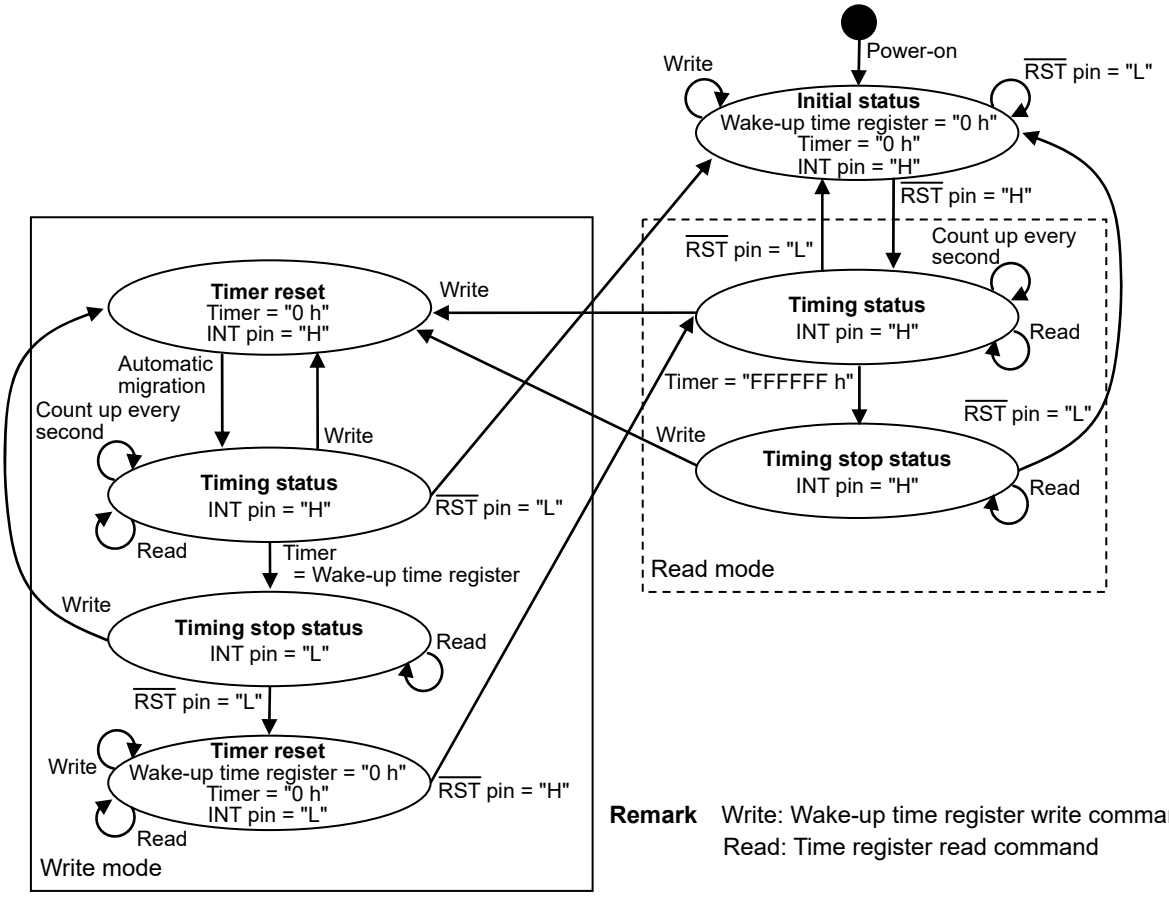


Figure 19 Output Timing of Handshake Time-out (CMOS Output)

2. 2 Read mode

After the timer starts to operate, if write operation is not performed to the wake-up time register, the interrupt signal is not output from the INT pin. The timer stops at "FFFFFF h". The timer value during timing can be confirmed by reading the time register. This operation is called "read mode".
In order for the timer to operate again, set the $\overline{\text{RST}}$ pin from "L" to "H" or perform write operation to the wake-up time register. Regarding the operation, refer to **Figure 14** and **Figure 15**.
Figure 20 and **Figure 21** show the status transition diagrams about the handshake time-out operation.



Remark Write: Wake-up time register write command
Read: Time register read command

Figure 20 Status Transition Diagram of Handshake Time-out (Nch Open-drain Output)

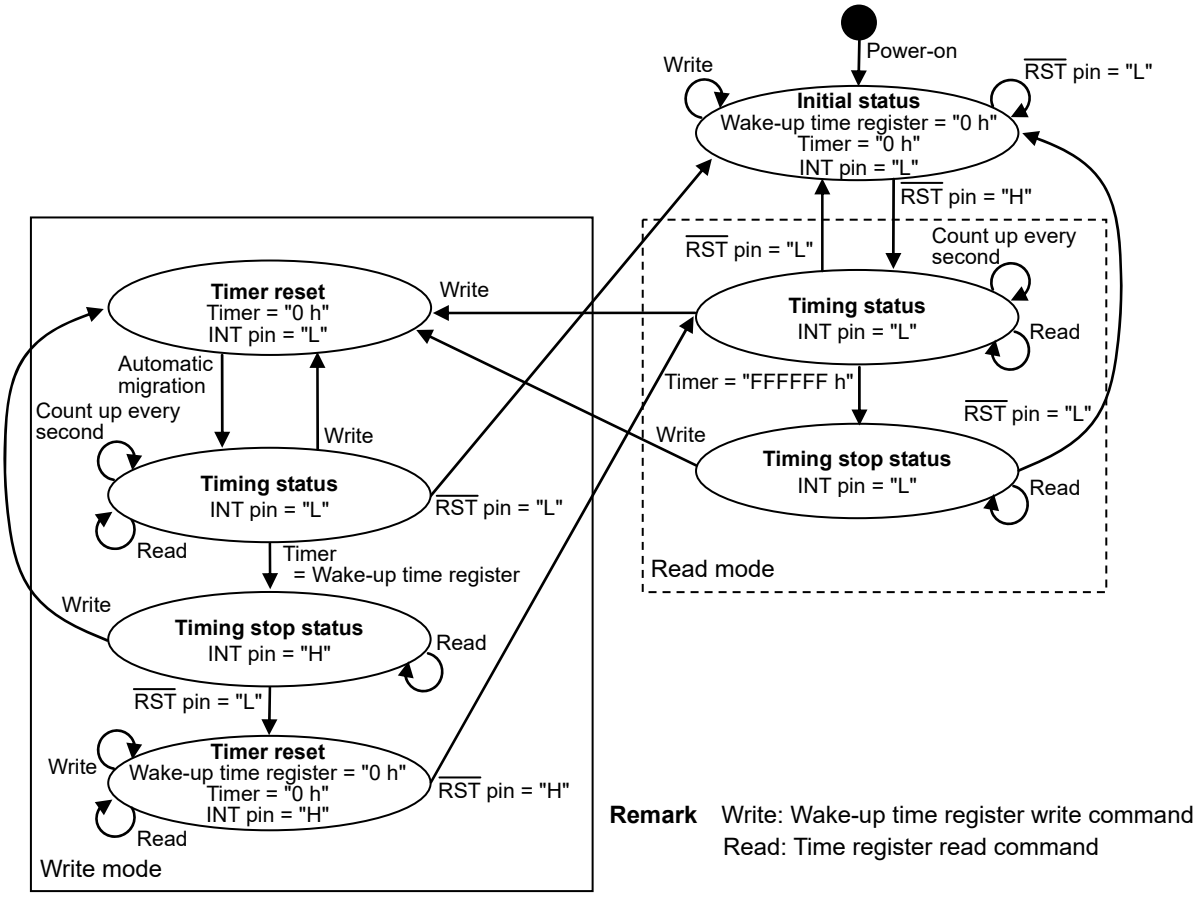


Figure 21 Status Transition Diagram of Handshake Time-out (CMOS Output)

■ Configuration of Registers

1. Time register

The time register is a 3-byte register that stores the timer value in the binary code.
The time register is read-only.
Perform the read operation of the time register in 3-byte unit from TM23 to TM0.

Example: 3 seconds (0000_0000_0000_0000_0000_0011)
45 minutes (0000_0000_0000_1010_1000_1100)
5 hours 30 minutes (0000_0000_0100_1101_0101_1000)

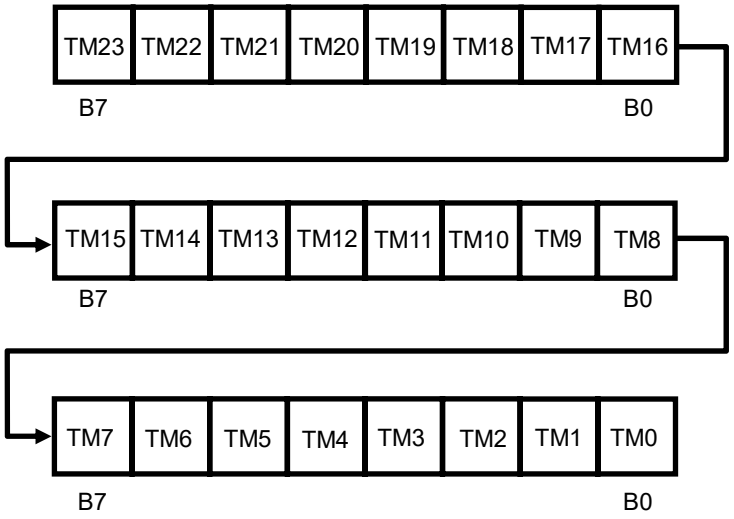


Figure 22

2. Wake-up time register

The wake-up time register is a 3-byte register that stores the wake-up time of the microcontroller in the binary code.
The wake-up time register is possible for write and read.
Perform the write and read operation of the wake-up time register in 3-byte unit from WU23 to WU0.
When performing the read operation of the wake-up time register, set the $\overline{RST}$ pin to "H". If the $\overline{RST}$ pin is set to "L", the time register data is read.

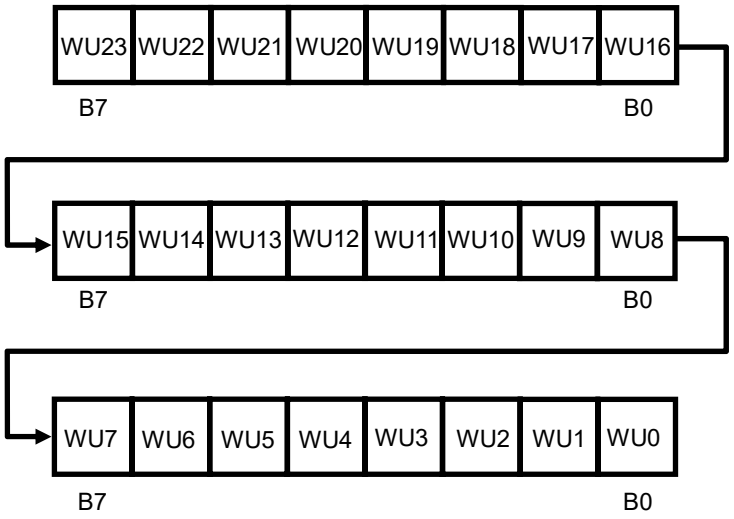


Figure 23

■ Serial Interface

The S-35710 Series transmits and receives various commands via I²C-bus serial interface to read / write data.

1. Start condition

When SDA changes from "H" to "L" with SCL at "H", the S-35710 Series recognizes start condition and the access operation is started.

2. Stop condition

When SDA changes from "L" to "H" with SCL at "H", the S-35710 Series recognizes stop condition and the access operation is completed. The S-35710 Series enters standby mode, consequently.

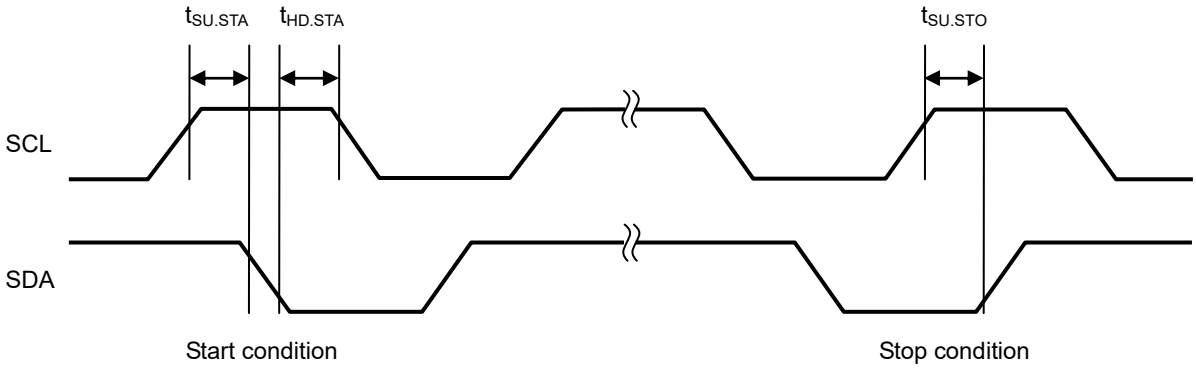


Figure 24 Start / Stop Condition

3. Data transmission and acknowledge

The data transmission is performed at every 1 byte after the start condition detection. Pay attention to the specification of $t_{SU.DAT}$ and $t_{HD.DAT}$ when changing SDA, and perform the operation when SCL is "L". If SDA changes when SCL is "H", the start / stop condition is recognized even during the data transmission, and the access operation will be interrupted.

Whenever a 1-byte data is received during data transimmion, the receiving device returns an acknowledge. For example, as shown in **Figure 25**, assume that the S-35710 Series is a receiving device, and the master device is a transmitting device. If the clock pulse at the 8th bit falls, the master device releases SDA. Consequently, the S-35710 Series, as an acknowledge, sets SDA to "L" during the 9th bit pulse. The access operation is not performed properly when the S-35710 Series does not output an acknowledge.

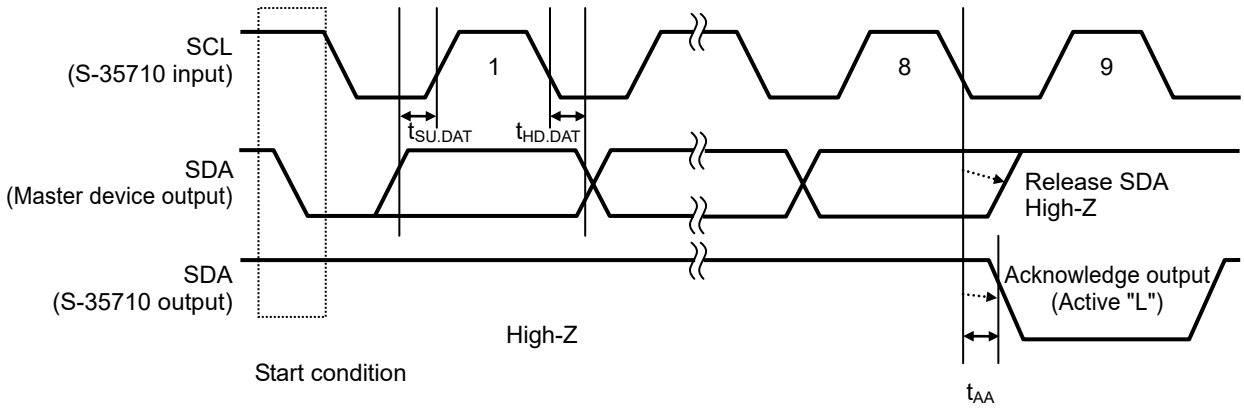


Figure 25 Acknowledge Output Timing

4. Data transmission format

After the start condition transmission, the 1st byte is a slave address and a command (read / write bit) that shows the transmission direction of the data at the 2nd byte or subsequent bytes.

The slave address of the S-35710 Series is specified to "0110010". The data can be written to the wake-up time register when read / write bit is "0", and the data of the wake-up time register or the time register can be read when read / write bit is "1".

When the data can be written to the wake-up time register, input the data from the master device in order of B7 to B0. The acknowledge ("L") is output from the S-35710 Series whenever a 1-byte data is input.

When the data of the wake-up time register or the time register can be read, the data from the S-35710 Series is output in order of B7 to B0 in byte unit. Input the acknowledge ("L") from the master device whenever a 1-byte data is input. However, do not input the acknowledge for the last data byte (NO_ACK). By this, the end of the data read is informed.

After the master device receives / transmits the acknowledge for the last data byte, input the stop condition to the S-35710 Series to finish the access operation.

When the master device inputs start condition without inputting stop condition at this time, the S-35710 Series becomes restart condition, and can transmit / receive the data continuously if the master device inputs the slave address continuously.

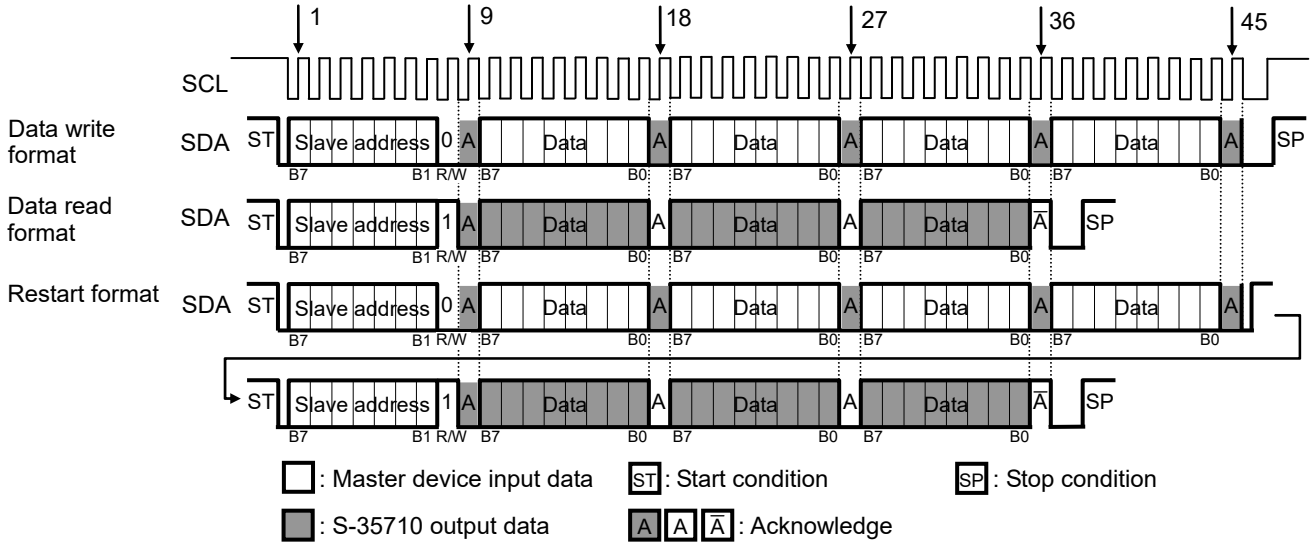


Figure 26 Data Transmission Format of Serial Interface

5. Read operation of time register

Transmit the start condition and slave address from the master device. The slave address of the S-35710 Series is specified to "0110010". Next, the data of the time register can be read when the read / write bit is "1".
The 2nd byte to the 4th byte are used as the time register. Each byte from B7 is transmitted.
When the read operation of the time register is finished, transmit "1" (NO_ACK) to the acknowledge after B0 is output from the master device, and then transmit the stop condition.
The time register is a 3-byte register. "1" is read if the read operation is performed continuously after reading 3 bytes of the time register. Regarding the time register, refer to "■ **Configuration of Registers**".

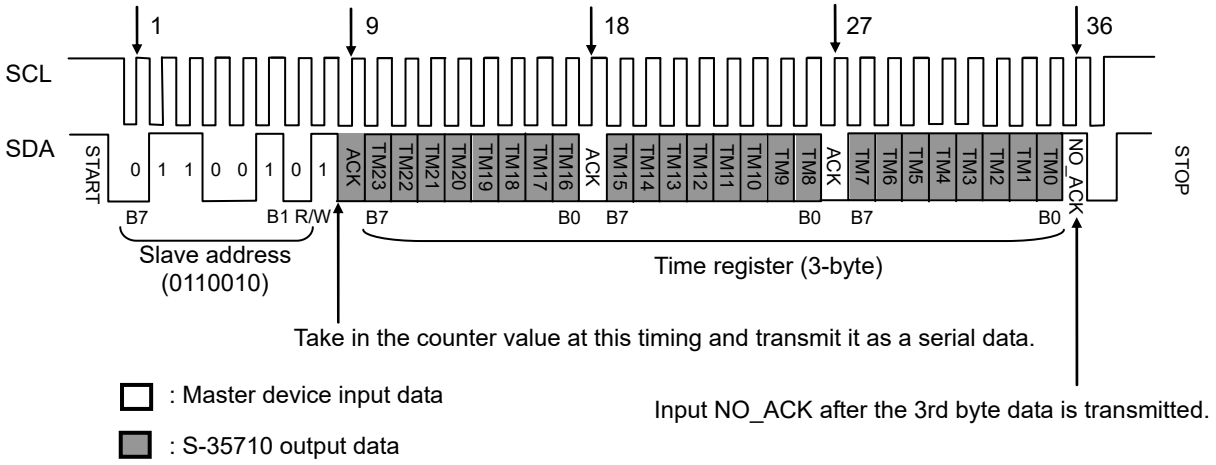
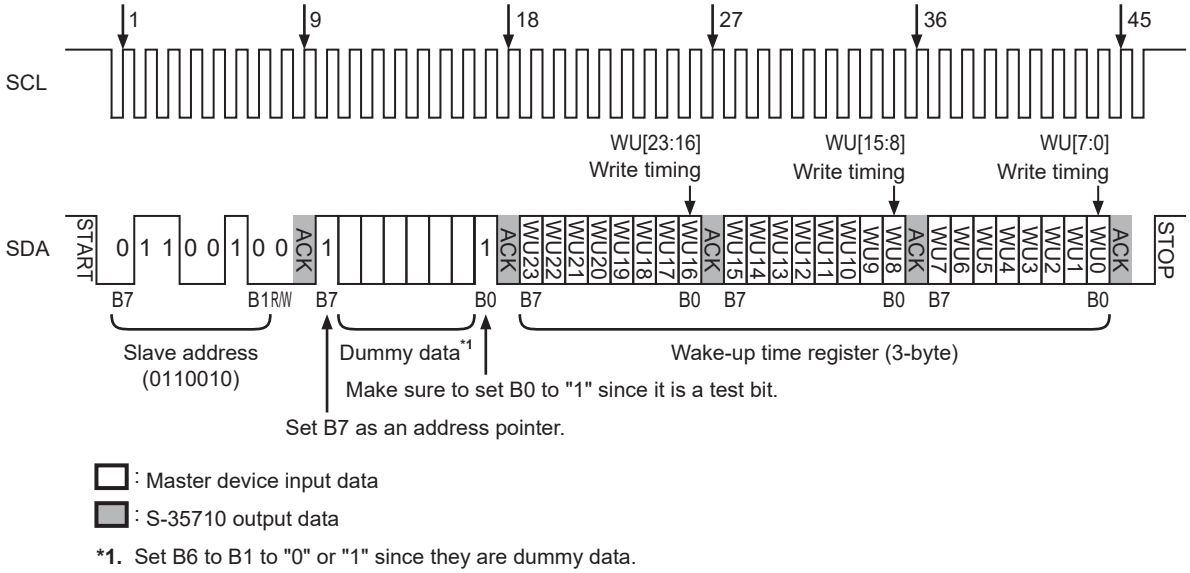


Figure 27 Read Timing of Time Register

6. Write operation of wake-up time register

Transmit the start condition and slave address from the master device. The slave address of the S-35710 Series is specified to "0110010". Next, transmit "0" to the read / write bit.
Transmit the 2nd byte data. Set B7 to "1" since it is an address pointer. Set B6 to B1 to "0" or "1" since they are dummy data. Make sure to set B0 to "1" since it is a test bit.
The 3rd byte to the 5th byte are used as the wake-up time register.
Transmit the stop condition from the master device to finish the access operation.
Regarding the wake-up time register, refer to "■ **Configuration of Registers**".
Write operation of the wake-up time register is performed each byte, so transmit the data in 3-byte unit. Note that the S-35710 Series may not operate as desired if the the data is not transmitted in 3-byte unit.



***1.** Set B6 to B1 to "0" or "1" since they are dummy data.

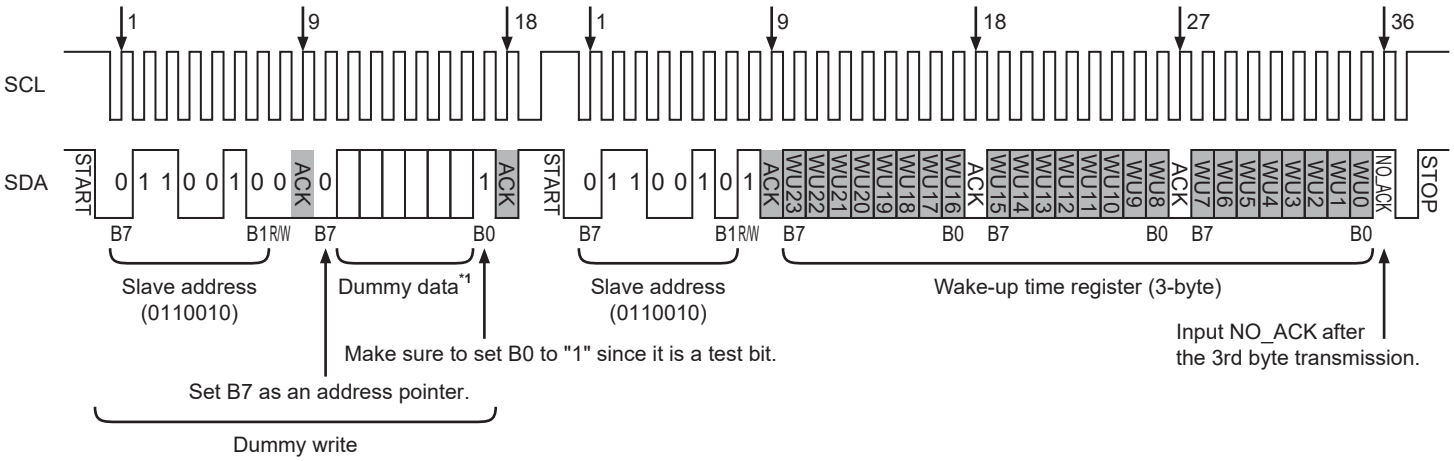
Figure 28 Write Timing of Wake-up Time Register

7. Read operation of wake-up time register

Perform the read operation of the wake-up time register with the restart format. Regarding the restart format, refer to "**4. Data transmission format**".
When performing the read operation of the wake-up time register, set the $\overline{RST}$ pin to "H". If the $\overline{RST}$ pin is set to "L", the time register data is read.

Transmit the start condition and the slave address from the master device. The slave address of the S-35710 Series is specified to "0110010". Next, transmit "0" to the read / write bit.
B7 in the 2nd byte is an address pointer. Set B7 to "0" when reading the wake-up time register. Next, transmit the dummy data to B6 to B1. Make sure to set B0 to "1" since it is a test bit. This processing is called "dummy write".
Then transmit the start condition, the slave address and the read / write bit. The data of the wake-up time register can be read when the read / write bit is set to "1".
Consequently, the data of the wake-up time register is output from the S-35710 Series. Each byte from B7 is transmitted.
When the read operation of the wake-up time register is finished, transmit "1" (NO_ACK) to the acknowledge after B0 output from the master device, and then transmit the stop condition.
The wake-up time register is a 3-byte register. "1" is read if the read operation is performed continuously after reading 3 bytes of the wake-up time register.
Regarding the wake-up time register, refer to "■ **Configuration of Registers**".

Moreover, the internal address pointer is reset if recognizing the stop condition. Therefore, do not transmit the stop condition after dummy write operation. The time register is read if performing the read operation of the register after transmitting the stop condition.



: Master device input data

: S-35710 output data

***1.** Set B6 to B1 to "0" or "1" since they are dummy data.

Figure 29 Read Timing of Wake-up Time Register

■ Release of SDA

The $\overline{RST}$ pin of the S-35710 Series does not perform the reset operation of the communication interface. Therefore, the stop condition is input to reset the internal interface circuit usually.
However, the S-35710 Series does not accept the stop condition from the master device when in the status that SDA outputs "L" (at the time of acknowledge outputting or reading). Consequently, it is necessary to finish the acknowledge output or read operation. **Figure 30** shows the SDA release method.

First, input the start condition from the master device (since SDA of the S-35710 Series outputs "L", the S-35710 Series can not detect the start condition). Next, input the clocks for 1-byte data access (9 clocks) from SCL. During the time, release SDA of the master device. By this, the SDA input / output before communication interrupt is completed, and SDA of the S-35710 Series becomes release status. Continuously, if the stop condition is input, the internal circuit resets and the communication returns to normal status.

It is strongly recommended that the SDA release method is performed at the time of system initialization after the power supply voltage of the master device is raised.

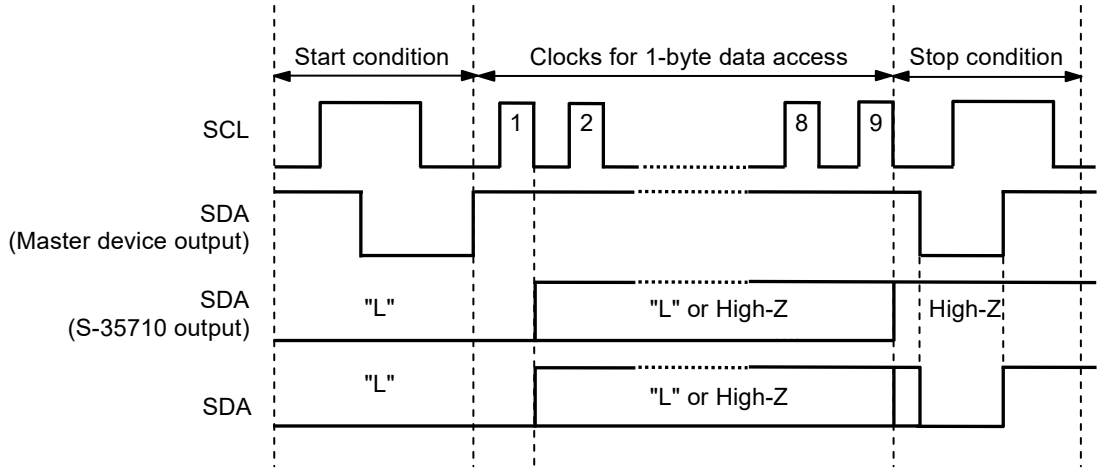
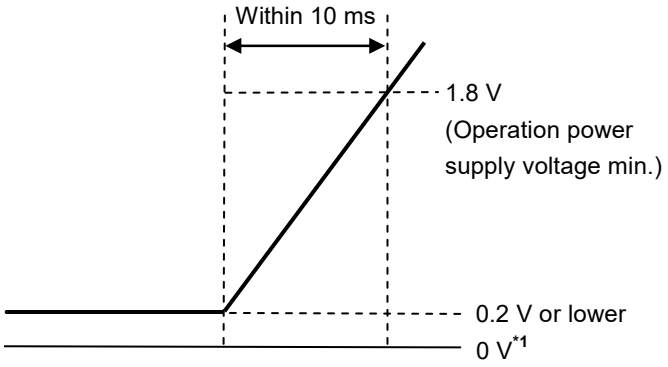


Figure 30 SDA Release Method

■ Power-on Detection Circuit

In order for the power-on detection circuit to operate normally, raise the power supply voltage of the IC from 0.2 V or lower so that it reaches 1.8 V of the operation power supply voltage minimum value within 10 ms, as shown in **Figure 31**.



***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35710 Series.

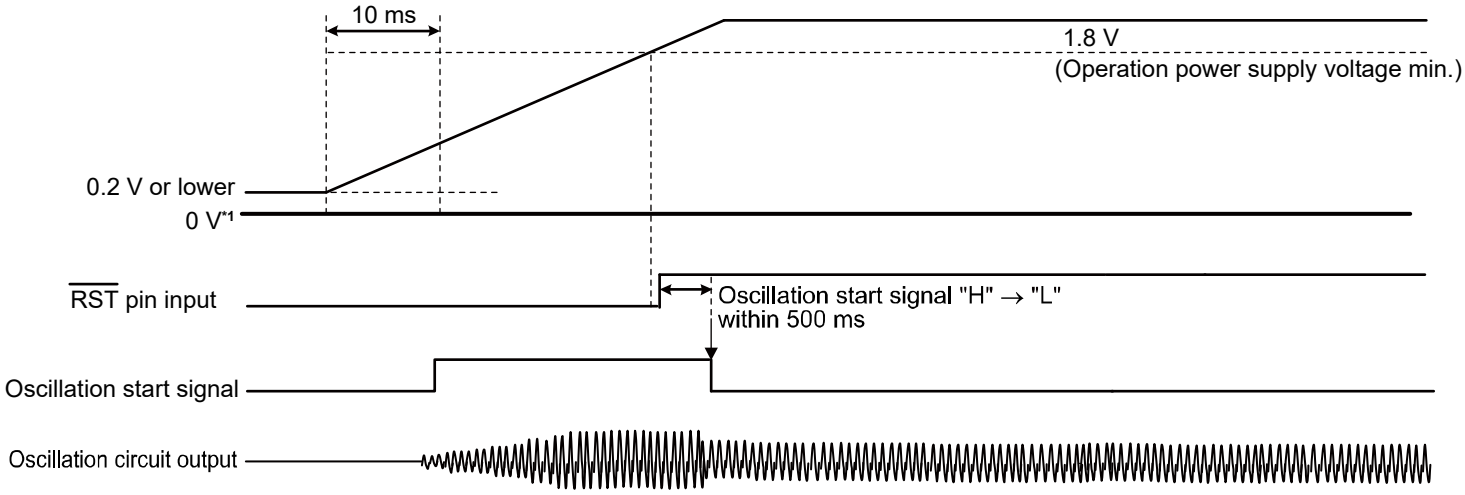
Figure 31 How to Raise Power Supply Voltage

If the power supply voltage of the S-35710 Series cannot be raised under the above conditions, the power-on detection circuit may not operate normally and an oscillation may not start. In such case, perform the operations shown in "**1. When power supply voltage is raised at $\overline{\text{RST}}$ pin = "L"** " and "**2. When power supply voltage is raised at $\overline{\text{RST}}$ pin = "H"**.

1. When power supply voltage is raised at $\overline{\text{RST}}$ pin = "L"

Set the $\overline{\text{RST}}$ pin to "L" until the power supply voltage reaches 1.8 V or higher. While the $\overline{\text{RST}}$ pin is set to "L", the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. If the $\overline{\text{RST}}$ pin is set to "H" after the power supply voltage reaches 1.8 V, the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained.
The current consumption increases as mentioned below while the $\overline{\text{RST}}$ pin is set to "L".

- When a product without a pull-up resistor is selected: 1.7 μA typ.
- When a product with a pull-up resistor is selected: 30 μA typ.



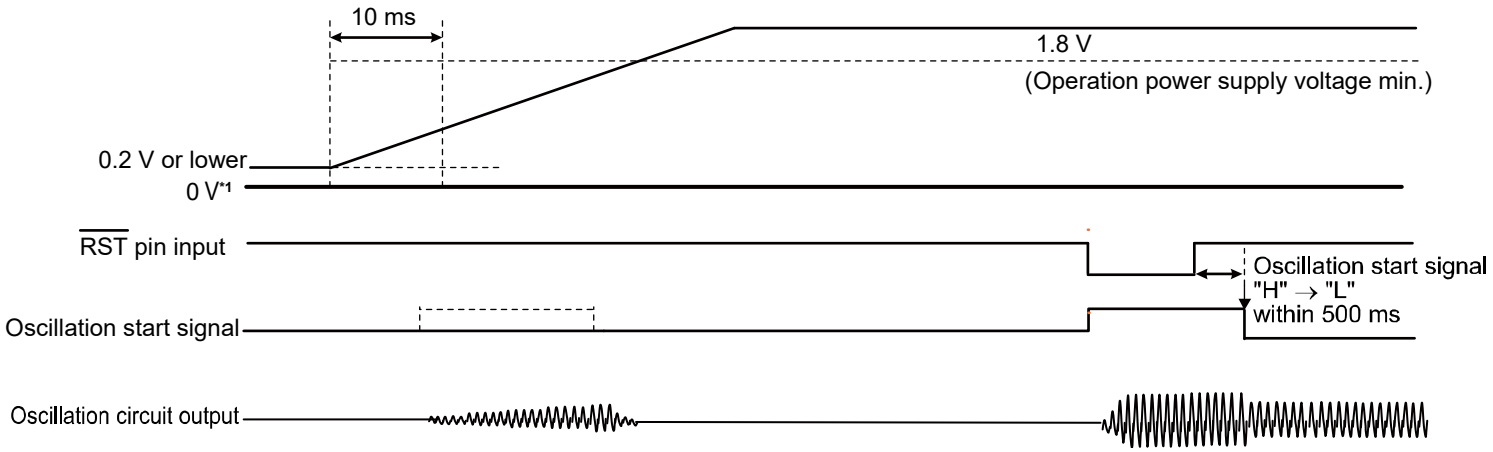
***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35710 Series.

Figure 32 When Power Supply Voltage is Raised at $\overline{\text{RST}}$ Pin = "L"

2. When power supply voltage is raised at $\overline{\text{RST}}$ pin = "H"

Set the $\overline{\text{RST}}$ pin to "L" after the power supply voltage reaches 1.8 V or higher. If the $\overline{\text{RST}}$ pin is set to "L" for 500 ms or longer, the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. After that, if the $\overline{\text{RST}}$ pin is set to "H", the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained. The current consumption increases as mentioned below while the $\overline{\text{RST}}$ pin is set to "L".

- When a product without a pull-up resistor is selected: 1.7 μA typ.
- When a product with a pull-up resistor is selected: 30 μA typ.



***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35710 Series.

Figure 33 When Power Supply Voltage is Raised at $\overline{\text{RST}}$ Pin = "H"

The $\overline{\text{RST}}$ pin has a built-in chattering elimination circuit. To determine the $\overline{\text{RST}}$ pin "H" input, perform communication subsequent to setting the interval of 3.5 periods (0.438 seconds) of clock (8 Hz) or longer after the $\overline{\text{RST}}$ pin changes from "L" to "H".
Regarding the chattering elimination of the $\overline{\text{RST}}$ pin, refer to "■ **$\overline{\text{RST}}$ Pin**".

■ $\overline{\text{RST}}$ Pin

1. Chattering elimination

The $\overline{\text{RST}}$ pin has a built-in chattering elimination circuit, and the output logic is active "L".
Sampling is carried out 3 times at a clock period of 8 Hz and the $\overline{\text{RST}}$ pin input signal is verified. If all of the sampling results are "L", the counter is reset, if all the results are "H", a count-up action is started.
The chattering elimination circuit can eliminate the pulse width of 2 periods (approximately 0.25 seconds) of the clock (8 Hz). To determine the $\overline{\text{RST}}$ pin "L" or "H" input, maintain the $\overline{\text{RST}}$ pin "L" or "H" input during the period longer than 3.5 periods (0.438 seconds) of clock (8 Hz). This is because, for example, if the $\overline{\text{RST}}$ pin "L" or "H" input is 0.375 seconds, the input may not be determined depending on the clock timing.

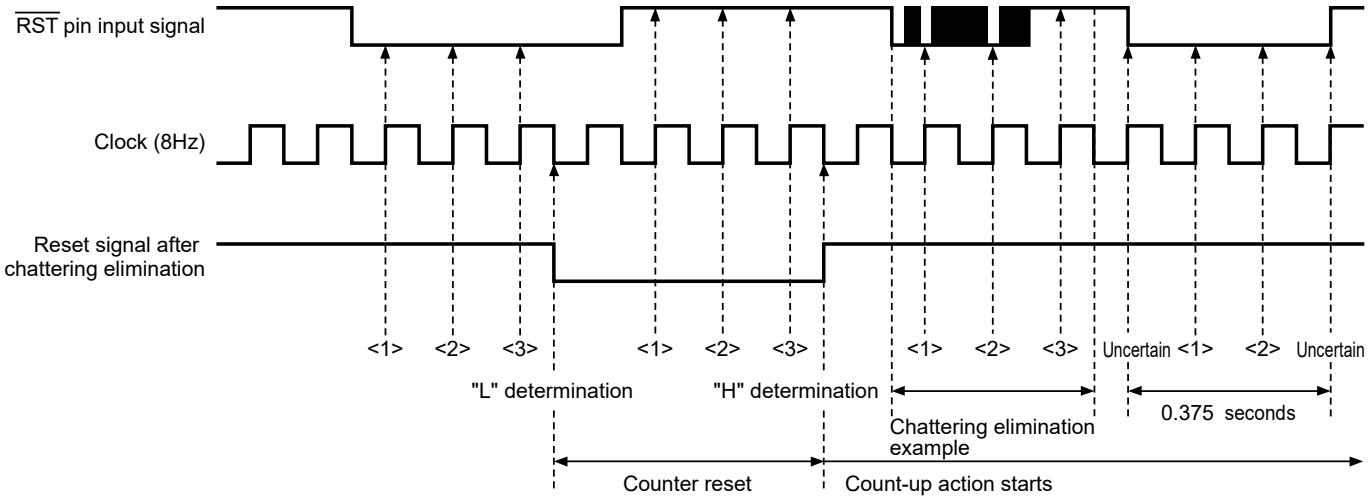


Figure 34 Example: Timing Chart of Chattering Elimination

2. Operation at power-on

At power-on, the reset signal after chattering elimination is "L" regardless of the $\overline{\text{RST}}$ pin status. Consequently, the S-35710 Series becomes initial status (Refer to "**Figure 16 Status Transition Diagram of One-shot Loop Time-out (Nch Open-drain Output)**", "**Figure 17 Status Transition Diagram of One-shot Loop Time-out (CMOS Output)**" and "**Figure 20 Status Transition Diagram of Handshake Time-out (Nch Open-drain Output)**", "**Figure 21 Status Transition Diagram of Handshake Time-out (CMOS Output)**") and can not perform write operation to the wake-up time register. When the reset signal after chattering elimination is "L", the no acknowledge is output in the 2nd or subserquent bytes if write operation is performed to the wake-up time register.
If the crystal oscillation circuit starts to oscillate after power-on, the clock operates and the reset signal after chattering elimination becomes "H", the S-35710 Series then migrates to read mode. This makes the write operation to the wake-up time register possible. **Figure 35** shows the timing chart at power-on.
The write-disable time period of the wake-up time register showed in **Figure 35** changes according to the oscillation start time. If the no acknowledge is output from the S-35710 Series at the time of write operation to the wake-up time register immediately after power-on, it is recommended to set a time interval of approximately 0.5 seconds to 1 second for the next communication until the oscillation is stabilized.

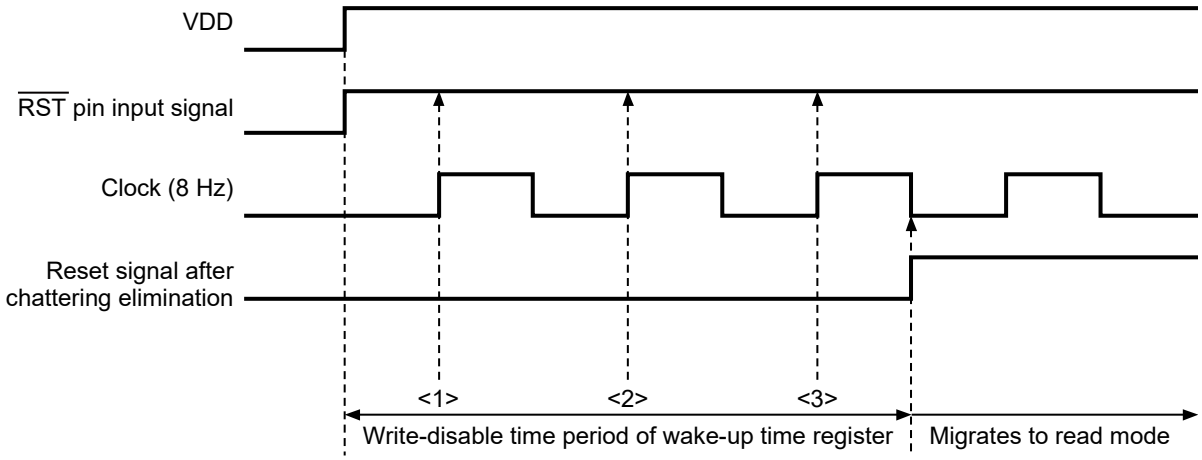
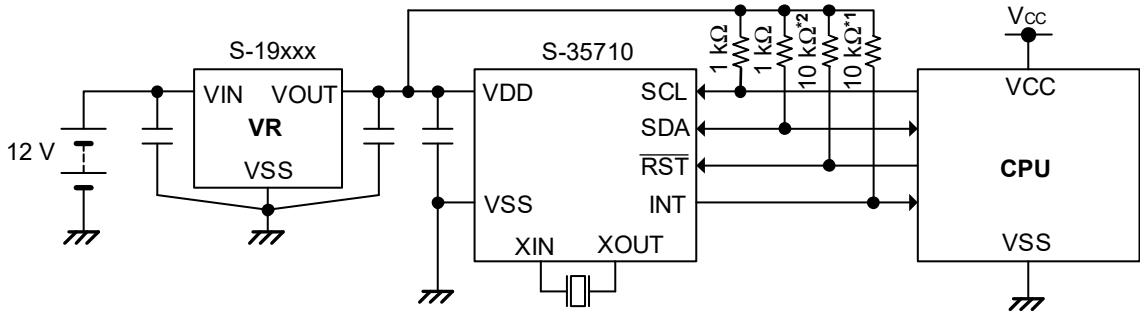


Figure 35 Timing Chart at Power-on

■ Example of Application Circuit



***1.** This resistor is unnecessary when a CMOS output product is selected.
***2.** This resistor is unnecessary when a product with a pull-up resistor is selected.

Figure 36

Caution 1. Start communication under stable condition after turnig on the system power supply.
2. The above connection diagrams do not guarantee operation. Set the constants after performing sufficient evaluation using the actual application.

■ Configuration of Crystal Oscillation Circuit

Since the S-35710 Series has built-in capacitors (C_g and C_d), adjustment of oscillation frequency is unnecessary.
However, the crystal oscillation circuit is sensitive to external noise and parasitic capacitance (C_P), these effects may become a factor to worsen the clock accuracy. Therefore, the following steps are recommended for optimizing the configuration of crystal oscillation circuit.

- Locate the bypass capacitor adjacent to the power supply pin of the S-35710 Series.
- Place the S-35710 Series and the quartz crystal as close to each other as possible, and shorten the wiring.
- Increase the insulation resistance between pins and the board wiring patterns of XIN and XOUT.
- Do not place any signal or power lines close to the crystal oscillation circuit.
- Locate the GND layer immediately below the crystal oscillation circuit.
  (In the case of a multi-layer board, only the layer farthest from the crystal oscillation circuit should be located as the GND layer. Do not locate a circuit pattern on the intermediate layers.)

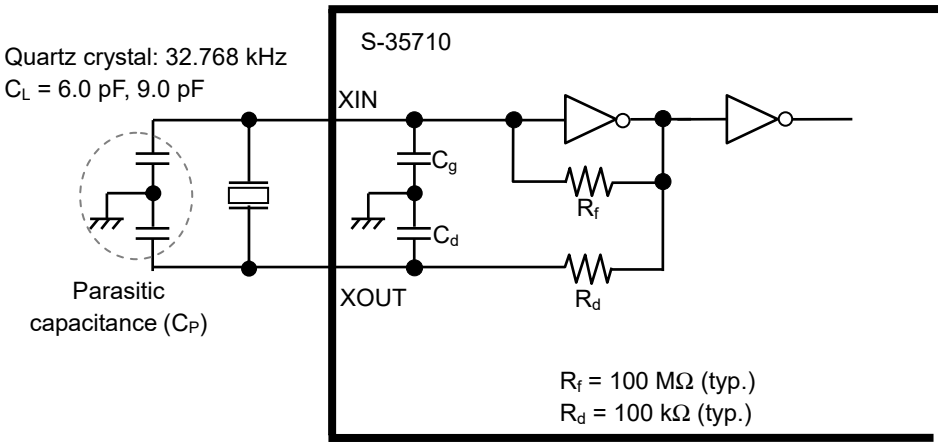


Figure 37 Configuration of Crystal Oscillation Circuit

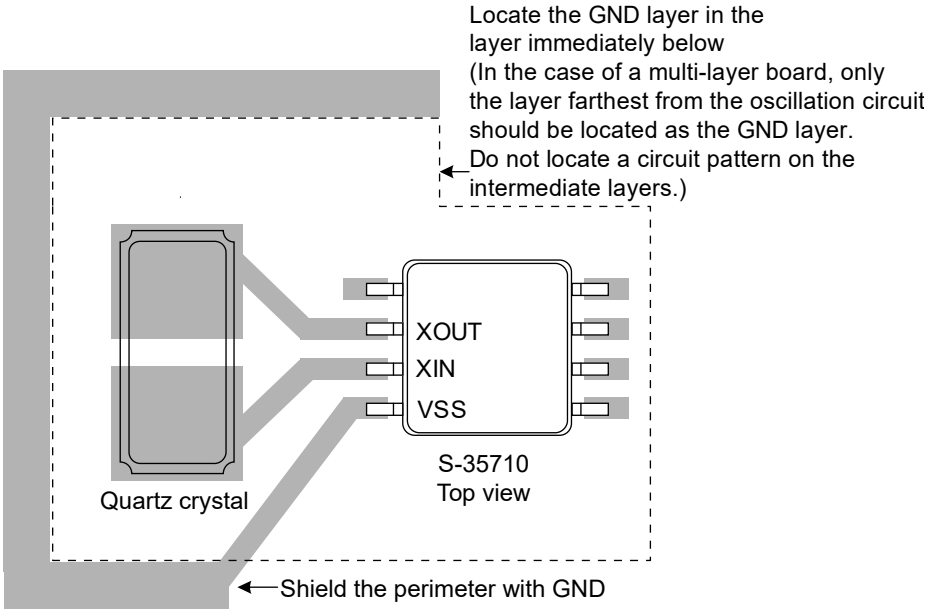


Figure 38 Example of Recommended Connection Pattern Diagram

Caution 1. Oscillation characteristics are subject to the variation of each component such as board parasitic capacitance, parasitic resistance, quartz crystal and external capacitor. When configuring crystal oscillation circuit, pay sufficient attention for them.
2. When using the product in automobile equipment, select the components which can be automobile carried for each component such as quartz crystal, external capacitor and board.

■ Cautions When Using Quartz Crystal

Request a matching evaluation between the IC and a quartz crystal to the quartz crystal maker.
Refer to **Table 10** for recommended quartz crystal characteristics values. When using a product in an environment over Ta = +85°C, it is recommended to ensure the oscillation allowance shown in **Table 10** at room temperature.

Table 10 Quartz Crystal Characteristics

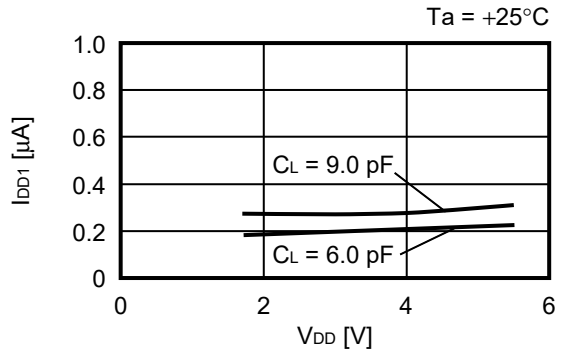
Quartz Crystal C_L Value (Load Capacitance)	R_1 Value (Equivalent Series Resistance)	Oscillation Allowance at Power-on
9.0 pF	80 kΩ max.	5 times or more
6.0 pF	80 kΩ max.	5 times or more

■ Precautions

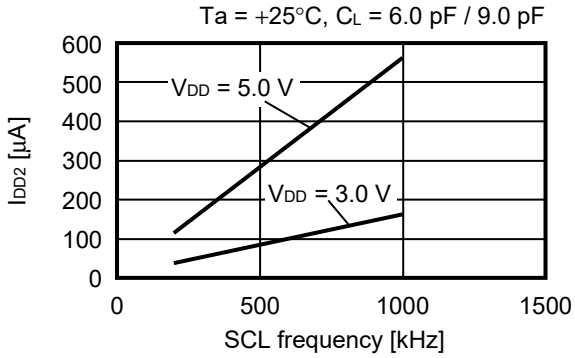
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

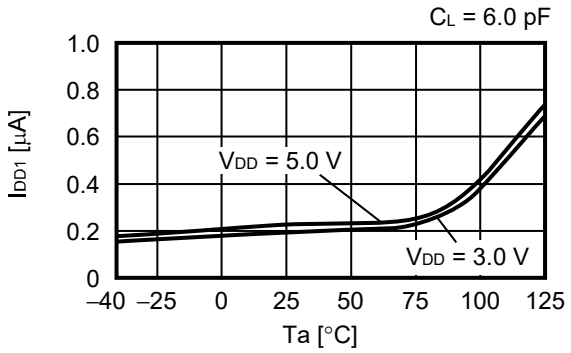
1. Current consumption 1 vs. Power supply voltage characteristics



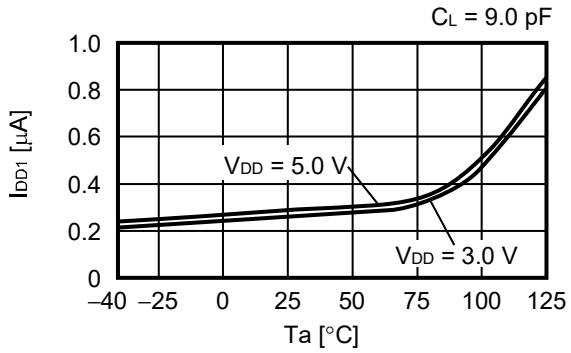
2. Current consumption 2 vs. SCL frequency characteristics



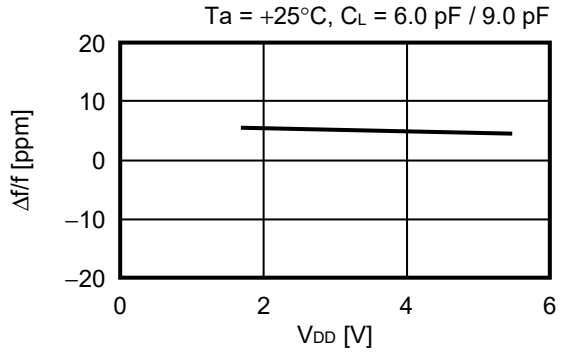
3. Current consumption 1 vs. Temperature characteristics



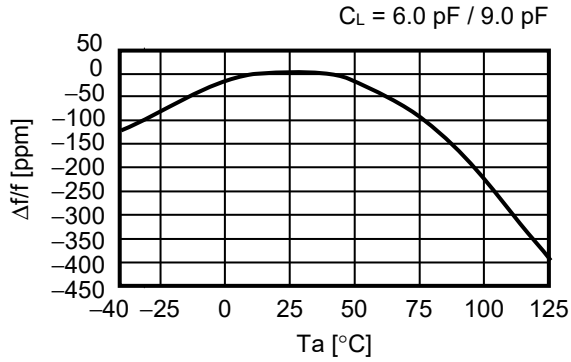
4. Current consumption 1 vs. Temperature characteristics



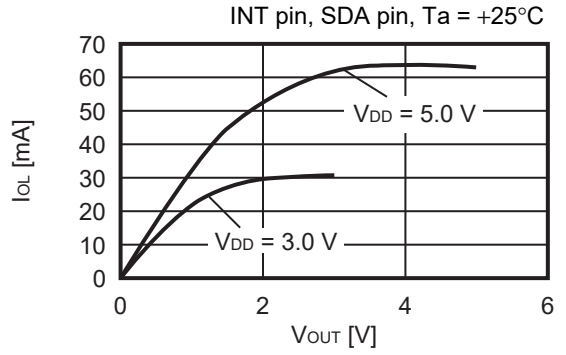
5. Oscillation frequency vs. Power supply voltage characteristics



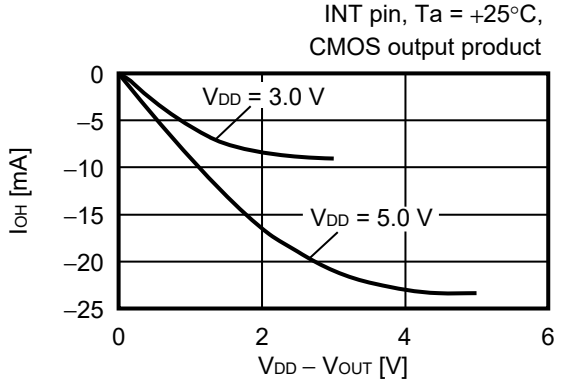
6. Oscillation frequency vs. Temperature characteristics



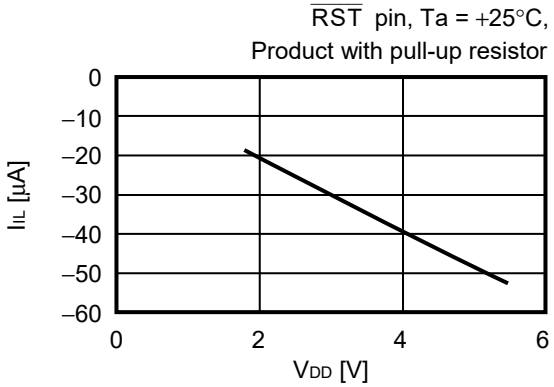
7. Low level output current vs. Output voltage characteristics

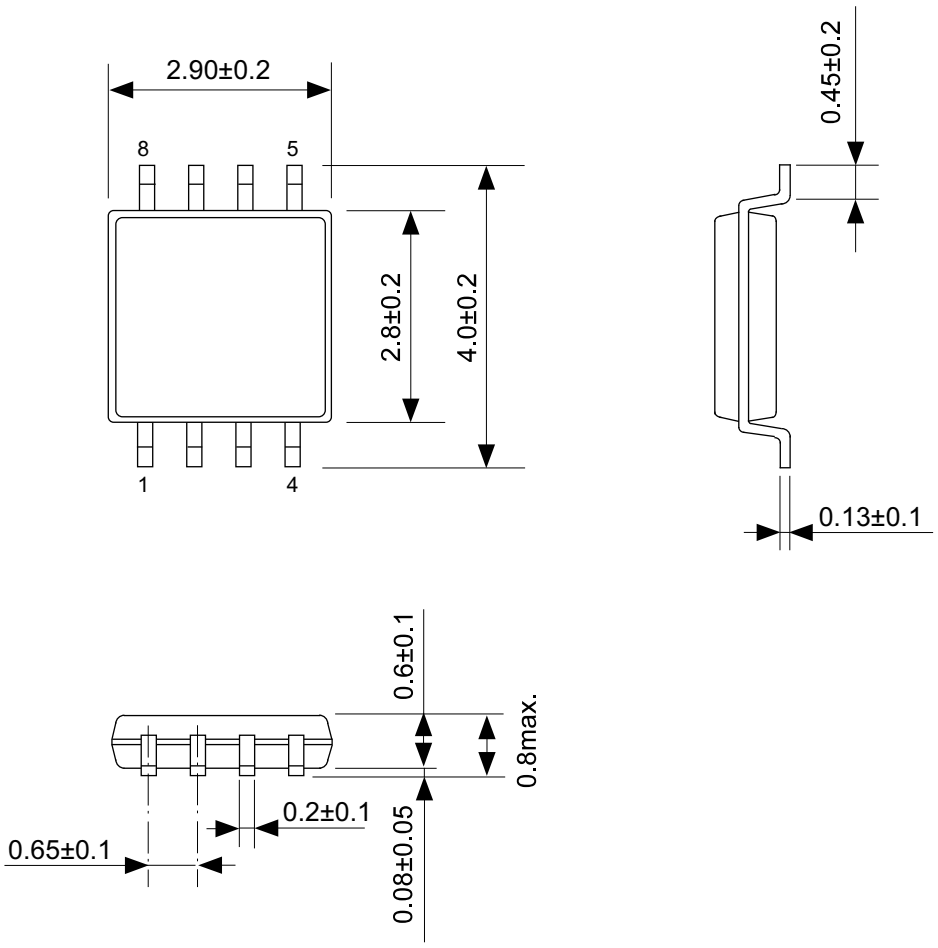


8. High level output current vs. V_{DD} – V_{OUT} characteristics



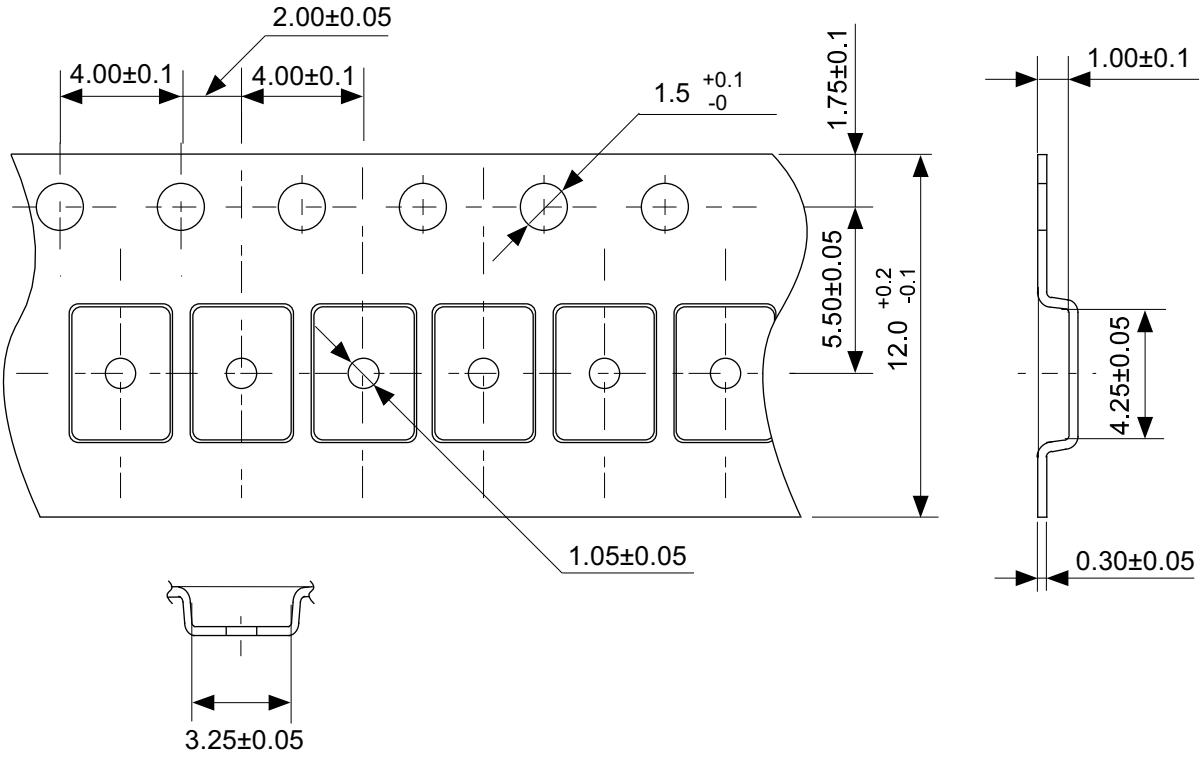
9. Low level input current vs. Power supply voltage characteristics

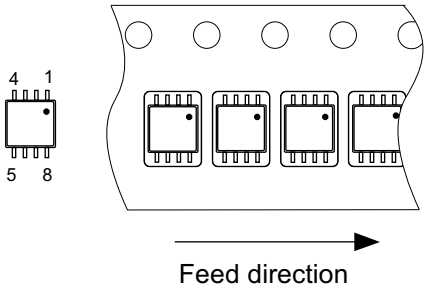




No. FM008-A-P-SD-1.2

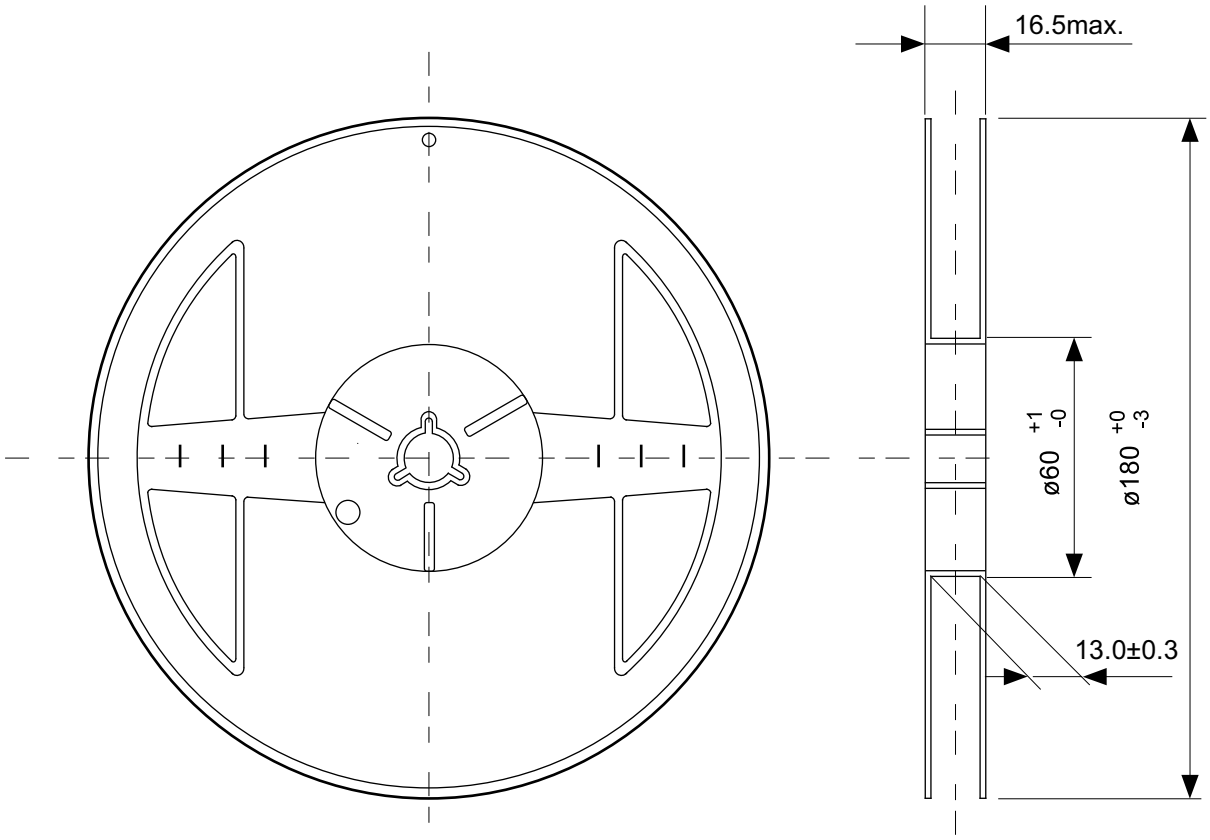
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	



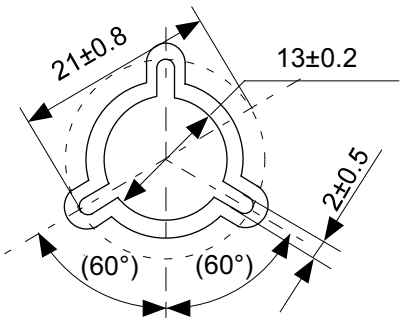


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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