Index

Features 1
Functions 1
Dimensions 1
Block Diagram 2
Pin Configuration 2
Pin Description 3
Electrical Characteristics 4
Test Circuits 5
Absolute Maximum Ratings 5
Ordering Information 5
POCSAG Signal Code Format 6
Flow Chart 8
Basic Operation 10
Internal Functions 16
Circuit Design 21

PAGING DECODER IC (POCSAG)

S-7040D

The S-7040D decoder IC has been designed in accordance with the CCIR* Radio Paging Code Number 1 (POCSAG** code). The S-7040D can be used for display pager since it processes the POCSAG signal internally and sends the decoded data to an external microprocessor. Furthermore the S-7040D can also be used for tone-only pager without a microprocessor. Eight kinds of paging tone cadences are generated for valid pagings to make the user know which information is received. The S-7040D has a battery saving function which drives signal receiving circuit intermittently.

* CCIR: International Radio Consultative Committee
** POCSAG: Post Office Code Standardization Advisory Group.

■ Features

- Operating voltage : 1.7 to 3.6 V (3.0 V typ.)
- Current consumption : 50 μA max. (3.0 V)
- Data rate : 512/1200 bps selectable (76kHz crystal)
  512bps (32kHz crystal)
- User address : 4 (2addresses/frame)
- User frame : 2
- Four cadences per an address
- External elements:
  Crystal oscillator (32 KHz/76 KHz), C_G, R_F
- Direct interface to IDROM (S-29131A / S-2913)
- 3 paging signals : Tone, LED, Vibrator
- CPU direct interface
  CPU control output and reference clock output for CPU (32 KHz or 76 KHz)

■ Functions

- Power on clearing
- BCH correction up to 2 bits
- Battery saving
- Battery low alert
- Extended function

■ Dimensions

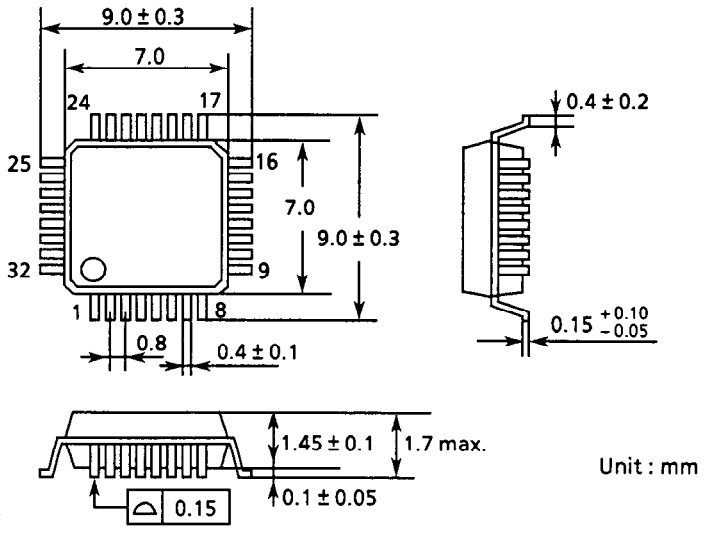


Figure 1

■ Block Diagram

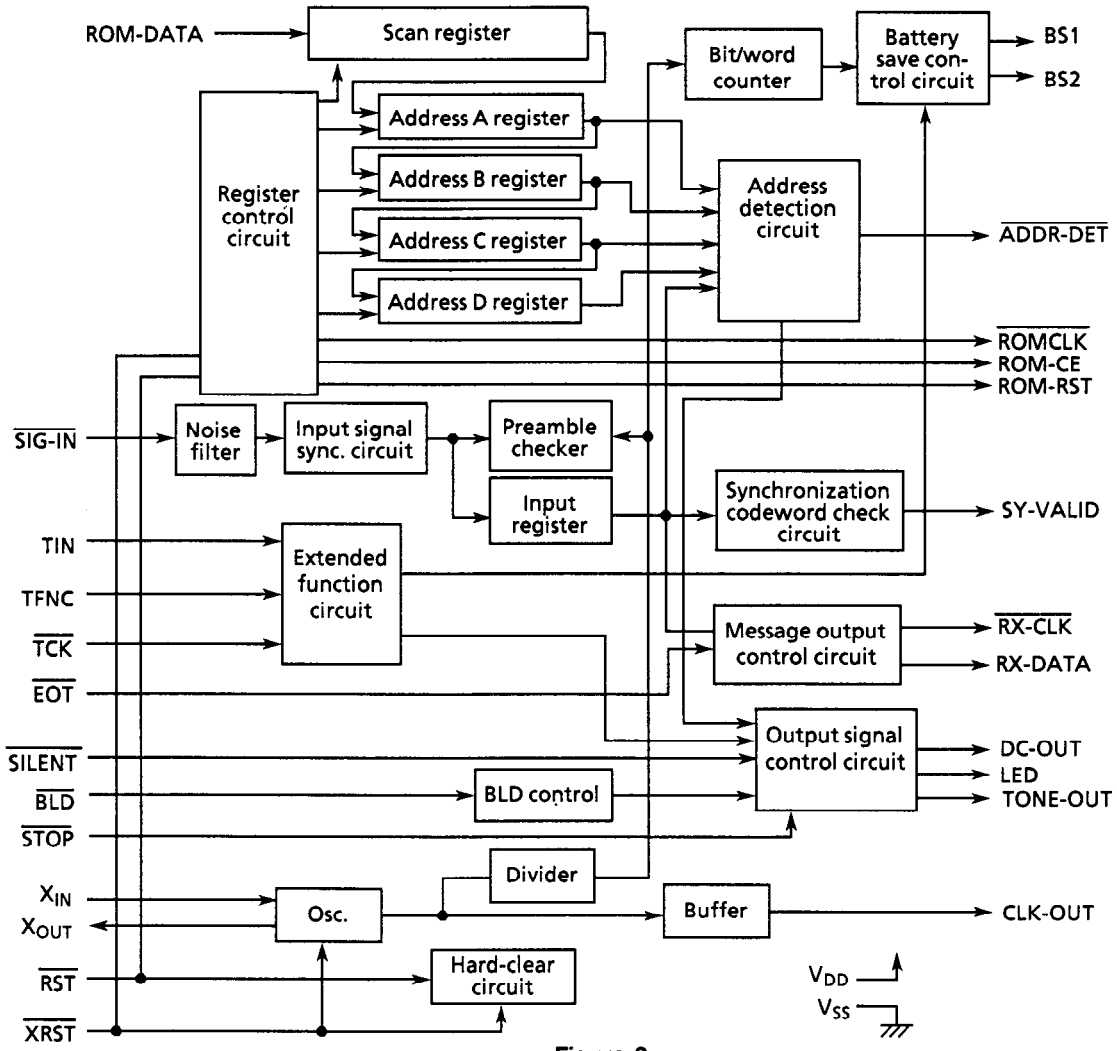


Figure 2

■ Pin Configuration

32-pin QFP

Top view

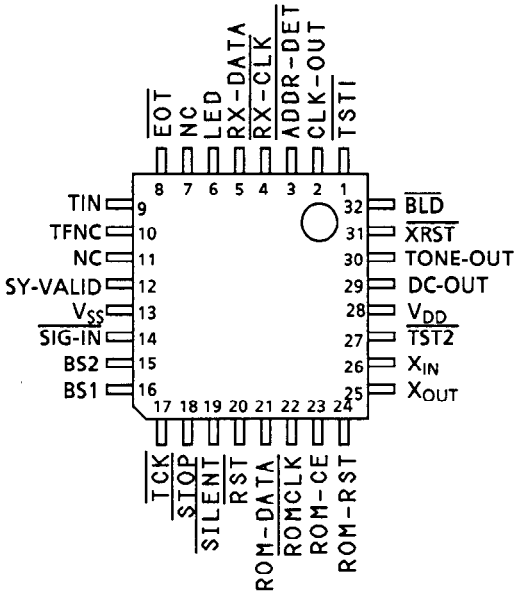


Figure 3

■ Pin Description

Table 1

Pin#	Name	In/Out	Description	Reset	Pull-up
1	$\overline{TST1}$	In	Test mode set pin. Ordinarily "H" or "OPEN".		○
2	CLK-OUT	Out	System clock output pin. Clock of oscillation circuit is buffered and transmitted.		
3	$\overline{ADDR\text{-}DET}$	Out	This pin will go "L" when programmed address is detected and will go "H" after output of received data.	H	
4	$\overline{RX\text{-}CLK}$	Out	Timing clock for received data output. Serial output of received data is enabled in synchronous to falling edge of the clock.	H	
5	RX-DATA	Out	Output pin for received data.	L	
6	LED	Out	Timing signal output pin for LED driving.	L	
7	—	—	Not connected (NC)	—	—
8	$\overline{EOT}$	In	This pin finishes message reception. A pulse signal input to this pin terminates reception forcibly.		○
9	TIN	In	Extended data input pin.		○
10	TFNC	In	Input pin for extended mode selection.		○
11	—	—	Not connected (NC)	—	—
12	SY-VALID	Out	This pin will go "H" when sync-code is detected and will go back "L" when the detection is failed. "H" is held during retry. This pin indicates that message reception is possible.	L	
13	V_{SS}	—	Negative power supply terminal.	—	—
14	$\overline{SIG\text{-}IN}$	In	Input pin for serial data (NRZ signal) from RF circuit (logic inversion is enabled by register). This pin has noise reduction circuit. Duty cycle of 25 to 75% is required.		
15	BS2	Out	Output pin for quick charge signal to RF circuit reference voltage.	L	
16	BS1	Out	Output pin for control signal of RF circuit power supply.	L	
17	$\overline{TCK}$	In	Extended clock input pin.		○
18	$\overline{STOP}$	In	External control to this pin inhibits TONE-OUT and LED output.		○
19	$\overline{SILENT}$	In	LED or vibrator is selected for call device when this pin is set "L" while TONE-OUT output for call is suppressed.		○
20	$\overline{RST}$	In	Input pin for reset with pull-up. Power on clear is enabled by attaching a condenser.		○
21	ROM-DATA	In	Input pin for IDROM data.		
22	$\overline{ROMCLK}$	Out	Output pin for IDROM synchronization clock.	Z	
23	ROM-CE	Out	Output pin for IDROM chip enable.	PL	
24	ROM-RST	Out	Output pin for IDROM reset.	Z	
25	X_{OUT}	Out	Output pin for crystal oscillator.		
26	X_{IN}	In	Input pin for crystal oscillator.		
27	$\overline{TST2}$	In	Input pin for test. Ordinarily "H" or "OPEN".		○
28	V_{DD}	—	Positive power supply terminal.	—	—
29	DC-OUT	Out	Timing signal output pin for vibrator control.	L	
30	TONE-OUT	Out	Output pin for paging tone. Tone frequencies are 2.7 KHz /3.2 KHz.	L	
31	$\overline{XRST}$	In	Input pin for oscillation control. "H" to this pin enables oscillation. "L" disables oscillation and resets the internal circuit. IDROM data is fetched after recovery. Connect to V_{DD} when the pin is not used. No pull-up.		
32	$\overline{BLD}$	In	This pin samples detection signal for voltage lowering of battery. Two continual detection of "L" leads to BLD tone output.		

Note
1. Reset means the state of each pin when $\overline{RST}$ = "L". Z stands for high impedance and PL for pull-down.
2. "○" in pull-up column means that the pin is pulled up to V_{DD}.

■ Electrical Characteristics

Table 2

(V_{DD} = 3.0 V, V_{SS} = 0 V, Ta = 25°C unless otherwise specified.)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Circuit	Note
Operating voltage	V_{DD}	Ta = -10°C~ + 70°C		1.7	3.0	3.6	V	①	1
Oscillation start voltage	V_{DOB}	Ta = -10°C~ + 70°C		2.0	—	3.6	V	①	2
Total average standby current consumption	I_N	f_O = 32768 Hz	V_{DD} = 1.7 V	—	4	15	μA	①	3
			V_{DD} = 3.0 V	—	20	40			
		f_O = 76800 Hz	VDD = 1.7 V	—	5	20			
			V_{DD} = 3.0 V	—	25	50			
Total leakage current	I_S	V_{DD} = 3.0 V		—	0.1	1.0	μA		—
TONE-OUT/LED output current	I_{OH1}	V_{DD} = 1.9 V, V_{OH} = 1.6 V		—	—	-500	μA		4
	I_{OL1}	V_{DD} = 1.9 V, V_{OL} = 0.3 V		500	—	—			
DC-OUT output current	I_{OH2}	V_{DD} = 1.9 V, V_{OH} = 1.6 V		—	—	-1000	μA		4
	I_{OL2}	V_{DD} = 1.9 V, V_{OL} = 0.3 V		1000	—	—			
Output voltage	V_{OH}	I_{OH} = -50 μA, V_{DD} = 3.0 V (*)		2.90	—	—	V		—
	V_{OL}	I_{OL} = 50 μA, V_{DD} = 3.0 V (*)		—	—	0.10			
Input voltage	V_{IH}	V_{DD} = 1.7~3.6 V		0.8 × V_{DD}	—		V	②	—
	V_{IL}	V_{DD} = 1.7~3.6 V		—	—	0.2 × V_{DD}			
Input current	V_{IN}	V_{IN} = V_{DD} or V_{SS}	No pull-up nor pull-down	—	—	± 0.1	μA	③	—
Pull-up current	I_{R1}	V_{IL} = 0 V (**)		-20	-10	-5	μA	④	—
	I_{R2}	V_{IH} = 2.8 V (**)		-100	-50	-25			
Pull-down current	I_{R3}	V_{IH} = 3.0 V (***)		20	10	5	μA		—
Power on capacitance	C_{PON}	External capacitance for power on clear		100	1000	10000	pF	—	—
$\overline{RST}$ pulse width	t_{RST}	Forcible signal input		10	—	—	μs	—	—
STOP pulse width	t_{STOP}			10	—	—	ms	—	—
$\overline{SILENT}$ pulse width	t_{SLNT}			10	—	—	ms	—	—
$\overline{EOT}$, TFNC, TIN, $\overline{TCK}$ pulse width	t_{CHAT}	76kHz/32kHz		30/70	—	—	μs	—	—
Frequency to IC deviation	△f/△IC			—	—	± 50	ppm	—	5
Frequency to voltage deviation	△f/△V			—	—	± 8	ppm	—	6
Recommended equivalent resistance	CI			—	—	45	kΩ	—	—

* CLK-OUT, $\overline{ADDR\text{-}DET}$, $\overline{RX\text{-}CLK}$, RX-DATA, SY-VALID, BS1, BS2, $\overline{ROMCLK}$, ROM-CE, ROM-RST

** $\overline{BLD}$, TFNC, $\overline{EOT}$, $\overline{STOP}$, $\overline{SILENT}$, $\overline{RST}$, $\overline{TST1}$, TIN, $\overline{TCK}$

*** ROM-CE

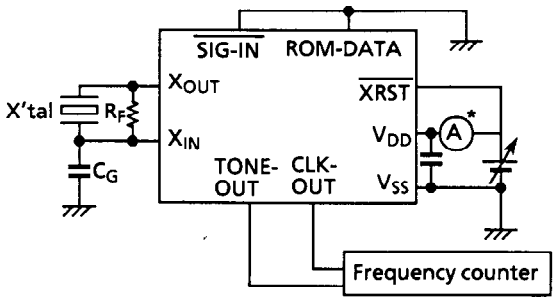
Notes:

1. Power supply voltage during frequency output from TONE-OUT is stable when $\overline{TCK}$ = low. A capacitor of 0.2 μF or more must be connected between V_{DD} and V_{SS}.
2. Voltage where 32 KHz or 76 KHz from CLK-OUT pin can be counted within 10 seconds after power on.
3. Pull-up current is excluded. Measured under the condition that $\overline{SIG\text{-}IN}$ and ROM-DATA are connected to V_{SS}, $\overline{XRST}$ to VDD, other pins are open and the oscillation circuit operates.
4. Current flowing into the IC is defined to be positive.
5. $$\triangle f/\triangle IC = \frac{f(V_{DD} = 3.0\ V) - f_0}{f_0} \times 10^6\ (ppm)$$ f_0: Average frequency when V_{DD} is 3.0 V
6. $$\triangle f/\triangle V = \frac{f_1(V_{DD} = 3.0\ V) - f_2(V_{DD} = 2.9\ V)}{f_1(V_{DD} = 3.0\ V)} \times 10^6\ (ppm)$$
7. When a trimmer capacitor is used, it should be inserted in C_G side.
8. Recommended external parts

Crystal (C_L = 12pF)			R_F	C_G
Seiko Instruments Inc.	DS-VT-200	(32768 Hz)	10 MΩ	24 pF
Seiko Instruments Inc.	DS-VTC-200	(76800 Hz)	10 MΩ	24 pF

■ Test Circuits

①

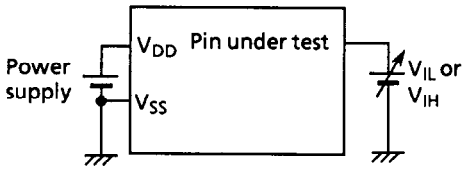


External crystal

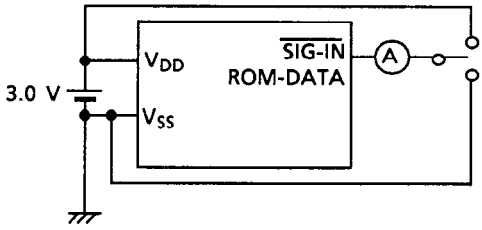
Crystal	R_F	C_G
32768 Hz	10 MΩ	24 pF
76800 Hz	10 MΩ	24 pF

Parameter	Measuring method
Current consumption	Connects $\overline{\text{SIG-IN}}$ and ROM-DATA to V_{SS}, $\overline{\text{XRST}}$ to VDD and sets other pins open. Inserts an ammeter to the position shown by *.
Oscillation start voltage	Connect a frequency counter to the CLKOUT pin.
Power supply voltage	Connect a frequency counter to the TONEOUT pin.

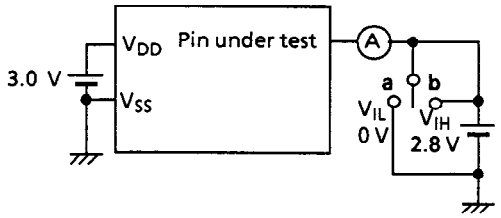
②



③



④



Switch a when I_{R1} is measured.
Switch b when I_{R2} is measured.

Figure 4

■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to 5.0	V
Input voltage	V_{IN}	V_{SS}-0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}	V_{SS} to V_{DD}	V
Storage temperature	T_{stg}	-40 to + 125	°C
Operating temperature	T_{opr}	-10 to + 70	°C

■ Ordering Information

S-7040XQP

Package type QP : QFP

Product name S-7040D : Tone frequency 2.7kHz/3.2kHz

■ POCSAG Signal Code Format

Transmission format of POCSAG signal code conforms with CCIR recommendation 584 which is shown in Figure 5. Transmission unit of a POCSAG signal is called block. A block comprises a preamble and one or more batches following the preamble.

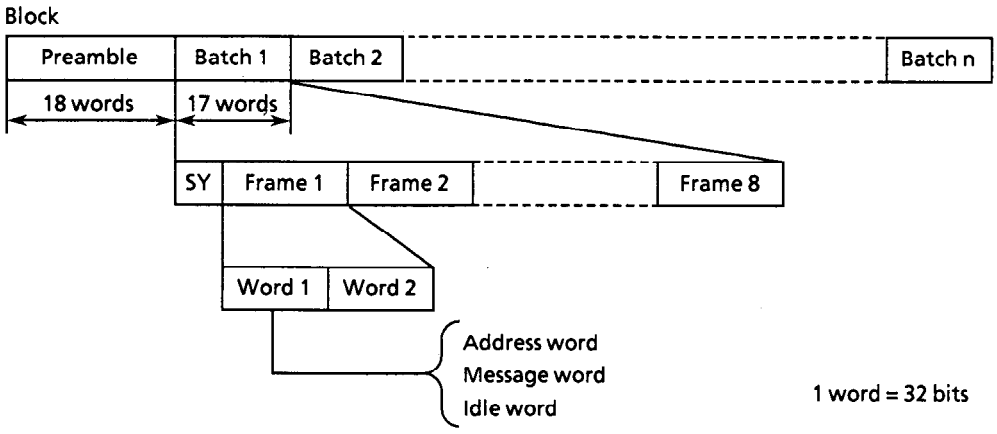


Figure 5 POCSAG code format

1. Preamble

Preamble at the beginning of a block gives notice that a POCSAG signal is sent to the S-7040D. A preamble consists of at least 576 bits (18 words) alternate signals of 1 and 0. Once preamble is received, the S-7040D starts synchronization between the internal circuit and the POCSAG signal.

Acceptable duty ratio of preamble ranges from 25% to 75%.

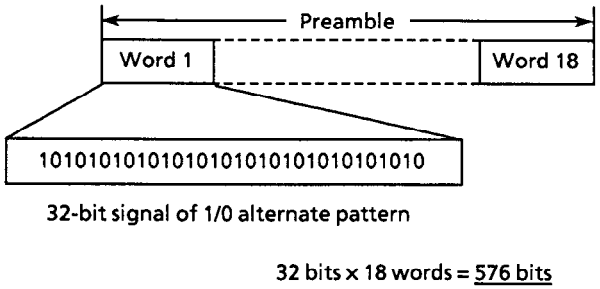


Figure 6 Preamble configuration

2. Batch

A batch, which is transmitted just after a preamble, contains information in a POCSAG signal and consists of a synchronization code (SY) and eight frames.

When the S-7040D recognizes preamble and SY as part of POCSAG signal, the decoder regards the following signal as POCSAG data and receives a frame. The S-7040D receives only a selected frame in a batch, frame whose number was assigned in ID-ROM in advance, and BS1 pin goes high only when a selected frame comes.

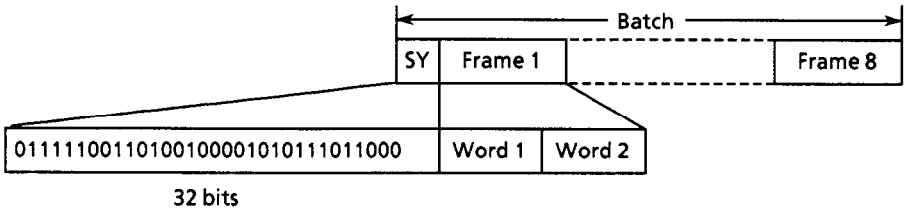


Figure 7 Batch configuration

Synchronization code (SY): 32-bit signal shown in Figure 7. When the SY is received after a preamble, the S-7040D considers them as a POCSAG code.

Frame: One frame consists of two words and a word consists of 32 bits. There are three types of words: address word, message word and idle word.

3. Word types
Three types of words are used as shown in Figure 8.

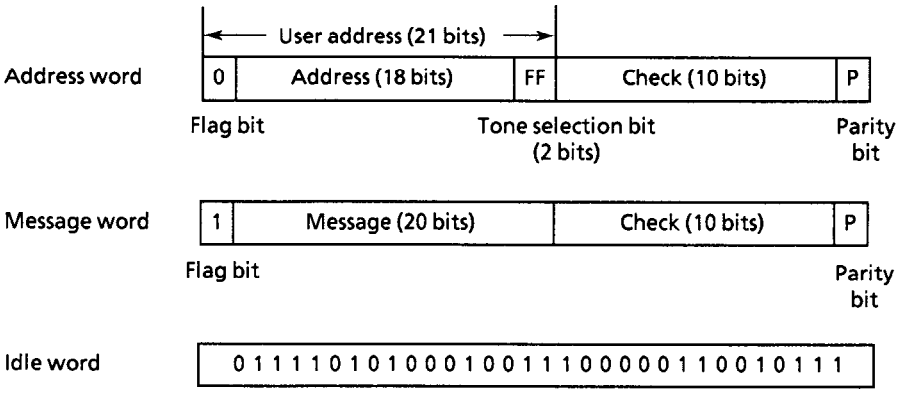


Figure 8 Kinds of words

The address word is sent first, then message word(s) follows in case of a display pager. Two or more message words can be sent continuously. (Tone-only pagers need no messages; idle words are used instead.) A flag bit determines whether the word is an address word or a message word. 0 shows an address word, and 1 shows a message word. The actual information is the address and tone selection bits (FF) in an address word and the message in a message word.

Address word: Each pager is distinguished by the data. An address should always be sent prior to information. Of the 21 bits in a user address, 18 bits are used for the actual address. Two tone selection bits select the calling tone (see "■ Basic Operation 6.1 Tone"). Check bits perform BCH check (see " Internal Functions 3. BCH decode function").

Message word: Of the 32 bits in a message word, 20 bits are used for the actual message. Even if a message is long enough to exceed a batch, subsequent message words are also received in the next batch until an address word is detected when a flag bit becomes 0. Thus plural message words can be sent continuously. A synchronization code (SY) must be inserted to continue message from frame 8 (last frame of a batch) to the next batch. The S-7040D gives the content of these message words to a CPU.

Idle word: If a batch does not have any information to send, idle words fill the blank portion of the batch. The Idle word cannot be assigned as an ID code.

■ Flow Chart

Flow charts for POCSAG signal process are shown in figures 9 and 10. These flow charts show the operations from power on to signal output for tone-only pager and display pager respectively.

1. Tone-only pager

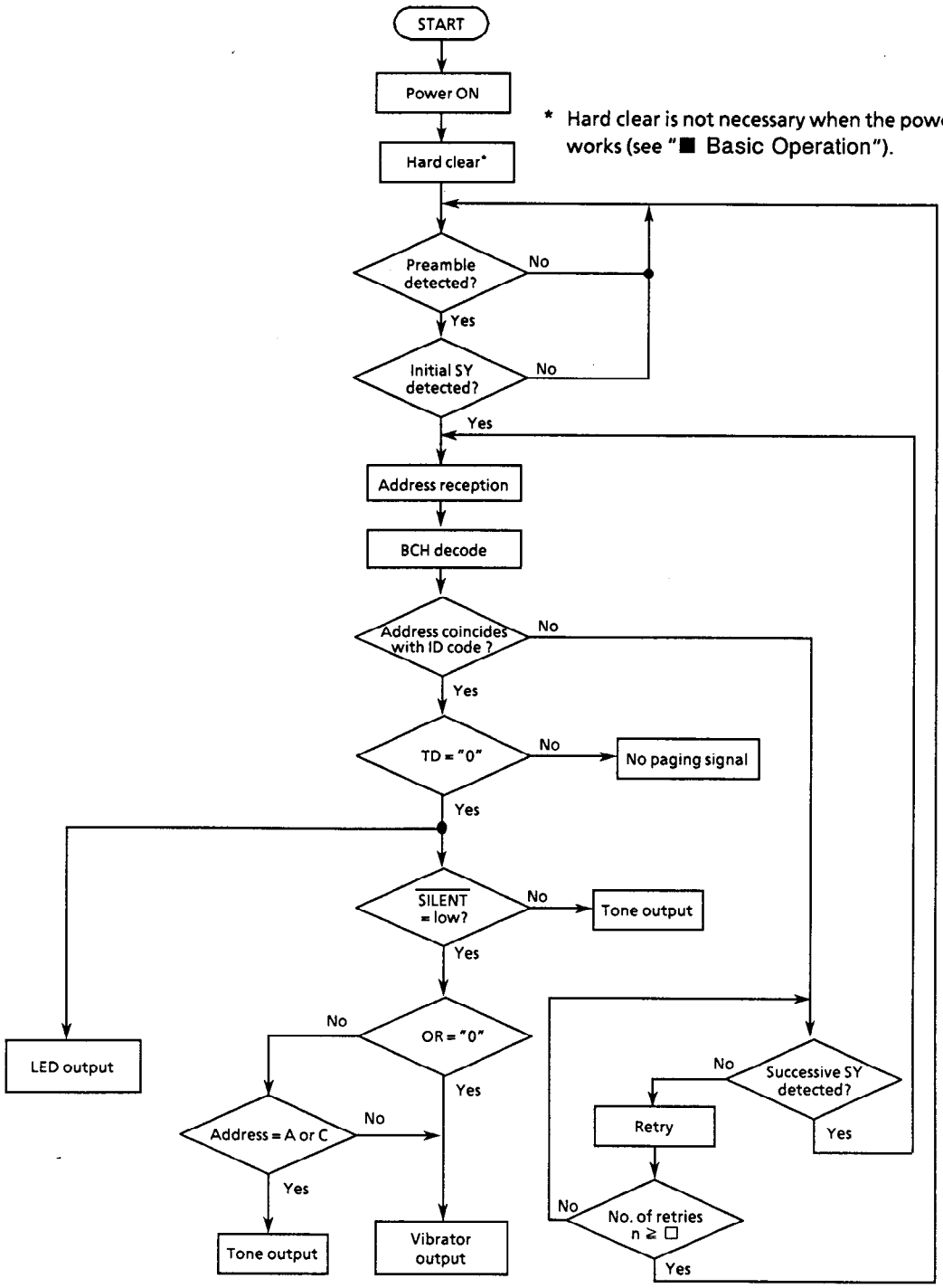


Figure 9

2. Display pager

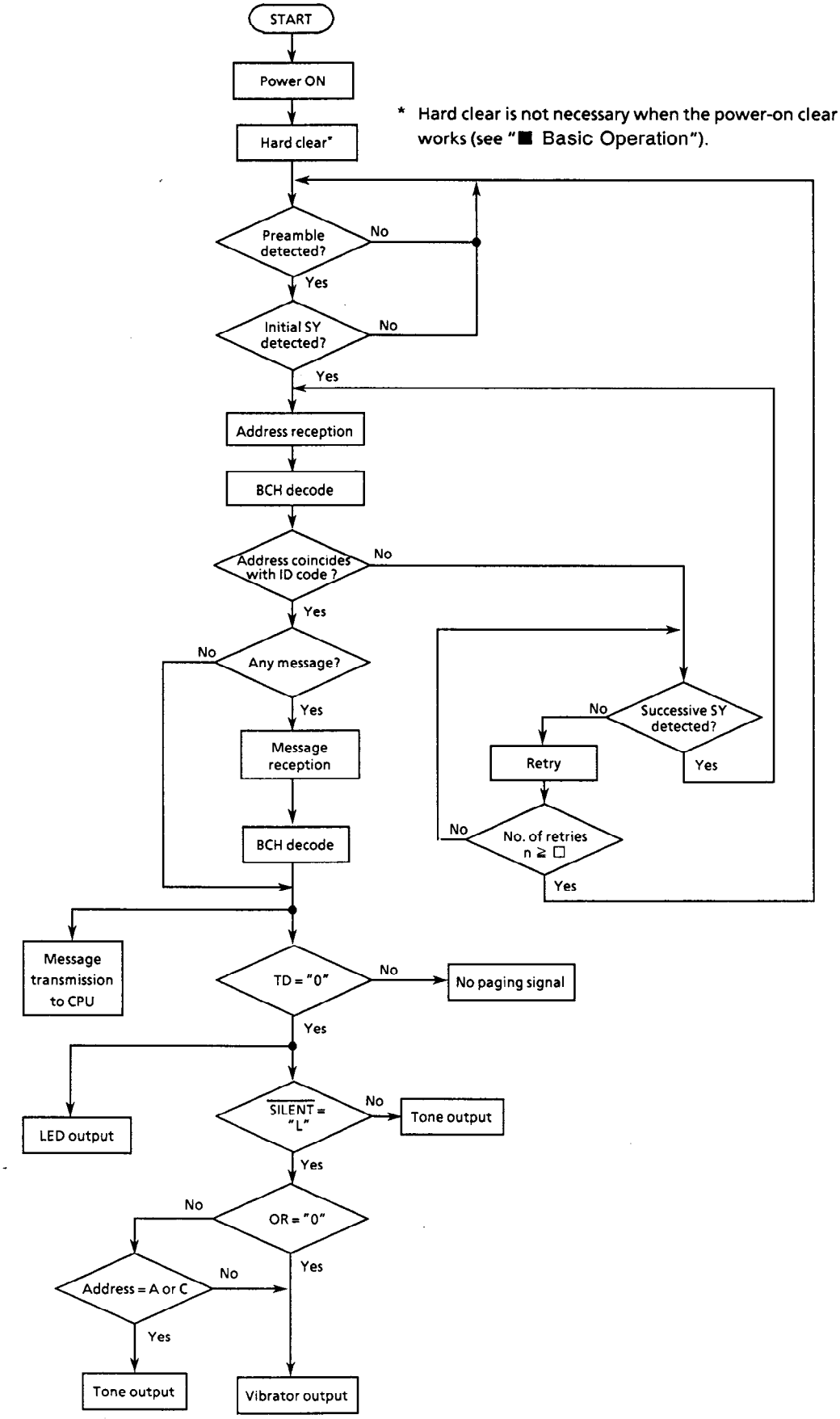


Figure 10

■ Basic Operation

1. Hard clear

The internal circuit is initialized by setting the $\overline{RST}$ pin to low. Then ID-ROM data are fetched in the S-7040D 500msec after the rising edge of reset signal. The initial tone is transmitted immediately after ID-ROM read (see "6.1 Tone" for waveform). The initial tone stops automatically after two seconds. POCSAG signal can be received 1sec (512bps) or 426msec (1200bps) after ID-ROM read.

The internal circuit is automatically initialized at power on when a capacitor whose capacitance is 100pF to 0.01μF is connected between $\overline{RST}$ pin and V_{SS} pin.

2. Detection of preamble

Preamble detection mode starts when the hard clear is completed or when the synchronization code is not detected even if the detection is repeated over the defined number of retries. When the decoder receives 12 consecutive bits consisting of an alternate pattern of 1, 0, 1, 0 in this mode, it regards the signal as preamble.

The S-7040D drives the RF circuit intermittently to save power consumption. When BS1 pin is high, the RF power is turned on to detect preamble. When the BS1 pin is low, preamble is not detected. Once preamble is detected, the BS1 pin holds high to detect synchronization code(SY). Figure 11 shows the BS1 timing and preamble.

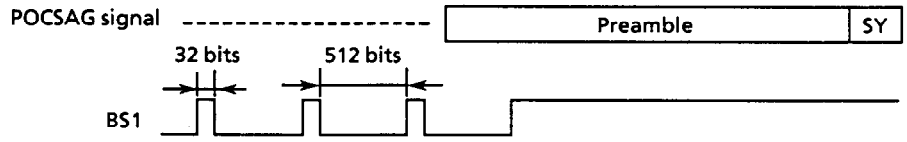


Figure 11 BS1 Timing and preamble

3. Detection of synchronization code(SY)

After detecting preamble, the S-7040D enters synchronization code(SY) detection mode. The first SY detected after the preamble is called the initial SY. When another batch continues, an SY is inserted between the batches and the SY is called successive SY.

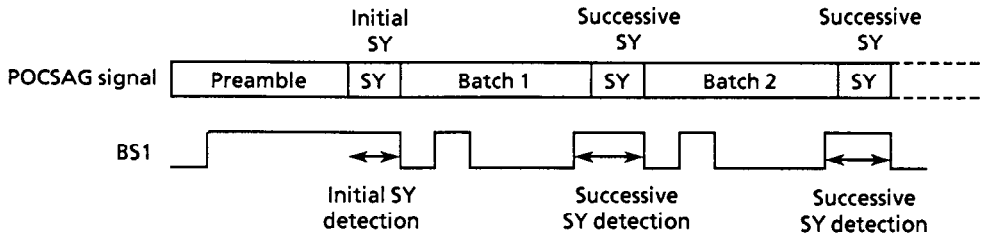


Figure 12 Initial SY and successive SY

3.1 Initial SY detection mode

Detection of the initial SY following preamble is performed during initial SY detection mode. The S-7040D compares the received data with the SY data kept in the S-7040D (see Fig.7). Receiving one bit of data the S-7040D compares the 32-bit data including this bit and those 31 bits received before it with the defined SY. If 30 or more bits coincide, the SY is considered to be detected. Even if the radio wave is disturbed by noise, SY can be detected as long as the number of fault bits is less than 2.

If SY is not detected after comparing 49 words (about 1.5K bits) in initial SY detection mode, the S-7040D returns to the preamble detection mode.

3.2 Successive SY detection mode

After the initial SY, successive SY is sent at the head of each batch. After the time for 8-frame (16-word) data, the S-7040D enters automatically successive SY detection mode. Since the signal is already synchronized, BS1 goes high in time with 32-bit output for successive SY and the S-7040D compares SY. In the same way as in initial SY detection mode, SY is detected even if the data contains up to two fault bits. When SY is detected, the bit/word counter is reset and processing of data in the next batch follows.

When SY is not detected, the S-7040D retries SY detection for the number of times specified in ID-ROM plus one. When the S-7040D fails to detect SY during these retires, it returns to preamble detection mode.

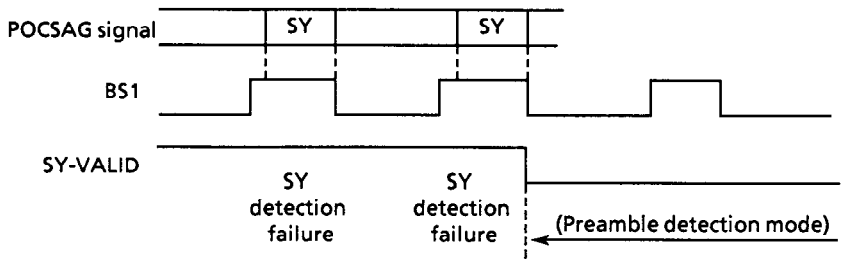
When the S-29131A is used for ID-ROM, bits R3 to R0 specifies the number for retry (see "■ Circuit Design 1. Interface to ID-ROM" for bit configuration of ID-ROM).

Table 4 Setup of the number for retry

R3	R2	R1	R0	The number of retries
0	0	0	0	1
1	0	0	0	9
1	1	1	1	16

If data is found to have consecutive 12-bit alternate pattern such as 1, 0, 1, 0 during the final retry, the S-7040D regards it as a preamble and enters the initial SY detection mode (see Figure 13).

(1) Case in which the S-7040D detects no SY and returns to the preamble detection mode



(2) Case in which the S-7040D detects preamble in the final retry

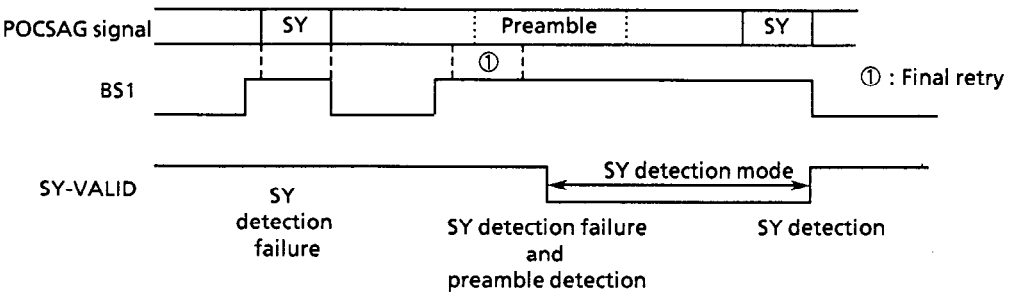


Figure 13 Operation for successive SY detection failure

4. Address detection

After finishing the SY detection, the S-7040D receives its own assigned frame. An address word is placed at the beginning of the frame. As shown in Figure 14 the latter 11 bits of the address word are check bits, and are used for error detection using BCH code (see "■ Internal Functions 3. BCH decode function"). The S-7040D compares the none erroneous address word with the fore addresses written in ID-ROM, and if they coincide, then receives a message word. Erroneous address words are ignored. If plural addresses are received at the same time, address A has priority over address B and address C has priority over address D. Only preferred address is received.

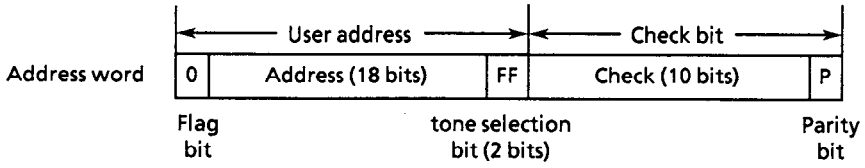


Figure 14 Address word configuration

5. Message detection

When an address word is detected, a message word is subsequently received. The S-7040D sends the message word to CPU, and the message is then sent to the pager display. The decoder continues to detect message words until an address or an idle word is detected.
As shown in figure 15, the latter 11 bits of the message word are check bits, and are used for error detection with BCH decode (see "■ Internal Functions 3. BCH decode function"). If an error is found, the message word is sent to CPU with error information (see table 5 "Error processing").

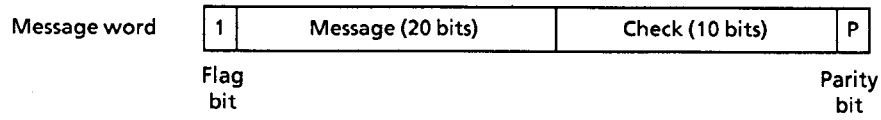


Figure 15 Message word configuration

When the S-7040D detects SY between message words, the following message is sent to the CPU again after SY is detected. If synchronization is failed at SY detection, message detection is terminated and $\overline{\text{ADDR-DET}}$ returns high.

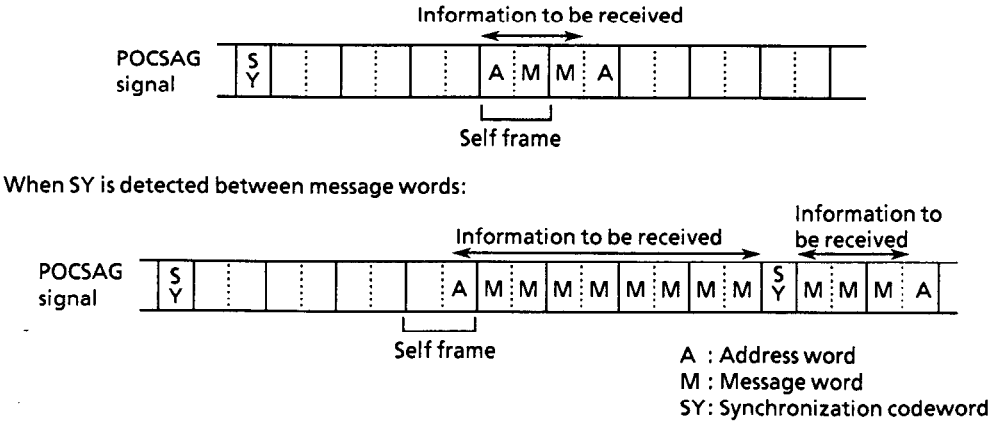


Figure 16 Information to be received

6. Paging signal

When the S-7040D detects an address (receives a call), not only by sending a message to a CPU but also by tone, light and vibration it notifies that the wearer is paged. 3 pins, TONE-OUT, DC-OUT (vibrator output) and LED, are assigned for paging signals. These signals are also transmitted at supply voltage lowering and after initialization. When the ID-ROM "TD" bit is set "1", no paging signal is transmitted.

6.1 Tone

Tone signal is transmitted from TONE-OUT pin at the end of pager initialization, address detection and supply voltage lowering respectively.

Completion of initialization: A tone is transmitted just after ID-ROM read following power-on clear or hard clear. This is called the initial tone and lasts 2 seconds at 2.7kHz single tone. Setting the $\overline{\text{STOP}}$ pin to low makes the initial tone stop. Setting the $\overline{\text{SILENT}}$ pin to low changes tone output to vibrator output.

Address reception: When address reception is completed, a tone is transmitted for 20 seconds. The waveform varies with contents of the tone selection bits. The transmission starts when the received data output is finished and 125msec after returning of the $\overline{\text{ADDR-DET}}$ pin to "H". The tone stops by setting $\overline{\text{STOP}}$ pin to low for longer than 10msec. 4 types of tone are assigned to each pair of addresses (A, C) and (B, D). When the decoder receives the next address during tone output, the tone output changes by the $\overline{\text{ADDR-DET}}$ timing.
The S-7040D has a single tone of 2.7kHz and a mixed tone of 2.7kHz and 3.2kHz. ID-ROM TM bit decides which pair of addresses single tone is assigned to (see "■ Circuit Design 1. Interface to ID-ROM").

Supply voltage lowering: When $\overline{\text{BLD}}$ pin goes low due to power supply voltage drop, Two 2.7kHz single tone outputs are transmitted at intervals of 32 seconds. This is called "BLD tone". The tone continues until $\overline{\text{STOP}}$ pin is set low for longer than 5.3s at 512bps or 2.3s at 1200bps.

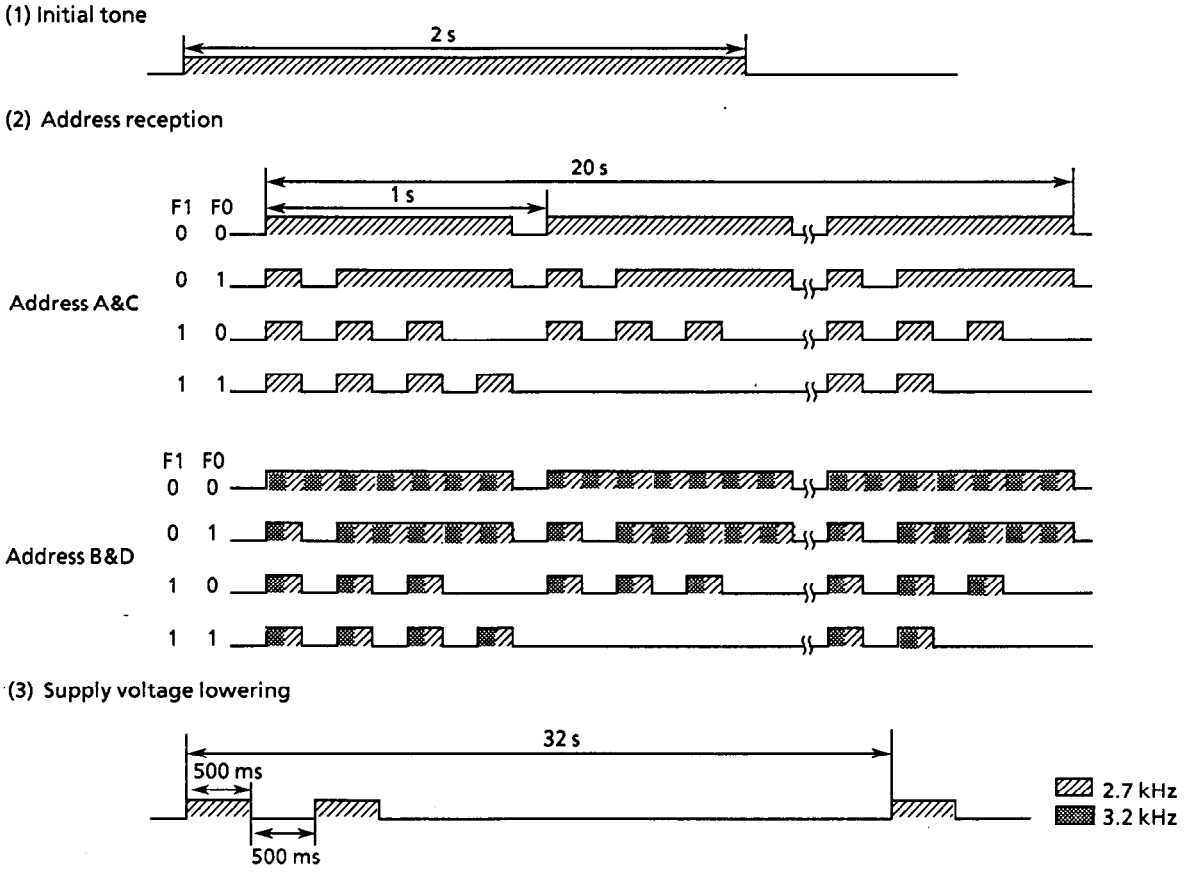


Figure 17 TONE-OUT output form

6.2 LED output

Control signals for LED drive are transmitted from LED pin. These signals are transmitted at completion of pager initialization, address reception and supply voltage lowering. The output waveforms are superposition of tone output signals and a 16-kHz modulation wave. The output signal of LED pin is transmitted regardless of the input signal of $\overline{\text{SILENT}}$ pin, and is halted when $\overline{\text{STOP}}$ pin is set low.

6.3 Vibrator drive control output

Vibrator drive control signals are transmitted from DC-OUT pin at completion of pager initialization and address reception, only when $\overline{\text{SILENT}}$ pin is set low. The signal stops by setting $\overline{\text{STOP}}$ pin to low.

If OR bit of the ID-ROM is set "H", a tone is transmitted at reception of address A or C regardless of $\overline{\text{SILENT}}$ pin (unconditional tone). DC-OUT is not transmitted in this case.

Completion of initialization: The vibrator signal is transmitted for 2s immediately after the hard clear.

Address reception: The vibrator signal is transmitted for 20s in synchronous to the LED output signal.

$\overline{\text{SILENT}}$		"H"	"L"
Initialization		(A)	(B)
Paging: Address A or C	(TM = L, OR = L)	(C)	(E)
	(TM = L, OR = H)	(C)	(C)
	(TM = H, OR = L)	(D)	(E)
	(TM = H, OR = H)	(D)	(D)
Paging: Address B or D	(TM = L)	(D)	(E)
	(TM = H)	(C)	(E)
Power supply voltage drop		(F)	(G)

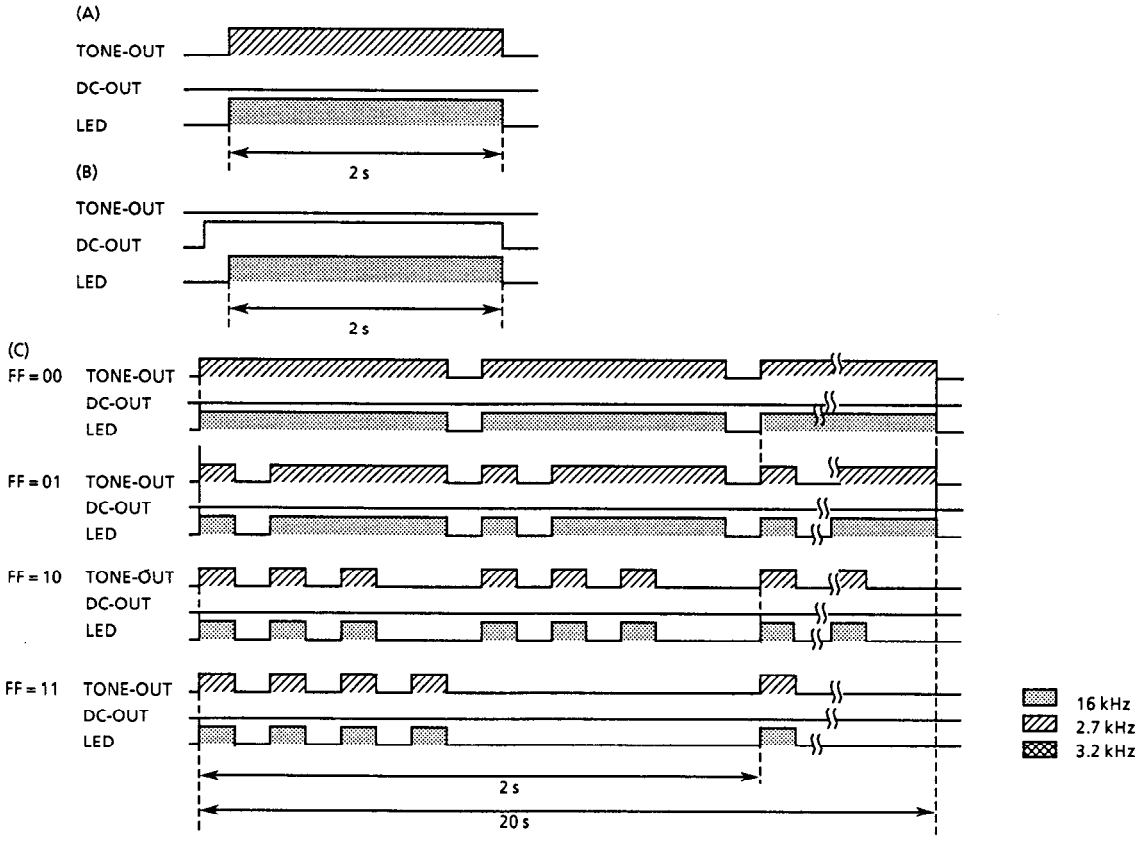


Figure 18-1 Relation ship between output waveforms of TONE-OUT, LED and DC-OUT

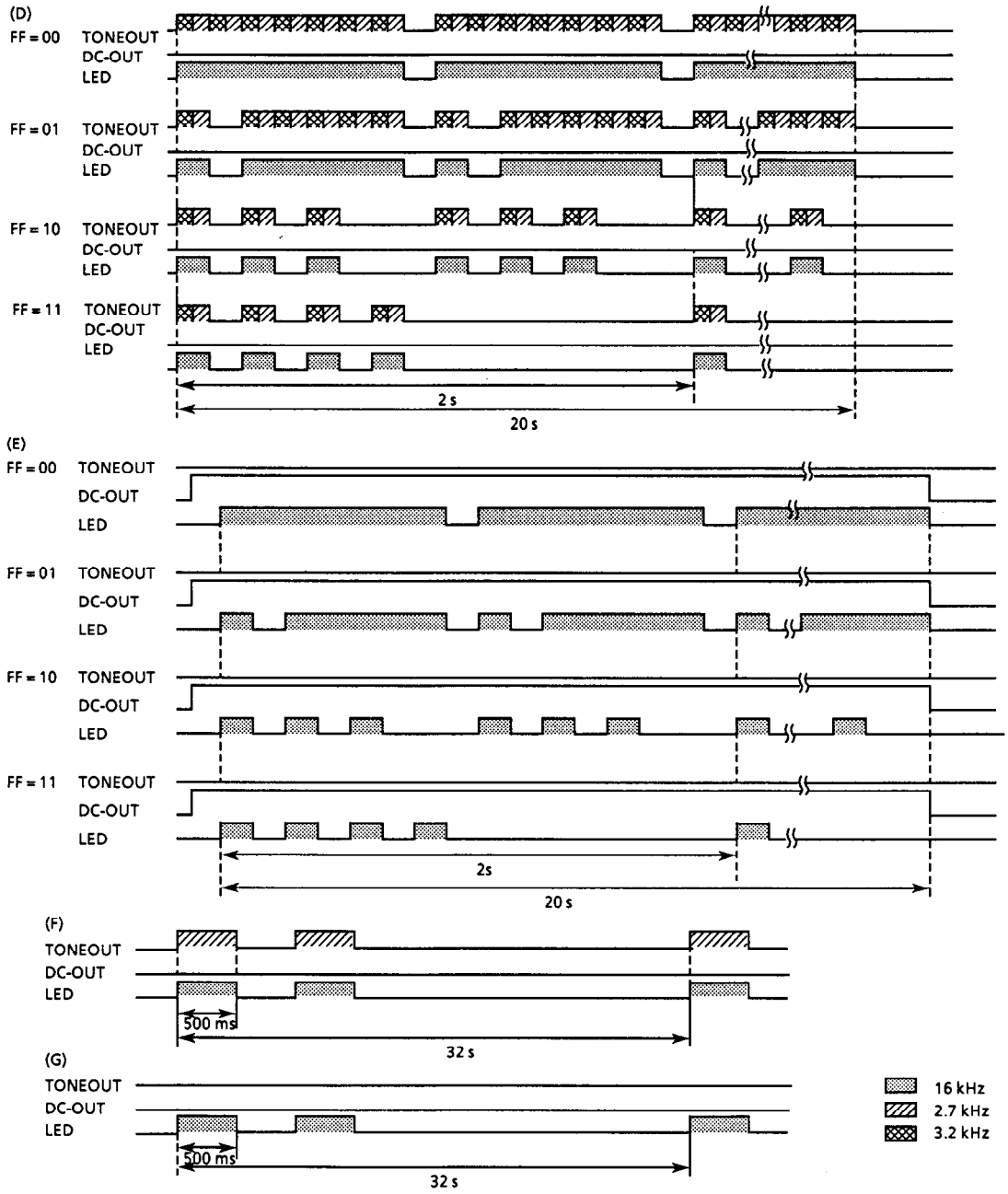


Figure 18-2 Relationship between output waveforms of TONE-OUT, LED and DC-OUT

■ Internal Functions

The S-7040D has the following functions to support its basic operations:

- Battery saving function to reduce power consumption
- Battery low alert function to notify supply voltage lowering
- BCH decode function to automatically correct address and message errors
- Extended function to enable forcible output of tone

These functions are explained below:

1. Battery saving function
   The battery saving function turns the RF circuit on and off intermittently to reduce the power consumption of the pager. Two signals are utilized: BS1 and BS2. BS1 activates the RF circuit. When the BS1 signal is set high, the RF circuit is turned on. BS2 is the timing pulse to detect preambles and synchronization codes. If BS1 is low, SIG-IN does not receive data and does not adjust synchronization.

1.1 BS1

Preamble detection: BS1 drives RF circuit intermittently. BS1 goes high for only one word out of 17 words. When BS1 goes high, the RF circuit is turned on and preamble detection is enabled.

SY detection: Holding BS1 high, the decoder keeps receiving POCSAG codes until the initial SY is detected up to 49 words, after preamble signal is detected. If no SY is detected during this period, the S-7040D returns to preamble detection mode. BS1 is also set high while consecutive SY detection. If the S-7040D fails to detect a consecutive SY over the defined number of retries, it returns to preamble detection mode.

After SY detection: The BS1 signal is controlled by the value of the bit/word counter. BS1 is set high synchronous to the timing of the frame specified in ID-ROM, and is kept high until all messages (only address for tone-only pagers) are received. BS1 is set high 16.5 bits in advance of the specified frame, which supplies power to the RF circuit early enough to activate (offset time).

1.2 BS2

Preamble detection: BS2 is set high for eight bits synchronous to BS1 high level.

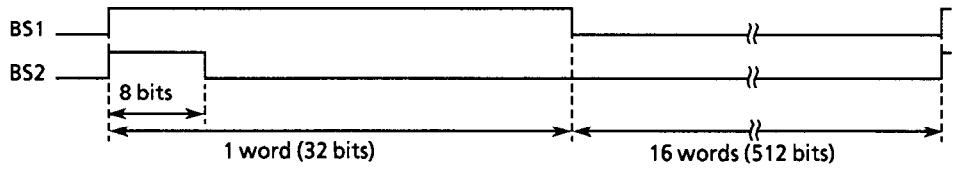
SY detection: BS2 is set high for eight or 16 bits, which is selected by the OF bit of ID-ROM, synchronous to BS1 high level.

1.3 Offset time selection

After preamble detection BS1 goes high when the assigned frame or a consecutive SY arrives and BS2 goes high just before a consecutive SY arrives. BS1 has an offset time which helps the RF/IF circuit to activate in advance before the assigned frame or a consecutive SY, and which can be set either 8.5 bits or 16.5 bits by the ID-ROM OF bit. BS2 offset time takes 8bits or 16bits according to the BS1 offset time.

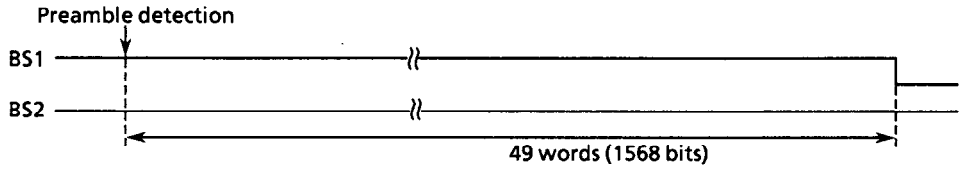
Figure 19 shows the timing of battery saving operation.

(A) Preamble detection mode



If preamble is detected, the mode is terminated and (B) starts.
If no preamble is detected, the operation is repeated until detection.

(B) SY detection following preamble detection



If SY is detected, the mode is terminated and (C) starts.
If no SY is detected during 49 words, the operation goes back to (A).

(C) After SY detection

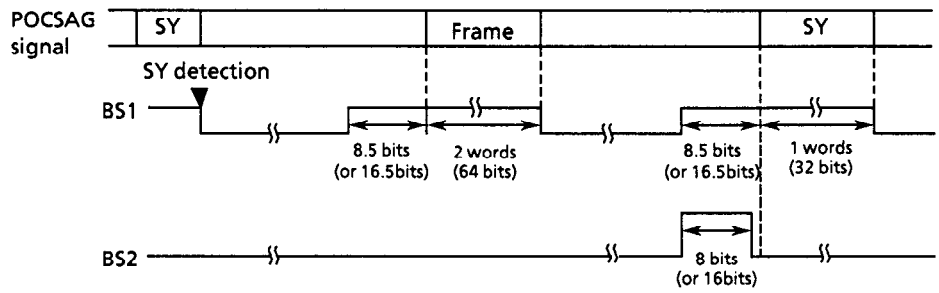


Figure 19 Battery saving

2. Battery low alert

Detection signals of an external voltage detector are entered from $\overline{\text{BLD}}$ pin, and these levels are sampled. Sampling of two consecutive "L" signals leads to the alert tone signal output. This tone continues until $\overline{\text{STOP}}$ pin is set high for more than 5.3 s at 512bps and 2.3s at 1200bps.
If the sampling coincides with the tone output, the detected at that point is not performed and postponed to the next sampling point.

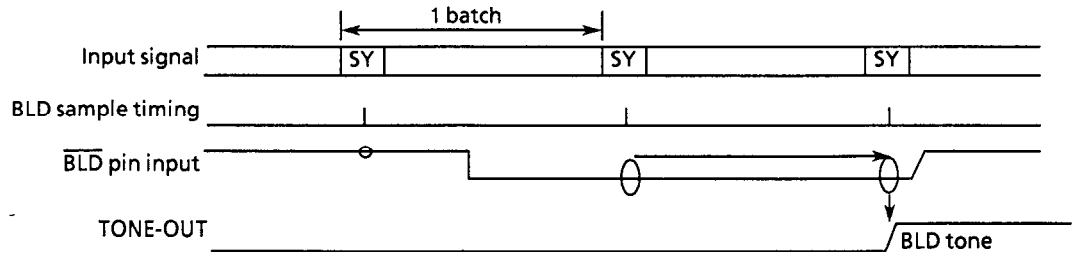


Figure 20 Sampling and detection of power supply voltage

3. BCH decode function

An address and a message word consist of 21-bit valid data and 11-bit check bits. Information in valid data is extracted and is checked with the check bits. When an error is found, corrections are made according to the number of erroneous bits and 21 valid data bits is extracted. The check bits consist of 10 BCH check bits and 1 parity bit as shown in Figure 21.

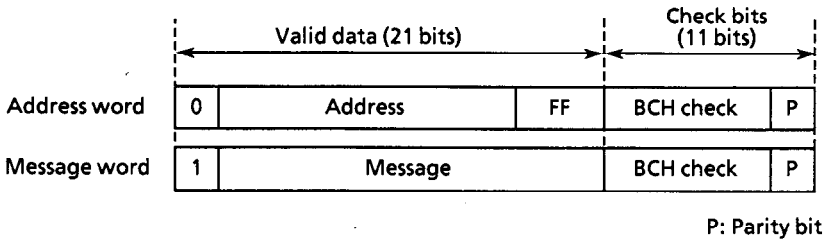


Figure 21 Address and message word composition

3.1 Error detection based on BCH code

BCH codes are the residual value of the 21 valid data divided by the generator polynomial specified by the POCSAG code. By dividing the received address word or message word by the polynomial, the presence and location of error bits are checked. If division produces the same residue, there is no error. The difference in the residue corresponds to the error. The value of the erroneous bits in address words or message words are corrected by the residue. The S-7040D detects random errors up to 2 bits both in an address word and in a message word and corrects them.

3.2 Error detection based on parity

Parity bit is added so that the total sum of the each bit (the number of bits having 1 as data) in a word should be even. If the total sum is odd, it is considered to be an error. This parity checks are performed after BCH error correction.
If an address word is erroneous, the address is ignored. If a message word is erroneous, the message is sent to the CPU with an error code.

Table 5 shows the error correction processing for both address words and message words.

Table 5 Error correction processing

BCH error	Correction	Parity error	Address word	Message word	Error code E1	Error code E0
0 bit	No	Yes/No	Received	Sent to CPU with error code	0	1/0
1 bit	Yes	No	Received	Sent to CPU with error code	0	1
1 bit	Yes	Yes	Received	Sent to CPU with error code	1	0
2 bits	Yes	No	Received	Sent to CPU with error code	1	0
2 bits	Yes	Yes	Ignored	Sent to CPU with error code	1	1
Other case	Yes/No	Yes/No	Ignored	Sent to CPU with error code	1	1

Note : BCH error correction is performed only to syndromes of 1 or 2 bits error, and is not performed to other syndromes.

4. Extended function

The S-7040D performs the functions shown in table 6 using four pins such as $\overline{RST}$, $\overline{TCK}$, TFNC and TIN. These functions are controlled by the microcomputer, regardless of IC operation.

Table 6

Input				Function
$\overline{RST}$	$\overline{TCK}$	TFNC	TIN	
L	L	×	×	Forcible output of BS1 and BS2
H	L	H	H/L	Forcible output of tone 2.7kHz output when TIN = "H", 3.2 kHz output when TIN = "L"
H	L	L	H/L	Forcible output of paging signals (tone, vibrator, LED)

4.1 Forcible output of BS1 and BS2

Setting $\overline{TCK}$ pin low while $\overline{RST}$ pin is low enables "H" output from BS1 and BS2, which can be applied to the synchronization test of RF circuit. CLK-OUT pin operates normally.

4.2 Forcible output of tone

If $\overline{TCK}$ pin is set low in normal mode (preamble detection mode), signals are transmitted from TONEOUT pin and LED pin, even if the ID-ROM TD bit inhibits tone output. The tone frequency is 2.7 kHz when TIN is high and 3.2 kHz when TIN is low.

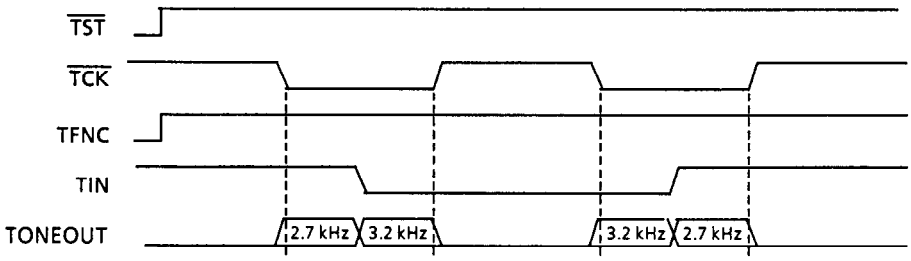


Figure 22 Tone forcible output timing

5.3 Forcible output of paging signals

If TFNC pin is set low in normal mode, the S-7040D enters forcible paging signlal output mode.* In this mode paging signals are not generated when a page is received, and the paging information is sent to the CPU. The CPU orders paging tone output from the TONE-OUT pin. The tone is determined as follows:

1. F1 data is set to TIN pin and a pulse is sent to $\overline{TCK}$.
2. F0 data is set to TIN pin and a pulse is sent to $\overline{TCK}$.

Then address B&D tone is transmitted when TIN is high, or address A&C tone is transmitted when TIN is low according to figure 17, p.5-43. TIN value should be kept until a paging is completed.

*) Mode change by TFNC pin can not be allowed during tone output. The change should be done before the rising edge of the $\overline{ADDR\text{-}DET}$.

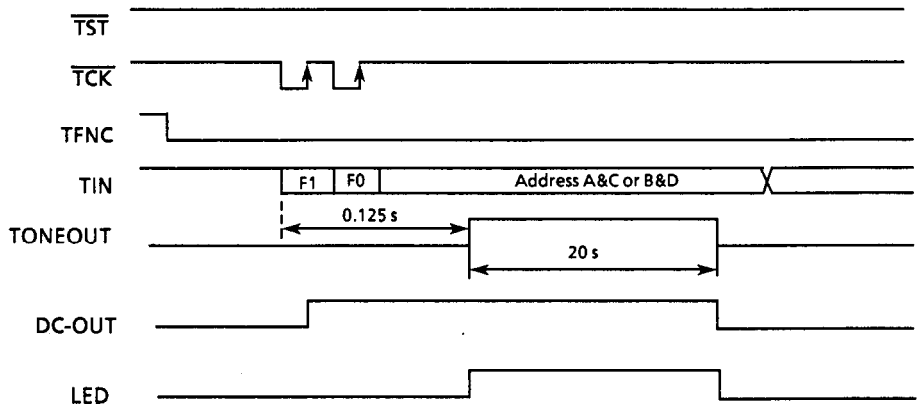


Figure 23 Timing for forcible output of paging tone

■ Circuit Design

1. Interface to ID-ROM

1.1 ID-ROM assignment

The S-29131A or S-2913 is used as an ID-ROM and is directly connected to the S-7040D. Table 7 shows the ID-ROM bit allocation, and tables 8 shows the function of each bit.

Table 7 ID-ROM bit allocation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$\overline{AE}$	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
A2	A1	A0	$\overline{BE}$	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
B5	B4	B3	B2	B1	B0	$\overline{CE}$	C17	C16	C15	C14	C13	C12	C11	C10	C9
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C8	C7	C6	C5	C4	C3	C2	C1	C0	$\overline{DE}$	D17	D16	D15	D14	D13	D12
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F20	F10	F00	F21
80	81	82	83	84	85	86	87	88	89	90	91	92			
F11	F01	R3	R2	R1	R0	OF	TM	OR	TD	XT	BR	SI			

Table 8 Function of each bit

Bit name	Function
A17~A0	Code for address A
B17~B0	Code for address B
C17~C0	Code for address C
D17~D0	Code for address D
$\overline{AE}$~$\overline{DE}$	Access enable bit for each address. "0" enables the address.
F20~F00	Frame assignment for address A, B (the first address)
F21~F01	Frame assignment for address C, D (the second address)
R3~R0	The number of retrials when synchronization code is not detected
OF	BS signal offset time "1" : 16.5bits for BS1, 16bits BS2 "0" : 8.5 bits for BS1, 8bits for BS2
TM	Mixed tone assignment "1" : Address A&C "0" : Address B&D
OR	Unconditional tone output for address A&C "1" : Yes, "0" : No
TD	Suppression of tone "1" : Yes, "0" : No (Forcible tone output can not be suppressed.)
XT	Crystal selection "1" : 76.8KHz, "0" : 32.768KHz
BR	Bit rate "1" : 1200bps, "0" : 512bps (Valid for XT = "1")
SI	Logic level for $\overline{SIG\text{-}IN}$ "1" : positive, "0" : negative

1.2 interface

The S-7040D triggers the ID-ROM and fetches the data in it. This operation is controlled by the ROM-CE, ROM-RST, $\overline{\text{ROMCLK}}$, and ROM-DATA pins.

ROM-CE: Chip enable signal for ID-ROM. If this pin is set high, the ID-ROM data is fetched.

ROM-RST: Command output. Read command for ID-ROM is transmitted

$\overline{\text{ROMCLK}}$: Clock signal for ID-ROM data reading. 4 kHz clock at 32kHz operation and 9.6 kHz clock at 76kHz operation for acquiring 113-bit data.

ROM-DATA : Data input from ID-ROM

Figure 24 shows the interface timing with the S-29131A. 96-bit ID-ROM data is fetched from the S-29131A, and additional 8-bit data data is read from the ID-ROM but the S-7040D does not hold it. When the $\overline{\text{RST}}$ pin is set to "L", ROM-RST and $\overline{\text{ROMCLK}}$ becomes "Hi-Z" and ROM-CE is pulled down, and that makes the external write/erase operation to the ID-ROM possible.

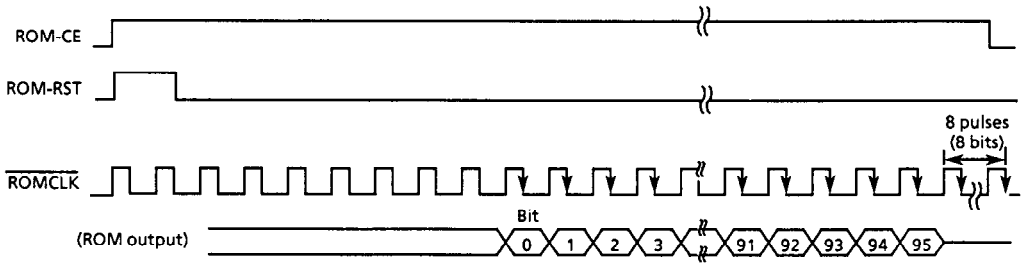


Figure 24 ID-ROM interface

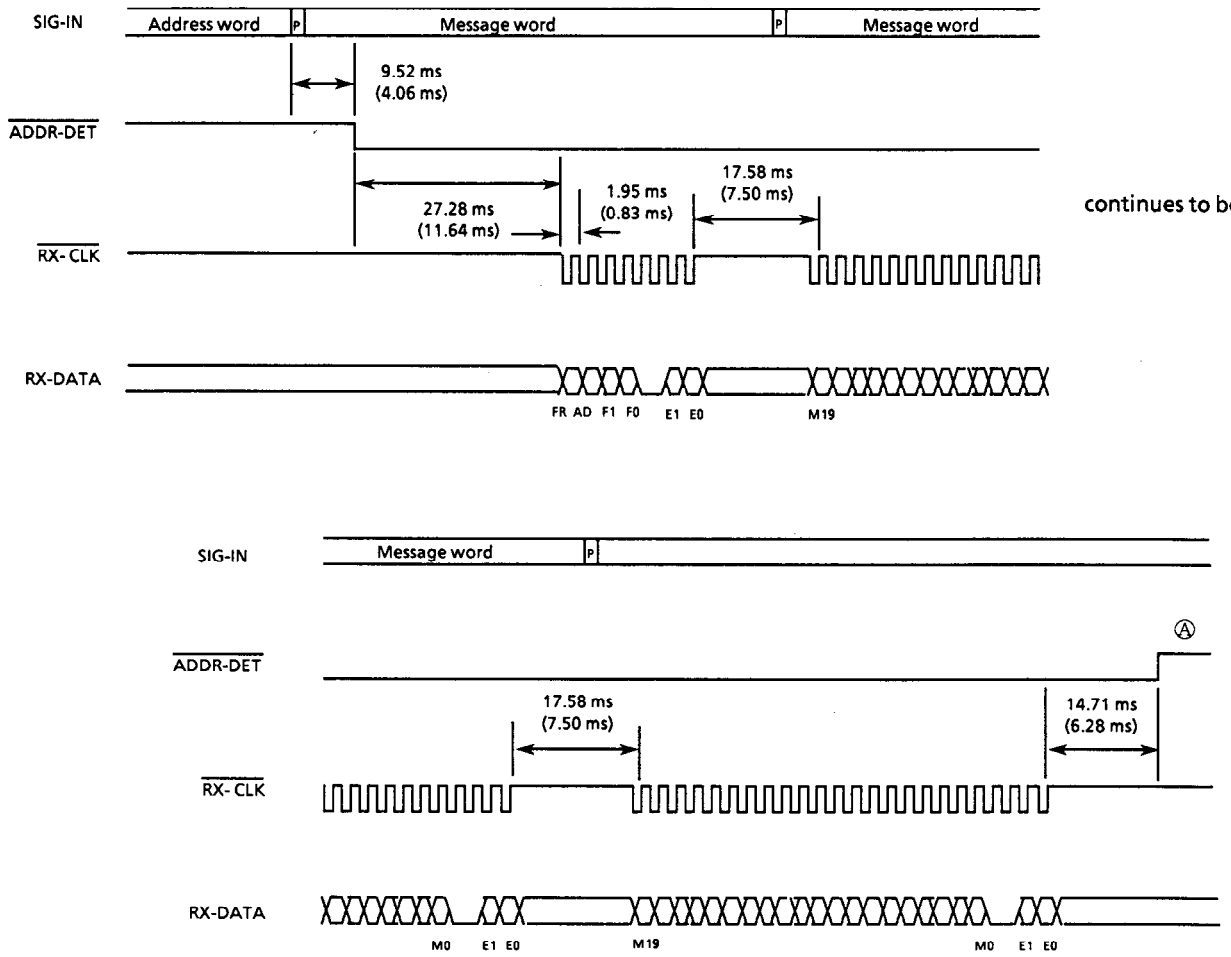
2. Interface to CPU for display pager
The S-7040D decodes the received data and sent it to the CPU. The CPU gets the data and displays it on a panel. The S-7040D is provided with four signal lines for these purposes.

SY-VALID : Indicates that the received POCSAG signal is synchronized i.e., the pager is in the reception area. In preamble detection mode, the pin set low. Detecting SY, SY-VALID goes high. When SY-VALID is high, the bit/word counter is synchronized with the received POCSAG signal and the decoder can decode it.

$\overline{\text{ADDR-DET}}$: $\overline{\text{ADDR-DET}}$ goes low when addresses are detected. When the reception of the message word following the address word is completed, this pin returns to high.
The message word reception is considered to be completed in the following cases:
- When the next address word is detected.
- When an idle word is detected.
- When an SY, inserted between consecutive message words, is not detected.
- When the $\overline{\text{EOT}}$ pin detects the low level.

$\overline{\text{RX-CLK}}$, RX-DATA : RX-DATA transmits the received message data to the CPU. $\overline{\text{RX-CLK}}$ is a clock signal for sending data. The CPU samples RX-DATA at the falling edge of $\overline{\text{RX-CLK}}$, and fetches data at the rising edge. The following data is sent to the CPU.
- At the address detection 8-bit data consisting of the address number and the tone selection bits.
- At the message word reception 24 bits of information is sent per message word. The information consists of 20 message data bits and 2 error code bits. Figure 25 shows the interface timing for each data.

Unit : msec



M19~M0 : Message data
FR : Frame
AD : Address order in a frame
E1, E0 : Error code
F1, F0 : Tone selection for the paged address
P : Parity bit
Ⓐ : When a message word continues, $\overline{\text{ADDR-DET}}$ keeps low.

Upper values indicate 512 bps case and lower values in parentheses indicate 1200 bps case.

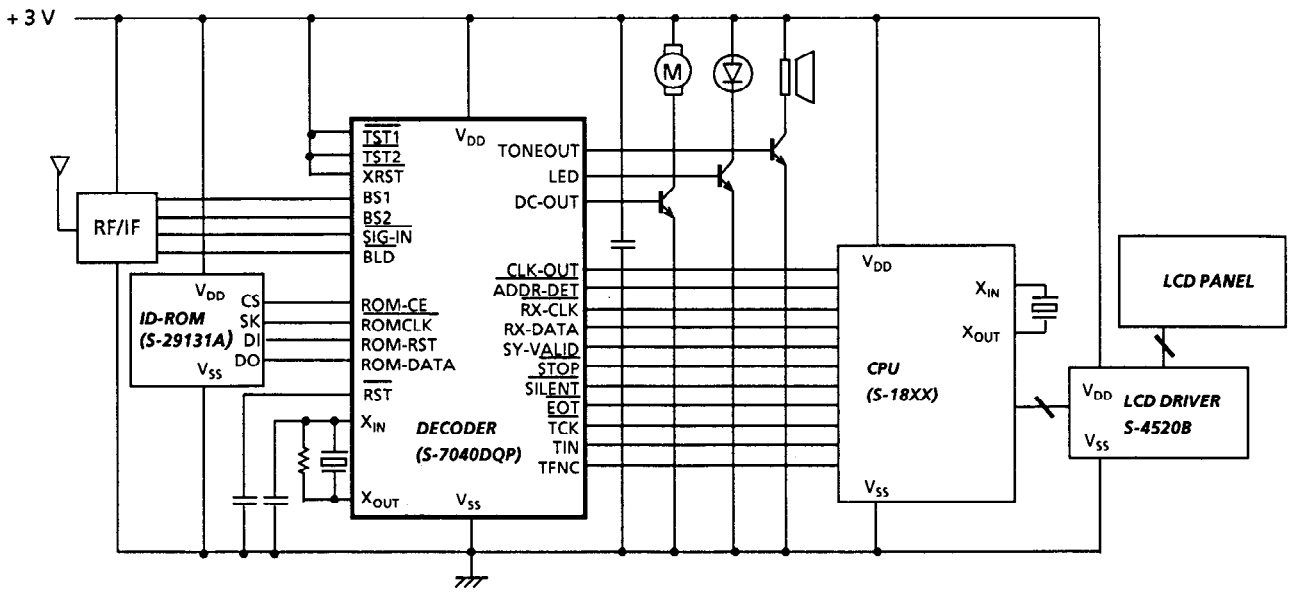
Relation between FR bit, AD bit and address

FR	AD	ADDRESS
0	1	A
0	0	B
1	1	C
1	0	D

Figure 25 CPU interface timing

3. Example for application

1 Information pager



2 Numeric pager

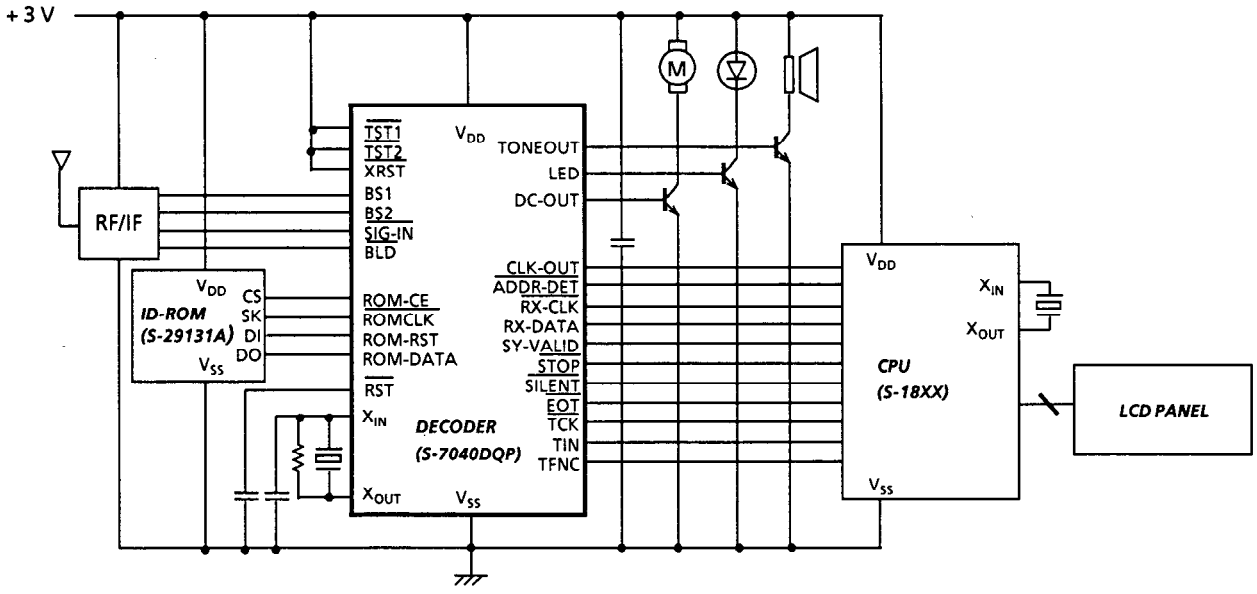


Figure 26 Example for application

Notes for the Paging Decoder ICs

- Please note that the products incorporating these ICs may infringe a patent depending upon applications, including the one in this document, the specifications of the products, and countries to which they are supplied.
- In the event that the aforesaid products including these ICs infringe a patent, Seiko Instruments Inc. shall not bear any responsibility for any matters with regard to and arising from such patent infringement.