

# BATTERY PROTECTION IC FOR SINGLE-CELL PACK S-8201 Series

The S-8201 Series are lithium-ion/lithium polymer rechargeable battery protection ICs incorporating high-accuracy voltage detection circuit and delay circuit. The S-8201 Series are suitable for protection of single-cell lithium ion/lithium polymer battery packs from overcharge, overdischarge and overcurrent.

## ■ Features

- (1) Internal high accuracy voltage detection circuit
  - Overcharge detection voltage 3.9 V to 4.4 V (5 mV step), Accuracy  $\pm 25$  mV (+25 °C),  $\pm 30$  mV (–5 °C to +55 °C)
  - Overcharge release voltage 3.8 V to 4.4 V<sup>\*1</sup>, Accuracy  $\pm 50$  mV
  - Overdischarge detection voltage 2.0 V to 3.0 V (10 mV step), Accuracy  $\pm 50$  mV
  - Overdischarge release voltage 2.0 V to 3.4 V<sup>\*2</sup>, Accuracy  $\pm 100$  mV
  - Overcurrent 1 detection voltage 0.05 V to 0.3 V (10 mV step) Accuracy  $\pm 15$  mV
  - Overcurrent 2 detection voltage 0.5 V (fixed) Accuracy  $\pm 100$  mV
- (2) High voltage device is used for charger connection pins.  
(VM pin and CO pin: Absolute maximum rating=28 V)
- (3) Delay times (Overcharge:  $t_{CU}$ , Overdischarge:  $t_{DL}$ , Overcurrent 1:  $t_{IOV1}$ , Overcurrent 2:  $t_{IOV2}$ ) are generated by an internal circuit. (No external capacitor is necessary.) Accuracy  $\pm 20\%$
- (4) The overcharge timer reset delay time (7 ms to 40 ms) is generated by an internal circuit only. (No external capacitor is necessary.)
- (5) Three-step overcurrent detection circuit is included. (Overcurrent 1, Overcurrent 2, Load short-circuiting)
- (6) Either charge function or charge inhibition function for 0 V battery can be selected.
- (7) Charger detection function and abnormal charge current detection function
  - The overdischarge hysteresis is released by detecting negative voltage at the VM pin (–0.7 V typ.). (Charger detection function)
  - When the output voltage of the DO pin is high and the voltage at the VM pin is equal to or lower than the charger detection voltage (–0.7 V typ.), the output voltage of the CO pin goes low. (Abnormal charge current detection function)
- (8) Low current consumption
  - Operation 3.5  $\mu$ A typ., 7.0  $\mu$ A max.
  - Power-down 0.1  $\mu$ A max.
- (9) Wide operating temperature range –40 °C to +85 °C
- (10) Small package 6-Pin SOT-23-6, 6-Pin SNB(B)

\*1. The overcharge hysteresis voltage is 0.0 V or can be selected from the range 0.1 V to 0.4 V in 50 mV step.

Overcharge hysteresis voltage ( $V_{HC}$ )=Overcharge detection voltage–Overcharge release voltage

\*2. The overdischarge hysteresis voltage is 0.0 V or can be selected from the range 0.1 V to 0.7 V in 100 mV step.

Overdischarge hysteresis voltage ( $V_{HD}$ )=Overdischarge release voltage–Overdischarge detection voltage

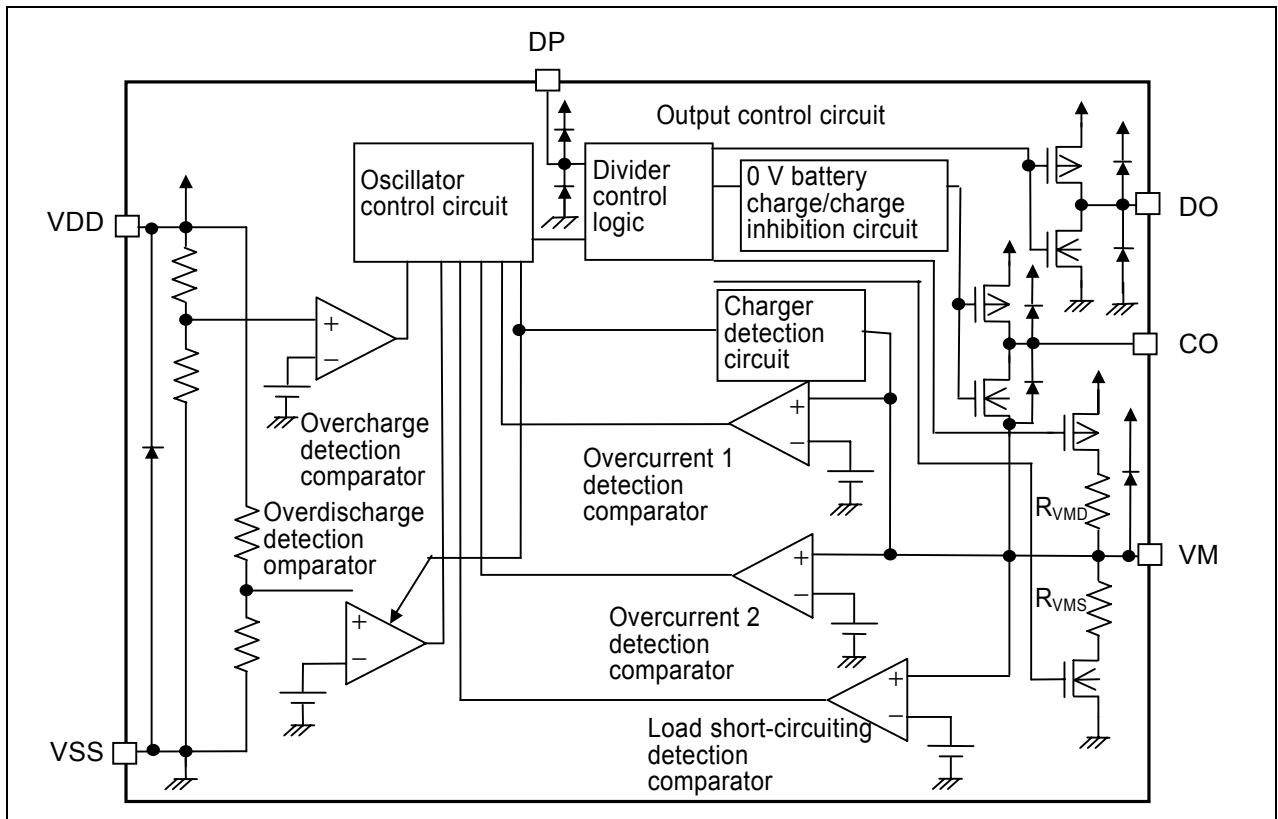
## ■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

**■ Packages**

Package name	Drawing code		
	Package	Tape	Reel
SOT-23-6	MP006-A	MP006-A	MP006-A
6-Pin SNB(B)	BD006-A	BD006-A	BD006-A

■ Block Diagram

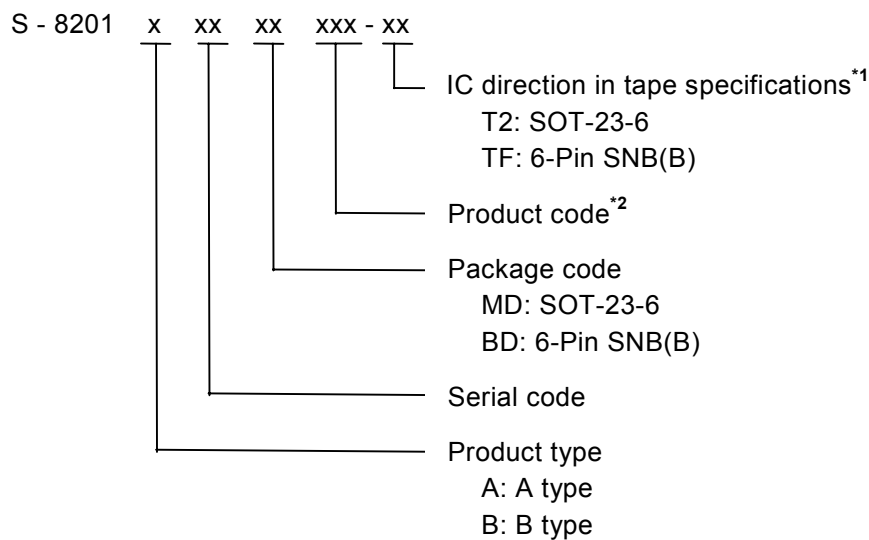


**Remark** The diodes in the figure are all parasitic diodes.

Figure 1

### ■ Product Name Structure

#### 1. Product Name



\*1. Refer to the taping specifications at the end of this book.

\*2. Refer to the "Table 1 to 2" in the "2. Product Name List".

**2. Product Name List**

**2-1. A type**

**Table 1 (1/2)**

Model No./Item	Overdischarge detection voltage	Overcharge release voltage	Overdischarge detection voltage	Overdischarge release voltage	Overcurrent 1 detection voltage	0 V battery charge function
S-8201AAABD-M5A-TF	4.3 V	4.1 V	2.3 V	2.3 V	0.13 V	Available
S-8201AABBD-M5B-TF	4.305 V	4.005 V	2.3 V	2.9 V	0.1 V	Available
S-8201AACBD-M5C-TF	4.295 V	3.995 V	2.3 V	2.9 V	0.1 V	Available
S-8201AADBD-M5D-TF	4.325 V	4.075 V	2.5 V	2.9 V	0.15 V	Unavailable
S-8201AAEBD-M5E-TF	4.350 V	4.150 V	2.3 V	3.0 V	0.20 V	Unavailable
S-8201AAFBD-M5F-TF	4.350 V	4.150 V	2.3 V	3.0 V	0.20 V	Available

**Table 1 (2/2)**

Model No./Item	Overcharge detection delay time	Overdischarge detection delay time	Overcurrent 1 detection delay time
S-8201AAABD-M5A-TF	4.6 s	150 ms	9 ms
S-8201AABBD-M5B-TF	4.6 s	150 ms	9 ms
S-8201AACBD-M5C-TF	4.6 s	150 ms	9 ms
S-8201AADBD-M5D-TF	1.2 s	150 ms	9 ms
S-8201AAEBD-M5E-TF	1.2 s	150 ms	9 ms
S-8201AAFBD-M5F-TF	1.2 s	150 ms	9 ms

**Remark** It is possible to change the detection voltages of the product other than above. The delay times can also be changed within the range-listed below. For details, contact SII marketing department.

**Table 2**

Delay time	Symbol	Selection range			Remarks
Overcharge detection delay time	$t_{CU}$	0.15 s	<b>1.2 s</b>	4.6 s	Choose from the left
Overdischarge detection delay time	$t_{DL}$	37.5 ms	<b>150 ms</b>	300 ms	Choose from the left
Overcurrent 1 detection delay time	$t_{OV1}$	4.5 ms	<b>9m s</b>	18 ms	Choose from the left

**Remark** Values surrounded by bold lines are used in standard products.

## 2-2. B type

Table 3 (1/2)

Model No./Item	Overdischarge detection voltage	Overcharge release voltage	Overdischarge detection voltage	Overdischarge release voltage	Overcurrent 1 detection voltage	0 V battery charge function
S-8201BAABD-M7A-TF	4.3 V	4.1 V	2.3 V	2.3 V	0.13 V	Available

Table 3 (2/2)

Model No./Item	Overcharge detection delay time	Overdischarge detection delay time	Overdischarge release delay time	Overcurrent 1 detection delay time
S-8201BAABD-M7A-TF	4.6 s	150 ms	1.18 ms	9 ms

**Remark** It is possible to change the detection voltages of the product other than above. The delay times can also be changed within the range-listed below. For details, contact SII marketing department.

Table 4

Delay time	Symbol	Selection range			Remarks
Overcharge detection delay time	$t_{CU}$	0.15 s	<b>1.2 s</b>	4.6 s	Choose from the left
Overdischarge detection delay time	$t_{DL}$	37.5 ms	<b>150 ms</b>	300 ms	Choose from the left
Overcurrent 1 detection delay time	$t_{IOV1}$	4.5 ms	<b>9m s</b>	18 ms	Choose from the left

**Remark** Values surrounded by bold lines are used in standard products.

## Pin Configurations

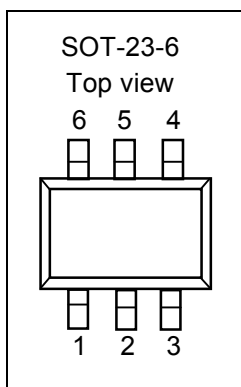


Figure 2

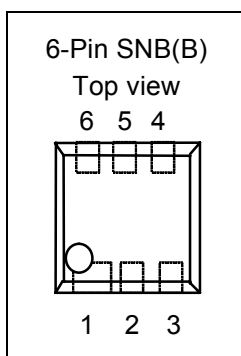


Figure 3

Table 5

Pin No.	Pin name	Pin description
1	DO	FET gate control pin for discharge (CMOS output)
2	VM	Voltage detection pin between VM pin and VSS pin (Overcurrent detection pin)
3	CO	FET gate control pin for charge (CMOS output)
4	DP	Test pin for delay time acceleration
5	VDD	Positive power input pin
6	VSS	Negative power input pin

Table 6

Pin No.	Pin name	Pin description
1	CO	FET gate control pin for charge (CMOS output)
2	VM	Voltage detection pin between VM pin and VSS pin (Overcurrent detection pin)
3	DO	FET gate control pin for discharge (CMOS output)
4	VSS	Negative power input pin
5	DP	Test pin for delay time acceleration
6	VDD	Positive power input pin

## Absolute Maximum Ratings

Table 7

(Ta=25 °C unless otherwise specified)

Item	Symbol	Applied pin	Absolute maximum ratings	Unit
Input voltage	$V_{DS}$	Between VDD and VSS	$V_{SS}-0.3$ to $V_{SS}+12^{*1}$	V
	$V_{DP}$	DP	$V_{SS}-0.3$ to $V_{DD}+0.3$	
	$V_{VM}$	VM	$V_{DD}-28$ to $V_{DD}+0.3$	
Output voltage	$V_{CO}$	CO	$V_{VM}-0.3$ to $V_{DD}+0.3$	mW
	$V_{DO}$	DO	$V_{SS}-0.3$ to $V_{DD}+0.3$	
Power dissipation	SOT-23-6	$P_D$	250	mW
	6-Pin SNB(B)		90	
Operating ambient temperature	$T_{opr}$	—	-40 to +85	°C
Storage temperature	$T_{stg}$	—	-55 to +125	

\*1. Do not apply pulse-like noise of  $\mu s$  order exceeding the above input voltage ( $V_{SS}+12$  V). The noise causes damage to the IC.

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

**■ Electrical Characteristics**
**1. Except Detection Delay Time (Ta=25°C)**
**Table 8**

(Ta=25 °C unless otherwise specified)

Item	Symbol	Condition	Remark	Min.	Typ.	Max.	Unit	Test circuit
<b>[Detection Voltage, Release Voltage]</b>								
Overcharge detection voltage, V <sub>CU</sub> =3.9 to 4.4 V, 5 mV Step	V <sub>CU</sub>	1	—	V <sub>CU</sub> -0.025	V <sub>CU</sub>	V <sub>CU</sub> +0.025	V	1
			Ta=-5 °C to 55 °C <sup>*1</sup>	V <sub>CU</sub> -0.03	V <sub>CU</sub>	V <sub>CU</sub> +0.03		
Overcharge release voltage, V <sub>CL</sub> =3.8 to 4.4 V	V <sub>CL</sub>	1	—	V <sub>CL</sub> -0.05	V <sub>CL</sub>	V <sub>CL</sub> +0.05		
Overdischarge detection voltage, V <sub>DL</sub> =2.0 to 3.0 V, 10 mV Step	V <sub>DL</sub>	2	—	V <sub>DL</sub> -0.05	V <sub>DL</sub>	V <sub>DL</sub> +0.05		2
Overdischarge release voltage, V <sub>DU</sub> =2.0 to 3.4 V,	V <sub>DU</sub>	2	—	V <sub>DU</sub> -0.1	V <sub>DU</sub>	V <sub>DU</sub> +0.1		
Overcurrent detection voltage 1, V <sub>IOV1</sub> =0.05 to 0.3 V, 10 mV Step	V <sub>IOV1</sub>	3	—	V <sub>IOV1</sub> -0.015	V <sub>IOV1</sub>	V <sub>IOV1</sub> +0.015		
Overcurrent detection voltage 2	V <sub>IOV2</sub>	3	—	0.4	0.5	0.6		
Load short-circuiting detection voltage	V <sub>SHORT</sub>	3	—	0.9	1.2	1.5		
Charger detection voltage	V <sub>CHA</sub>	4	—	-1.0	-0.7	-0.4		
<b>[Operation Voltage]</b>								
Operation voltage between VDD pin and VSS pin	V <sub>DSOP1</sub>	—	Internal circuit operating voltage	1.5	—	8	V	—
Operation voltage between VDD pin and VM pin	V <sub>DSOP2</sub>	—	Internal circuit operating voltage	1.5	—	28		
<b>[Current Consumption]</b>								
Current consumption in normal operation	I <sub>OPE</sub>	5	V <sub>DD</sub> =3.5 V, V <sub>VM</sub> =0 V	1.0	3.5	7.0	μA	2
Current consumption at power down	I <sub>PDN</sub>	5	V <sub>DD</sub> =V <sub>VM</sub> =1.5 V	—	—	0.1		
<b>[Output Resistance]</b>								
CO pin High resistance	R <sub>COH</sub>	7	V <sub>CO</sub> =3.0 V, V <sub>DD</sub> =3.5 V, V <sub>VM</sub> =0 V	2.5	5	10	kΩ	4
CO pin Low resistance	R <sub>COL</sub>	7	V <sub>CO</sub> =0.5 V, V <sub>DD</sub> =4.5 V, V <sub>VM</sub> =0 V	2.5	5	10		
DO pin High resistance	R <sub>DOH</sub>	8	V <sub>DO</sub> =3.0 V, V <sub>DD</sub> =3.5 V, V <sub>VM</sub> =0 V	2.5	5	10		
DO pin Low resistance	R <sub>DOL</sub>	8	V <sub>DO</sub> =0.5 V, V <sub>DD</sub> =V <sub>VM</sub> =1.8 V	2.5	5	10		
<b>[VM Internal Resistance]</b>								
Internal resistance between VM pin and VDD pin	R <sub>VMD</sub>	6	V <sub>DD</sub> =1.8 V, V <sub>VM</sub> =0 V	100	300	900	kΩ	3
Internal resistance between VM pin and VSS pin	R <sub>VMS</sub>	6	V <sub>DD</sub> =3.5 V, V <sub>VM</sub> =1.0 V	10	20	40		
<b>[0 V Battery Charging Function]</b>								
0 V battery charge starting charger voltage	V <sub>OCHA</sub>	11	0 V battery charging available	1.2	—	—	V	2
0 V battery charge inhibition battery voltage	V <sub>OINH</sub>	12	0 V battery charging unavailable	—	—	0.5		

\*1 Since products are not screened at low and high temperature, the specification for this temperature range is guaranteed by design, not tested in production.



2. Except Detection Delay Time ( $T_a = -40$  to  $85$  °C<sup>\*1</sup>)

Table 9

( $T_a = -40$  to  $85$  °C unless otherwise specified)

Item	Symbol	Condition	Remark	Min.	Typ.	Max.	Unit	Test circuit
<b>[Detection voltage, Release Voltage]</b>								
Overcharge detection voltage, $V_{CU}=3.9$ to $4.4$ V, 5 mV Step	$V_{CU}$	1	—	$V_{CU}-0.055$	$V_{CU}$	$V_{CU}+0.040$	V	1
Overcharge release voltage, $V_{CL}=3.8$ to $4.4$ V	$V_{CL}$	1	—	$V_{CL}-0.08$	$V_{CL}$	$V_{CL}+0.065$		
Overdischarge detection voltage, $V_{DL}=2.0$ to $3.0$ V, 10 mV Step	$V_{DL}$	2	—	$V_{DL}-0.08$	$V_{DL}$	$V_{DL}+0.08$		2
Overdischarge release voltage, $V_{DU}=2.0$ to $3.4$ V	$V_{DU}$	2	—	$V_{DU}-0.13$	$V_{DU}$	$V_{DU}+0.13$		
Overcurrent 1 detection voltage, $V_{IOV1}=0.05$ to $0.3$ V, 10 mV Step	$V_{IOV1}$	3	—	$V_{IOV1}-0.021$	$V_{IOV1}$	$V_{IOV1}+0.021$		
Overcurrent 2 detection voltage	$V_{IOV2}$	3	—	0.37	0.5	0.63		
Load short-circuiting detection voltage	$V_{SHORT}$	3	—	0.7	1.2	1.7		
Charger detection voltage	$V_{CHA}$	4	—	-1.2	-0.7	-0.2		
<b>[Operation voltage]</b>								
Operation voltage between VDD pin and VSS pin	$V_{DSOP1}$	—	Internal circuit operating voltage	1.5	—	8	V	—
Operation voltage between VDD pin and VM pin	$V_{DSOP2}$	—	Internal circuit operating voltage	1.5	—	28		
<b>[Current consumption]</b>								
Current consumption in normal operation	$I_{OPE}$	5	$V_{DD}=3.5$ V, $V_{VM}=0$ V	0.7	3.5	8.0	μA	2
Current consumption at power down	$I_{PDN}$	5	$V_{DD}=V_{VM}=1.5$ V	—	—	0.1		
<b>[Output Resistance]</b>								
CO pin High resistance	$R_{COH}$	7	$V_{CO}=3.0$ V, $V_{DD}=3.5$ V, $V_{VM}=0$ V	1.2	5	15	kΩ	4
CO pin Low resistance	$R_{COL}$	7	$V_{CO}=0.5$ V, $V_{DD}=4.5$ V, $V_{VM}=0$ V	1.2	5	15		
DO pin High resistance	$R_{DOH}$	8	$V_{DO}=3.0$ V, $V_{DD}=3.5$ V, $V_{VM}=0$ V	1.2	5	15		
DO pin Low resistance	$R_{DOL}$	8	$V_{DO}=0.5$ V, $V_{DD}=V_{VM}=1.8$ V	1.2	5	15		
<b>[VM Internal Resistance]</b>								
Internal resistance between VM pin and VDD pin	$R_{VMD}$	6	$V_{DD}=1.8$ V, $V_{VM}=0$ V	78	300	1310	kΩ	3
Internal resistance between VM pin and VSS pin	$R_{VMS}$	6	$V_{DD}=3.5$ V, $V_{VM}=1.0$ V	7.2	20	44		
<b>[0 V Battery Charging Function]</b>								
0 V battery charge starting charger voltage	$V_{0CHA}$	11	0 V battery charging available	1.7	—	—	V	2
0 V battery charge inhibition battery voltage	$V_{0INH}$	12	0 V battery charging unavailable	—	—	0.3		

\*1. Since products are not screened at low and high temperature, the specification for this temperature range is guaranteed by design, not tested in production.

## 3. Detection Delay Time

## 3-1. S-8201AAA, S-8201AAB, S-8201AAC

Table 10

Item	Symbol	Condition	Remark	Min.	Typ.	Max.	Unit	Test circuit
<b>[Delay Time] 25 °C</b>								
Overcharge detection delay time	t <sub>CU</sub>	9	—	3.7	4.6	5.5	s	5
Overdischarge detection delay time	t <sub>DL</sub>	9	—	120	150	180	ms	
Overcurrent 1 detection delay time	t <sub>I<sub>OV1</sub></sub>	10	—	7.2	9	11		
Overcurrent 2 detection delay time	t <sub>I<sub>OV2</sub></sub>	10	—	3.6	4.5	5.4		
Load short-circuiting detection delay time	t <sub>SHORT</sub>	10	—	450	600	720	μs	
Overcharge timer reset delay time	t <sub>tr</sub>	13	—	10	18	28	ms	
<b>[Delay Time] -40 to 85 °C<sup>*1</sup></b>								
Overcharge detection delay time	t <sub>CU</sub>	9	—	2.5	4.6	7.8	s	5
Overdischarge detection delay time	t <sub>DL</sub>	9	—	83	150	255	ms	
Overcurrent 1 detection delay time	t <sub>I<sub>OV1</sub></sub>	10	—	5	9	15		
Overcurrent 2 detection delay time	t <sub>I<sub>OV2</sub></sub>	10	—	2.5	4.5	7.7		
Load short-circuiting detection delay time	t <sub>SHORT</sub>	10	—	310	600	1020	μs	
Overcharge timer reset delay time	t <sub>tr</sub>	13	—	7	18	40	ms	

\*1. Since products are not screened at low and high temperature, the specification for this temperature range is guaranteed by design.

## 3-2. S-8201AAD, S-8201AAE, S-8201AAF

Table 11

Item	Symbol	Condition	Remark	Min.	Typ.	Max.	Unit	Test circuit
<b>[Delay Time] 25 °C</b>								
Overcharge detection delay time	t <sub>CU</sub>	9	—	0.96	1.2	1.4	s	5
Overdischarge detection delay time	t <sub>DL</sub>	9	—	120	150	180	ms	
Overcurrent 1 detection delay time	t <sub>I<sub>OV1</sub></sub>	10	—	7.2	9	11		
Overcurrent 2 detection delay time	t <sub>I<sub>OV2</sub></sub>	10	—	1.8	2.24	2.7		
Load short-circuiting detection delay time	t <sub>SHORT</sub>	10	—	220	320	380	μs	
Overcharge timer reset delay time	t <sub>tr</sub>	13	—	10	18	28	ms	
<b>[Delay Time] -40 to 85 °C<sup>*1</sup></b>								
Overcharge detection delay time	t <sub>CU</sub>	9	—	0.7	1.2	2.0	s	5
Overdischarge detection delay time	t <sub>DL</sub>	9	—	83	150	255	ms	
Overcurrent 1 detection delay time	t <sub>I<sub>OV1</sub></sub>	10	—	5	9	15		
Overcurrent 2 detection delay time	t <sub>I<sub>OV2</sub></sub>	10	—	1.2	2.24	3.8		
Load short-circuiting detection delay time	t <sub>SHORT</sub>	10	—	150	320	540	μs	
Overcharge timer reset delay time	t <sub>tr</sub>	13	—	7	18	40	ms	

\*1. Since products are not screened at low and high temperature, the specification for this temperature range is guaranteed by design.

3-3. S-8201BAA

Table 12

Item	Symbol	Condition	Remark	Min.	Typ.	Max.	Unit	Test circuit
<b>[Delay Time] 25 °C</b>								
Overcharge detection delay time	$t_{CU}$	9	—	3.7	4.6	5.5	s	5
Overdischarge detection delay time	$t_{DL}$	9	—	120	150	180	ms	
Overdischarge release delay time	$t_{DU}$	9	—	0.94	1.18	1.42		
Overcurrent 1 detection delay time	$t_{IOV1}$	10	—	7.2	9	11		
Overcurrent 2 detection delay time	$t_{IOV2}$	10	—	3.6	4.5	5.4		
Load short-circuiting detection delay time	$t_{SHORT}$	10	—	450	600	720	$\mu$ s	
Overcharge timer reset delay time	ttr	13	—	10	18	28	ms	
<b>[Delay Time] -40 to 85 °C<sup>*1</sup></b>								
Overcharge detection delay time	$t_{CU}$	9	—	2.5	4.6	7.8	s	5
Overdischarge detection delay time	$t_{DL}$	9	—	83	150	255	ms	
Overdischarge release delay time	$t_{DU}$	9	—	0.65	1.18	2.01		
Overcurrent 1 detection delay time	$t_{IOV1}$	10	—	5	9	15		
Overcurrent 2 detection delay time	$t_{IOV2}$	10	—	2.5	4.5	7.7		
Load short-circuiting detection delay time	$t_{SHORT}$	10	—	310	600	1020	$\mu$ s	
Overcharge timer reset delay time	ttr	13	—	7	18	40	ms	

\*1. Since products are not screened at low and high temperature, the specification for this temperature range is guaranteed by design.

## ■ Test Circuits

**Caution** Unless otherwise specified, the output voltage ( $V_{CO}$ ) levels at CO pin and DO pin and “H” and “L” at the  $V_{DO}$  are judged by the threshold voltage (1.0 V) of the N channel FET. Judge the CO pin level with respect to  $V_{VM}$  and the DO pin level with respect to  $V_{SS}$ .

### (1) Test Condition 1 (Test Circuit 1): Overcharge Detection Voltage, Overcharge Release Voltage

The overcharge detection voltage ( $V_{CU}$ ) is defined as the voltage between VDD pin and VSS pin at which  $V_{CO}$  goes from “H” to “L” when the voltage  $V_1$  is gradually increased from the starting condition of  $V_1=3.5$  V. The overcharge release voltage ( $V_{CL}$ ) is defined as the voltage between VDD pin and VSS pin at which  $V_{CO}$  goes from “L” to “H” when the voltage  $V_1$  is then gradually decreased.

The overcharge hysteresis voltage ( $V_{HC}$ ) is defined as the difference between the overcharge detection voltage ( $V_{CU}$ ) and the overcharge release voltage ( $V_{CL}$ ).

### (2) Test Condition 2 (Test Circuit 2): Overdischarge Detection Voltage, Overdischarge Release Voltage

The overdischarge detection voltage ( $V_{DL}$ ) is defined as the voltage between VDD pin and VSS pin at which  $V_{DO}$  goes from “H” to “L” when the voltage  $V_1$  is gradually decreased from the starting condition of  $V_1=3.5$  V,  $V_2=0$  V. The overdischarge release voltage ( $V_{DU}$ ) is defined as the voltage between VDD pin and VSS pin at which  $V_{DO}$  goes from “L” to “H” when the voltage  $V_1$  is then gradually increased.

The overdischarge hysteresis voltage ( $V_{HD}$ ) is defined as the difference between the overcharge release voltage ( $V_{DU}$ ) and the overdischarge detection voltage ( $V_{DL}$ ).

### (3) Test Condition 3 (Test Circuit 2): Overcurrent 1 Detection Voltage, Overcurrent 2 Detection Voltage, Load Short-circuiting Detection Voltage

The overcurrent 1 detection voltage is defined by the voltage between VM pin and VSS pin whose delay time for changing  $V_{DO}$  from “H” to “L” lies between the minimum and the maximum value of the overcurrent 1 detection delay time when the voltage  $V_2$  is increased rapidly within 10  $\mu$ s from the starting condition  $V_1=3.5$  V and  $V_2=0$  V.

The overcurrent 2 detection voltage is defined by the voltage between VM pin and VSS pin whose delay time for changing  $V_{DO}$  from “H” to “L” lies between the minimum and the maximum value of the overcurrent 2 detection delay time when the voltage  $V_2$  is increased rapidly within 10  $\mu$ s from the starting condition  $V_1=3.5$  V and  $V_2=0$  V.

The load short-circuiting detection voltage is defined by the voltage between VM pin and VSS pin whose delay time for changing  $V_{DO}$  from “H” to “L” lies between the minimum and the maximum value of the load short-circuiting detection delay time when the voltage  $V_2$  is increased rapidly within 10 $\mu$ s from the starting condition  $V_1=3.5$  V and  $V_2=0$  V.

### (4) Test Condition 4 (Test Circuit 2): Charger Detection Voltage (=Abnormal Charge Current Detection Voltage)

Set  $V_1=1.8$  V and  $V_2=0$  V. Increase  $V_1$  gradually until  $V_1=V_{DL}+(V_{HD}/2)$ , then decrease  $V_2$  from 0 V gradually. The voltage between VM pin and VSS pin when  $V_{DO}$  goes from “L” to “H” is the charger detection voltage ( $V_{CHA}$ ). Charger detection voltage can be measured only in the product whose overdischarge hysteresis  $V_{HD} \neq 0$ .

Set  $V_1=3.5$  V and  $V_2=0$  V. Decrease  $V_2$  from 0 V gradually. The voltage between VM pin and VSS pin when  $V_{CO}$  goes from “H” to “L” is the abnormal charge current detection voltage. The abnormal charge current detection voltage has the same value as the charger detection voltage ( $V_{CHA}$ ).

**(5) Test Condition 5 (Test Circuit 2): Normal Operation Current Consumption, Power-down Current Consumption**

Set  $V1=3.5\text{ V}$  and  $V2=0\text{ V}$  under normal condition. The current  $I_{DD}$  flowing through VDD pin is the normal operation consumption current ( $I_{OPE}$ ).

Set  $V1=V2=1.5\text{ V}$  under overdischarge condition. The current  $I_{DD}$  flowing through VDD pin is the power-down current consumption ( $I_{PDN}$ ).

**(6) Test Condition 6 (Test Circuit 3): Internal Resistance between VM Pin and VDD Pin, Internal Resistance between VM Pin and VSS Pin**

Set  $V1=1.8\text{ V}$  and  $V2=0\text{ V}$ . The resistance between VM pin and VDD pin is the internal resistance ( $R_{VMD}$ ) between VM pin and VDD pin.

Set  $V1=3.5\text{ V}$  and  $V2=1.0\text{ V}$ . The resistance between VM pin and VSS pin is the internal resistance ( $R_{VMS}$ ) between VM pin and VSS pin.

**(7) Test Condition 7 (Test Circuit 4): CO Pin H Resistance, CO Pin L Resistance**

Set  $V1=3.5\text{ V}$ ,  $V2=0\text{ V}$  and  $V3=3.0\text{ V}$ . CO pin resistance is the CO pin H resistance ( $R_{COH}$ ).

Set  $V1=4.5\text{ V}$ ,  $V2=0\text{ V}$  and  $V3=0.5\text{ V}$ . CO pin resistance is the CO pin L resistance ( $R_{COL}$ ).

**(8) Test Condition 8 (Test Circuit 4): DO Pin H Resistance, DO Pin L Resistance**

Set  $V1=3.5\text{ V}$ ,  $V2=0\text{ V}$  and  $V4=3.0\text{ V}$ . DO pin resistance is the DO pin H resistance ( $R_{DOH}$ ).

Set  $V1=1.8\text{ V}$ ,  $V2=0\text{ V}$  and  $V4=0.5\text{ V}$ . DO pin resistance is the DO pin L resistance ( $R_{DOL}$ ).

**(9) Test Condition 9 (Test Circuit 5): Overcharge Detection Delay Time, Overdischarge Detection Delay Time, Overdischarge Release Delay Time**

The overcharge detection delay time ( $t_{CU}$ ) is the time needed for  $V_{CO}$  to change from "H" to "L" just after the V1 rapid increase within  $10\text{ }\mu\text{s}$  from the overcharge detection voltage ( $V_{CU}$ )  $-0.2\text{ V}$  to the overcharge detection voltage ( $V_{CU}$ )  $+0.2\text{ V}$  in the condition  $V2=0\text{ V}$ .

The overdischarge detection delay time ( $t_{DL}$ ) is the time needed for  $V_{DO}$  to change from "H" to "L" just after the V1 rapid decrease within  $10\text{ }\mu\text{s}$  from the overdischarge detection voltage ( $V_{DL}$ )  $+0.2\text{ V}$  to the overdischarge detection voltage ( $V_{DL}$ )  $-0.2\text{ V}$  in the condition  $V2=0\text{ V}$ .

The overdischarge release delay time ( $t_{DU}$ ) is the time needed for  $V_{DO}$  to change from "L" to "H" just after the V1 rapid increase within  $10\text{ }\mu\text{s}$  from the overdischarge release voltage ( $V_{DU}$ )  $-0.2\text{ V}$  to the overdischarge release voltage ( $V_{DU}$ )  $+0.2\text{ V}$  in the condition  $V2=0\text{ V}$ .

**(10) Test Condition 10 (Test Circuit 5): Overcurrent 1 Detection Delay Time, Overcurrent 2 Detection Delay Time, Load Short-circuiting Detection Delay Time, Abnormal Charge Current Detection Delay Time**

Set  $V1=3.5\text{ V}$  and  $V2=0\text{ V}$ . Increase  $V2$  from  $0\text{ V}$  to  $0.35\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ). The time needed for  $V_{DO}$  to go "L" is overcurrent detection delay time 1 ( $t_{IOV1}$ ).

Set  $V1=3.5\text{ V}$  and  $V2=0\text{ V}$ . Increase  $V2$  from  $0\text{ V}$  to  $0.7\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ). The time needed for  $V_{DO}$  to go "L" is overcurrent detection delay time 2 ( $t_{IOV2}$ ).

Set  $V1=3.5\text{ V}$  and  $V2=0\text{ V}$ . Increase  $V2$  from  $0\text{ V}$  to  $1.6\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ). The time needed for  $V_{DO}$  to go "L" is the load short-circuiting detection delay time ( $t_{SHORT}$ ).

Set  $V1=3.5\text{ V}$  and  $V2=0\text{ V}$ . Decrease  $V2$  from  $0\text{ V}$  to  $-1.1\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ). The time needed for  $V_{CO}$  to go "L" is the abnormal charge current detection delay time. The abnormal charge current detection delay time has the same value as the overcharge detection delay time.

**(11) Test Condition 11 (Test Circuit 2): 0 V Battery Charge Starting Charger Voltage (Product with 0 V Battery Charge Function)**

Set  $V1=V2=0\text{ V}$  and decrease  $V2$  gradually. The voltage between  $VDD$  pin and  $VM$  pin when  $V_{CO}$  goes "H" ( $V_{VM}+0.1\text{ V}$  or higher) is the 0 V battery charge starting charger voltage ( $V_{0CHA}$ ).

**(12) Test Condition 12 (Test Circuit 2): 0 V Battery Charge Inhibition Battery Voltage (Product with 0 V Battery Charge Inhibition Function)**

Set  $V1=0\text{ V}$  and  $V2=-4\text{ V}$  and increase  $V1$  gradually. The voltage between  $VDD$  pin and  $VSS$  pin when  $V_{CO}$  goes "H" ( $V_{VM}+0.1\text{ V}$  or higher) is the 0 V battery charge inhibition battery voltage ( $V_{0INH}$ ).

**(13) Test Condition 13 (Test Circuit 5): Overcharge Timer Reset Delay Time**

Set  $V2=0\text{ V}$ . Increase  $V1$  from overcharge detection voltage ( $V_{CU}$ )  $-0.2\text{ V}$  to overcharge detection voltage ( $V_{CU}$ )  $+0.2\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ), then decrease  $V1$  again to overcharge detection voltage ( $V_{CU}$ )  $-0.2\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ) after half the overcharge detection delay time ( $t_{CU}$ ) has elapsed.

Following  $t_{tr\text{ Min.}}$ , again increase  $V1$  to overcharge detection voltage ( $V_{CU}$ )  $+0.2\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ) and check that  $V_{CO}$  changes from "H" to "L" after the overcharge detection delay time from when  $V1$  is first increased momentarily (within  $10\text{ }\mu\text{s}$ ) to overcharge detection voltage ( $V_{CU}$ )  $+0.2\text{ V}$ .

Set  $V2=0\text{ V}$ . Increase  $V1$  from overcharge detection voltage ( $V_{CU}$ )  $-0.2\text{ V}$  to overcharge detection voltage ( $V_{CU}$ )  $+0.2\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ), then decrease  $V1$  again to overcharge detection voltage ( $V_{CU}$ )  $-0.2\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ) after half the overcharge detection delay time ( $t_{CU}$ ) has elapsed.

Following  $t_{tr\text{ Max.}}$ , again increase  $V1$  to overcharge detection voltage ( $V_{CU}$ )  $+0.2\text{ V}$  momentarily (within  $10\text{ }\mu\text{s}$ ) and check that  $V_{CO}$  stays "H" after the overcharge detection delay time from when  $V1$  is first increased momentarily (within  $10\text{ }\mu\text{s}$ ) to overcharge detection voltage ( $V_{CU}$ )  $+0.2\text{ V}$ .

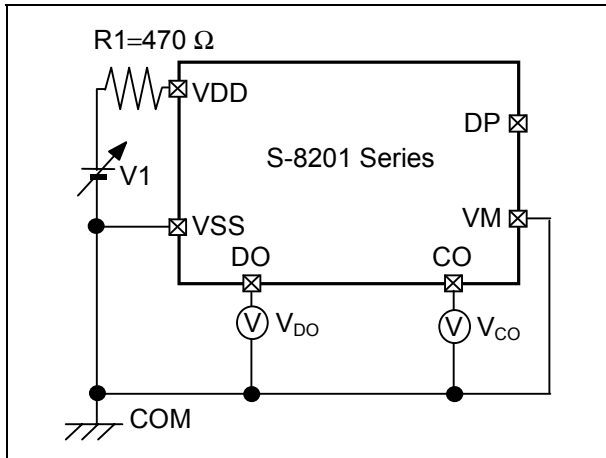


Figure 4 Test Circuit 1

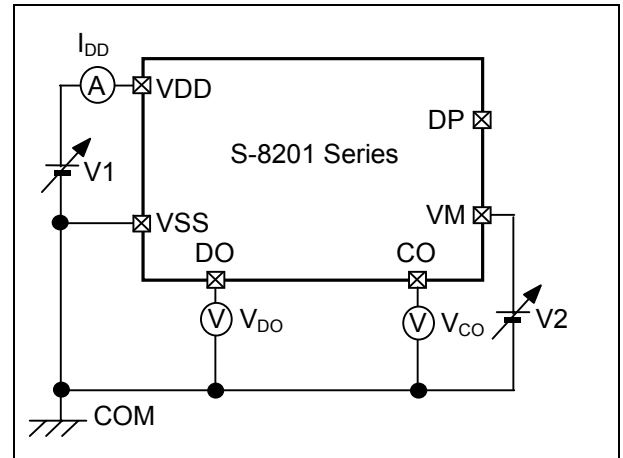


Figure 5 Test Circuit 2

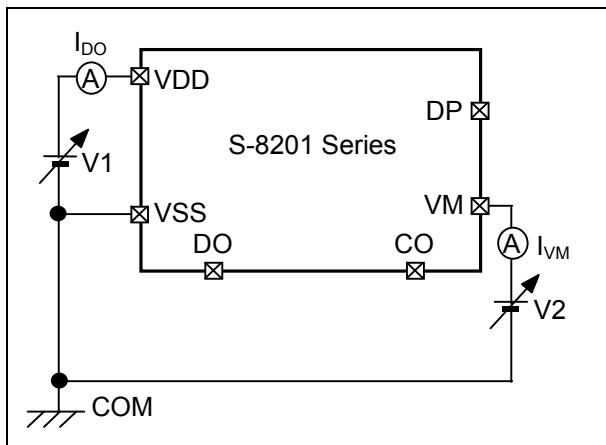


Figure 6 Test Circuit 3

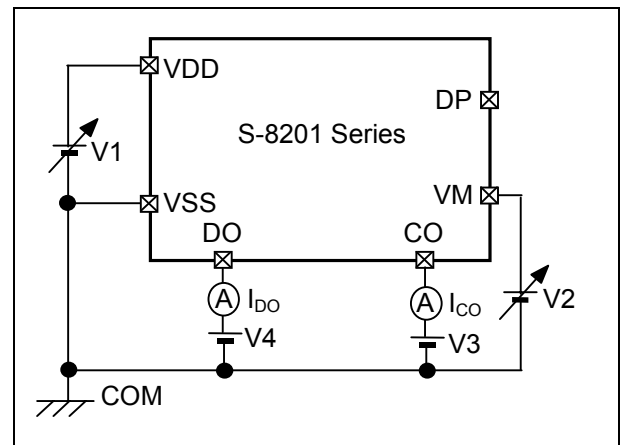


Figure 7 Test Circuit 4

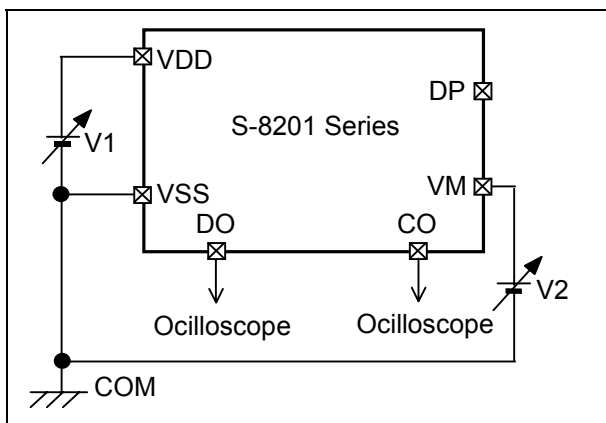


Figure 8 Test Circuit 5

## ■ Operation

**Remark** Refer to the “■ Example for Battery Protection IC Connection”.

### 1. Normal Condition

The S-8201 Series monitors the voltage of the battery connected between VDD pin and VSS pin and the voltage difference between VM pin and VSS pin to control charging and discharging. When the battery voltage is in the range from the overdischarge detection voltage ( $V_{DL}$ ) to the overcharge detection voltage ( $V_{CU}$ ), and the VM pin voltage is in the range from the charger detection voltage ( $V_{CHA}$ ) to the overcurrent 1 detection voltage ( $V_{IOV1}$ ), the IC turns both the charging and discharging control FETs on. This condition is called the normal condition, and in this condition charging and discharging can be carried out freely.

**Caution** When a battery is connected to the IC for the first time, the battery may not enter dischargeable state. In this case, set the VM pin voltage equal to the VSS pin voltage or connect a charger to enter the normal condition.

### 2. Overcurrent Condition (Overcurrent 1 Detection, Overcurrent 2 Detection, and Load Short-circuiting Detection)

When the condition in which VM pin voltage is equal to or higher than the overcurrent detection voltage, condition that caused by the excess of discharging current over a specified value, continues longer than the overcharge detection delay time in a battery under the normal condition, the S-8201 Series turns the discharging control FET off to stop discharging. This condition is called the overcurrent condition. Though the VM pin and VSS pin are shorted by the resistor in the IC ( $R_{VMS}$ ) under the overcurrent condition provided that the VM pin voltage is pulled to the  $V_{DD}$  level by the load as long as the load is connected.

The VM pin voltage returns to  $V_{SS}$  level when the load is released. The overcurrent condition returns to the normal condition when the impedance between the EB+ and EB- pin (Refer to **Figure 14**) becomes higher than the automatic recoverable impedance and the IC detects that the VM pin potential is lower than the overcurrent 1 detection voltage ( $V_{IOV1}$ ).

**Caution** The automatic recoverable impedance changes depending on the battery voltage and overcurrent 1 detection voltage settings.



### 3. Overcharge Condition

When the battery voltage becomes higher than the overcharge detection voltage ( $V_{CU}$ ) during charging under the normal condition and the detection continues for the overcharge detection delay time ( $t_{CU}$ ) or longer, the S-8201 Series turns the charging control FET off to stop charging. This condition is called the overcharge condition.

The overcharge condition is released by the following two cases ((1) and (2)):

- (1) When the battery voltage falls below the overcharge release voltage, which is equal to the overcharge detection voltage ( $V_{CU}$ )–overcharge detection hysteresis voltage ( $V_{HC}$ ), the S-8201 Series turns the charging control FET on and turns to the normal condition.
- (2) When a load is connected and discharging starts, the S-8201 Series turns the charging control FET on and returns to the normal condition. Just after the load is connected and discharging starts, the discharging current flows through the parasitic diode in the charging control FET. At this moment the VM pin potential becomes  $V_f$  voltage, the voltage for the parasitic diode, higher than  $V_{SS}$  level. When the battery voltage goes under the overcharge detection voltage ( $V_{CU}$ ) and provided that the VM pin voltage is higher than the overcurrent 1 detection voltage, the S-8201 Series releases the overcharge condition.

**Caution 1. If the battery is charged to a voltage higher than the overcharge detection voltage ( $V_{CU}$ ) and the battery voltage does not fall below the overcharge detection voltage ( $V_{CU}$ ) even when a heavy load is connected, the detection of overcurrent 1, overcurrent 2 and load short-circuiting does not work. Since an actual battery has the internal impedance of several dozens of  $m\Omega$ , the battery voltage drops immediately after a heavy load which causes overcurrent is connected, and the detection of overcurrent 1, overcurrent 2 and load short-circuiting then works.**

- 2. When a charger is connected after the overcharge detection, the overcharge condition is not released even if the battery voltage is below the overcharge release voltage  $V_{CL}$  ( $=V_{CU}-V_{HC}$ ). The overcharge condition is released when the VM pin voltage goes over the charger detection voltage ( $V_{CHA}$ ) by removing the charger.**
- 3. If the overcharge release pulse for less than the overcharge timer reset delay time ( $t_{tr}$ ) is input during the overcharge detection delay time ( $t_{CU}$ ) that after exceeding the overcharge detection voltage ( $V_{CU}$ ), the  $t_{CU}$  keeps the count. However, if the overcharge release pulse is input for  $t_{tr}$  or longer under the same conditions, the  $t_{CU}$  count is reset.**

### 4. Overdischarge Condition

When the battery voltage falls below the overdischarge detection voltage ( $V_{DL}$ ) during discharging under the normal condition and the detection continues for the overdischarge detection delay time ( $t_{DL}$ ) or longer, the S-8201 Series turns the discharging control FET off to stop discharging. This condition is called the overdischarge condition. When the discharging control FET turns off, the VM pin voltage is pulled up by the resistor between VM pin and VDD pin in the IC ( $R_{VMD}$ ). The voltage difference between VM pin and VDD pin then falls below 1.3 V (typ.), the current consumption is reduced to the power-down current consumption ( $I_{PDN}$ ). This condition is called the power-down condition.

The power-down condition is released when a charger is connected and the voltage difference between VM pin and VDD pin becomes 1.3 V (typ.) or higher. Moreover when the battery voltage becomes the overdischarge detection voltage ( $V_{DL}$ ) or higher the S-8201 Series turns the discharging FET on and returns to the normal condition.

## 5. Charger Detection

When a battery in the overdischarge condition is connected to a charger and provided that the VM pin voltage is lower than the charger detection voltage ( $V_{CHA}$ ), the S-8201 Series releases the overdischarge condition and turns the discharging control FET on as the battery voltage becomes equal to or higher than the overdischarge detection voltage ( $V_{DL}$ ) since the charger detection function works. This action is called charger detection.

When a battery in the overdischarge condition is connected to a charger and provided that the VM pin voltage is not lower than the charger detection voltage ( $V_{CHA}$ ), the S-8201 Series releases the overdischarge condition when the battery voltage reaches the overdischarge detection voltage ( $V_{DL}$ ) + overdischarge hysteresis ( $V_{HD}$ ) or higher.

## 6. Abnormal Charge Current Detection

If the VM pin voltage falls below the charger detection voltage ( $V_{CHA}$ ) during charging under normal condition and it continues for the overcharge detection delay time ( $t_{CU}$ ) or longer, the charging control FET turns off and charging stops. This action is called the abnormal charge current detection.

Abnormal charge current detection works when the DO pin voltage is "H" and the VM pin voltage falls below the charger detection voltage ( $V_{CHA}$ ). Consequently, if an abnormal charge current flows to an over-discharged battery, the S-8201 Series turns the charging control FET off and stops charging after the battery voltage becomes higher than the overdischarge detection voltage which make the DO pin voltage "H", and still after the overcharge detection delay time ( $t_{CU}$ ) elapses.

Abnormal charge current detection is released when the voltage difference between VM pin and VSS pin becomes less than charger detection voltage ( $V_{CHA}$ ).

## 7. Delay Circuits

The detection delay times are generated by dividing the approximate 3.5 kHz clock with a counter.

**Caution1.** The detection delay time for overcurrent 2 and load and short-circuiting start when the overcurrent 1 is detected. As soon as the overcurrent 2 or load short-circuiting is detected over the detection delay time for overcurrent 2 or load short-circuiting after the detection of overcurrent 1, the S-8201 Series turns the discharging control FET off.

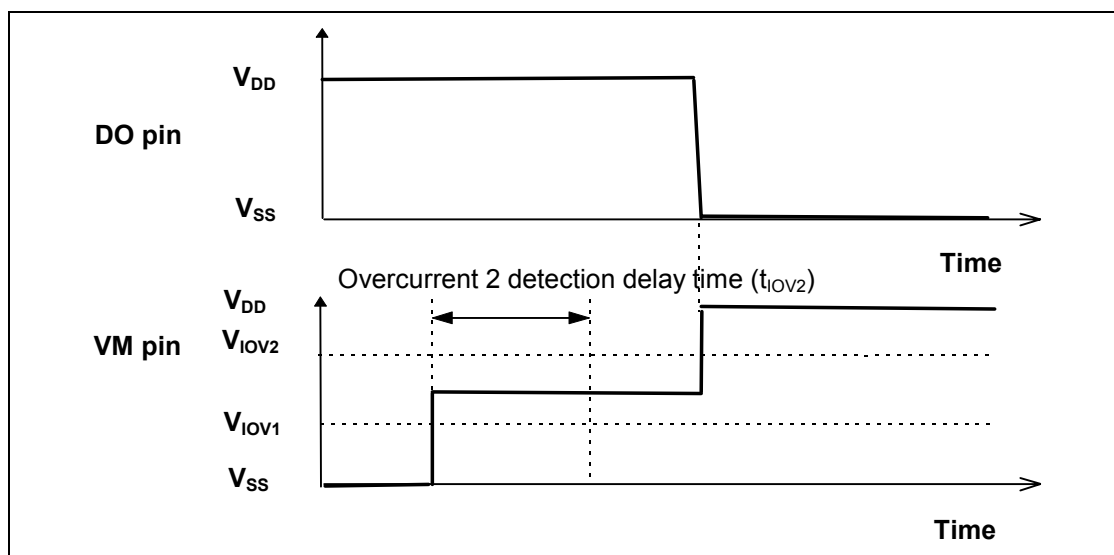


Figure 9

2. When the overcurrent is detected and it continues for longer than the overdischarge detection delay time without releasing the load, the condition changes to the power-down condition when the battery voltage falls below the overdischarge detection voltage.
3. When the battery voltage falls below the overdischarge detection voltage due to the overcurrent, the S-8201 Series turns the discharging control FET off by the overcurrent detection. And in this case the recovery of the battery voltage is so slow that the battery voltage after the overdischarge detection delay time is still lower than the overdischarge detection voltage, the S-8201 Series transits to the power-down condition.

## 8. DP Pin

The DP pin is a test pin for delay time acceleration. When the DP pin is set to the VDD pin potential, the delay time is reduced by about 1/15 to 1/40. (25°C). The DP pin should be left open during normal operation.

## 9. 0 V Battery Charge Function

This function is used to recharge the connected battery whose voltage is 0 V due to the self-discharge. When the 0V battery charge starting charger voltage ( $V_{0CHA}$ ) or higher is applied between EB+ and EB- pins by connecting a charger, the charging control FET gate is fixed to VDD pin voltage. When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging control FET turns on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than the overdischarge release voltage ( $V_{DU}$ ), the S-8201 Series enters the normal condition.

**Caution 1. Some battery providers do not recommend charging for completely self-discharged battery. Please ask battery providers before determining the 0 V battery charge function.**

- 2. The 0 V battery charge function has higher priority than the abnormal charge current detection function. Consequently, a product with the 0 V battery charge function charges a battery forcedly and abnormal charge current cannot be detected when the battery voltage is low.**

## 10. 0 V battery charge inhibition function

This function inhibits the recharging when a battery which is short-circuited (0 V) internally is connected. When the battery voltage is 0.6 V (typ.) or lower, the charging control FET gate is fixed to EB- pin voltage to inhibit charging. When the battery voltage is the 0 V battery charge inhibition battery voltage ( $V_{0INH}$ ) or higher, charging can be performed.

**Caution Some battery providers do not recommend charging for completely self-discharged battery. Please ask battery providers before determining the 0 V battery charge function.**

■ Timing Chart

1. Overcharge and Overdischarge Detection

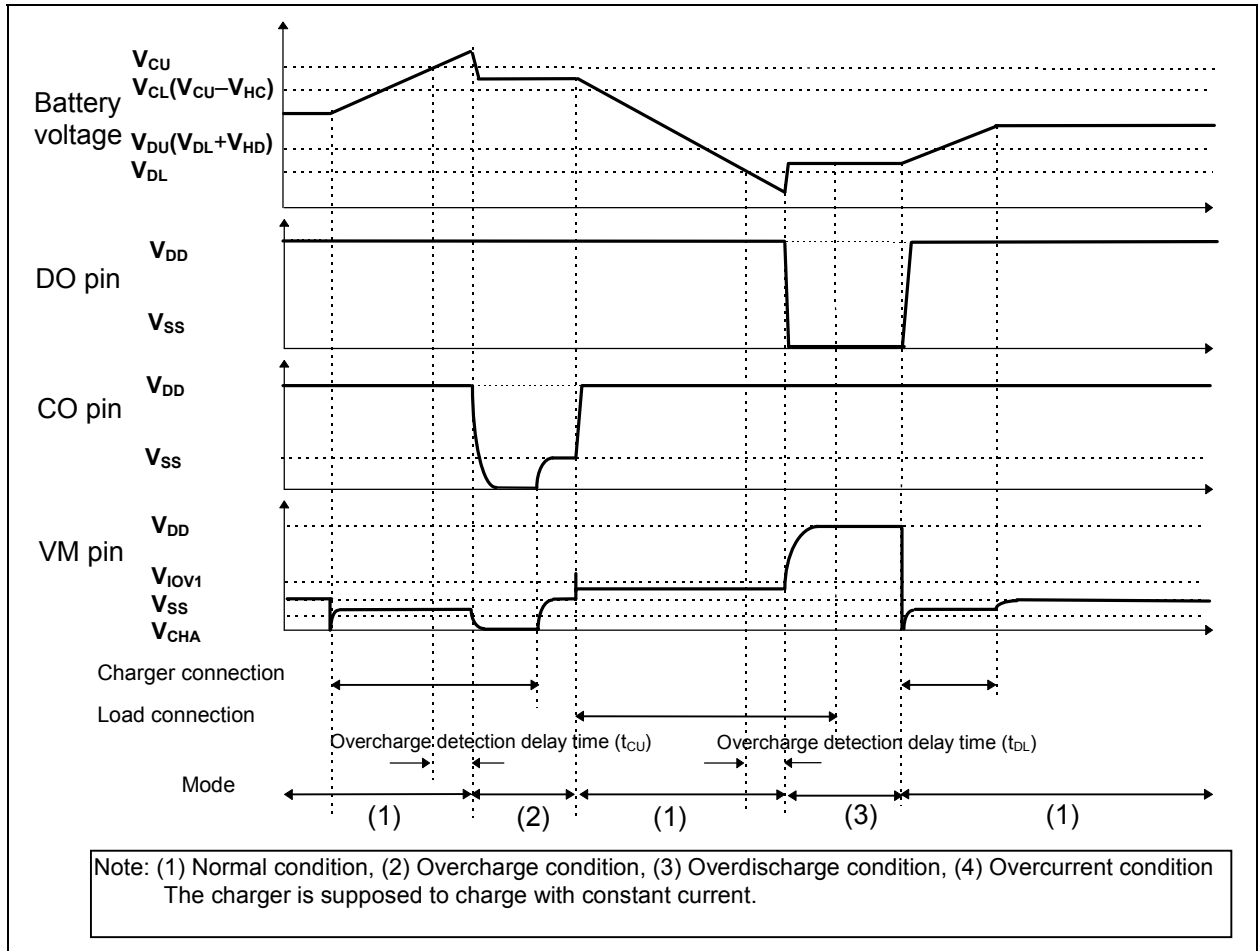
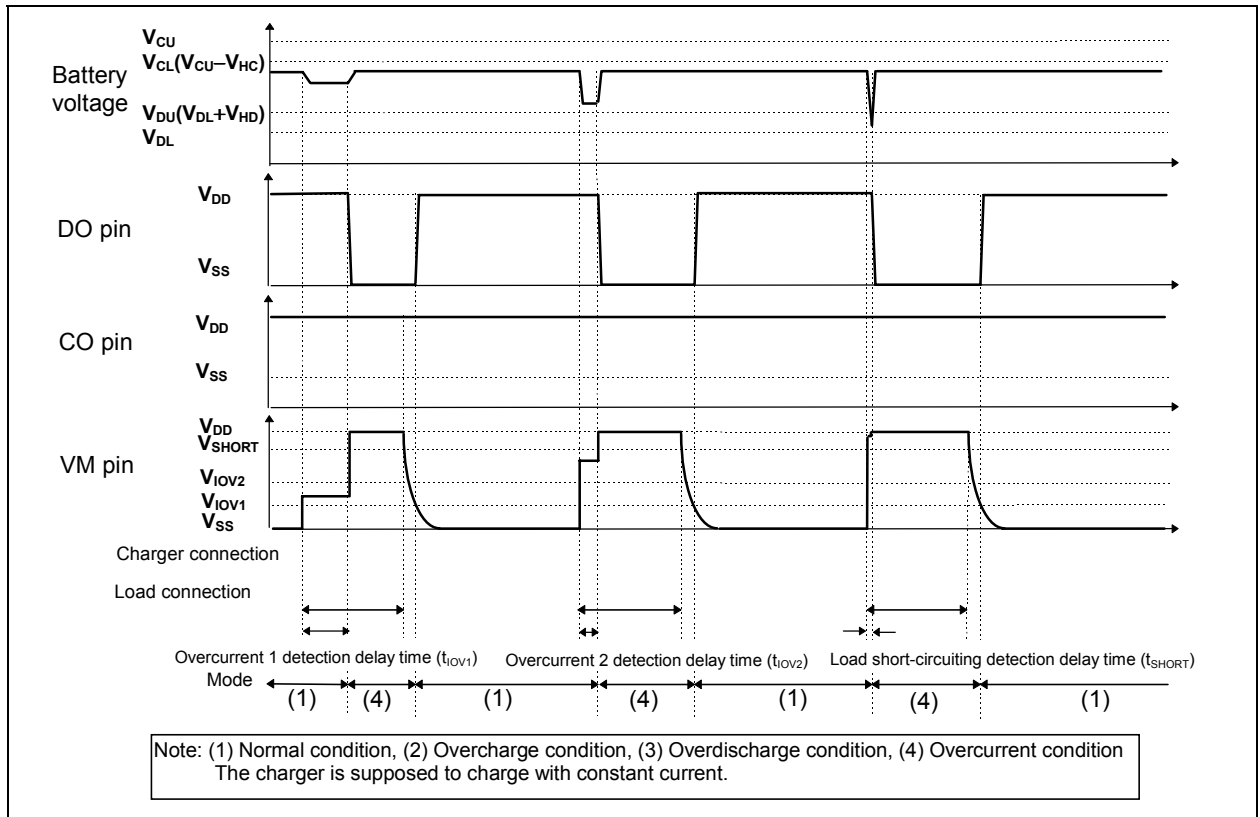


Figure 10

**2. Overcurrent Detection**



**Figure 11**

### 3. Charger Detection

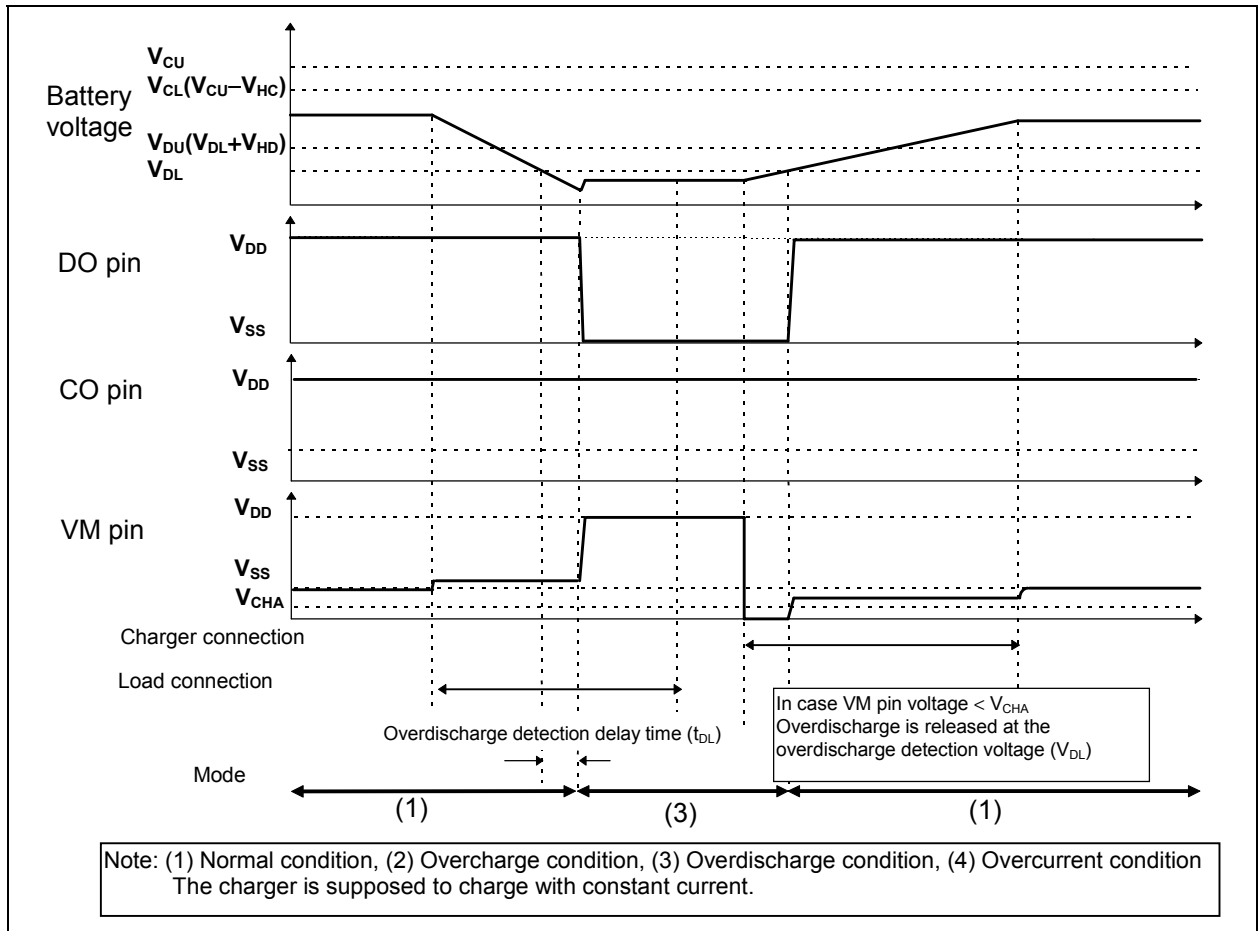
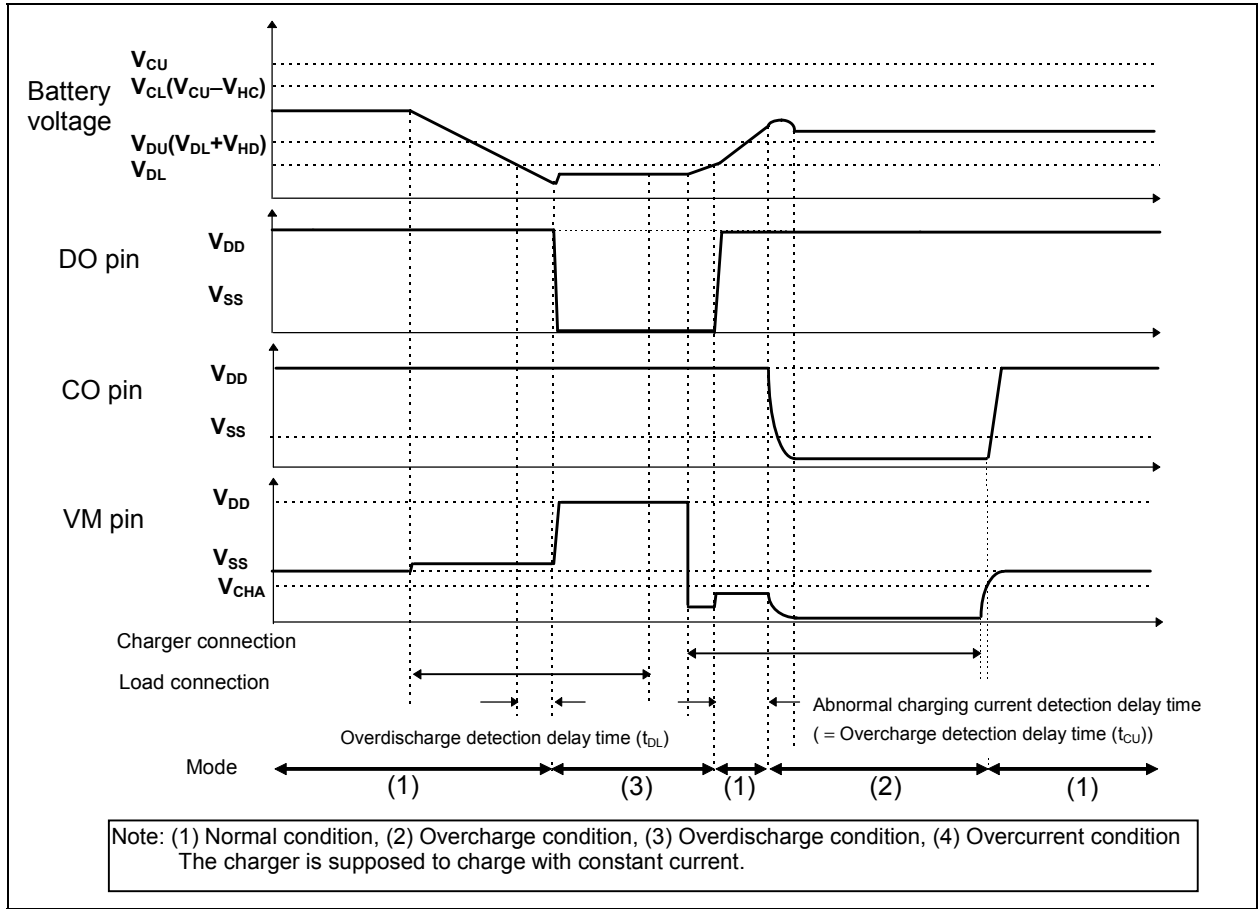


Figure 12

**4. Abnormal Charge Current Detection**



**Figure 13**



■ Example for Battery Protection IC Connection

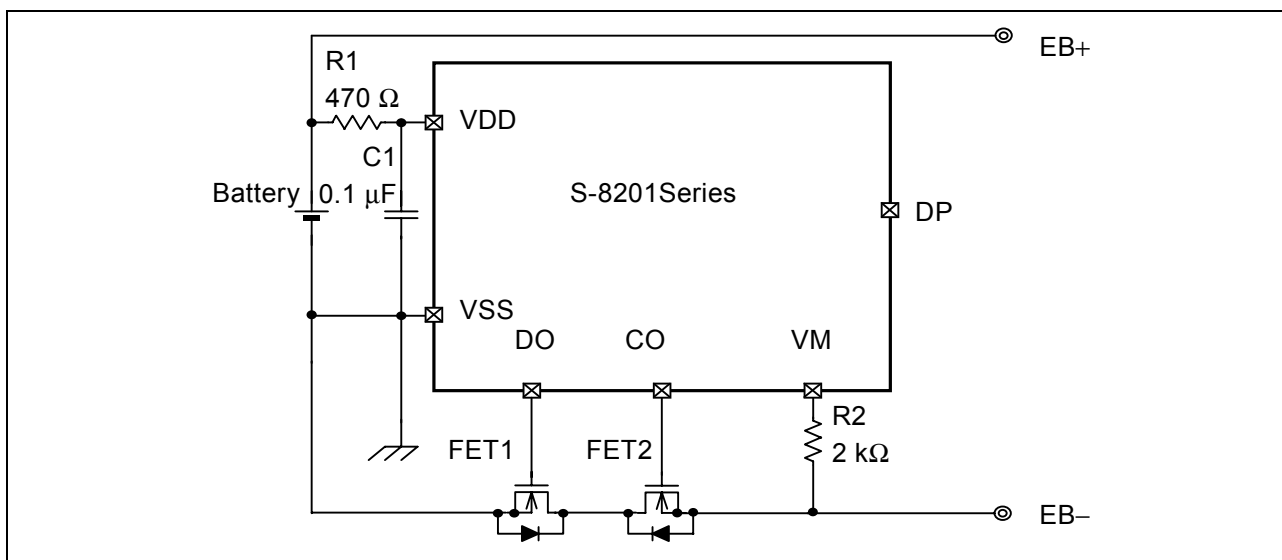


Figure 14

Table 13 Constant for External Components

Symbol	Parts	Purpose	Recommend	Min.	Max.	Remarks
FET1	Nch MOS FET	Charge control	—	—	—	Threshold voltage ≤ overdischarge detection voltage <sup>*1</sup> , Gate to source withstand voltage ≥ Charger voltage
FET2	Nch MOS FET	Discharge control	—	—	—	Threshold voltage ≤ overdischarge detection voltage <sup>*1</sup> , Gate to source withstand voltage ≥ Charger voltage
R1	Resistor	ESD protection, For power fluctuation	470 Ω	300 Ω	1 kΩ	Resistance should be as small as possible to avoid lowering of the overcharge detection accuracy caused by VDD pin current. <sup>*2</sup>
C1	Capacitor	For power fluctuation	0.1 μF	0.022 μF	1.0 μF	Install a capacitor of 0.022 μF or higher between VDD pin and VSS pin. <sup>*3</sup>
R2	Resistor	Protection for reverse connection of a charger	2 kΩ	300 Ω	4 kΩ	Select a resistance as large as possible to prevent current when a charger is reversely connected. <sup>*4</sup>

- \*1. If the threshold voltage of an EFT is low, the FET may not cut the charging current.  
If an FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.  
If the withstand voltage between the gate and source is lower than the charger voltage, the FET may destroy.
- \*2. If R1 has a high resistance, the voltage between VDD pin and VSS pin may exceed the absolute maximum rating when a charger is connected reversely since the current flows from the charger to the IC. Insert a resistor of 300 Ω or higher as R1 for ESD protection.
- \*3. If a capacitor of less than 0.022 μF is installed as C1, DO may oscillate when load short-circuiting is detected. Be sure to install a capacitor of 0.022 μF or higher as C1.
- \*4. If R2 has a resistance higher than 4 kΩ, the charging current may not be cut when a high-voltage charger is connected.

**Caution** 1. The DP pin should be open.  
2. The above connection diagram and constants will not guarantees successful operation.  
Perform through evaluation using the actual application to set the constant.

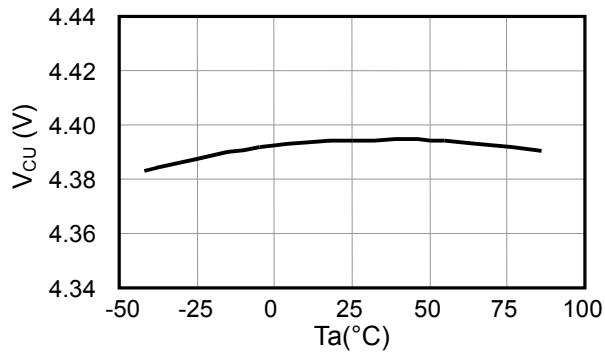
**■ Precautions**

- The application condition for input voltage, output voltage and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

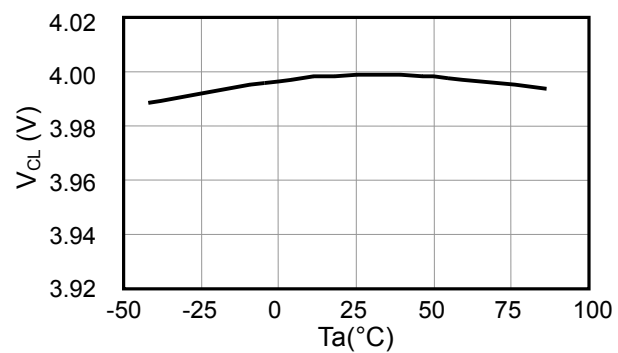
## ■ Typical Characteristics (Typical Data)

### 1. Detection/Release Voltage Temperature Characteristics

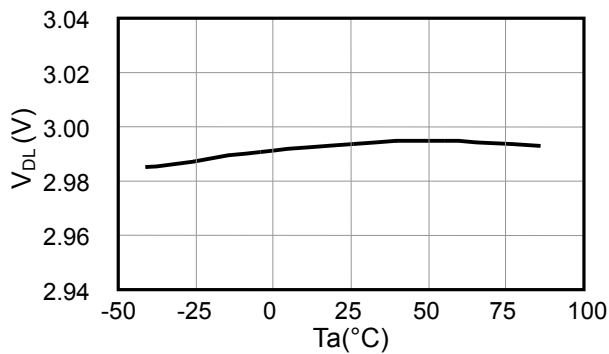
Overcharge detection voltage vs. temperature



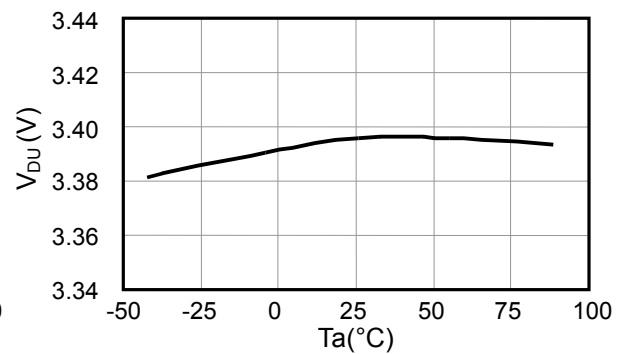
Overcharge release voltage vs. temperature



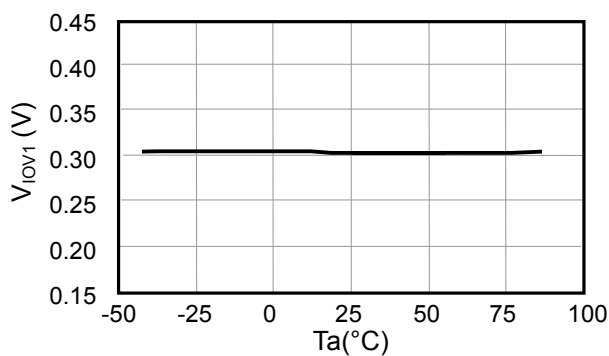
Overdischarge detection voltage vs. temperature



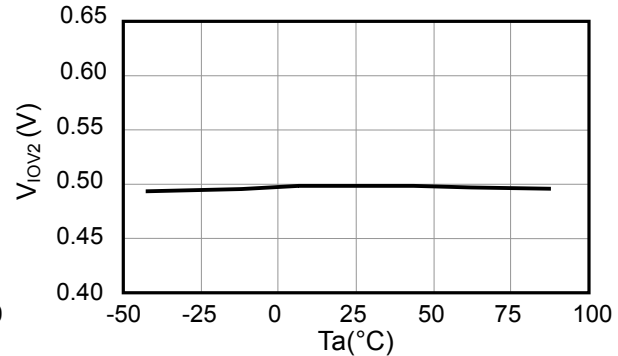
Overdischarge release voltage vs. temperature



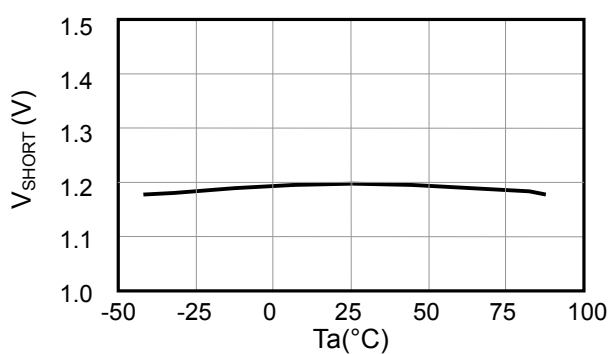
Overcurrent1 detection voltage vs. temperature



Overcurrent 2 detection voltage vs. temperature

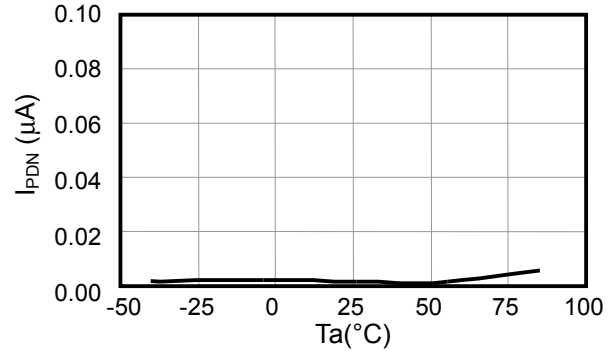
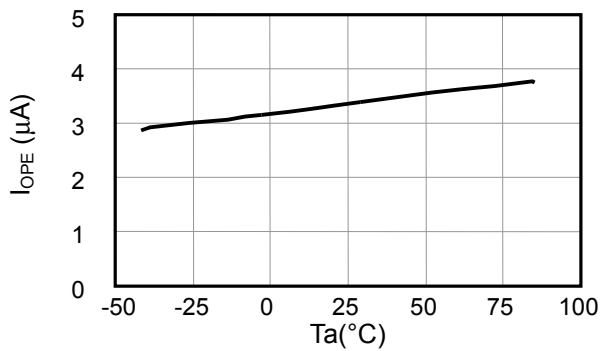


Load short-circuiting detection voltage vs. temperature



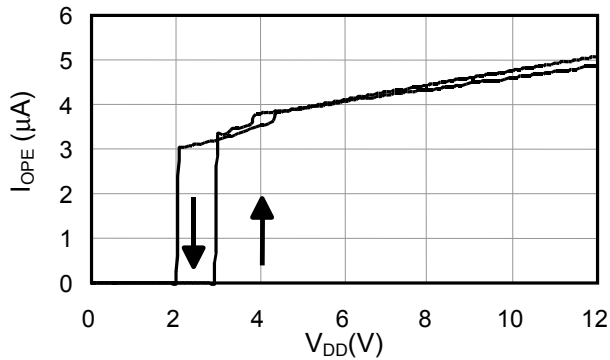
## 2. Current Consumption Temperature Characteristics

Current consumption vs. temperature in normal mode    Current consumption vs. temperature in power-down mode



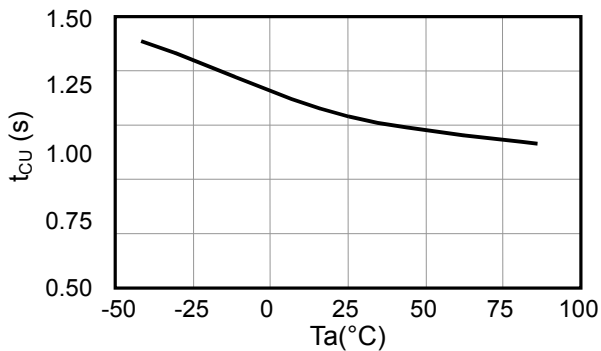
## 3. Current Consumption Power Voltage Characteristics ( $T_a=25^{\circ}C$ )

Current consumption power supply voltage dependency

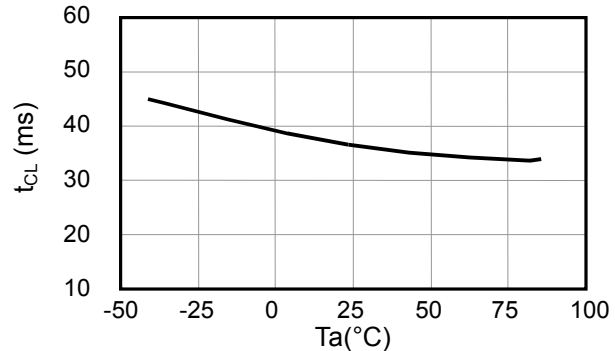


## 4. Detection/Release Delay Time Temperature Characteristics

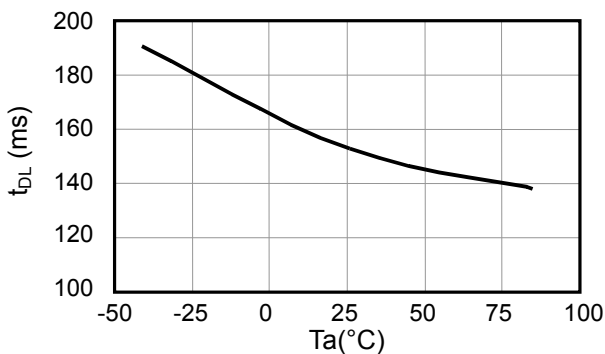
Overcharge detection delay time vs. temperature



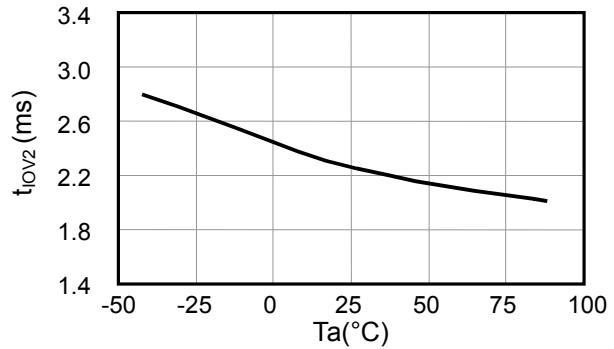
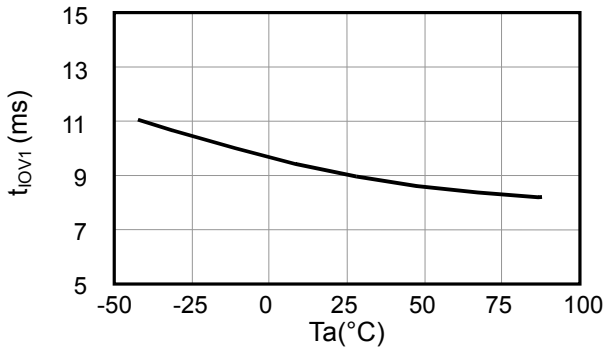
Overcharge release delay time vs. temperature



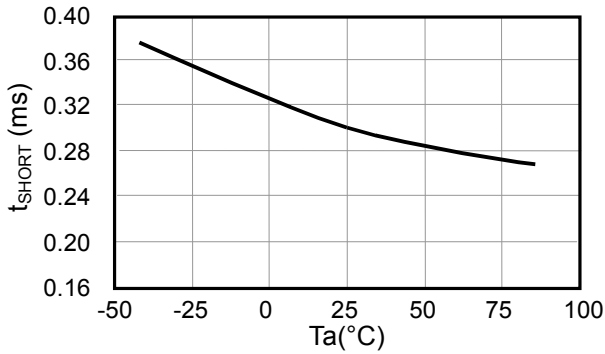
Overdischarge detection delay time vs. temperature



Overcurrent 1 detection delay time vs. temperature Overcurrent 2 detection delay time vs. temperature

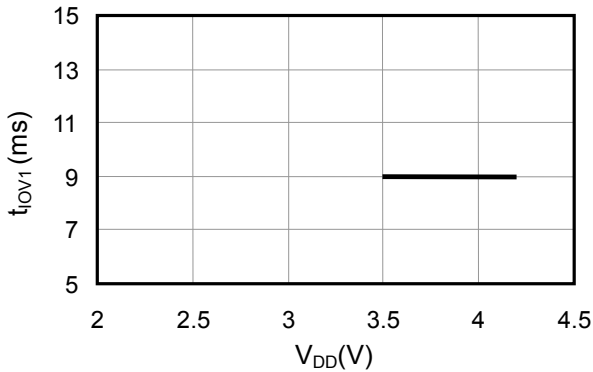


Load short-circuiting delay time vs. temperature

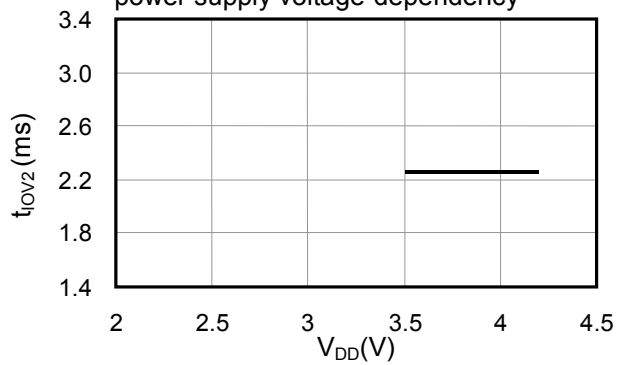


**5. Delay Time Power-voltage Characteristics (Ta=25°C)**

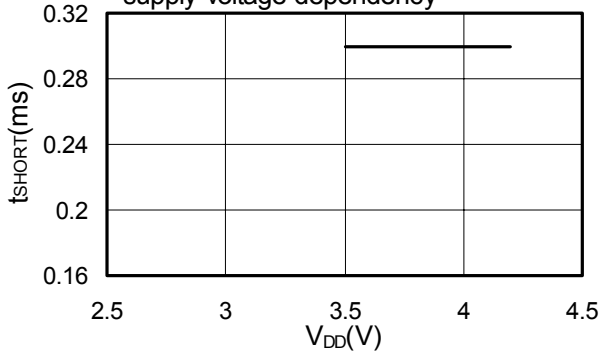
Overcurrent 1 detection delay time vs. power supply voltage dependency



Overcurrent 2 detection delay time vs. power supply voltage dependency

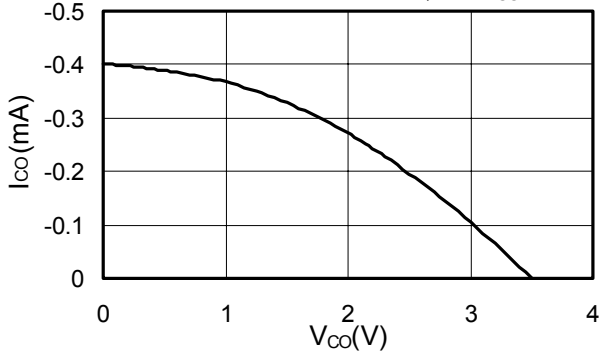


Load short-circuiting delay time vs. power supply voltage dependency

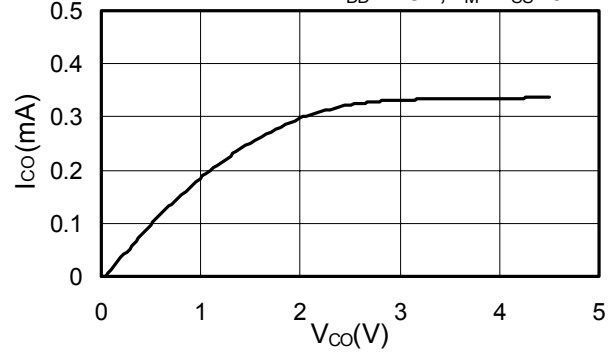


**6. CO Pin/DO Pin Output Current Characteristics (Ta=25°C)**

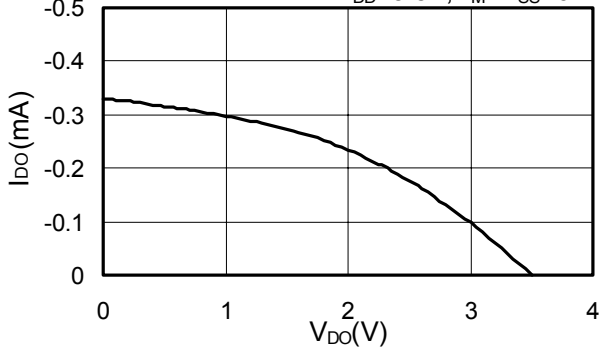
CO pin source current characteristics

 $V_{DD}=3.5V, V_M=V_{SS}=0V$ 

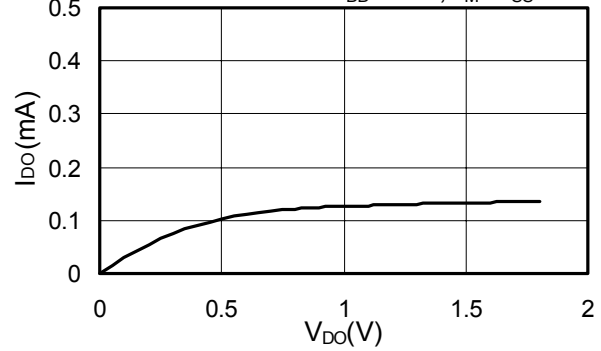
CO pin sink current characteristics

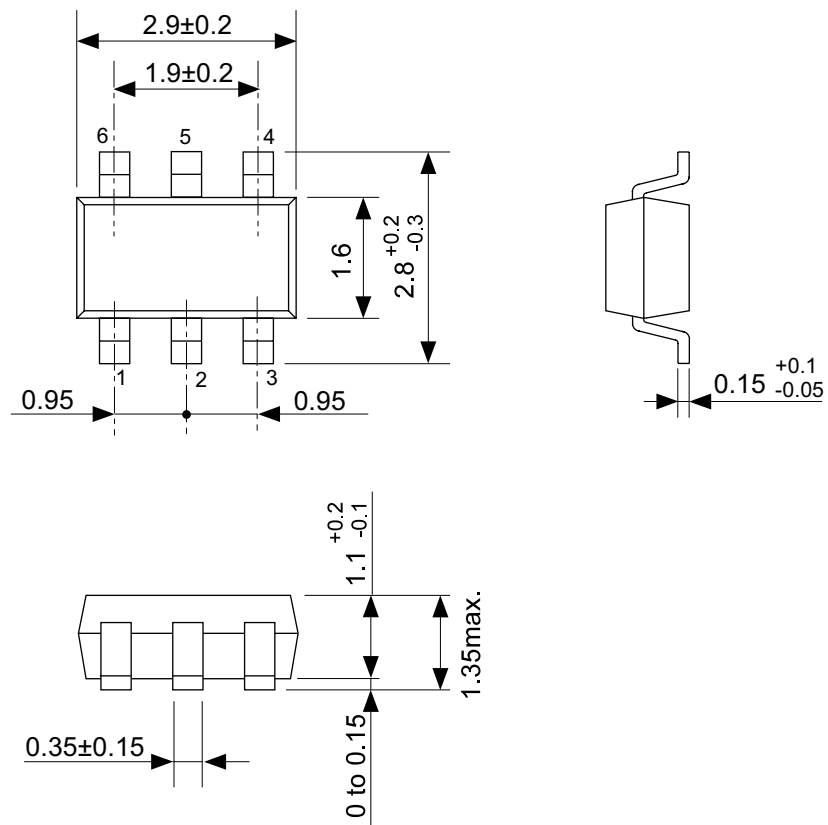
 $V_{DD}=4.5V, V_M=V_{SS}=0V$ 

DO pin source current characteristics

 $V_{DD}=3.5V, V_M=V_{SS}=0V$ 

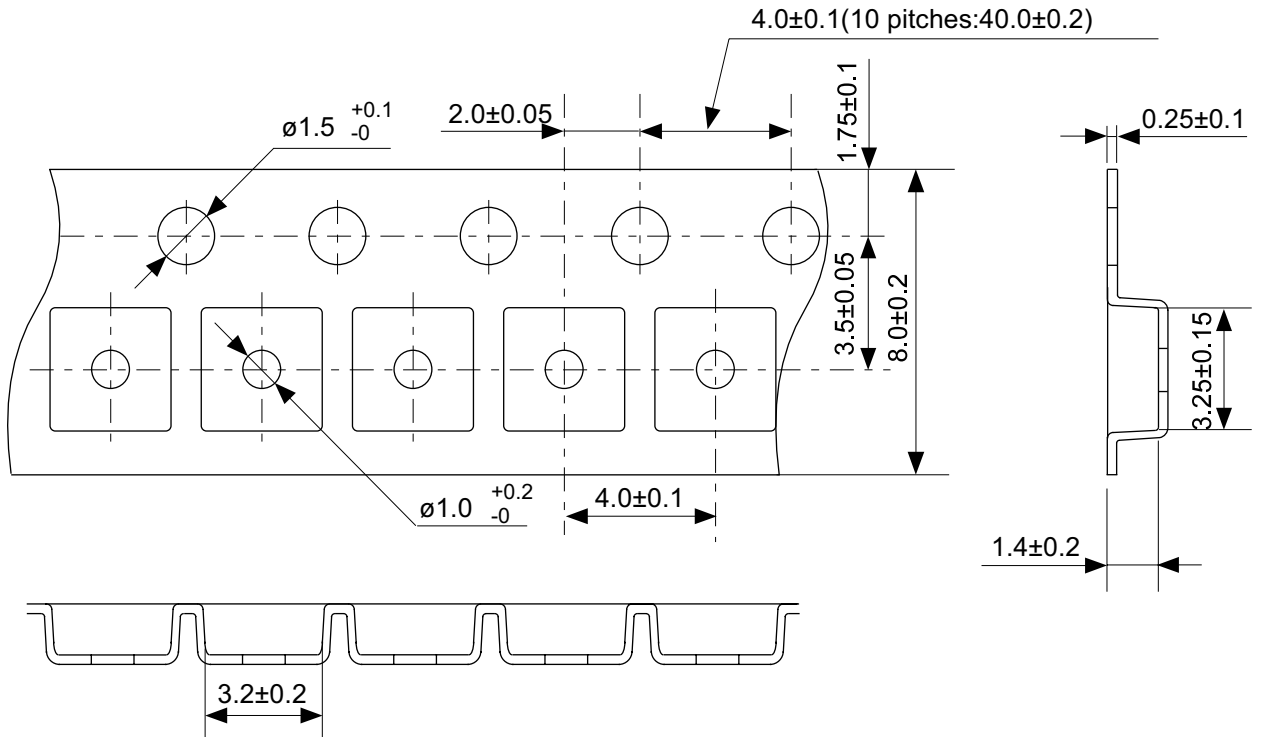
DO pin sink current characteristics

 $V_{DD}=1.8V, V_M=V_{SS}=0V$ 

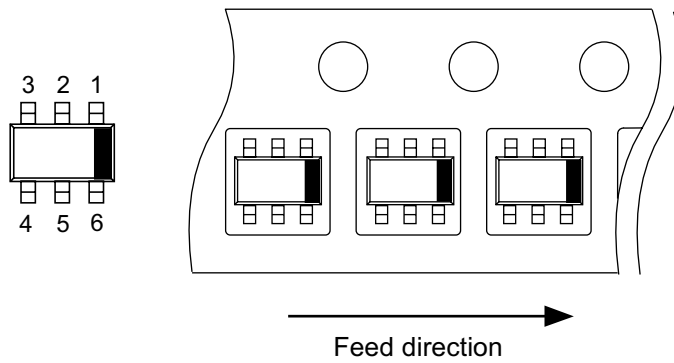


No. MP006-A-P-SD-1.1

TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instr <a href="http://www.DataSheet4U.com">www.DataSheet4U.com</a>	



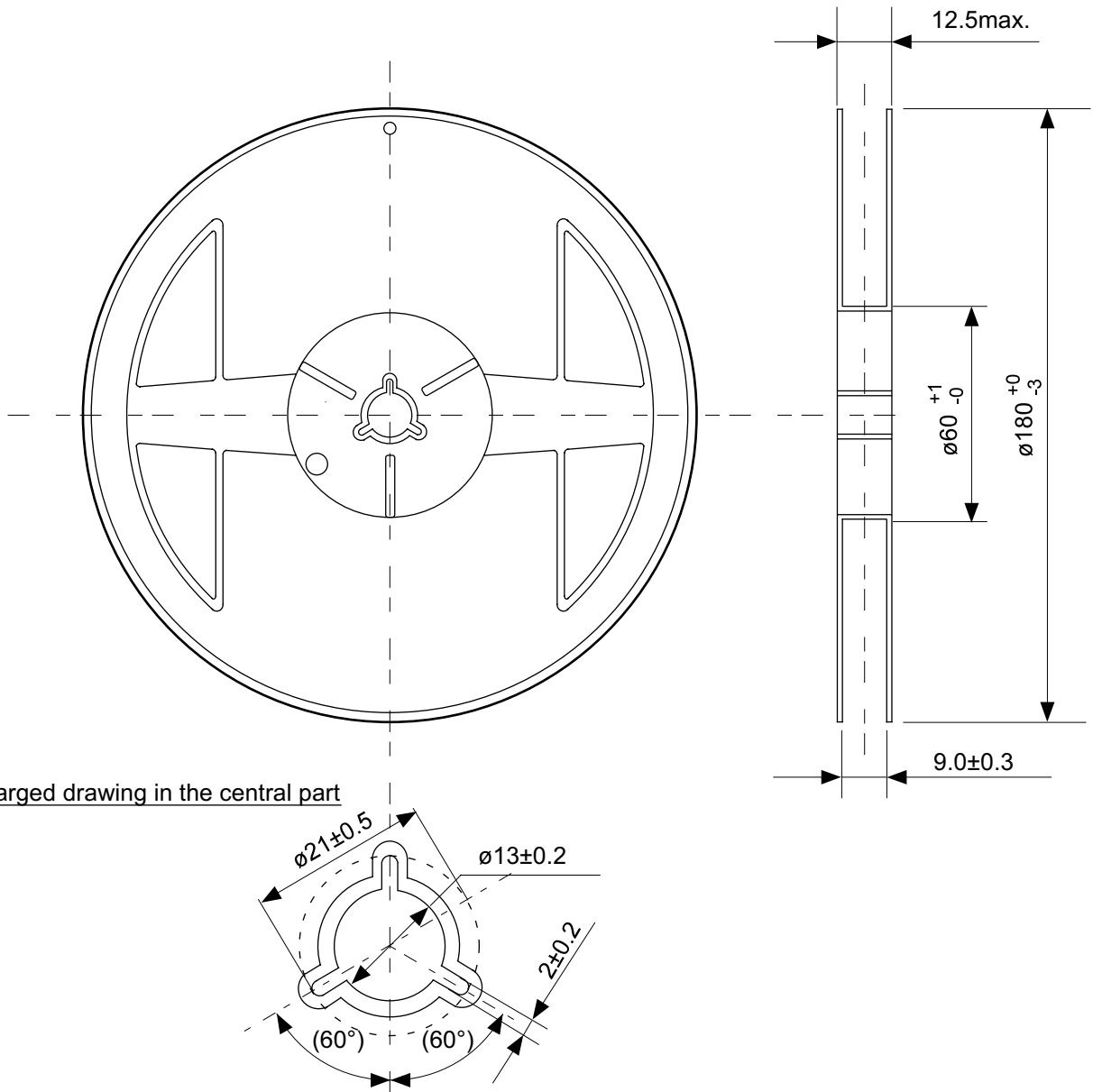
TF(T2) type



No. MP006-A-C-SD-3.1

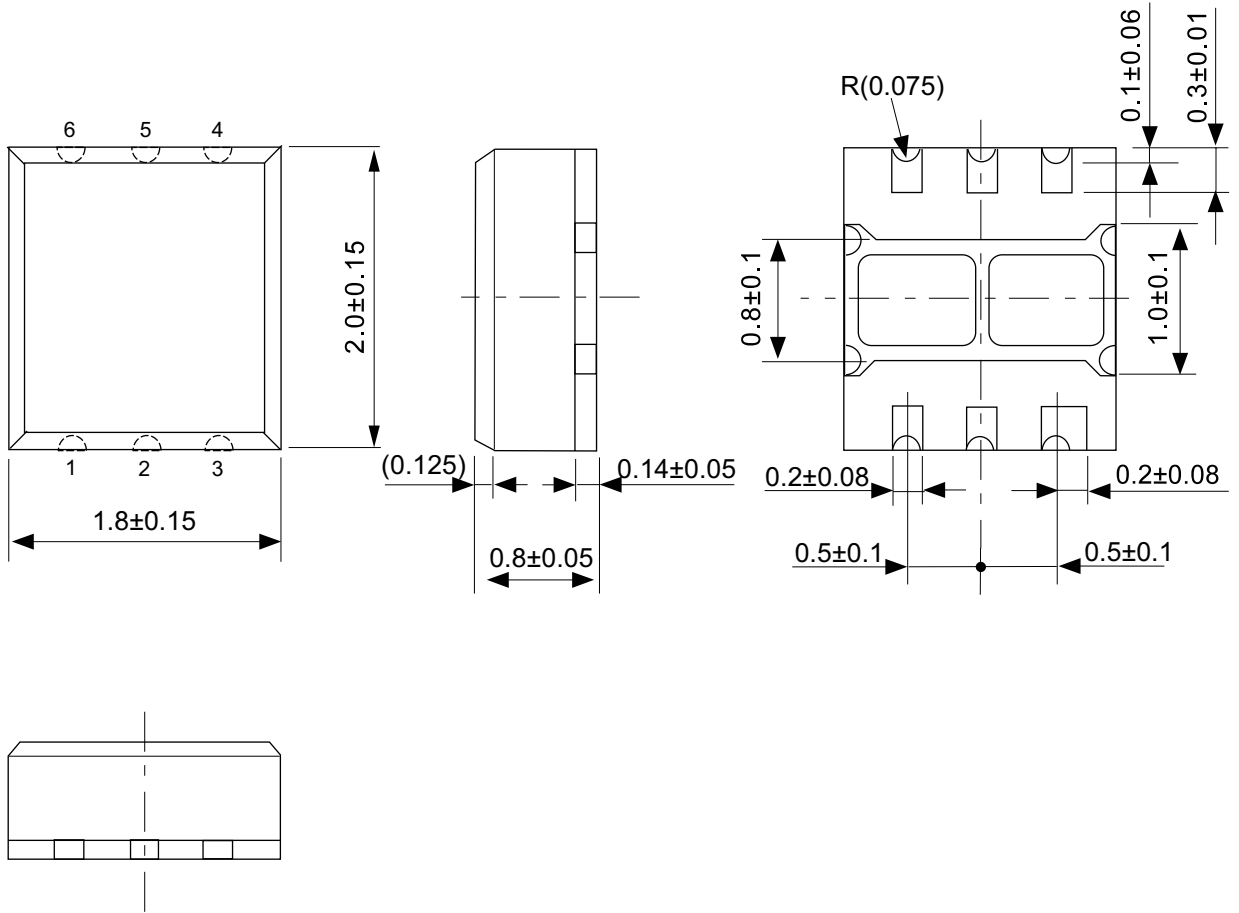
TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
SCALE	
UNIT	mm
Seiko Instruments Inc. www.DataSheet4U.com	





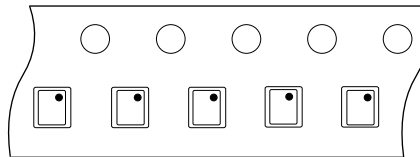
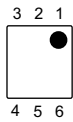
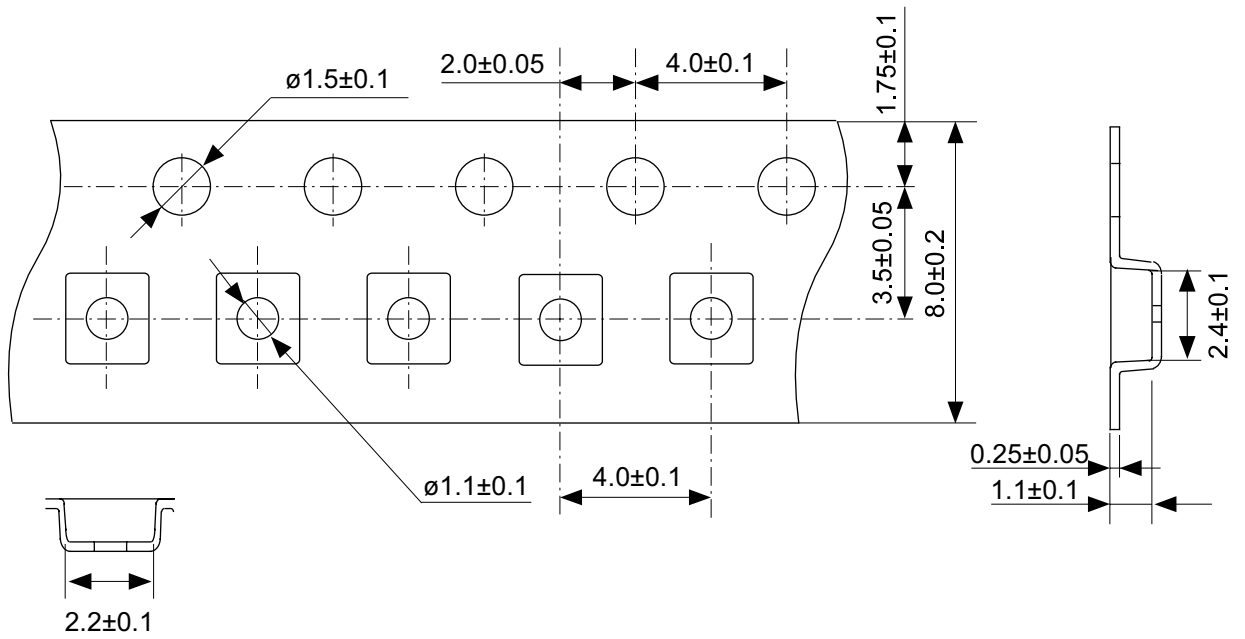
No. MP006-A-R-SD-2.1

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
SCALE		QTY	3,000
UNIT	mm		
Seiko Instruments Data Sheet			



No. BD006-A-P-SD-1.1

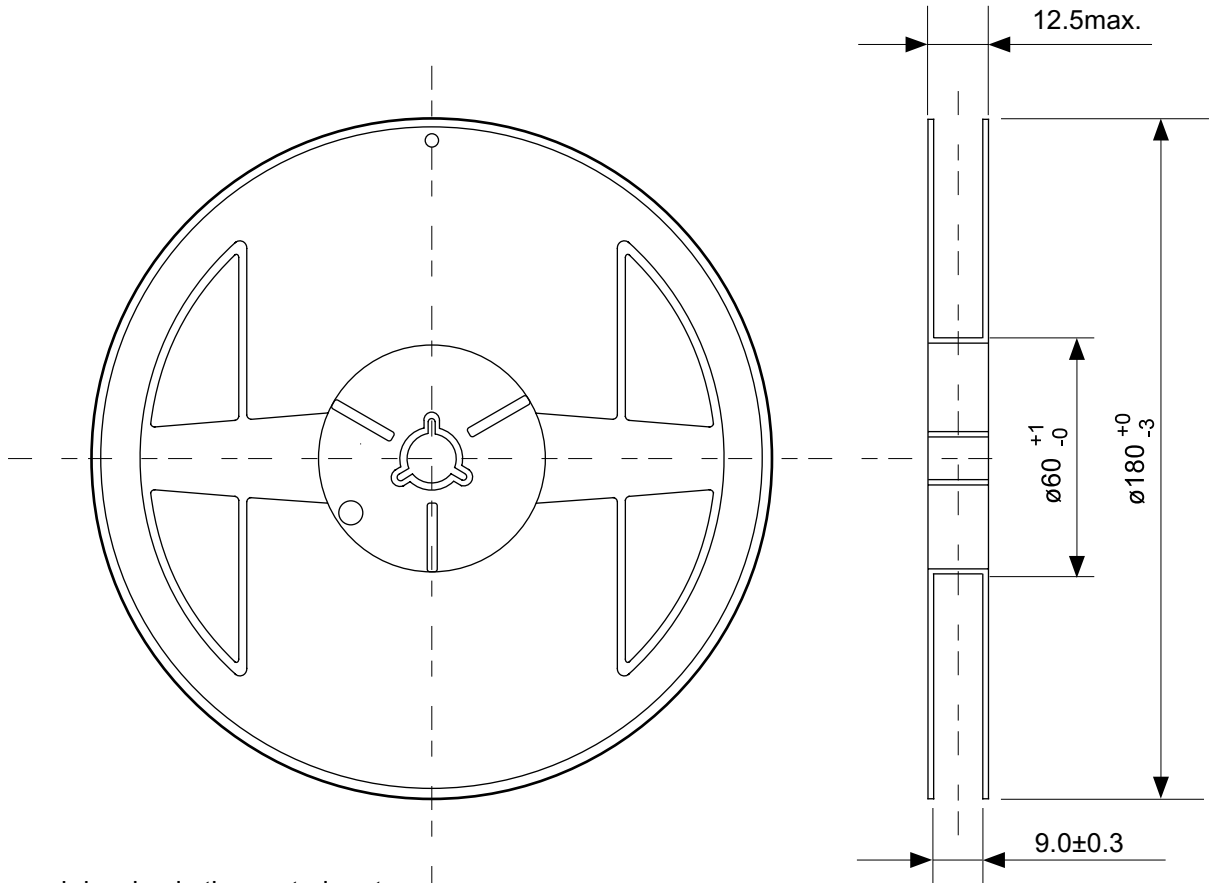
TITLE	SNB6B-A-PKG Dimensions
No.	BD006-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc. www.DataSheet4U.com	



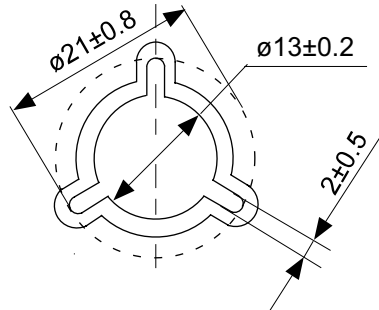
Feed direction

No. BD006-A-C-SD-2.1

TITLE	SNB6B-A-Carrier Tape
No.	BD006-A-C-SD-2.1
SCALE	
UNIT	mm



Enlarged drawing in the central part



No. BD006-A-R-SD-1.1

TITLE	SNB6B-A-Reel		
No.	BD006-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		

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