The S-8229 Series is a battery monitoring IC developed using CMOS technology. Compared with conventional CMOS voltage detectors, the S-8229 Series is ideal for the applications that require high-withstand voltage due to its maximum operation voltage as high as 24 V.
The S-8229 Series is capable of confirming the voltage in stages since it detects three voltage values.

■ Features

- Detection voltage accuracy: ±1.0%
- Hysteresis characteristics: V_{HYS1} to V_{HYS3} = 0 mV, 50 mV, 300 mV, 400 mV, 500 mV
- Current consumption: During operation: I_{DD1} = 9.0 µA max. ($-V_{DETtotal}$*1 ≥ 42 V)
  I_{DD1} = 11.0 µA max. ($-V_{DETtotal}$*1 < 42 V)
  During power-off: I_{DD2} = 0.1 µA max.
- Operation voltage range: V_{DD} = 3.6 V to 24 V
- Detection voltage: $-V_{DET1(S)}$ to $-V_{DET3(S)}$ = 10.5 V to 21.5 V (0.1 V step)
- Output form: Nch open-drain output
- Output logic*2: Full charge all on, full charge all off
- Operation temperature range: Ta = –40°C to +85°C
- Lead-free (Sn 100%), halogen-free

***1.** $-V_{DETtotal}$: Total detection voltage
$-V_{DETtotal} = -V_{DET1(S)} + -V_{DET2(S)} + -V_{DET3(S)}$

***2.** Full charge all on: When the input voltage is equal to or higher than each of the three detection voltage values, $V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{SS}$.
Full charge all off: When the input voltage is equal to or higher than each of the three detection voltage values, $V_{OUT1} = V_{OUT2} = V_{OUT3}$ = "High-Z".

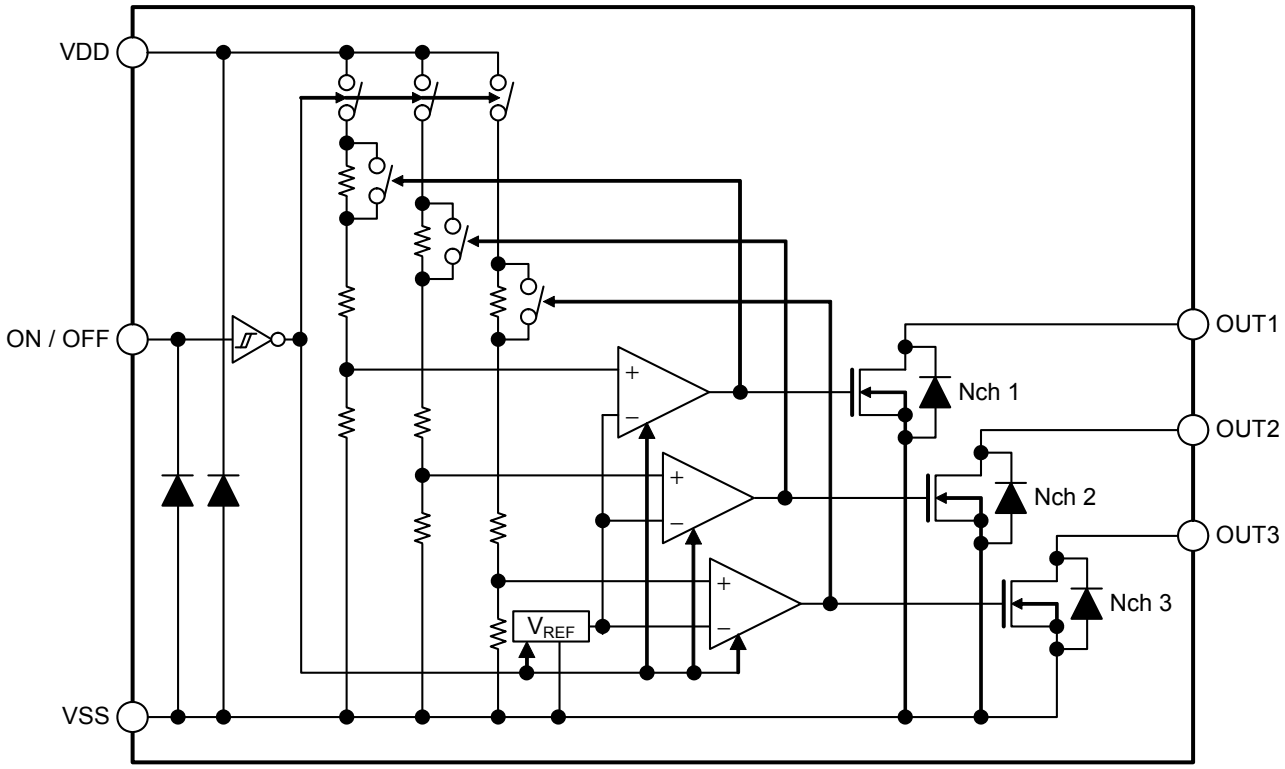
■ Application

- Rechargeable lithium-ion battery pack

■ Packages

- SOT-23-6
- SNT-6A

■ Block Diagram

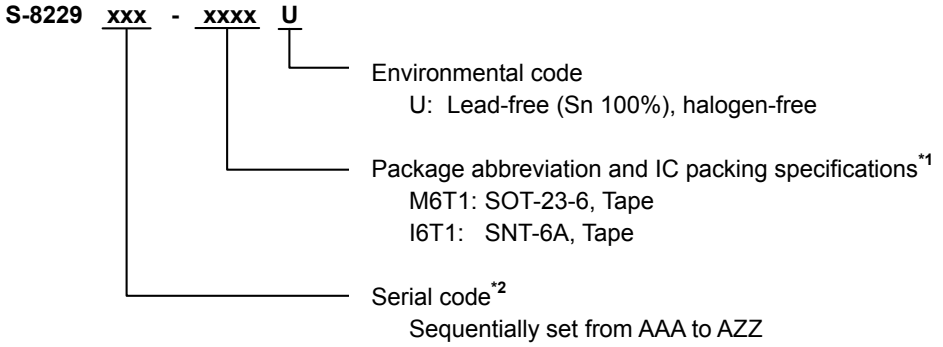


Remark Diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD	–
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product name list

3. 1 SOT-23-6

Table 2

Product Name	Detection Voltage 1 [$-V_{DET1(S)}$]	Detection Voltage 2 [$-V_{DET2(S)}$]	Detection Voltage 3 [$-V_{DET3(S)}$]	Hysteresis Width 1 [$V_{HYS1(S)}$]	Hysteresis Width 2 [$V_{HYS2(S)}$]	Hysteresis Width 3 [$V_{HYS3(S)}$]	Output Logic*1
S-8229AAA-M6T1U	19.400 V	18.100 V	15.300 V	0 V	0 V	0 V	Full charge all on
S-8229AAB-M6T1U	19.400 V	18.100 V	15.300 V	0.500 V	0.500 V	0.500 V	Full charge all on
S-8229AAC-M6T1U	19.500 V	18.000 V	15.500 V	0.050 V	0.050 V	0.050 V	Full charge all on
S-8229AAG-M6T1U	15.600 V	14.800 V	13.600 V	0.500 V	0.500 V	0.500 V	Full charge all on
S-8229AAH-M6T1U	20.000 V	18.500 V	16.000 V	0.500 V	0.500 V	0.500 V	Full charge all on
S-8229AAI-M6T1U	20.000 V	18.500 V	16.000 V	0.050 V	0.050 V	0.050 V	Full charge all on
S-8229AAJ-M6T1U	15.100 V	14.300 V	13.100 V	0.500 V	0.500 V	0.500 V	Full charge all on
S-8229AAK-M6T1U	15.600 V	14.400 V	12.400 V	0 V	0 V	0 V	Full charge all on
S-8229AAM-M6T1U	19.200V	17.900 V	12.500 V	0 V	0 V	0 V	Full charge all on

***1.** Full charge all on: When the input voltage is equal to or higher than each of the three detection voltage values, $V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{SS}$.
Full charge all off: When the input voltage is equal to or higher than each of the three detection voltage values, $V_{OUT1} = V_{OUT2} = V_{OUT3}$ = "High-Z".

Remark Please contact our sales office for products other than the above.

3. 2 SNT-6A

Table 3

Product Name	Detection Voltage 1 [$-V_{DET1(S)}$]	Detection Voltage 2 [$-V_{DET2(S)}$]	Detection Voltage 3 [$-V_{DET3(S)}$]	Hysteresis Width 1 [$V_{HYS1(S)}$]	Hysteresis Width 2 [$V_{HYS2(S)}$]	Hysteresis Width 3 [$V_{HYS3(S)}$]	Output Logic*1
S-8229AAF-I6T1U	18.000 V	15.000 V	21.500 V	0.050 V	0.050 V	0.050 V	Full charge all on

***1.** Full charge all on: When the input voltage is equal to or higher than each of the three detection voltage values, $V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{SS}$.
Full charge all off: When the input voltage is equal to or higher than each of the three detection voltage values, $V_{OUT1} = V_{OUT2} = V_{OUT3}$ = "High-Z".

Remark Please contact our sales office for products other than the above.

■ Pin Configurations

1. SOT-23-6

Top view

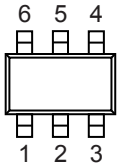


Figure 2

Table 4

Pin No.	Symbol	Description
1	OUT1	Voltage detection output pin 1
2	OUT2	Voltage detection output pin 2
3	OUT3	Voltage detection output pin 3
4	VSS	GND pin
5	VDD	Voltage input pin
6	ON / OFF	ON / OFF pin

2. SNT-6A

Top view

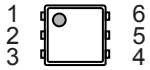


Figure 3

Table 5

Pin No.	Symbol	Description
1	OUT3	Voltage detection output pin 3
2	OUT2	Voltage detection output pin 2
3	OUT1	Voltage detection output pin 1
4	ON / OFF	ON / OFF pin
5	VDD	Voltage input pin
6	VSS	GND pin

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Input voltage		V_{DD}	V_{SS} − 0.3 to V_{SS} + 26	V
		$V_{ON / OFF}$	V_{SS} − 0.3 to V_{SS} + 26	V
Output voltage n		V_{OUTn}	V_{SS} − 0.3 to V_{SS} + 26	V
Power dissipation	SOT-23-6	P_D	650[*1]	mW
	SNT-6A		400[*1]	mW
Operation ambient temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

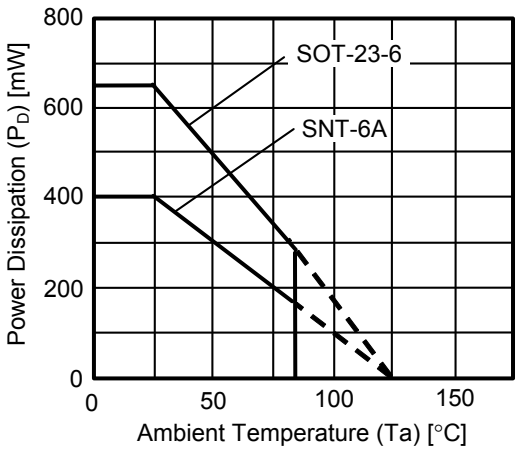


Figure 4 Power Dissipation of Package (When Mounted on Board)

Remark n = 1 to 3

■ Electrical Characteristics

Table 7

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage n*1	$-V_{DETn}$	–	$-V_{DETn(S)} \times 0.99$	$-V_{DETn(S)}$	$-V_{DETn(S)} \times 1.01$	V	1
Hysteresis width n*2	V_{HYSn}	$300\ mV \le V_{HYSn(S)} \le 500\ mV$	$-V_{HYSn(S)} \times 0.8$	$-V_{HYSn(S)}$	$-V_{HYSn(S)} \times 1.2$	V	1
		$0\ V \le V_{HYSn(S)} \le 50\ mV$	$-V_{HYSn(S)} - 0.025$	$-V_{HYSn(S)}$	$-V_{HYSn(S)} + 0.025$	V	1
ON / OFF pin input voltage "H"	V_{SH}	V1 = V3 = 22 V	1.5	–	–	V	1
ON / OFF pin input voltage "L"	V_{SL}	V1 = V3 = 22 V	–	–	0.3	V	1
Operation voltage range between VDD pin and VSS pin	V_{DD}	–	3.6	–	24	V	–
Current consumption during operation	I_{DD1}	V1 = 22 V, V2 = 3 V, $-V_{DETtotal}$*3 ≥ 42 V	–	4.0	9.0	μA	2
		V1 = 22 V, V2 = 3 V, $-V_{DETtotal}$*3 < 42 V	–	5.0	11.0	μA	2
Current consumption during power-off	I_{DD2}	V1 = 22 V, V2 = 0 V	–	–	0.1	μA	2
Output sink current n	I_{OUTn}	Full charge all on, V1 = 22 V, V2 = 3 V, V3 = 1 V	10	–	–	mA	3
		Full charge all off, V1 = 10 V, V2 = 3 V, V3 = 1 V	5	–	–	mA	3
Output leak current n	I_{LEAKn}	V1 = 22 V, V2 = 0 V, V3 = 22 V	–	–	0.1	μA	3
Detection voltage temperature coefficient*4	$\frac{\Delta -V_{DETn}}{\Delta Ta \bullet -V_{DETn}}$	Ta = –40°C to +85°C*5	–	±100	±200	ppm/°C	1

***1.** $-V_{DETn}$: Actual detection voltage value, $-V_{DETn(S)}$: Set detection voltage

***2.** V_{HYSn}: Actual hysteresis width, $-V_{HYSn(S)}$: Set hysteresis width

***3.** $-V_{DETtotal}$: Total detection voltage
$-V_{DETtotal} = -V_{DET1(S)} + -V_{DET2(S)} + -V_{DET3(S)}$

***4.** The Change in temperature of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DETn}}{\Delta Ta}\ [mV/°C]^{*1} = -V_{DETn(S)}\ (typ.)\ [V]^{*2} \times \frac{\Delta - V_{DETn}}{\Delta Ta \bullet -V_{DETn}}\ [ppm/°C]^{*3} \div 1000$$

- ***1.** Change in temperature of the detection voltage
- ***2.** Set detection voltage
- ***3.** Detection voltage temperature coefficient

***5.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

Remark n = 1 to 3

■ Test Circuits

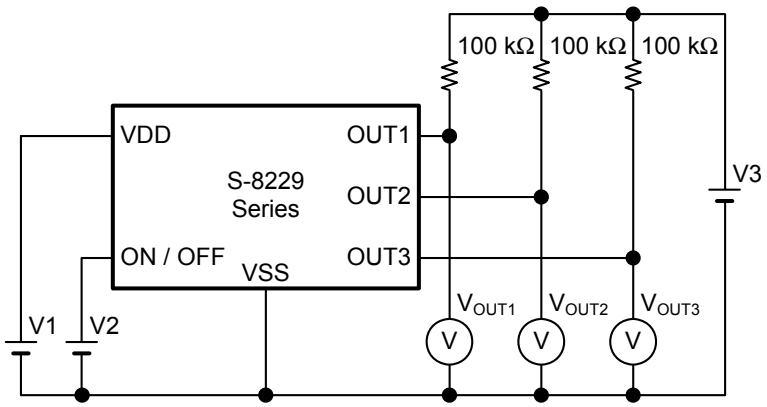


Figure 5 Test Circuit 1

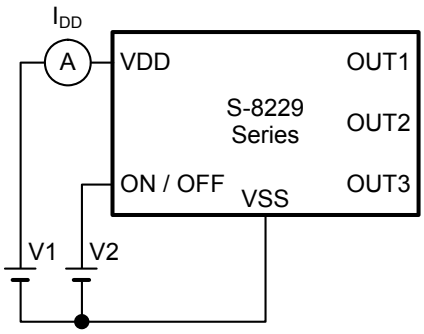


Figure 6 Test Circuit 2

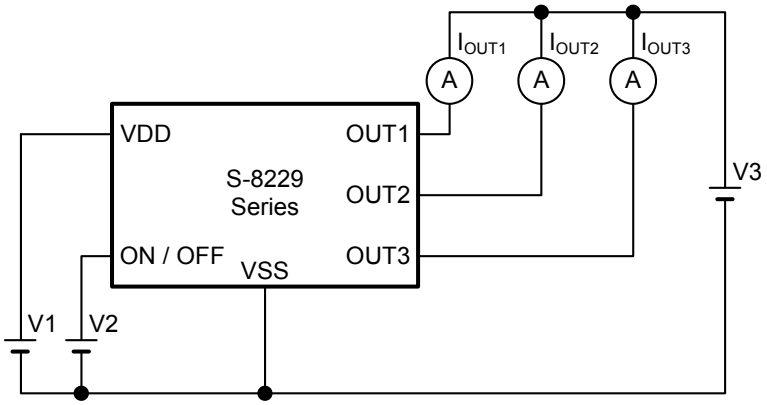


Figure 7 Test Circuit 3

■ Standard Circuit

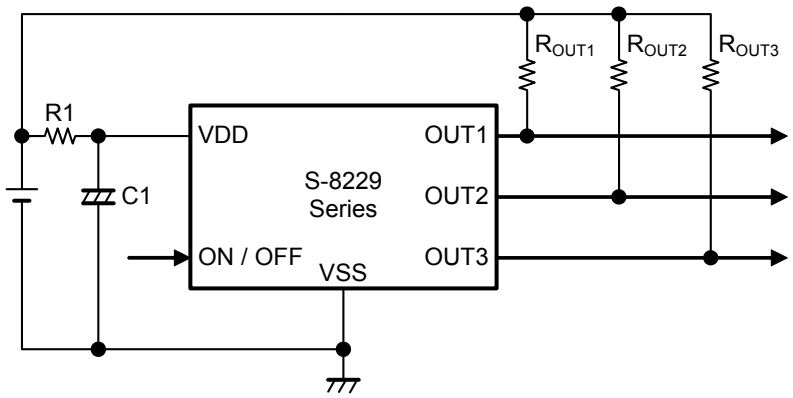


Figure 8

Table 8 Constants for External Components

Symbol	Purpose	Typ.	Remark
R1*1	For power fluctuation	470 Ω	Set the value as small as possible to prevent deterioration of the detection voltage.
C1	For power fluctuation	0.1 μF	Set R1 × C1 ≥ 40 × 10^{-6}.
R_{OUTn}*2	For output pin pull-up	100 kΩ	Make sure the power dissipation of the S-8229 Series is not exceeded.

***1.** Set up R1 as 100 kΩ or less to prevent oscillation.

***2.** Set up each of R_{OUTn} as 620 Ω or more so that the power dissipation is not exceeded.

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

Remark n = 1 to 3

■ Operation

1. Basic operation

The basic operation when $V_{ON / OFF} \geq V_{SH}$ is shown as follows.

1. 1 When the power supply voltage (V_{DD}) increases

The OUTn pin becomes release status if V_{DD} is equal to or higher than the release voltage ($+V_{DETn}$).

Table 9 Set Conditions at Releasing

Output Logic	V_{OUTn}	Nch n
Full charge all on	V_{SS}	On
Full charge all off	High-Z	Off

1. 2 When V_{DD} decreases

The OUTn pin becomes detection status if V_{DD} is equal to or lower than the detection voltage ($-V_{DETn}$).

Table 10 Set Conditions at Detecting

Output Logic	V_{OUTn}	Nch n
Full charge all on	High-Z	Off
Full charge all off	V_{SS}	On

1. 3 When $V_{DD} \leq$ minimum operation voltage

The OUTn pin voltage is indefinite.

Remark n = 1 to 3

2. ON / OFF pin

This pin starts and stops the S-8229 Series.

When $V_{ON / OFF}$ is set to V_{SL} or lower, the entire internal circuit stops operating, and Nch n (refer to **Figure 1** in "**■ Block Diagram**") is turned off, reducing current consumption significantly.
The ON / OFF pin is configured as shown in **Figure 9**. The ON / OFF pin is not internally pulled up or pulled down, so do not use the ON / OFF pin in the floating status. When not using the ON / OFF pin, connect the pin to the VDD pin.

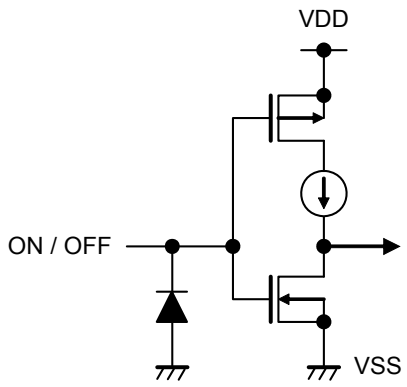


Figure 9

Remark n = 1 to 3

■ Timing Charts

1. Nch open-drain output (full charge all on, $V_{ON\,/\,OFF} \geq V_{SH}$)

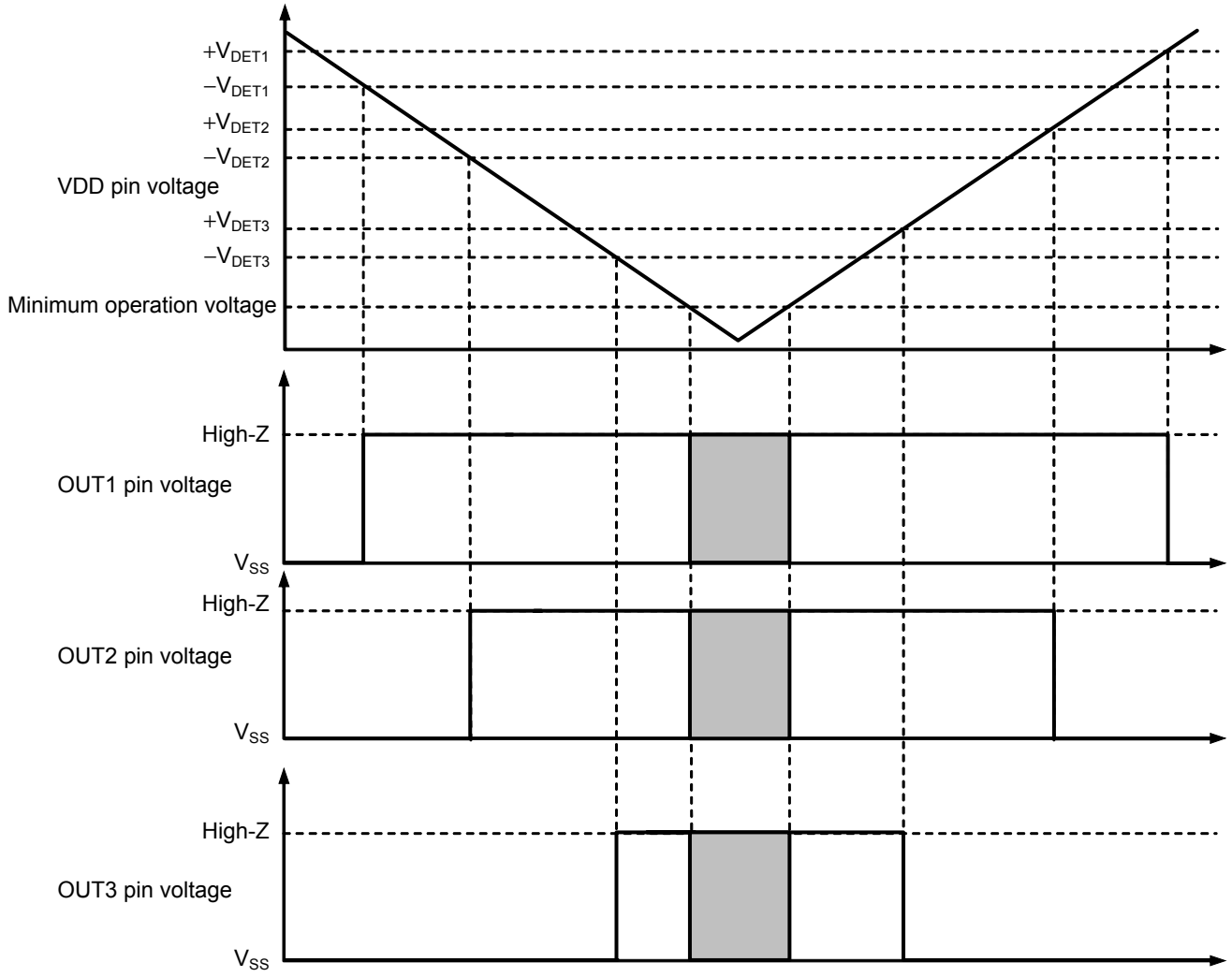


Figure 10

Remark When V_{DD} is equal to or lower than the minimum operation voltage, the output voltage from the OUT1 pin to the OUT3 pin is indefinite in the shaded area.

2. Nch open-drain output (full charge all off, $V_{ON\,/\,OFF} \geq V_{SH}$)

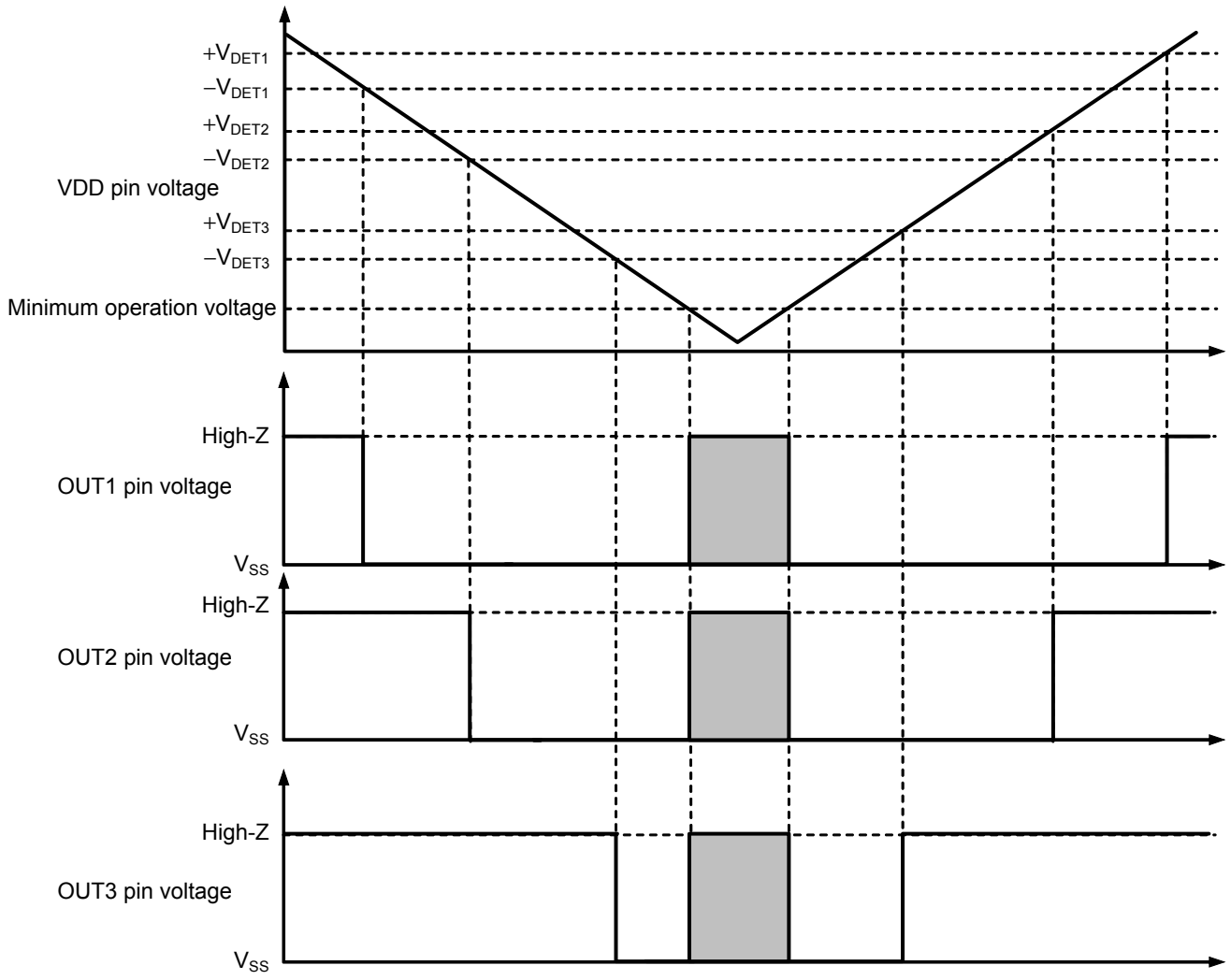


Figure 11

Remark When V_{DD} is equal to or lower than the minimum operation voltage, the output voltage from the OUT1 pin to the OUT3 pin is indefinite in the shaded area.

■ Application Circuits

1. Detection of residual quantity of the battery used by LED

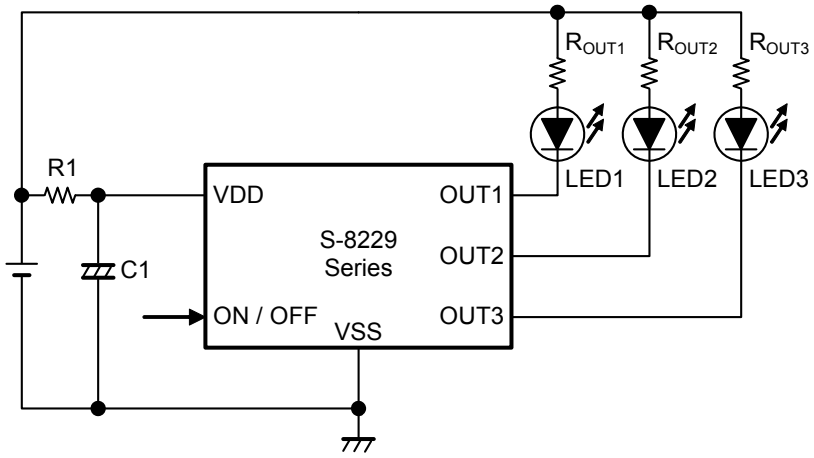


Figure 12

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

2. Change of detection voltage

When the detection voltage is changed by using a resistance divider, set $R_A \leq 100\ k\Omega$ to prevent oscillation, as shown in **Figure 13**.
The detection voltage after changing is calculated by using the following equation.

$$\text{Detection voltage} = \frac{R_A + R_B}{R_B} \times -V_{DETn} + R_A \times I_{DD}$$

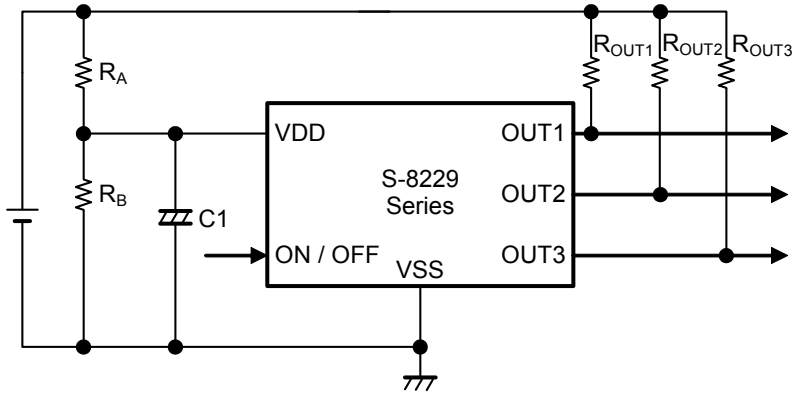


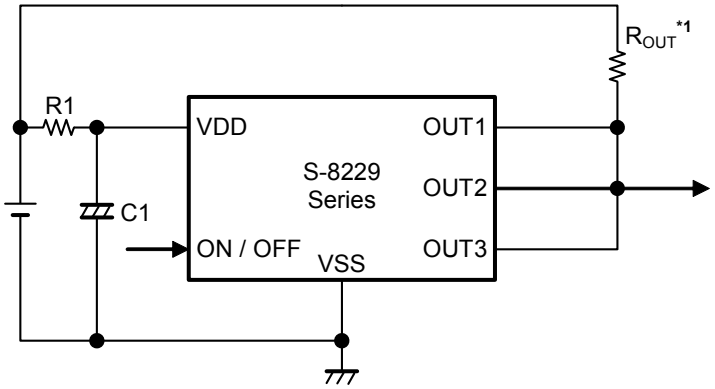
Figure 13

Caution 1. Note that the detection voltage may deviate from the value determined by the ratio of R_A and R_B in the case of the above connection diagram.
2. The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

Remark n = 1 to 3

3. Short-circuit of the output pin

In the case of $-V_{DET1(S)} = -V_{DET2(S)} = -V_{DET3(S)}$, $+V_{DET1} = +V_{DET2} = +V_{DET3}$, the load current can be increased by short-circuiting the output pin, as shown in **Figure 14.**



***1.** Set up R_{OUT} as 220 Ω or more so that the power dissipation is not exceeded.

Figure 14

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

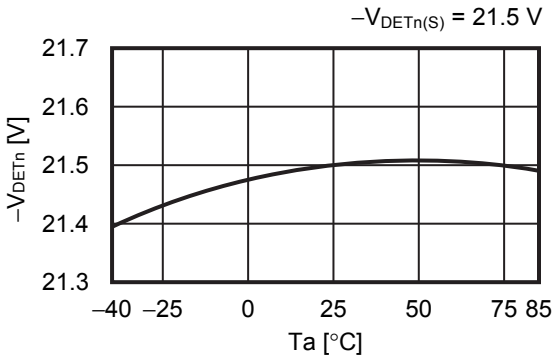
■ Precautions

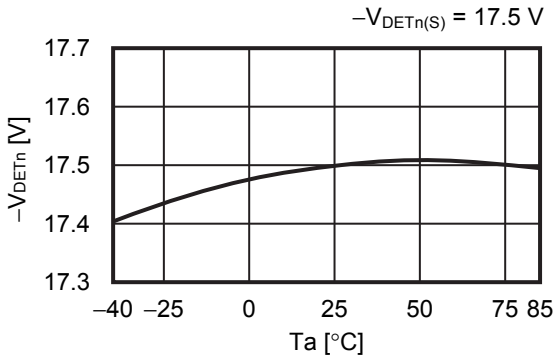
- The application conditions for the input voltage, output voltage, and output pin pull-up resistance should not exceed the package power dissipation.
- Wiring patterns for the VDD pin, the VOUT pin and the VSS pin should be designed so that the impedance is low.
- Note that the detection voltage may deviate due to the resistance component of output sink current and the VSS pin wiring.
- In applications where a resistor is connected to the input (refer to **Figure 8** in "**■ Standard Circuit**"), the feed-through current which is generated when the output switches causes a voltage drop equal to feed-through current × input resistance. In this state, the feed-through current stops and its resultant voltage drop disappears, and the output switches. The feed-through current is then generated again, a voltage drop appears. Note that an oscillation may be generated for this reason.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

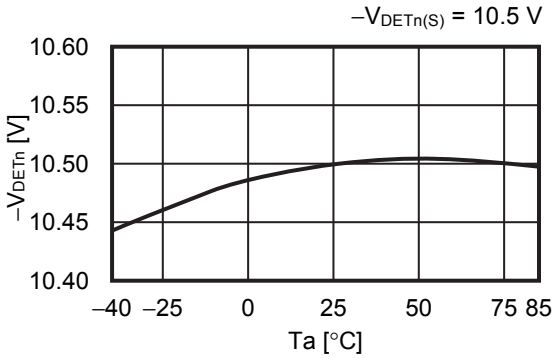
■ Characteristics (Typical Data)

1. Detection voltage

1. 1 $-V_{DETn}$ vs. Ta

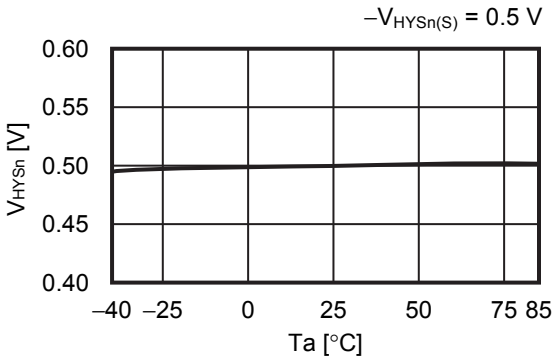


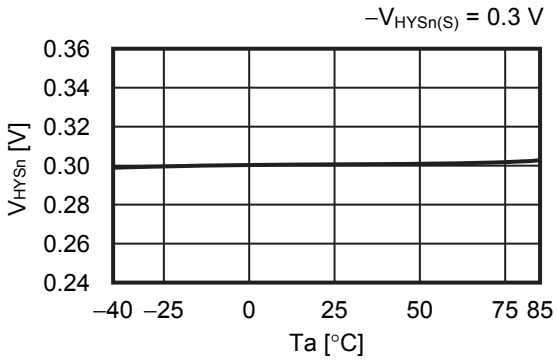


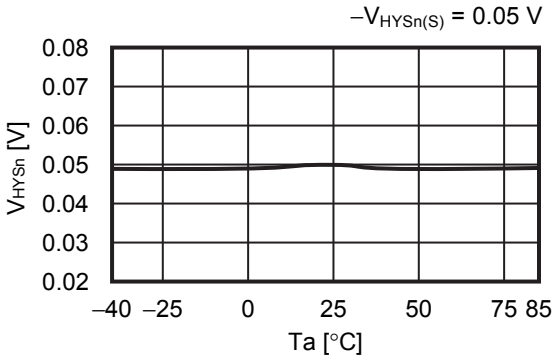


2. Hysteresis width

2. 1 $-V_{HYSn}$ vs. Ta



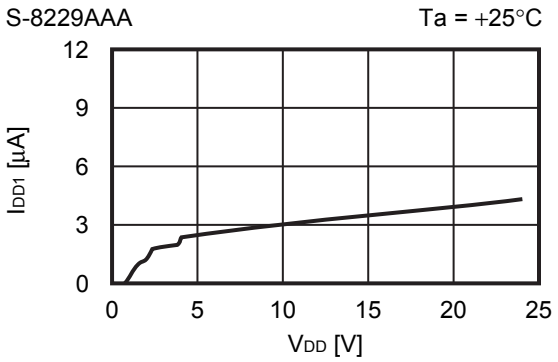




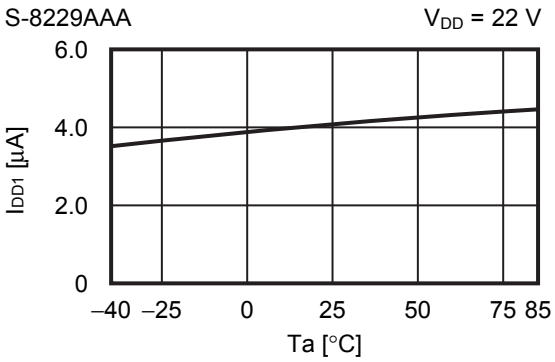
Remark n = 1 to 3

3. Current consumption

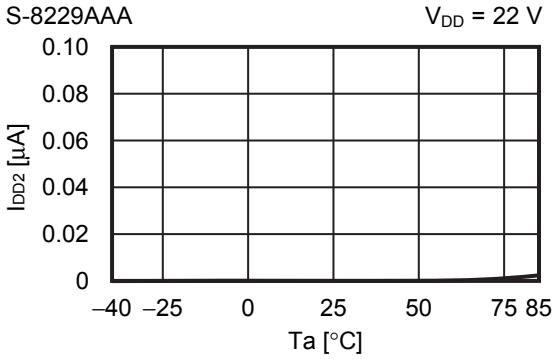
3. 1 I_{DD1} vs. V_{DD}



3. 2 I_{DD1} vs. Ta

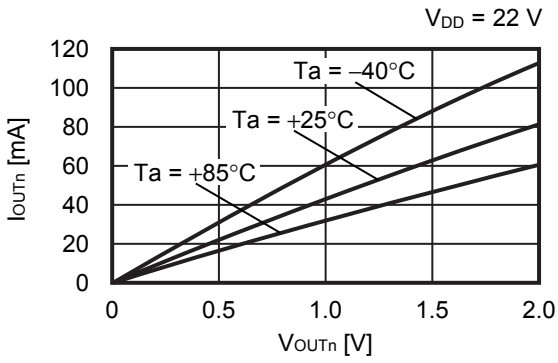


3. 3 I_{DD2} vs. Ta

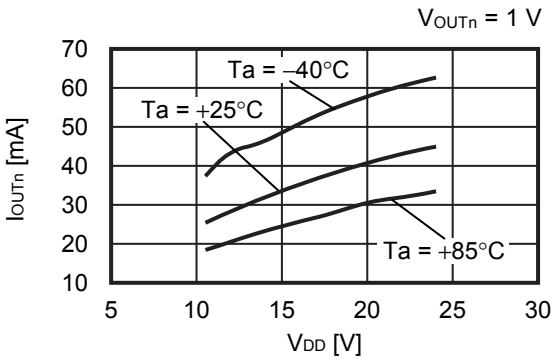


4. Output current

4. 1 I_{OUTn} vs. V_{OUTn}



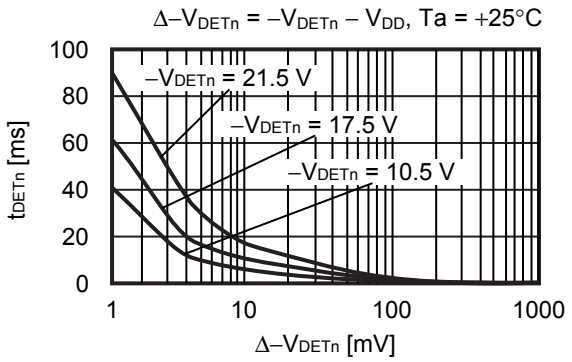
4. 2 I_{OUTn} vs. V_{DD}



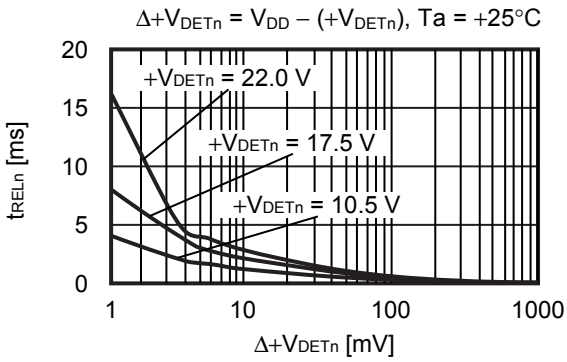
Remark n = 1 to 3

5. Response time

5. 1 t_{DETn} vs. $\Delta-V_{DETn}$



5. 2 t_{RELn} vs. $\Delta+V_{DETn}$



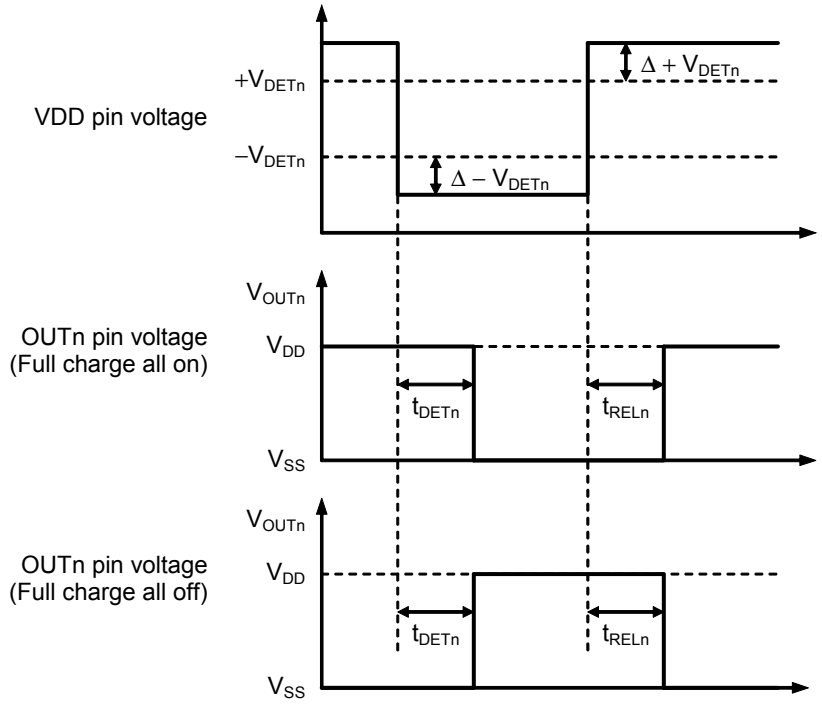


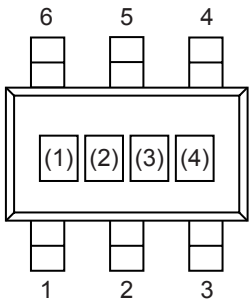
Figure 15 Test Condition of Response Time

Remark 1. Refer to "**Figure 5 Test Circuit 1**" for the test condition of the response time.
2. n = 1 to 3

■ Marking Specifications

1. SOT-23-6

Top view



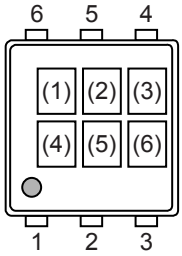
(1) to (3): Product code (Refer to **Product name vs. Product code**)
(4): Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8229AAA-M6T1U	Y	S	A
S-8229AAB-M6T1U	Y	S	B
S-8229AAC-M6T1U	Y	S	C
S-8229AAG-M6T1U	Y	S	G
S-8229AAH-M6T1U	Y	S	H
S-8229AAI-M6T1U	Y	S	I
S-8229AAJ-M6T1U	Y	S	J
S-8229AAK-M6T1U	Y	S	K
S-8229AAM-M6T1U	Y	S	M

2. SNT-6A

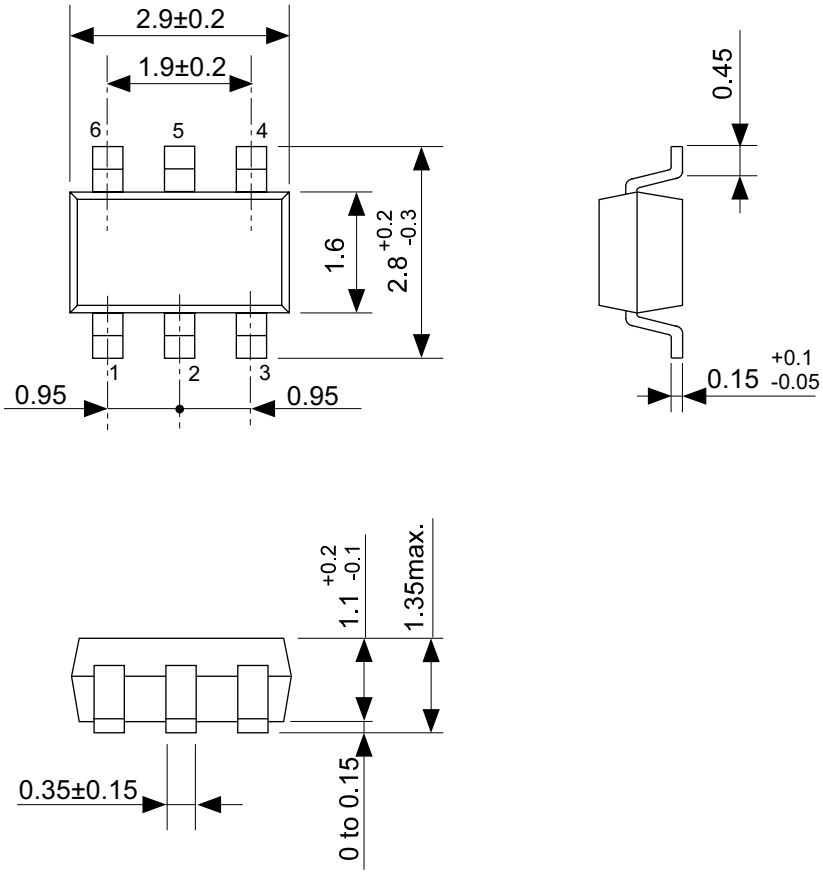
Top view



(1) to (3): Product code (Refer to **Product name vs. Product code**)
(4) to (6): Lot number

Product name vs. Product code

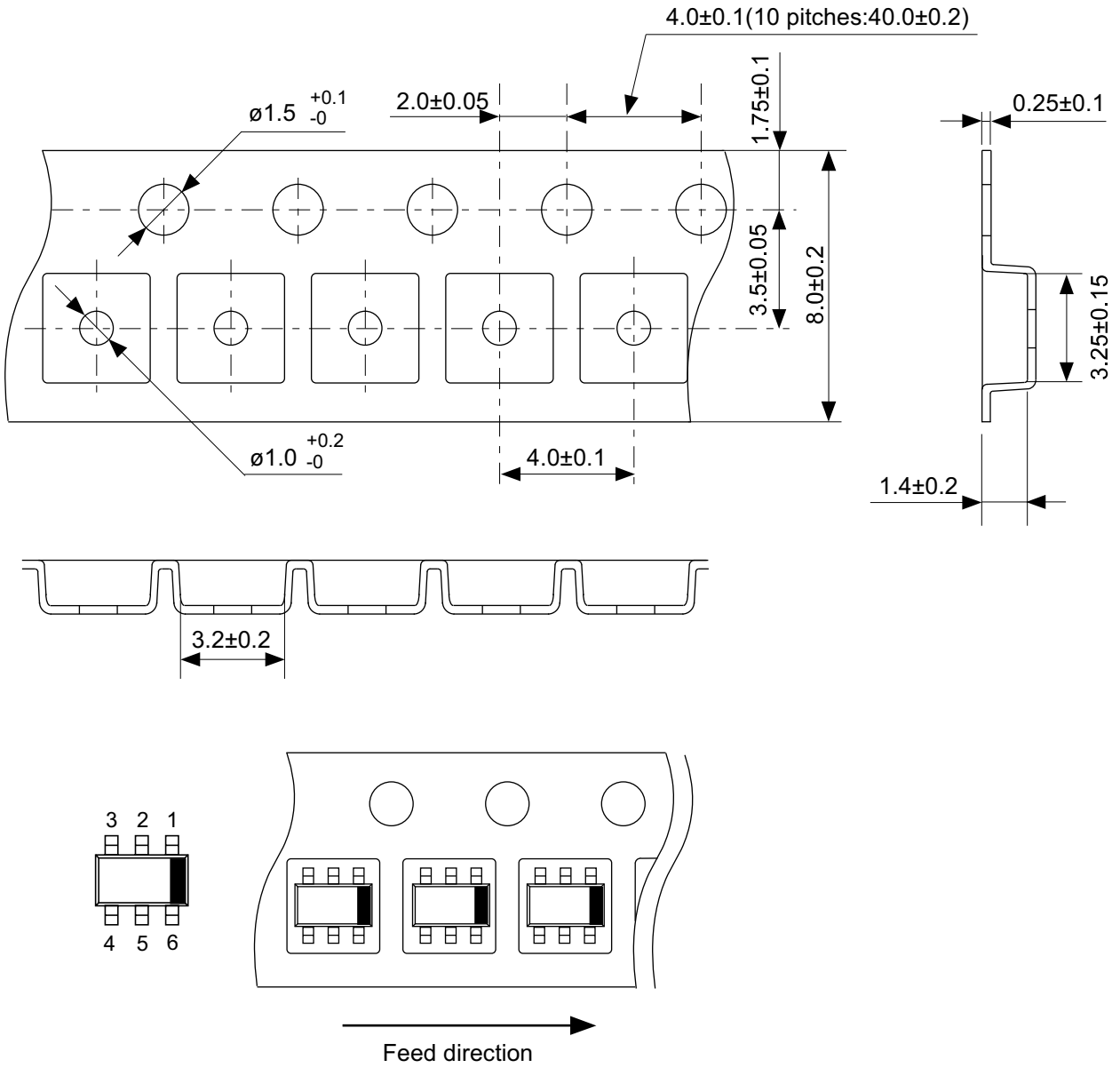
Product Name	Product Code		
	(1)	(2)	(3)
S-8229AAF-I6T1U	Y	S	F



No. MP006-A-P-SD-2.1

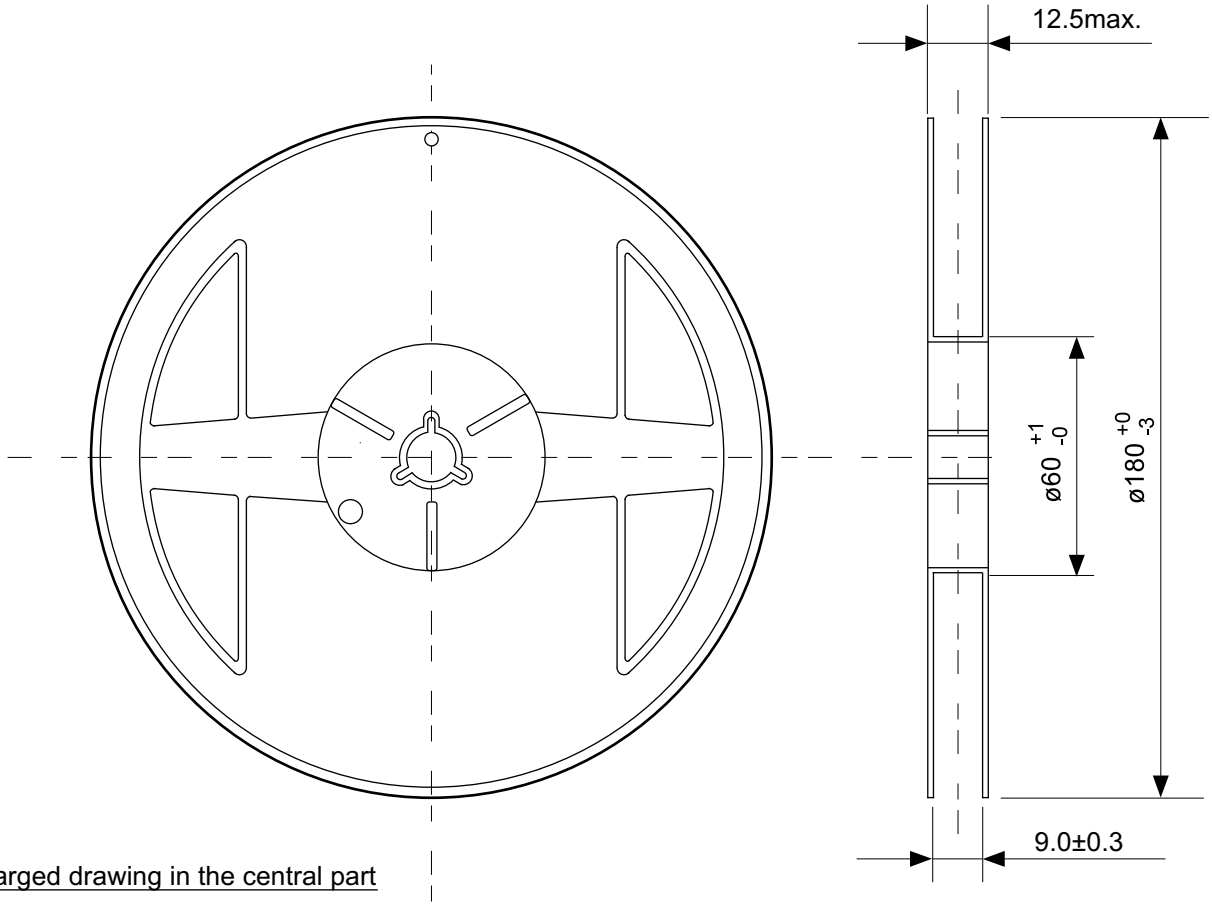
TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

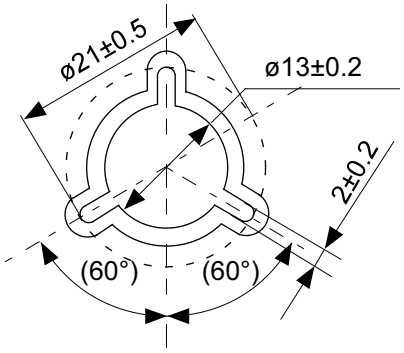


No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
ANGLE	
UNIT	mm
ABLIC Inc.	

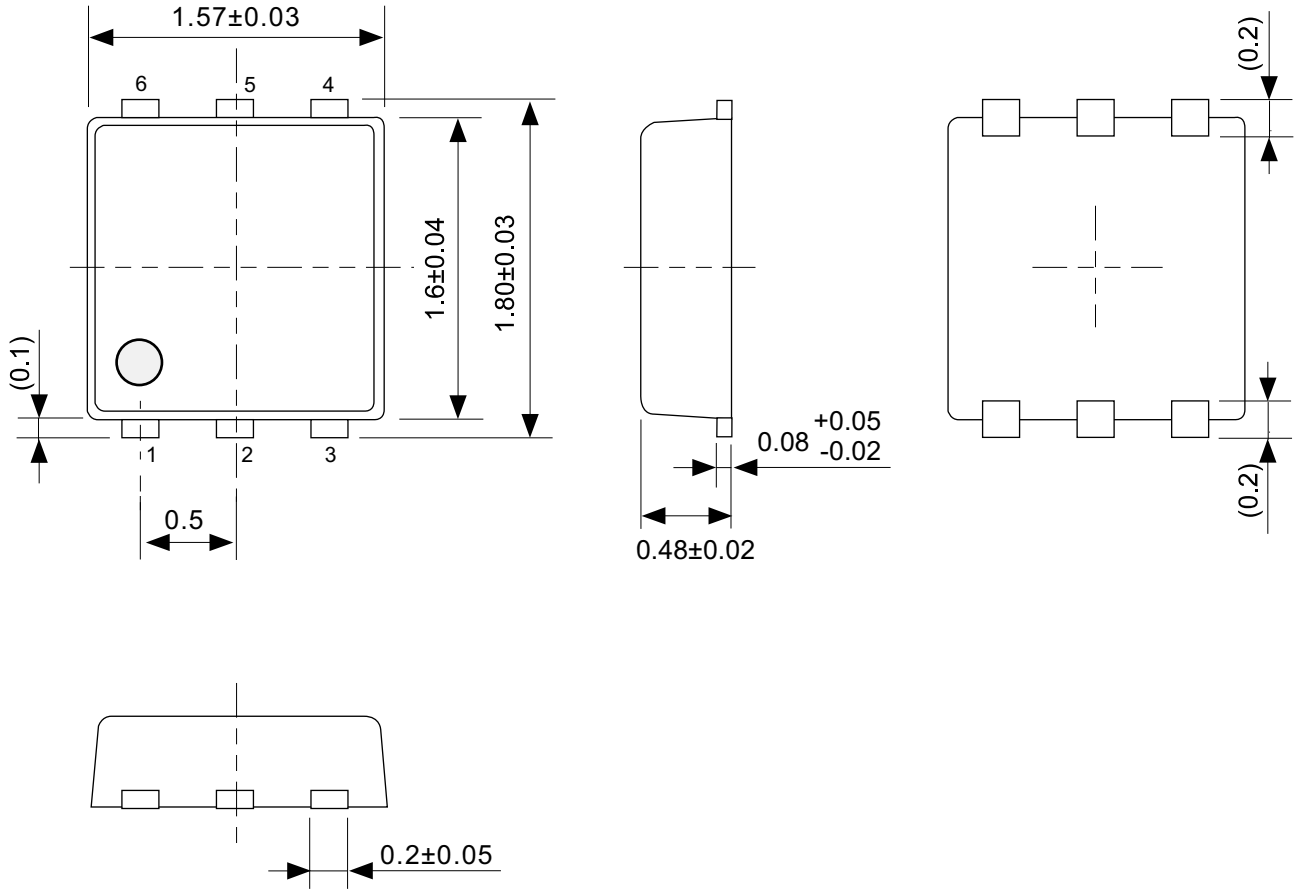


Enlarged drawing in the central part



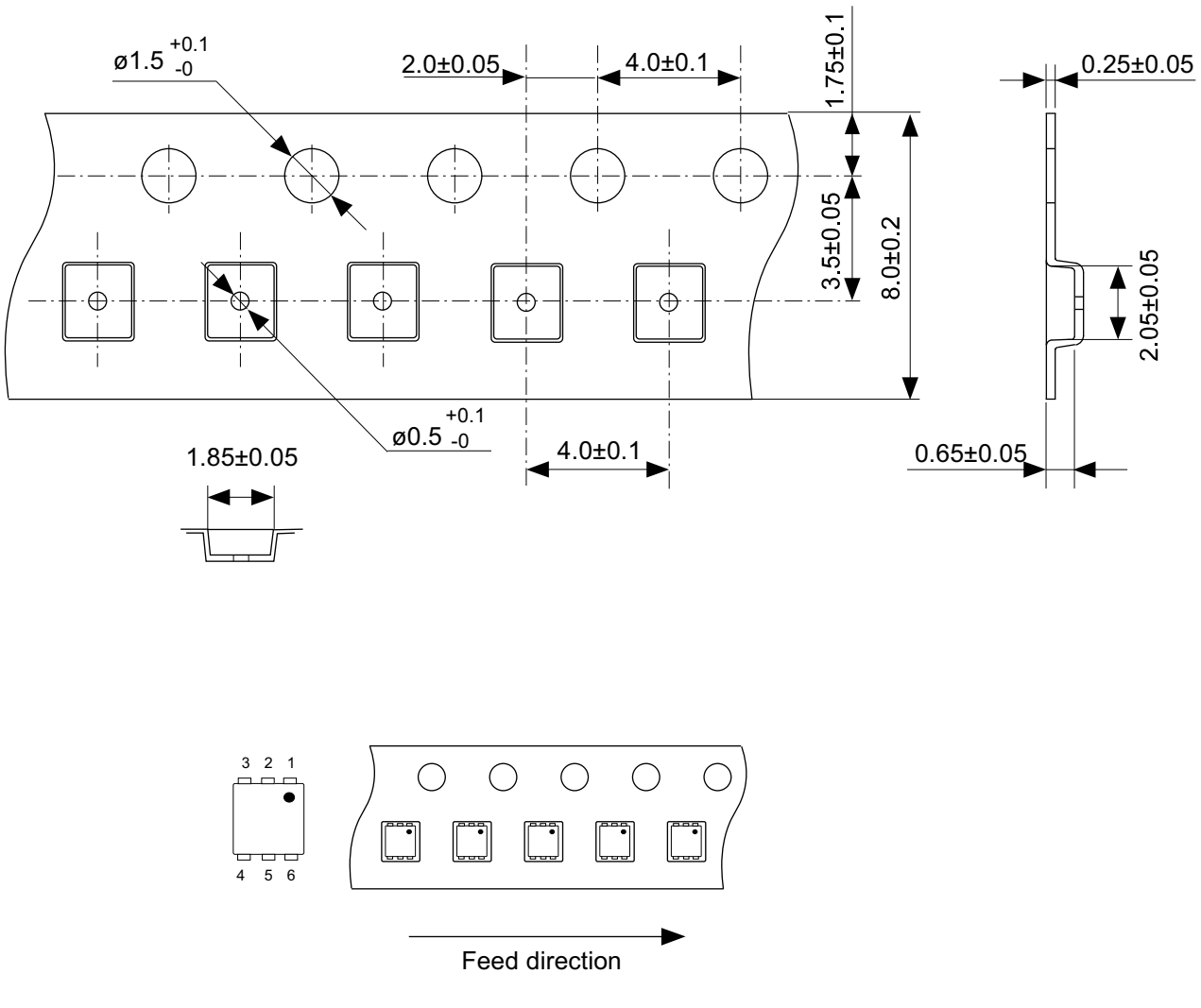
No. MP006-A-R-SD-2.1

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
ANGLE		QTY	3,000
UNIT	mm		
ABLIC Inc.			



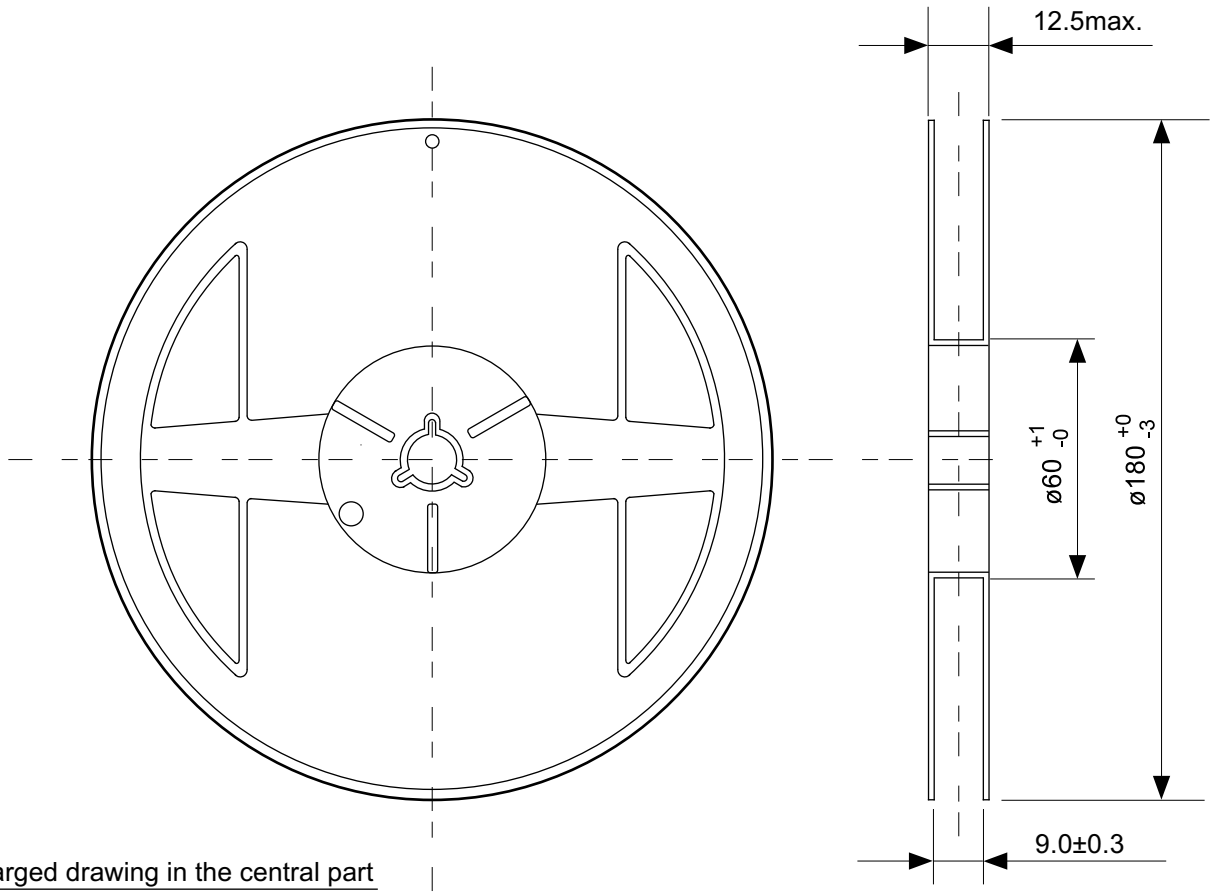
No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

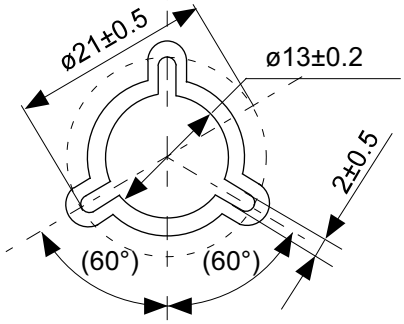


No. PG006-A-C-SD-2.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

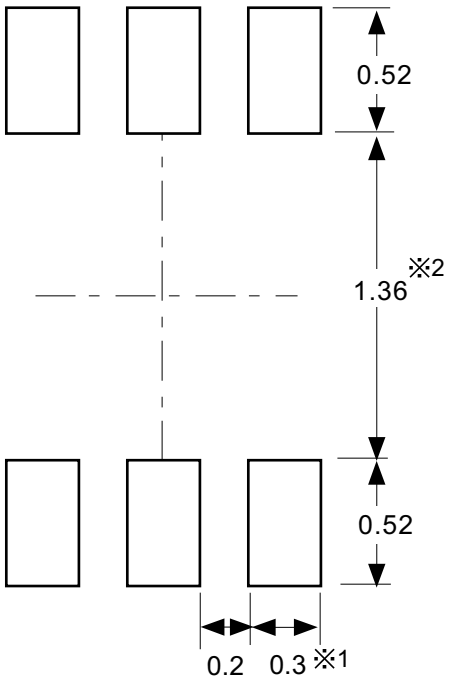


Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝**SNT**パッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.4-2019.07