BATTERY PROTECTION IC FOR 2-SERIAL-CELL PACK

S-8242 Series

The S-8242 Series are protection ICs for 2-serial-cell lithium-ion/lithium-polymer rechargeable batteries and include high-accuracy voltage detectors and delay circuits.
These ICs are suitable for protecting 2-cell rechargeable lithium-ion/lithium-polymer battery packs from overcharge, overdischarge, and overcurrent.

■ Features

(1) High-accuracy voltage detection for each cell

- Overcharge detection voltage n (n = 1, 2) 3.9 V to 4.4 V (50 mV steps) Accuracy ±25 mV
- Overcharge release voltage n (n = 1, 2) 3.8 V to 4.4 V[*1] Accuracy ±50 mV

  ***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage

  (Overcharge hysteresis voltage n (n = 1, 2) can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV steps.)

- Overdischarge detection voltage n (n = 1, 2) 2.0 V to 3.0 V (100 mV steps) Accuracy ±50 mV
- Overdischarge release voltage n (n = 1, 2) 2.0 V to 3.4 V[*2] Accuracy ±100 mV

  ***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage

  (Overdischarge hysteresis voltage n (n = 1, 2) can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV steps.)

(2) Two-level overcurrent detection (overcurrent 1, overcurrent 2)

- Overcurrent detection voltage 1 0.05 V to 0.30 V (50 mV steps) Accuracy ±15 mV
- Overcurrent detection voltage 2 1.2 V (fixed) Accuracy ±300 mV

(3) Delay times (overcharge, overdischarge, overcurrent) are generated by an internal circuit (external capacitors are unnecessary).

(4) 0 V battery charge function available/unavailable are selectable.

(5) Charger detection function and abnormal charge current detection function

- The overdischarge hysteresis is released by detecting negative voltage at the VM pin (−0.7 V typ.). (Charger detection function)
- When the output voltage of the DO pin is high and the voltage at the VM pin is equal to or lower than the charger detection voltage (−0.7 V typ.), the output voltage of the CO pin goes low. (Abnormal charge current detection function)

(6) High-withstanding-voltage devices Absolute maximum rating: 28 V

(7) Wide operating temperature range −40°C to +85 °C

(8) Low current consumption

- Operation mode 10 μA max. (+25°C)
- Power-down mode 0.1 μA max. (+25°C)

(9) Small package SOT-23-6W, 6-Pin SNB(B)

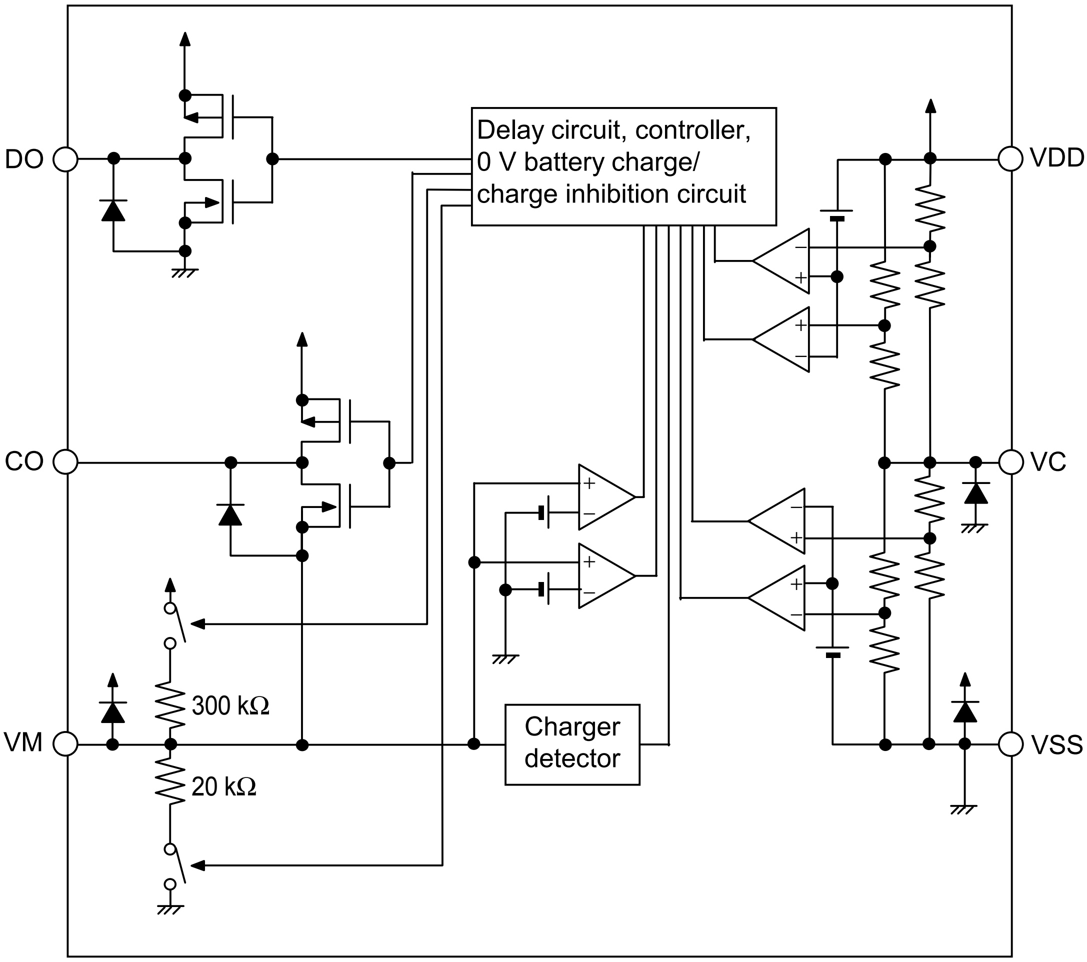
■ Applications

- Lithium-ion rechargeable battery packs
- Lithium-polymer rechargeable battery packs

■ Package

- SOT-23-6W (PKG drawing code: MP006-B)
- 6-Pin SNB(B) (PKG drawing code: BD006-A)

■ Block Diagram



Remark The diodes in the block diagram are parasitic diodes.

Figure 1 Block Diagram

■ Product Name Structure

1. Product Name

S−8242A **xx** − **XXXX**

Indicates package type and packing specification of IC [*1]
M6T2: SOT-23-6W, tape product
B6T1: 6-pin SNB(B), tape product

Additional number
Sequentially set from AA to ZZ

***1.** Refer to the taping drawing.

2. Product Name List

Table 1

Product Name/Parameter	Overcharge Detection Voltage V_{CU}	Overcharge Release Voltage V_{CL}	Overdischarge Detection Voltage V_{DL}	Overdischarge Release Voltage V_{DU}	Overcurrent Detection Voltage 1 V_{IOV1}	0 V Battery Charge
S-8242AAA-M6T2	4.325 V	4.075 V	2.200 V	2.900 V	0.210 V	Unavailable
S-8242AAA-B6T1	4.325 V	4.075 V	2.200 V	2.900 V	0.210 V	Unavailable

Remark If a product with the required detection voltage does not appear in the above list, contact our sales office.

■ Pin Assignment

SOT-23-6W
Top view

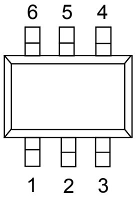


Figure 2

Table 2

Pin No.	Pin Name	Function
1	DO	Connection of discharge control FET gate (CMOS output)
2	CO	Connection of charge control FET gate (CMOS output)
3	VM	Voltage detection between VM and VSS (overcurrent/charger detection pin)
4	VC	Connection for negative voltage of battery 1 and positive voltage of battery 2
5	VDD	Connection for positive power supply input and positive voltage of battery 1
6	VSS	Connection for negative power supply input and negative voltage of battery 2

Remark For the external views, refer to the package drawings.

6-Pin SNB(B)
Top view

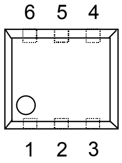


Figure 3

Table 3

Pin No.	Pin Name	Function
1	VM	Voltage detection between VM and VSS (overcurrent/charger detection pin)
2	CO	Connection of charge control FET gate (CMOS output)
3	DO	Connection of discharge control FET gate (CMOS output)
4	VSS	Connection for negative power supply input and negative voltage of battery 2
5	VC	Connection for negative voltage of battery 1 and positive voltage of battery 2
6	VDD	Connection for positive power supply input and positive voltage of battery 1

Remark For the external views, refer to the package drawings.

■ Absolute Maximum Ratings

Table 4

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Applicable Pins	Absolute Maximum Rating		Unit
Input voltage between VDD and VSS[*1]	V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 12		V
VC input pin voltage	V_{VC}	VC	V_{SS} − 0.3 to V_{DD}+ 0.3		
VM pin input voltage	V_{VM}	VM	V_{DD} − 28 to V_{DD} + 0.3		
DO pin output voltage	V_{DO}	DO	V_{SS} − 0.3 to V_{DD} + 0.3		
CO pin output voltage	V_{CO}	CO	V_{VM} − 0.3 to V_{DD} + 0.3		
Power dissipation	P_D	—	SOT-23-6W	300	mW
		—	6-Pin SNB(B)	90	
Operating temperature range	Topr	—	−40 to +85		°C
Storage temperature range	Tstg	—	−55 to +125		

***1.** Even pulse (μs) noise exceeding the above input voltage (V_{SS} + 12 V) may damage the IC, so do not allow such noise to be applied.

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Electrical Characteristics

Table 5 (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Conditions	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage n	V_{CUn}	3.90 to 4.40 V, adjustable	V_{CUn} – 0.025	V_{CUn}	V_{CUn} + 0.025	V	1	1
Overcharge release voltage n	V_{CLn}	3.80 to 4.40 V, adjustable	V_{CLn} – 0.05	V_{CLn}	V_{CLn} + 0.05	V	1	1
Overdischarge detection voltage n	V_{DLn}	2.0 to 3.0 V, adjustable	V_{DLn} – 0.05	V_{DLn}	V_{DLn} + 0.05	V	2	1
Overdischarge release voltage n	V_{DUn}	2.0 to 3.40 V, adjustable	V_{DUn} – 0.10	V_{DUn}	V_{DUn} + 0.10	V	2	1
Overcurrent detection voltage 1	V_{IOV1}	0.05 to 0.3 V, adjustable	V_{IOV1} – 0.015	V_{IOV1}	V_{IOV1} + 0.015	V	3	1
Overcurrent detection voltage 2	V_{IOV2}	—	0.9	1.2	1.5	V	3	1
Charger detection voltage	V_{CHA}	—	–1.0	–0.7	–0.4	V	4	1
Temperature coefficient 1	T_{COE1}	Ta = 0 to 50°C*1	–1.0	0	1.0	mV/°C	—	—
Temperature coefficient 2	T_{COE2}	Ta = 0 to 50°C*2	–0.5	0	0.5	mV/°C	—	—
DELAY TIME								
Overcharge detection delay time	t_{CU}	—	0.92	1.15	1.38	s	9	1
Overdischarge detection delay time	t_{DL}	—	115	144	173	ms	9	1
Overcurrent detection delay time 1	t_{IOV1}	—	7.2	9	11	ms	10	1
Overcurrent detection delay time 2	t_{IOV2}	FET gate capacitance = 2000 pF	220	300	380	μs	10	1
0 V BATTERY CHARGE FUNCTION								
0 V charge starting charger voltage	V_{0CHA}	0 V charge available	1.2	—	—	V	11	1
0 V battery charge inhibition battery voltage	V_{0INH}	0 V charge unavailable	—	—	0.5	V	12	1
INTERNAL RESISTANCE								
Resistance between VM and VDD	R_{VMD}	V1 = V2 = 1.5 V V_{VM} = 0 V	100	300	900	kΩ	6	2
Resistance between VM and VSS	R_{VMS}	V1 = V2 = 3.5 V V_{VM} = 1.0 V	5	10	20	kΩ	6	2
INPUT VOLTAGE								
Operating voltage between VDD and VSS	V_{DSOP1}	Internal circuit operating voltage	1.5	—	10	V	–	–
Operating voltage between VDD and VM	V_{DSOP2}	Internal circuit operating voltage	1.5	—	28	V	–	–
INPUT CURRENT								
Current consumption during operation	I_{OPE}	V1 = V2 = 3.5 V, V_{VM} = 0 V	—	5	10	μA	5	2
Current consumption at power down	I_{PDN}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	—	—	0.1	μA	5	2
VC pin current	I_{VC}	V1 = V2 = 3.5 V, V_{VM} = 0 V	–0.3	0	0.3	μA	5	2
OUTPUT RESISTANCE								
CO pin H resistance	R_{COH}	$V_{CO} = V_{DD} - 0.5$ V	2	4	8	kΩ	7	3
CO pin L resistance	R_{COL}	$V_{CO} = V_{VM} + 0.5$ V	2	4	8	kΩ	7	3
DO pin H resistance	R_{DOH}	$V_{DO} = V_{DD} - 0.5$ V	2	4	8	kΩ	8	3
DO pin L resistance	R_{DOL}	$V_{DO} = V_{SS} + 0.5$ V	2	4	8	kΩ	8	3

***1.** Voltage temperature coefficient 1: Overcharge detection voltage

***2.** Voltage temperature coefficient 2: Overcurrent detection voltage 1

■ Test Circuits

Remark Unless otherwise specified, the output voltage levels “H” and “L” at CO and DO pins are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.

1. Overcharge detection voltage, overcharge release voltage

(Test Condition 1, Test Circuit 1)

Overcharge detection voltage 1 (V_{CU1}) is defined as the voltage between the VDD and VC pins at which V_{CO} goes from “H” to “L” when the voltage V1 is gradually increased from the starting condition of V1 = V2 = 3.5 V, V3 = 0 V. Overcharge release voltage 1 (V_{CL1}) is defined as the voltage between the VDD and VC pins at which V_{CO} goes from “L” to “H” when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage 1 (V_{HC1}) is defined as the difference between overcharge detection voltage 1 (V_{CU1}) and overcharge release voltage 1 (V_{CL1}).

Overcharge detection voltage 2 (V_{CU2}) is defined as the voltage between the VC and VSS pins at which V_{CO} goes from “H” to “L” when the voltage V2 is gradually increased from the starting condition of V1 = V2 = 3.5 V, V3 = 0 V. Overcharge release voltage 2 (V_{CL2}) is defined as the voltage between the VC and VSS pins at which V_{CO} goes from “L” to “H” when the voltage V2 is then gradually decreased. Overcharge hysteresis voltage 2 (V_{HC2}) is defined as the difference between overcharge detection voltage 2 (V_{CU2}) and overcharge release voltage 2 (V_{CL2}).

2. Overdischarge detection voltage, overdischarge release voltage

(Test Condition 2, Test Circuit 1)

Overdischarge detection voltage 1 (V_{DL1}) is defined as the voltage between the VDD and VC pins at which V_{DO} goes from “H” to “L” when the voltage V1 is gradually decreased from the starting condition of V1 = V2 = 3.5 V, V3 = 0 V. Overdischarge release voltage 1 (V_{DU1}) is defined as the voltage between the VDD and VC pins at which V_{DO} goes from “L” to “H” when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage 1 (V_{HD1}) is defined as the difference between overdischarge release voltage 1 (V_{DU1}) and overdischarge detection voltage 1 (V_{DL1}).

Overdischarge detection voltage 2 (V_{DL2}) is defined as the voltage between the VC and VSS pins at which V_{DO} goes from “H” to “L” when the voltage V2 is gradually decreased from the starting condition of V1 = V2 = 3.5 V, V3 = 0 V. Overdischarge release voltage 2 (V_{DU2}) is defined as the voltage between the VC and VSS pins at which V_{DO} goes from “L” to “H” when the voltage V2 is then gradually increased. Overdischarge hysteresis voltage 2 (V_{HD2}) is defined as the difference between overdischarge release voltage 2 (V_{DU2}) and overdischarge detection voltage 2 (V_{DL2}).

3. Overcurrent detection voltage 1, overcurrent detection voltage 2

(Test Condition 3, Test Circuit 1)

Overcurrent detection voltage 1 (V_{IOV1}) is defined as the voltage between the VM and VSS pins whose delay time for changing V_{DO} from “H” to “L” lies between the minimum and the maximum value of overcurrent delay time 1 when the voltage V3 is increased rapidly within 10 μs from the starting condition of V1 = V2 = 3.5V, V3 = 0 V.

Overcurrent detection voltage 2 (V_{IOV2}) is defined as the voltage between the VM and VSS pins whose delay time for changing V_{DO} from “H” to “L” lies between the minimum and the maximum value of overcurrent delay time 2 when the voltage V3 is increased rapidly within 10 μs from the starting condition of V1 = V2 = 3.5V, V3 = 0 V.

4. Charger detection voltage (abnormal charge current detection voltage)

(Test Condition 4, Test Circuit 1)

The charger detection voltage (V_{CHA}) is defined as the voltage between the VM and VSS pins at which V_{DO} goes from "L" to "H" when the voltage V3 is gradually decreased from 0 V after the voltage V1 is gradually increased from the starting condition of V1 = 1.8 V, V2 = 3.5 V, V3 = 0 V until the voltage V1 becomes V_{DL1} + (V_{HD1}/2).

The charger detection voltage can be measured only in a product whose overdischarge hysteresis $V_{HD} \neq 0$ V.

The abnormal charge current detection voltage is defined as the voltage between the VM and VSS pins at which V_{CO} goes from "H" to "L" when the voltage V3 is gradually decreased from the starting condition of V1 = V2 = 3.5 V, V3 = 0 V. The value of the abnormal charge current detection voltage is the same as that of the charger detection voltage (V_{CHA}).

5. Operating current consumption, power-down current consumption, VC pin current

(Test Condition 5, Test Circuit 2)

The operating current consumption (I_{OPE}) is the current I_{SS} that flows through the VSS pin and the VC pin current (I_{VC}) is the current I_C that flows through the VC pin under the set conditions of V1 = V2 = 3.5 V and S1:OFF, S2:ON (normal status).

The power-down current consumption (I_{PDN}) is the current I_{SS} that flows through the VSS pin under the set conditions of V1 = V2 = 1.5 V and S1:ON, S2:OFF (overdischarge status).

6. Resistance between VM and VDD, resistance between VM and VSS

(Test Condition 6, Test Circuit 2)

The resistance between VM and VDD (R_{VMD}) is the resistance between VM and VDD under the set conditions of V1 = V2 = 1.5 V and S1:OFF, S2:ON.

The resistance between VM and VSS (R_{VMS}) is the resistance between VM and VSS under the set conditions of V1 = V2 = 3.5 V and S1:ON, S2:OFF.

7. CO pin H resistance, CO pin L resistance

(Test Condition 7, Test Circuit 3)

The CO pin H resistance (R_{COH}) is the resistance at the CO pin under the set conditions of V1 = V2 = 3.5 V, V4 = 6.5 V.

The CO pin L resistance (R_{COL}) is the resistance at the CO pin under the set conditions of V1 = V2 = 4.5 V, V4 = 0.5 V.

8. DO pin H resistance, DO pin L resistance

(Test Condition 8, Test Circuit 3)

The DO pin H resistance (R_{DOH}) is the resistance at the DO pin under the set conditions of V1 = V2 = 3.5 V, V5 = 6.5 V.

The DO pin L resistance (R_{DOL}) is the resistance at the DO pin under the set conditions of V1 = V2 = 4.5 V, V5 = 0.5 V.

9. Overcharge detection delay time, overdischarge detection delay time

(Test Condition 9, Test Circuit 1)

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to change from "H" to "L" just after the voltage V1 momentarily increases within 10 μs from overcharge detection voltage 1 (V_{CU1}) − 0.2 V to overcharge detection voltage 1 (V_{CU1}) + 0.2 V under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to change from "H" to "L" just after the voltage V1 momentarily decreases within 10 μs from overcharge detection voltage 1 (V_{DL1}) + 0.2 V to overcharge detection voltage 1 (V_{DL1}) – 0.2 V under the set condition of V1 = V2 = 3.5 V, V3 = 0 V.

10. Overcurrent detection delay time 1, overcurrent detection delay time 2

(Test Condition 10, Test Circuit 1)

Overcurrent detection delay time 1 (t_{IOV1}) is the time needed for V_{DO} to go to "L" after the voltage V3 momentarily increases within 10 μs from 0 V to 0.35 V under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

Overcurrent detection delay time 2 (t_{IOV2}) is the time needed for V_{DO} to go to "L" after the voltage V3 momentarily increases within 10 μs from 0 V to 2.0 V under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

11. 0 V charge starting charger voltage (products in which 0 V charge is available)

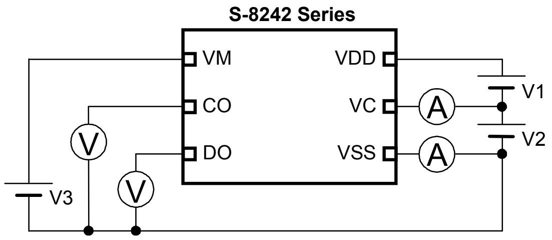
(Test Condition 11, Test Circuit 1)

The 0 V charge starting charger voltage (V_{0CHA}) is defined as the voltage between the VDD and VM pins at which V_{CO} goes to "H" (V_{VM} + 0.1 V or higher) when the voltage V3 is gradually decreased from the starting condition of V1 = V2 = V3 = 0 V.

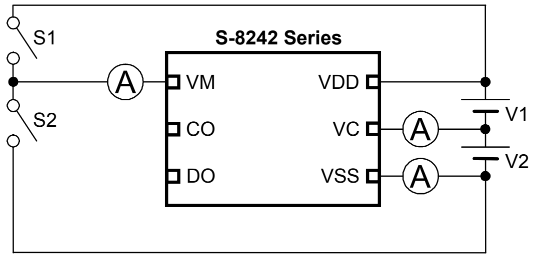
12. 0 V charge inhibition battery voltage (products in which 0 V charge is unavailable)

(Test Condition 12, Test Circuit 1)

The 0 V charge inhibition charger voltage (V_{0INH}) is defined as the voltage between the VDD and VSS pins at which V_{CO} goes to "H" (V_{VM} + 0.1 V or higher) when the voltages V1 and V2 are gradually increased from the starting condition of V1 = V2 = 0 V, V3 = –4 V.



Test Circuit 1



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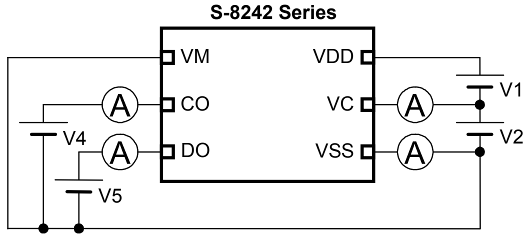


Test Circuit 3

Figure 4

■ Description of Operation

Remark Refer to ■ **Standard Circuit**.

1. Normal status

This IC monitors the voltage of the battery connected between the VDD and VSS pins and the voltage difference between the VM and VSS pins to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage n (V_{DLn}) to overcharge detection voltage n (V_{CUn}), and the VM pin voltage is in the range from the charger detection voltage (V_{CHA}) to overcurrent detection voltage 1 (V_{IOV1}), the IC turns both the charging and discharging control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.

Caution When the battery is connected for the first time, discharging may not be enabled. In this case, short the VM and VSS pins or connect the charger to restore the normal status.

2. Overcharge status

When the battery voltage becomes higher than overcharge detection voltage n (V_{CUn}) during charging in the normal status and detection continues for the overcharge detection delay time (t_{CU}) or longer, the S-8242 Series turns the charging control FET off to stop charging. This condition is called the overcharge status. The overcharge status is released in the following two cases (a and b).

a) When the battery voltage falls below overcharge release voltage n (V_{CLn}), the S-8242 Series turns the charging control FET on and returns to the normal status.

b) When a load is connected and discharging starts, the S-8242 Series turns the charging control FET on and returns to the normal status. Just after the load is connected and discharging starts, the discharging current flows through the parasitic diode in the charging control FET. At this moment the VM pin potential becomes V_f, the voltage for the parasitic diode, higher than the V_{SS} level. When the battery voltage goes under overcharge detection voltage n (V_{CUn}) and provided that the VM pin voltage is higher than overcurrent detection voltage 1, the S-8242 Series releases the overcharge condition.

Cautions 1. If the battery is charged to a voltage higher than overcharge detection voltage n (V_{CUn}) and the battery voltage does not fall below overcharge detection voltage n (V_{CUn}) even when a heavy load is connected, overcurrent 1 and overcurrent 2 do not function until the battery voltage falls below overcharge detection voltage n (V_{CUn}). Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and overcurrent 1 and overcurrent 2 function.

2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below overcharge release voltage n (V_{CLn}). The overcharge status is released when the VM pin voltage goes over the charger detection voltage (V_{CHA}) by removing the charger.

3. Overdischarge status

When the battery voltage falls below overdischarge detection voltage n (V_{DLn}) during discharging in the normal status and detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8242 Series turns the discharging control FET off to stop discharging. This condition is called the overdischarge status. When the discharging control FET is turned off, the VM pin voltage is pulled up by the resistor between the VM and VDD pins in the IC (R_{VMD}). When the voltage difference between the VM and VDD pins then is 1.3 V (typ.) or lower, the current consumption is reduced to the power-down current consumption (I_{PDN}). This condition is called the power-down status.

The power-down status is released when a charger is connected and the voltage difference between the VM and VDD pins becomes 1.3 V (typ.) or higher. Moreover, when the battery voltage becomes overdischarge detection voltage n (V_{DLn}) or higher, the S-8242 Series turns the discharging FET on and returns to the normal status.

4. Charger detection

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than the charger detection voltage (V_{CHA}), the overdischarge hysteresis is released via the charge detection function; therefore, the S-8242 Series releases the overdischarge status and turns the discharging control FET on when the battery voltage becomes equal to or higher than overdischarge detection voltage n (V_{DLn}) since the charger detection function works. This action is called charger detection.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is not lower than the charger detection voltage (V_{CHA}), the S-8242 Series releases the overdischarge status when the battery voltage reaches overdischarge detection voltage n (V_{DUn}) or higher.

5. Abnormal charge current detection

If the VM pin voltage falls below the charger detection voltage (V_{CHA}) during charging in the normal status and detection continues for the overcharge detection delay time (t_{CU}) or longer, the charging control FET is turned off and charging stops. This action is called the abnormal charge current detection.

Abnormal charge current detection works when the DO pin voltage is “H” and the VM pin voltage falls below the charger detection voltage (V_{CHA}). Consequently, if an abnormal charge current flows to an over-discharged battery, the S-8242 Series turns the charging control FET off and stops charging after the battery voltage becomes higher than overdischarge detection voltage n (V_{DLn}) making the DO pin voltage “H”, and after the overcharge detection delay time (t_{CU}) elapses.

Abnormal charge current detection is released when the voltage difference between the VM pin and VSS pin becomes less than charger detection voltage (V_{CHA}).

6. Overcurrent status

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or higher than the overcurrent detection voltage because the discharge current is higher than the specified value and the status lasts for the overcurrent detection delay time, the discharge control FET is turned off and discharging is stopped. This status is called the overcurrent status.

In the overcurrent status, the VM and VSS pins are shorted by the resistor between VM and VSS (R_{VMS}) in the IC. However, the voltage of the VM pin is at the V_{DD} potential due to the load as long as the load is connected. When the load is disconnected, the VM pin returns to the V_{SS} potential.

This IC detects the status when the impedance between the EB+ pin and EB– pin (refer to Figure 10) increases and is equal to the impedance that enables automatic restoration and the voltage at the VM pin returns to overcurrent detection voltage 1 (V_{IOV1}) or lower and the overcurrent status is restored to the normal status.

Caution The impedance that enables automatic restoration varies depending on the battery voltage and the set value of overcurrent detection voltage 1.

7. 0 V battery charge function

0 V battery charge “available”[*1, *2]

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ and EB– pins by connecting a charger, the charging control FET gate is fixed to the VDD pin voltage. When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage due to the charger voltage, the charging control FET is turned on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than overdischarge release voltage n (V_{DUn}), the S-8242 Series enters the normal status.

0 V battery charge “unavailable”[*1]

This function inhibits recharging when a battery that is internally short-circuited (0 V) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charging control FET gate is fixed to the EB– pin voltage to inhibit charging. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or higher, charging can be performed.

***1.** Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

***2.** The 0 V battery charge function has higher priority than the abnormal charge current detection function. Consequently, a product in which use of the 0 V battery charge function is enabled charges a battery forcibly and the abnormal charge current cannot be detected when the battery voltage is low.

8. Delay circuit

The detection delay times are determined by dividing a clock of approximately 3.5 kHz by the counter.

Caution The overcurrent detection delay time 2(t_{IOV2}) starts when the overcurrent detection voltage 1(V_{IOV1}) is detected. As soon as the overcurrent detection voltage 2(V_{IOV2}) is detected over the detection delay time for overcurrent 2(t_{IOV2}) after the detection of overcurrent 1, the S-8242 turns the discharging control FET off.

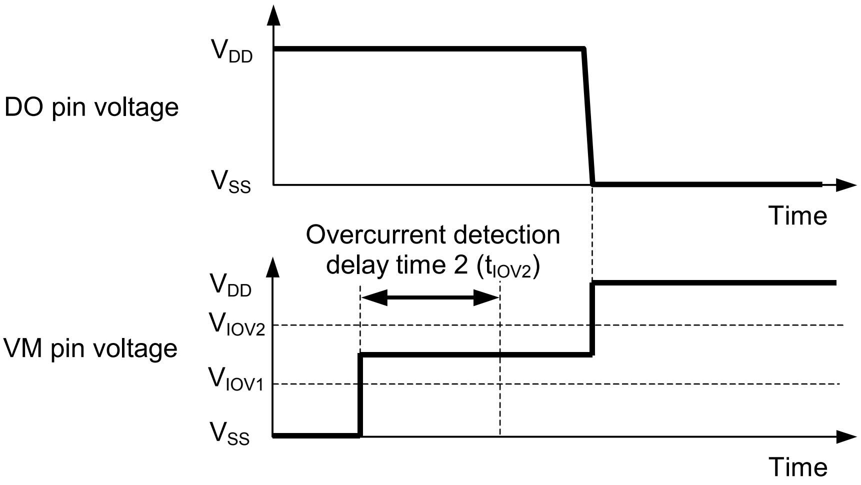
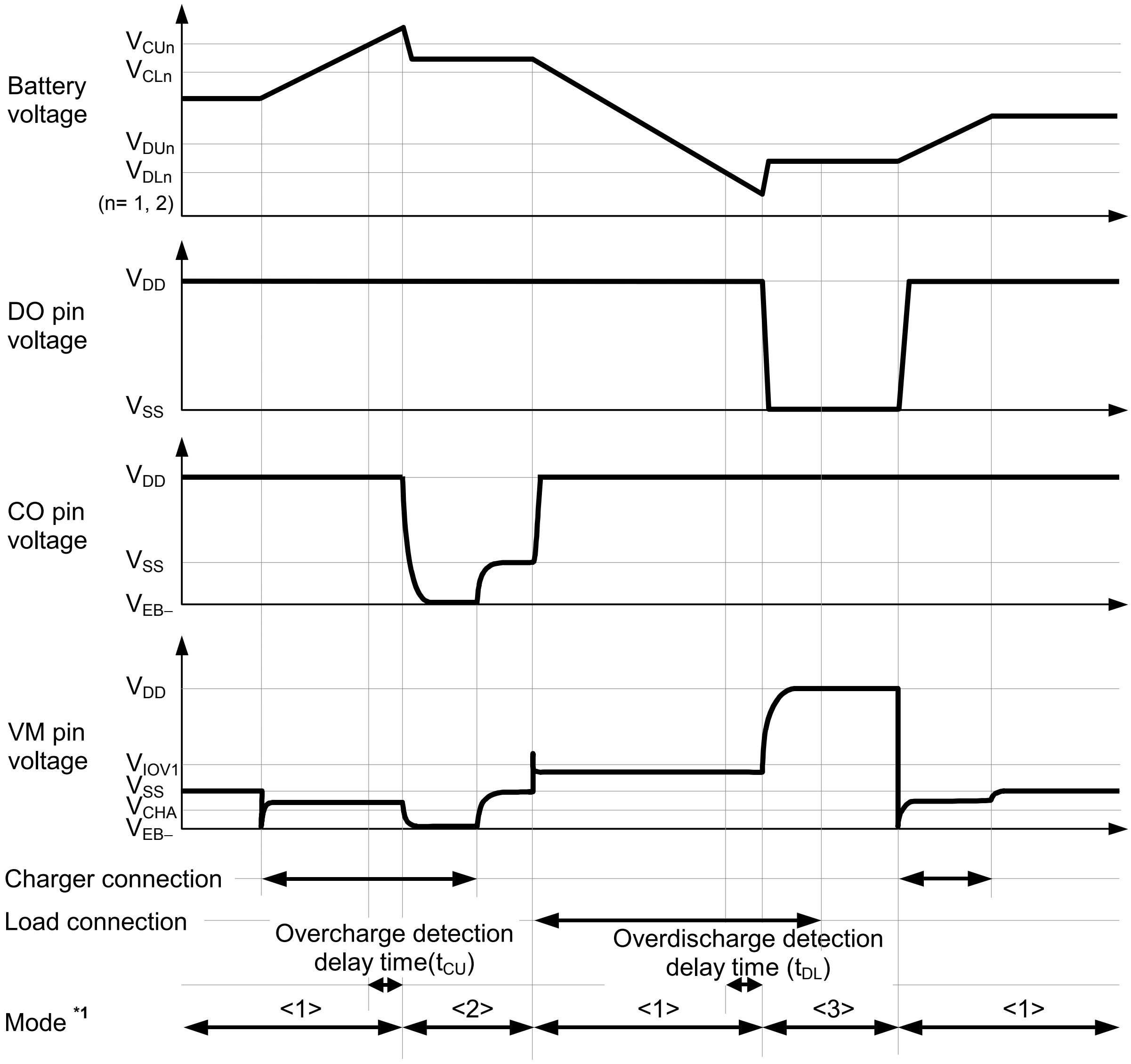


Figure 5

Caution When overcurrent is detected and continues for longer than the overdischarge detection delay time (t_{DL}) without the load being released, the status changes to the power-down status when the battery voltage falls below overdischarge detection voltage n (V_{DLn}).
When the battery voltage falls below overdischarge detection voltage n (V_{DLn}) due to overcurrent, the S-8242 Series turns the discharging control FET off via overcurrent detection. In this case the recovery of the battery voltage is so slow that if the battery voltage after the overdischarge detection delay time is still lower than the overdischarge detection voltage, the S-8242 Series shifts to the power-down status.

■ Operation Timing Chart

1. Overcharge detection, overdischarge detection

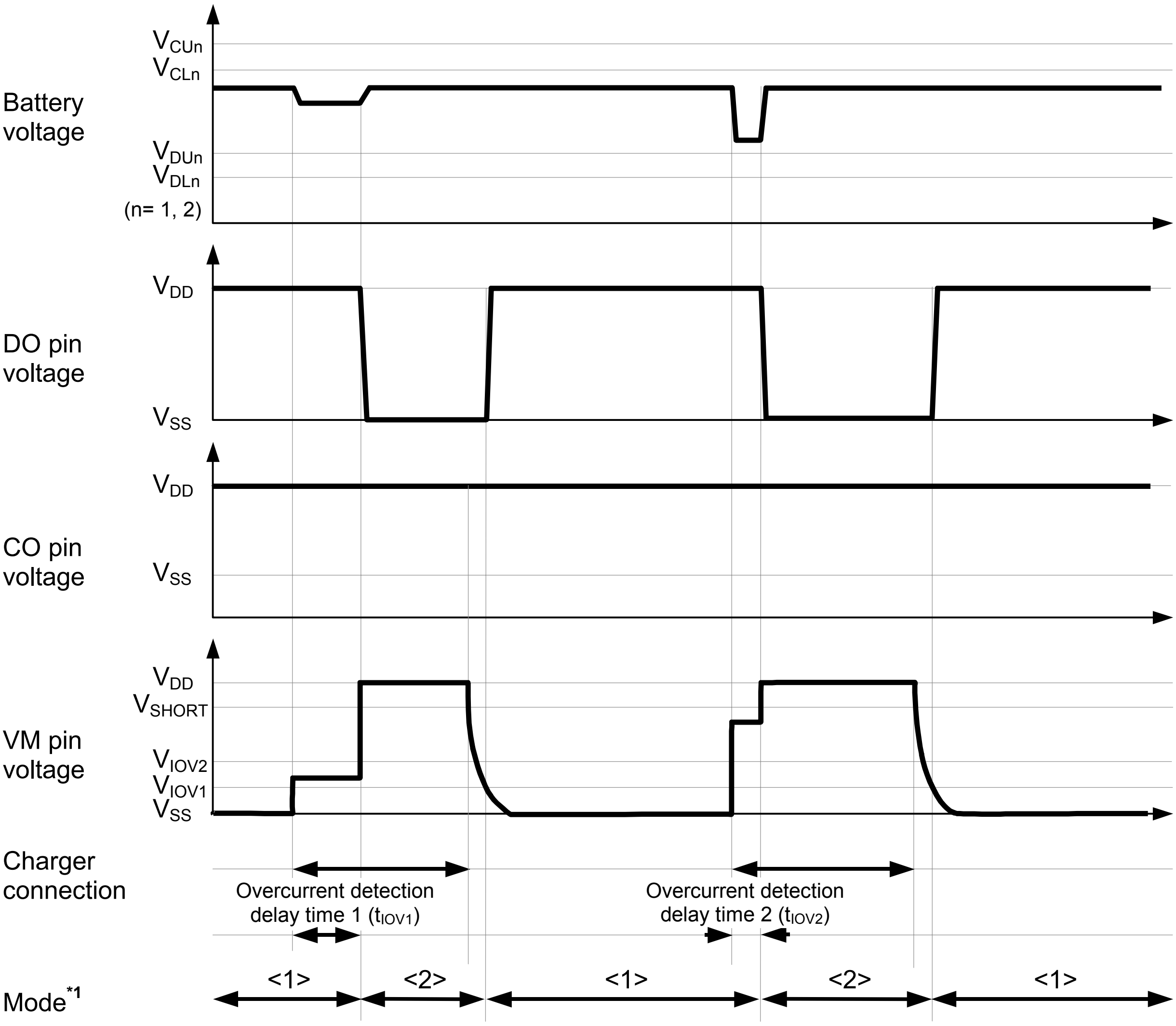


***1.** <1>: Normal mode
<2>: Overcharge mode
<3>: Overdischarge mode

Remark The charger is assumed to charge with a constant current.

Figure 6

2. Overcurrent detection

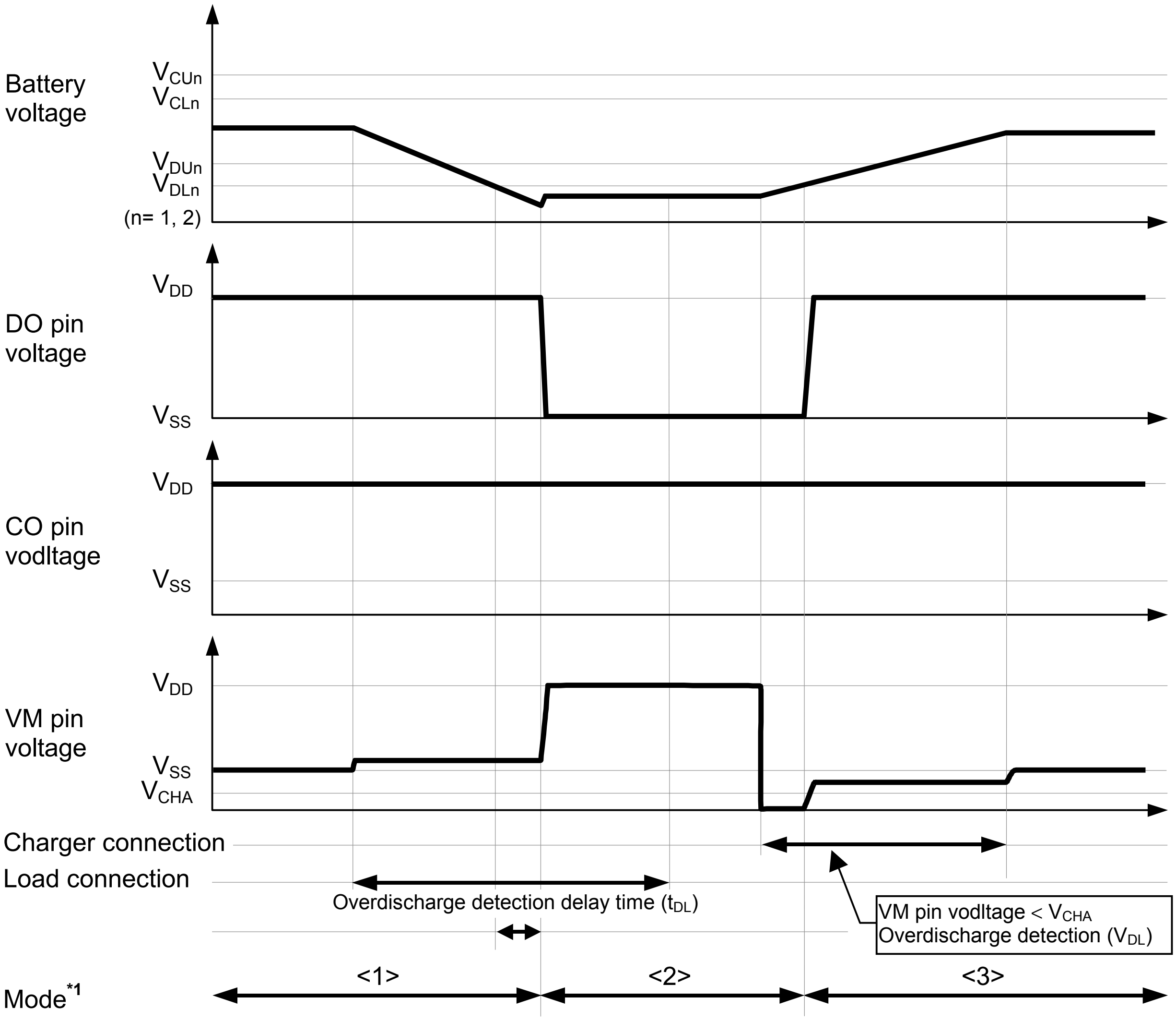


***1.** <1>: Normal mode
<2>: Overcurrent mode

Remark The charger is assumed to charge with a constant current.

Figure 7

3. Charger detection

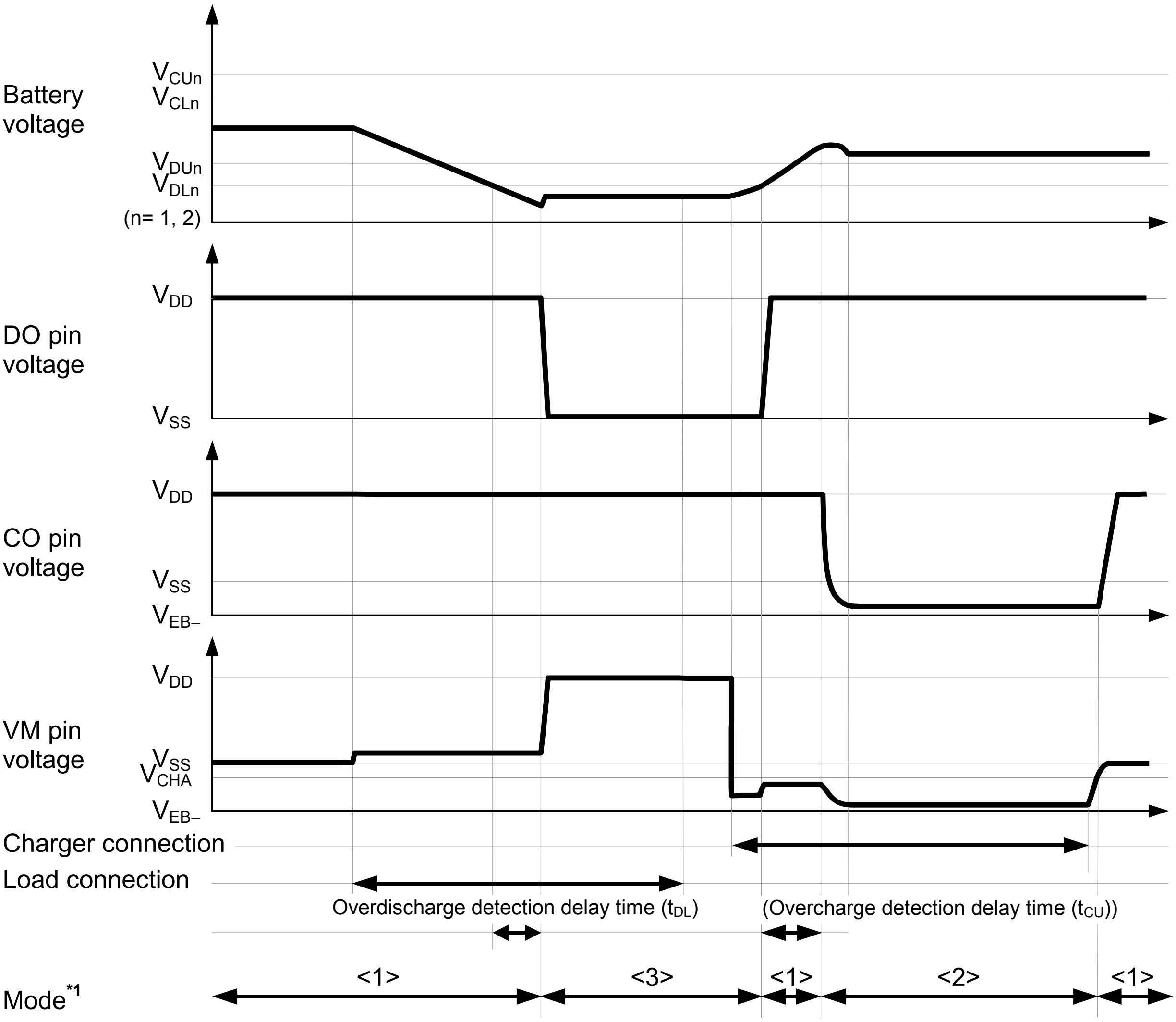


***1.** <1>: Normal mode
<2>: Overdischarge mode

Remark The charger is assumed to charge with a constant current.

Figure 8

4. Abnormal charge current detection



***1.** <1>: Normal mode
<2>: Overcharge mode
<3>: Overdischarge mode

Remark The charger is assumed to charge with a constant current.

Figure 9

■ Standard Circuit

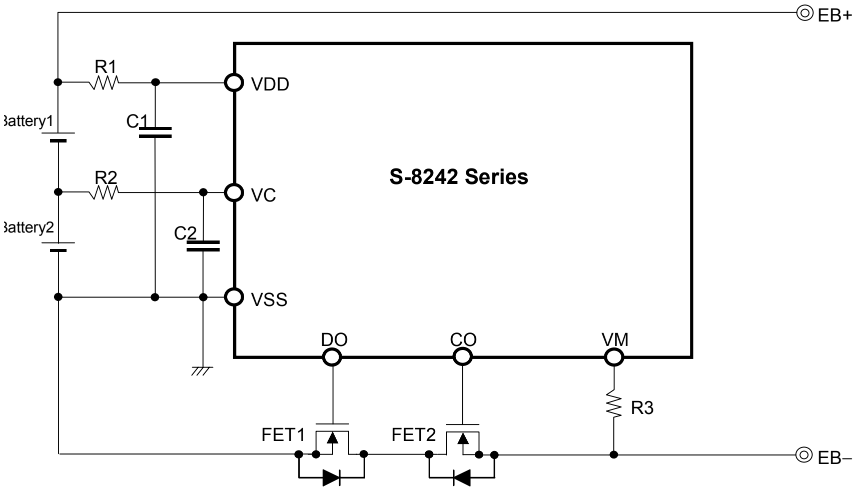


Figure 10

Table 6 Constants for External Components

Symbol	Part	Purpose	Recommended Value	Min.	Max.	Remarks
FET1	N-channel MOSFET	Discharge control	—	—	—	Threshold voltage ≤ Overdischarge detection voltage[*1] Gate to source withstanding voltage ≥ Charger voltage[*2]
FET2	N-channel MOSFET	Charge control	—	—	—	Threshold voltage ≤ Overdischarge detection voltage[*1] Gate to source withstanding voltage ≥ Charger voltage[*2]
R1	Resistor	ESD protection For power fluctuation	470 Ω	300 Ω	1 kΩ	Resistance should be as small as possible to avoid lowering the overcharge detection accuracy due to current consumption. [*3]
C1	Capacitor	For power fluctuation	0.1 μF	0.022 μF	1.0 μF	Connect a capacitor of 0.022 μF or higher between VDD and VSS. [*4]
R2	Resistor	ESD protection For power fluctuation	470 Ω	300 Ω	1 kΩ	Make the input filter constant of the VDD pin and the VC pin same.
C2	Capacitor	For power fluctuation	0.1 μF	0.022 μF	1.0 μF	Install a capacitor of 0.022 μF or higher between VC and VSS. [*4]
R3	Resistor	Protection for reverse connection of a charger	2 kΩ	300 Ω	4 kΩ	Select as large a resistance as possible to prevent current when a charger is connected in reverse. [*5]

***1.** If the threshold voltage of an FET is low, the FET may not cut the charging current.
If an FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

***2.** If the withstanding voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.

***3.** If R1 has a high resistance, the voltage between VDD and VSS may exceed the absolute maximum rating when a charger is connected in reverse since the current flows from the charger to the IC.
Insert a resistor of 300 Ω or higher as R1 for ESD protection.

***4.** If a capacitor of less than 0.022 μF is connected as C1, DO may oscillate when load short-circuiting is detected. Be sure to connect a capacitor of 0.022 μF or higher as C1.

***5.** If R3 has a resistance higher than 4 kΩ, the charging current may not be cut when a high-voltage charger is connected.

Caution The standard circuit above does not guarantee proper operation.
Evaluation in the actual application is needed to determine the correct constants.

■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order; however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VM and VSS pins or connect the battery charger to return to the normal status.
- Do not expose this IC to an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
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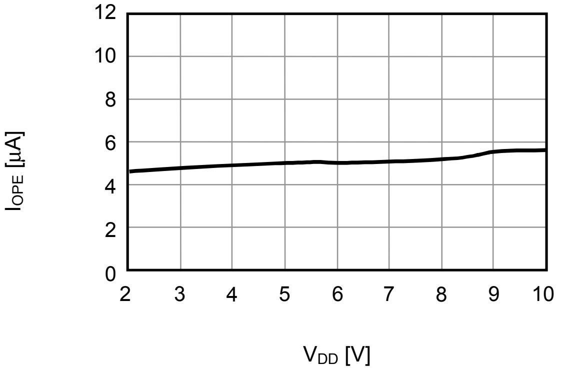
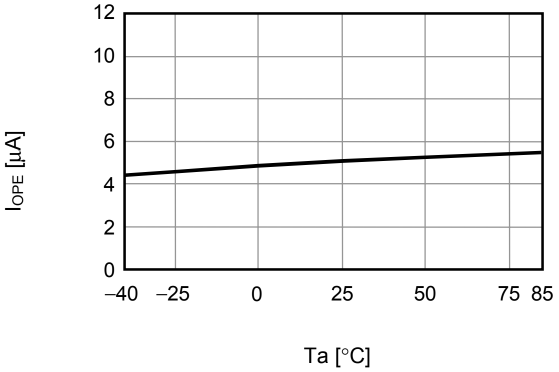
■ Characteristics (Typical Data)

(1) Current consumption

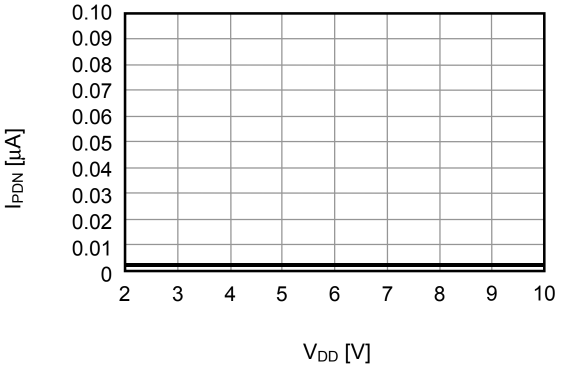
1. I_{OPE} – V_{DD}



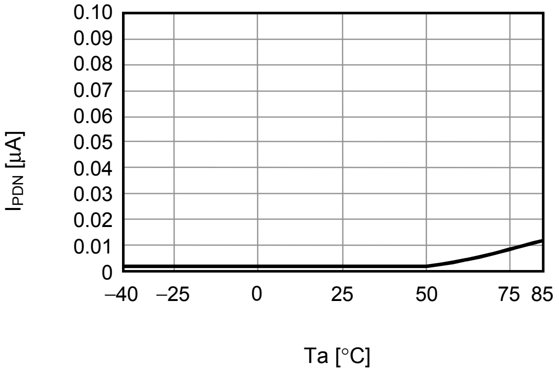
2. I_{OPE} – Ta



3. I_{PDN} – V_{DD}

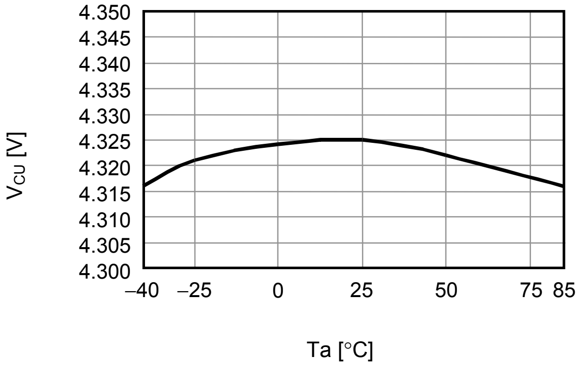


4. I_{PDN} – Ta

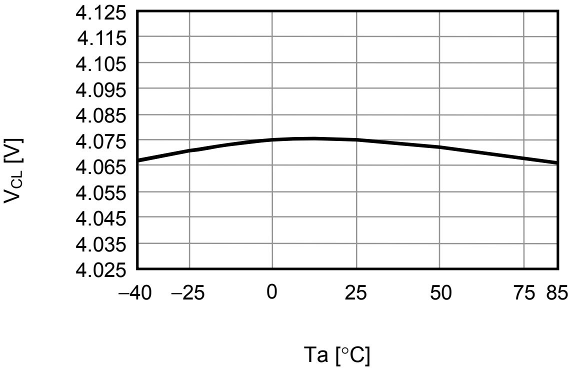


(2) Overcharge detection/release voltage, overdischarge detection/release voltage, overcurrent detection voltage, and delay time

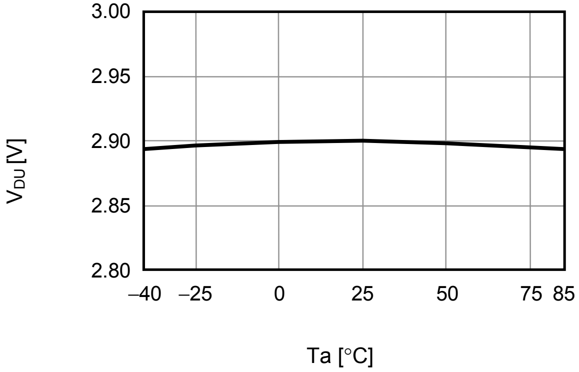
1. V_{CU} – Ta



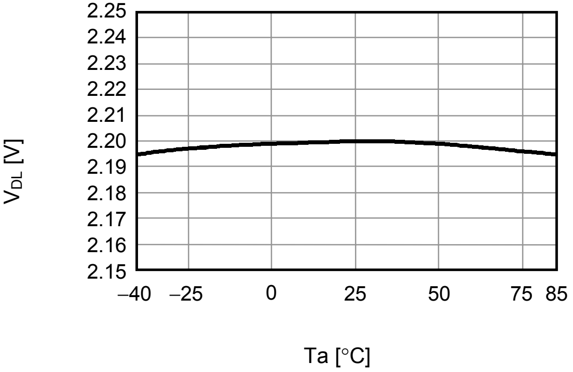
2. V_{CL} – Ta



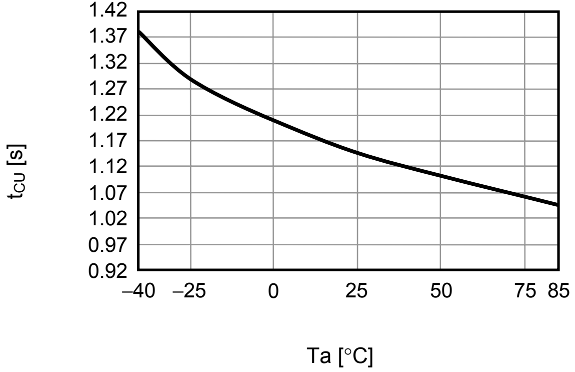
3. V_{DU} – Ta



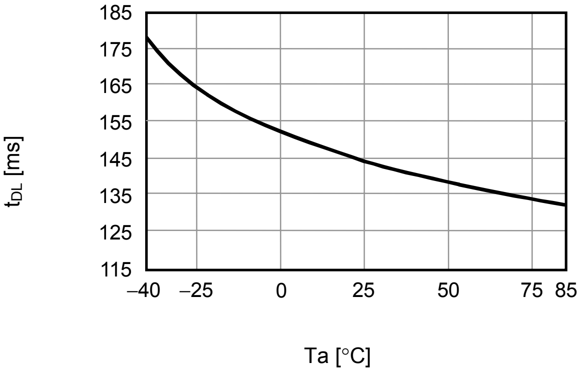
4. V_{DL} – Ta



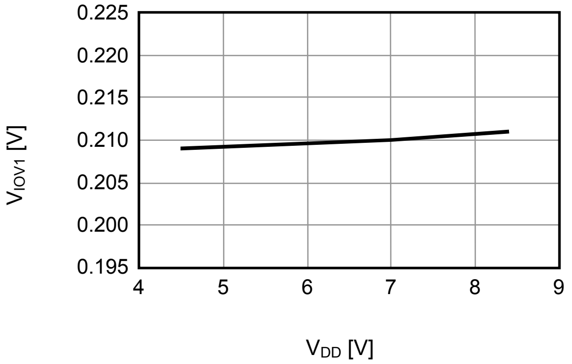
5. t_{CU} – Ta



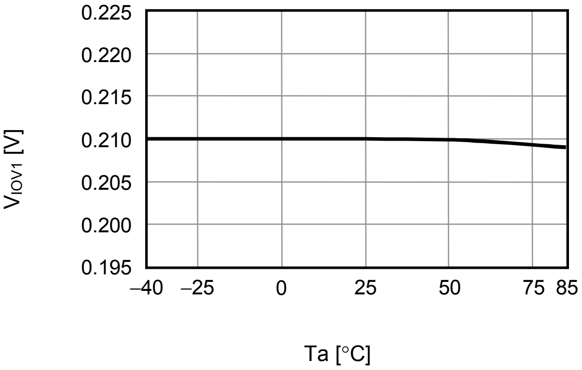
6. t_{DL} – Ta



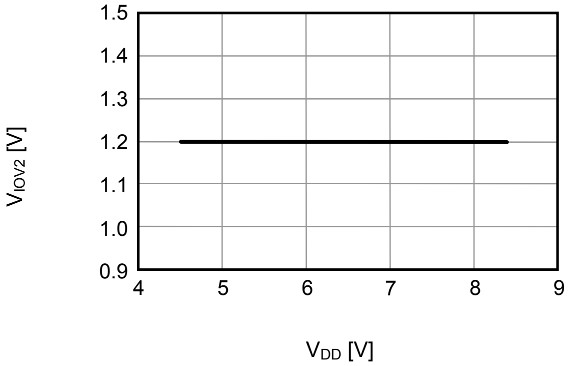
7. V_{IOV1} – V_{DD}



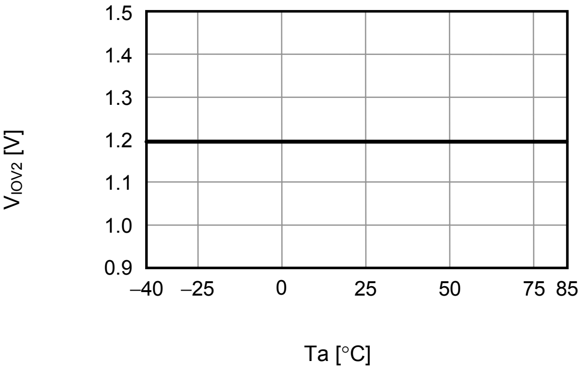
8. V_{IOV1} – Ta



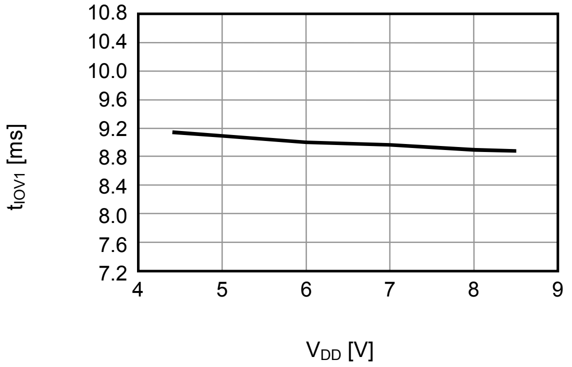
9. V_{IOV2} – V_{DD}



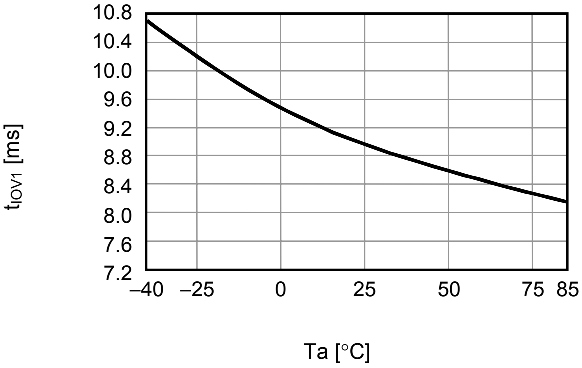
10. V_{IOV2} – Ta



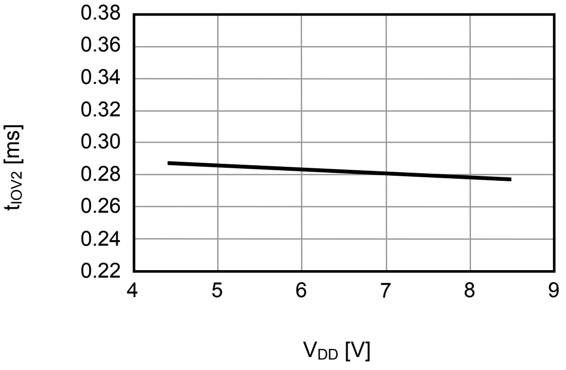
11. t_{IOV1} – V_{DD}



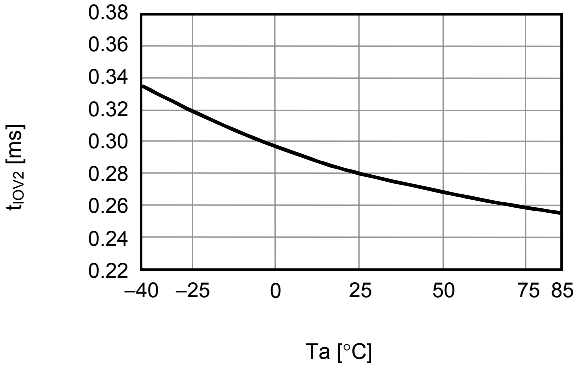
12. t_{IOV1} – Ta



13. t_{IOV2} – V_{DD}

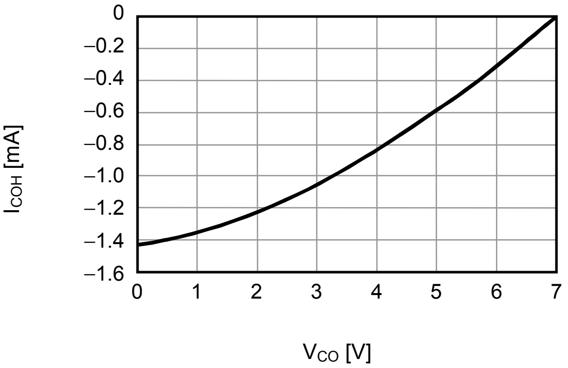


14. t_{IOV2} – Ta

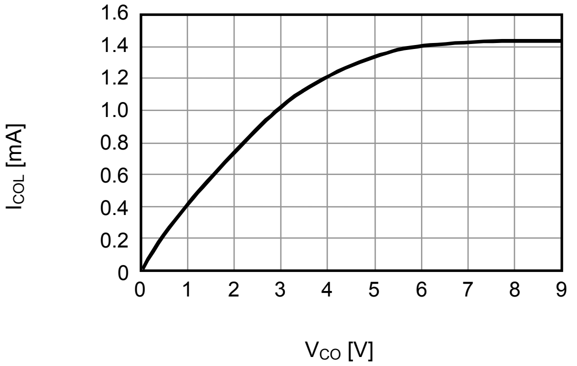


(3) CO/DO pin

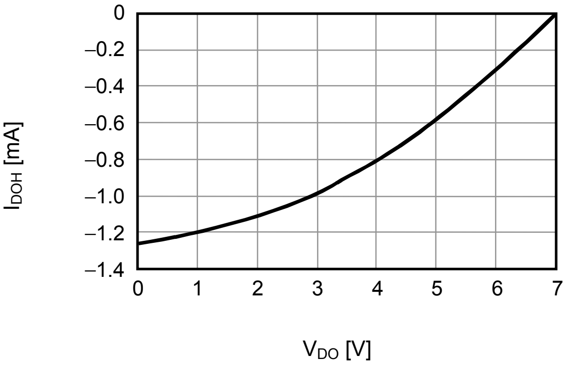
1. I_{COH} – V_{CO}



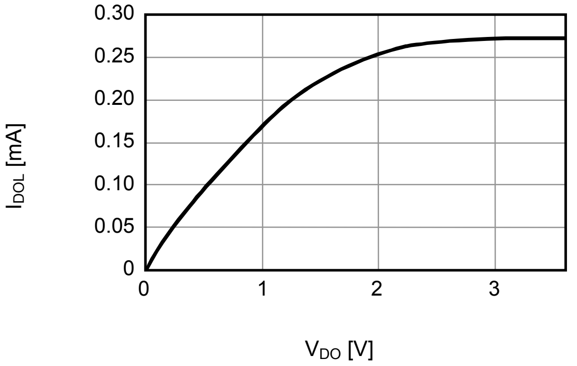
2. I_{COL} – V_{CO}

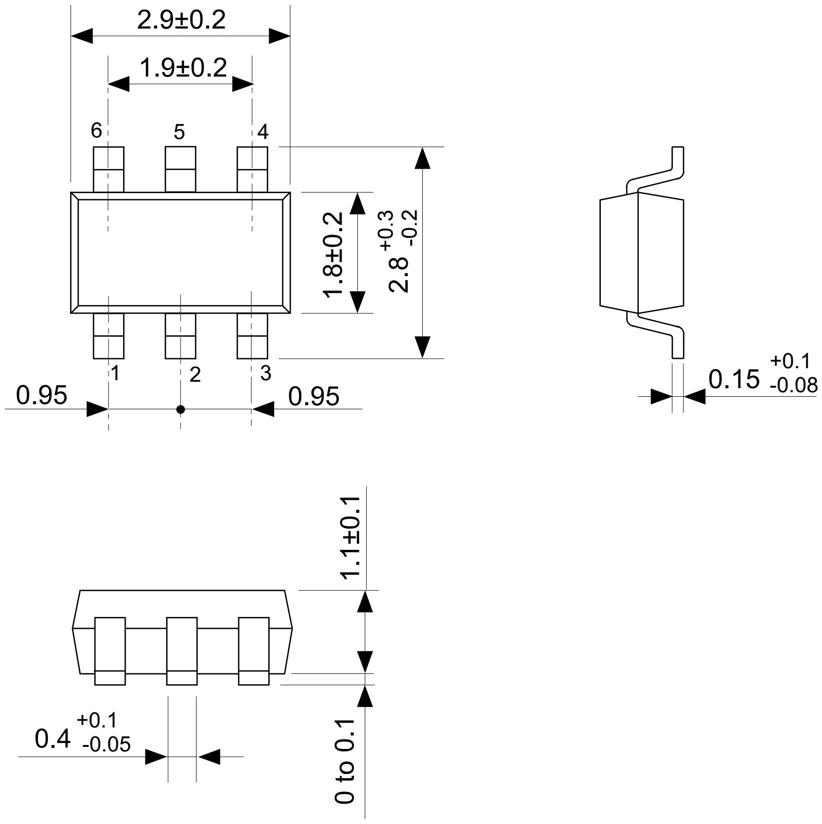


3. I_{DOH} – V_{DO}



4. I_{DOL} – V_{DO}





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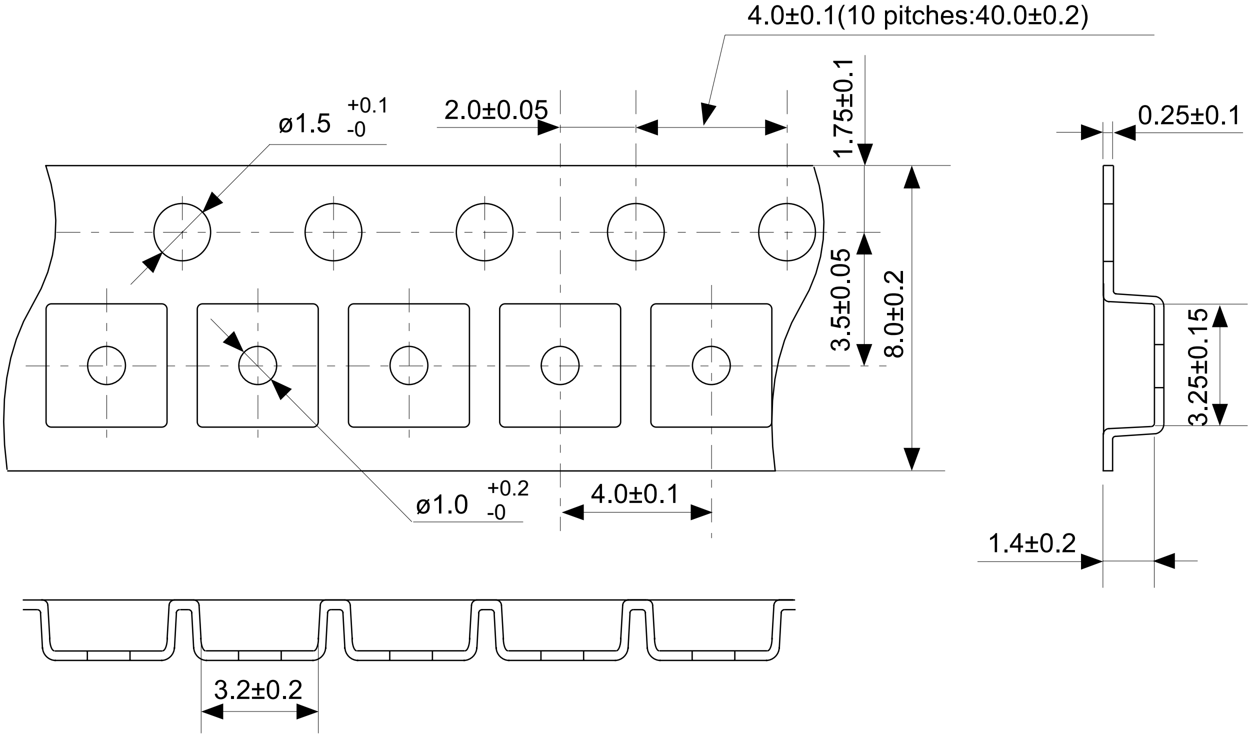
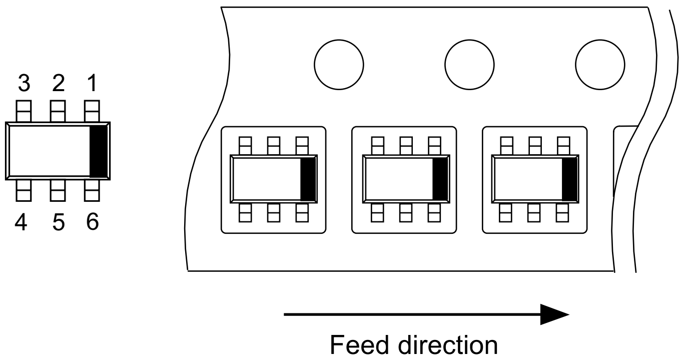
Seiko Instruments Inc.





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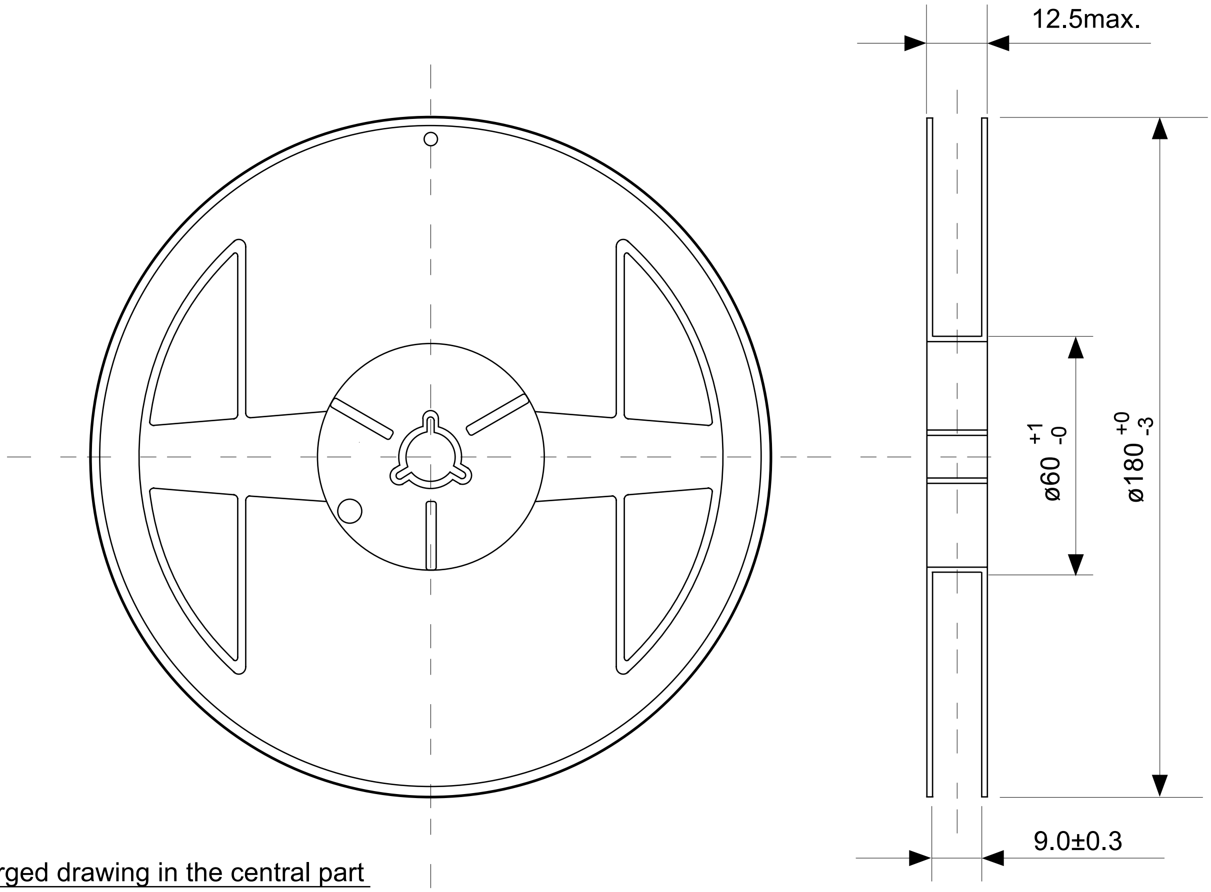

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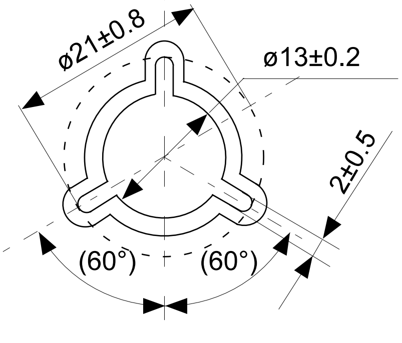

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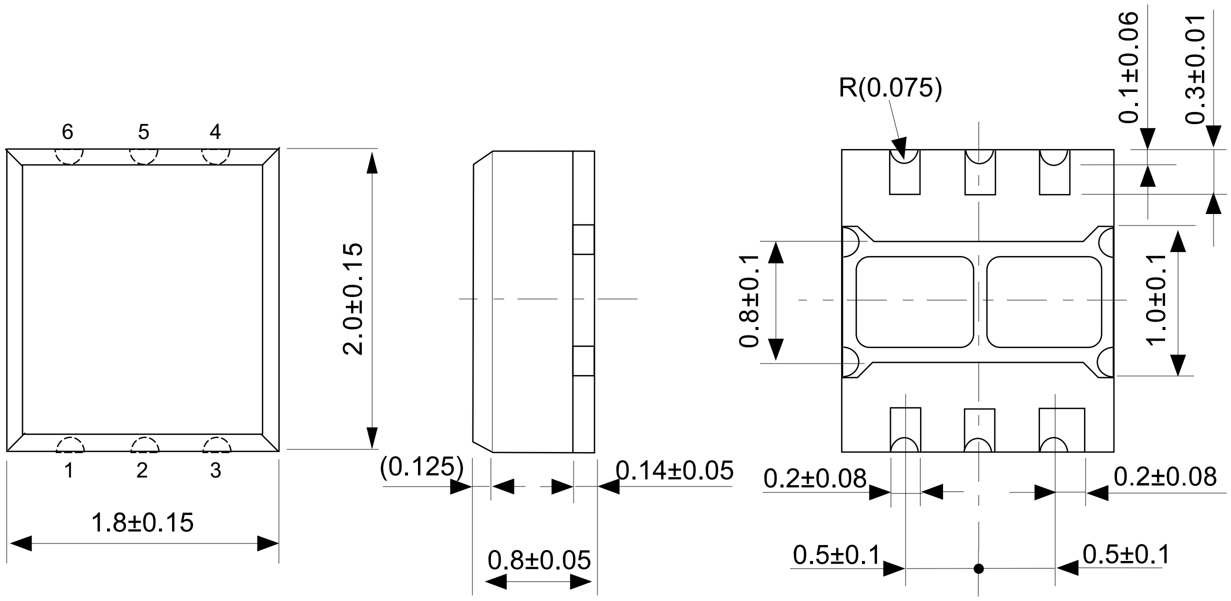

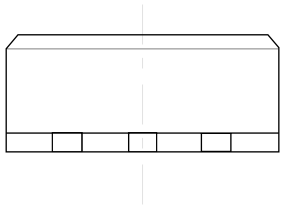

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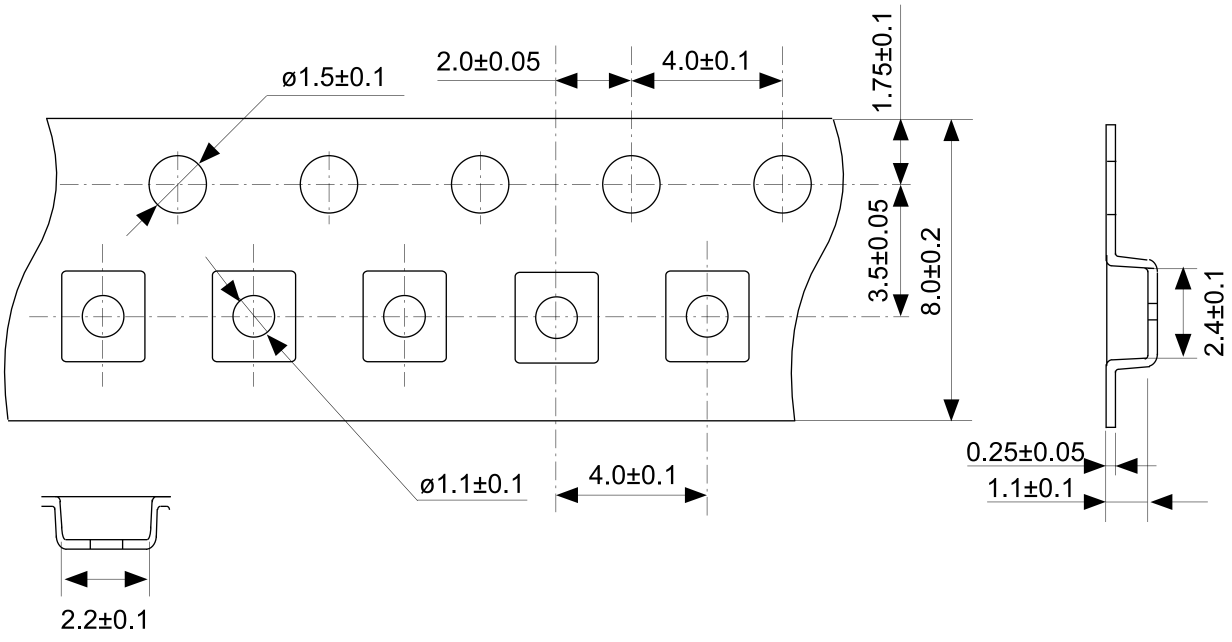

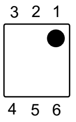

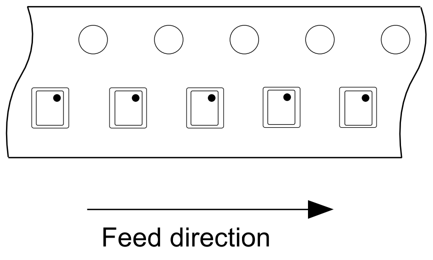

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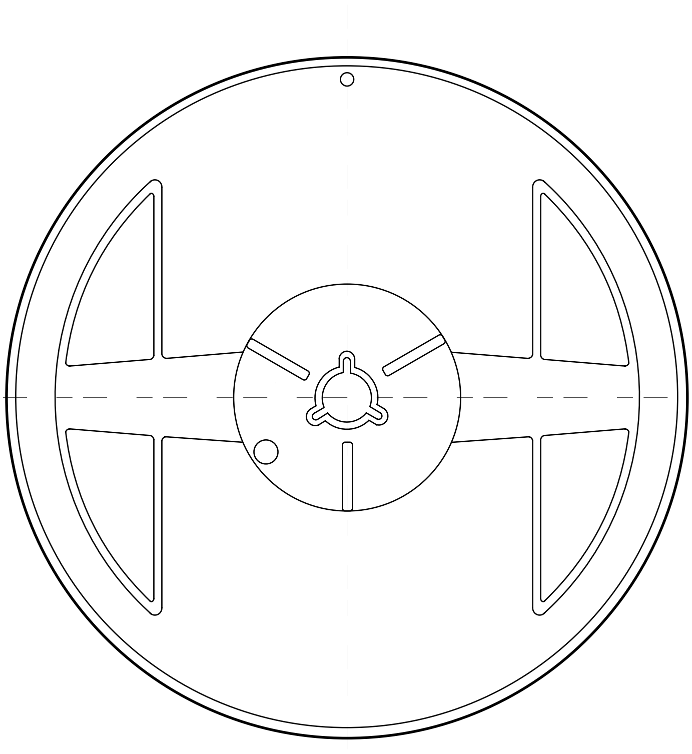

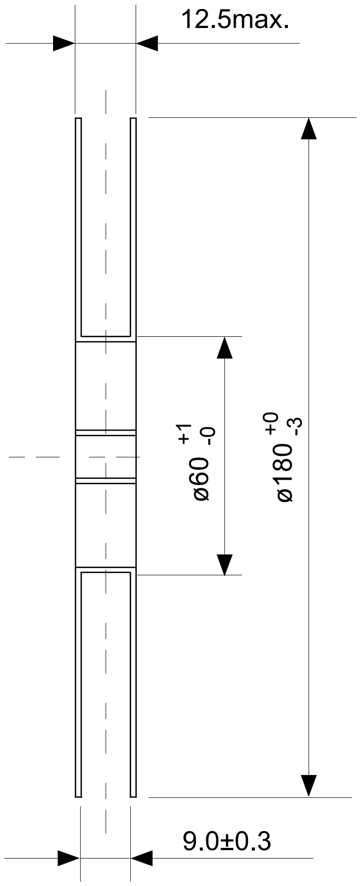

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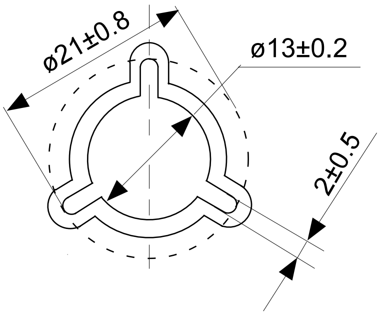

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