

BATTERY MONITORING IC FOR 1-CELL PACKwww.ablicinc.com

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Rev.1.1_01

The S-8259A Series is an IC including high-accuracy voltage detection circuits and delay circuits.

The S-8259A Series is suitable for monitoring overcharge and overdischarge for 1-cell lithium-ion / lithium polymer rechargeable battery packs.

■ Features

- High-accuracy voltage detection circuit

| | | |
|---------------------------------|----------------------------------|------------------|
| Overcharge detection voltage | 3.500 V to 4.600 V (5 mV step) | Accuracy ±20 mV |
| Overcharge release voltage | 3.100 V to 4.600 V ^{*1} | Accuracy ±50 mV |
| Overdischarge detection voltage | 2.000 V to 3.400 V (10 mV step) | Accuracy ±50 mV |
| Overdischarge release voltage | 2.000 V to 3.400 V ^{*2} | Accuracy ±100 mV |
- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary).
- CO pin output logic is selectable: Active "H", active "L"
- Wide operation temperature range: Ta = -40°C to +85°C
- Low current consumption

| | |
|-----------------------|---------------------------------------|
| During operation: | 1.5 μA typ., 3.0 μA max. (Ta = +25°C) |
| During overdischarge: | 2.0 μA max. (Ta = +25°C) |
- Lead-free (Sn 100%), halogen-free

*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected from a range of 0 V to 0.4 V in 50 mV step.)

*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected from a range of 0.1 V to 0.7 V in 100 mV step.)

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Package

- SOT-23-6

■ **Block Diagram**

1. CO pin output logic active "H"

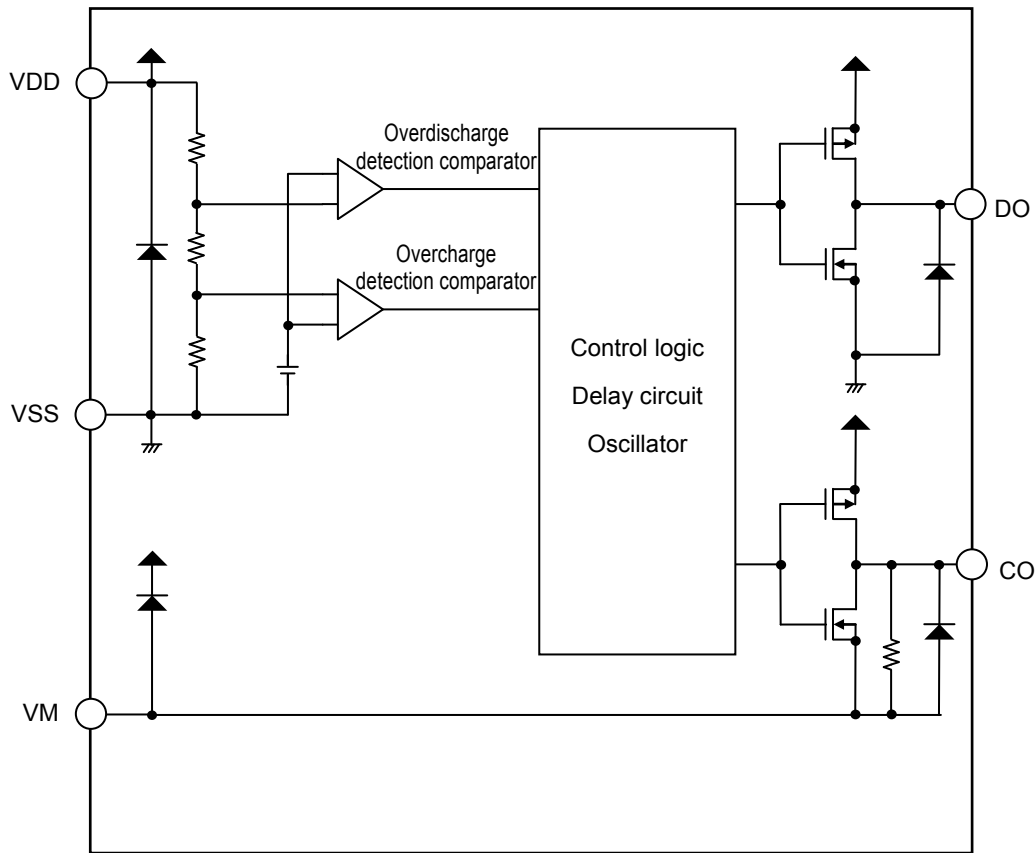


Figure 1

2. CO pin output logic active "L"

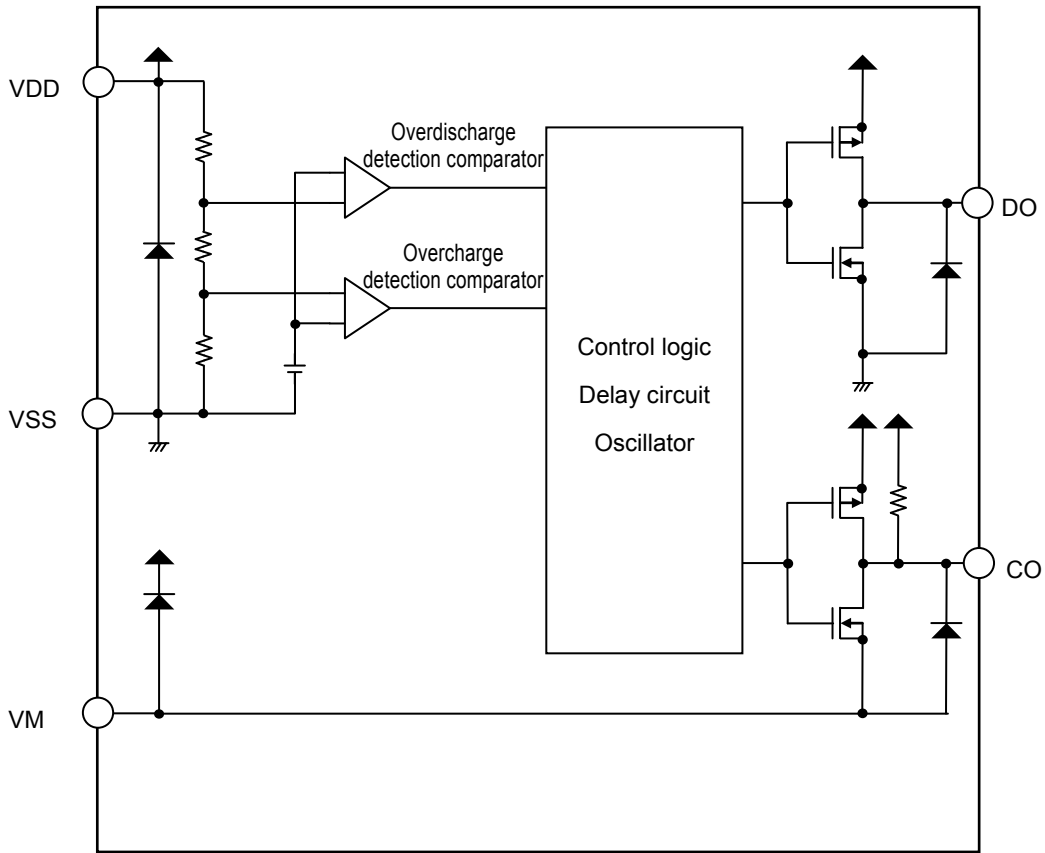
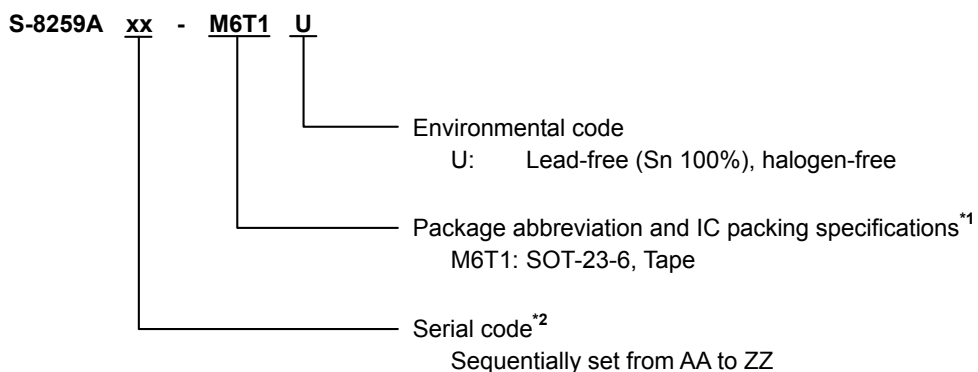


Figure 2

■ **Product Name Structure**

1. **Product name**



*1. Refer to the tape drawing.

*2. Refer to "3. Product name list".

2. **Package**

Table 1 Package Drawing Codes

| Package Name | Dimension | Tape | Reel |
|--------------|--------------|--------------|--------------|
| SOT-23-6 | MP006-A-P-SD | MP006-A-C-SD | MP006-A-R-SD |

3. Product name list

Table 2

| Product Name | Overcharge Detection Voltage [V _{CU}] | Overcharge Release Voltage [V _{CL}] | Overdischarge Detection Voltage [V _{DL}] | Overdischarge Release Voltage [V _{DU}] | Overcharge Detection Delay Time [t _{CU}] | Overcharge Release Delay Time [t _{CL}] | Overdischarge Detection Delay Time [t _{DL}] | CO Pin Output Logic*1 |
|-----------------|---|---|--|--|--|--|---|-----------------------|
| S-8259AAA-M6T1U | 4.275 V | 4.175 V | 2.300 V | 2.600 V | 1.0 s | 32 ms | 128 ms | Active "L" |
| S-8259AAB-M6T1U | 4.250 V | 4.100 V | 2.500 V | 3.000 V | 1.0 s | 128 ms | 256 ms | Active "L" |
| S-8259AAC-M6T1U | 3.900 V | 3.800 V | 2.000 V | 2.300 V | 1.0 s | 32 ms | 128 ms | Active "L" |
| S-8259AAD-M6T1U | 4.200 V | 4.100 V | 2.500 V | 3.000 V | 256 ms | 2.0 s | 32 ms | Active "L" |
| S-8259AAE-M6T1U | 4.200 V | 4.200 V | 2.800 V | 3.000 V | 1.0 s | 4.0 s | 256 ms | Active "L" |
| S-8259AAG-M6T1U | 3.650 V | 3.650 V | 2.500 V | 3.000 V | 1.0 s | 4.0 s | 1.0 s | Active "L" |
| S-8259AAH-M6T1U | 4.425 V | 4.325 V | 2.600 V | 2.900 V | 1.0 s | 32 ms | 128 ms | Active "L" |
| S-8259AAI-M6T1U | 4.350 V | 4.350 V | 2.600 V | 3.000 V | 1.0 s | 4.0 s | 128 ms | Active "L" |
| S-8259AAJ-M6T1U | 4.250 V | 4.250 V | 2.300 V | 2.600 V | 1.0 s | 4.0 s | 1.0 s | Active "L" |
| S-8259AAK-M6T1U | 4.375 V | 4.375 V | 2.800 V | 3.000 V | 1.0 s | 4.0 s | 1.0 s | Active "L" |
| S-8259AAL-M6T1U | 3.475 V | 3.475 V | 2.800 V | 2.880 V | 256 ms | 64 ms | 32 ms | Active "H" |
| S-8259AAM-M6T1U | 4.050 V | 4.050 V | 2.500 V | 3.000 V | 128 ms | 32 ms | 128 ms | Active "L" |
| S-8259AAN-M6T1U | 3.600 V | 3.600 V | 2.900 V | 2.980 V | 256 ms | 64 ms | 32 ms | Active "H" |
| S-8259AAO-M6T1U | 4.200 V | 4.200 V | 3.300 V | 3.400 V | 256 ms | 64 ms | 32 ms | Active "H" |
| S-8259AAP-M6T1U | 4.250 V | 4.150 V | 2.800 V | 3.000 V | 1.0 s | 128 ms | 128 ms | Active "L" |
| S-8259AAQ-M6T1U | 4.170 V | 3.770 V | 2.800 V | 3.400 V | 1.0 s | 1.0 s | 256 ms | Active "L" |

*1. CO pin output logic active "H" / active "L" is selectable.

Remark 1. Please contact our sales office for the products with detection voltage value other than those specified above.

2. The delay times can be changed within the range listed in **Table 3**. For details, please contact our sales office.

Table 3

| Delay Time | Symbol | Selection Range | | | | | | Remark |
|------------------------------------|-----------------|-----------------|--------|--------|--------|-------|-------|-------------------------------|
| Overcharge detection delay time | t _{CU} | 128 ms | 256 ms | 512 ms | 1.0 s | 2.0 s | 4.0 s | Select a value from the left. |
| Overcharge release delay time | t _{CL} | 32 ms | 64 ms | 128 ms | 1.0 s | 2.0 s | 4.0 s | Select a value from the left. |
| overdischarge detection delay time | t _{DL} | 32 ms | 64 ms | 128 ms | 256 ms | – | – | Select a value from the left. |

■ **Pin Configuration**

1. SOT-23-6

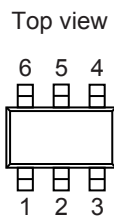


Figure 3

Table 4

| Pin No. | Symbol | Description |
|---------|------------------|--|
| 1 | DO | Output pin for overdischarge detection (CMOS output) |
| 2 | VM | Negative power supply input pin for CO pin |
| 3 | CO | Output pin for overcharge detection (CMOS output) |
| 4 | NC ^{*1} | No connection |
| 5 | VDD | Input pin for positive power supply |
| 6 | VSS | Input pin for negative power supply |

*1. The NC pin is electrically open.
 The NC pin can be connected to VDD pin or VSS pin.

■ **Absolute Maximum Ratings**

Table 5

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Applied Pin | Absolute Maximum Rating | Unit |
|---|-----------|-------------|----------------------------------|------|
| Input voltage between VDD pin and VSS pin | V_{DS} | VDD | $V_{SS} - 0.3$ to $V_{SS} + 6$ | V |
| VM pin input voltage | V_{VM} | VM | $V_{DD} - 28$ to $V_{DD} + 0.3$ | V |
| DO pin output voltage | V_{DO} | DO | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| CO pin output voltage | V_{CO} | CO | $V_{VM} - 0.3$ to $V_{DD} + 0.3$ | V |
| Power dissipation | P_D | – | 650*1 | mW |
| Operation ambient temperature | T_{opr} | – | –40 to +85 | °C |
| Storage temperature | T_{stg} | – | –55 to +125 | °C |

*1. When mounted on board
[Mounted board]

- (1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
- (2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

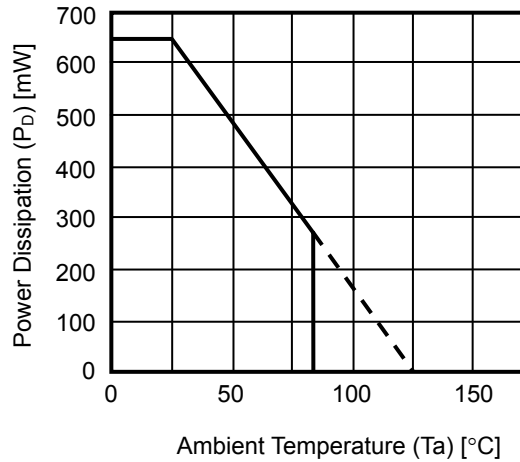


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ **Electrical Characteristics**

1. **Ta = +25°C**

Table 6

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|-------------------|--|-------------------------|-----------------|-------------------------|------|--------------|
| Detection Voltage | | | | | | | |
| Overcharge detection voltage | V _{CU} | – | V _{CU} – 0.020 | V _{CU} | V _{CU} + 0.020 | V | 1 |
| | | Ta = –10°C ~ +60°C*1 | V _{CU} – 0.025 | V _{CU} | V _{CU} + 0.025 | V | 1 |
| Overcharge release voltage | V _{CL} | V _{CL} ≠ V _{CU} | V _{CL} – 0.050 | V _{CL} | V _{CL} + 0.050 | V | 1 |
| | | V _{CL} = V _{CU} | V _{CL} – 0.025 | V _{CL} | V _{CL} + 0.020 | V | 1 |
| Overdischarge detection voltage | V _{DL} | – | V _{DL} – 0.050 | V _{DL} | V _{DL} + 0.050 | V | 2 |
| Overdischarge release voltage | V _{DU} | V _{DL} ≠ V _{DU} | V _{DU} – 0.100 | V _{DU} | V _{DU} + 0.100 | V | 2 |
| Input Voltage | | | | | | | |
| Operation voltage between VDD pin and VSS pin | V _{DSOP} | – | 1.5 | – | 6.0 | V | – |
| Input Current | | | | | | | |
| Current consumption during operation | I _{OPe} | V _{DD} = 3.4 V, V _{VM} = 0 V | – | 1.5 | 3.0 | μA | 3 |
| Current consumption during overdischarge | I _{OPeD} | V _{DD} = 1.5 V, V _{VM} = 0 V | – | – | 2.0 | μA | 3 |
| Output Resistance | | | | | | | |
| CO pin resistance "H" 1 | R _{COH1} | – | 5 | 10 | 20 | kΩ | 4 |
| CO pin resistance "L" 1 | R _{COL1} | – | 5 | 10 | 20 | kΩ | 4 |
| DO pin resistance "H" | R _{DOH} | – | 5 | 10 | 20 | kΩ | 4 |
| DO pin resistance "L" | R _{DOL} | – | 5 | 10 | 20 | kΩ | 4 |
| CO pin resistance "H" 2 | R _{COH2} | Active "L" | 1 | 4 | – | MΩ | 4 |
| CO pin resistance "L" 2 | R _{COL2} | Active "H" | 1 | 4 | – | MΩ | 4 |
| Delay Time | | | | | | | |
| Overcharge detection delay time | t _{CU} | – | t _{CU} × 0.7 | t _{CU} | t _{CU} × 1.3 | – | 5 |
| Overcharge release delay time | t _{CL} | – | t _{CL} × 0.7 | t _{CL} | t _{CL} × 1.3 | – | 5 |
| Overdischarge detection delay time | t _{DL} | – | t _{DL} × 0.7 | t _{DL} | t _{DL} × 1.3 | – | 5 |

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

BATTERY MONITORING IC FOR 1-CELL PACK
S-8259A Series

Rev.1.1_01

2. Ta = -40°C to +85°C*1

Table 7

(Ta = -40°C to +85°C*1 unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|-------------------|--|-------------------------|-----------------|-------------------------|------|--------------|
| Detection Voltage | | | | | | | |
| Overcharge detection voltage | V _{CU} | – | V _{CU} – 0.045 | V _{CU} | V _{CU} + 0.030 | V | 1 |
| Overcharge release voltage | V _{CL} | V _{CL} ≠ V _{CU} | V _{CL} – 0.080 | V _{CL} | V _{CL} + 0.060 | V | 1 |
| | | V _{CL} = V _{CU} | V _{CL} – 0.050 | V _{CL} | V _{CL} + 0.030 | V | 1 |
| Overdischarge detection voltage | V _{DL} | – | V _{DL} – 0.080 | V _{DL} | V _{DL} + 0.060 | V | 2 |
| Overdischarge release voltage | V _{DU} | V _{DL} ≠ V _{DU} | V _{DU} – 0.130 | V _{DU} | V _{DU} + 0.110 | V | 2 |
| Input Voltage | | | | | | | |
| Operation voltage between VDD pin and VSS pin | V _{DSOP} | – | 1.5 | – | 6.0 | V | – |
| Input Current | | | | | | | |
| Current consumption during operation | I _{OPE} | V _{DD} = 3.4 V, V _{VM} = 0 V | – | 1.5 | 4.0 | μA | 3 |
| Current consumption during overdischarge | I _{OPEd} | V _{DD} = 1.5 V, V _{VM} = 0 V | – | – | 3.0 | μA | 3 |
| Output Resistance | | | | | | | |
| CO pin resistance "H" 1 | R _{COH1} | – | 2.5 | 10 | 30 | kΩ | 4 |
| CO pin resistance "L" 1 | R _{COL1} | – | 2.5 | 10 | 30 | kΩ | 4 |
| DO pin resistance "H" | R _{DOH} | – | 2.5 | 10 | 30 | kΩ | 4 |
| DO pin resistance "L" | R _{DOL} | – | 2.5 | 10 | 30 | kΩ | 4 |
| CO pin resistance "H" 2 | R _{COH2} | Active "L" | 0.5 | 4 | – | MΩ | 4 |
| CO pin resistance "L" 2 | R _{COL2} | Active "H" | 0.5 | 4 | – | MΩ | 4 |
| Delay Time | | | | | | | |
| Overcharge detection delay time | t _{CU} | – | t _{CU} × 0.5 | t _{CU} | t _{CU} × 2.5 | – | 5 |
| Overcharge release delay time | t _{CL} | – | t _{CL} × 0.5 | t _{CL} | t _{CL} × 2.5 | – | 5 |
| Overdischarge detection delay time | t _{DL} | – | t _{DL} × 0.5 | t _{DL} | t _{DL} × 2.5 | – | 5 |

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) are judged by $V_{VM} + 1.0$ V, and the output voltage levels "H" and "L" at DO pin (V_{DO}) are judged by $V_{SS} + 1.0$ V. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS} .

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

1.1 Active "H"

Overcharge detection voltage (V_{CU}) is defined as the voltage V_1 at which V_{CO} goes from "L" to "H" when the voltage V_1 is gradually increased from the starting condition of $V_1 = 3.4$ V. Overcharge release voltage (V_{CL}) is defined as the voltage V_1 at which V_{CO} goes from "H" to "L" when the voltage V_1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL} .

1.2 Active "L"

Overcharge detection voltage (V_{CU}) is defined as the voltage V_1 at which V_{CO} goes from "H" to "L" when the voltage V_1 is gradually increased from the starting condition of $V_1 = 3.4$ V. Overcharge release voltage (V_{CL}) is defined as the voltage V_1 at which V_{CO} goes from "L" to "H" when the voltage V_1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL} .

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage V_1 at which V_{DO} goes from "H" to "L" when the voltage V_1 is gradually decreased from the starting condition of $V_1 = 3.4$ V. Overdischarge release voltage (V_{DU}) is defined as the voltage V_1 at which V_{DO} goes from "L" to "H" when the voltage V_1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between V_{DU} and V_{DL} .

3. Current consumption during operation (Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through VDD pin (I_{DD}) under the set condition of $V_1 = 3.4$ V.

4. Current consumption during overdischarge (Test circuit 3)

The current consumption during overdischarge (I_{OPED}) is I_{DD} under the set condition of $V_1 = 1.5$ V.

5. CO pin resistance "H" 1 (Test circuit 4)

5.1 Active "H"

The CO pin resistance "H" 1 (R_{COH1}) is the resistance between VDD pin and CO pin under the set conditions of $V_1 = 4.7$ V, $V_2 = 4.3$ V.

5.2 Active "L"

The CO pin resistance "H" 1 (R_{COH1}) is the resistance between VDD pin and CO pin under the set conditions of $V_1 = 3.4$ V, $V_2 = 3.0$ V.

6. CO pin resistance "L" 1 (Test circuit 4)

6.1 Active "H"

The CO pin resistance "L" 1 (R_{COL1}) is the resistance between VM pin and CO pin under the set conditions of $V_1 = 3.4$ V, $V_2 = 0.4$ V.

6.2 Active "L"

The CO pin resistance "L" 1 (R_{COL1}) is the resistance between VM pin and CO pin under the set conditions of $V_1 = 4.7$ V, $V_2 = 0.4$ V.

7. DO pin resistance "H"
(Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of $V1 = 3.4\text{ V}$, $V3 = 3.0\text{ V}$.

8. DO pin resistance "L"
(Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of $V1 = 1.8\text{ V}$, $V3 = 0.4\text{ V}$.

9. CO pin resistance "H" 2 (Active "L")
(Test circuit 4)

The CO pin resistance "H" 2 (R_{COH2}) is the resistance between VDD pin and CO pin under the set conditions of $V1 = 4.7\text{ V}$, $V2 = 0\text{ V}$.

10. CO pin resistance "L" 2 (Active "H")
(Test circuit 4)

The CO pin resistance "L" 2 (R_{COL2}) is the resistance between VDD pin and CO pin under the set conditions of $V1 = 4.7\text{ V}$, $V2 = 4.7\text{ V}$.

11. Overcharge detection delay time
(Test circuit 5)

11.1 Active "H"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "H" just after the voltage $V1$ increases and exceeds V_{CU} under the set condition of $V1 = 3.4\text{ V}$.

11.2 Active "L"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "L" just after the voltage $V1$ increases and exceeds V_{CU} under the set condition of $V1 = 3.4\text{ V}$.

12. Overcharge release delay time
(Test circuit 5)

12.1 Active "H"

The overcharge release delay time (t_{CL}) is the time needed for V_{CO} to go to "L" just after the voltage $V1$ decreases and falls below V_{CL} under the set condition of $V1 = 4.7\text{ V}$.

12.2 Active "L"

The overcharge release delay time (t_{CL}) is the time needed for V_{CO} to go to "H" just after the voltage $V1$ decreases and falls below V_{CL} under the set condition of $V1 = 4.7\text{ V}$.

13. Overdischarge detection delay time
(Test circuit 5)

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to go to "L" after the voltage $V1$ decreases and falls below V_{DL} under the set condition of $V1 = 3.4\text{ V}$.

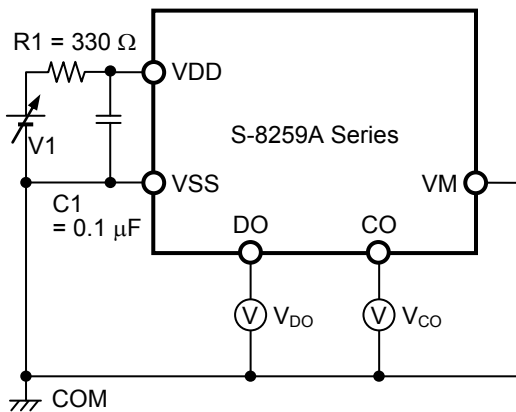


Figure 5 Test Circuit 1

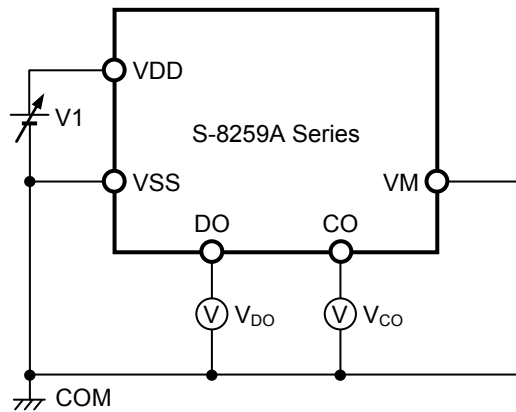


Figure 6 Test Circuit 2

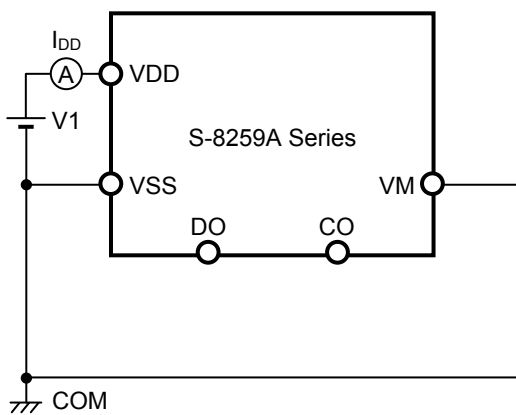


Figure 7 Test Circuit 3

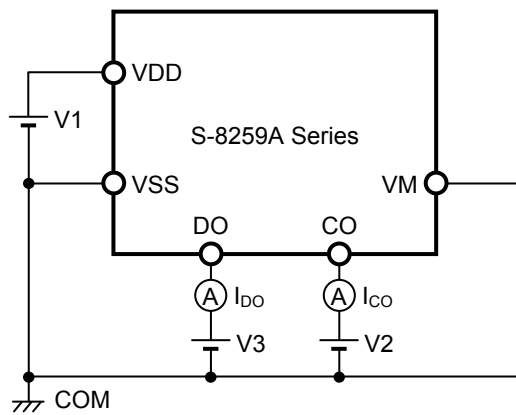


Figure 8 Test Circuit 4

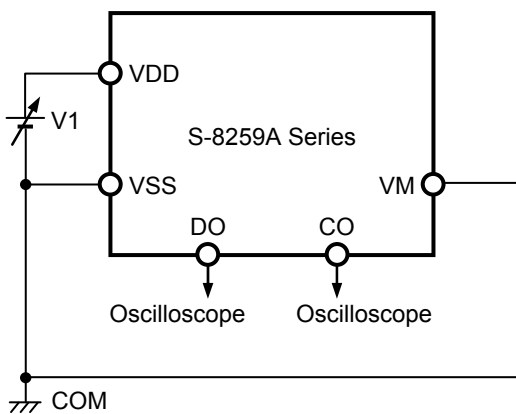


Figure 9 Test Circuit 5

■ Operation

Remark Refer to "■ Connection Example".

1. Normal status

The S-8259A Series monitors the voltage of the battery connected between VDD pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to overcharge detection voltage (V_{CU}), CO pin and DO pin both output the release signals. This condition is called the normal status.

2. Overcharge status

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, CO pin outputs the overcharge detection signal. This condition is called the overcharge status.

When the battery voltage falls below the overcharge release voltage (V_{CL}) and the condition continues for the overcharge release delay time (t_{CL}) or longer, the S-8259A Series releases the overcharge status.

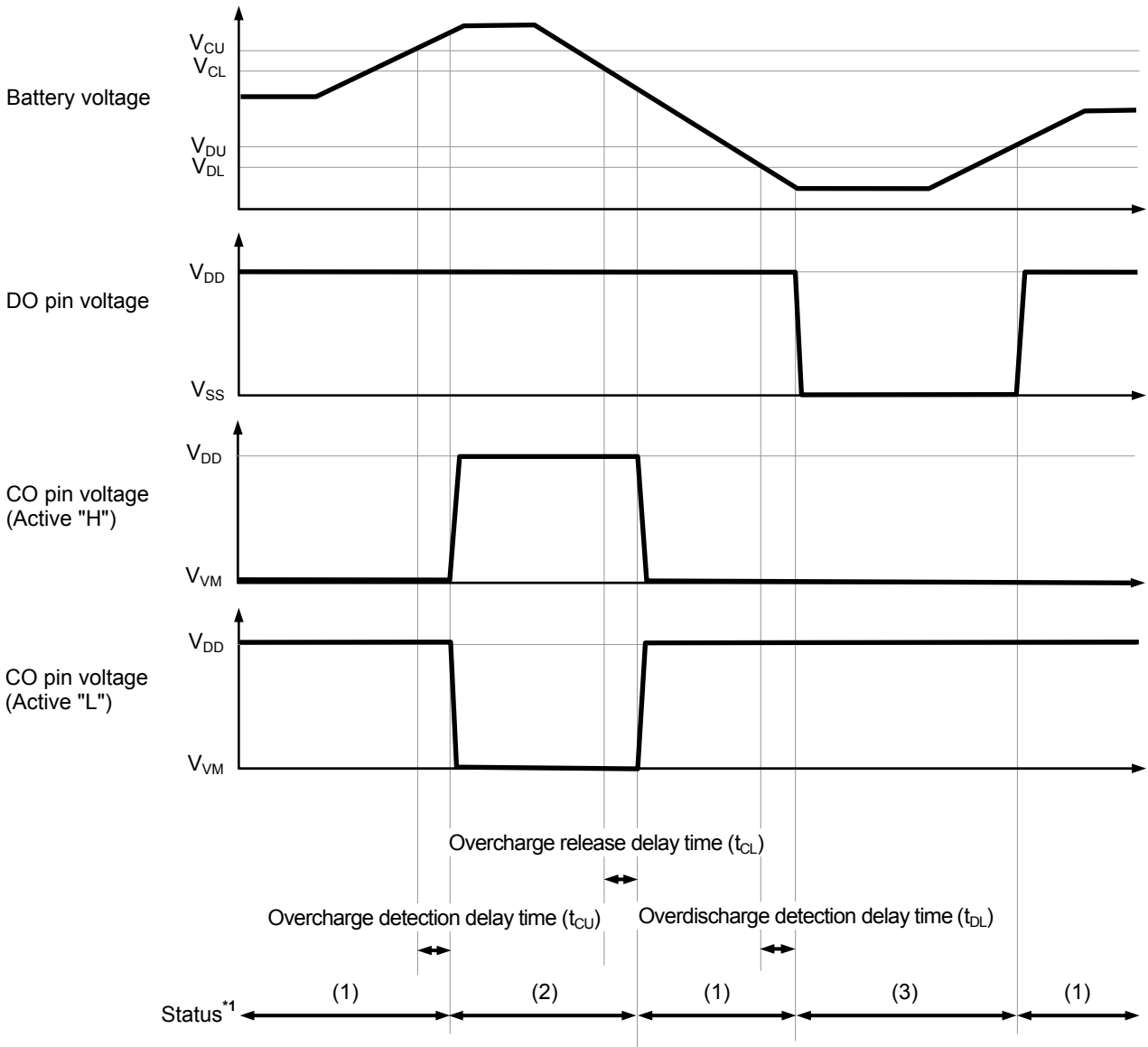
3. Overdischarge status

When the battery voltage falls below V_{DL} during discharging in the normal status and the condition continues for the overdischarge detection delay time (t_{DL}) or longer, DO pin outputs the overdischarge detection signal. This condition is called the overdischarge status.

When the battery voltage exceeds the overdischarge release voltage (V_{DU}), the S-8259A Series releases the overdischarge status.

■ **Timing Chart**

1. Overcharge detection, overdischarge detection



*1. (1): Normal status
 (2): Overcharge status
 (3): Overdischarge status

Figure 10

■ Connection Example

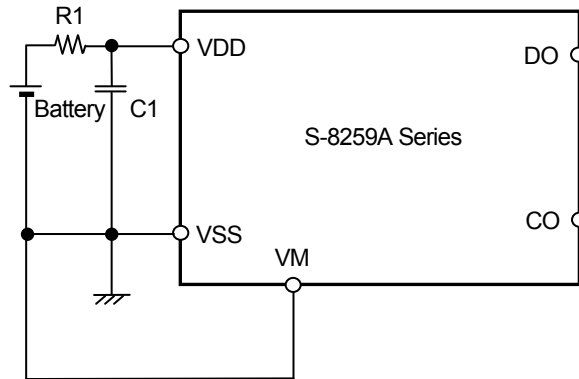


Figure 11

Table 8 Constants for External Components

| Symbol | Part | Purpose | Min. | Typ. | Max. | Remark |
|--------|-----------|--|---------------------|-------------------|-------------------|--------|
| R1 | Resistor | ESD protection, For power fluctuation | 150 Ω | 330 Ω | 1 k Ω | - |
| C1 | Capacitor | For power fluctuation | 0.068 μF | 0.1 μF | 1.0 μF | - |

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

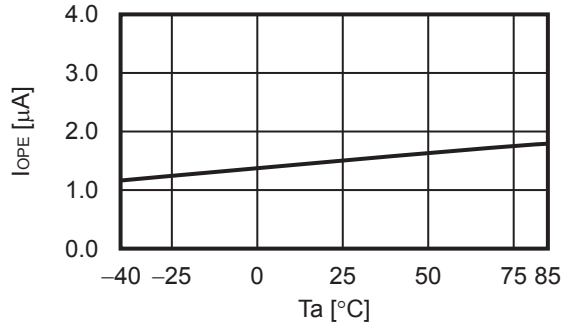
■ **Precautions**

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

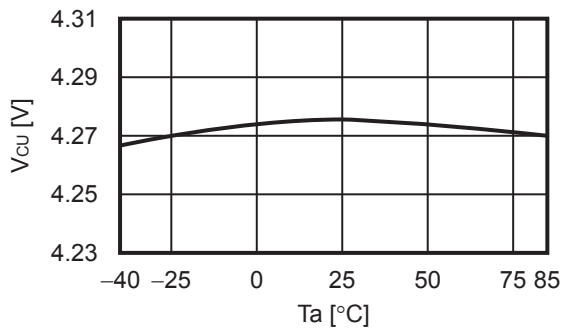
1. Current consumption

1.1 I_{OPE} vs. T_a

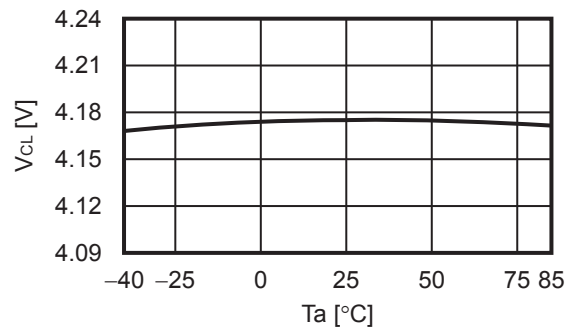


2. Detection voltage

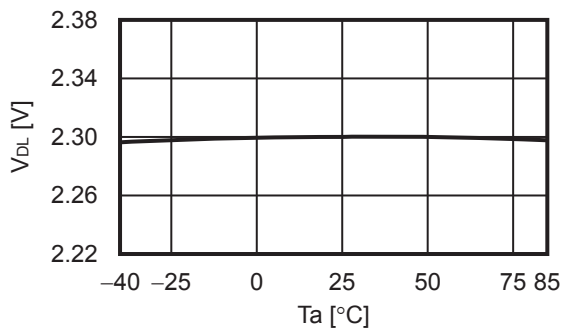
2.1 V_{CU} vs. T_a



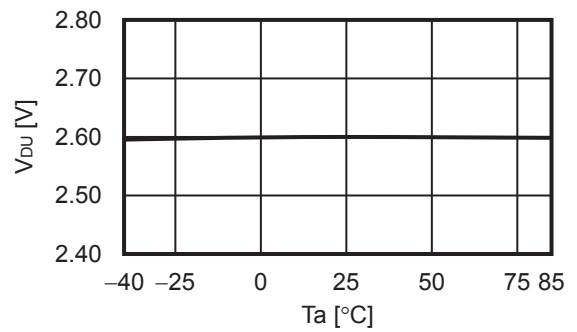
2.2 V_{CL} vs. T_a



2.3 V_{DL} vs. T_a

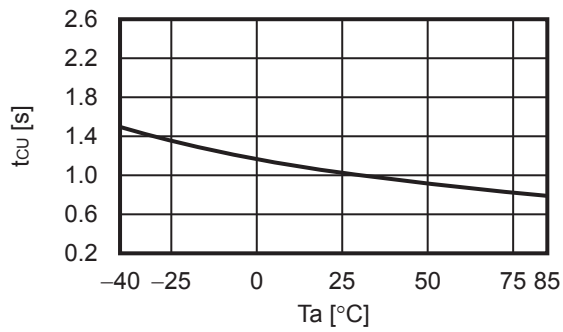


2.4 V_{DU} vs. T_a

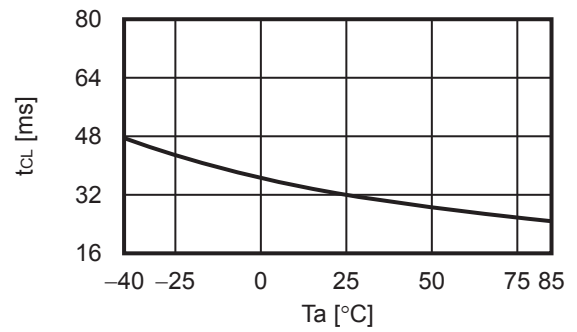


3. Delay time

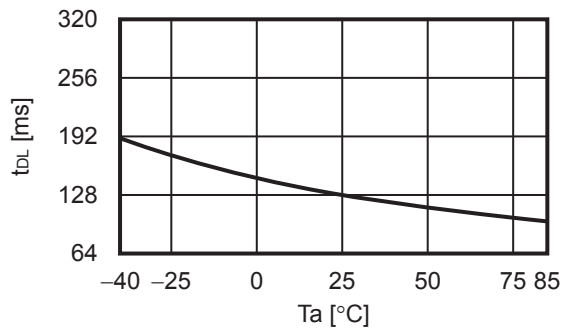
3.1 t_{CU} vs. T_a



3.2 t_{CL} vs. T_a

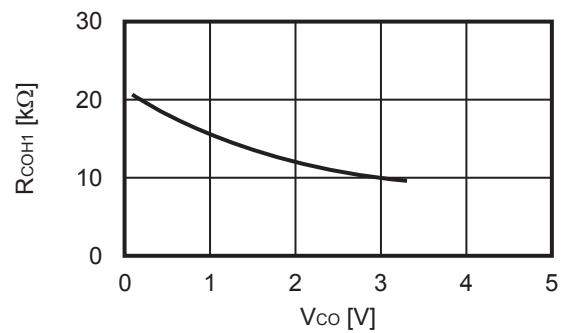


3.3 t_{DL} vs. T_a

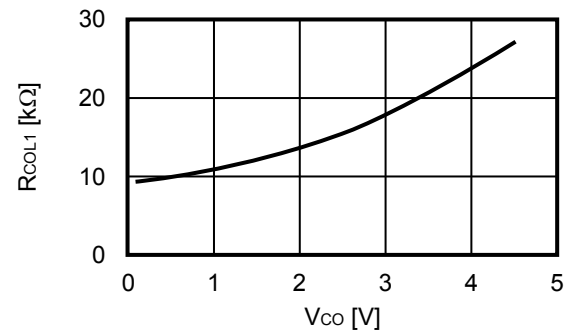


4. Output resistance

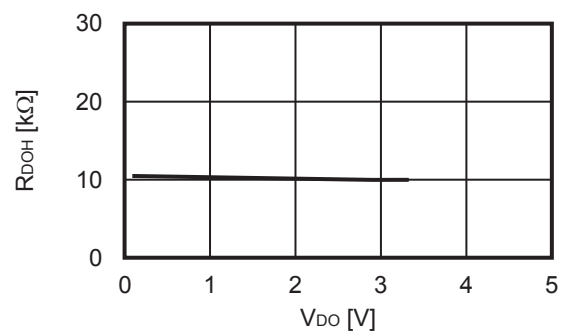
4.1 R_{COH1} vs. V_{CO}



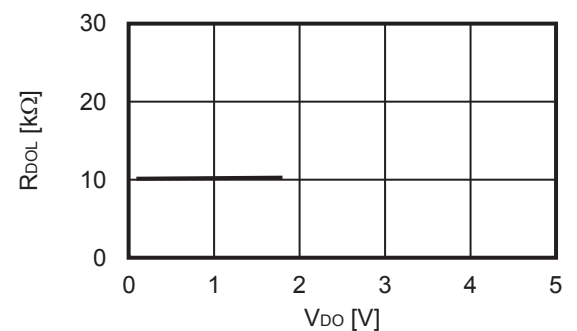
4.2 R_{COL1} vs. V_{CO}



4.3 R_{DOH} vs. V_{DO}

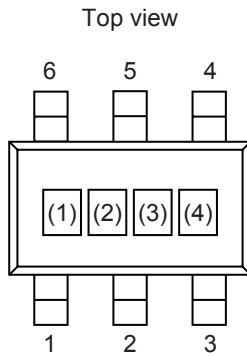


4.4 R_{DOL} vs. V_{DO}



■ **Marking Specifications**

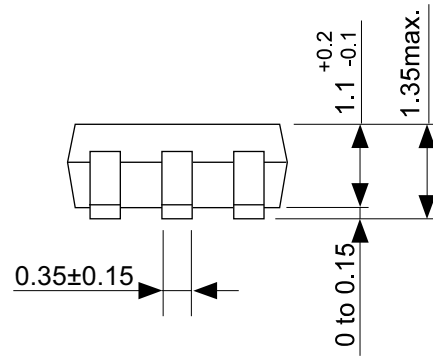
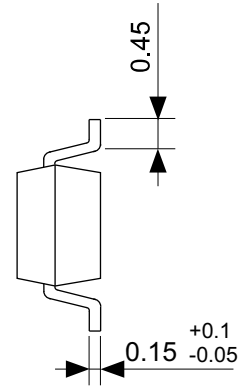
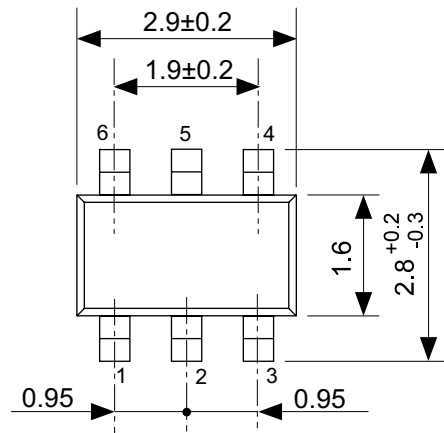
1. **SOT-23-6**



(1) to (3): Product code (refer to **Product name vs. Product code**)
(4): Lot number

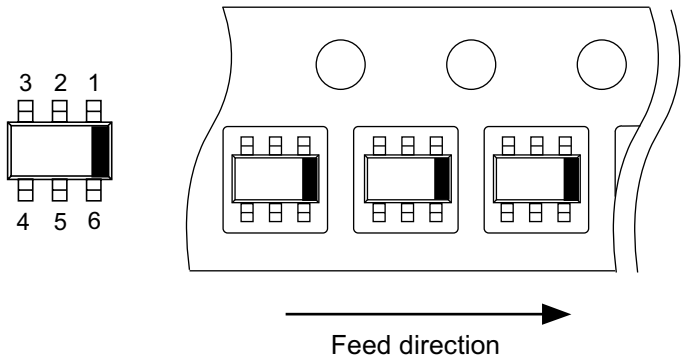
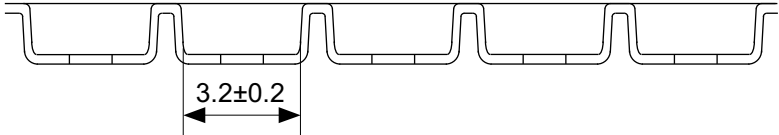
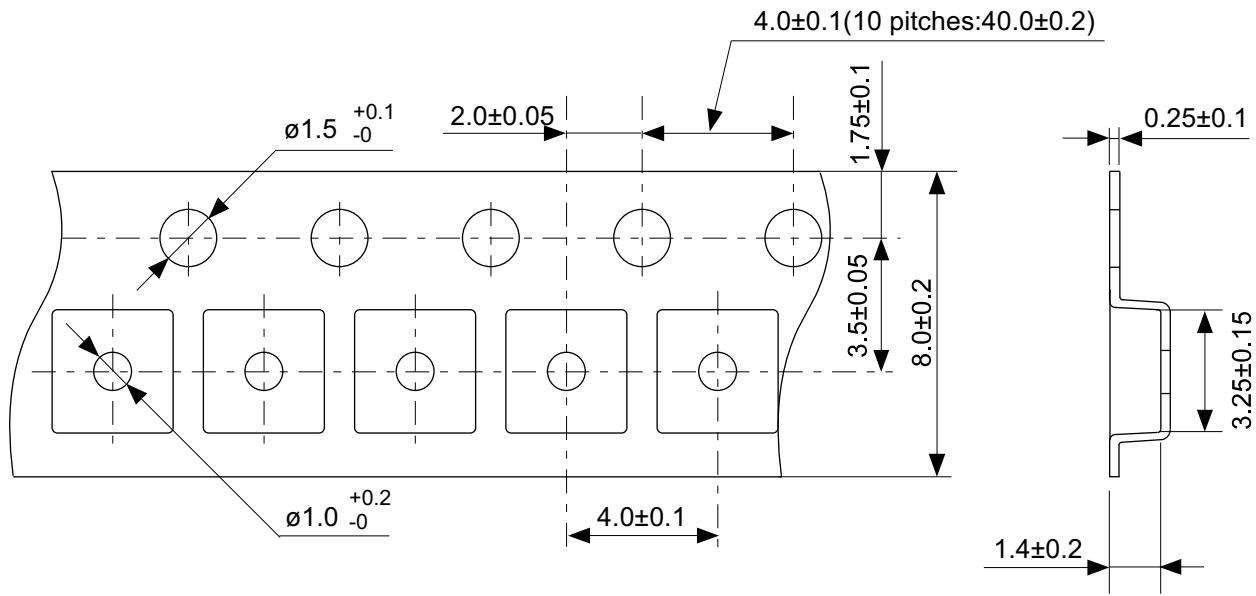
Product name vs. Product code

| Product Name | Product Code | | |
|-----------------|--------------|-----|-----|
| | (1) | (2) | (3) |
| S-8259AAA-M6T1U | H | 5 | A |
| S-8259AAB-M6T1U | H | 5 | B |
| S-8259AAC-M6T1U | H | 5 | C |
| S-8259AAD-M6T1U | H | 5 | D |
| S-8259AAE-M6T1U | H | 5 | E |
| S-8259AAG-M6T1U | H | 5 | G |
| S-8259AAH-M6T1U | H | 5 | H |
| S-8259AAI-M6T1U | H | 5 | I |
| S-8259AAJ-M6T1U | H | 5 | J |
| S-8259AAK-M6T1U | H | 5 | K |
| S-8259AAL-M6T1U | H | 5 | L |
| S-8259AAM-M6T1U | H | 5 | M |
| S-8259AAN-M6T1U | H | 5 | N |
| S-8259AAO-M6T1U | H | 5 | O |
| S-8259AAP-M6T1U | H | 5 | P |
| S-8259AAQ-M6T1U | H | 5 | Q |



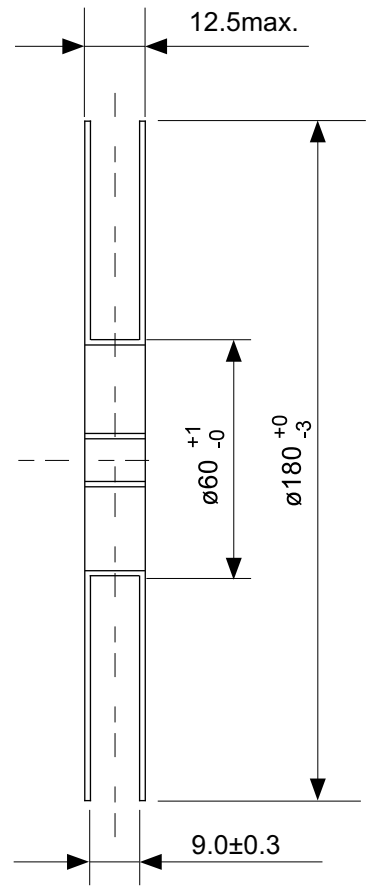
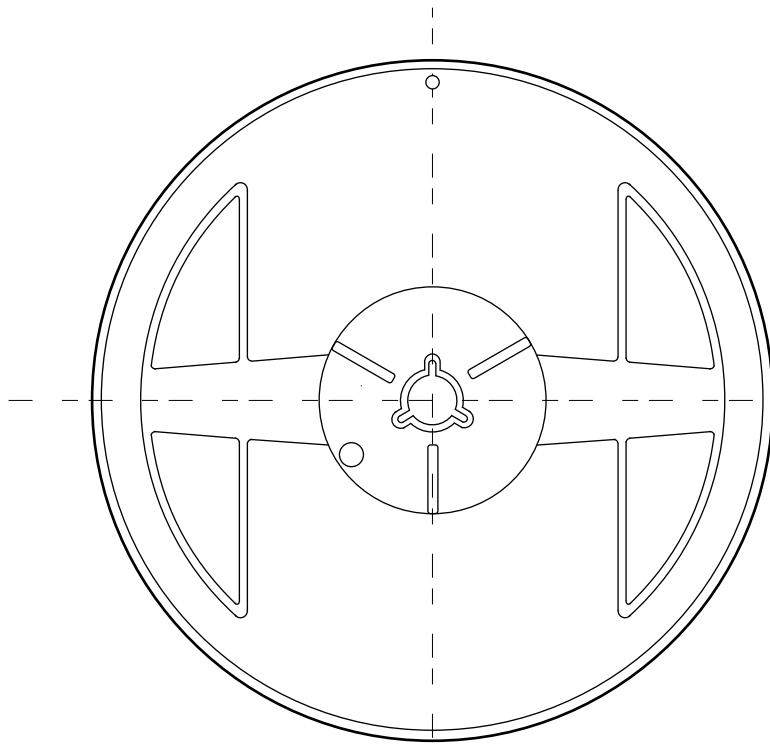
No. MP006-A-P-SD-2.1

| | |
|-------------------|-------------------------|
| TITLE | SOT236-A-PKG Dimensions |
| No. | MP006-A-P-SD-2.1 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |

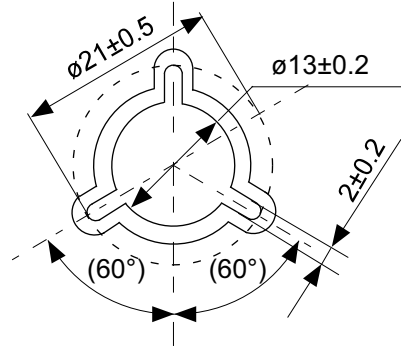


No. MP006-A-C-SD-3.1

| | |
|-------------------|-----------------------|
| TITLE | SOT236-A-Carrier Tape |
| No. | MP006-A-C-SD-3.1 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |



Enlarged drawing in the central part



No. MP006-A-R-SD-2.1

| | | | |
|-------------------|------------------|-----|-------|
| TITLE | SOT236-A-Reel | | |
| No. | MP006-A-R-SD-2.1 | | |
| ANGLE | | QTY | 3,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |

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