

The S-8426A Series is a CMOS IC designed for use in the switching circuits of primary and backup power supplies on a single chip. It consists of two voltage regulators, three voltage detectors, a power supply switch and its controller, as well as other functions.

In addition to the switching function between the primary and backup power supply, the S-8426A Series can provide the micro controllers with three types of voltage detection output signals corresponding to the power supply voltage.

Moreover adopting a special sequence for switch control enables the effective use of the backup power supply, making this IC ideal for configuring a backup system.

■ Features

- Low power consumption
 - Normal operation: 15 μ A Max. ($V_{IN} = 6$ V)
 - Backup: 4.5 μ A Max.
- Voltage regulator
 - Output voltage tolerance : $\pm 2\%$
 - Output voltage: Independently selectable in 0.1 V steps in the range of 2.3 to 5.4 V
- Three built-in voltage detectors (CS, PREEND, RESET)
 - Detection voltage precision: $\pm 2\%$
 - Detection voltage: Selectable in 0.1 V steps in the range of 2.4 to 5.3 V (CS voltage detector)
Selectable in 0.1 V steps in the range of 1.7 to 3.4 V (PREEND, RESET voltage detector)
- Switching circuit for primary power supply and backup power supply configurable on one chip
- Efficient use of backup power supply possible
- Special sequence
 - Backup voltage is not output when the primary power supply voltage does not reach the initial voltage at which the switch unit operates.
- Lead-free, Sn 100%, halogen-free*1

*1. Refer to “■ Product Name Structure” for details.

■ Applications

- Video camera recorders
- Still video cameras
- Memory cards
- SRAM backup equipment

■ Packages

- 8-Pin TSSOP
- 8-Pin SOP(JEDEC)

■ **Block Diagram**

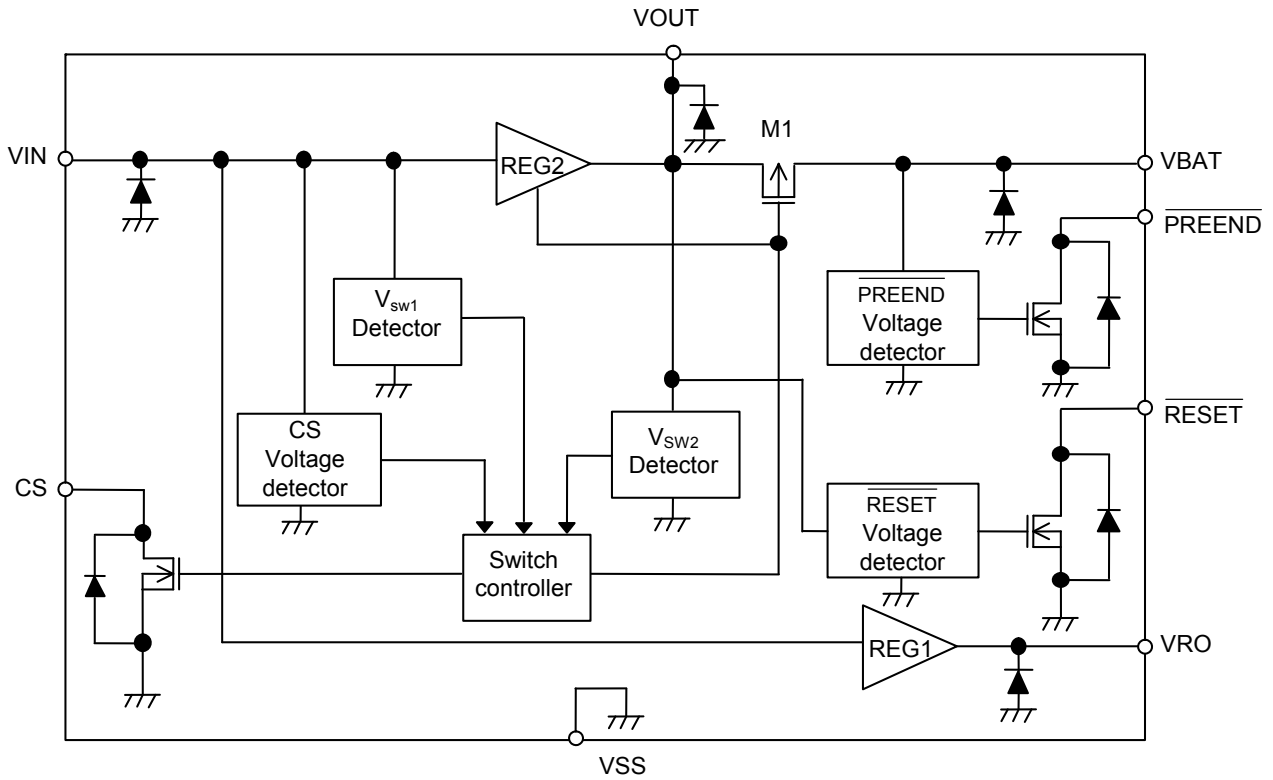
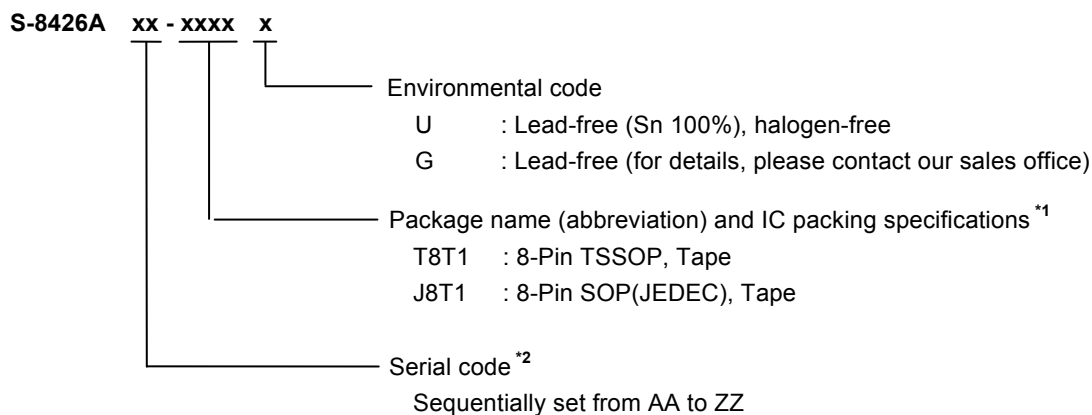


Figure 1

■ Product Name Structure

1. Product Name



*1. Refer to the taping specifications.

*2. Refer to the "3. Product Name List".

2. Package

| Package Name | | Drawing Code | | |
|------------------|------------------------|--------------|--------------|--------------|
| | | Package | Tape | Reel |
| 8-Pin TSSOP | Environmental code = G | FT008-A-P-SD | FT008-E-C-SD | FT008-E-R-SD |
| | Environmental code = U | FT008-A-P-SD | FT008-E-C-SD | FT008-E-R-S1 |
| 8-Pin SOP(JEDEC) | Environmental code = G | FJ008-A-P-SD | FJ008-D-C-SD | FJ008-D-R-SD |
| | Environmental code = U | FJ008-A-P-SD | FJ008-D-C-SD | FJ008-D-R-S1 |

3. Product Name List

Table 1

| Model No. | Output Voltage V_{RO} | Output Voltage V_{OUT} | CS Voltage $-V_{DET1}$ | CS Voltage $+V_{DET1}$ | RESET Voltage $-V_{DET2}$ | RESET Voltage $+V_{DET2}$ | PREEND Voltage $-V_{DET3}$ | PREEND Voltage $+V_{DET3}$ | Switch Voltage V_{SW1} |
|-----------------|----------------------------|-----------------------------|---------------------------|---------------------------|------------------------------|------------------------------|-------------------------------|-------------------------------|------------------------------|
| S-8426AAA-J8T1x | 5.000 | 5.000 | 4.500 | $+V_{OUT} \times 0.95$ | 2.900 | 3.068 | 2.100 | 2.207 | $+V_{DET4}^{*1} \times 0.77$ |

*1. $+V_{DET4}$ can be calculated by $-V_{DET1}$ with the following equation.

$$+V_{DET4} = (+V_{DET1}) + 15 \times \{(-V_{DET1}) - 0.8\} \div 372$$

Caution Set the CS voltage so that the switch voltage (V_{SW1}) is equal to or greater than the RESET detection voltage ($-V_{DET2}$).

Remark 1. The selection range is as follows.

V_{RO}, V_{OUT} : 2.3 to 5.4 V (0.1 V steps)

$-V_{DET1}$: 2.4 to 5.3 V (0.1 V steps)

$-V_{DET2}$: 1.7 to 3.4 V (0.1 V steps)

$-V_{DET3}$: 1.7 to 3.4 V (0.1 V steps)

2. V_{SW1} : $+V_{DET1} \times 0.85$ or $+V_{DET1} \times 0.77$

When $V_{SW2} > +V_{DET1}$, $+V_{DET4} \times 0.85$ or $+V_{DET4} \times 0.77$

3. If a product with a voltage other than above is required, contact our sales representative.

4. x: G or U

5. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ **Pin Configurations**

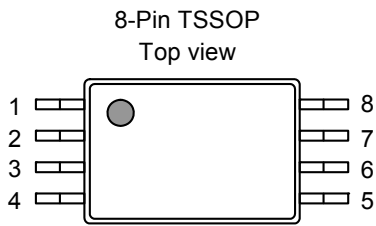


Figure 2

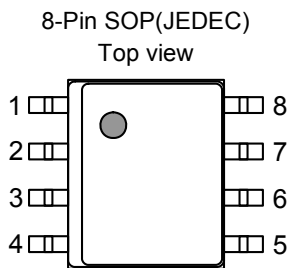


Figure 3

Table 2

| Pin No. | Symbol | Description |
|---------|--------|---------------------------------------|
| 1 | VSS | Ground |
| 2 | PREEND | Output pin of PREEND voltage detector |
| 3 | VBAT*1 | Backup power supply input pin |
| 4 | CS | Output pin of CS voltage detector |
| 5 | RESET | Output pin of RESET voltage detector |
| 6 | VOUT*1 | Output pin of voltage regulator 2 |
| 7 | VIN*1 | Primary power supply input pin |
| 8 | VRO*1 | Output pin of voltage regulator 1 |

*1. Mount capacitors between VSS (GND pin) and the VIN, VBAT, VOUT, and VRO pins. (Refer to the “■ Standard Circuit”)

Table 3

| Pin No. | Symbol | Description |
|---------|--------|---------------------------------------|
| 1 | VSS | Ground |
| 2 | PREEND | Output pin of PREEND voltage detector |
| 3 | VBAT*1 | Backup power supply input pin |
| 4 | CS | Output pin of CS voltage detector |
| 5 | RESET | Output pin of RESET voltage detector |
| 6 | VOUT*1 | Output pin of voltage regulator 2 |
| 7 | VIN*1 | Primary power supply input pin |
| 8 | VRO*1 | Output pin of voltage regulator 1 |

*1. Mount capacitors between VSS (GND pin) and the VIN, VBAT, VOUT, and VRO pins. (Refer to the “■ Standard Circuit”)

■ Absolute Maximum Ratings

Table 4

(Unless otherwise specified: Ta = 25 °C)

| Item | Symbol | Absolute Maximum Ratings | Unit |
|-------------------------------------|-------------------|------------------------------|------|
| Primary power supply input voltage | V_{IN} | $V_{SS}-0.3$ to $V_{SS}+18$ | V |
| Backup power supply input voltage | V_{BAT} | $V_{SS}-0.3$ to $V_{SS}+18$ | V |
| Output voltage of voltage regulator | V_{RO}, V_{OUT} | $V_{SS}-0.3$ to $V_{IN}+0.3$ | V |
| CS output voltage | V_{CS} | $V_{SS}-0.3$ to $V_{SS}+18$ | V |
| RESET output voltage | V_{RESET} | $V_{SS}-0.3$ to $V_{SS}+18$ | V |
| PREEND output voltage | V_{PREEND} | $V_{SS}-0.3$ to $V_{SS}+18$ | V |
| Power dissipation | 8-Pin TSSOP | 700^{*1} | mW |
| | 8-Pin SOP(JEDEC) | 850^{*1} | mW |
| Operating ambient temperature | T_{opr} | -40 to +85 | °C |
| Storage temperature | T_{stg} | -40 to +125 | °C |

*1. At mounted on printed circuit board
[Mounted board]

- (1) Board size: 114.3 mm × 76.2 mm × 1.6 mm
- (2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

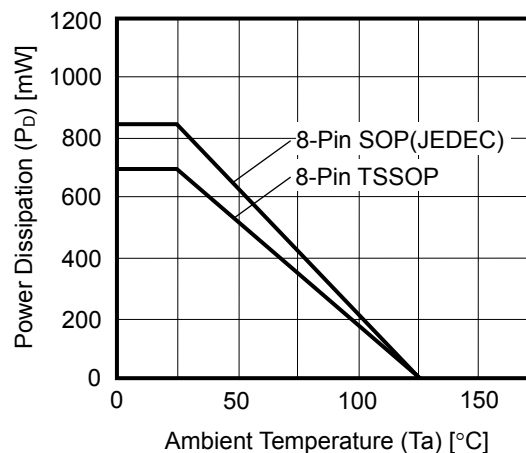


Figure 4 Power Dissipation of Package (Mounted on Printed Circuit Board)

■ **Electrical Characteristics**

1. S-8426AAA

Table 5 (1 / 2)

(Unless otherwise specified: Ta = 25 °C)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit | Test Circuit | |
|-------------------|-------------------------------------------|---------------------------------------------------------------|-------------------------------------------------------------|------------------------|------------------------|------------------------|--------------|---|
| Voltage regulator | Output voltage 1 | V_{RO} | $V_{IN} = 6\text{ V}, I_{RO} = 30\text{ mA}$ | 4.900 | 5.000 | 5.100 | V | 1 |
| | Dropout voltage 1 | V_{drop1} | $V_{IN} = 6\text{ V}, I_{RO} = 30\text{ mA}$ | – | 356 | 474 | mV | 1 |
| | Load stability 1 | ΔV_{RO1} | $V_{IN} = 6\text{ V}, I_{RO} = 0.1\text{ to }40\text{ mA}$ | – | 50 | 100 | mV | 1 |
| | Input stability 1 | ΔV_{RO2} | $V_{IN} = 6\text{ to }16\text{ V}, I_{RO} = 30\text{ mA}$ | – | 5 | 20 | mV | 1 |
| | Output voltage temperature coefficient 1 | $\frac{\Delta V_{RO}}{\Delta Ta \cdot V_{RO}}$ | Ta = –40 to +85 °C | – | ±100 | – | ppm/°C | 1 |
| | Output voltage 2 | V_{OUT} | $V_{IN} = 6\text{ V}, I_{OUT} = 50\text{ mA}$ | 4.900 | 5.000 | 5.100 | V | 1 |
| | Dropout voltage 2 | V_{drop2} | $V_{IN} = 6\text{ V}, I_{OUT} = 50\text{ mA}$ | – | 401 | 540 | mV | 1 |
| | Load stability 2 | ΔV_{OUT1} | $V_{IN} = 6\text{ V}, I_{OUT} = 0.1\text{ to }60\text{ mA}$ | – | 50 | 100 | mV | 1 |
| | Input stability 2 | ΔV_{OUT2} | $V_{IN} = 6\text{ to }16\text{ V}, I_{OUT} = 50\text{ mA}$ | – | 10 | 30 | mV | 1 |
| | Output voltage temperature coefficient 2 | $\frac{\Delta V_{OUT}}{\Delta Ta \cdot V_{OUT}}$ | Ta = –40 to +85 °C | – | ±100 | – | ppm/°C | 1 |
| | Primary power input voltage | V_{IN} | – | – | – | 16 | V | 1 |
| Voltage detector | CS detection voltage | $-V_{DET1}$ | V_{IN} voltage detection | 4.410 | 4.500 | 4.590 | V | 2 |
| | CS release voltage | $+V_{DET1}$ | – | $+V_{OUT} \times 0.93$ | $+V_{OUT} \times 0.95$ | $+V_{OUT} \times 0.97$ | V | 2 |
| | RESET detection voltage | $-V_{DET2}$ | V_{OUT} voltage detection | 2.842 | 2.900 | 2.958 | V | 2 |
| | RESET release voltage | $+V_{DET2}$ | – | 2.994 | 3.068 | 3.142 | V | 2 |
| | PREEND detection voltage | $-V_{DET3}$ | V_{BAT} voltage detection | 2.058 | 2.100 | 2.142 | V | 2 |
| | PREEND release voltage | $+V_{DET3}$ | – | 2.154 | 2.207 | 2.260 | V | 2 |
| | Operating voltage | V_{ODT} | V_{IN} or V_{BAT} | 1.7 | – | 16 | V | 2 |
| | Detection voltage temperature coefficient | $\frac{\Delta - V_{DET1}}{\Delta Ta \cdot -V_{DET1}}$ | Ta = –40 to +85 °C | – | ±100 | – | ppm/°C | 2 |
| | | $\frac{\Delta - V_{DET2}}{\Delta Ta \cdot -V_{DET2}}$ | Ta = –40 to +85 °C | – | ±100 | – | ppm/°C | 2 |
| | | $\frac{\Delta - V_{DET3}}{\Delta Ta \cdot -V_{DET3}}$ | Ta = –40 to +85 °C | – | ±100 | – | ppm/°C | 2 |
| Sink current | I_{SINK} | $V_{DS} = 0.5\text{ V},$ $V_{IN} = V_{BAT} = 2.0\text{ V}$ | RESET | 1.50 | 2.30 | – | mA | 3 |
| | | | PREEND | 1.50 | 2.30 | – | mA | 3 |
| | | | CS | 1.50 | 2.30 | – | mA | 3 |
| Leakage current | I_{LEAK} | $V_{DS} = 16\text{ V}, V_{IN} = 16\text{ V}$ | – | – | 0.1 | μA | 3 | |

Table 5 (2 / 2)

| Item | | Symbol | Conditions | Min. | Typ. | Max. | Unit | Test Circuit |
|-----------------------------------|---------------------------------------------------|--------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|--------------------------|---------------|
| Switch unit | Switch voltage | V_{SW1} | $V_{BAT} = 2.8\text{ V}$, V_{IN} voltage detection | $+V_{DET4}^{*1}$ $\times 0.75$ | $+V_{DET4}^{*1}$ $\times 0.77$ | $+V_{DET4}^{*1}$ $\times 0.79$ | V | 4 |
| | CS output inhibit voltage | V_{SW2} | $V_{BAT} = 3.0\text{ V}$, V_{OUT} voltage detection | V_{OUT} $\times 0.93$ | V_{OUT} $\times 0.95$ | V_{OUT} $\times 0.97$ | V | 5 |
| | V_{BAT} switch leakage current | I_{LEAK} | $V_{IN} = 6\text{ V}$, $V_{BAT} = 0\text{ V}$ | – | – | 0.1 | μA | 6 |
| | V_{BAT} switch resistance | R_{SW} | $V_{IN} = \text{Open}$, $V_{BAT} = 3.0\text{ V}$, $I_{OUT} = 10\text{ to }500\ \mu\text{A}$ | – | 30 | 60 | Ω | 7 |
| | Switch voltage temperature coefficient | $\frac{\Delta V_{SW1}}{\Delta Ta \cdot V_{SW1}}$ | $Ta = -40\text{ to }+85^\circ\text{C}$ | – | ± 100 | – | ppm/ $^\circ\text{C}$ | 4 |
| | CS output inhibit voltage temperature coefficient | $\frac{\Delta V_{SW2}}{\Delta Ta \cdot V_{SW2}}$ | $Ta = -40\text{ to }+85^\circ\text{C}$ | – | ± 100 | – | ppm/ $^\circ\text{C}$ | 5 |
| Total | Current consumption | I_{SS1} | $V_{IN} = 6\text{ V}$, $V_{BAT} = 3.0\text{ V}$, no load | – | 6 | 15 | μA | 8 |
| | | I_{SS2} | $V_{IN} = 16\text{ V}$, $V_{BAT} = 3.0\text{ V}$, no load | – | 7 | 20 | μA | 8 |
| | | I_{BAT1} | $V_{IN} = 6\text{ V}$, $V_{BAT} = 3.0\text{ V}$, no load | – | 0.5 | 3.5 | μA | 8 |
| | | I_{BAT2} | $V_{IN} = \text{Open}$, $V_{BAT} = 3.0\text{ V}$, no load | $Ta = 25^\circ\text{C}$ | – | 1.5 | 4.5 | μA |
| | $Ta = 85^\circ\text{C}$ | | | – | – | 5.0 | μA | 8 |
| Backup power supply input voltage | V_{BAT} | – | 1.7 | – | 4.0 | V | 7 | |

*1. $+V_{DET4}$ can be calculated by $-V_{DET1}$ with the following equation.

$$+V_{DET4} = (+V_{DET1}) + 15 \times \{(-V_{DET1}) - 0.8\} \div 372$$

Remark The number in the Test Circuit column corresponds to the circuit number in the “■ Test Circuits” section.

■ **Test Circuits**

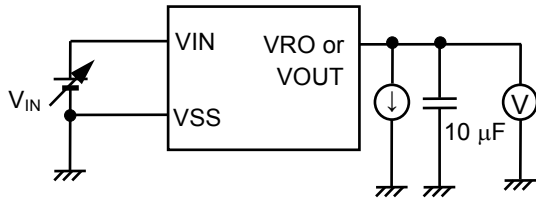
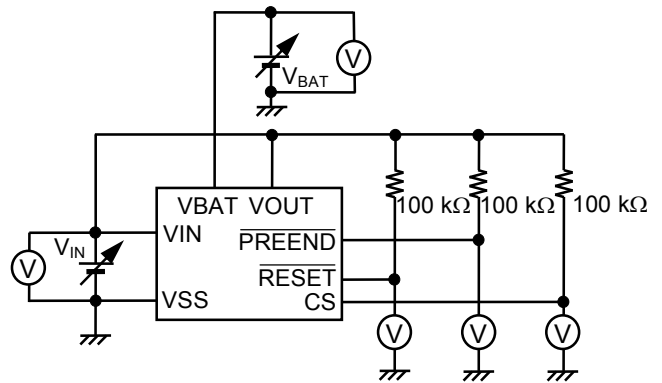


Figure 5 Test Circuit 1



To measure V_{DET3} , apply 6 V to V_{IN} .

Figure 6 Test Circuit 2

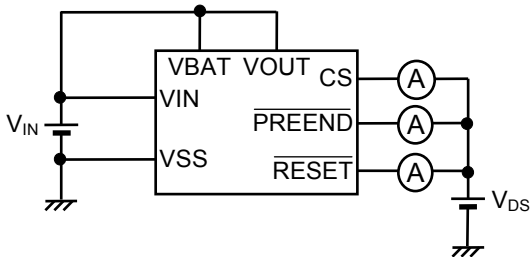
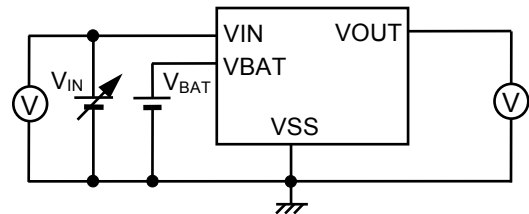


Figure 7 Test Circuit 3



Measure the value after applying 6 V to V_{IN} .

Figure 8 Test Circuit 4

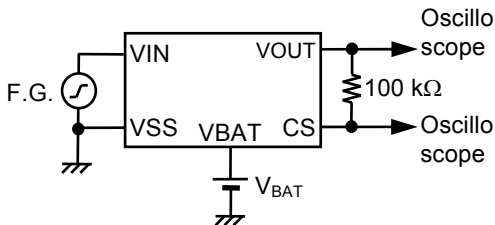


Figure 9 Test Circuit 5

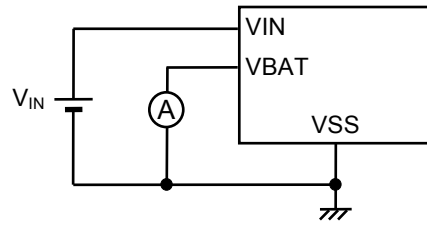
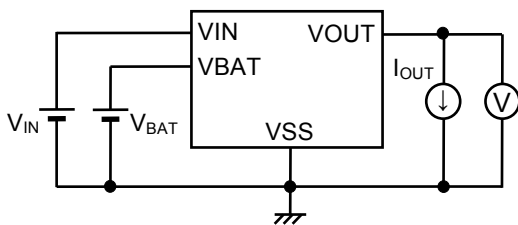
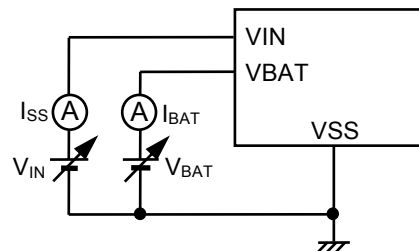


Figure 10 Test Circuit 6



Leave open and measure the value after applying 6 V to V_{IN} .

Figure 11 Test Circuit 7



To measure I_{BAT2} , apply 6 V to V_{IN} and then leave V_{IN} open and measure I_{BAT} .

Figure 12 Test Circuit 8

■ Operation

The internal configuration of the S-8426A Series is as follows.

- Voltage regulator 1, which stabilizes input voltage (V_{IN}) and outputs it to V_{RO}
- Voltage regulator 2, which stabilizes input voltage (V_{IN}) and outputs it to V_{OUT}
- CS voltage detector, which monitors input voltage (V_{IN})
- \overline{PREEND} voltage detector, which monitors output voltage (V_{BAT})
- \overline{RESET} voltage detector, which monitors output voltage (V_{OUT})
- Switch unit

The functions and operations of the above-listed elements are described below.

1. Voltage Regulators

The S-8426A Series features on-chip voltage regulators with a small dropout voltage. The voltage of the VRO and VOUT pins (the output pins of the voltage regulator) can separately be selected for the output voltage in 0.1 V steps between the range of 2.3 to 5.4 V.

1.1 Dropout voltage V_{drop1} , V_{drop2}

Assume that the voltage output from the VRO pin is $V_{RO(E)}$ under the conditions of output voltage 1 described in the electrical characteristics table. V_{IN1} is defined as the input voltage at which output voltage from the VRO pin becomes 98% of $V_{RO(E)}$ when the input voltage V_{IN} is decreased. Then, the dropout voltage V_{drop1} is calculated by the following expression.

$$V_{drop1} = V_{IN1} - V_{RO(E)} \times 0.98$$

Similarly, assume that the voltage of the VOUT pin is $V_{OUT(E)}$ under the conditions of output voltage 2 described in the electrical characteristics table. V_{IN2} is defined as the input voltage at which the output voltage from the VOUT pin becomes 98% of $V_{OUT(E)}$. Then, the dropout voltage V_{drop2} is calculated by the following expression.

$$V_{drop2} = V_{IN2} - V_{OUT(E)} \times 0.98$$

2. Voltage Detector

The S-8426A Series incorporates three high-precision, low power consuming voltage detectors with hysteresis characteristics. The power of the CS voltage detector is supplied from the VIN and VBAT pins. Therefore, the output is stable as long as the primary or backup power supplies are within the operating voltage range (1.7 to 16 V). All outputs are Nch open-drain, and need pull-up resistors of about 100 k Ω .

2.1 CS Voltage Detector

The CS voltage detector monitors the input voltage (V_{IN}) (VIN pin voltage). The detection voltage can be selected from between 2.4 and 5.3 V in 0.1 V steps. The result of detection is output at the CS pin: "Low" for lower voltage than the detection level and "High" for higher voltage than the release level (however, when the VOUT pin voltage is the CS output inhibit voltage (V_{SW2}), a low level is output).

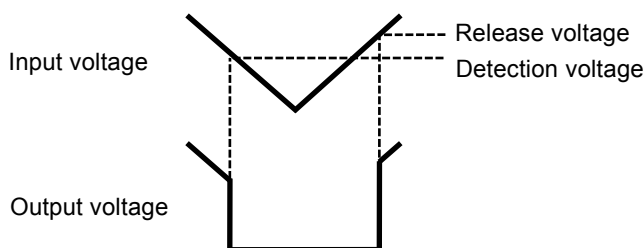


Figure 13 Definition of Detection and Release Voltages

2.2 $\overline{\text{PREEND}}$ Voltage Detector

The $\overline{\text{PREEND}}$ voltage detector monitors input voltage (V_{BAT}) (VBAT pin voltage). The detection voltage can be selected in the range of 1.7 to 3.4 V in 0.1 V step. By using this function, IC notifies if the backup battery is scarce. The result of detection is output at the $\overline{\text{PREEND}}$ pin: “Low” for lower voltages than the detection level and “High” for higher voltages than the release level.

2.3 $\overline{\text{RESET}}$ Voltage Detector

The $\overline{\text{RESET}}$ voltage detector monitors output voltage (V_{OUT}) (VOUT pin voltage). The detection voltage can be selected in the range of 1.7 to 3.4 V in 0.1 V step. The result of detection is output at the $\overline{\text{RESET}}$ pin: “Low” for lower voltages than the detection level and “High” for higher voltages than the release level. $\overline{\text{RESET}}$ outputs the normal logic if the VOUT pin voltage is 1.0 V or more.

Caution The $\overline{\text{PREEND}}$ and $\overline{\text{RESET}}$ voltage detectors use the different pins, respectively. Practically, the current is taken from the VBAT side, and consider the I/O voltage difference (V_{diff}) of M1 when M1 is ON.

3. Switch Unit

The switch unit consists of the V_{SW1} and V_{SW2} detectors, a switch controller, voltage regulator 2, and switch transistor M1 (Refer to **Figure 14**).

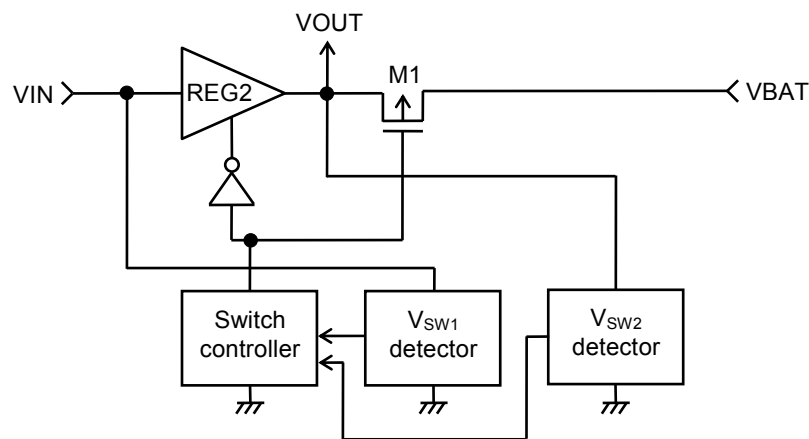


Figure 14

3.1 V_{SW1} Detector

The V_{SW1} detector monitors the power supply voltage V_{IN} and sends the results of detection to the switch controller. The detection voltage (V_{SW1}) can be set to $77 \pm 2\%$ or $85 \pm 2\%$ of the CS release voltage ($+V_{DET1}$).

In the products $V_{SW2} > +V_{DET1}$, the setting value is $77 \pm 2\%$ or $85 \pm 2\%$ of $+V_{DET4}$ which is calculated with the following equation.

$$+V_{DET4} = (-V_{DET1}) + 15 \times \{ (-V_{DET1}) - 0.8 \} \div 372$$

3.2 V_{SW2} Detector

The V_{SW2} detector monitors the VOUT pin voltage and keeps the CS release voltage output low until the VOUT pin voltage rises to V_{SW2} voltage. The CS pin output then changes from low to high if the VIN pin voltage is more than the CS release voltage ($+V_{DET1}$) when the VOUT pin voltage rises to $95 \pm 2\%$ of the output voltage of voltage regulator 2 (V_{OUT}). The CS pin output changes from high to low regardless of the V_{SW2} voltage when the VIN pin voltage drops to less than the CS detection voltage ($-V_{DET1}$).

The CS pin output remains high if the VIN pin voltage stays higher than the CS detection voltage ($-V_{DET1}$) when the VOUT pin voltage drops to less than the V_{SW2} voltage due to an undershoot.

3.3 Switch Controller

The switch controller controls voltage regulator 2 and switch transistor M1. There are two statuses corresponding to the power supply voltage (V_{IN}) (or power supply voltage (V_{BAT})) sequence: a special sequence status and a normal sequence status. When the power supply voltage (V_{IN}) rises and becomes equal to or exceeds the CS release voltage ($+V_{DET1}$), the normal sequence status is entered, but until then the special sequence status is maintained.

(1) Special sequence status

The switch controller sets voltage regulator 2 ON and switch transistor M1 OFF from the initial status until the primary power supply voltage (V_{IN}) is connected and reaches more than the CS release voltage ($+V_{DET1}$) in order to prevent consumption of the backup power supply regardless of the V_{SW1} detector status. This status is called the special sequence status.

(2) Normal sequence status

The switch controller enters the normal sequence status from the special sequence status once the primary power supply voltage (V_{IN}) reaches more than the CS release voltage ($+V_{DET1}$).

Once the normal sequence is entered, the switch controller switches voltage regulator 2 and switch transistor M1 ON/OFF as shown in **Table 6** according to the power supply voltage V_{IN} . The time required for voltage regulator 2 to be switched from OFF to ON is a few hundred μs at most. During this interval, voltage regulator 2 and switch transistor M1 may both switch OFF and the VOUT pin voltage may drop. To prevent this, connect a capacitor of 10 μF or more to the VOUT pin.

When the VOUT pin voltage becomes lower than the $\overline{\text{RESET}}$ detection voltage, the status returns to the special sequence status.

Table 6 ON/OFF Switching of Voltage Regulator 2 and Switch Transistor M1 According to Power Supply Voltage (V_{IN})

| Power Supply Voltage (V_{IN}) | Voltage Regulator 2 | Switch Transistor M1 | VOUT Pin Voltage |
|-----------------------------------|---------------------|----------------------|---------------------|
| $V_{IN} > V_{SW1}$ | ON | OFF | V_{OUT} |
| $V_{IN} < V_{SW1}$ | OFF | ON | $V_{BAT} - V_{dif}$ |

3.4 Switch Transistor M1

Voltage regulator 2 is also used to switch from VIN pin to VOUT pin. Therefore, no reverse current flows from VOUT pin to VIN pin when voltage regulator 2 is OFF. The output voltage of voltage regulator 2 can be selected from between 2.3 V and 5.4 V in 0.1 V steps.

The on-resistance of switch transistor M1 is 60 Ω or lower ($I_{OUT} = 10$ to 500 μA).

Therefore, when M1 is switched ON and VOUT pin is connected to VBAT pin, the voltage drop (V_{dif}) caused by M1 is $60 \times I_{OUT}$ (output current) at maximum., and $V_{BAT} - V_{dif}$ (max.) is output to the VOUT pin at minimum.

When voltage regulator 2 is ON and M1 is OFF, the leakage current of M1 is kept below 0.1 μA max. ($V_{IN} = 6$ V, $T_a = 25$ $^{\circ}\text{C}$) with the VBAT pin grounded (VSS pin).

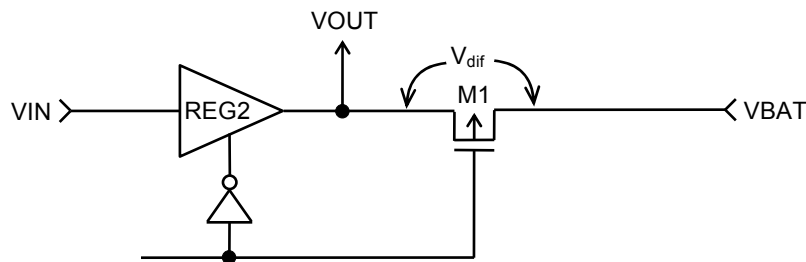
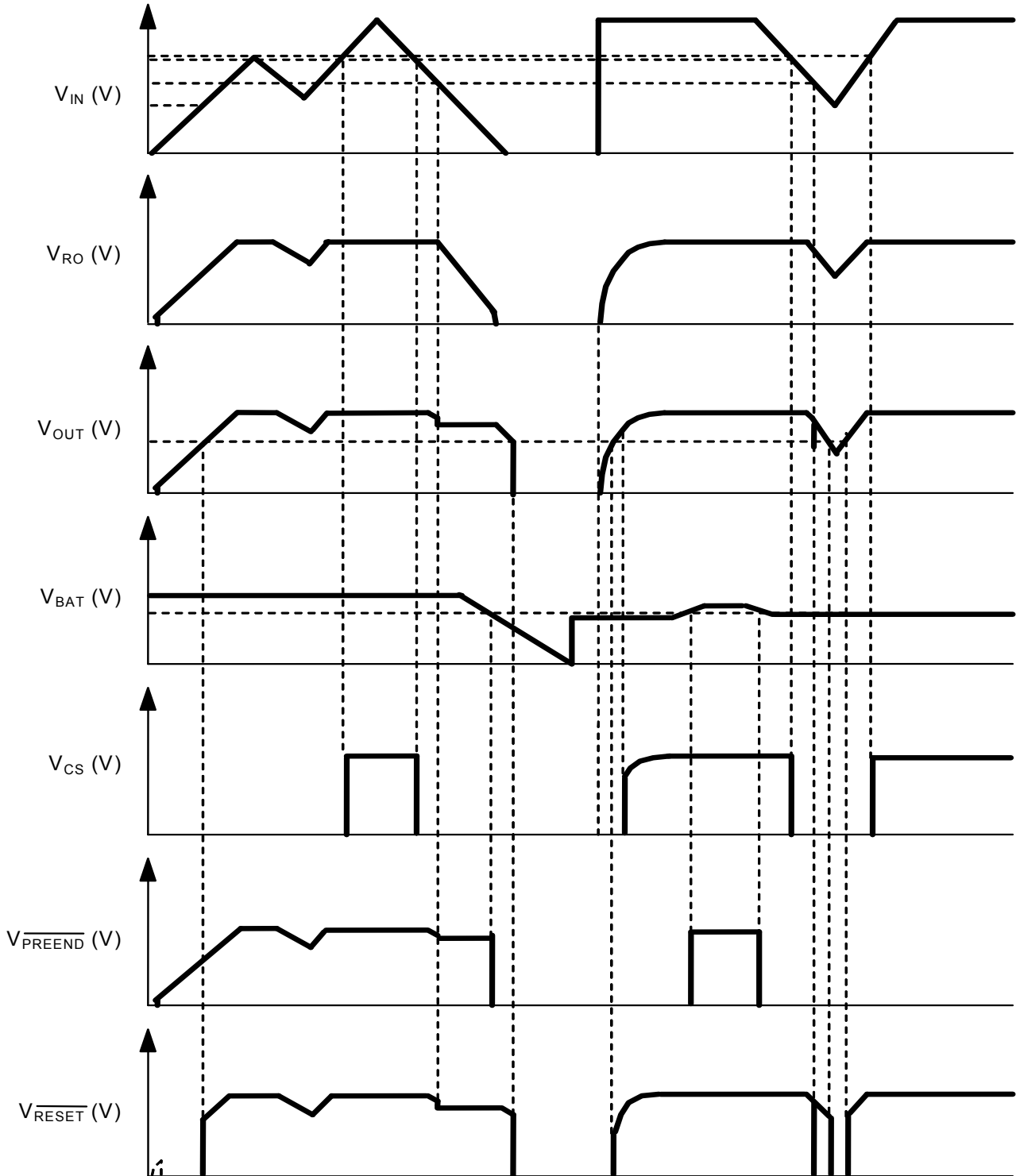


Figure 15 Definition of V_{dif}

■ Timing Chart



Remark CS, \overline{PREEND} and \overline{RESET} are pulled up to V_{OUT} . Y-axis is an arbitrary scale.

Figure 16 Operation Timing Chart

■ **Standard Circuit**

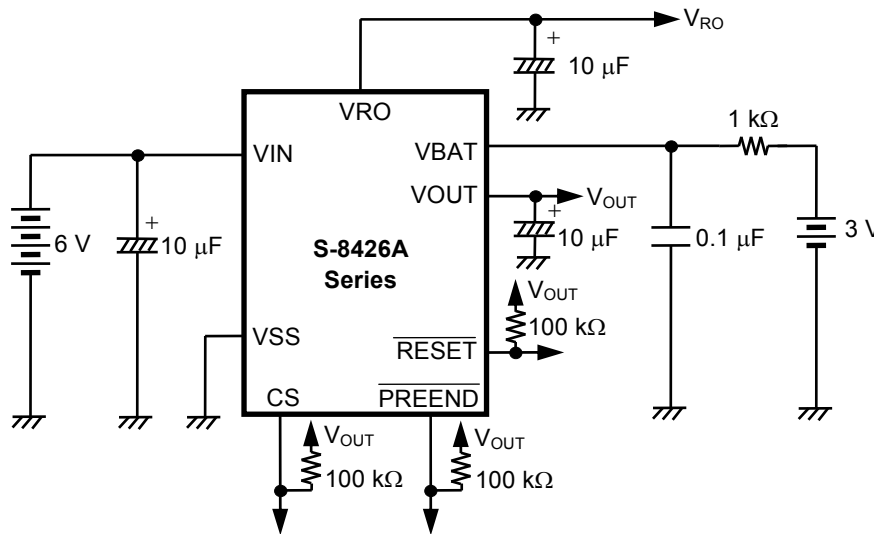


Figure 17

- Caution 1.** Be sure to add a 10 μF or more capacitor to the VOUT and VRO pins.
2. The above connections and values will not guarantee correct operation. Before setting these values, perform sufficient evaluation on the application to be actually used.

■ **Precautions**

- In applications with small I_{RO} or I_{OUT} , the output voltages V_{RO} and V_{OUT} may rise, causing the load stability to exceed standard levels. Set I_{RO} and I_{OUT} to 10 μA or more.
- Attach the proper capacitor to the VOUT pin to prevent the $\overline{\text{RESET}}$ voltage detector (which monitors the VOUT pin) from coming active due to undershoot.
- Watch for overshoot and ensure it does not exceed the ratings of the IC chips and/or capacitors attached to the VRO and VOUT pins.
- Add a 10 μF or more capacitor to the VOUT and VRO pins.
- When V_{IN} rises from the voltage more than V_{SW1} , a low pulse of less than 4 ms flows through the $\overline{\text{PREEND}}$ pin even when V_{BAT} is more than the $\overline{\text{PREEND}}$ release voltage. Thus when monitoring the $\overline{\text{PREEND}}$ pin, make sure to take the 4 ms interval or more after the rise of V_{IN} .
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Application Circuits

1. When Using Timer Micro controllers for Backup to display $\overline{\text{PREEND}}$ in the primary CPU

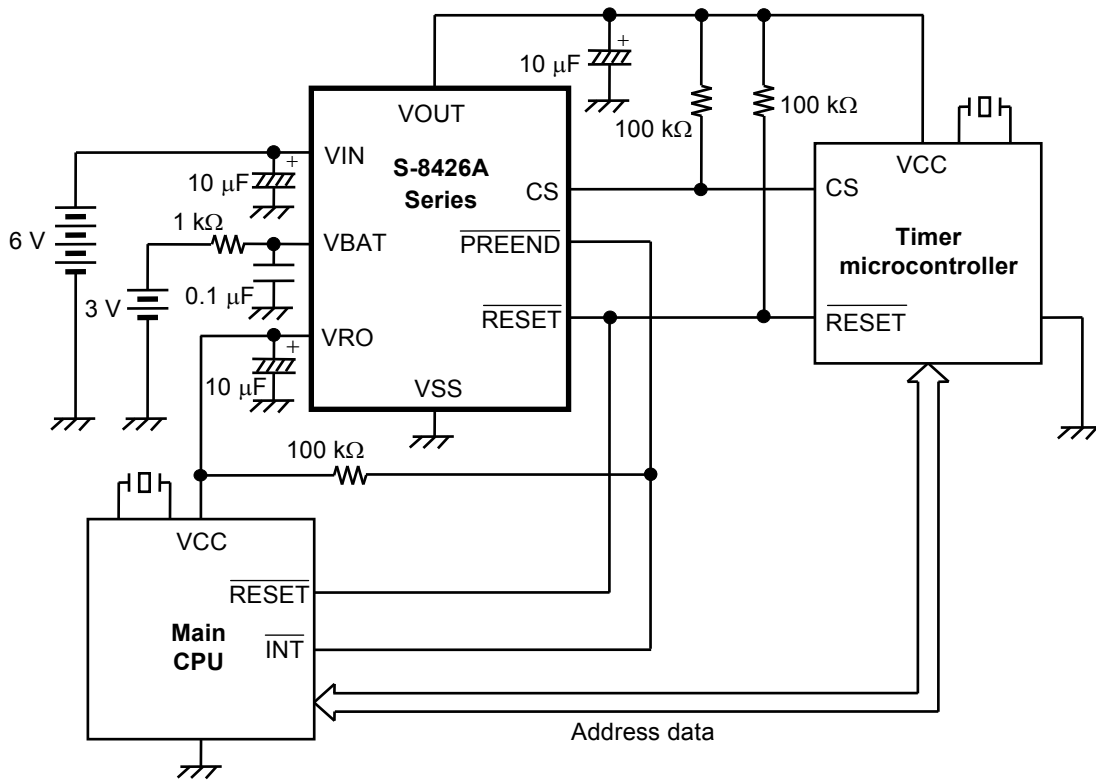


Figure 18 Application Circuit 1

2. When Using Secondary Battery as Backup Battery

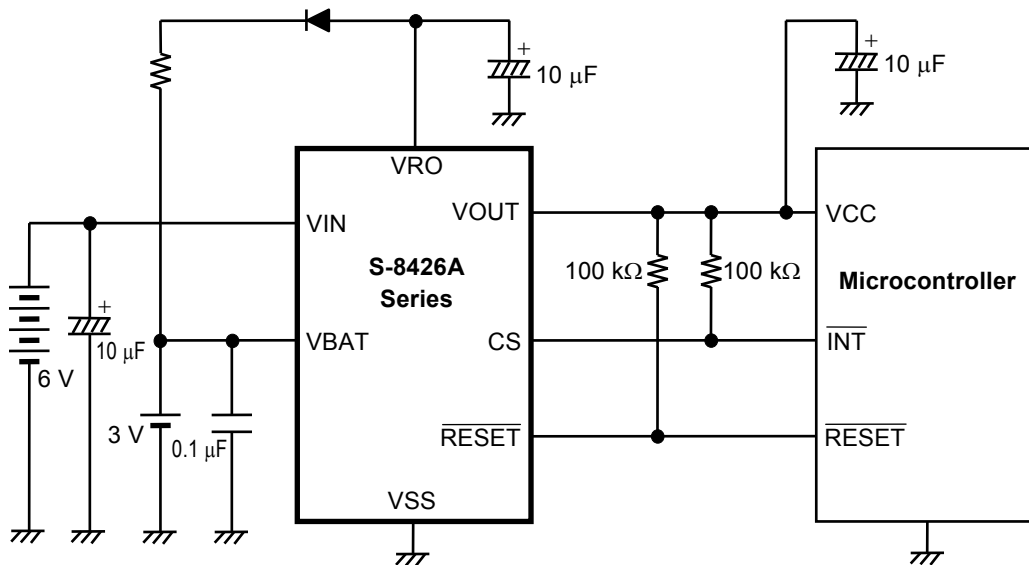


Figure 19 Application Circuit 2

Remark The backup battery can be floating-recharged by using voltage regulator 1.

3. Memory Card

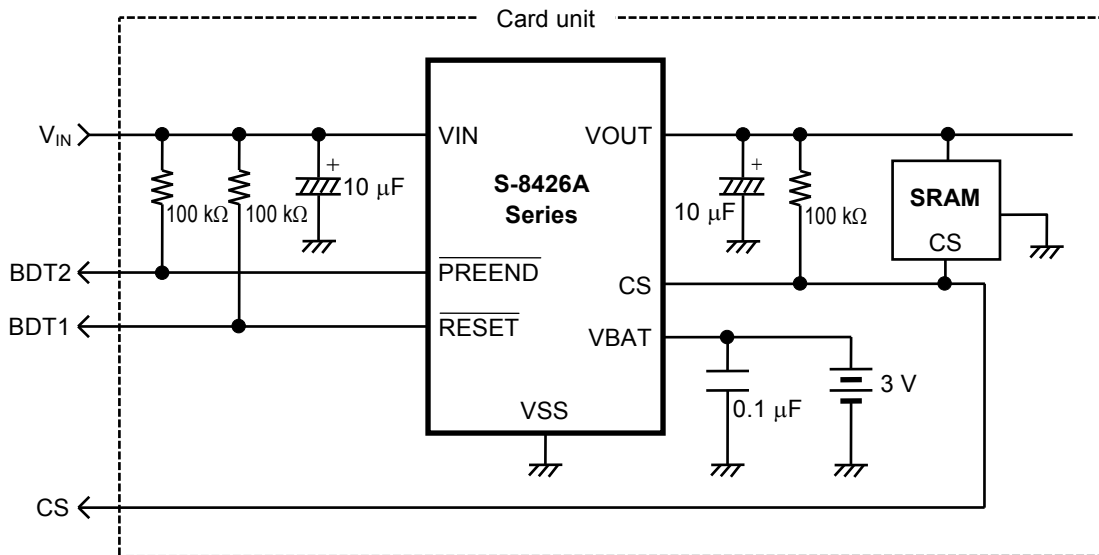


Figure 20 Application Circuit 3

Caution The above connections and values will not guarantee correct operation. Before setting these values, perform sufficient evaluation on the application to be actually used.

■ Transient Response

1. Line Transient Response Against Input Voltage Variation

The input voltage variation differs depending on whether the power supply input (0 to 10 V square wave) is applied or the power supply variation (6 V and 10 V square waves) is applied. This section describes the ringing waveforms and parameter dependency of each type. The test circuit is shown for reference.

1.1 Power supply application: 0 to 10 V Square wave

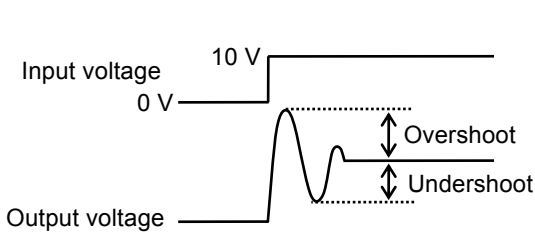


Figure 21 Power Supply Application: 0 to 10 V Square Wave

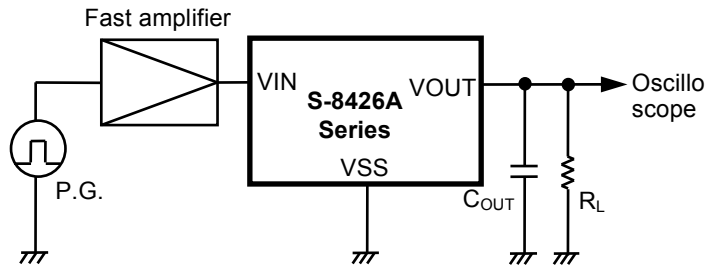


Figure 22 Test Circuit

VOUT pin

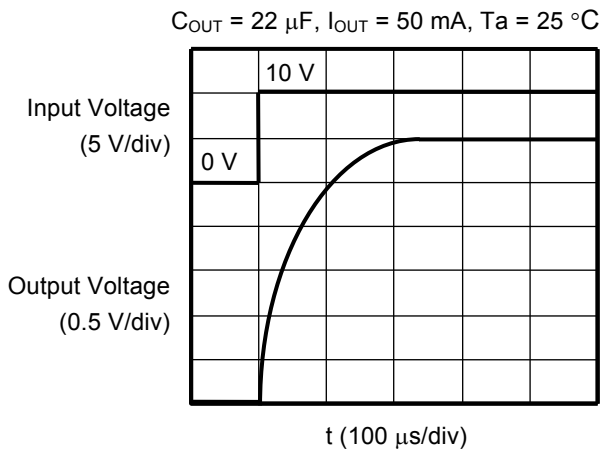


Figure 23 Ringing Waveform of Power Supply Application (VOUT Pin)

VRO pin

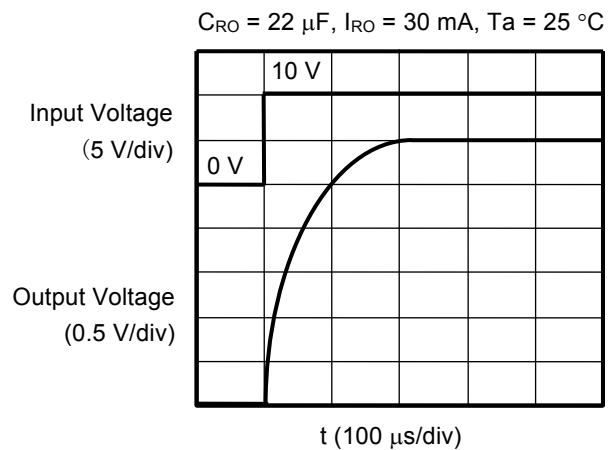
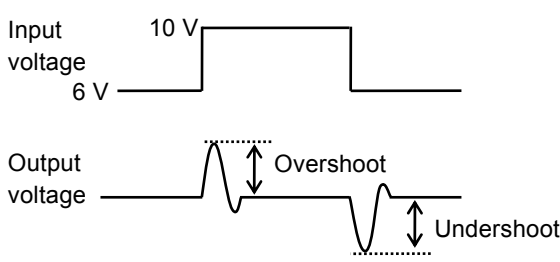


Figure 24 Ringing Waveform of Power Supply Application (VRO Pin)

1.2 Power supply variation: 6 V and 10 V square waves



**Figure 25 Power Supply Variation:
 6 V and 10 V Square Waves**

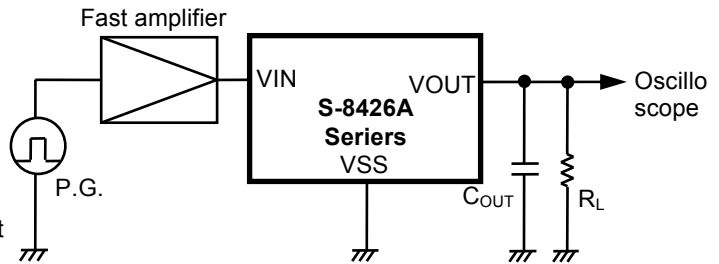
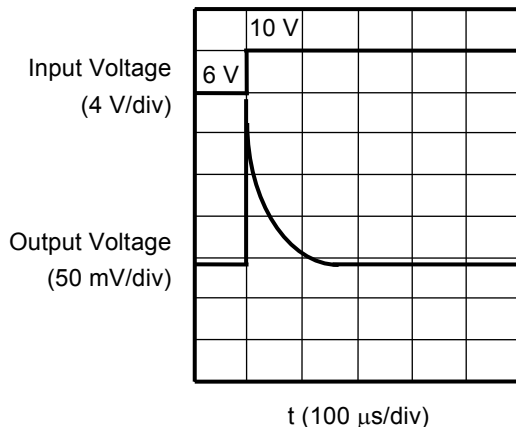


Figure 26 Test Circuit

VOUT pin



$C_{OUT} = 22 \mu F, I_{OUT} = 50 \text{ mA}, T_a = 25 \text{ }^\circ\text{C}$

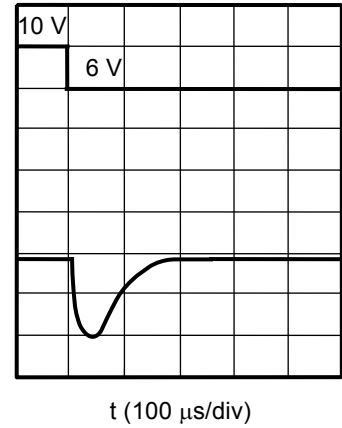
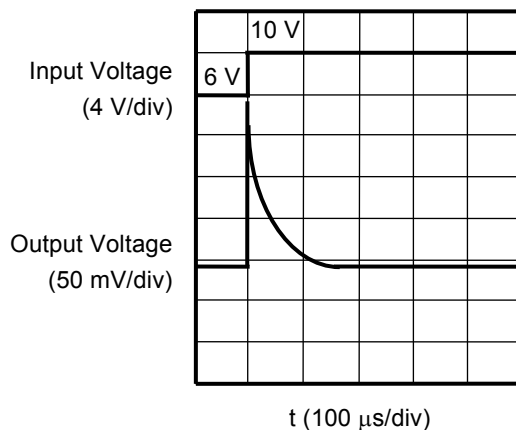


Figure 27 Ringing Waveform of Power Supply Variation (VOUT Pin)

VRO pin



$C_{RO} = 22 \mu F, I_{RO} = 30 \text{ mA}, T_a = 25 \text{ }^\circ\text{C}$

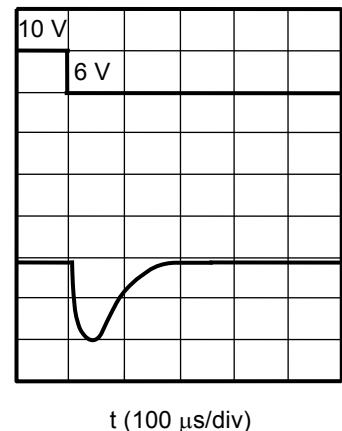


Figure 28 Ringing Waveform of Power Supply Variation (VRO Pin)

1.3 Reference data: Dependency of output current (I_{OUT}), load capacitance (C_{OUT}), input variation width (ΔV_{IN}), temperature (T_a)

For reference, the following pages describe the results of measuring the ringing amounts at the VOUT and VRO pins using the output current (I_{OUT}), load capacitance (C_{OUT}), input variation width (ΔV_{IN}), and temperature (T_a) as parameters.

(1) I_{OUT} Dependency

(a) VOUT pin

$C_{OUT} = 22 \mu F, V_{IN} = 6 \leftrightarrow 10 V, T_a = 25 \text{ }^\circ C$

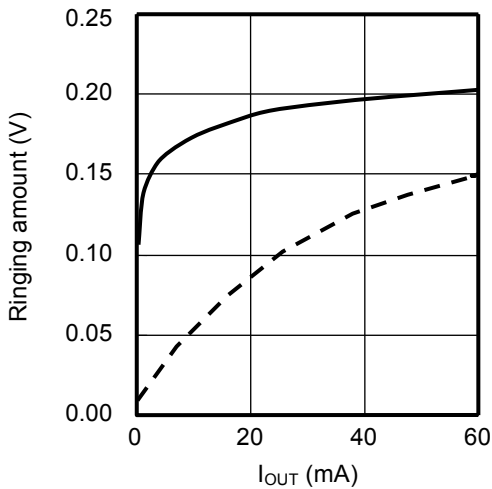


Figure 29

(b) VRO pin

$C_{RO} = 22 \mu F, V_{IN} = 6 \leftrightarrow 10 V, T_a = 25 \text{ }^\circ C$

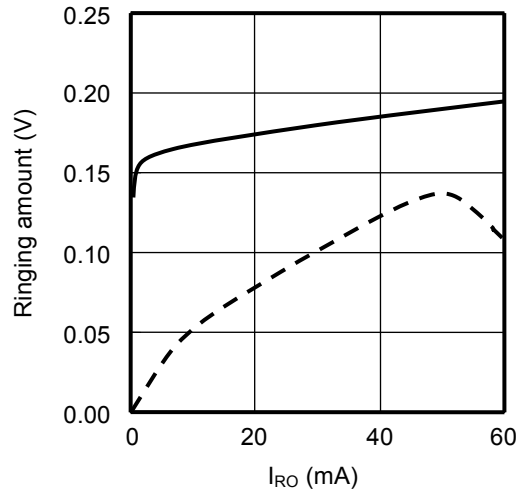


Figure30

— Overshoot
- - - Undershoot

(2) C_{OUT} Dependency

(a) VOUT pin

$I_{OUT} = 50 \text{ mA}, V_{IN} = 6 \leftrightarrow 10 V, T_a = 25 \text{ }^\circ C$

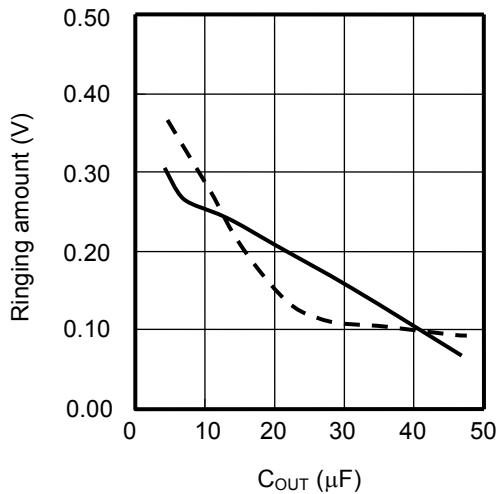


Figure 31

(b) VRO pin

$I_{RO} = 30 \text{ mA}, V_{IN} = 6 \leftrightarrow 10 V, T_a = 25 \text{ }^\circ C$

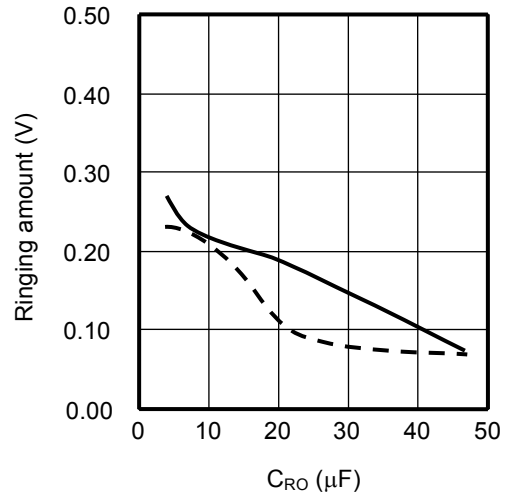


Figure32

— Overshoot
- - - Undershoot

(3) ΔV_{IN} Dependency

ΔV_{IN} shows the difference between the low voltage fixed to 6 V and the high voltage.
 For example, $\Delta V_{IN} = 2$ V means the difference between 6 V and 8 V.

(a) VOUT pin

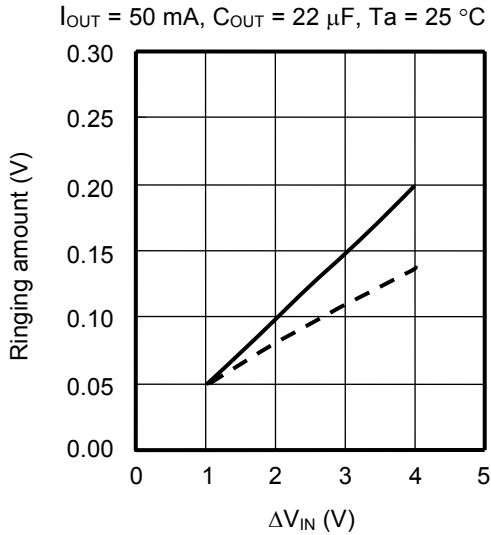


Figure 33

(b) VRO pin

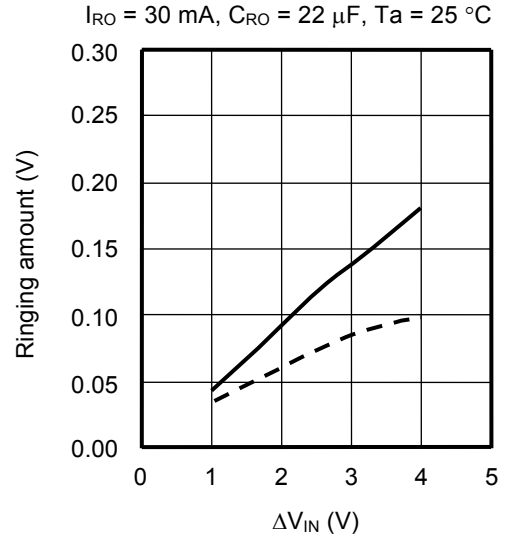


Figure 34

————— Overshoot
 - - - - - Undershoot

(4) Temperature Dependency

(a) VOUT pin

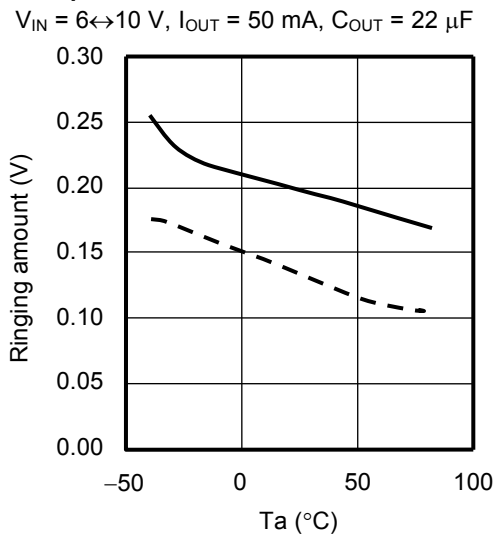


Figure 35

(b) VRO pin

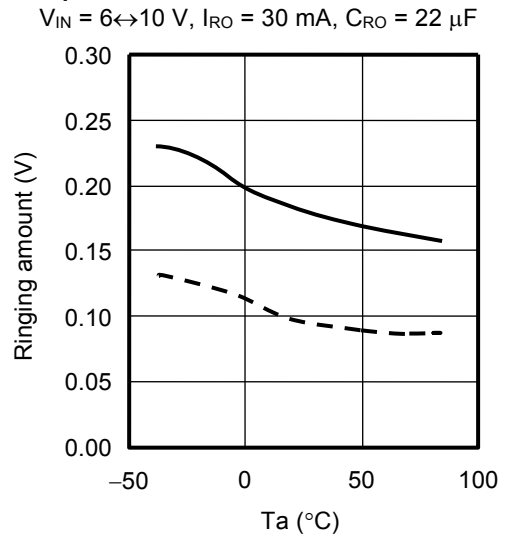


Figure 36

————— Overshoot
 - - - - - Undershoot

2. Load Transient Response Based on Output Current Fluctuation

The overshoot and undershoot are caused in the output voltage if the output current fluctuates between 10 μ A and 50 mA (V_{RO} is between 10 μ A and 30 mA) while the input voltage is constant. **Figure 37** shows the output voltage variation due to the output current. **Figure 38** shows the test circuit for reference. The latter half of this section describes ringing waveform and parameter dependency.

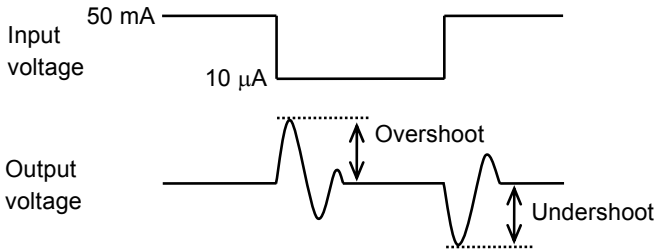


Figure 37 Output Voltage Variation due to Output Current

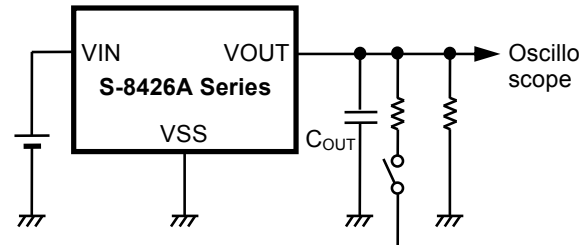


Figure 38 Test Circuit

2.1 Load Variation

Figure 39 shows the ringing waveforms at the VOUT pin and **Figure 40** shows the ringing waveforms at the VRO pin due to the load variation, respectively.

VOUT pin

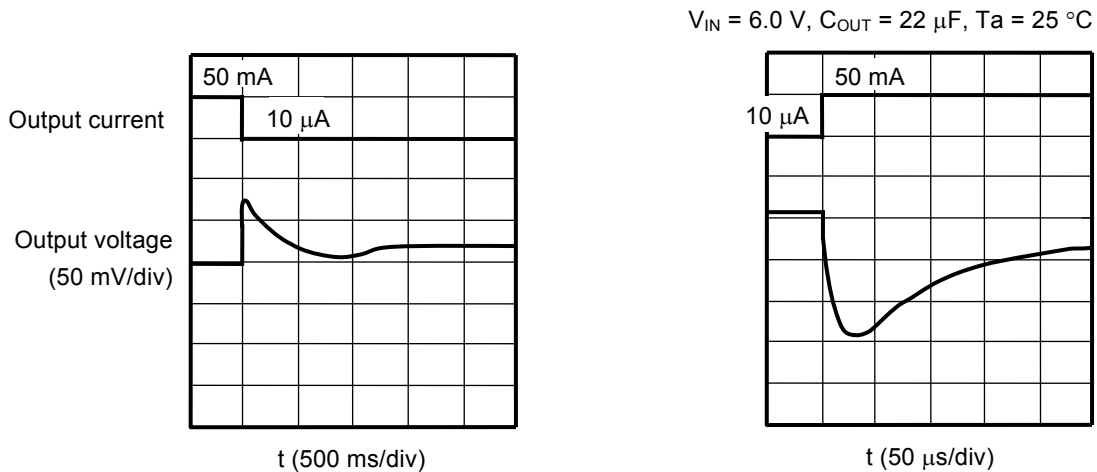


Figure 39 Ringing Waveform due to Load Variation (VOUT Pin)

VRO pin

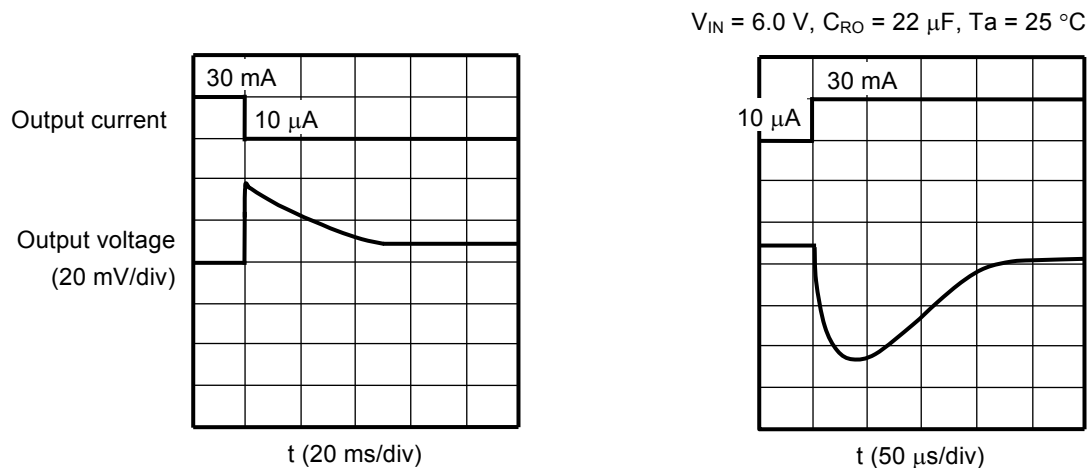


Figure 40 Ringing Waveform due to Load Variation (VRO Pin)

2.2 Reference data: Dependency of input voltage (V_{IN}), load capacitance (C_{OUT}), output variation width (ΔI_{OUT}), and temperature (T_a)

(1) V_{IN} Dependency

(a) VOUT pin

$C_{OUT} = 22 \mu F$, $I_{OUT} = 50 \text{ mA} \leftrightarrow 10 \mu A$, $T_a = 25 \text{ }^\circ\text{C}$

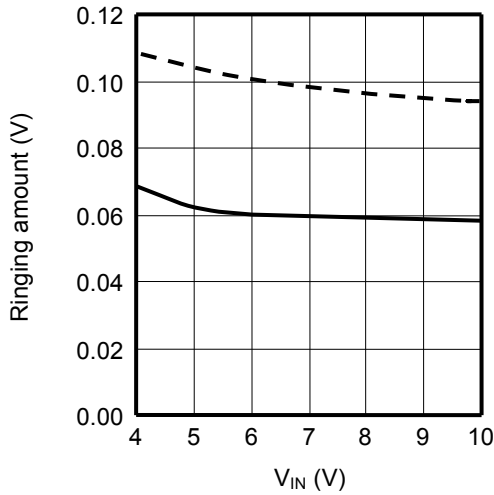


Figure 41

(b) VRO pin

$C_{RO} = 22 \mu F$, $I_{RO} = 30 \text{ mA} \leftrightarrow 10 \mu A$, $T_a = 25 \text{ }^\circ\text{C}$

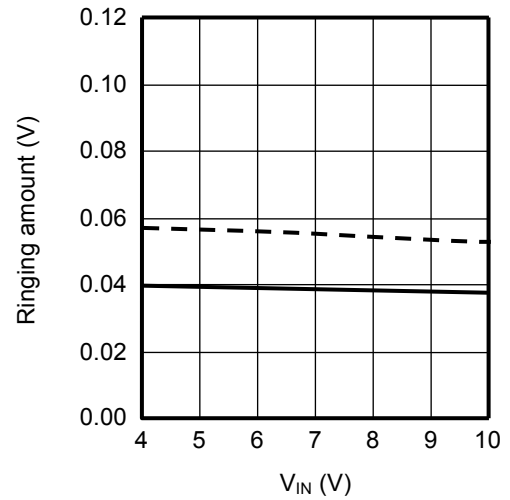


Figure 42

— Overshoot
 - - - Undershoot

(2) C_{OUT} Dependency

(a) VOUT pin

$V_{IN} = 6.0 \text{ V}$, $I_{OUT} = 50 \text{ mA} \leftrightarrow 10 \mu A$, $T_a = 25 \text{ }^\circ\text{C}$

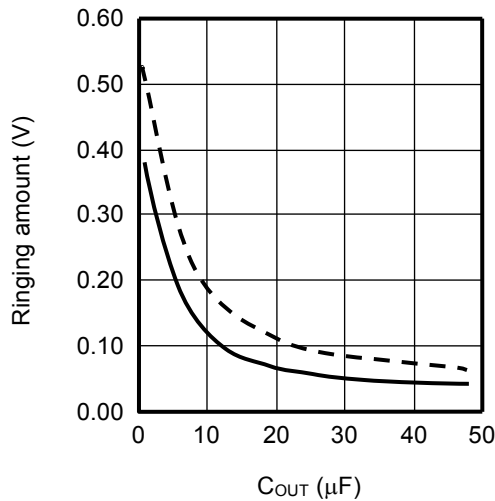


Figure 43

(b) VRO pin

$V_{IN} = 6.0 \text{ V}$, $I_{RO} = 30 \text{ mA} \leftrightarrow 10 \mu A$, $T_a = 25 \text{ }^\circ\text{C}$

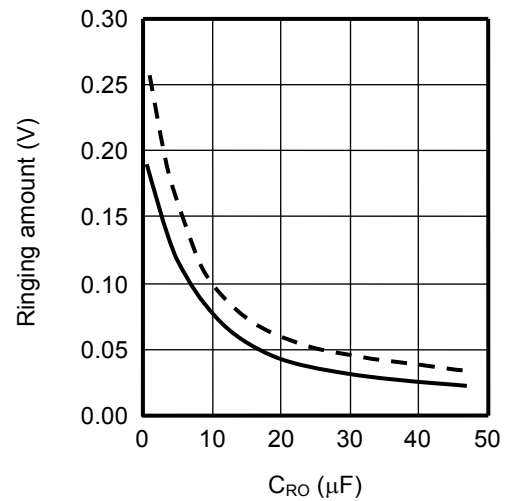


Figure 44

— Overshoot
 - - - Undershoot

(3) ΔI_{OUT} Dependency

ΔI_{OUT} and ΔI_{RO} show the fluctuation between the low current stabilized at 10 μA and the high current. For example, $\Delta I_{OUT} = 10$ mA means a fluctuation between 10 μA and 10 mA.

(a) VOUT pin

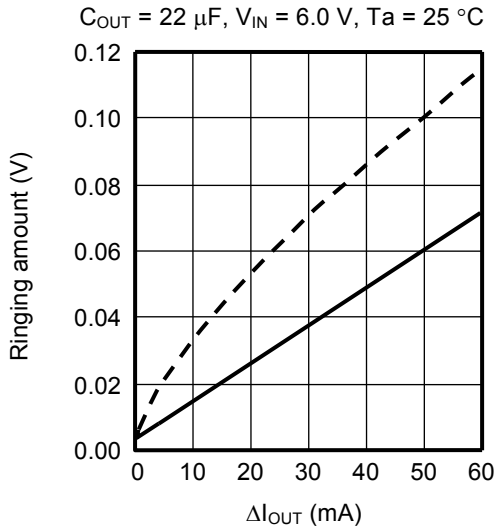


Figure 45

(b) VRO pin

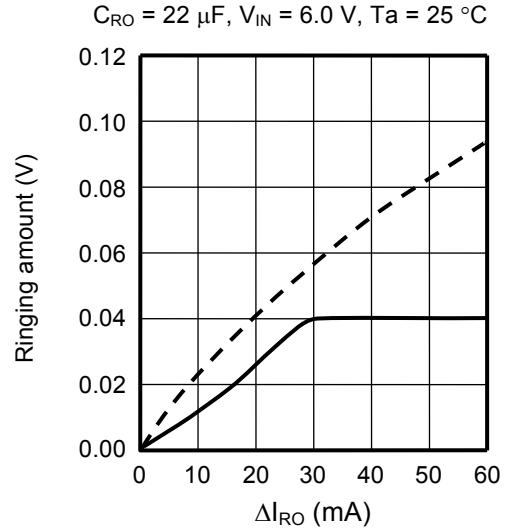


Figure 46

— Overshoot
- - - Undershoot

(4) Temperature Dependency

(a) VOUT pin

$V_{IN} = 6.0 V, I_{OUT} = 50 \text{ mA} \leftrightarrow 10 \mu A, C_{OUT} = 22 \mu F$

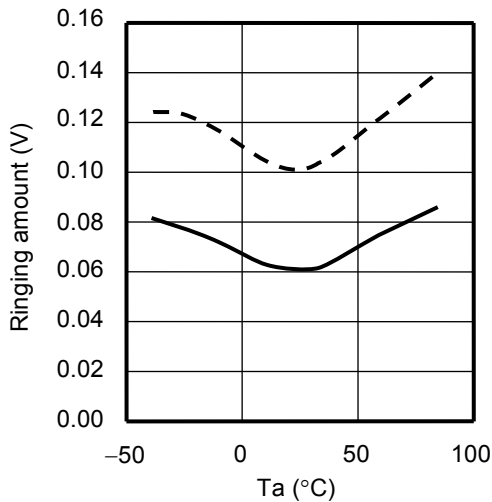


Figure 47

(b) VRO pin

$V_{IN} = 6.0 V, I_{RO} = 30 \text{ mA} \leftrightarrow 10 \mu A, C_{RO} = 22 \mu F$

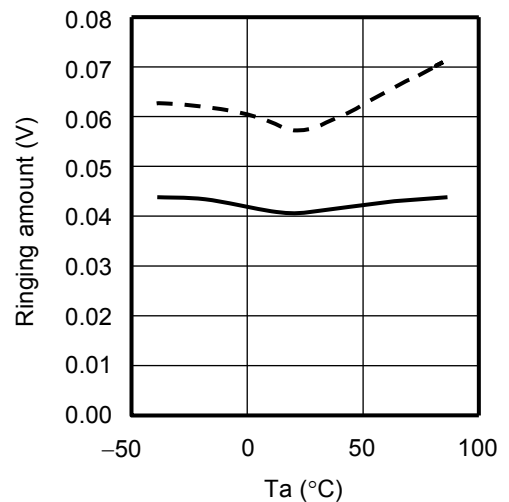


Figure 48

— Overshoot
- - - Undershoot

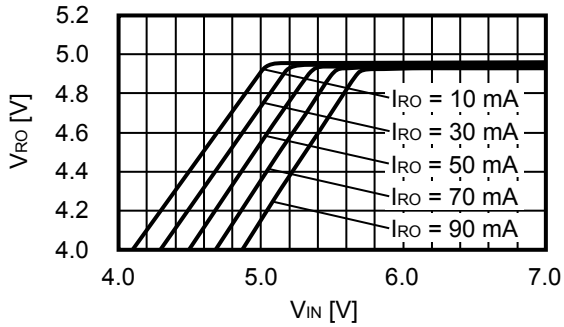
- Caution 1.** Be sure to add a 10 μF or more capacitor to the VOUT and VRO pins.
2. The above connections and values will not guarantee correct operation. Before setting these values, perform sufficient evaluation on the application to be actually used.

■ **Characteristics (Typical Data)**

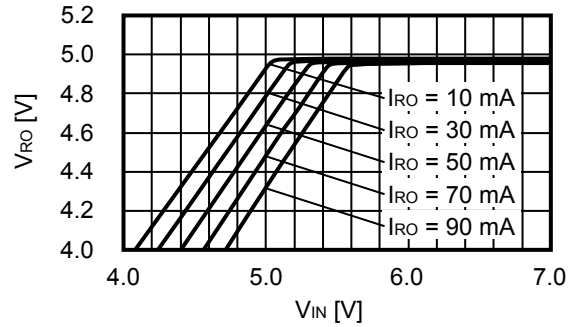
1. Voltage Regulator Unit ($V_{RO} = V_{OUT} = 5.0\text{ V}$)

1.1 Input Voltage (V_{IN}) vs. Output Voltage (V_{RO}) Characteristics (REG1)

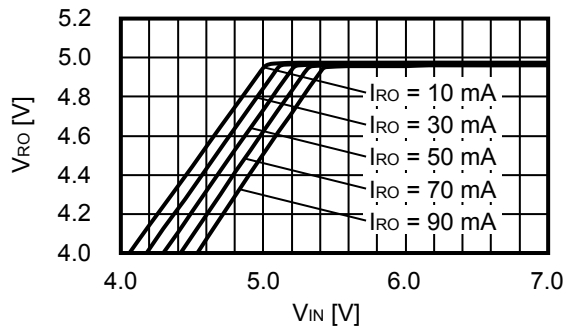
(1) $T_a = 85\text{ }^\circ\text{C}$



(2) $T_a = 25\text{ }^\circ\text{C}$

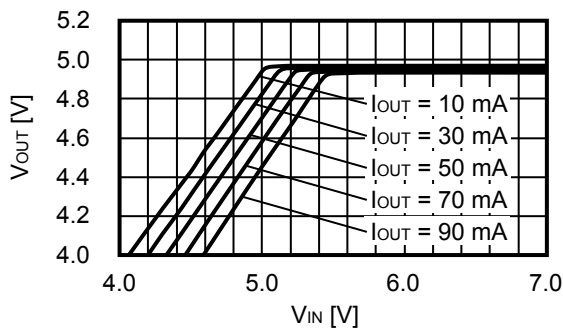


(3) $T_a = -40\text{ }^\circ\text{C}$

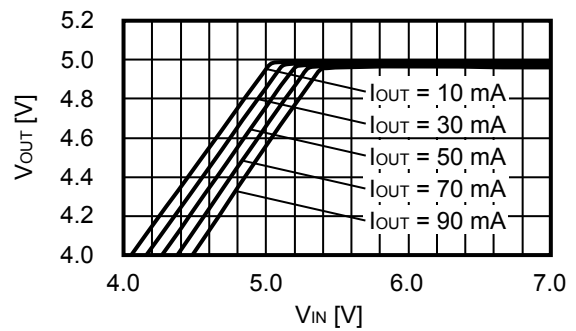


1.2 Input Voltage (V_{IN}) vs. Output Voltage (V_{OUT}) Characteristics (REG2)

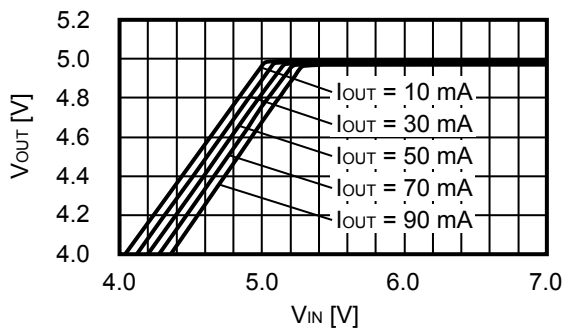
(1) $T_a = 85\text{ }^\circ\text{C}$



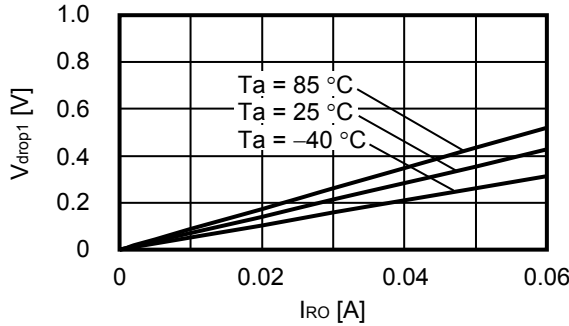
(2) $T_a = 25\text{ }^\circ\text{C}$



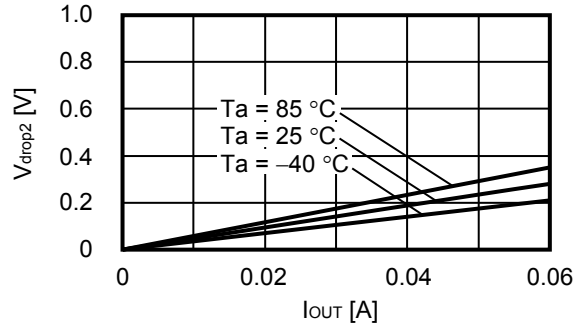
(3) $T_a = -40\text{ }^\circ\text{C}$



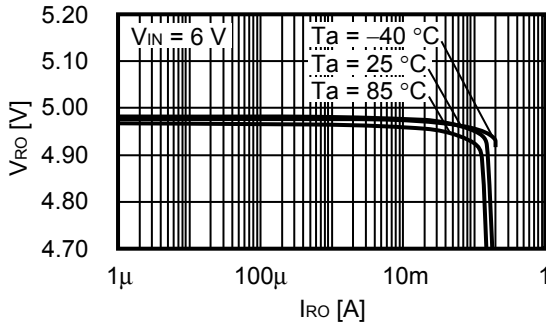
1.3 Output Current (I_{RO}) vs. Dropout Voltage (V_{drop1}) Characteristics



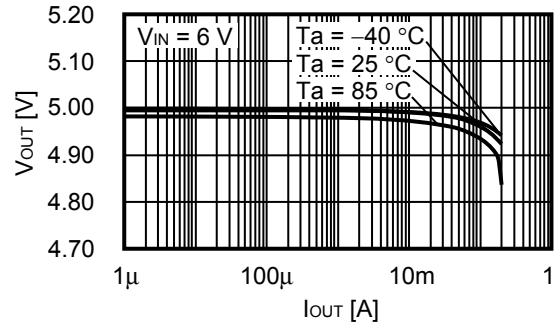
1.4 Output Current (I_{OUT}) vs. Dropout Voltage (V_{drop2}) Characteristics



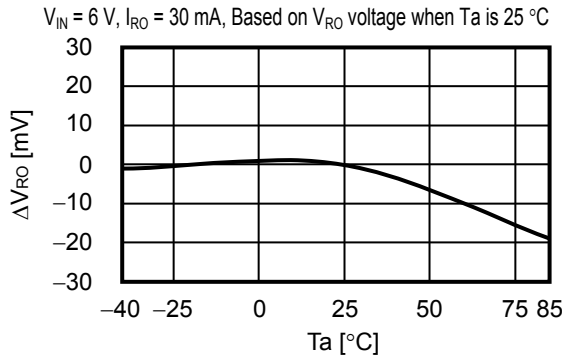
1.5 Output Current (I_{RO}) vs. Output Voltage (V_{RO}) Characteristics



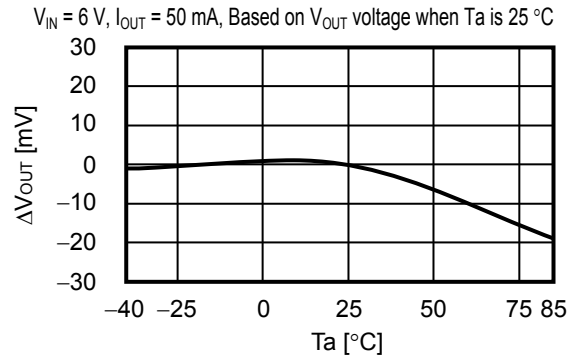
1.6 Output Current (I_{OUT}) vs. Output Voltage (V_{OUT}) Characteristics



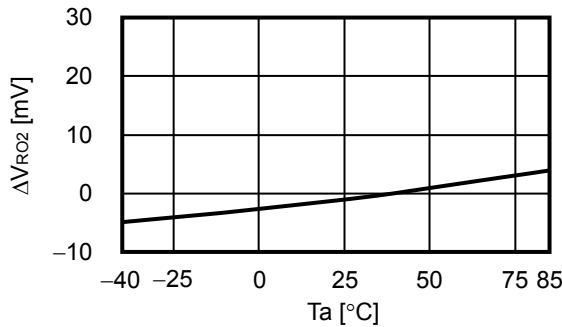
1.7 Output voltage (V_{RO}) Temperature Characteristics



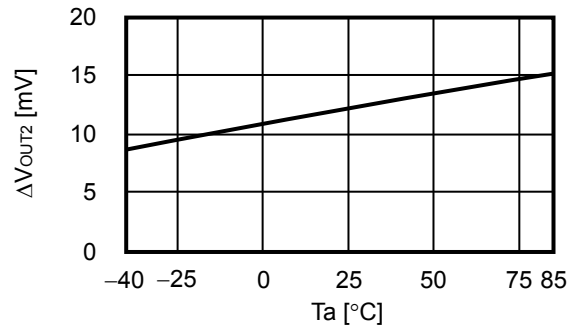
1.8 Output voltage (V_{OUT}) Temperature Characteristics



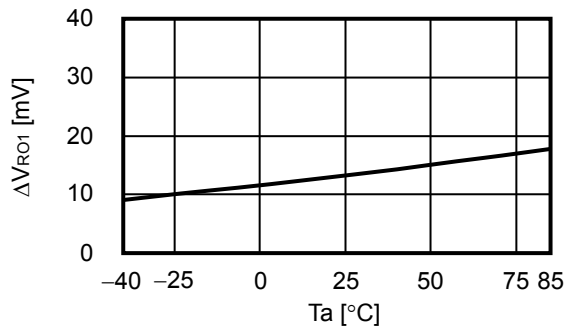
1.9 Input Stability (V_{RO}) Temperature Characteristics



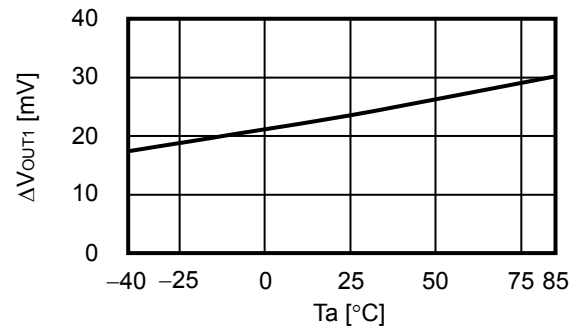
1.10 Input Stability (V_{OUT}) Temperature Characteristics



1. 11 Load Stability (V_{RO}) Temperature Characteristics



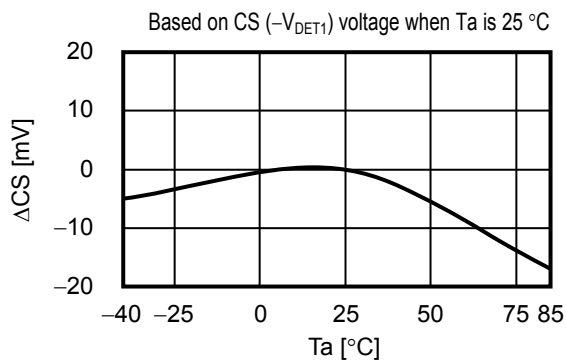
1. 12 Load Stability (V_{RO}) Temperature Characteristics



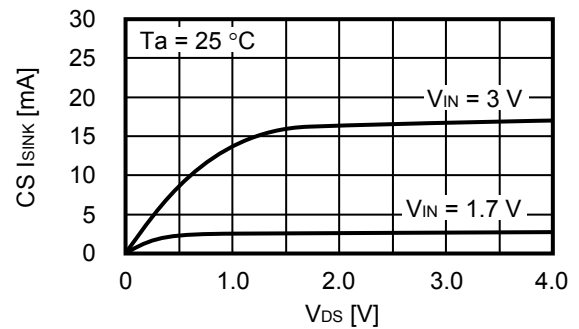
2. Voltage Detector

2. 1 CS Voltage Detector ($-V_{DET1} = 4.5 V$)

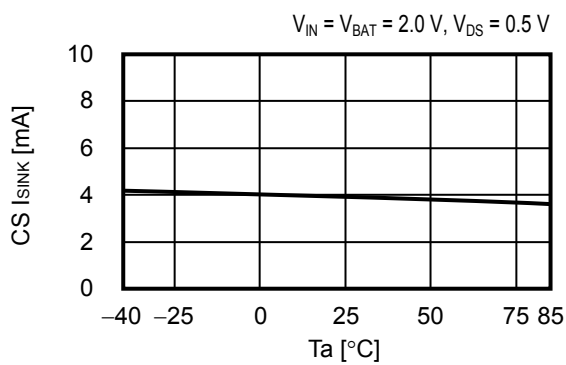
(1) Detection voltage ($-V_{DET1}$) temperature characteristics



(2) Output current (I_{SINK}) characteristics

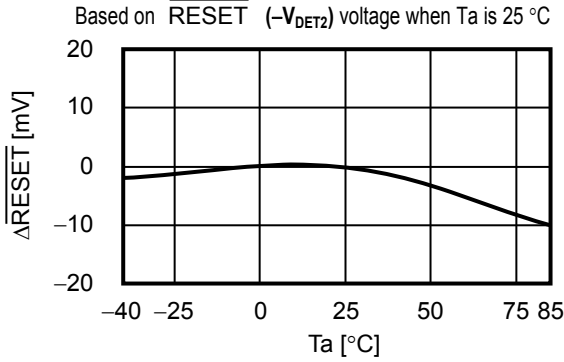


(3) Output current (I_{SINK}) temperature characteristics

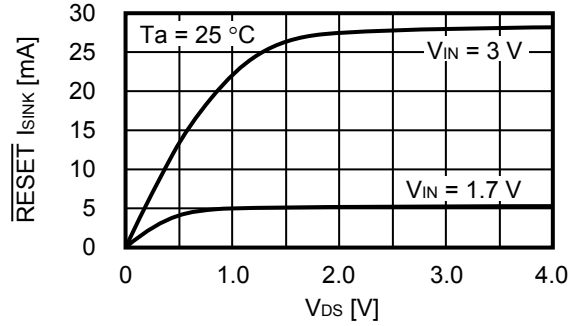


2.2 $\overline{\text{RESET}}$ Voltage Detector ($-V_{\text{DET}2} = 2.9 \text{ V}$)

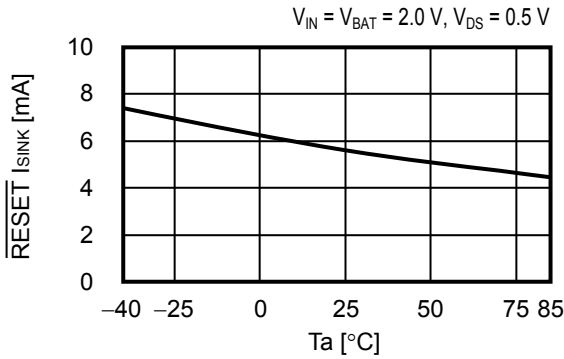
(1) Detection voltage ($-V_{\text{DET}2}$) temperature characteristics



(2) Output current (I_{SINK}) characteristics

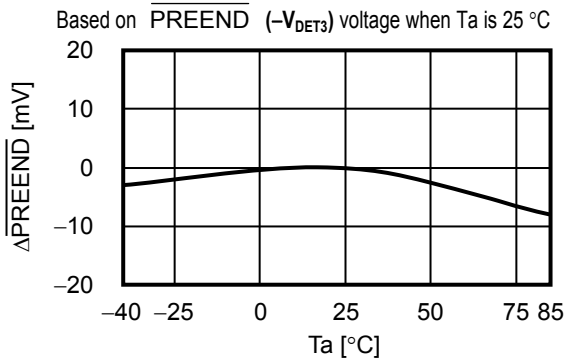


(3) Output current (I_{SINK}) temperature characteristics

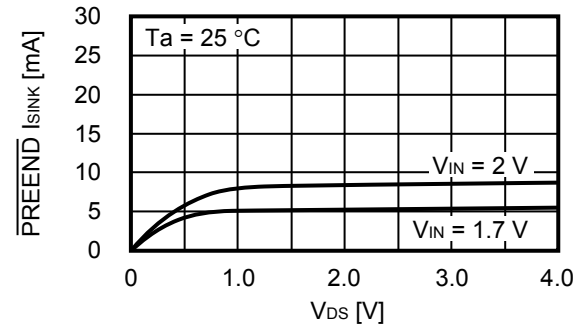


2.3 $\overline{\text{PREEND}}$ Voltage Detector ($-V_{\text{DET}3} = 2.1 \text{ V}$)

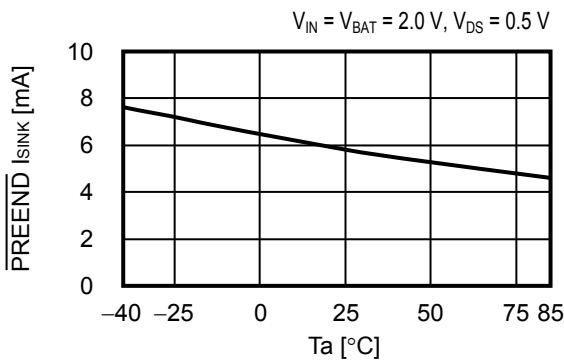
(1) Detection voltage ($-V_{\text{DET}3}$) temperature characteristics



(2) Output current (I_{SINK}) characteristics

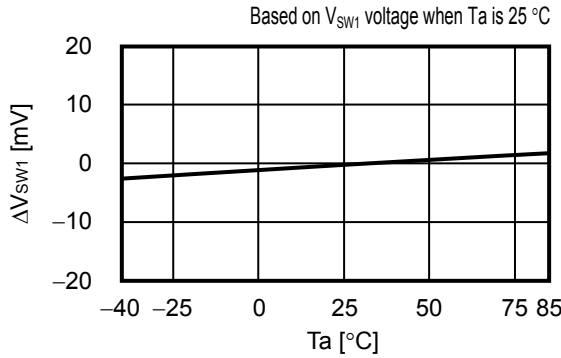


(3) Output current (I_{SINK}) temperature characteristics

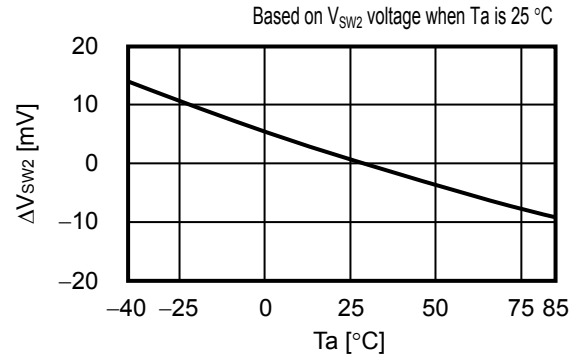


3. Switch Unit

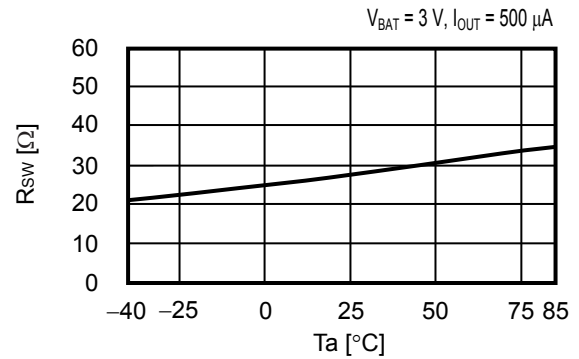
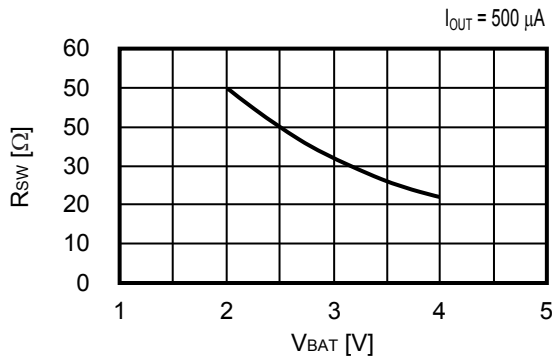
3.1 Switch Voltage (V_{SW1}) Temperature Characteristics



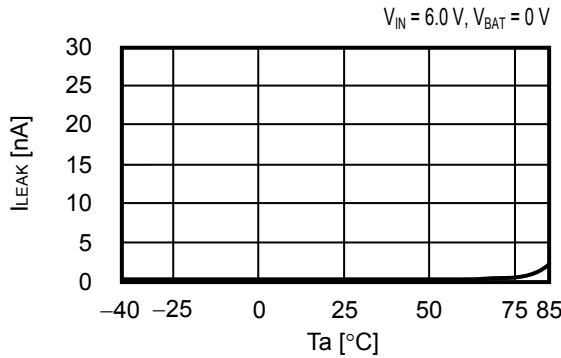
3.2 CS Output Inhibit Voltage (V_{SW2}) Temperature Characteristics



3.3 Input Voltage (V_{BAT}) vs. V_{BAT} Switch Resistance (R_{SW}) Characteristics **3.4 V_{BAT} Switch Resistance (R_{SW}) Temperature Characteristics**

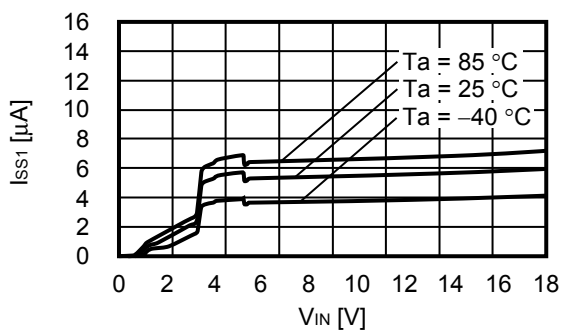


3.5 V_{BAT} Switch Leakage Current (I_{LEAK}) Temperature Characteristics

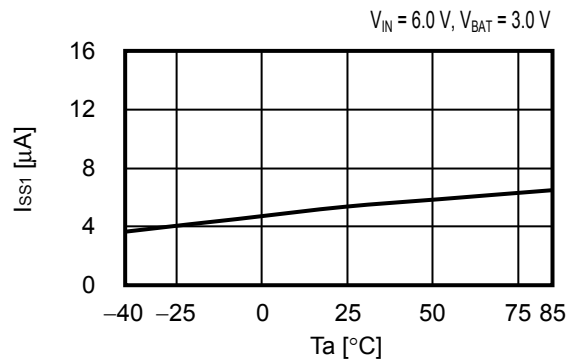


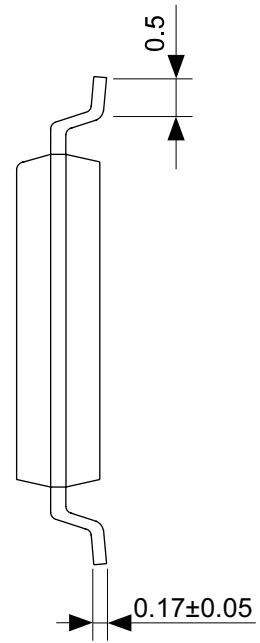
4. Consumption Current

4.1 V_{IN} vs. V_{IN} Consumption Current (I_{SS1}) Characteristics



4.2 Consumption Current Temperature





No. FT008-A-P-SD-1.2

| | |
|-------------------|-------------------------|
| TITLE | TSSOP8-E-PKG Dimensions |
| No. | FT008-A-P-SD-1.2 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |



No. FT008-E-C-SD-1.0

| | |
|-------------------|-----------------------|
| TITLE | TSSOP8-E-Carrier Tape |
| No. | FT008-E-C-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |



Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

| | | | |
|-------------------|------------------|------|-------|
| TITLE | TSSOP8-E-Reel | | |
| No. | FT008-E-R-SD-1.0 | | |
| ANGLE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |

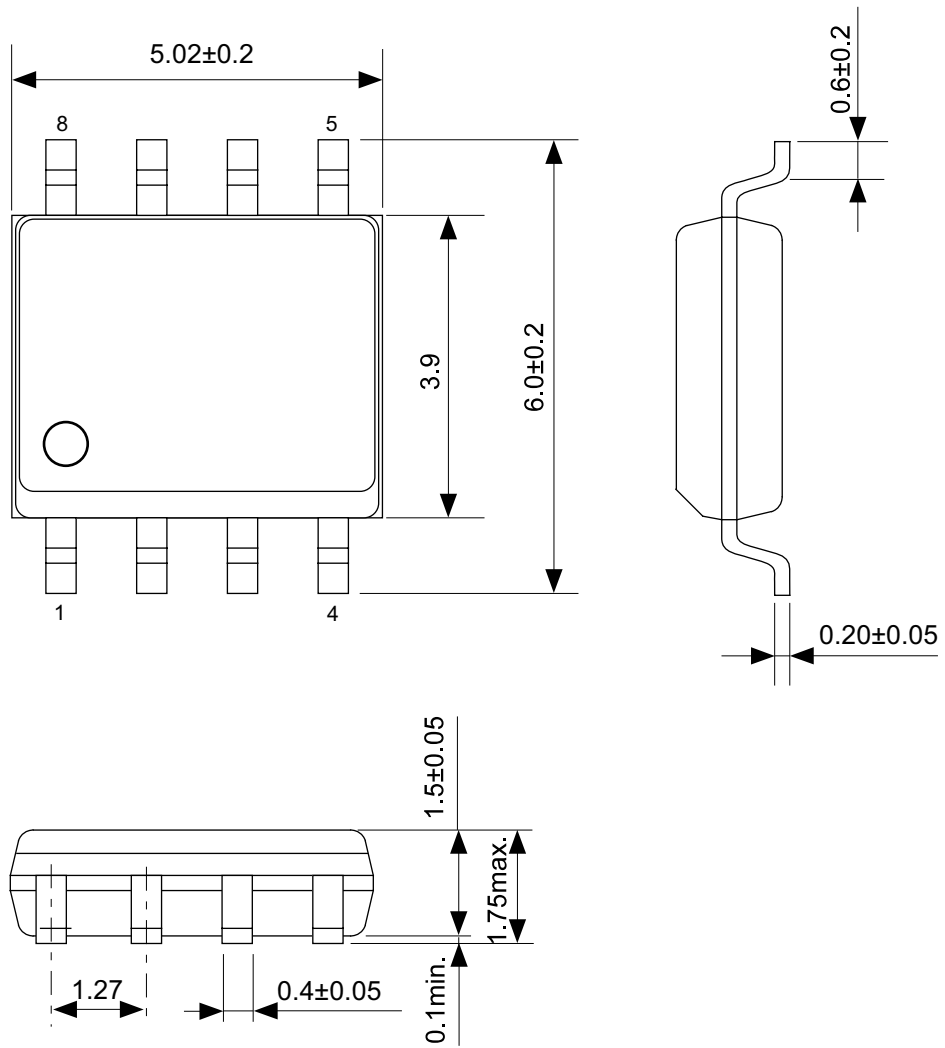


Enlarged drawing in the central part



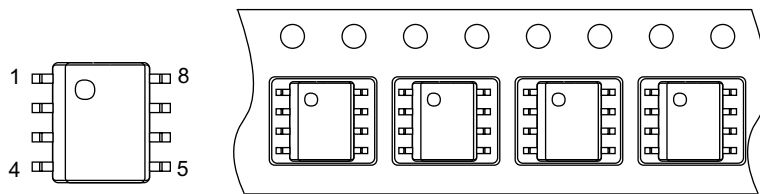
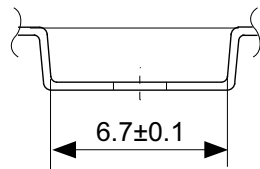
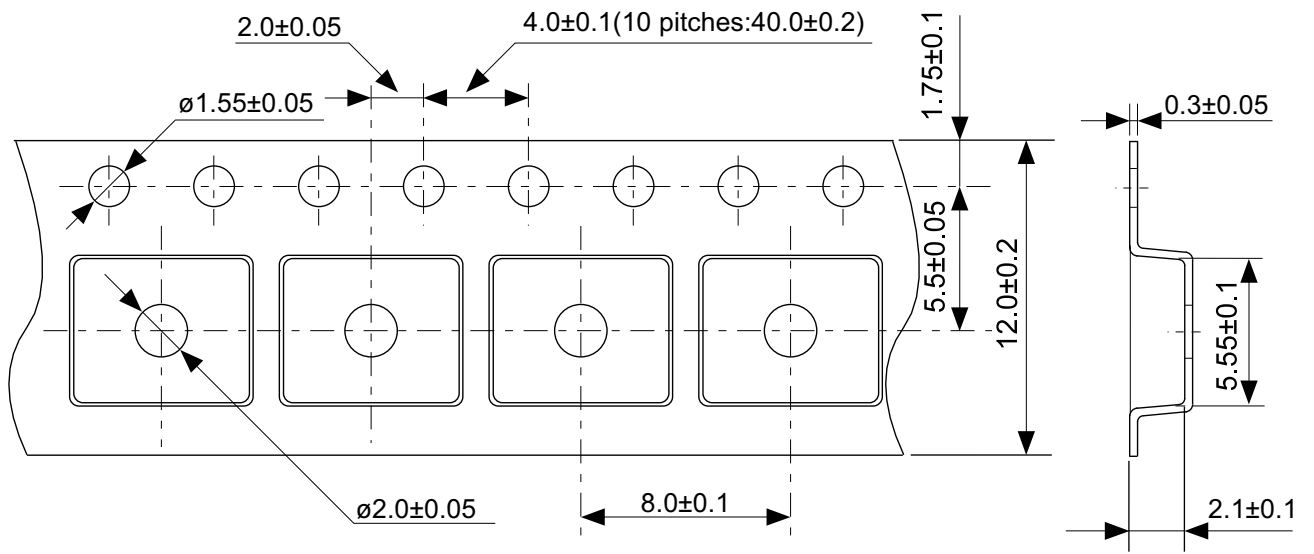
No. FT008-E-R-S1-1.0

| | | | |
|-------------------|------------------|------|-------|
| TITLE | TSSOP8-E-Reel | | |
| No. | FT008-E-R-S1-1.0 | | |
| ANGLE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |



No. FJ008-A-P-SD-2.2

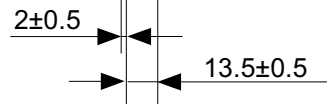
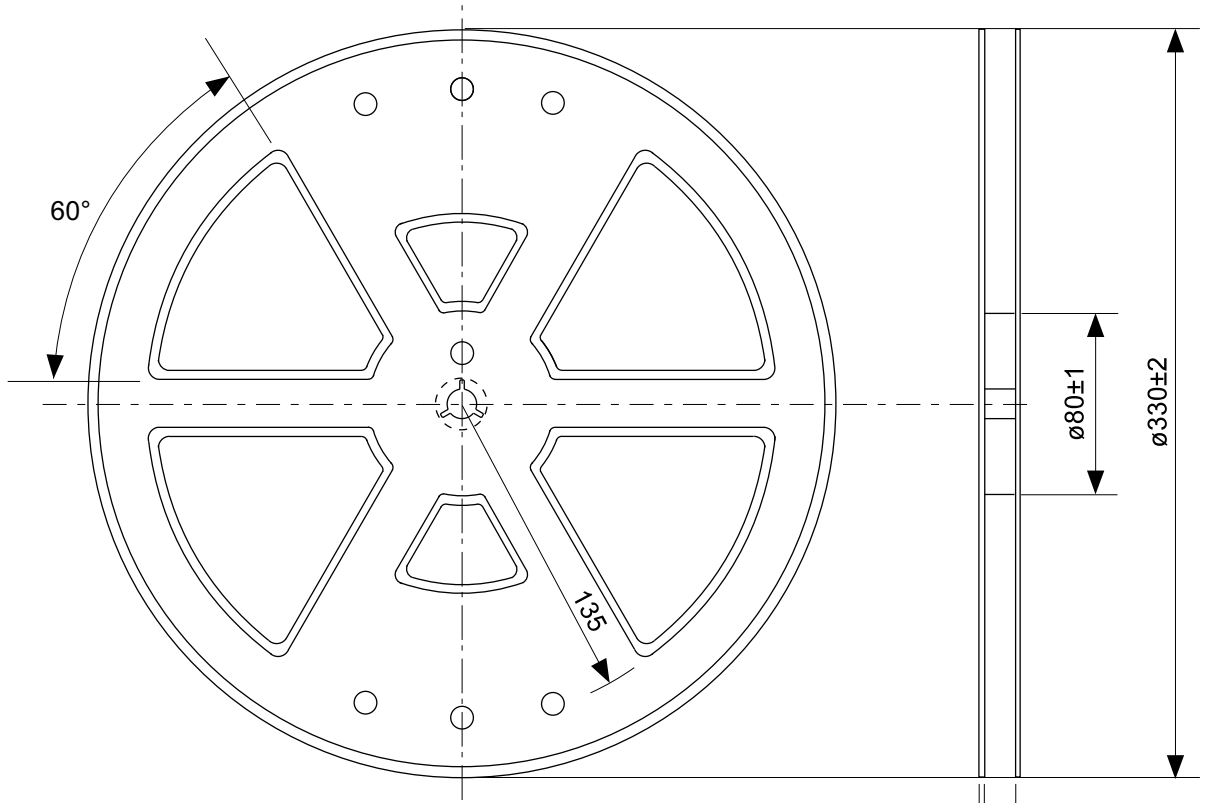
| | |
|-------------------|------------------------|
| TITLE | SOP8J-D-PKG Dimensions |
| No. | FJ008-A-P-SD-2.2 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |



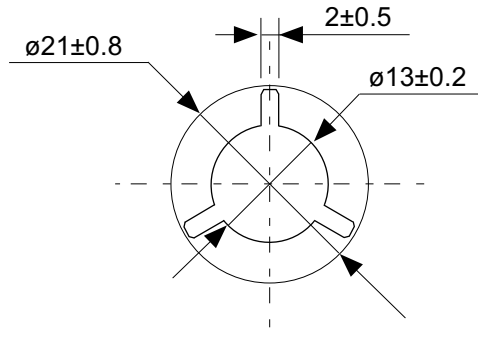
→
Feed direction

No. FJ008-D-C-SD-1.1

| | |
|-------------------|----------------------|
| TITLE | SOP8J-D-Carrier Tape |
| No. | FJ008-D-C-SD-1.1 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |

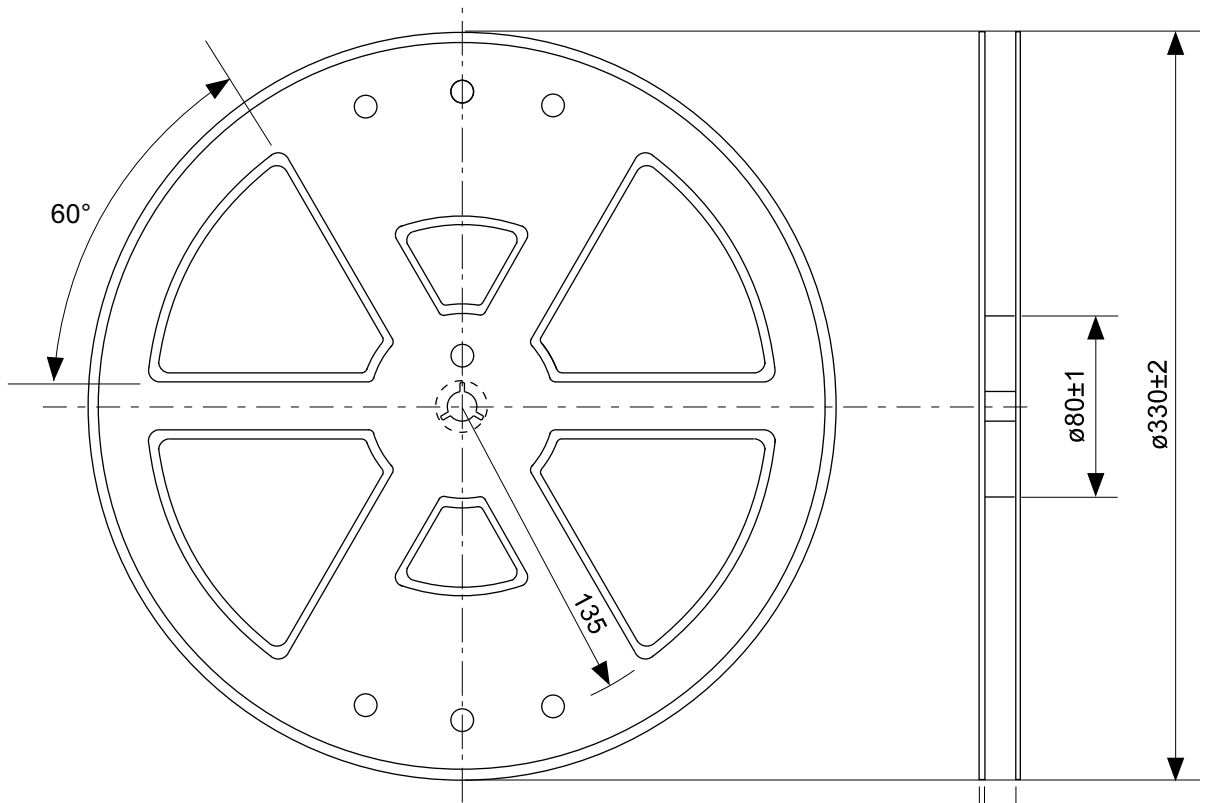


Enlarged drawing in the central part

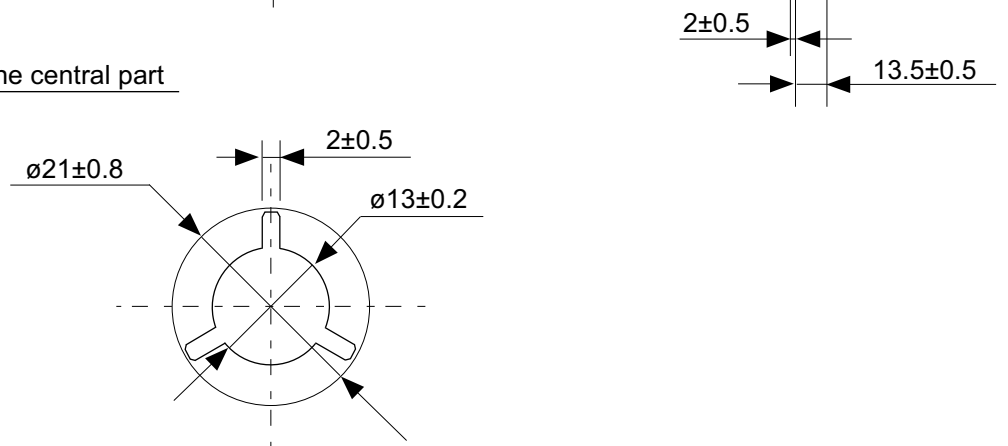


No. FJ008-D-R-SD-1.1

| | | | |
|-------------------|------------------|------|-------|
| TITLE | SOP8J-D-Reel | | |
| No. | FJ008-D-R-SD-1.1 | | |
| ANGLE | | QTY. | 2,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |



Enlarged drawing in the central part



No. FJ008-D-R-S1-1.0

| | | | |
|-------------------|------------------|------|-------|
| TITLE | SOP8J-D-Reel | | |
| No. | FJ008-D-R-S1-1.0 | | |
| ANGLE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |

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