Contents

CMOS POWER MANAGEMENT IC

S-8470 Series

The S-8470 Series is a CMOS power management IC for portable telephones. It contains a watchdog timer circuit, in addition to four series-type voltage regulators and four voltage detectors.

■ Features

- Four built-in high-precision voltage regulators with external transistors, whose accuracies are ±2%.
  REG4 can have a MOS FET built-in.
  These output voltages can be selected by 0.1 V step between 2 V and 6 V.
- Four built-in high-precision voltage detectors, whose accuracies are ±2%.
  One of them can set a delay time with an external capacitor. (S-8470AFS/CFS)
  These detection voltages can be selected by 0.1 V step between 2 V and 6 V.
  The detection pins are selected from V_{IN} or V_{OUT} by option.
- Built-in watchdog timer circuit that detects MPU runaway and generates a $\overline{\text{RESET}}$ signal: Can set the time out period with an external capacitor (5 s max.) (S-8470AFS/CFS)
- Low current consumption
- All voltage regulators and voltage detectors with the exception of $\overline{\text{RESET}}$ can be powered on/off. In the S-8470CFS, $\overline{\text{RESET}}$ can be powered on/off.
- There are 3 different type in the series, S-8470AFS/BFS/CFS, whose functions vary according to $\overline{\text{RESET}}$ signal and the watchdog timer.
- 24-pin shrink SOP package (pin pitch : 0.8 mm)

■ Applications

- Portable telephone
- Next generation cordlessphone
- Two-way radio equipment
- Other portable equipment

■ Selection Guidelines for $\overline{\text{RESET}}$ and the Watchdog Timer

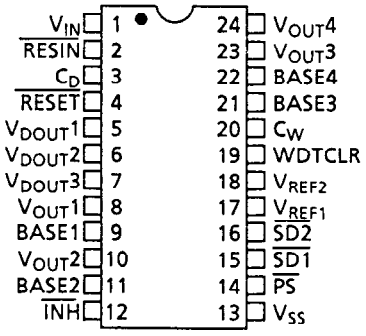
Table 1

Name of series	Functions
S-8470AFS	Always operates $\overline{\text{RESET}}$: (Delay time can be specified using an external capacitor) Can shutdown the watchdog timer.
S-8470BFS	Always operates $\overline{\text{RESET}}$. No watchdog timer.
S-8470CFS	Can shutdown $\overline{\text{RESET}}$: (Delay time can be specified using an external capacitor) and a watchdog timer.

■ Pin Assignment

1. S-8470AFS/CFS

24 pinSSOP
Top view



2. S-8470BFS

24 pinSSOP
Top view

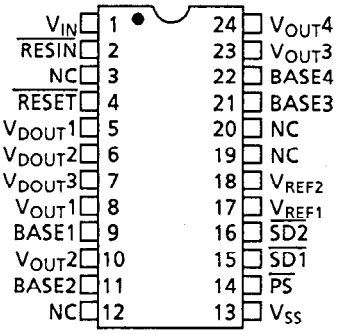
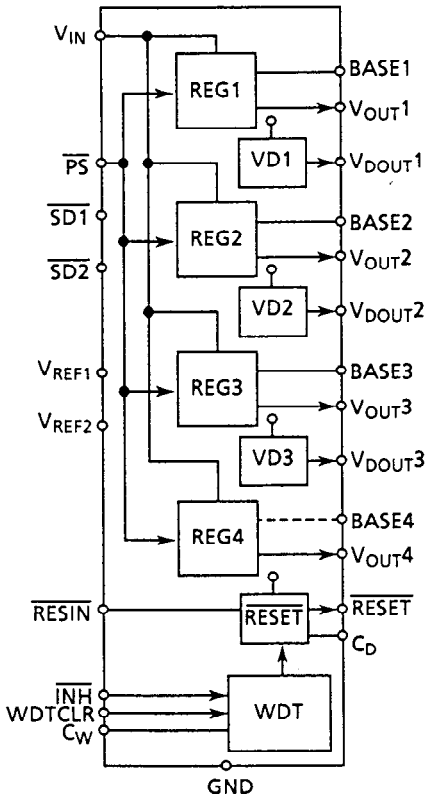


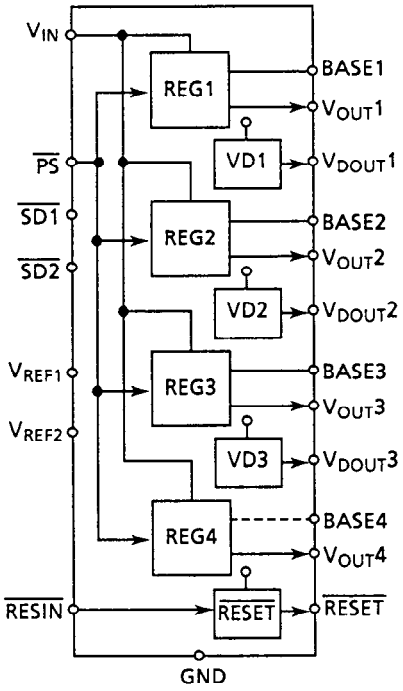
Figure 1

■ Block Diagram

1. S-8470AFS



2. S-8470BFS



3. S-8470CFS

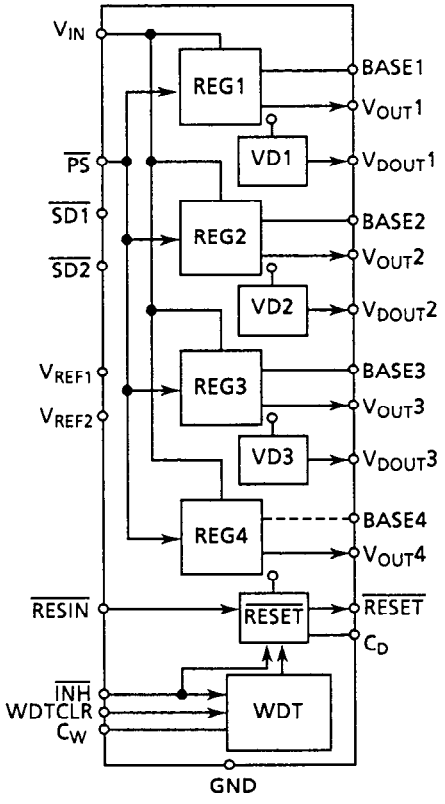


Figure 2

WDT = Watchdog timer
SD1 and SD2 = Shutdown pin

■ Options

Table 2

Item	Applicable pin	Contents of option
Pin to detect the voltage of voltage detectors	VD1	One of V_{IN}, $V_{OUT}1$, $V_{OUT}2$, $V_{OUT}3$, $V_{OUT}4$
	VD2	One of V_{IN}, $V_{OUT}1$, $V_{OUT}2$, $V_{OUT}3$, $V_{OUT}4$
	VD3	One of V_{IN}, $V_{OUT}1$, $V_{OUT}2$, $V_{OUT}3$, $V_{OUT}4$
	RESET	One of V_{IN}, $V_{OUT}1$, $V_{OUT}2$, $V_{OUT}3$ $V_{OUT}4$
Output voltage of voltage detectors during shutdown	VD1	"L" or "Hi-Z"
	VD2	"L" or "Hi-Z"
	VD3	"L" or "Hi-Z"
	RESET**	"L" or "Hi-Z"
Shutdown control input	SD1*	Shutdown of REG1, REG2, REG3, REG4, VD1, VD2, VD3
	SD2*	Shutdown of REG1, REG2, REG3, REG4, VD1, VD2, VD3
Shutdown prohibition		Shutdown prohibition of REG1, REG2, REG3, REG4, VD1, VD2, VD3
Power transistor of voltage regulators	REG4	Internal or External
Output voltage of voltage regulators and detection voltage of voltage detectors	VD1 to VD3, RESET, REG1 to REG4	Can be set freely by 0.1 V step between 2 V and 6 V (Accuracy : ± 2%)

* It cannot be allowed that shutdown of any circuit is controlled by two or more SD inputs.
** RESET signal is output when INH = "L" (the S-8470CFS only)
Please contact our sales department on other options than Table 1.

■ Pin Description

Table 3

Name	Description	Shutdown
V_{IN}	Positive power input of REG1 to REG4	
BASE1	Base current sink terminal to connect to the base of the external PNP transistor of REG1	V_{IN}
$V_{OUT}1$	REG1 output	Hi-Z
BASE2	Base current sink terminal to connect to the base of the external PNP transistor of REG2	V_{IN}
$V_{OUT}2$	REG2 output	Hi-Z
BASE3	Base current sink terminal to connect to the base of the external PNP transistor of REG3	V_{IN}
$V_{OUT}3$	REG3 output	Hi-Z
BASE4	Base current sink terminal to connect to the base of the external PNP transistor of REG4 (NC when using the built-in MOS FET of REG4)	V_{IN}
$V_{OUT}4$	REG4 output	Hi-Z
$\overline{SD1}$ to $\overline{SD2}$	Shutdown control signals input of REG1 to REG4 and VD1 to VD3	
$\overline{PS}$	Current consumption alternative signal input of REG1 to REG4	
$V_{DOUT}1$ to $V_{DOUT}3$	VD1 to VD3 Nch opendrain output	L or Hi-Z
$\overline{RESET}$	Nch opendrain output of voltage detector (VD) for generating $\overline{RESET}$	L or Hi-Z
$\overline{RESIN}$	Compulsory $\overline{RESET}$ signal input of VD for generating $\overline{RESET}$	
C_D*	Output terminal to connect the capacitor for output signal delay of VD for generating $\overline{RESET}$	L
WDCLR*	Clear signal input for watchdog timer (WDT)	
C_W*	Output terminal to connect the capacitor for setting timeout period of WDT	L
$\overline{INH}$*	S-8470AFS : Shutdown control signal input for the WDT S-8470CFS : Shutdown control signal input for the WDT and VD for generating $\overline{RESET}$	
V_{REF1}, V_{REF2}	Reference voltage output	
GND	Ground	

* Excluding the S-8470BFS

■ Absolute Maximum Ratings

Table 4

(Unless otherwise specified : Ta = 25°C)

Parameter	Symbol	Applicable terminal	Ratings	Unit
Input voltage	V_{IN}	V_{IN}, $\overline{SD1}$ to $\overline{SD2}$, $\overline{PS}$, $\overline{RESIN}$, WDTCLR, BASE1 to BASE4, $\overline{INH}$	V_{SS} – 0.3 to 12	V
Output voltage of voltage regulators	V_{OUT}	$V_{OUT}1$, $V_{OUT}2$, $V_{OUT}3$, $V_{OUT}4$	V_{SS} – 0.3 to V_{IN} + 0.3	V
Output voltage of voltage detectors	V_{DOUT}	$V_{DOUT}1$ to $V_{DOUT}3$, $\overline{RESET}$	V_{SS} – 0.3 to 12	V
Output current*	I_{OUT}	$V_{OUT}4$	100	mA
Power dissipation	P_D		650	mW
Operating temperature	T_{opr}		– 40 to + 85	°C
Storage temperature	T_{stg}		– 40 to + 125	°C

* When using a built-in MOS FET

DO NOT APPLY the voltage to V_{REF1}, V_{REF2}, C_W**, and C_D**. (** Excluding the S-8470BFS)

■ Electrical Characteristics

1. General

Table 5

(Unless otherwise specified : Ta = 25°C)

Parameter		Symbol	Applicable terminal	Test conditions	Min.	Typ.	Max.	Unit	Test circuit
Current consumption*		I_{REGON}	REG1 to 4	$\overline{SD1}$ to $\overline{2}$ = $\overline{PS}$ = "H" V_{IN} = 6 V	—	6.3	9	μA	1
		I_{REGPS}	REG1 to 4	$\overline{SD1}$ to $\overline{2}$ = "H", $\overline{PS}$ = "L" V_{IN} = 6 V	—	1.4	2	μA	
		I_{REGOF}	REG1 to 4	$\overline{SD1}$ to $\overline{2}$ = "L", V_{IN} = 6 V	—	—	0.1	μA	
		I_{VDON}	VD1 to 3	$\overline{SD1}$ to $\overline{2}$ = "H", V_{IN} = 6 V	—	1.0	2.0	μA	
		I_{VDOF}	VD1 to 3	$\overline{SD1}$ to $\overline{2}$ = "L", V_{IN} = 6 V	—	—	0.1	μA	
		I_{RESON}	$\overline{RESET}$	$\overline{INH}$ = "H", V_{IN} = 6 V	—	1.7	3.5	μA	
		I_{RESOF}**	$\overline{RESET}$	$\overline{SD1}$ to $\overline{2}$ = $\overline{INH}$ = "L" V_{IN} = 6 V	—	—	0.5	μA	
		I_{WDTON}***	WDT	$\overline{INH}$ = "H", V_{IN} = 6 V	—	1.7	3.5	μA	
		I_{WDTOF}***	WDT	$\overline{INH}$ = "L", V_{IN} = 6 V	—	—	0.3	μA	
		I_{REFON}	V_{IN}	V_{IN} = 6 V	—	4.0	7.0	μA	
		I_{REFOF}****	V_{IN}	$\overline{SD1}$ to $\overline{2}$ = $\overline{INH}$ = "L" V_{IN} = 6 V	—	—	0.2	μA	
		I_{DDOF}	V_{IN}	$\overline{SD1}$ to $\overline{2}$ = $\overline{INH}$ = $\overline{PS}$ = "L"	—	—	*****	μA	
	S-8470AFS S-8470CFS	I_{DD1}	V_{IN}	$\overline{SD1}$ to $\overline{2}$ = $\overline{PS}$ = "H", V_{IN} = 6 V	—	36	56	μA	
		I_{DD2}	V_{IN}	$\overline{SD1}$ to $\overline{2}$ = "H", $\overline{PS}$ = "L", V_{IN} = 6 V	—	16	28	μA	
	S-8470BFS	I_{DD1}	V_{IN}	$\overline{SD1}$ to $\overline{2}$ = $\overline{PS}$ = "H", V_{IN} = 6 V	—	34	53	μA	
		I_{DD2}	V_{IN}	$\overline{SD1}$ to $\overline{2}$ = "H", $\overline{PS}$ = "L", V_{IN} = 6 V	—	14	25	μA	
Input threshold voltage		V_{SL}	$\overline{SD1}$ to $\overline{2}$, $\overline{PS}$, $\overline{RESIN}$, $\overline{INH}$	V_{IN} = 6 V "L"	—	—	0.3	V	2, 4
		V_{SH}		V_{IN} = 6 V "H"	2.4	—	—	V	
Operating input voltage		V_{OP}	V_{IN}		2.0	—	10	V	1

* Current consumption per voltage regulator or detector when REG1 through 4 and $\overline{SD1}$ and $\overline{2}$ are connected to the V_{IN} (excluding the BASE current of the external PNP transistor)

** Excluding S-8470AFS/BFS

*** Excluding S-8470BFS

**** Excluding S-8470AFS

***** Refer to the following current consumption calculation method (at the time of shutdown)(S-8470CFS).

At the time of shutdown (when $\overline{SD1}$ to $\overline{2}$ = "L" and $\overline{INH}$ = "L"):
When the IC is not provided with a shutdown prohibition circuit:

$$I_{REGOF} \times 4 + I_{VDOF} \times 3 + I_{RESOF} + I_{WDTOF} + I_{REFOF}$$

During operation (when $\overline{SD1}$ to $\overline{2}$ = $\overline{INH}$ = "H"):

$$I_{REGON} \times 4 + I_{VDON} \times 3 + I_{RESON} + I_{WDTON} + I_{REFON}$$

2. Voltage regulator

Table 6

(Unless otherwise specified : Ta = 25°C)

Parameter	Symbol	Applicable terminals	Test conditions	Min.	Typ.	Max.	Unit	Test circuit
Output voltage	$V_{OUT}1$	$V_{OUT}1$	V_{IN} = 3.2 V, I_{OUT} = 60 mA	2.94	3.00	3.06	V	2
	$V_{OUT}2$	$V_{OUT}2$	V_{IN} = 3.2 V, I_{OUT} = 60 mA	2.94	3.00	3.06	V	
	$V_{OUT}3$	$V_{OUT}3$	V_{IN} = 3.4 V, I_{OUT} = 60 mA	3.136	3.200	3.264	V	
	$V_{OUT}4$*	$V_{OUT}4$	V_{IN} = 3.7 V, I_{OUT} = 15 mA	3.136	3.200	3.264	V	
Output voltage at the time of shutdown	*** $V_{OSD1\sim4}$	$V_{OUT}1$ to 4	V_{IN} = 10 V, Load: 1 MΩ	—	—	0.1	V	
I/O voltage difference*	V_{diff}	$V_{OUT}4$	I_{OUT} = 15 mA	—	0.2	0.35	V	
Line regulation	$\Delta V_{OUTL}1$	$V_{OUT}1$	V_{IN} = 3.2 to 4.8 V, I_{OUT} = 60 mA	—	20	40	mV	
	$\Delta V_{OUTL}2$	$V_{OUT}2$	V_{IN} = 3.2 to 4.8 V, I_{OUT} = 60 mA	—	20	40	mV	
	$\Delta V_{OUTL}3$	$V_{OUT}3$	V_{IN} = 3.4 to 4.8 V, I_{OUT} = 60 mA	—	20	40	mV	
	$\Delta V_{OUTL}4$*	$V_{OUT}4$	V_{IN} = 3.7 to 4.8 V, I_{OUT} = 15 mA	—	20	40	mV	
Load regulation	$\Delta V_{OUTD}1$	$V_{OUT}1$	V_{IN} = 3.2 V, I_{OUT} = 1 to 60 mA	—	25	50	mV	
	$\Delta V_{OUTD}2$	$V_{OUT}2$	V_{IN} = 3.2 V, I_{OUT} = 1 to 60 mA	—	25	50	mV	
	$\Delta V_{OUTD}3$	$V_{OUT}3$	V_{IN} = 3.4 V, I_{OUT} = 1 to 60 mA	—	25	50	mV	
	$\Delta V_{OUTD}4$*	$V_{OUT}4$	V_{IN} = 3.7 V, I_{OUT} = 50 μA to 15 mA	—	25	50	mV	
Output voltage temp. coefficient	$\frac{\Delta V_{OUT}}{\Delta Ta}$	$V_{OUT}1$ to $V_{OUT}4$	Ta = −40°C to +85°C	—	**	—	mV/°C	
Base sink current	*** $I_{SINK\ 1\text{-}4}$	BASE1 to BASE4	V_{IN} = 3.2 V, V_{DS} = 2 V, Base current of transistor	1	—	—	mA	3

2SA1362 or one of whose V_{sat} is less than 0.1 V (I_{OUT} = 60 mA) is used as an external transistor.

* When using a built-in MOS FET.
The specification when using an external transistor is the same as $V_{OUT}3$.

** Equation parameter : $\pm 0.71 \times \frac{V_{OUT}1 \text{ to } V_{OUT}4 \text{ (typ.)}}{5.0}$

*** I_{SINK4} and I_{BLEAK4} are not specified when using a built-in MOS FET.

3. Voltage detector

Table 7

(Unless otherwise specified: Ta = 25°C)

Parameter	Symbol	Applicable terminals	Test conditions	Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET1}$	$V_{DOUT}1$		3.234	3.300	3.366	V	4
	$-V_{DET2}$	$V_{DOUT}2$		3.724	3.800	3.876	V	
	$-V_{DET3}$	$V_{DOUT}3$		3.626	3.700	3.774	V	
	$-V_{RESET}$	$\overline{RESET}$		2.94	3.00	3.06	V	
Release voltage	$+V_{DET1}$	$V_{DOUT}1$		3.329	3.465	3.601	V	
	$+V_{DET2}$	$V_{DOUT}2$		3.847	3.990	4.133	V	
	$+V_{DET3}$	$V_{DOUT}3$		3.743	3.885	4.027	V	
	$+V_{RESET}$	$\overline{RESET}$		2.981	3.100	3.219	V	
Detection vol. temp. coefficient	$\frac{\Delta -V_{DET}}{\Delta Ta}$	$V_{DOUT}1$ to 3, $\overline{RESET}$	Ta = −40°C to +85°C	—	*	—	mV/°C	
Sink current	I_{OL}		V_{DS} = 0.5 V, V_{IN} = 2.0 V	1.00	1.60	—	mA	
Leakage current	I_{LEAK}	$V_{DOUT}1$ to 3, $\overline{RESET}$	V_{DS} = 10 V, V_{IN} = 10 V	—	—	0.1	μA	5
Delay time**	t_d	$\overline{RESET}$	C_D = 4.7 nF	31	45	59	ms	6

* Equation parameter: $\pm 0.5 \times \frac{-V_{DET}1 \text{ to } -V_{DET}3 \text{ (typ.) or } -V_{RESET} \text{ (typ.)}}{4.2}$

** Equation parameter for the delay time (ms): 9.6 x capacitor (nF) (Excluding the S-8470BFS)

4. Watchdog timer (Excluding the S-8470BFS)

Table 8

(Unless otherwise specified: Ta = 25°C)

Parameter	Symbol	Applicable terminals	Test conditions	Min.	Typ.	Max.	Unit	Test circuit
Timeout period*	t_{OUT}	$\overline{RESET}$	C_W = 4.7 nF	31	45	59	ms	7
Input threshold voltage	V_{SL}	WDTCLR	V_{IN} = 3.3 V, "L"	—	—	0.3	V	8
	V_{SH}		V_{IN} = 3.3 V, "H"	1.5	—	—	V	
Input pulse width	t_W	WDTCLR	V_{IN} = 3.3 V, "H"	50	—	1000	μs	

* Equation parameter for the timeout period (ms): 9.6 x capacitor (nF)

■ Test Circuits

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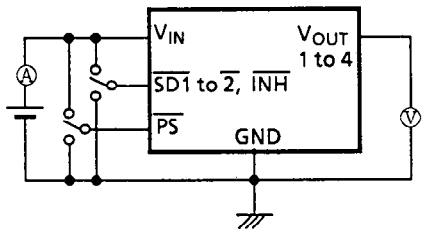

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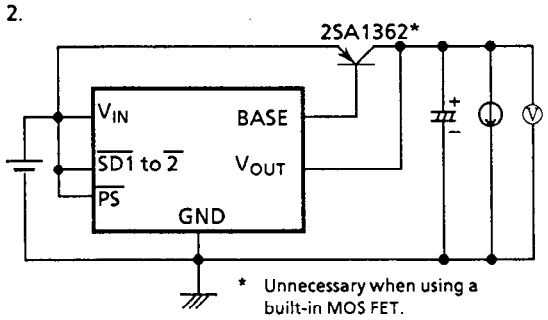

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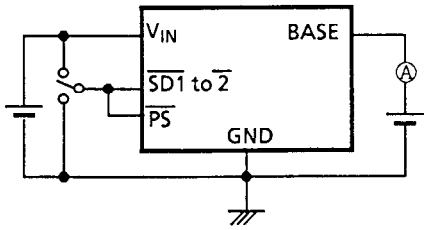

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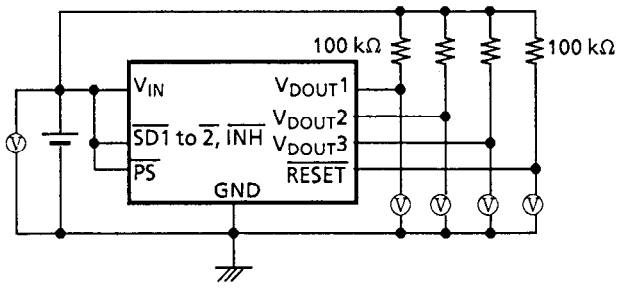

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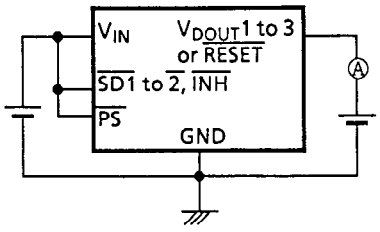

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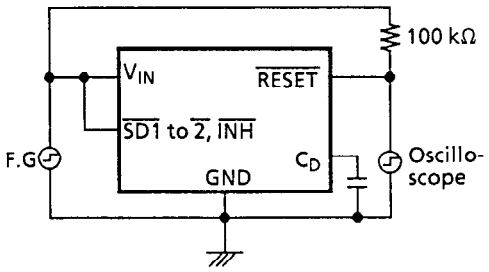

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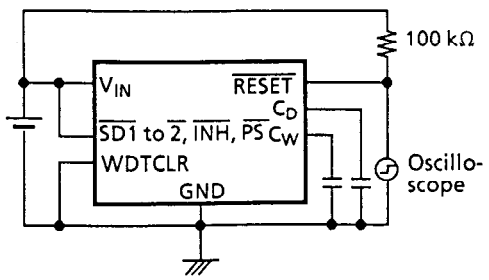

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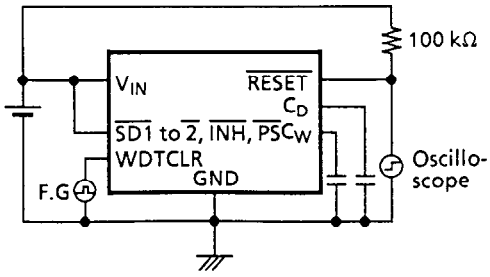
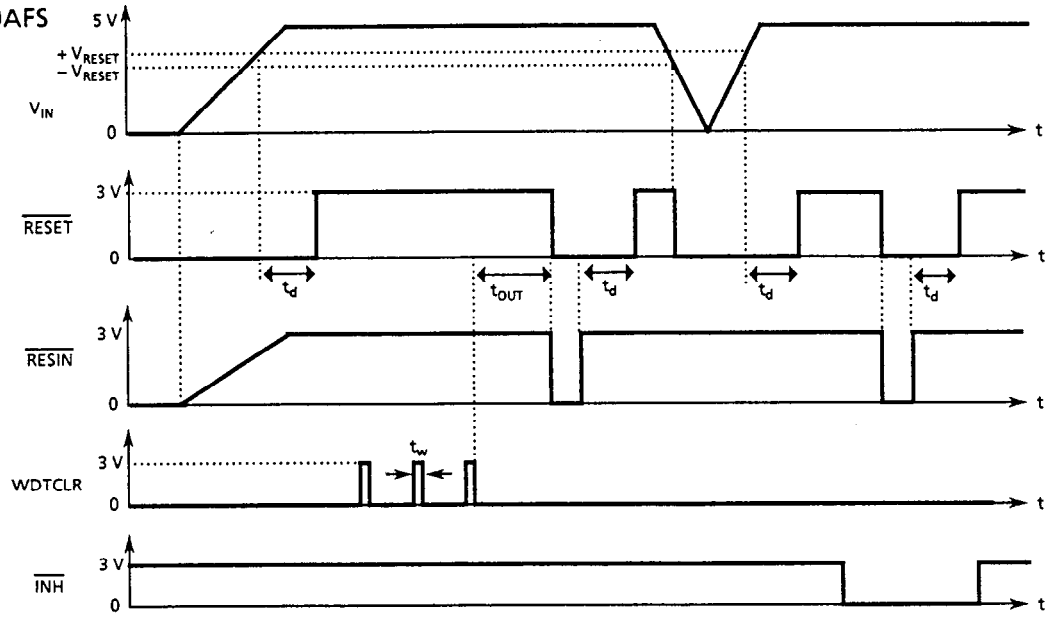


** Excluding the S-8470BFS

Figure 3

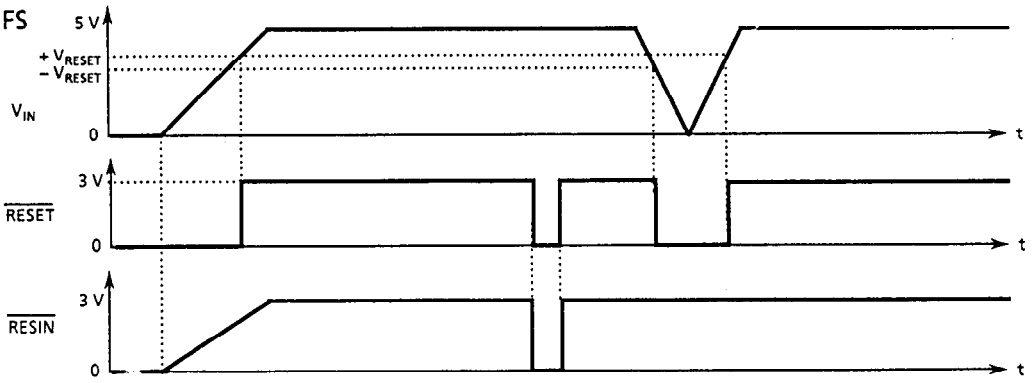
■ Operation Timing Chart

1. S-8470AFS



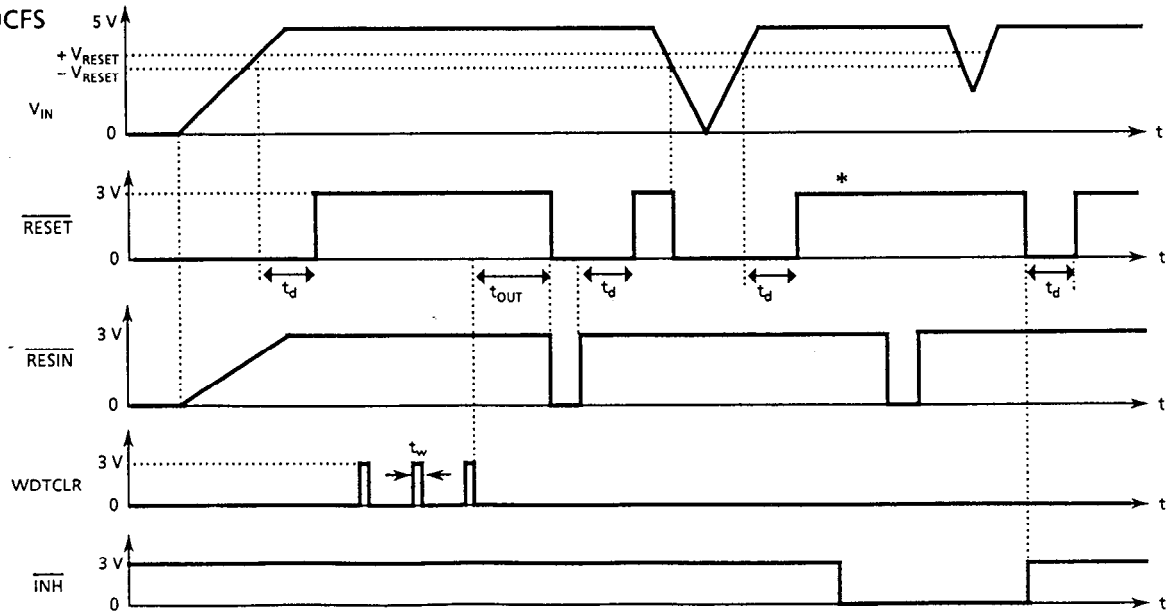
• The $\overline{\text{RESET}}$ detector is connected to $V_{OUT}4$, and its output is pulled up to $V_{OUT}4$.

2. S-8470BFS



• The $\overline{\text{RESET}}$ detector is connected to $V_{OUT}4$, and its output is pulled up to $V_{OUT}4$.

3. S-8470CFS



• The $\overline{\text{RESET}}$ detector is connected to $V_{OUT}4$, and its output is pulled up to $V_{OUT}4$.
* When $\overline{\text{INH}}$ = "L", $\overline{\text{RESET}}$ is set to "Hi - Z".

Figure 4

■ Operation

The S-8470 Series consists of four voltage regulators, three voltage detectors, a shutdown input circuit, a voltage detector with delay circuit for generating $\overline{\text{RESET}}$, and a watchdog timer. (The S-8470BFS is provided with neither a delay circuit for $\overline{\text{RESET}}$ nor a watchdog timer)

1. High-precision voltage regulators (REG1, REG2, REG3, and REG4)

The S-8470 Series contains four voltage regulators, each of whose output voltages can set independently by 0.1 V step between 2 V and 6 V. The accuracy of their output voltages is ±2%.

REG1, REG2 and REG3: Can be used as voltage regulator with large output current, by connecting a PNP transistor externally

REG4: Can be selected by option from large output current type by a PNP transistor and built-in MOS FET type.

The S-8470AFS has a reference voltage circuit. It outputs 1.2 V of reference voltage to V_{REF1}, V_{REF2} terminal, which required 0.1 μF of capacitor. This voltage is supplied to all the voltage regulators and detectors. This standard voltage circuit halts its function when $\overline{\text{SD1}}$, $\overline{2}$ and $\overline{\text{INH}}$ are all turned "L." This enables the current consumption to be reduced to 0.2 μA (I_{REFOF}) (in the S-8470AFS, however, the standard voltage circuit is always operating). It becomes shutdown status (I_{REGOF} = 0.1 μA max.) when $\overline{\text{SD1}}$ and $\overline{\text{SD2}}$ go low.

The voltage regulator (REG4) with an internal MOSFET turns OFF the M1 transistor; or the voltage regulator with an external PNP transistor cuts off the sink current of the BASE, and shortcircuits between the BASE and the EMITTER of the external transistor via the internal transistor. This enables the output voltage to be set to approximately 0 V.

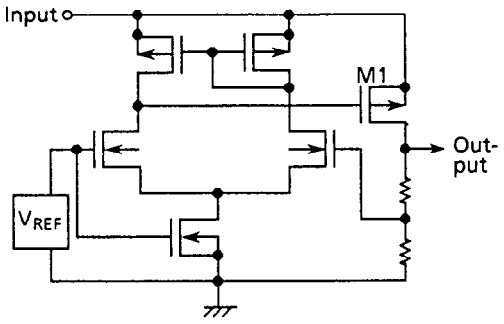


Figure 5 Voltage regulator with built-in MOS FET

$\overline{\text{PS}}$ changes the current consumption per voltage regulator: 9 μA max. when $\overline{\text{PS}}$ is high, and 2 μA max. when $\overline{\text{PS}}$ is low. This terminal is used for reducing current consumption, under voltage being kept to output to REG1 to REG4. Note that output load current (I_{OUT}) must be less than 10 mA during 2 μA max. mode.

[I/O voltage diffrence V_{diff}]

When using REG4 with built-in MOS FET, Vinitial represents the V_{OUT} when V_{IN} = 3.7 V and I_{OUT} = 15 mA. Inputting (Vinitial + V_{diff}) to V_{IN} causes output of 95% of Vinitial to V_{OUT} temrinal.

NOTES: Because a short-circuit protection circuit and an thermal shutdown circuit are not mounted in REG1 to REG4, use REG1 to REG4 within the power dissipation of the package.

When using the built-in transistor at $V_{OUT}4$, set $\overline{\text{PS}}$ to "H."

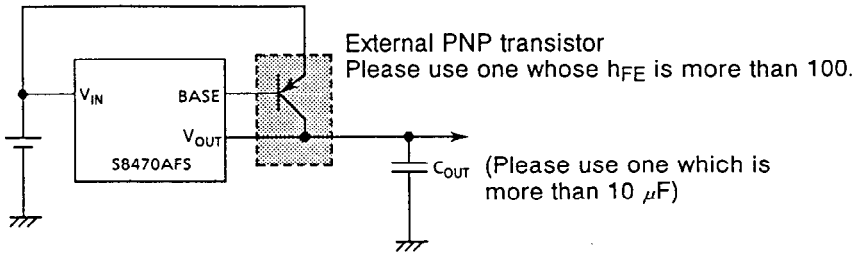


Figure 6 Voltage regulator with external PNP transistor

2. Voltage detectors (VD1, VD2, and VD3)

The S-8470 Series has three voltage detectors, each of whose detection terminal is selected by option as Table 8. The power is suppplied from V_{IN}. The output forms are Nch opendrain. Using shutdown function by $\overline{SD1}$ to $\overline{SD2}$ realises a power save system. The output logic of voltage detectors during shutdown is selected from low and high impedance by option (see Table 9).

NOTE: Output is undefined when V_{IN} terminal voltage is less than 2 V.
Please use about 100 kΩ of pull up resistor.

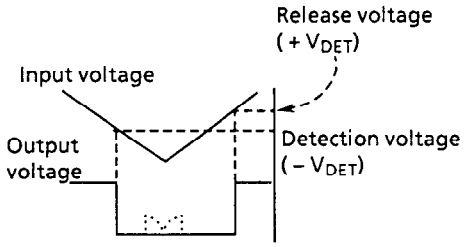


Figure 7 Waveform of voltage detector

Table 9 Detection voltage of voltage detectors

Voltage detectors	Detected terminal	Detection voltage value	Output during shutdown
VD1 to VD3	One of V_{IN}, $V_{OUT}1$, $V_{OUT}2$, $V_{OUT}3$ and $V_{OUT}4$	Can be set by 0.1 V step between 2 V and 6 V	"L" or "Hi-Z" (selected by option)

3. Shutdown circuit (applied to $\overline{SD1}$ to $\overline{SD2}$, $\overline{PS}$ and $\overline{INH}$)

The shutdown circuit, constructed by MOS transistor gate input, is high impedance, therefore input bias current is nearly zero or about 100 pA at most. The S-8470AFS is in shutdown status while $\overline{SD}$ is low.
No element exists between power supply (V_{IN}) of this circuit and $\overline{SD1}$, and input voltage up to 12 V (maximum rating) can be applied to $\overline{SD1}$, regardless of V_{IN} temrinal input voltage.
Do not fail to connect $\overline{SD1}$ to $\overline{SD2}$, $\overline{PS}$ and $\overline{INH}$* to V_{IN}, while the shutdown circuit is not used.

* Excluding the S-8470BFS

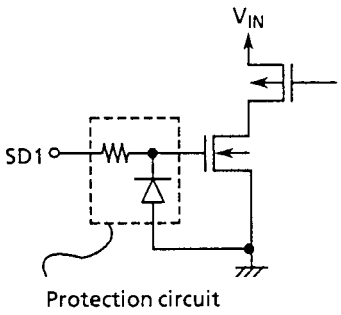


Figure 8 Shutdown input circuit

NOTES:
- High level is specified at 2.4 V or more, and low level at 0.3 V or less. Some variation may occur depending on the supply voltage.
- Negative voltage should not be applied because the V_{IN} terminal and GND terminal are connected by a protection diode.
- Do not float the input terminal or set voltages between levels low and high . This will increase the quiescent current.

4. Voltage detector for generating $\overline{\text{RESET}}$ with delay circuit

This is a voltage detector for generating $\overline{\text{RESET}}$ with built-in delay circuit, whose output form is Nch opendrain. The voltage detector (VD) for generating $\overline{\text{RESET}}$ runs all the while 2 V or more of voltage is applied to V_{IN}. The external capacitor (C_D) is charged at the constant current by a constant current source (I_C = 125 nA). Comparator output goes high when V_C is higher than the reference voltage (V_{REF}) , and a signal is output. The time until V_C becomes V_{REF} is the delay time (or undetected momentary power fail time or time-out period) and can be calculated by the following equation. Calculate the capacitor value from the necessary delay time.

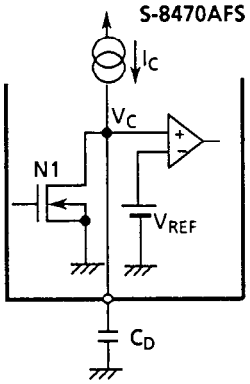


Figure 9 Delay circuit

Delay time (ms) = delay coefficient * × C (nF)

* 6.5 ≦ delay coefficient ≦ 12.6 (9.6 typ., Ta = 25 °C)

No delay occurs at a fall edge because the external capacitor discharges rapidly through transistor N1. Determine the capacitor value (≦70 nF) from the necessary delay time. Open the terminal if the delay time is unnecessary. (In this case, a propagation delay of about 400 μs occurs, depending on the internal parasitic capacity.) If the C_D terminal is connected to the GND terminal, VD for generating $\overline{\text{RESET}}$ does not release and $\overline{\text{RESET}}$ holds low.
The VD for generating $\overline{\text{RESET}}$ outputs $\overline{\text{RESET}}$ signal under two status besides voltage drop. One status is when $\overline{\text{RESET}}$ goes compulsory low by turning $\overline{\text{RESIN}}$ to low. Another is when the watchdog timer is timed out. In latter case, $\overline{\text{RESIN}}$ returns to high after the delay time to be set after timeout period. $\overline{\text{RESIN}}$ has the same characteristics as that of the input terminal of the shutdown circuit.

S-8470AFS: Regardless of the input state of $\overline{\text{SD1}}$ and $\overline{2}$, it runs the VD for generating $\overline{\text{RESET}}$, as long as 2 V or more is applied to V_{IN}.

S-8470CFS: Turning $\overline{\text{INH}}$ to "L" forces the output of the $\overline{\text{RESET}}$ pin to go either "L" or "Hi-Z." (by option) However, it still functions as a voltage detector. If there is an interrupt forcing $\overline{\text{RESET}}$ to go "L" while $\overline{\text{INH}}$ is "L," when $\overline{\text{INH}}$ goes "H," $\overline{\text{RESET}}$ goes "L." Also, when turning $\overline{\text{SD 1}}$ and 2 to "L," it quits its voltage detection function. This allows the current consumption to be reduced to 0.5 μA or less. The output at that time can be selected either "L" or "Hi-Z." (by option)

4.2 Voltage Detector Without A Delay Circuit (S-8470BFS)

Regardless of the input state of $\overline{\text{SD1}}$ and $\overline{2}$, VD for generating $\overline{\text{RESET}}$ is operating. This is because VD for generating $\overline{\text{RESET}}$ is provided with an independent the reference voltage circuit, as long as 2 V or more are applied to the V_{IN}. The voltage detector for generating $\overline{\text{RESET}}$ detects the drop in the voltage and also forces the $\overline{\text{RESET}}$ output to go low by setting the $\overline{\text{RESET}}$ pin to "L" (GND).

NOTES:
- The $\overline{\text{RESIN}}$ pin has the same characteristic as in the input circuit of the power-off input pin.
- Keep open $\overline{\text{RESIN}}$ when not used, because it is internally pulled up 100 kΩ to V_{IN}. Do not apply voltage except for the GND level to the C_D terminal.
- The output of the VD for generating $\overline{\text{RESET}}$ is undefined when less than 2 V of voltage is applied to V_{IN}. Please use about 100 kΩ of pull up resistor, because the output level is Nch open-drain.

Table 10 Detection voltage of VD for $\overline{\text{RESET}}$

Voltage detector	Detected terminal	Detection voltage value	Outputs when the $\overline{\text{INH}}$ pin is "L." *
$\overline{\text{RESET}}$	One of V_{IN}, $V_{OUT}1$, $V_{OUT}2$, $V_{OUT}3$ and $V_{OUT}4$	Can be set by 0.1 step between 2 V and 6V	"L" or "Hi-Z" (by option)

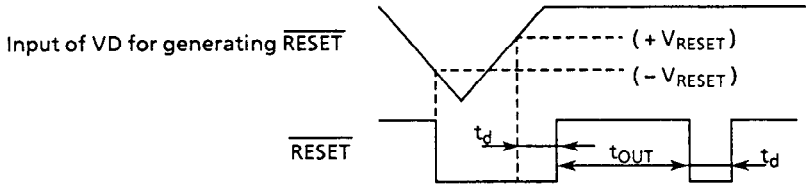
* For only S-8470CFS

5. Watchdog timer (Excluding the S-8470BFS)

If the voltage of input terminal of VD for generating $\overline{\text{RESET}}$ exceeds release voltage ($+V_{RESET}$), $\overline{\text{RESET}}$ goes high. (A delay is enabled by mounting an external capacitor on the C_D terminal.) The timer is cleared if a positive pulse is input to the WDTCLR terminal within the timeout period (set by the value of the external capacitor mounted on the C_W terminal). However, if the positive pulse is not input, $\overline{\text{RESET}}$ goes low. If the voltage of input terminal is more than detection voltage ($-V_{RESET}$), $\overline{\text{RESET}}$ goes high again after the delay time by the external capacitor mounted on the C_D terminal. This procedure is shown in Figure 10. To clear the watchdog timer, apply a positive pulse with width of 50 to 1000 μs at height wave of 2.4 V or more to the WDTCLR terminal. (If a larger pulse is applied, a quiescent current of 1 mA continues to flow for the period beyond 1000 μs.) The WDTCLR terminal has the same characteristics as the input circuit of the shutdown terminal. When you want to shut down the watch dog timer, set the $\overline{\text{INH}}$ pin to "L" (GND). In the S-8470CFS, turning the $\overline{\text{INH}}$ pin "L" forces output of the $\overline{\text{RESET}}$ pin to go "L" or "Hi-Z" (by option).

NOTE: • Do not open the C_W terminal or apply voltage of except for the GND level.

• If voltage is applied to the V_{IN} terminal, the WDTCLR terminal should not be floated, or a



Timeout period t_{OUT} (ms) = 9.6 x C_W capacitor value (nF, ≦ 520 nF)

Figure 10 Timing of the watchdog timer

■ Transient Response

1. Transient Response Characteristics at Power ON

Overshoot or undershoot occurs in the output voltage at the power ON. This section describes parameter dependency characteristics for both overshoot and undershoot. For reference, Figure 12 depicts the measuring circuit.

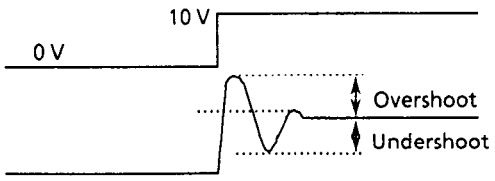


Figure 11

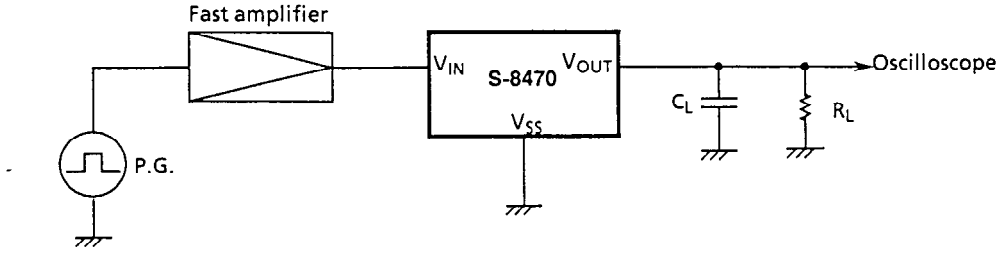


Figure 12

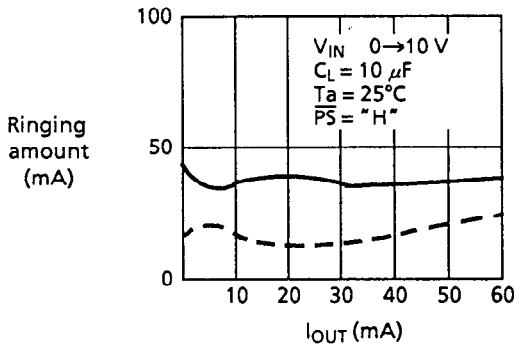
Table 11 Transient Response Parameter Dependency at Power ON

Parameter	Conditions	Method to decrease overshoot	Method to decrease undershoot
Output current I_{OUT}	External : 60 mA max Internal : 15 mA max	—	—
Load capacitance C_L		—	Increase
Power supply voltage V_{IN}	10 V max	—	—
Temperature Ta	-40 to +85°C	Low temperature	Low temperature

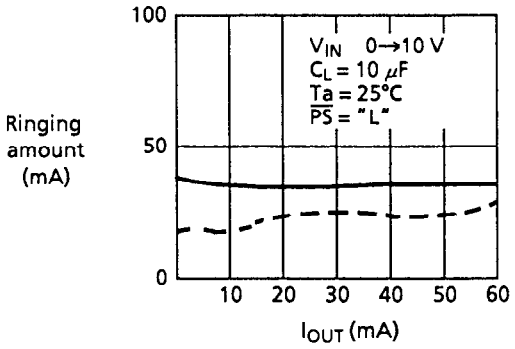
Reference Data When Powering On

1. I_{OUT} dependency

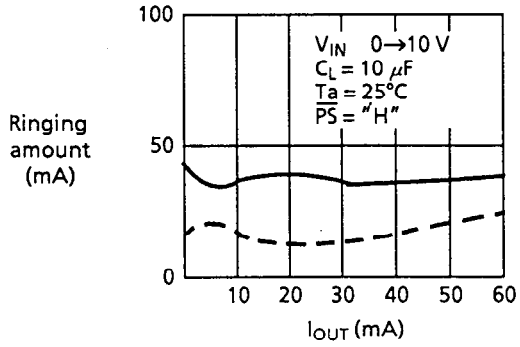
1.1 V_{OUT1}, V_{OUT2}



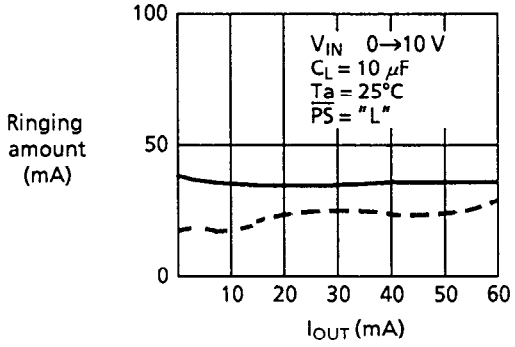
1.2 V_{OUT1}, V_{OUT2}



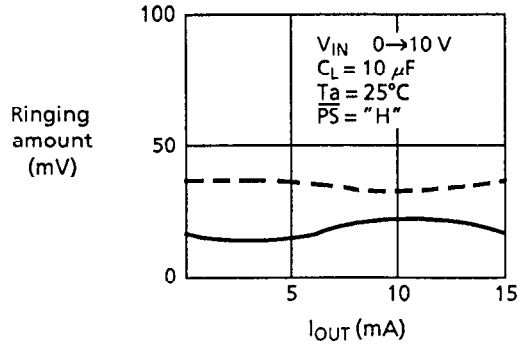
1.3 V_{OUT3}, V_{OUT4} (external transistor)

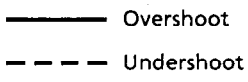


1.4 V_{OUT3}, V_{OUT4} (external transistor)



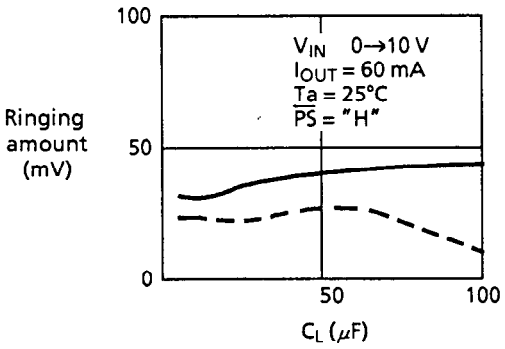
1.5 V_{OUT4} (internal transistor)



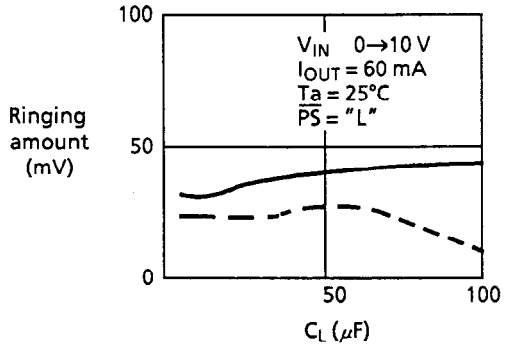


2. C_L dependency

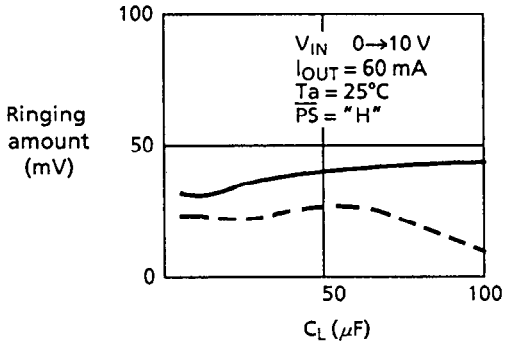
2.1 V_{OUT1}, V_{OUT2}



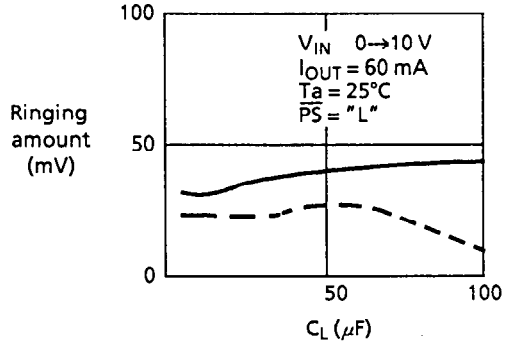
2.2 V_{OUT1}, V_{OUT2}



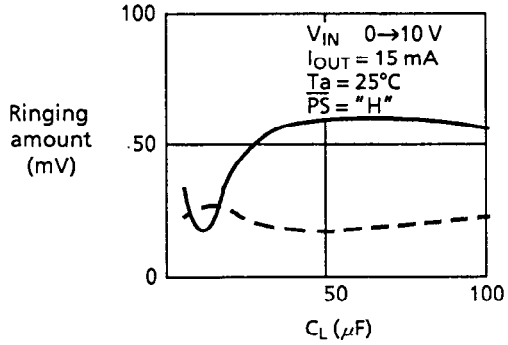
2.3 V_{OUT3}, V_{OUT4} (external transistor)

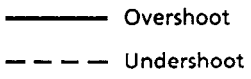


2.4 V_{OUT3}, V_{OUT4} (external transistor)



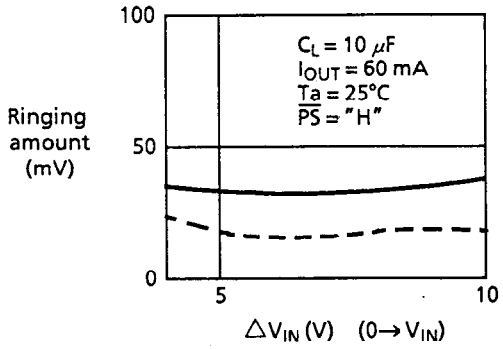
2.5 V_{OUT4} (internal transistor)



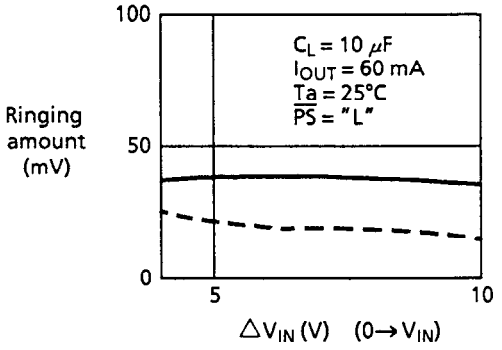


3. V_{IN} dependency

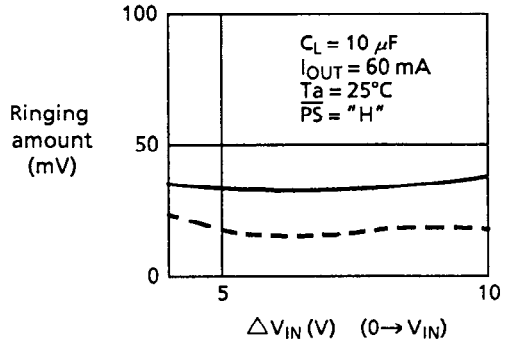
3.1 V_{OUT1}, V_{OUT2}



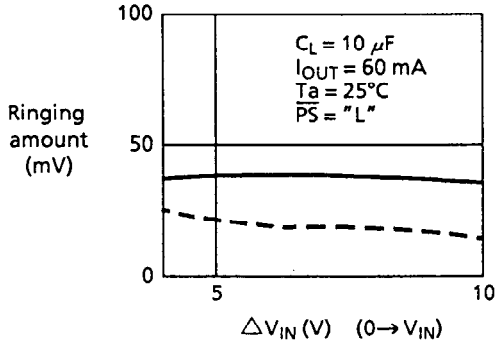
3.2 V_{OUT1}, V_{OUT2}



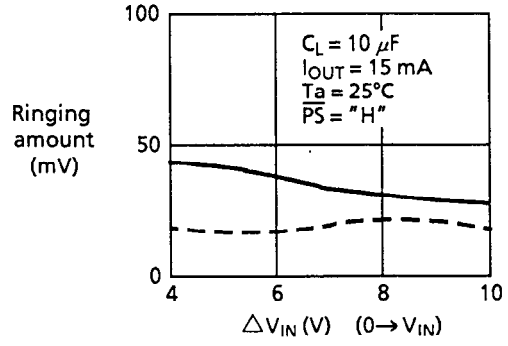
3.3 V_{OUT3}, V_{OUT4} (external transistor)

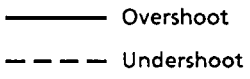


3.4 V_{OUT3}, V_{OUT4} (external transistor)



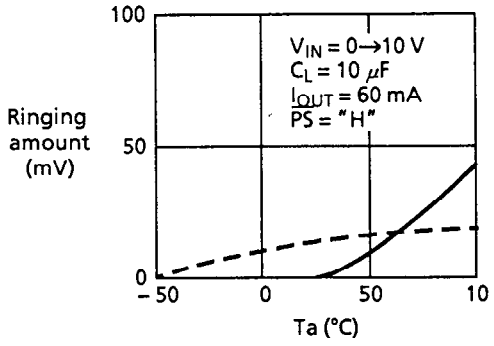
3.5 V_{OUT4} (internal transistor)



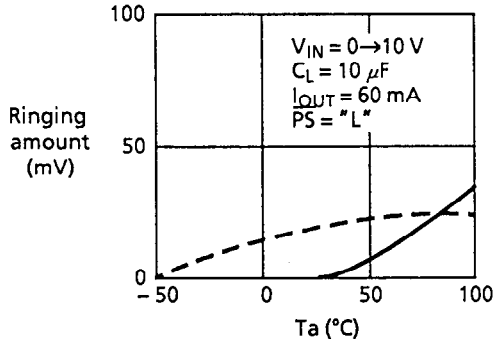


4. Temperature dependency

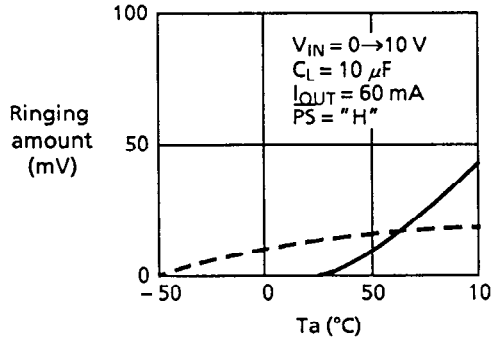
4.1 V_{OUT1}, V_{OUT2}



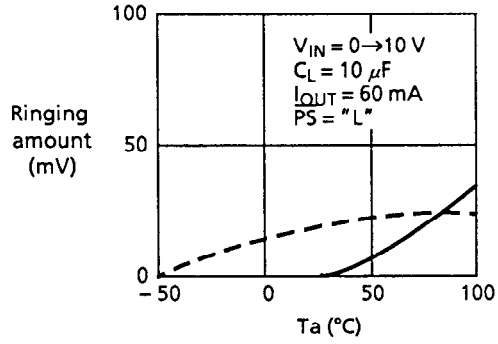
4.2 V_{OUT1}, V_{OUT2}



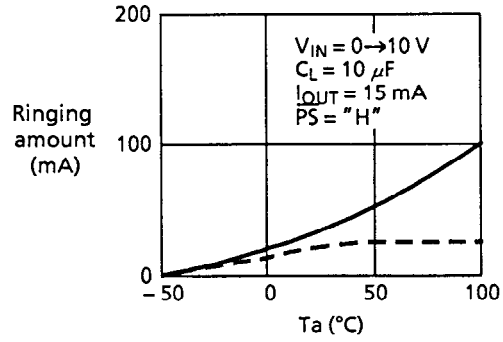
4.3 V_{OUT3}, V_{OUT4} (external transistor)

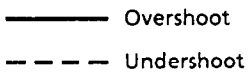


4.4 V_{OUT3}, V_{OUT4} (external transistor)



4.5 V_{OUT4} (internal transistor)





2. Transient Response Characteristics When Input Voltage Varies

Overshoot or undershoot occurs in the output voltage when the input voltage varies. This section describes parameter dependency characteristics for both overshoot and undershoot. For reference, Figure 14 depicts the measuring circuit.

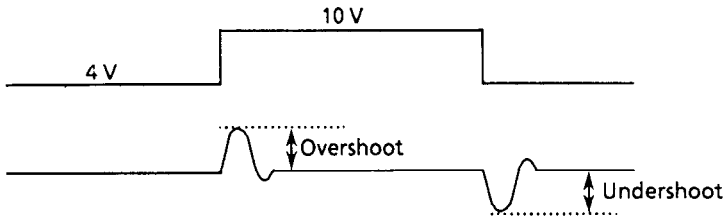


Figure 13

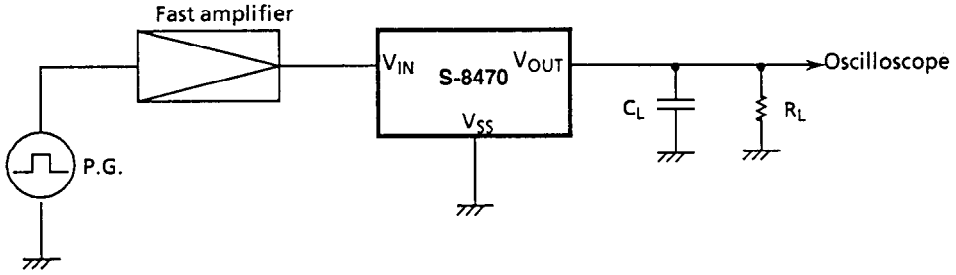


Figure 14 Measuring Circuit

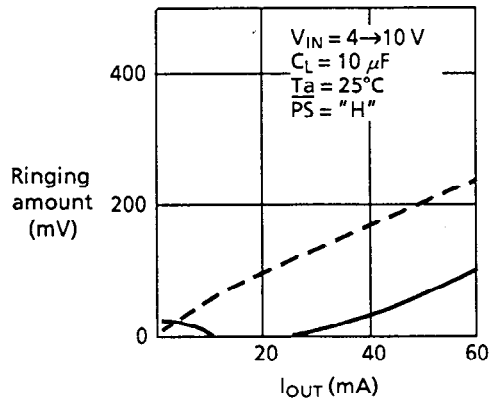
Table 12 Transient Response Parameter Dependency When Input Voltage Varies

Parameter		Conditions	Method to decrease overshoot	Method to decrease undershoot
Output current	I_{OUT}	External : 60 mA max Internal : 15 mA max	Decrease	Decrease
Load capacitance	C_L		Increase	Increase
Input voltage variation	$\triangle V_{IN}$	4~10 V	Decrease	Decrease
Temperature	Ta	- 40 to 85 °C	——	High temperature

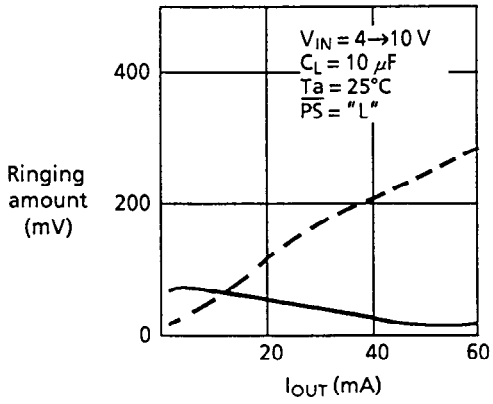
Reference Data When Input Voltage Varies

1. I_{OUT} dependency (V_{IN} = 4 V→10 V)

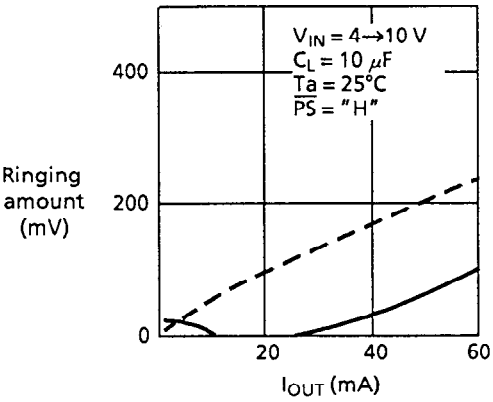
1.1 V_{OUT1}, V_{OUT2}



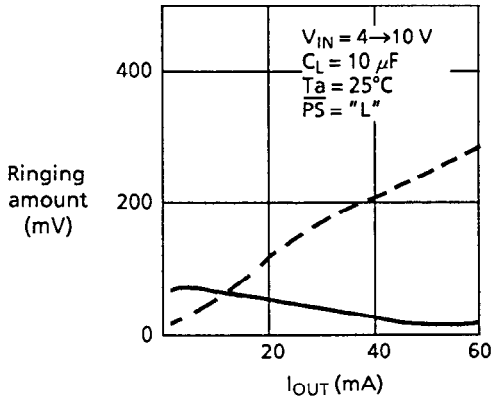
1.2 V_{OUT1}, V_{OUT2}



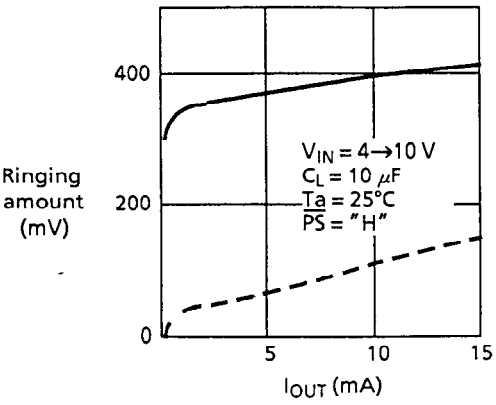
1.3 V_{OUT3}, V_{OUT4} (external transistor)

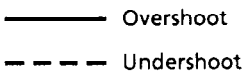


1.4 V_{OUT3}, V_{OUT4} (external transistor)



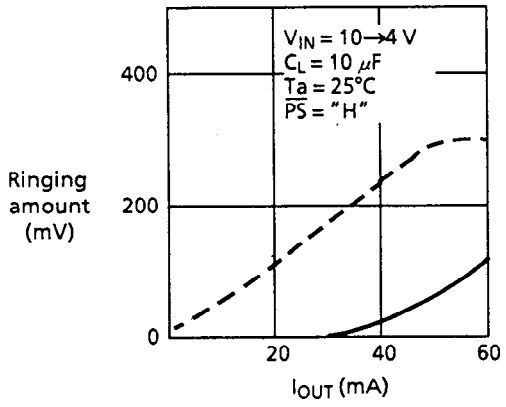
1.5 V_{OUT4} (internal transistor)



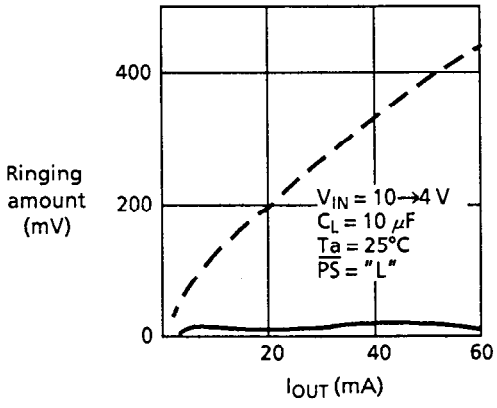


2. I_{OUT} dependency (V_{IN} = 10 V→4 V)

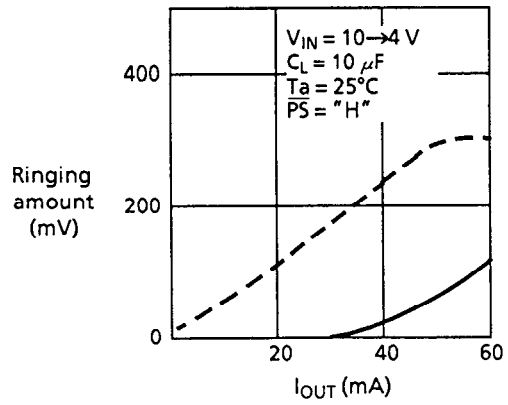
2.1 V_{OUT1}, V_{OUT2}



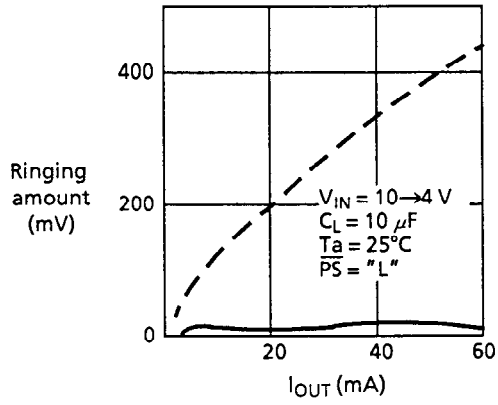
2.2 V_{OUT1}, V_{OUT2}



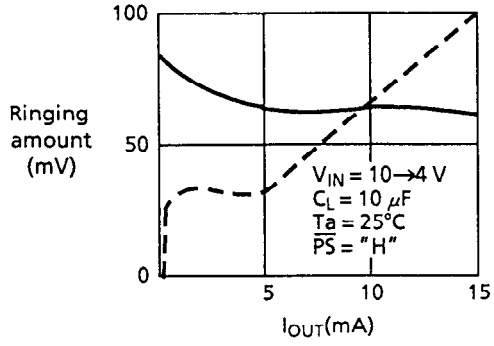
2.3 V_{OUT3}, V_{OUT4} (external transistor)

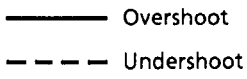


2.4 V_{OUT3}, V_{OUT4} (external transistor)



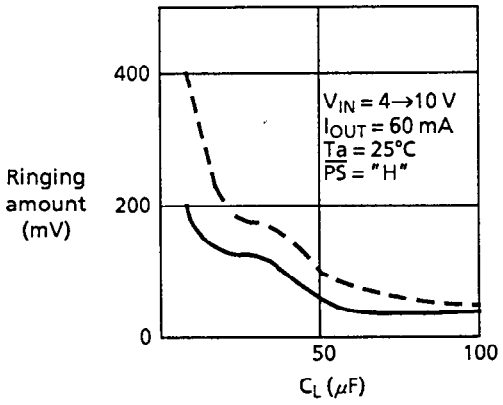
2.5 V_{OUT} (internal transistor)



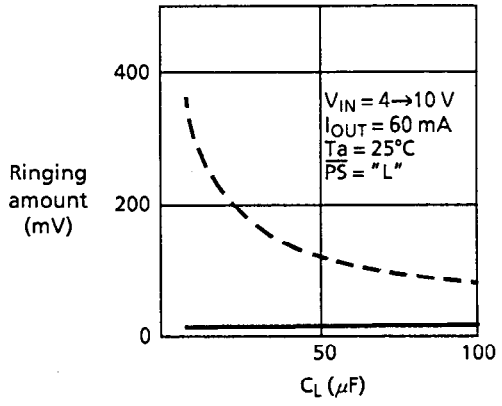


3. C_L dependency (V_{IN} = 4 V→10 V)

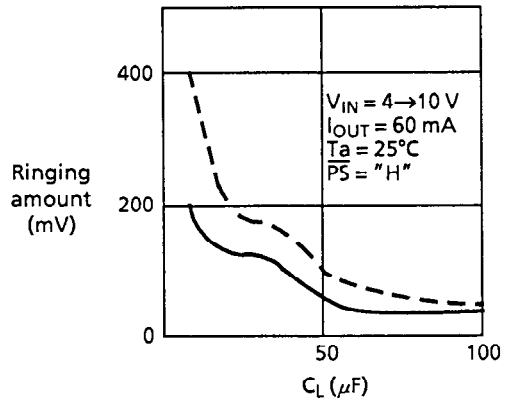
3.1 V_{OUT1}, V_{OUT2}



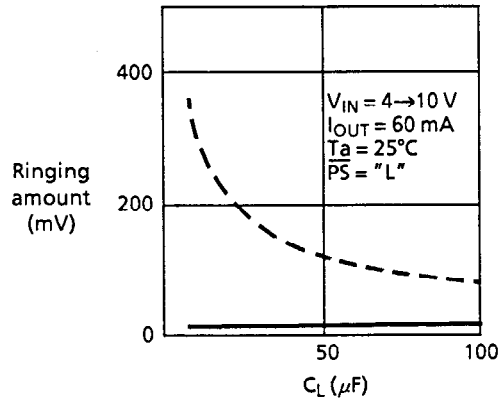
3.2 V_{OUT1}, V_{OUT2}



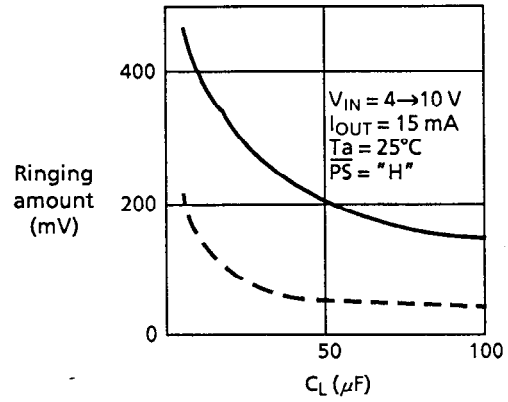
3.3 V_{OUT3}, V_{OUT4} (external transistor)

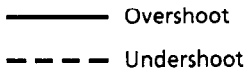


3.4 V_{OUT3}, V_{OUT4} (external transistor)



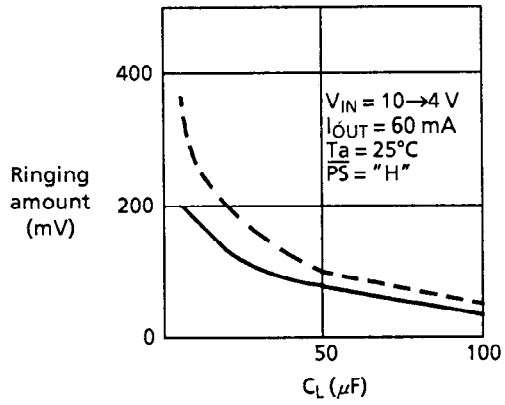
3.5 V_{OUT4} (internal transistor)



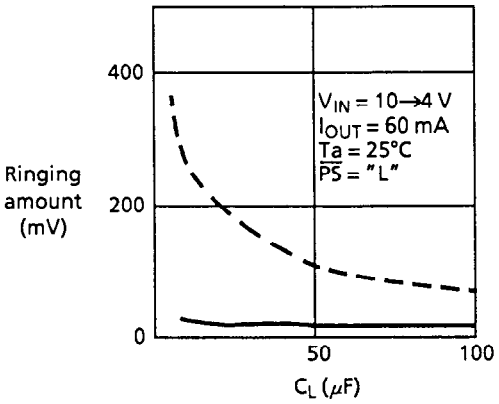


4. C_L dependency (V_{IN} = 10 V→4 V)

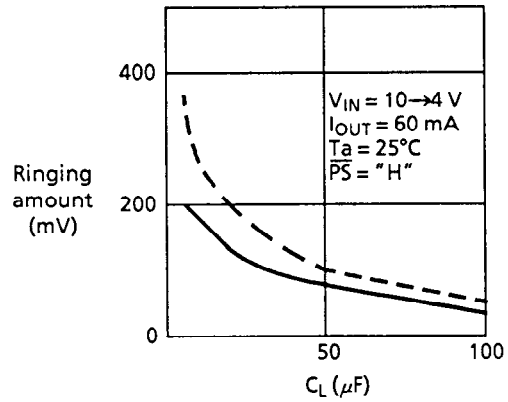
4.1 V_{OUT1}, V_{OUT2}



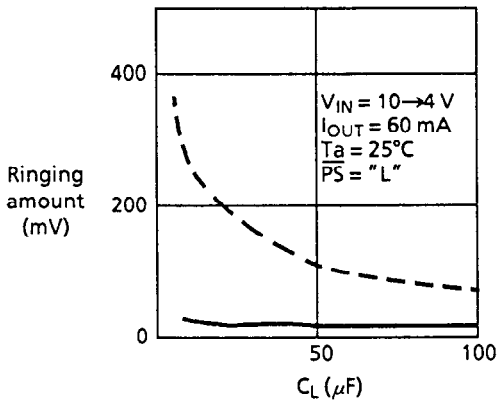
4.2 V_{OUT1}, V_{OUT2}



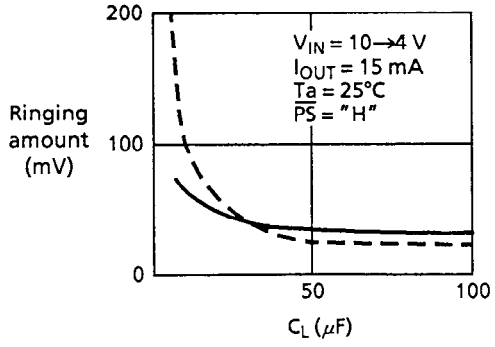
4.3 V_{OUT3}, V_{OUT4} (external transistor)

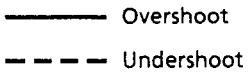


4.4 V_{OUT3}, V_{OUT4} (external transistor)



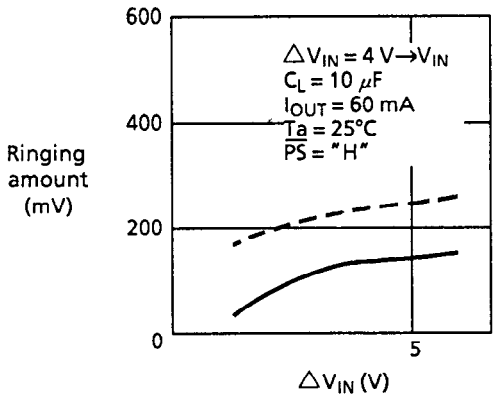
4.5 V_{OUT4} (internal transistor)



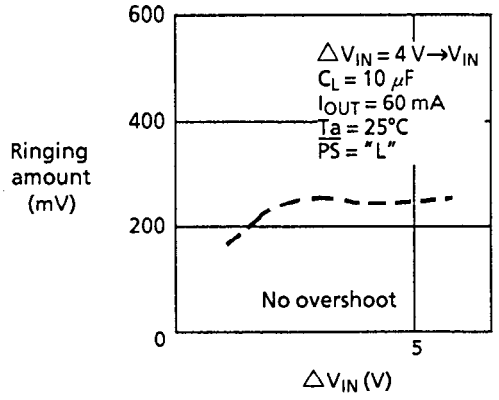


5. $\triangle V_{IN}$ dependency (4 V→V_{IN})

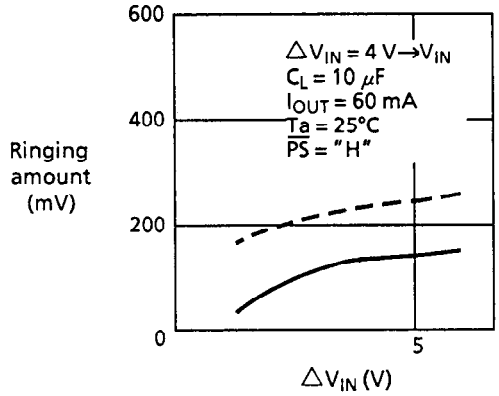
5.1 V_{OUT1}, V_{OUT2}



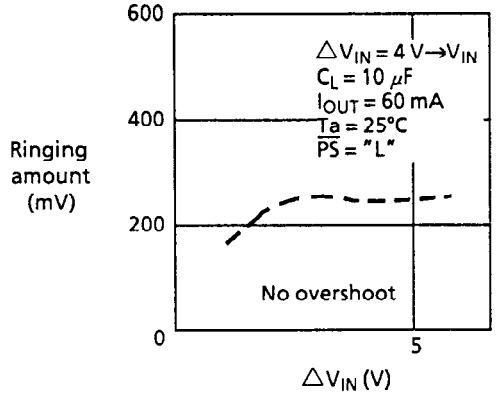
5.2 V_{OUT1}, V_{OUT2}



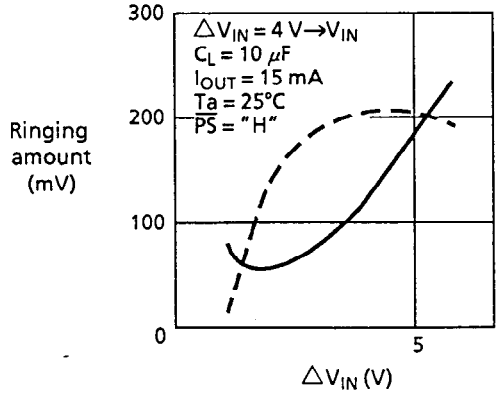
5.3 V_{OUT3}, V_{OUT4} (external transistor)

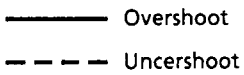


5.4 V_{OUT3}, V_{OUT4} (external transistor)



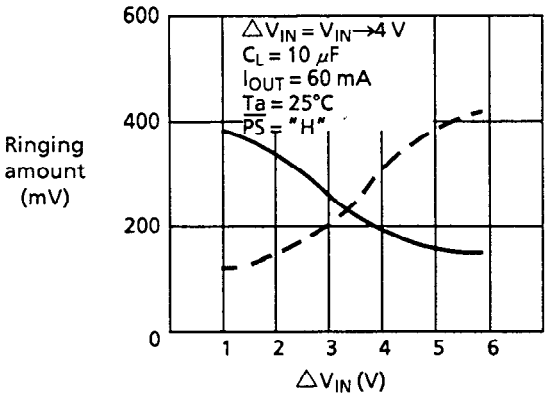
5.5 V_{OUT4} (internal transistor)



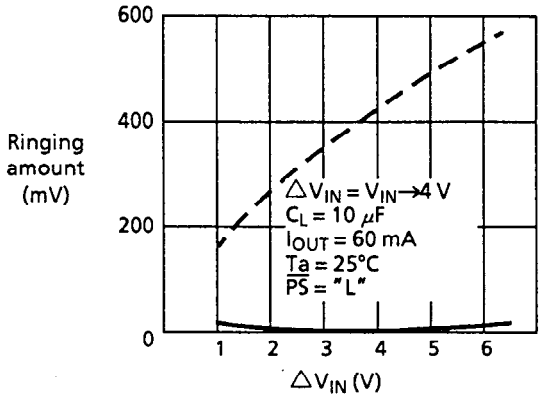


6. $\triangle V_{IN}$ dependency ($V_{IN} \rightarrow 4$ V)

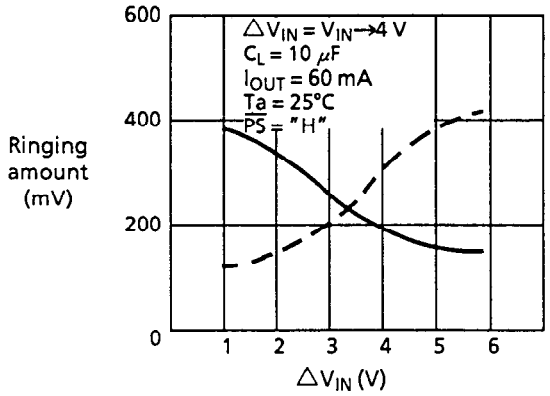
6.1 V_{OUT1}, V_{OUT2}



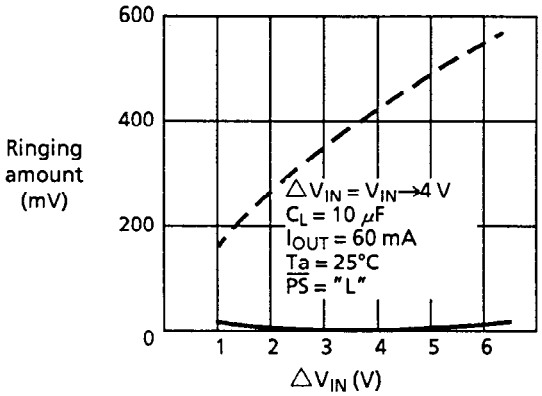
6.2 V_{OUT1}, V_{OUT2}



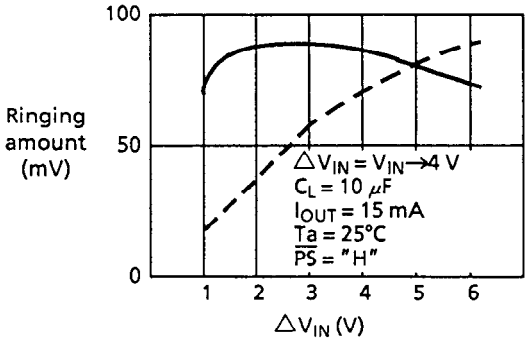
6.3 V_{OUT3}, V_{OUT4} (external transistor)

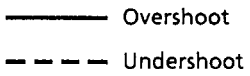


6.4 V_{OUT3}, V_{OUT4} (external transistor)



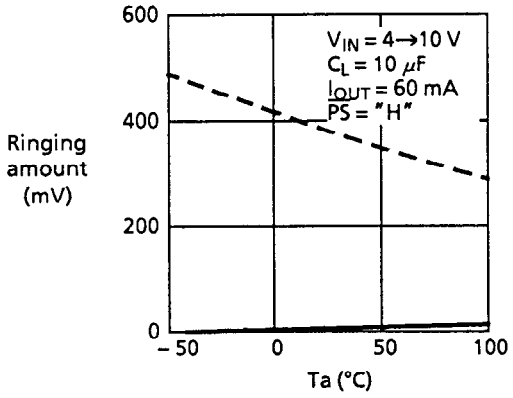
6.5 V_{OUT4} (internal transistor)



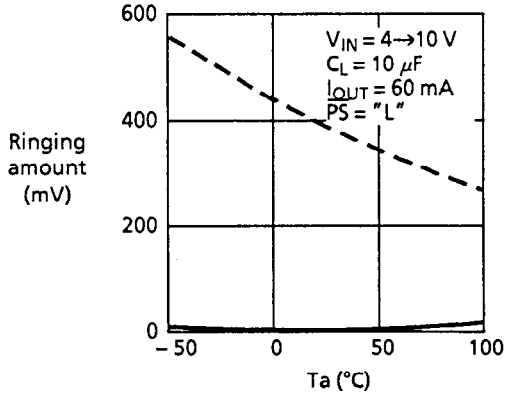


7. Temperature dependency (4 V→10 V)

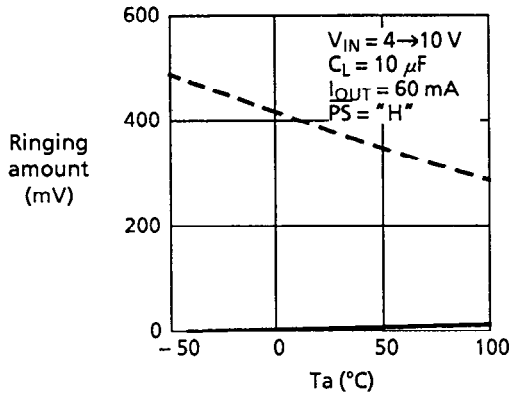
7.1 V_{OUT1}, V_{OUT2}



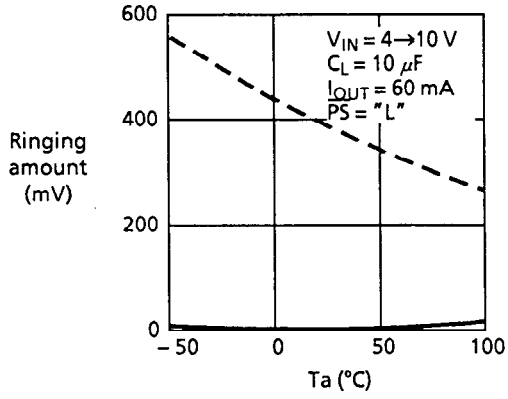
7.2 V_{OUT1}, V_{OUT2}



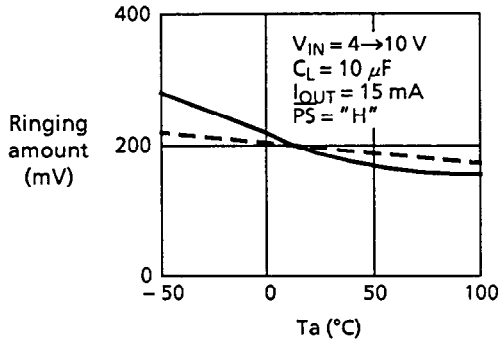
7.3 V_{OUT3}, V_{OUT4} (external transistor)

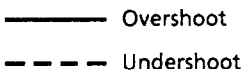


7.4 V_{OUT3}, V_{OUT4} (external transistor)



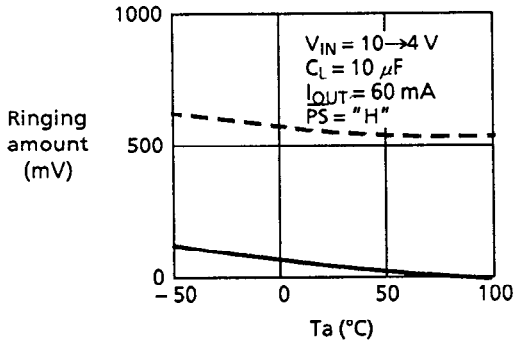
7.5 V_{OUT4} (internal transistor)



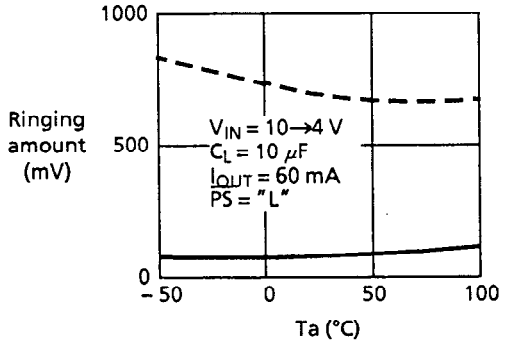


8. Temperature dependency (10 V→4 V)

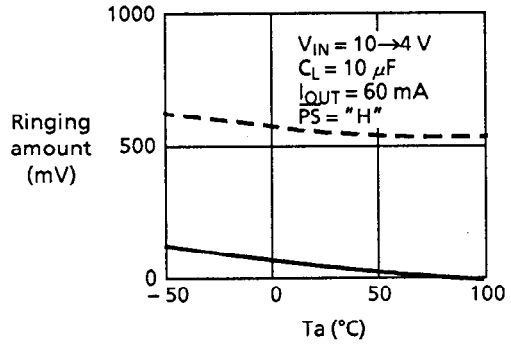
8.1 V_{OUT1}, V_{OUT2}



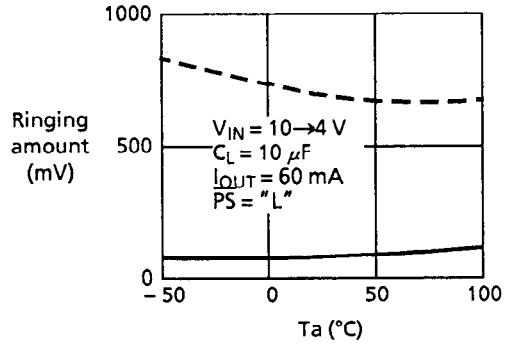
8.2 V_{OUT1}, V_{OUT2}



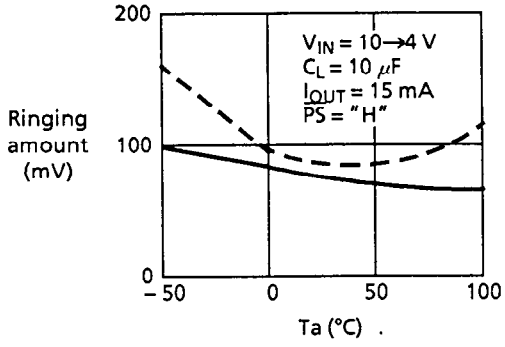
8.3 V_{OUT3}, V_{OUT4} (external transistor)

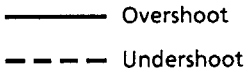


8.4 V_{OUT3}, V_{OUT4} (external transistor)



8.5 V_{OUT4} (internal transistor)





3. Transient Response Characteristics When Output Current Varies

Overshoot or undershoot occurs in the output voltage when the output current varies. This section describes parameter dependency characteristics for both overshoot and undershoot. For reference, Figure 16 depicts the measuring circuit.

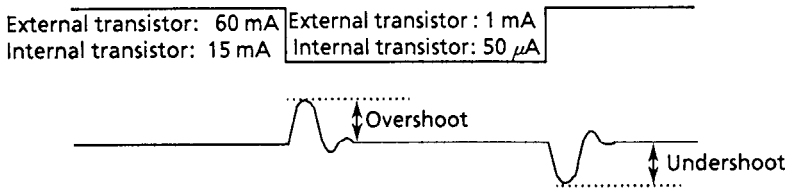


Figure 15

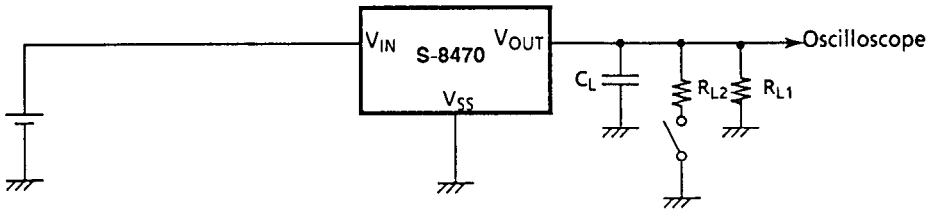


Figure 16 Measuring Circuit

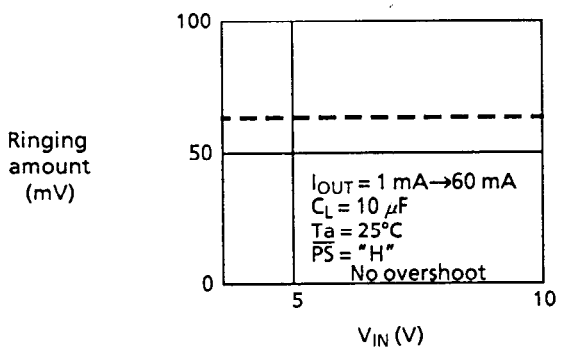
Table 13 Transient Response Parameter Dependency When Output Voltage Varies

Parameter		Conditions	Method to decrease overshoot	Method to decrease undershoot
Input voltage	V_{IN}		—	—
Load capacitance	C_L		Increase	Increase
Output current variation	I_{OUT}	External : 60 mA ↔ 1 mA Internal : 15 mA ↔ 50 μA	Decrease	Decrease
Temperature	Ta	- 40 to 85 °C	—	—

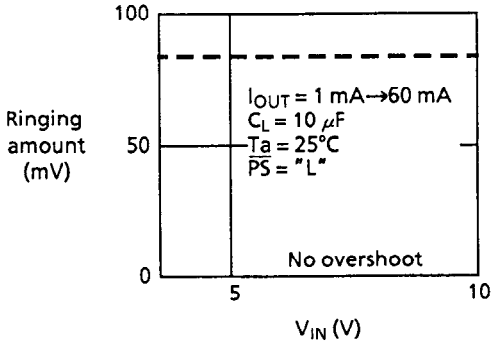
Reference Data When Output Current Varies

1. V_{IN} dependency (external transistor : 1 mA→60 mA, internal transistor : 50 μA→15 mA)

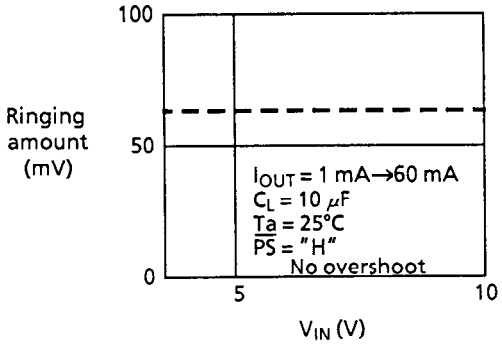
1.1 V_{OUT1}, V_{OUT2}



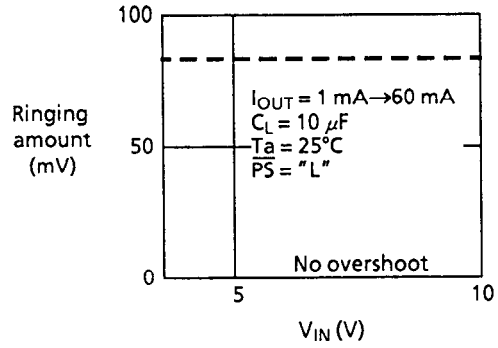
1.2 V_{OUT1}, V_{OUT2}



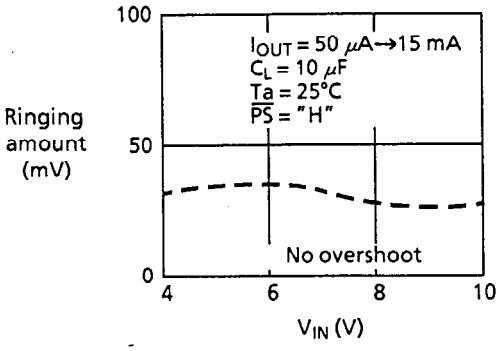
1.3 V_{OUT3}, V_{OUT4} (external transistor)

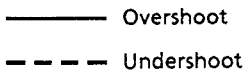


1.4 V_{OUT3}, V_{OUT4} (external transistor)



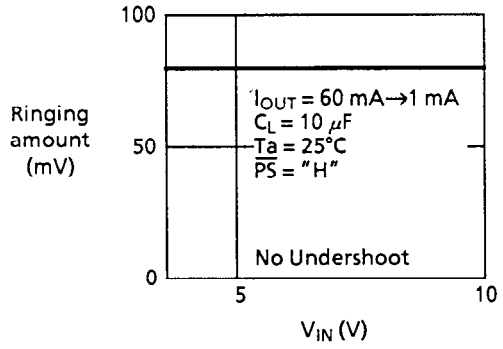
1.5 V_{OUT4} (internal transistor)



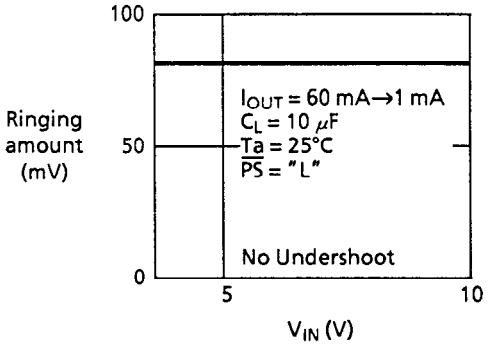


2. V_{IN} dependency (external transister : 60 mA→1 mA, internal transister : 15 mA→50 μA)

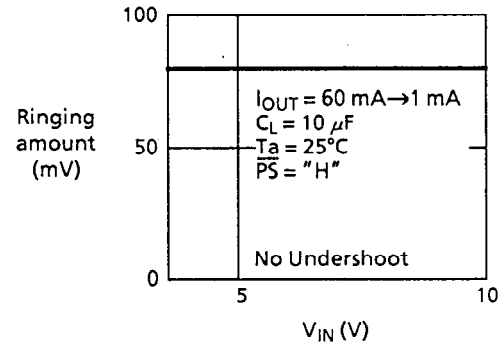
2.1 V_{OUT1}, V_{OUT2}



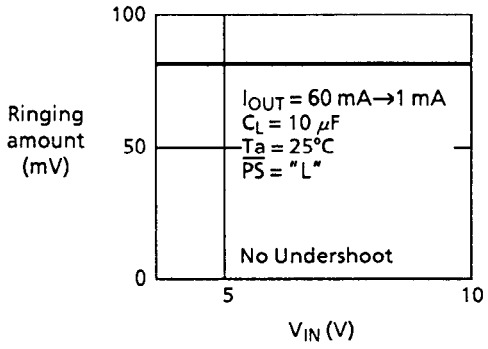
2.2 V_{OUT1}, V_{OUT2}



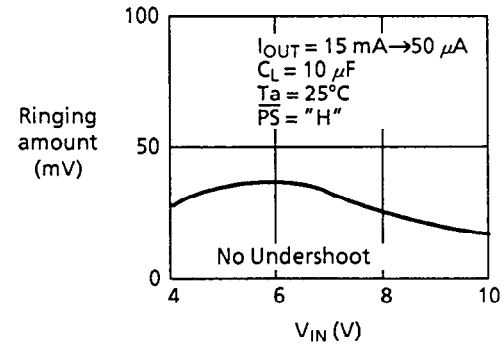
2.3 V_{OUT3}, V_{OUT4} (external transister)

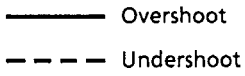


2.4 V_{OUT3}, V_{OUT4} (external transister)



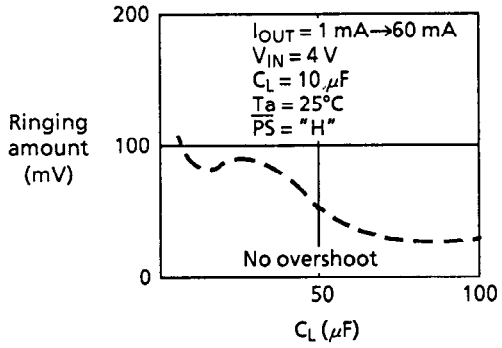
2.5 V_{OUT4} (internal transister)



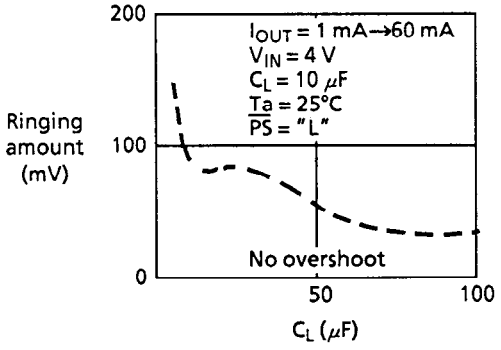


3. C_L dependency (external transister : 1 mA→60 mA / internal transister : 50 μA→15 mA)

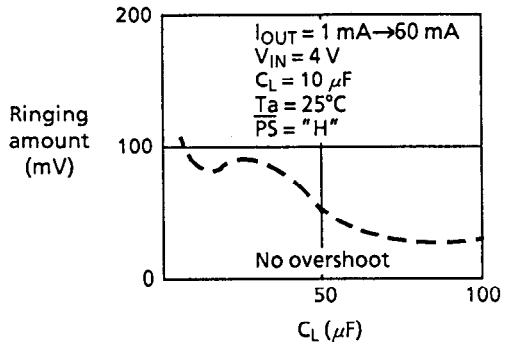
3.1 V_{OUT1}, V_{OUT2}



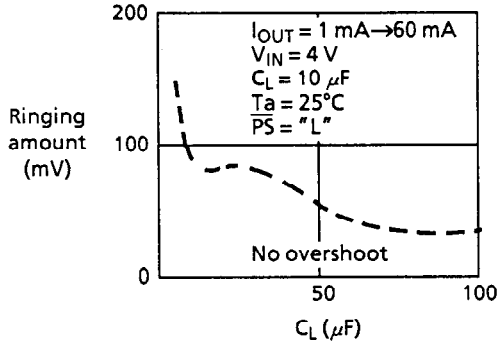
3.2 V_{OUT1}, V_{OUT2}



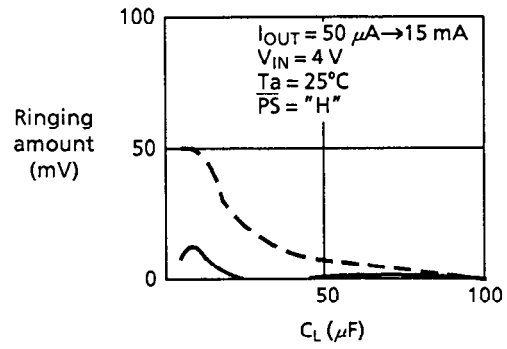
3.3 V_{OUT3}, V_{OUT4} (external transister)

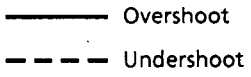


3.4 V_{OUT3}, V_{OUT4} (external transister)



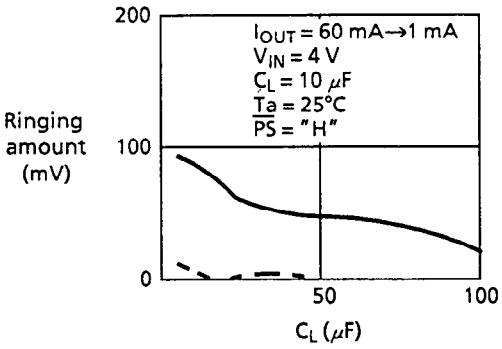
3.5 V_{OUT4} (internal transister)



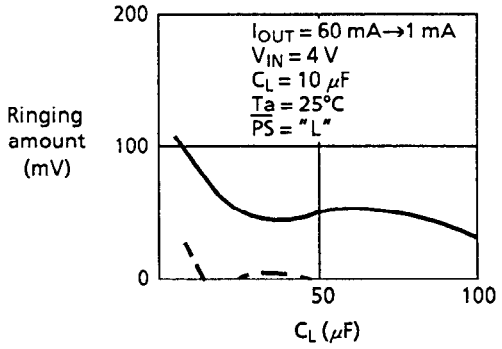


4. C_L dependency (external transister : 60 mA→1 mA, internal transister : 15 mA→50 μA)

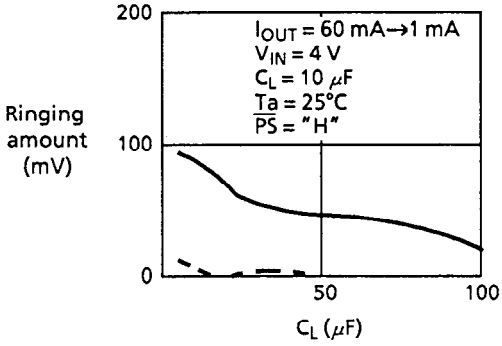
4.1 V_{OUT1}, V_{OUT2}



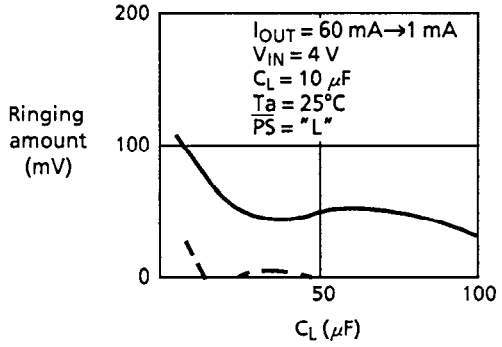
4.2 V_{OUT1}, V_{OUT2}



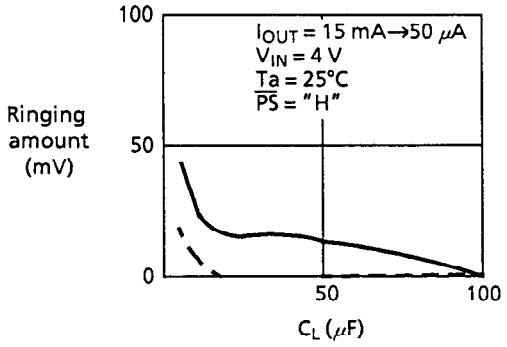
4.3 V_{OUT3}, V_{OUT4} (external transister)

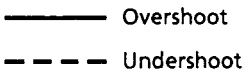


4.4 V_{OUT3}, V_{OUT4} (external transister)



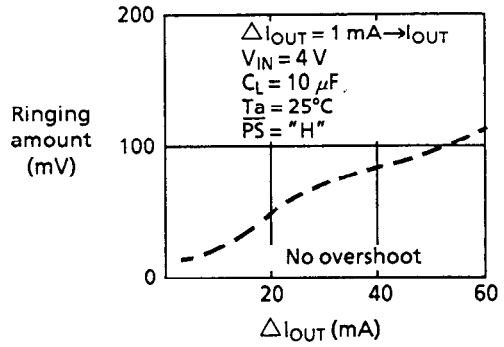
4.5 V_{OUT4} (internal transister)



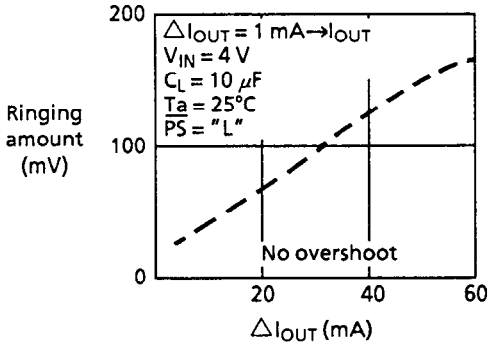


5. $\triangle I_{OUT}$ dependency (external transister : 1 mA→I_{OUT} / internal transister : 50 μA→I_{OUT})

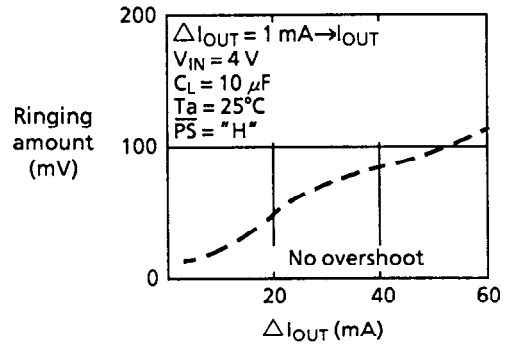
5.1 V_{OUT1}, V_{OUT2}



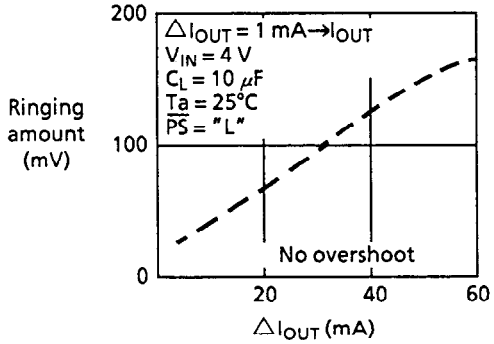
5.2 V_{OUT1}, V_{OUT2}



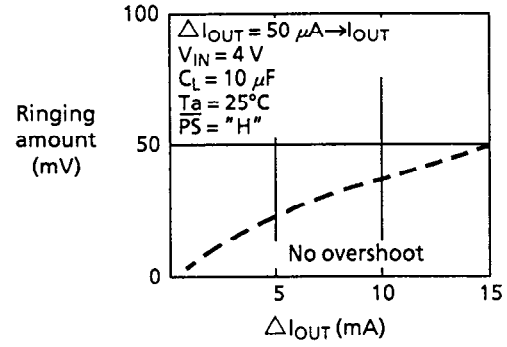
5.3 V_{OUT3}, V_{OUT4} (external transister)

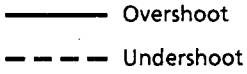


5.4 V_{OUT3}, V_{OUT4} (external transister)



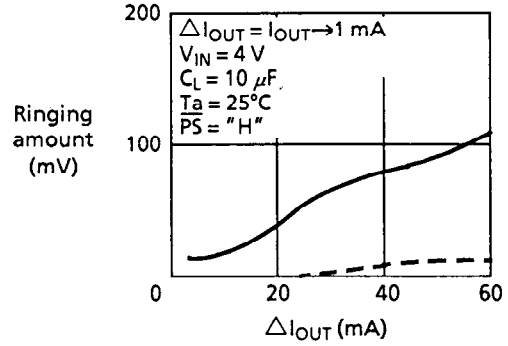
5.5 V_{OUT4} (internal transister)



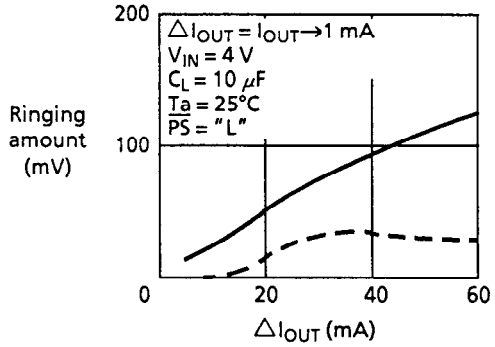


6. $\triangle I_{OUT}$ dependency (external transister : I_{OUT}→1 mA, internal transister : I_{OUT}→50 μA)

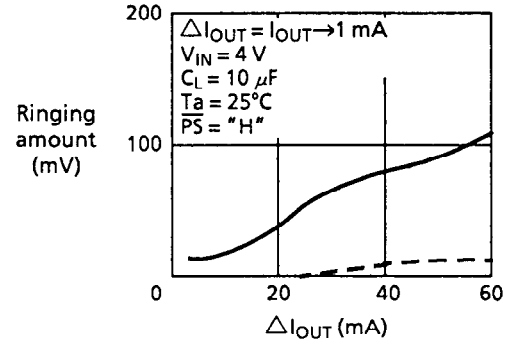
6.1 V_{OUT1}, V_{OUT2}



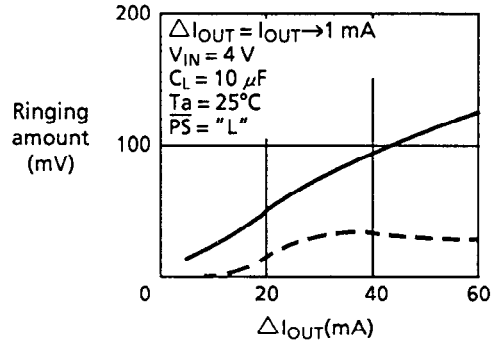
6.2 V_{OUT1}, V_{OUT2}



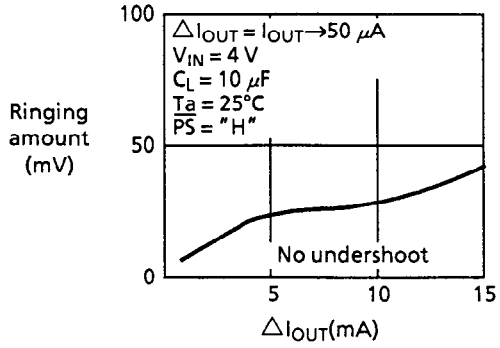
6.3 V_{OUT3}, V_{OUT4} (external transister)

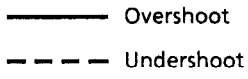


6.4 V_{OUT3}, V_{OUT4} (external transister)



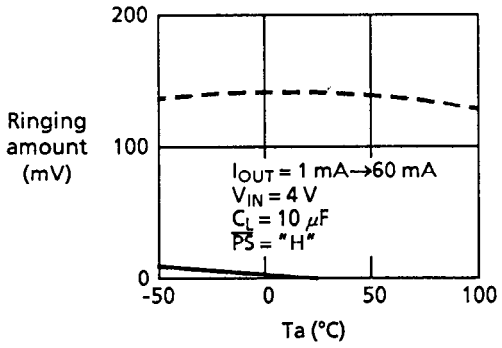
6.5 V_{OUT4} (internal transister)



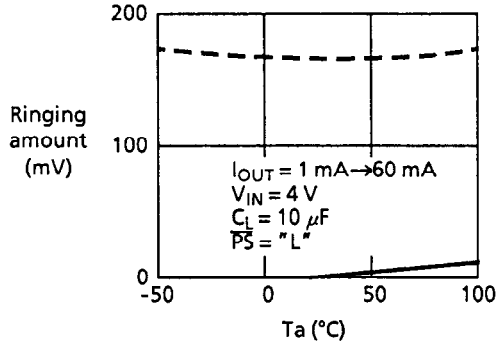


7. Temperature dependency (external transister : 1 mA→60 mA / internal transister : 50 μA→15 mA)

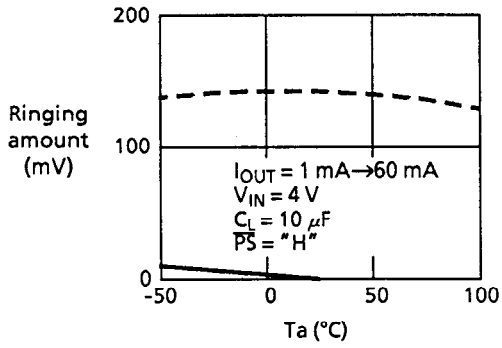
7.1 V_{OUT1}, V_{OUT2}



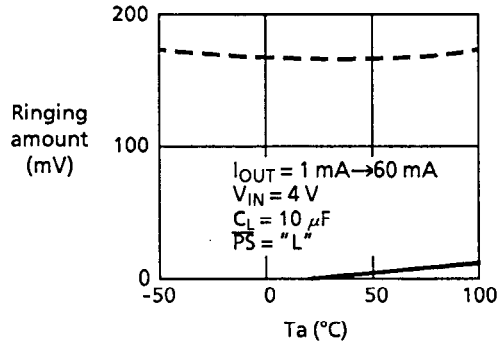
7.2 V_{OUT1}, V_{OUT2}



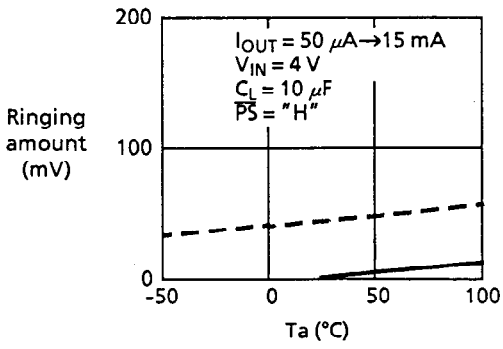
7.3 V_{OUT3}, V_{OUT4} (external transister)

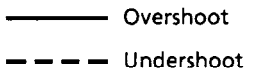


7.4 V_{OUT3}, V_{OUT4} (external transister)



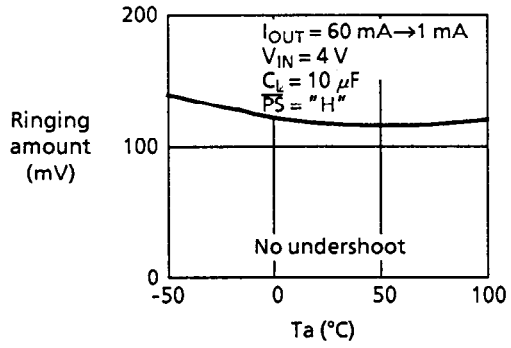
7.5 V_{OUT4} (internal transister)



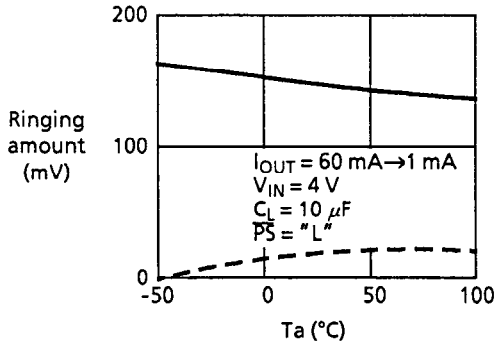


8. Temperature dependency (external transister : 60 mA→1 mA / internal transister : 15 mA→50 μA)

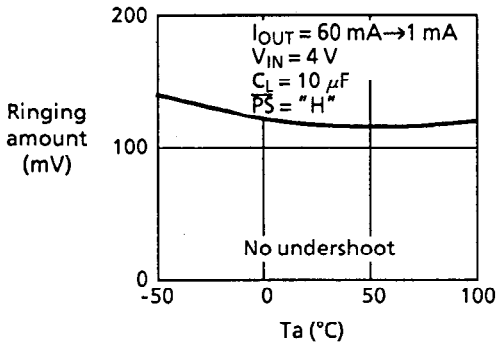
8.1 V_{OUT1}, V_{OUT2}



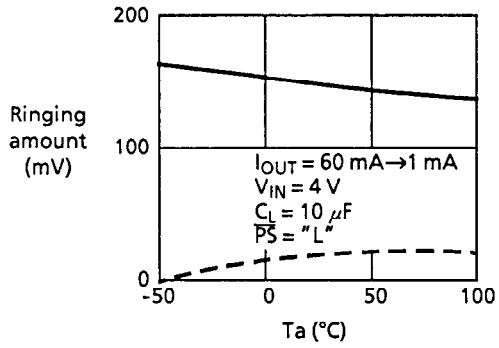
8.2 V_{OUT1}, V_{OUT2}



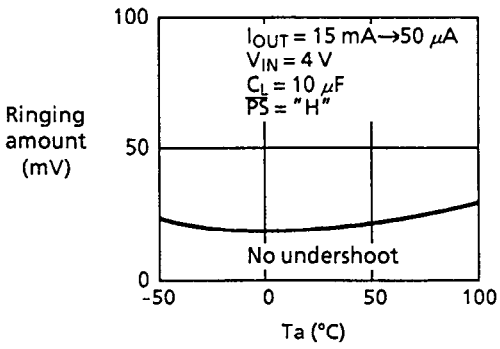
8.3 V_{OUT3}, V_{OUT4} (external transister)

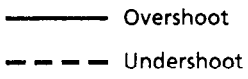


8.4 V_{OUT3}, V_{OUT4} (external transister)



8.5 V_{OUT4} (internal transister)



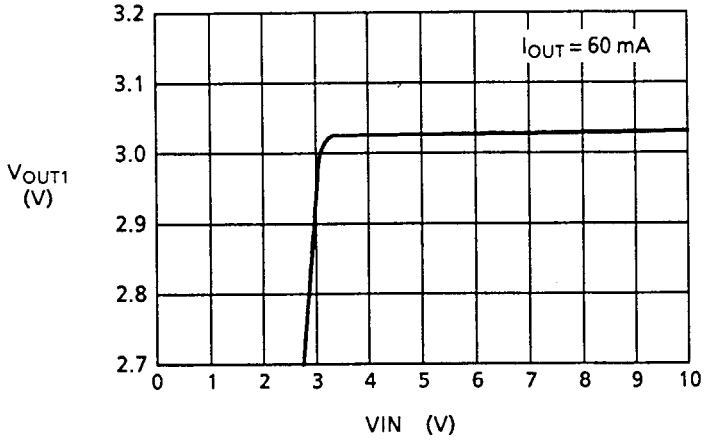


■ Characteristics

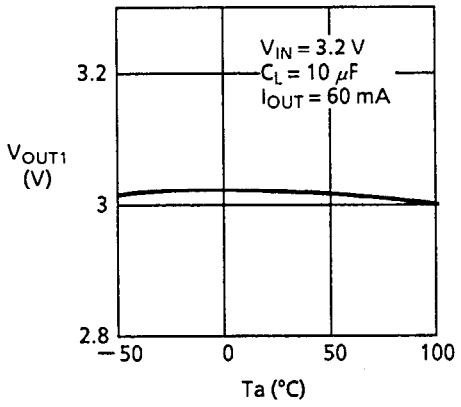
1. Voltage regulator

1-1 Output voltage characteristics

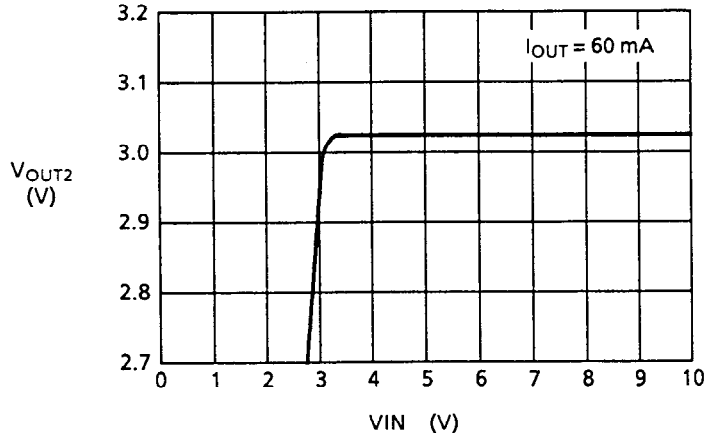
1-1-1 V_{OUT1}-V_{IN}



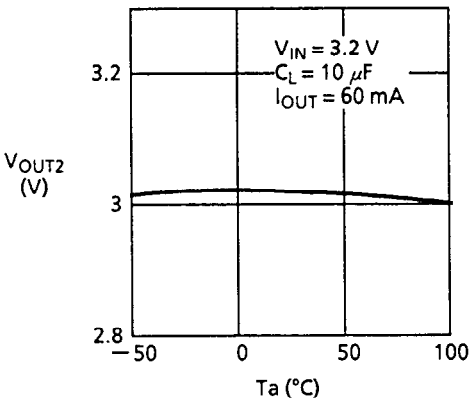
1-1-2 V_{OUT1}-Temperature



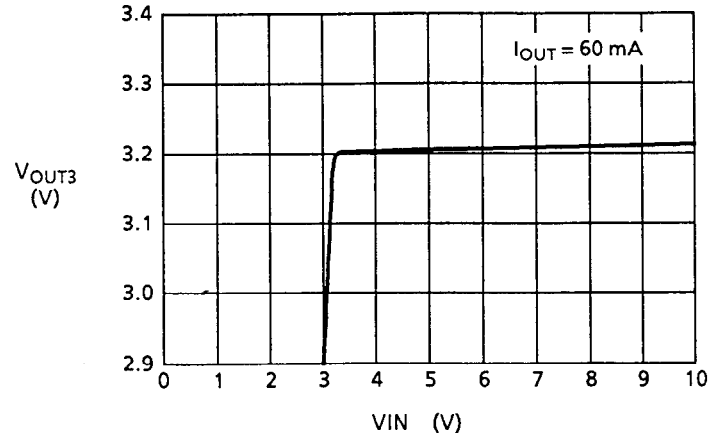
1-1-3 V_{OUT2}-V_{IN}



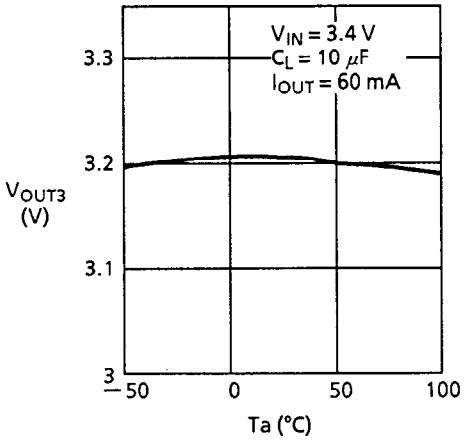
1-1-4 V_{OUT2}-Temperature



1-1-5 V_{OUT3}-V_{IN}



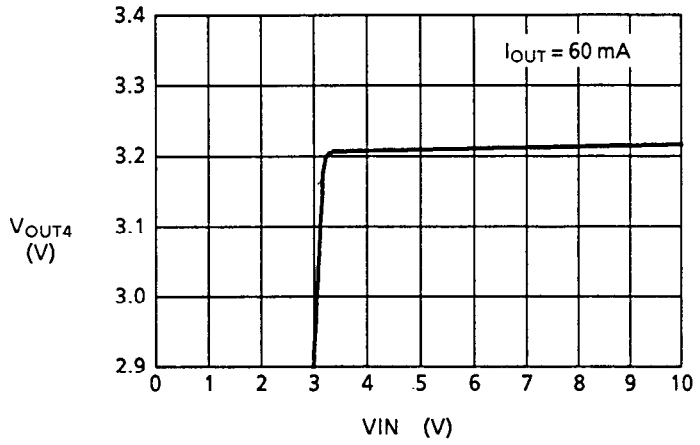
1-1-6 V_{OUT3}-Temperature



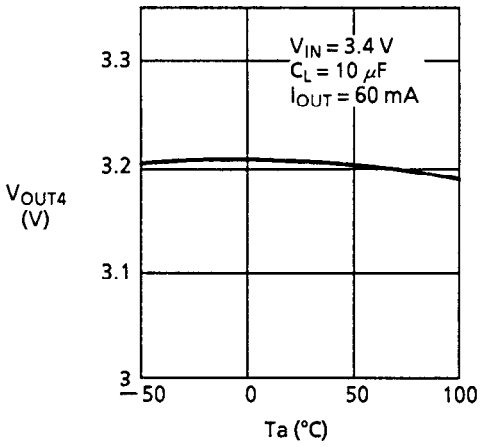
Overshoot

Undershoot

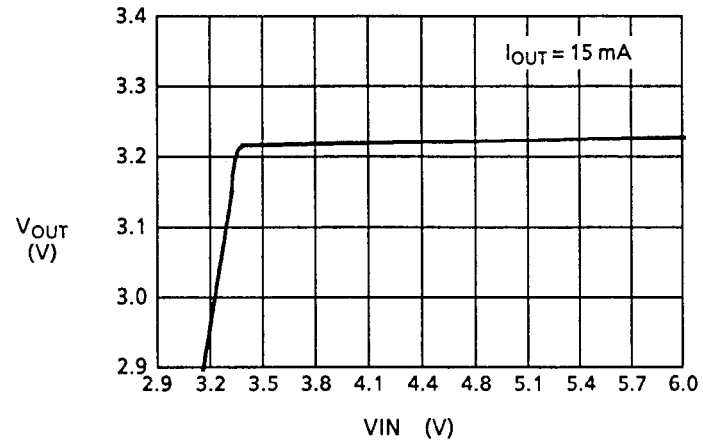
1-1-7 V_{OUT4}-V_{IN} (external transister)



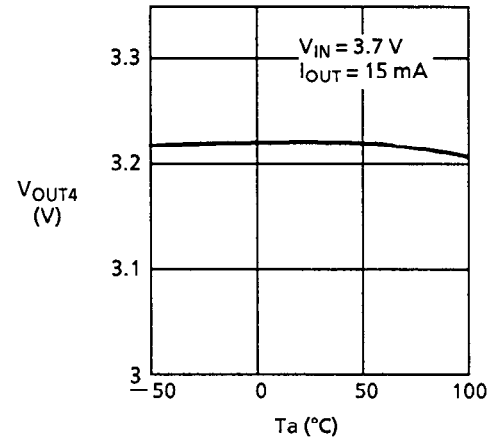
1-1-8 V_{OUT4}-Temperature (external transister)



1-1-9 V_{OUT4}-V_{IN} (external transister)

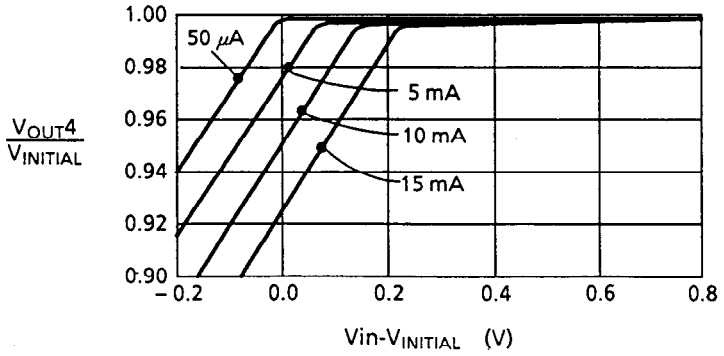


1-1-10 V_{OUT4}-Temperature (external transister)

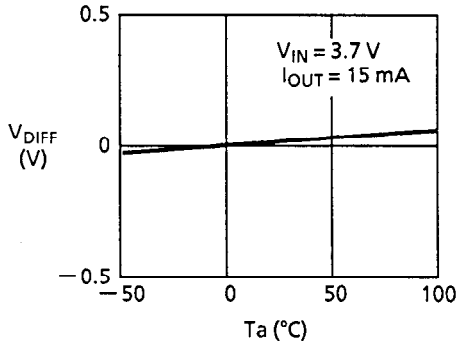


1-2 Input/Output voltage difference characteristics (V_{OUT4} internal transistor)

1-2-1 V_{IN} dependency



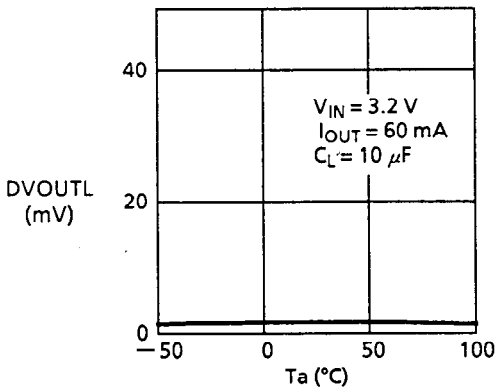
1-2-2 V_{DIFF}-Temperature



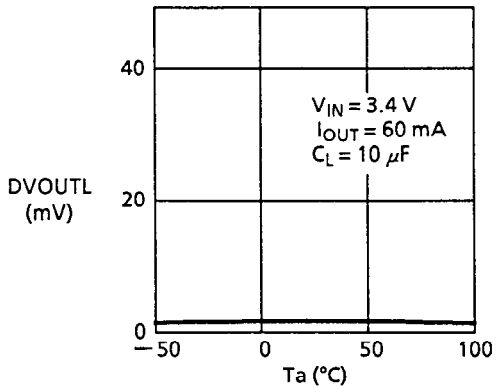
$V_{INITIAL}$: V_{OUT} value when input voltage is 3.7 V

1-3 Input stability ($\triangle V_{OUT1}$, $V_{OUT2}V_{OUTL}$) - Temperature

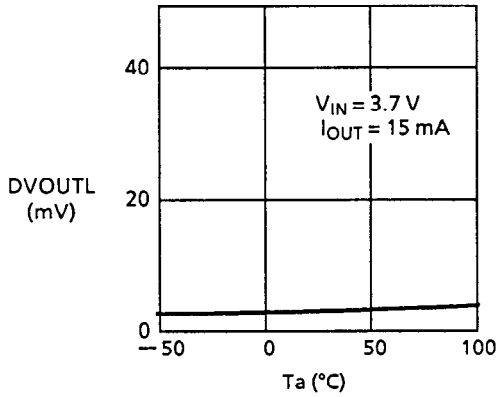
1-3-1 V_{OUT1}, V_{OUT2}



1-3-2 V_{OUT3}, V_{OUT4} (external transister)

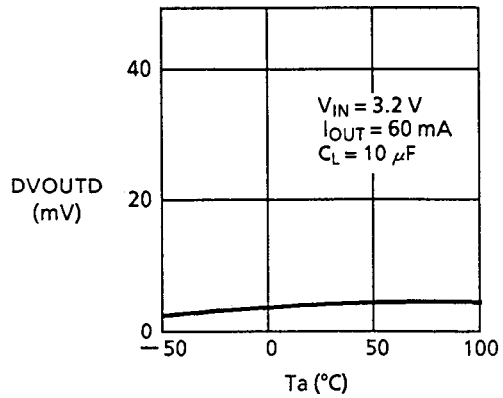


1-3-3 V_{OUT4} (internal transister)

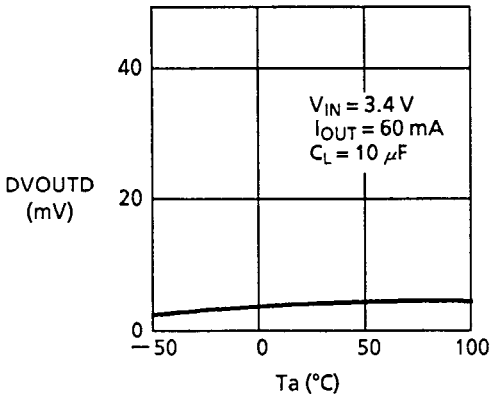


1-4 Load stability ($\triangle V_{OUTD}$) - Temperature

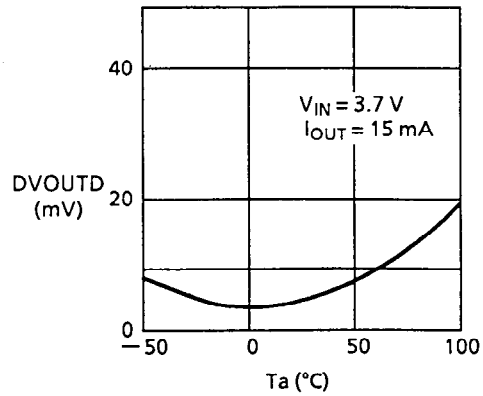
1-4-1 V_{OUT1}, V_{OUT2}



1-4-2 V_{OUT3}, V_{OUT4} (external transister)

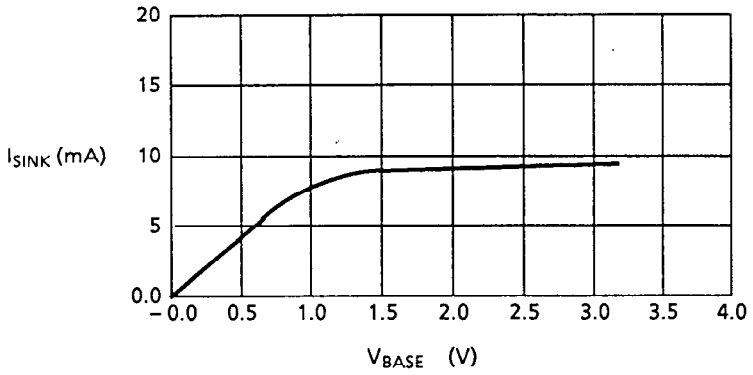


1-4-3 V_{OUT4} (internal transister)

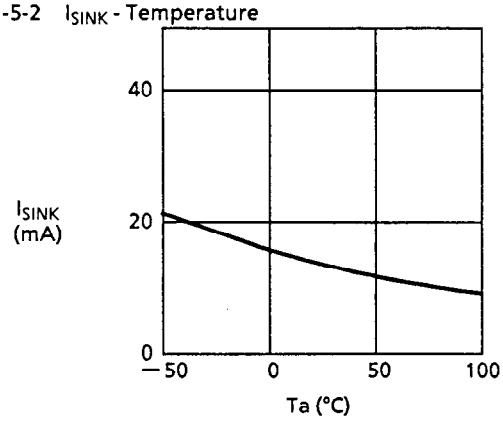


1-5 Base sink current (I_{SINK}) characteristics

1-5-1 I_{SINK} - V_{BASE}



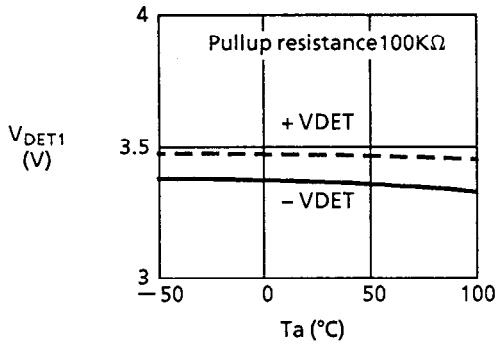
1-5-2 I_{SINK} - Temperature



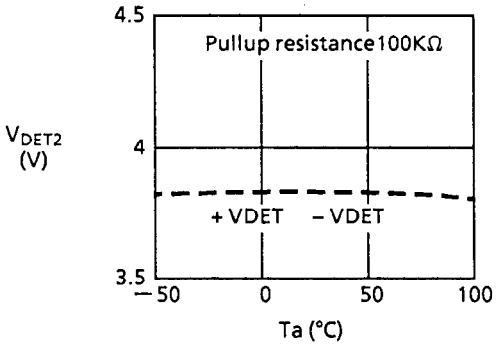
2 Voltage detector

2-1 Detection Release voltage - Temperature

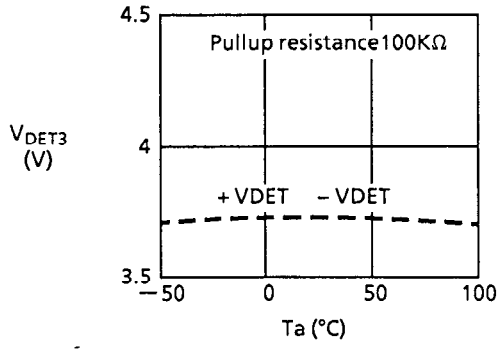
2-1-1 V_{DOUT1}



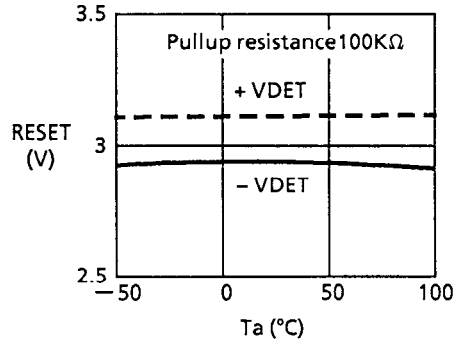
2-1-2 V_{DOUT2}



2-1-3 V_{OUT3}

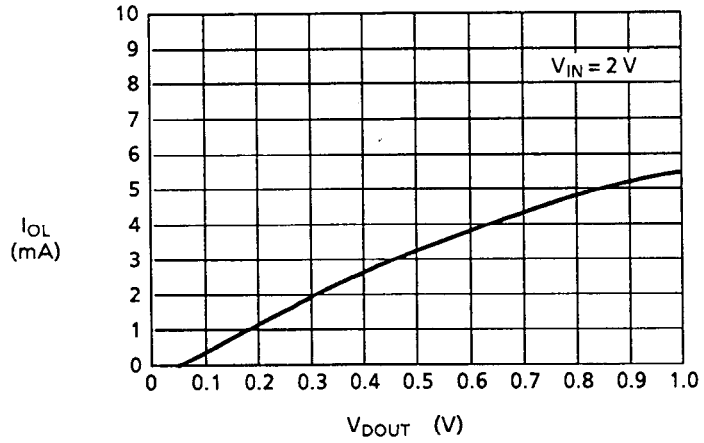


2-1-4 $\overline{RESET}$

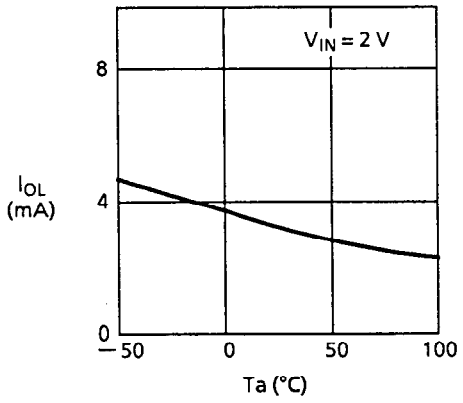


2-2 Sink current (I_{OL}) characteristics

2-2-1 I_{OL} - V_{DOUT}

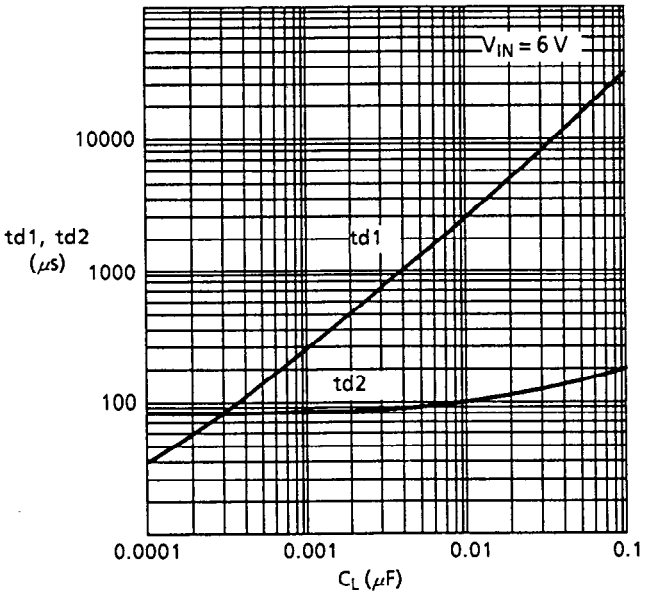


2-2-2 I_{OL} - Temperature

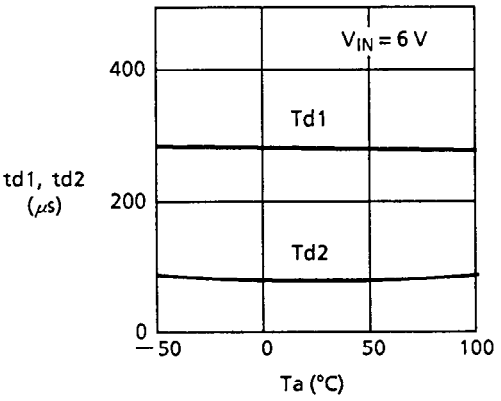


2-3 Dynamic responce

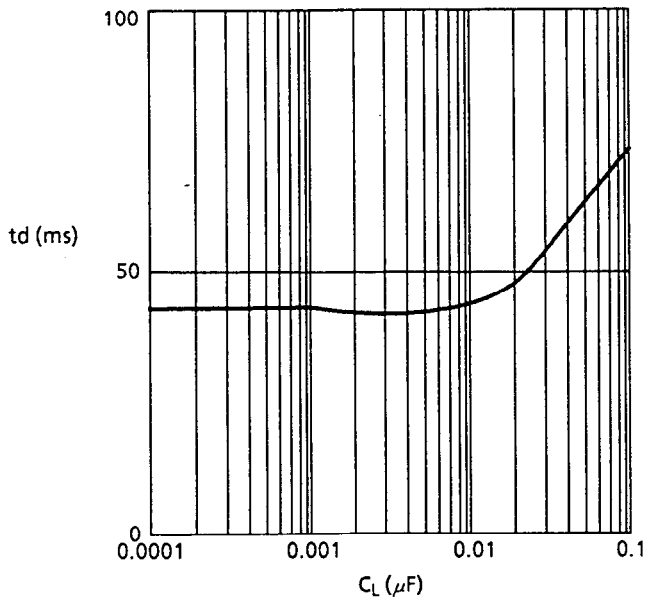
2-3-1 td1, td2 - C_L



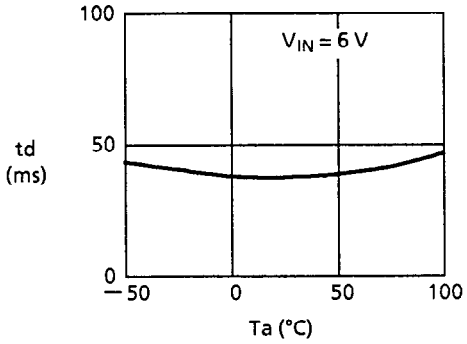
2-3-2 td1, td2 - Temperature



2-3-3 $\overline{\text{RESET}}$ with delay - C_L



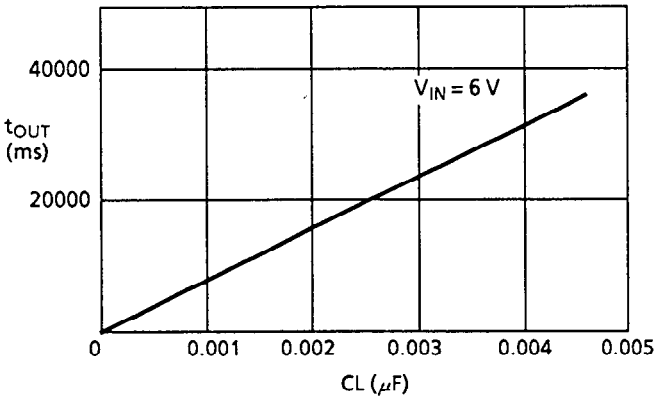
2-3-4 $\overline{\text{RESET}}$ with delay - Temperature



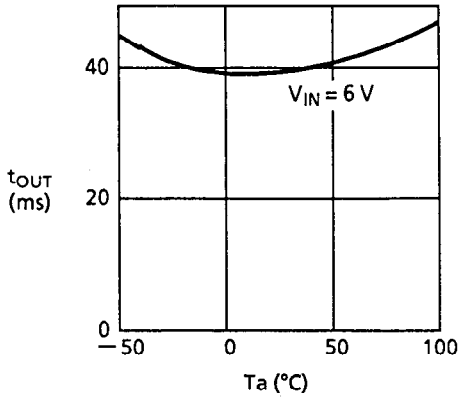
3 Watchdag Timer

3-1 Time out (t_{OUT}) characteristics

3-1-1 t_{OUT} - C_L

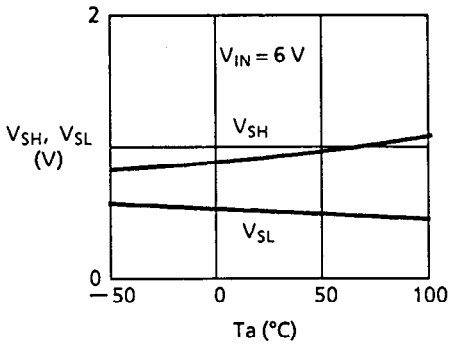


3-1-2 t_{OUT} - Temperature



4 Overall characteristics

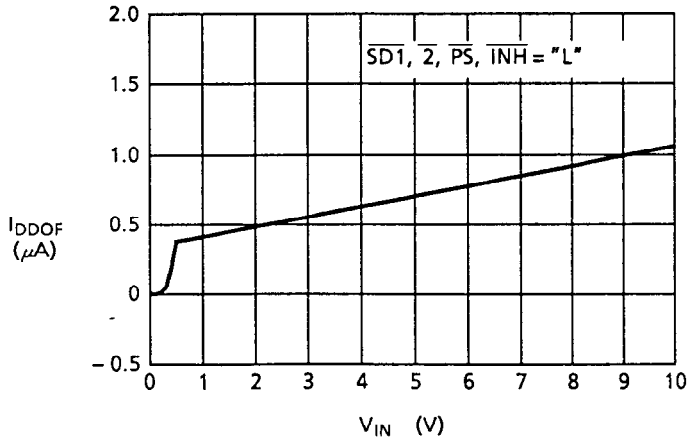
4-1 V_{SH}, V_{SL} - Temperature



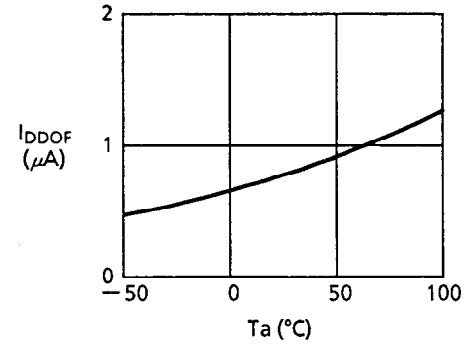
$\overline{SD1}$, $\overline{SD2}$
$\overline{RS}$, $\overline{RESIN}$, $\overline{INH}$
$\overline{WDTCLR}$

4-2 Current consumption (I_{DDOF}) characteristics

4-2-1 I_{DDOF} - V_{IN} *



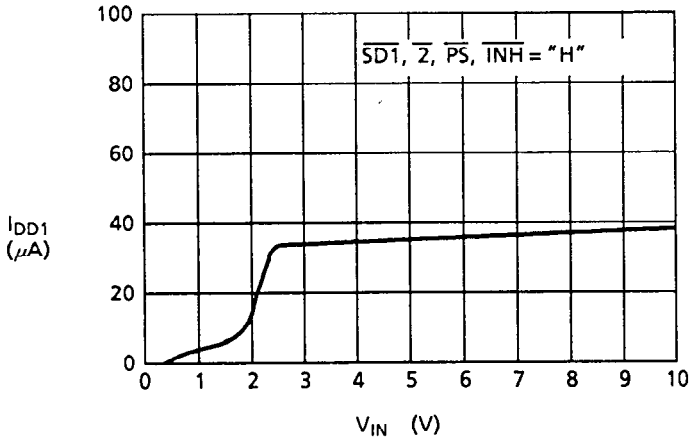
4-2-2 I_{DDOF} - Temperature



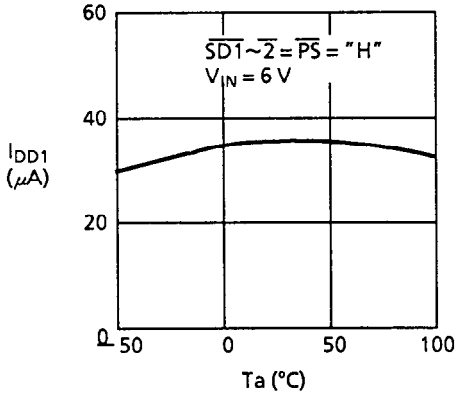
* Without a shutdown prohibition.When the shut-down is not prohibited

4-3 Current consumption (I_{DD1}) characteristics

4-3-1 I_{DD1} - V_{IN}

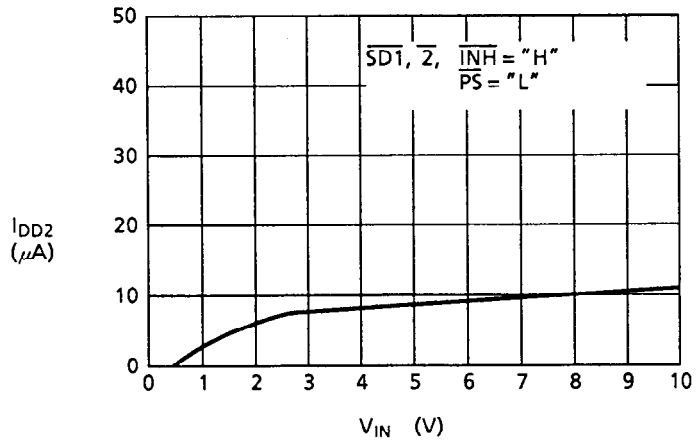


4-3-2 I_{DD1} - Temperature

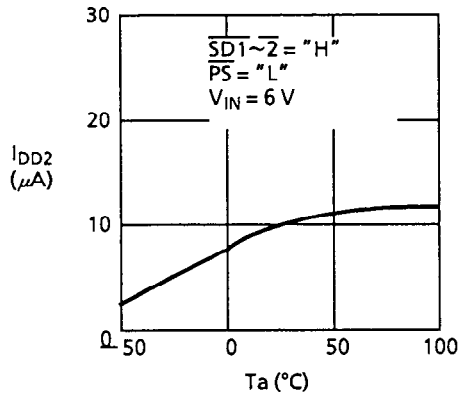


4-4 Current consumption (I_{DD2}) characteristics

4-4-1 I_{DD2} - V_{IN}



4-4-2 I_{DD2} - Temperature



■ Application Circuit (S-8470CFS, REG4 external Tr)

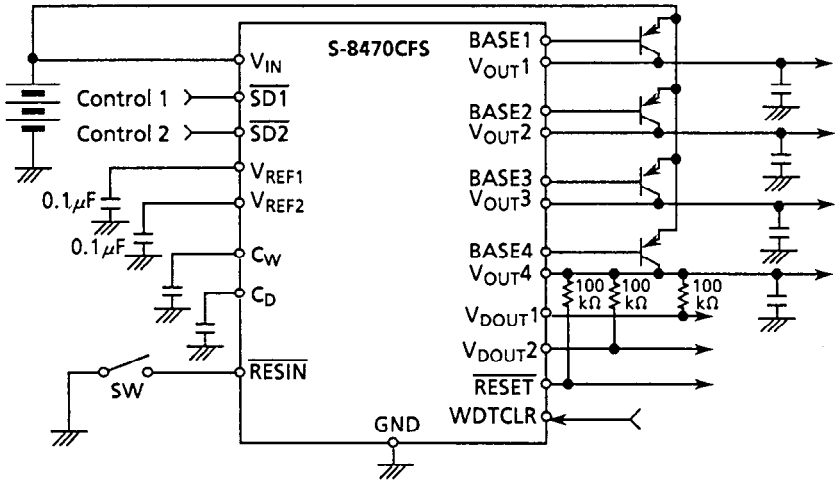


Figure 17

■ Notes

- When using the internal transistor at $V_{OUT}4$, always turn the $\overline{PS}$ "H." If you leave the $\overline{PS}$ "L," the transient response characteristics may deteriorate.
- The S-8470 series is not provided with a short-circuit protection circuit. In the event that short-circuit occurs during the IC mounting operation, the resulting overcurrent may damage components on the IC.
- DO NOT APPLY the ripple voltage to the V_{IN} under the following conditions:

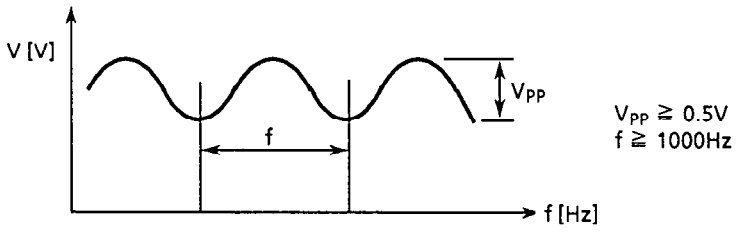
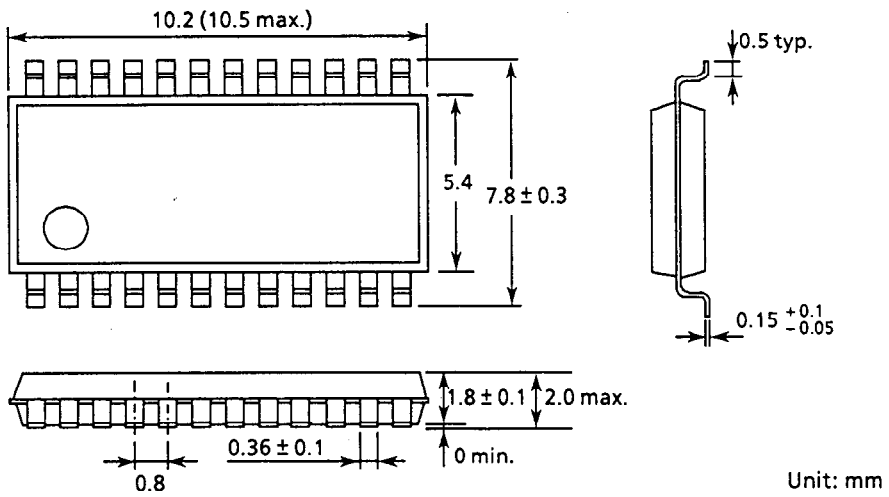


Figure 18

- Always attach a 10 μF or more capacitor to the V_{OUT} (V_{OUT} 1 through 4).
- Attach an about 0.1 μF capacitor to V_{REF1} and V_{REF2}.
- When the V_{IN} voltage fluctuates over 1.5 V, set the through-rate for the V_{IN} fluctuation to under 3 V/ms.
- When the S-8470 series detects the output voltage of the voltage regulator, overshoot or undershoot occurs in the voltage regulator depending upon operating conditions. Referring to the "Transient Response Characteristics," use the S-8470 series at the proper detection voltage and load capacitance.
- A rise in the output voltage may occur in such an application that the output current of the external Tr. voltage regulator is less than 1 mA (when using the voltage regulator with an internal power Tr., it is 50 μA).
- When the external Tr. is connected to the voltage regulator, the base current increases if $V_{IN}<V_{OUT}1$ through 4.
- When you design a new product for actual massproduction using the application circuits described herein, consider the tolerance, temperature and other characteristics of the parts you employ. Seiko Instruments Inc. shall not bear the responsibility for any patent infringement with regard to and/or arising from the circuits described herein.

■ Dimensions

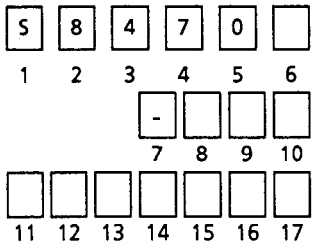
24-pin SSOP



Unit: mm

Figure 19

■ Marking



1 through 5:	Model name
6:	A = S8470AFS, B = S-8470BFS, C = S-8470CFS
8 through 10:	Mask option number
11:	Assembly code
12:	Year of assembly (last digit)
13:	Month of assembly
	Jan. = 1, Feb. = 2, Mar. = 3
	Apr. = 4, May = 5, Jun. = 6
	Jul. = 7, Aug. = 8, Sept. = 9
	Oct. = X, Nov. = Y, Dec. = Z
14 through 17:	Lot number

Figure 20

■ Taping

1. Tape specifications

Types T1 and T2 are available depending upon the direction of the IC on the tape.

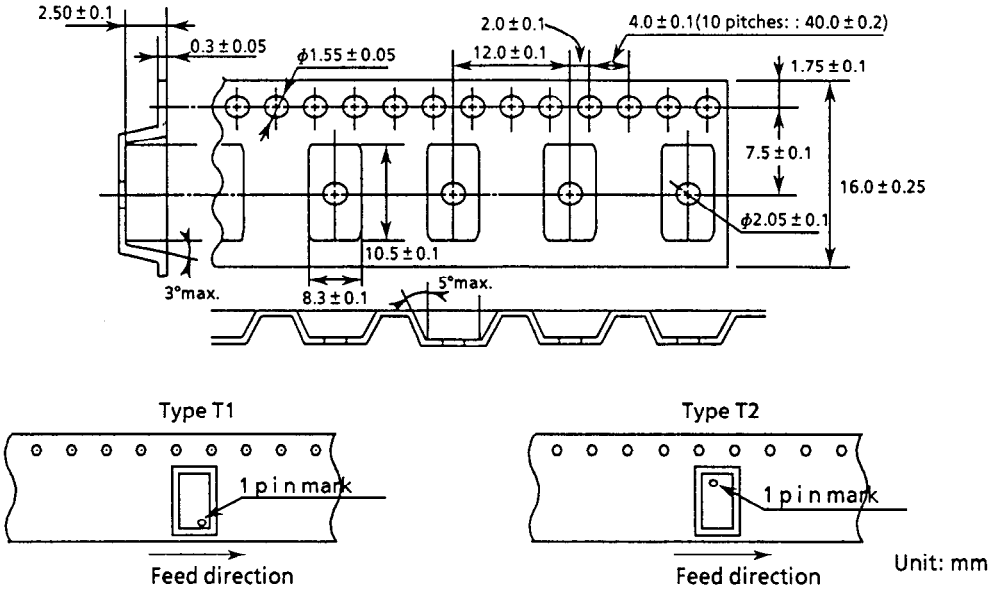


Figure 21

2. Reel specifications

1 reel holds 2000 ICs.

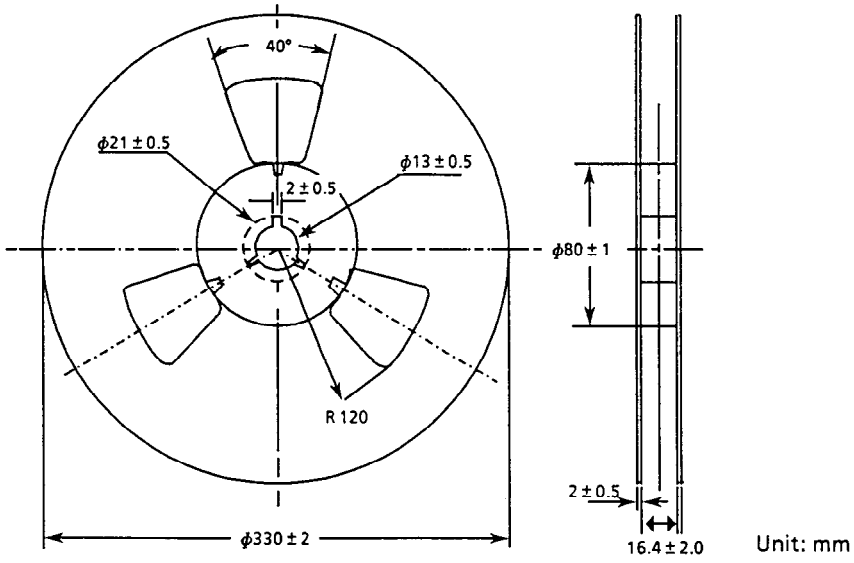


Figure 22