MINI ANALOG SERIES
LOW INPUT OFFSET VOLTAGE CMOS OPERATIONAL AMPLIFIER
S-89713B Series

The mini-analog series is a group of ICs that incorporate a general purpose analog circuit in a small package.
The S-89713B Series is an auto-zero operation, zero-drift operational amplifier that has I/O of low input offset voltage and Rail-to-Rail[*1]. This IC is suitable for applications requiring less offset voltage.
The S-89713B Series is dual operational amplifier (with 2 circuits).

***1**. Rail-to-Rail is a trademark of Motorola, Inc.

■ Features

- Low input offset voltage : 10 μV Max.
- Low voltage operation : V_{DD} = 2.65 V to 5.5 V
- Low current consumption : I_{DD} = 165 μA Typ. (for 1 circuit)
  : I_{DD} = 330 μA Typ. (for 2 circuits)
- No external capacitors required for internal phase compensation
- Rail-to-Rail I/O
- Small packages: : SNT-8A, TMSOP-8
- Lead-free product

■ Application

- Various sensor interface
- High-accuracy current detection
- Strain gauge amplifiers
- Game
- Various electric devices

■ Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SNT-8A	PH008-A	PH008-A	PH008-A	PH008-A
TMSOP-8	FM008-A	FM008-A	FM008-A	–

■ Block Diagram

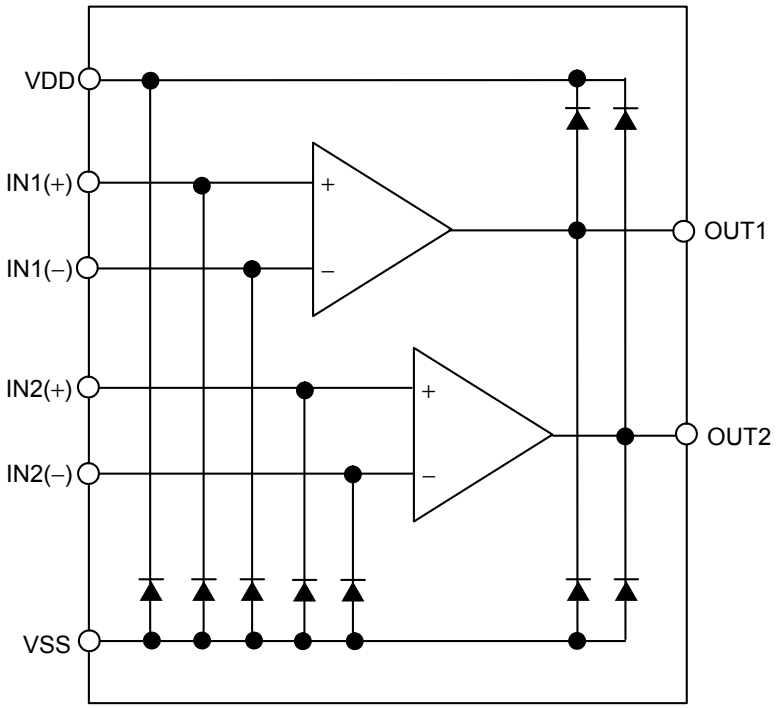


Figure 1

■ Product Name Structure

Users can select the product type for the S-89713B Series. Regarding the contents of the product name, refer to "**1. Product name**". Regarding the product type, refer to "**2. Product name list**".

1. Product name

(1) SNT-8A

S-89713B – I8T1 G

Product name (abbreviation) and IC packing specifications*1
I8T1 : SNT-8A, Tape

***1.** Refer to the tape specifications.

(2) TMSOP-8

S-89713B – K8T2 U

Product name (abbreviation) and IC packing specifications*1
K8T2 : TMSOP-8, Tape

***1.** Refer to the tape specifications.

2. Product list

Table 1

Product name	Package
S-89713B-I8T1G	SNT-8A
S-89713B-K8T2U	TMSOP-8

■ Pin Configurations

SNT-8A
Top view

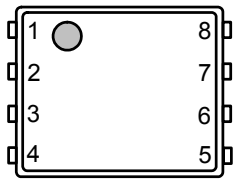


Figure 2

Table 2

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(–)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(–)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

TMSOP-8
Top view

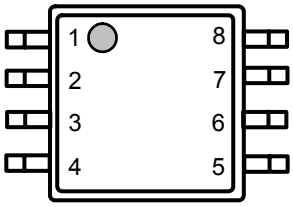


Figure 3

Table 3

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(–)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(–)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Parameter		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD}	V_{SS}–0.3 to V_{SS}+6.0	V
Input voltage		$V_{IN(+)}$,$V_{IN(-)}$	V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage		V_{OUT}	V_{SS}–0.3 to V_{DD}+0.3	V
Differential input voltage		V_{IND}	±5.5	V
Output pin current		I_{SOURCE}	10.0	mA
		I_{SINK}	10.0	mA
Power dissipation	SNT-8A	P_D	450*1	mW
	TMSOP-8		650*1	mW
Operating ambient temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

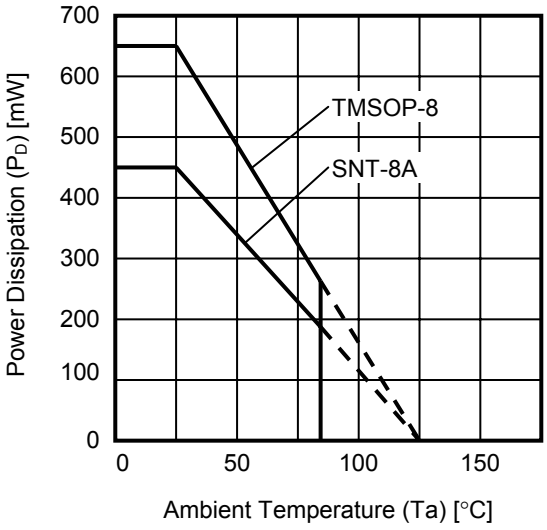


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 5

DC Electrical Characteristics (Ta = +25°C, V_{DD} = 3.0 V unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Operation power supply voltage range	V_{DD}	–	2.65	3.00	5.50	V	–
Current consumption (for 2 circuits)	I_{DD}	$V_{CMR} = V_{OUT} = V_{DD}/2$	–	330	380	μA	5
Input offset voltage	V_{IO}	$V_{CMR} = V_{DD}/2$	−10	±1	+10	μV	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta Ta}$	$V_{CMR} = V_{DD}/2$	–	±0.1	–	μV/°C	1
Input offset current	I_{IO}	–	–	±140	–	pA	–
Input bias current	I_{BIAS}	–	–	±70	–	pA	–
Common-mode input voltage range	V_{CMR}	–	V_{SS}−0.1	–	V_{DD}+0.1	V	2
Voltage gain (open loop)	A_{VOL}	$V_{SS}+0.1\ V \le V_{OUT} \le V_{DD}-0.1\ V$ $V_{CMR} = V_{DD}/2$, R_L = 10 kΩ	110	130	–	dB	8
Maximum output swing voltage	V_{OH}	R_L = 10 kΩ	2.9	–	–	V	3
	V_{OL}	R_L = 10 kΩ	–	–	0.1	V	4
Common-mode input signal rejection ratio	CMRR	$V_{SS}-0.1\ V \le V_{CMR} \le V_{DD}+0.1\ V$	106	130	–	dB	2
Power supply voltage rejection ratio	PSRR	V_{DD} = 2.65 V to 5.50 V	106	120	–	dB	1
Source current	I_{SOURCE}	$V_{OUT} = V_{DD}-0.1$ V	1.3	1.6	–	mA	6
Sink current	I_{SINK}	V_{OUT} = 0.1 V	1.6	2.0	–	mA	7

Table 6

AC Electrical Characteristics (Ta = +25°C, V_{DD} = 3.0 V unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 13**)	–	0.16	–	V/μs
Gain-bandwidth product	GBP	C_L = 0 pF	–	240	–	kHz

■ Test Circuit (Per Circuit)

1. Power supply voltage rejection ratio, input offset voltage

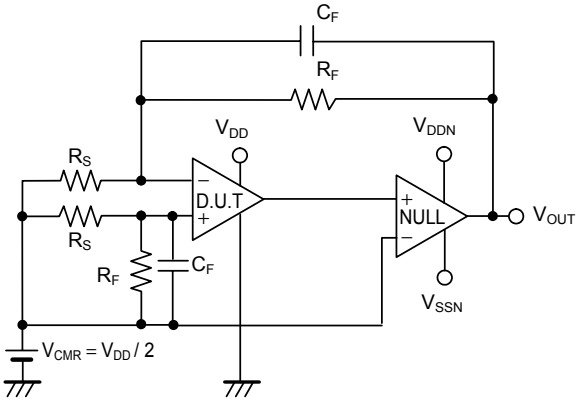


Figure 5

- **Power supply voltage rejection ratio (PSRR)**
  The power supply voltage rejection ratio (PSRR) can be calculated by the following expression, with V_{OUT} measured at each V_{DD}.

  Test conditions:
  When V_{DD} = 2.65 V: $V_{DD} = V_{DD1}$, $V_{OUT} = V_{OUT1}$,
  When V_{DD} = 5.5 V: $V_{DD} = V_{DD2}$, $V_{OUT} = V_{OUT2}$

$$\text{PSRR} = 20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{\left(V_{OUT1} - \frac{V_{DD1}}{2}\right) - \left(V_{OUT2} - \frac{V_{DD2}}{2}\right)} \right| \times \frac{R_F + R_S}{R_S} \right)$$

- **Input offset voltage (V_{IO})**

$$\left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

2. Common-mode input signal rejection ratio, common-mode input voltage range

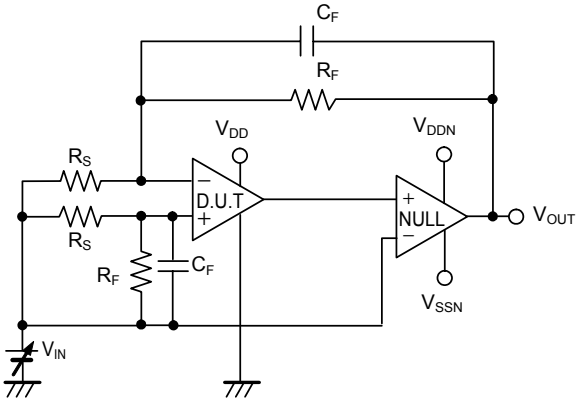


Figure 6

- **Common-mode input signal rejection ratio (CMRR)**
  The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with V_{OUT} measured at each V_{IN}.

  Test conditions:
  When $V_{IN} = V_{CMR\ Max.}$: $V_{IN} = V_{IN1}$, $V_{OUT} = V_{OUT1}$,
  When $V_{IN} = V_{CMR\ Min.}$: $V_{IN} = V_{IN2}$, $V_{OUT} = V_{OUT2}$

$$\text{CMRR} = 20 \log \left(\left| \frac{V_{IN1} - V_{IN2}}{(V_{OUT1} - V_{IN1}) - (V_{OUT2} - V_{IN2})} \right| \times \frac{R_F + R_S}{R_S} \right)$$

- **Common-mode input voltage range (V_{CMR})**
  The common-mode input voltage range is the range of V_{IN} in which V_{OUT} satisfies the common-mode input signal rejection ratio specifications.

3. Maximum output swing voltage (V_{OH})

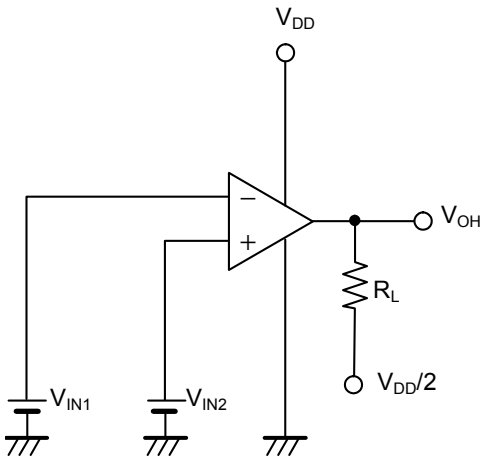


Figure 7

- **Maximum output swing voltage (V_{OH})**

Test conditions:

$$V_{IN1} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

R_L = 10 kΩ

4. Maximum output swing voltage (V_{OL})

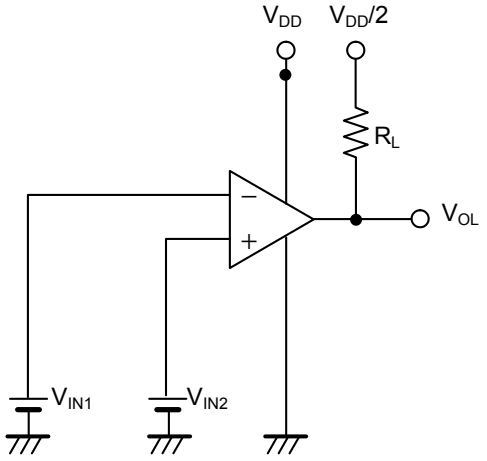


Figure 8

- **Maximum output swing voltage (V_{OL})**

Test conditions:

$$V_{IN1} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

R_L = 10 kΩ

5. Current consumption

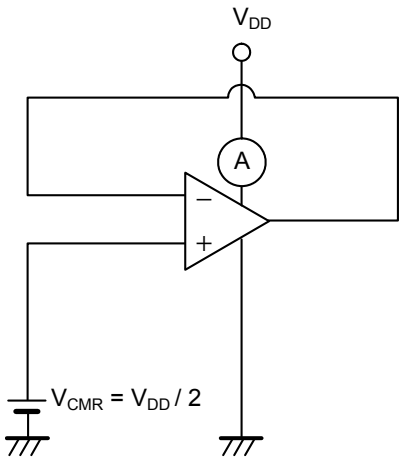


Figure 9

- **Current consumption (I_{DD})**

6. Source current

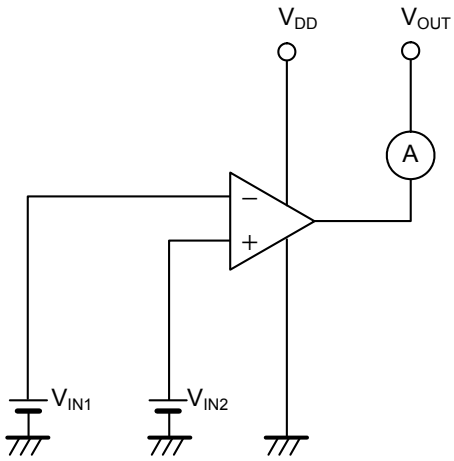


Figure 10

- **Source current (I_{SOURCE})**

Test conditions:

$V_{OUT} = V_{DD} - 0.1$ V

$V_{IN1} = \frac{V_{DD}}{2} - 0.1$ V

$V_{IN2} = \frac{V_{DD}}{2} + 0.1$ V

7. Sink current

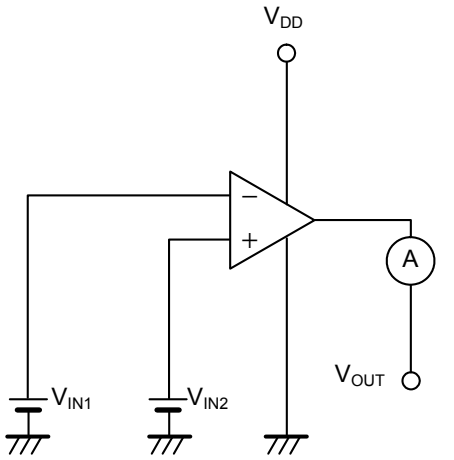


Figure 11

- **Sink current (I_{SINK})**

Test conditions:

$V_{OUT} = 0.1$ V

$V_{IN1} = \frac{V_{DD}}{2} + 0.1$ V

$V_{IN2} = \frac{V_{DD}}{2} - 0.1$ V

8. Voltage gain (open loop)

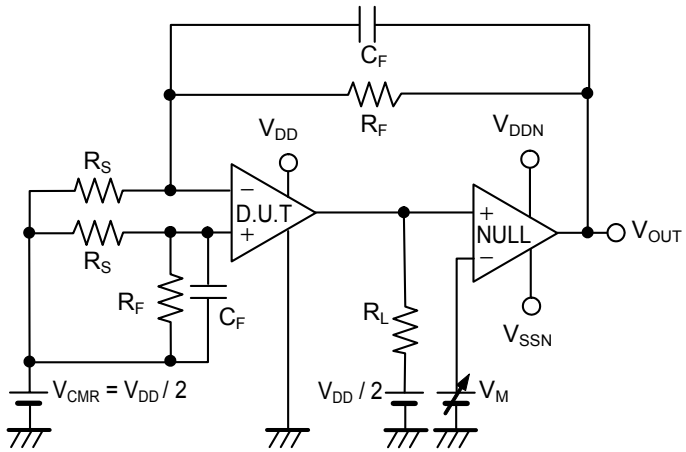


Figure 12

- **Voltage-gain (open loop) (A_{VOL})**
  The voltage gain (A_{VOL}) can be calculated by the following expression, with measured V_{OUT} at each V_M.

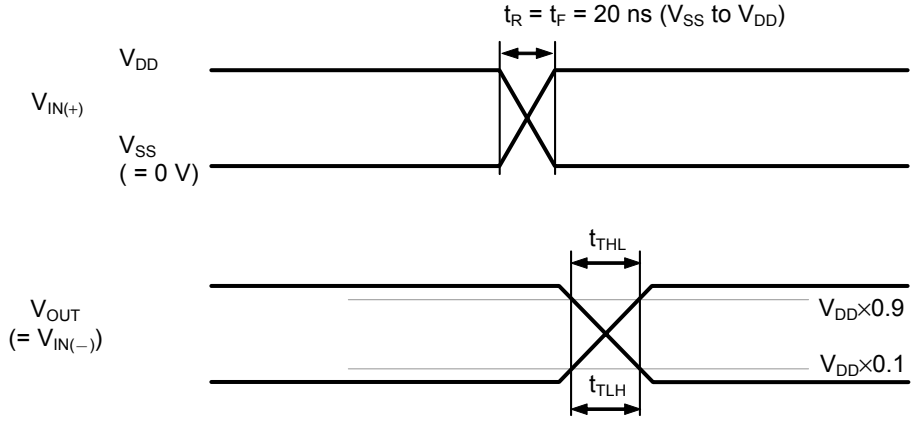
  Test conditions:
  When $V_M = V_{DD} - 0.1$ V: $V_M = V_{M1}$, $V_{OUT} = V_{OUT1}$,
  When $V_M = 0.1$ V: $V_M = V_{M2}$, $V_{OUT} = V_{OUT2}$

$$A_{VOL} = 20 \log \left(\left| \frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

  $R_L = 10\ k\Omega$

9. Slew rate (SR)

Measured by the voltage follower circuit.

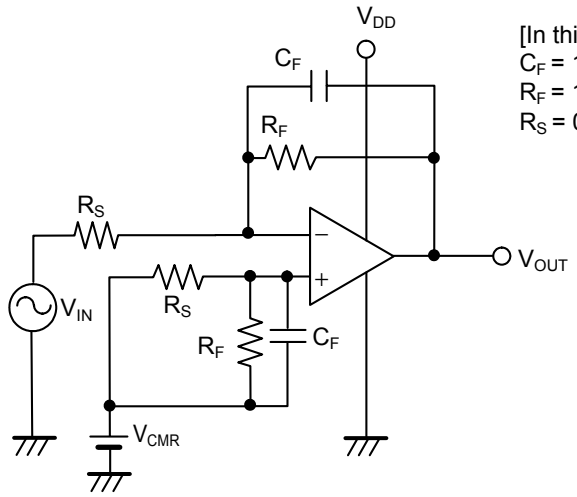


At fall
$$SR = \frac{V_{DD} \times 0.8}{t_{THL}}$$

At rise
$$SR = \frac{V_{DD} \times 0.8}{t_{TLH}}$$

Figure 13

■ Usage Example



[In this example; Gain = ×1000]
C_F = 1000 pF
R_F = 100 kΩ
R_S = 0.1 kΩ

Figure 14

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
- Use this IC with the output voltage 10 mA or less.
- This IC operates stably even directly connecting a load capacitance 150 pF or less to the output pin, as seen in **Figure 15**. When using a load capacitance 150 pF or larger, set a resistor 470 Ω or more, as seen in **Figure 16**. In case of connecting a filter for noise prevention, and using a load capacitance 150 pF or more, also set a resistor 470 Ω or more as seen in **Figure 17**.

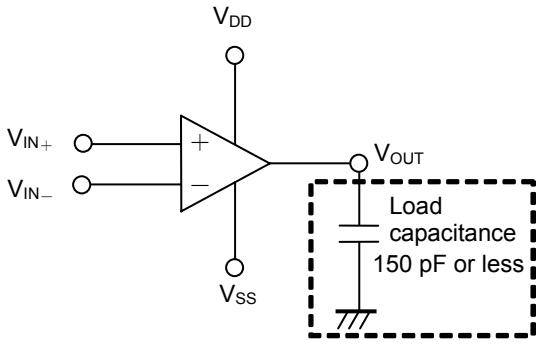


Figure 15

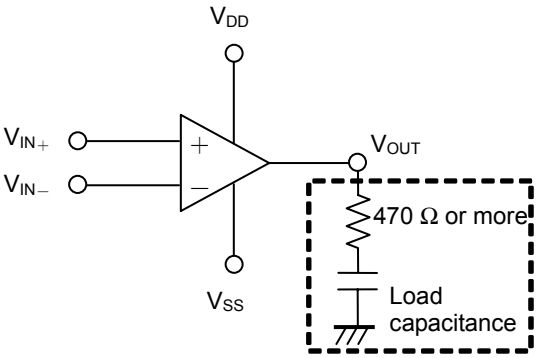


Figure 16

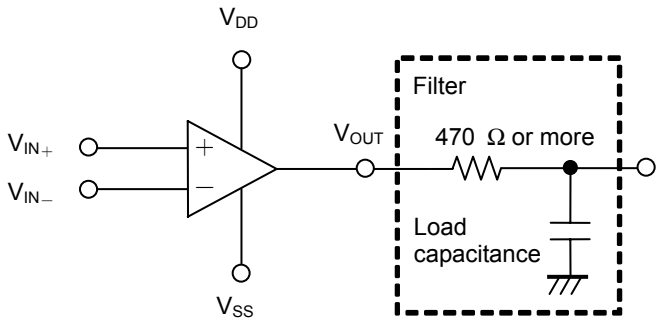
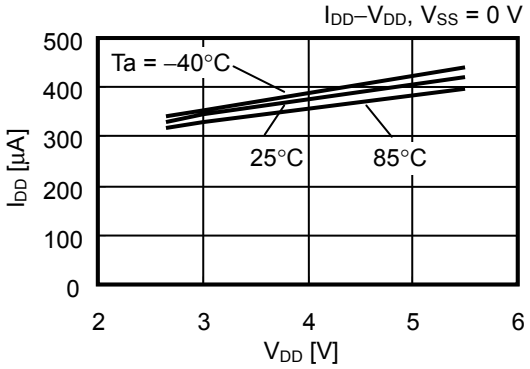


Figure 17

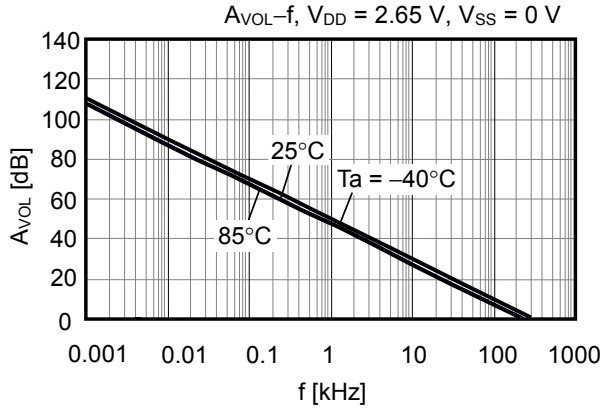
Caution The above connection diagram and constant will not guarantee successful operation. Perform through evaluation using the actual application to set the constant.

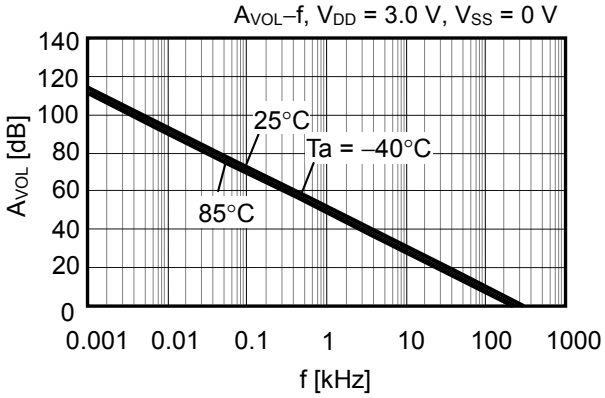
■ Characteristics (Typical Data)

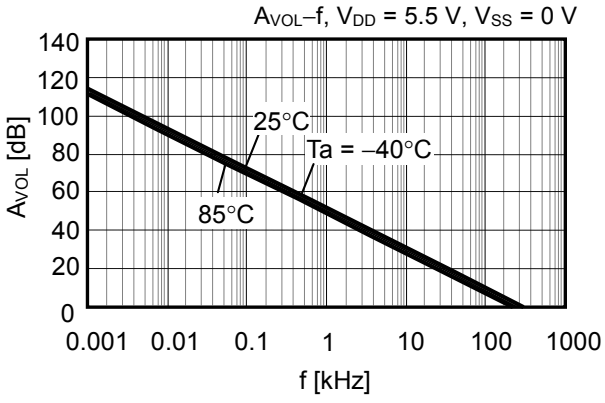
1. Current consumption (for 2 circuits) vs. Power supply voltage



2. Voltage gain vs. Frequency

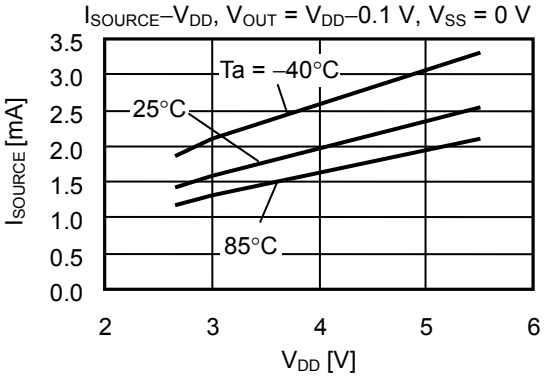




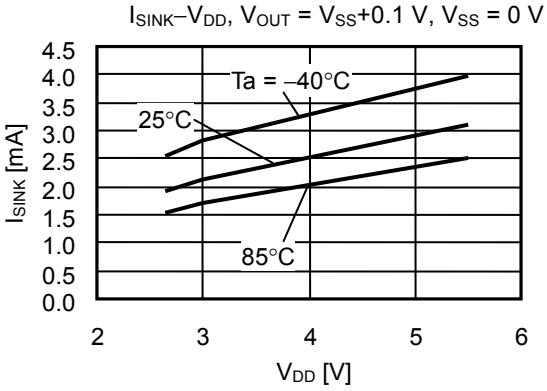


3. Output current

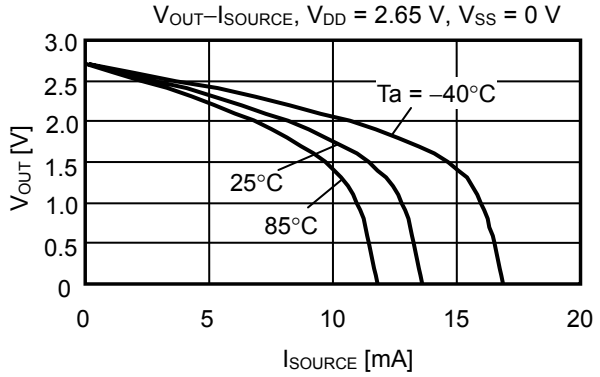
3. 1 I_{SOURCE} vs. Power supply voltage

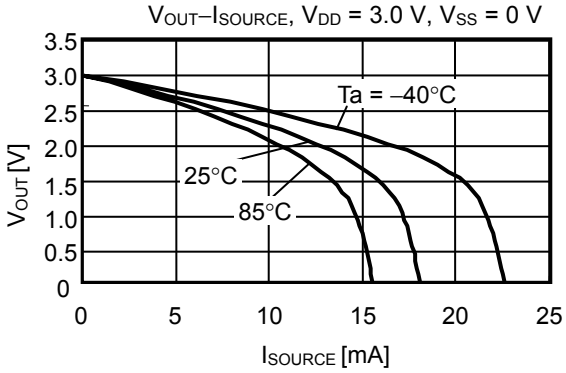


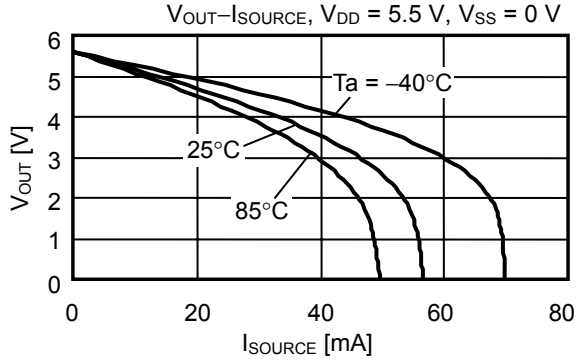
3.2 I_{SINK} vs. Power supply voltage



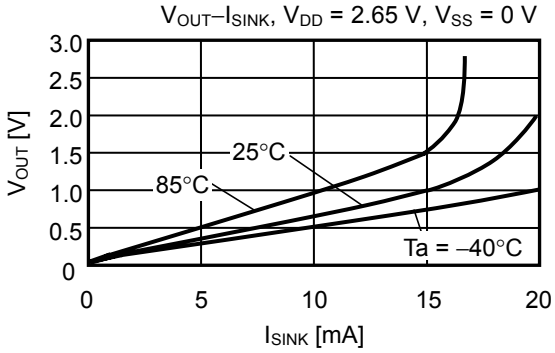
3.3 Output voltage (V_{OUT}) vs. I_{SOURCE} characteristics

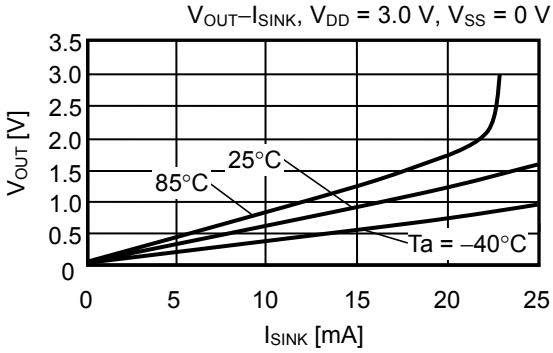


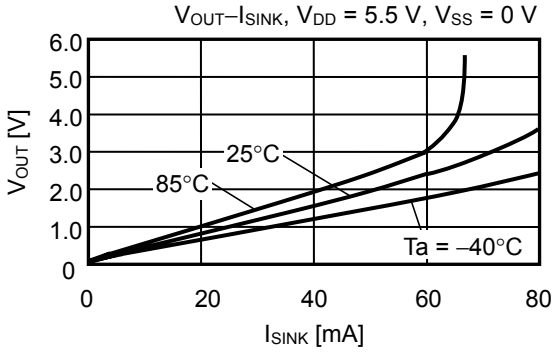




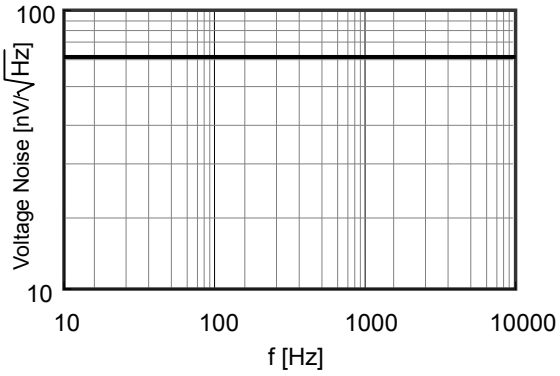
3. 4 Output voltage (V_{OUT}) vs. I_{SINK}

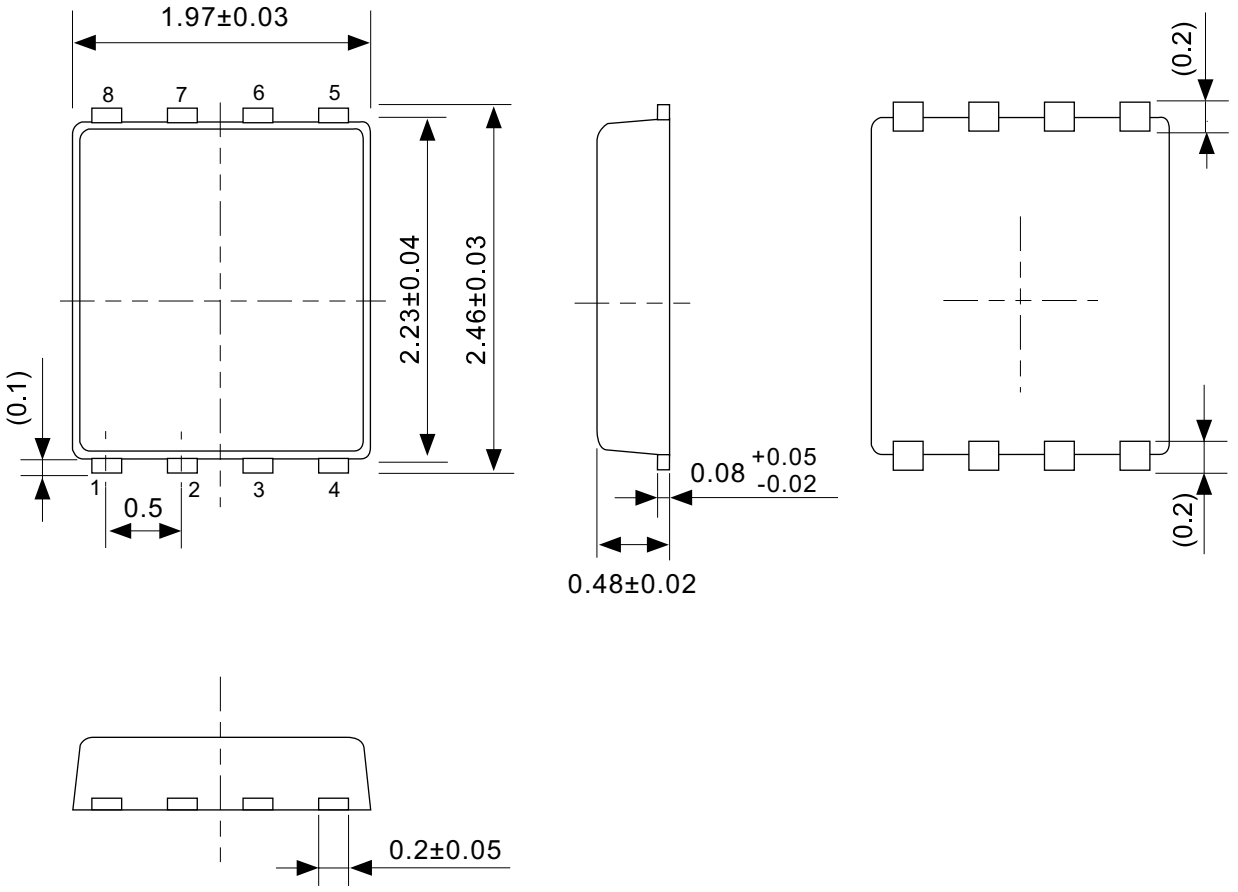






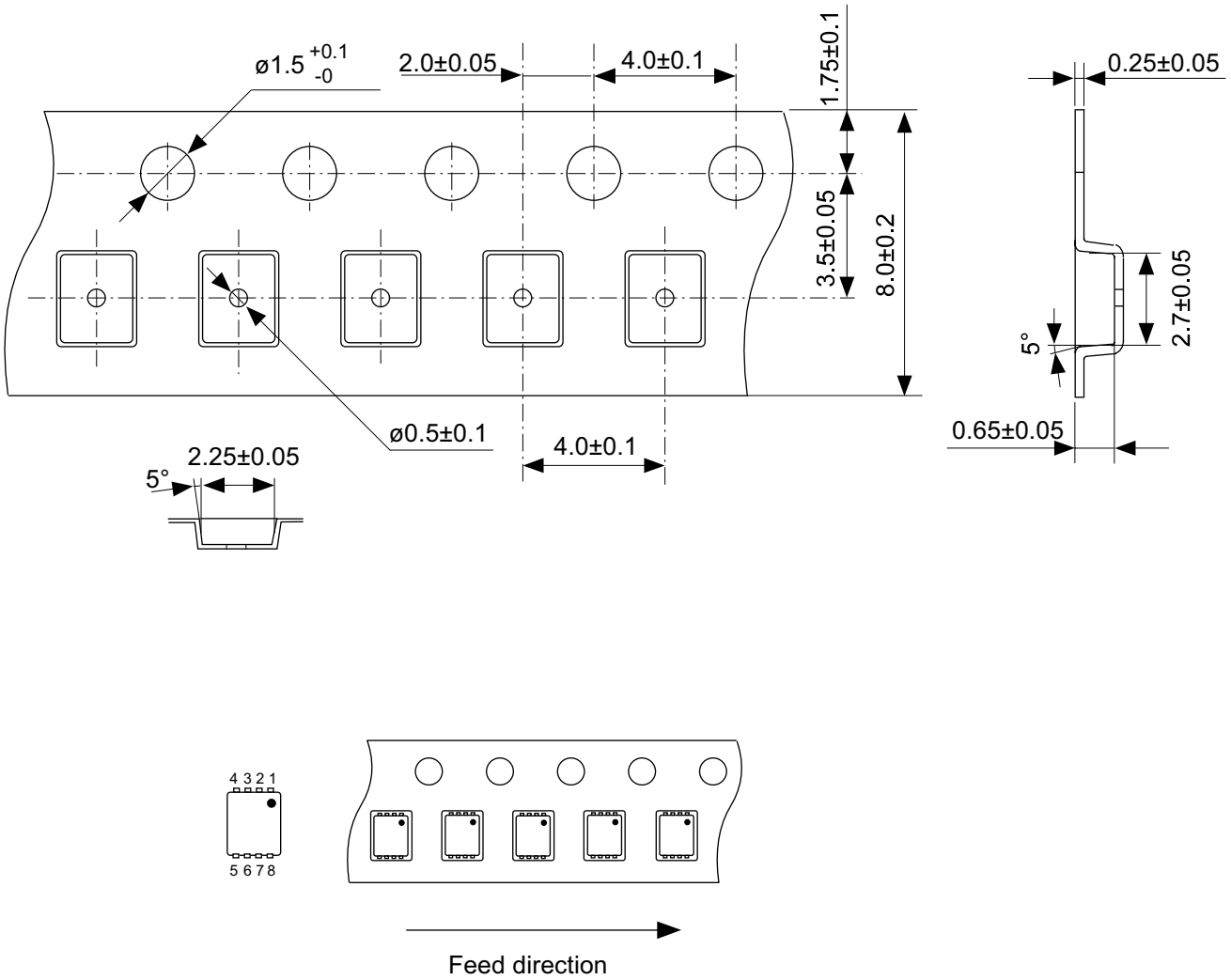
4. Input-referred noise voltage vs. Frequency characteristics





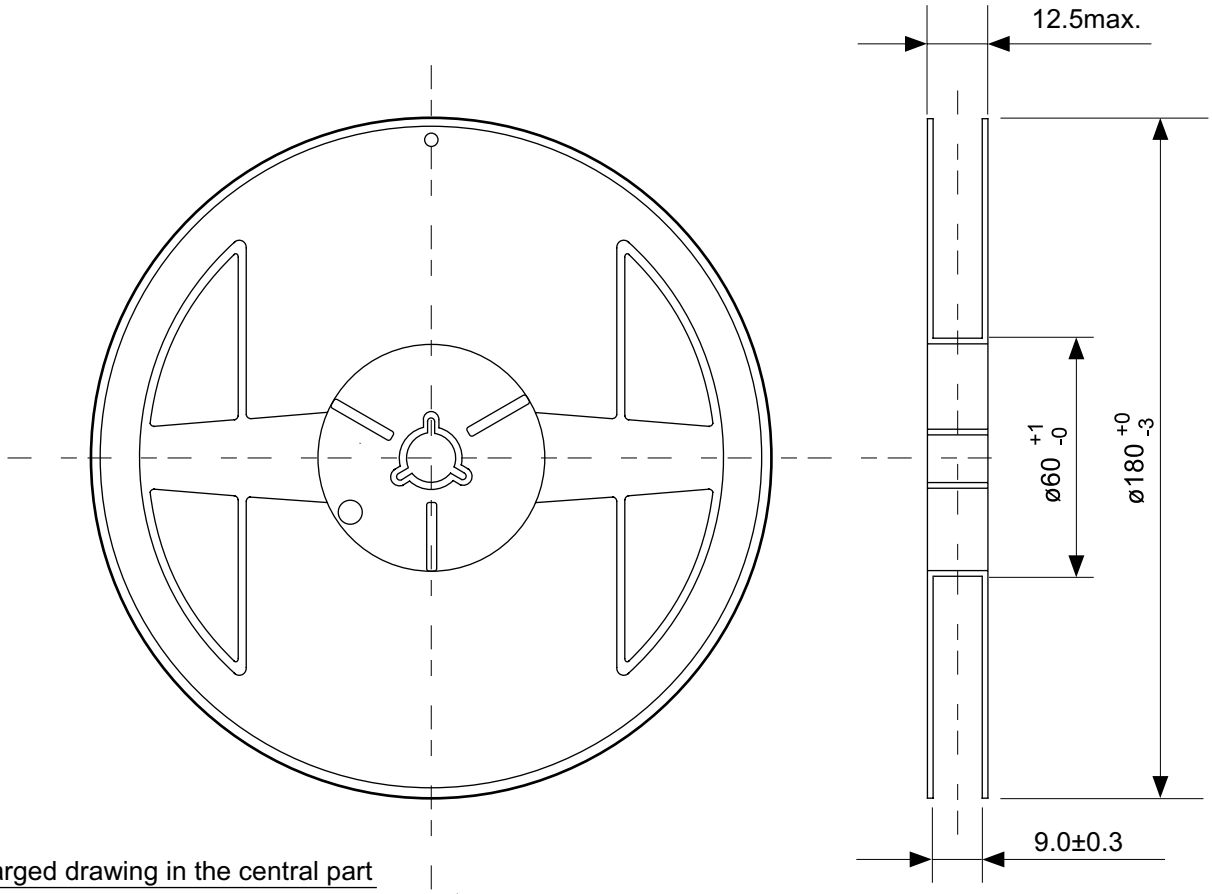
No. PH008-A-P-SD-2.0

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

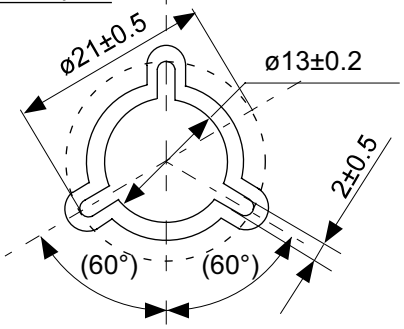


No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

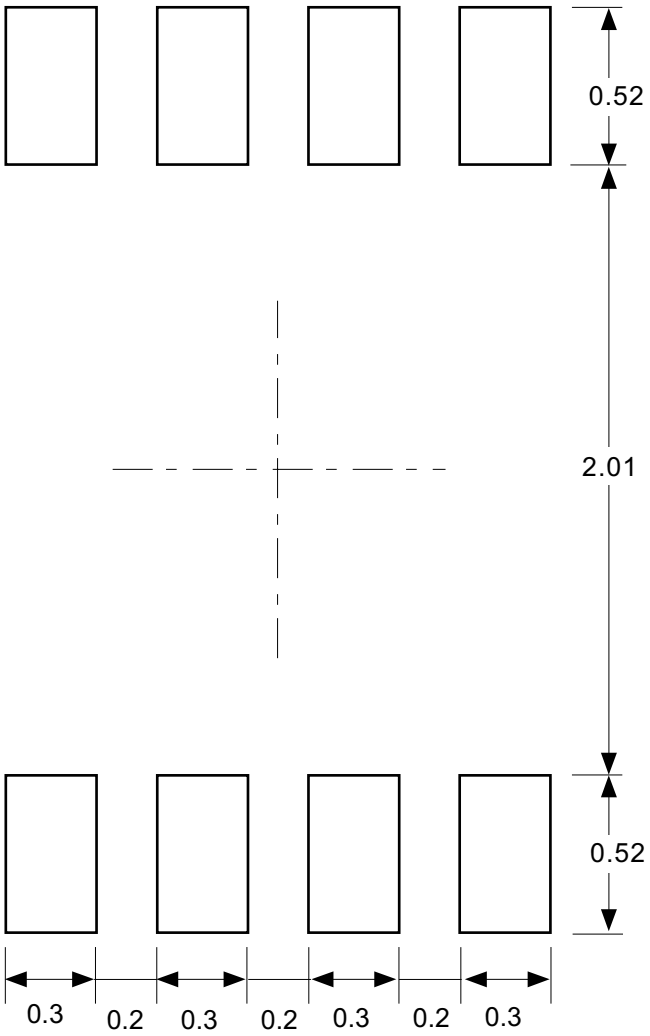


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
Seiko Instruments Inc.			

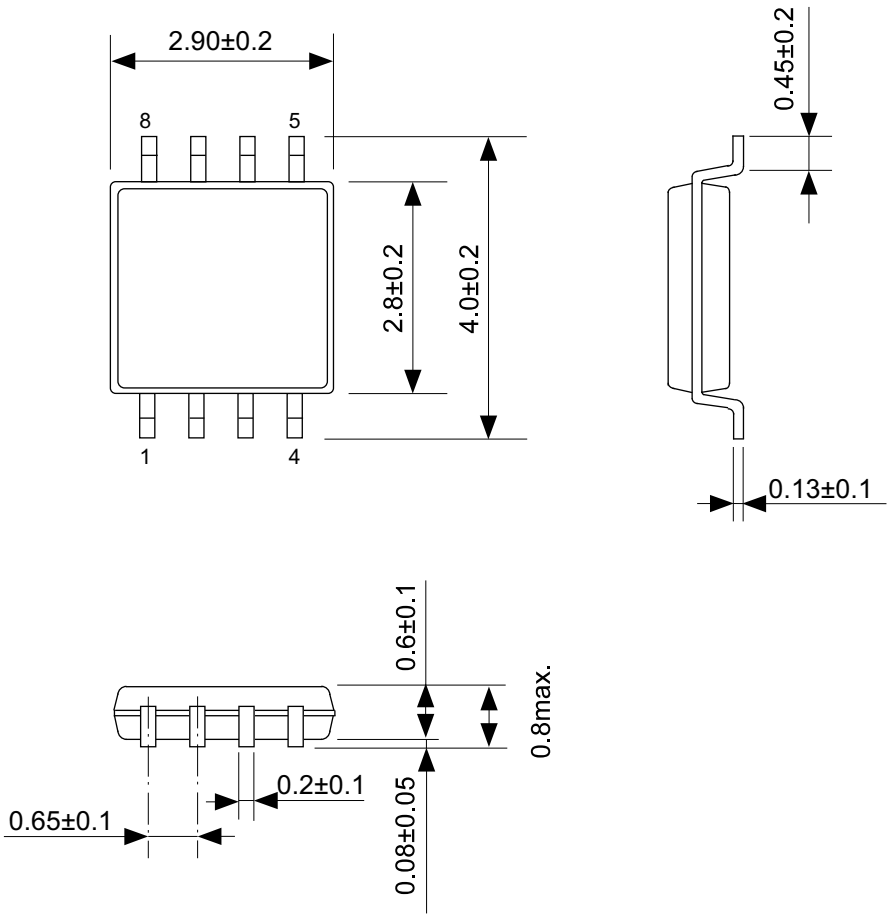


Caution Making the wire pattern under the package is possible. However, note that the package may be upraised due to the thickness made by the silk screen printing and of a solder resist on the pattern because this package does not have the standoff.

注意 パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフが無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージが持ち上がることがありますのでご配慮ください。

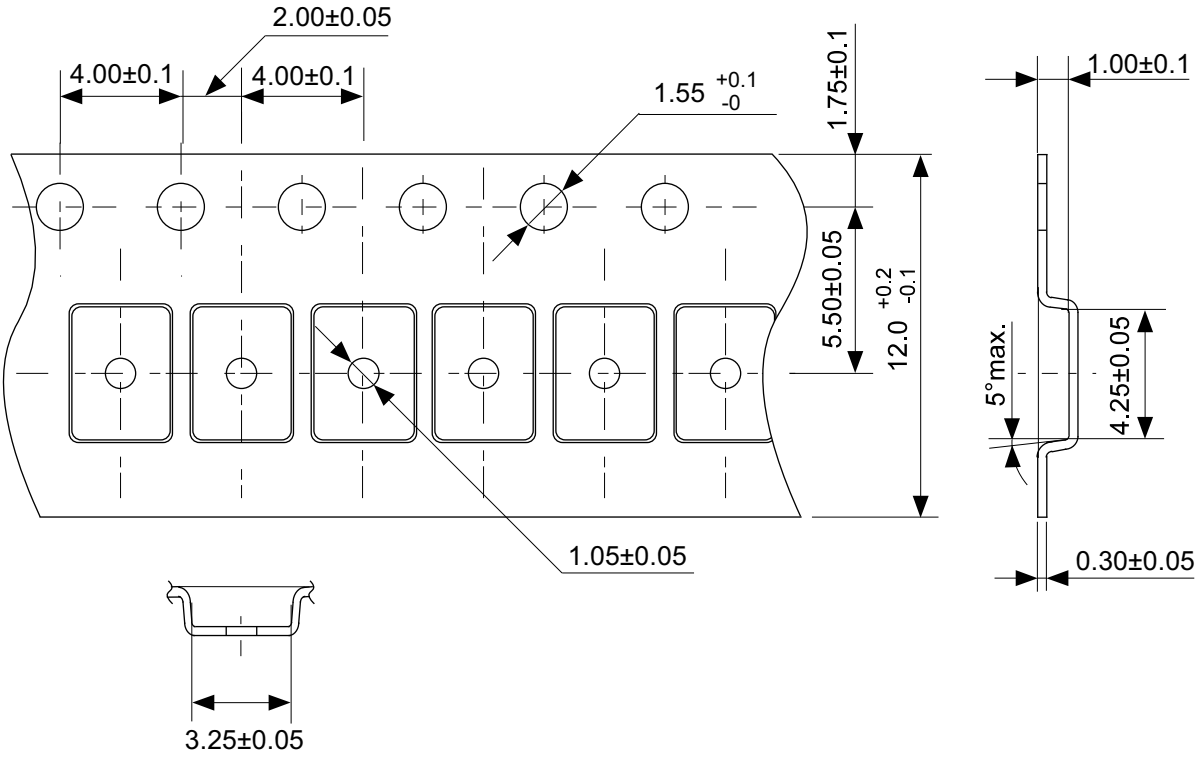
No. PH008-A-L-SD-3.0

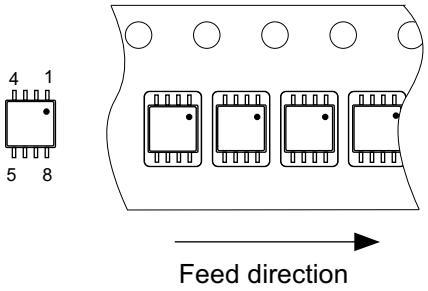
TITLE	SNT-8A-A-Land Recommendation
No.	PH008-A-L-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



No. FM008-A-P-SD-1.0

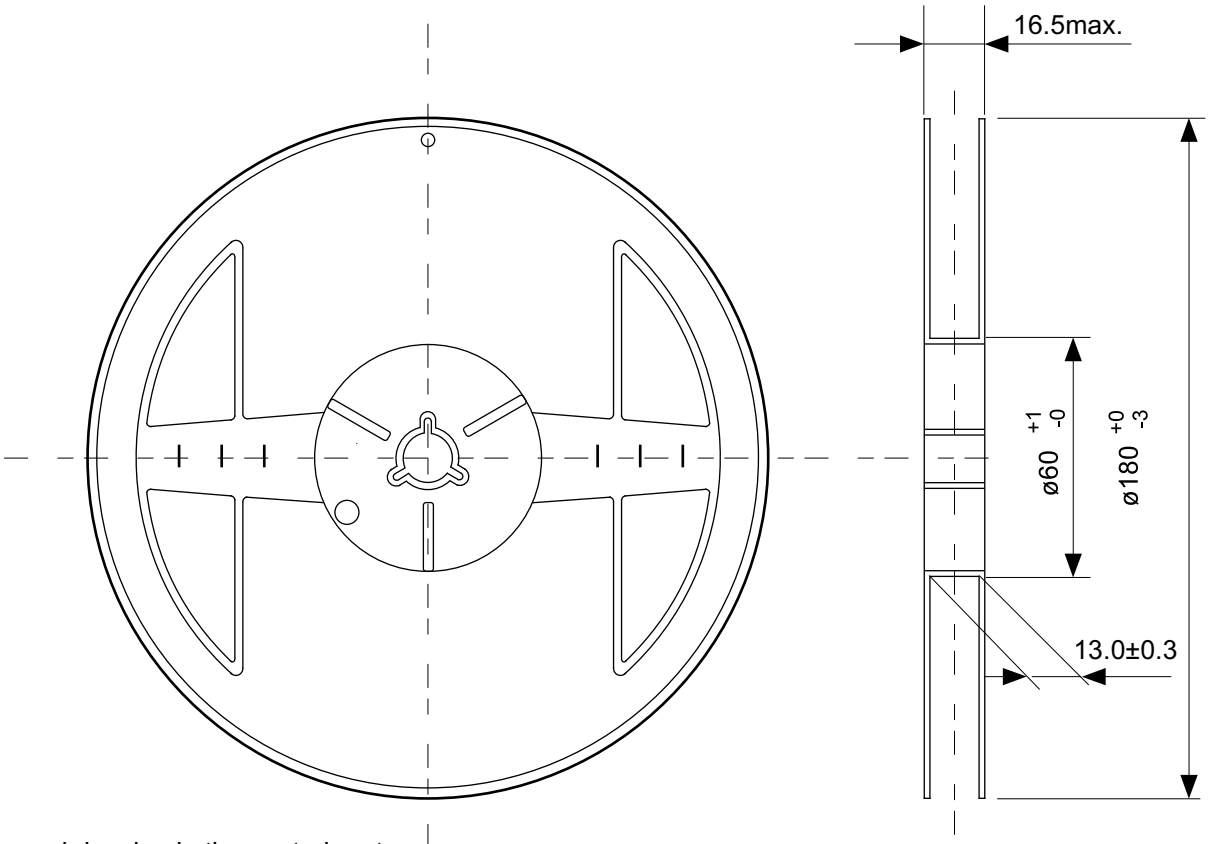
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.0
SCALE	
UNIT	mm
	Seiko Instruments Inc.



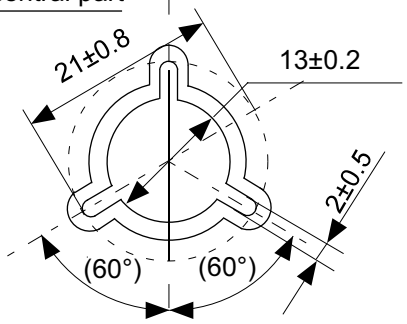


No. FM008-A-C-SD-1.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-1.0
SCALE	
UNIT	mm
	Seiko Instruments Inc.



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
SCALE		QTY.	4,000
UNIT	mm		
	Seiko Instruments Inc.		

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