

8V P-Channel Enhancement-Mode MOSFET

$V_{DS} = -8V$

$R_{DS(ON)}, V_{GS} @ -4.5V, I_{DS} @ \pm 3.5A = 68 m\Omega$

$R_{DS(ON)}, V_{GS} @ -2.5V, I_{DS} @ \pm 3A = 81 m\Omega$

$R_{DS(ON)}, V_{GS} @ -1.8V, I_{DS} @ \pm 2A = 118 m\Omega$

Features

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

Fully Characterized Avalanche Voltage and Current

Improved Shoot-Through FOM

we declare that the material of product compliance with RoHS requirements.

S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

▼ Simple Drive Requirement

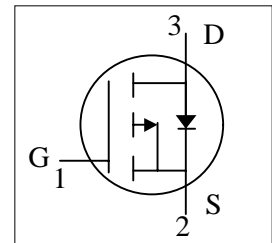
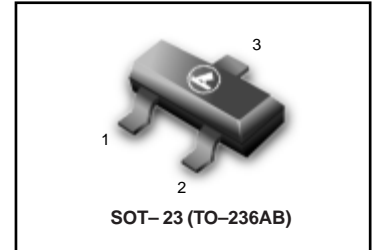
▼ Small Package Outline

▼ Surface Mount Device

Ordering Information

Device	Marking	Shipping
LP2305DSL1G S-LP2305DSL1G	P5S	3000/Tape&Reel
LP2305DSL3G S-LP2305DSL3G	P5S	10000/Tape&Reel

LP2305DSL1G
S-LP2305DSL1G



Maximum Ratings and Thermal Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 8	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current	I_D	-3.5	A
Pulsed Drain Current ¹⁾	I_{DM}	-12	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Total Device Dissipation FR-5 Board $T_A = 25^\circ C$	P_D	1100	mW

Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Thermal Resistance Junction-ambient ³	110	$^\circ C/W$

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static ¹⁾						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-8			V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -3.5A$		47.0	68.0	m Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -2.5V, I_D = -3A$		55.0	81.0	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -1.8V, I_D = -2A$		67.0	118.0	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.45		-0.8	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -6.4V, V_{GS} = 0V$			1	μA
Gate Body Leakage	I_{GSS}	$V_{GS} = \pm 8V, V_{DS} = 0V$			± 100	nA
Forward Transconductance	g_{fs}	$V_{DS} = -5V, I_D = -3.5A$		8.5		S
On-State Drain Current ²⁾	$I_{D(on)}$	$V_{DS} \leq -5V, V_{GS} = -4.5V$	-6			A
		$V_{DS} \leq -5V, V_{GS} = -2.5V$	-3			
Source-Drain Diode						
Max. Diode Forward Current	I_S			-1.6		A
Diode Forward Voltage	V_{SD}	$I_S = -1.6A, V_{GS} = 0V$			-1.2	V
Dynamic ³⁾						
Input Capacitance	C_{iss}	$V_{DS} = -4V, V_{GS} = 0, f = 1MHz$		1245		pF
Output Capacitance	C_{oss}			375		
Reverse Transfer Capacitance	C_{rss}			210		
Switching ³⁾						
Turn-On Time	$t_{d(on)}$	$V_{DD} = -4V, R_L = 4\Omega$ $I_D = -1.0A, V_{GEN} = -4.5V$ $R_G = 6\Omega$		13	20	ns
	t_r			25	40	
Turn-Off Time	$t_{d(off)}$			55	80	
	t_f			19	35	

Note: 1. Static parameters are based on package level with recommended wire-bonding

2.For DESIGN AID ONLY, not subject to production testing.

3.Pulse test: $PW \leq 300\mu s$ duty cycle $\leq 2\%$.

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TYPICAL ELECTRICAL CHARACTERISTICS

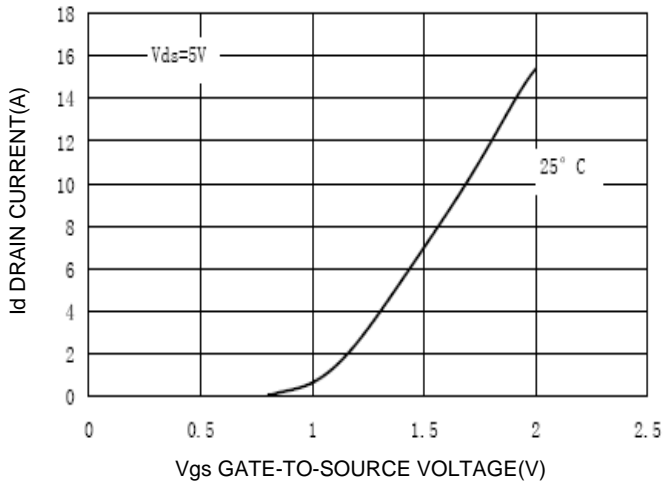


Figure 1. Transfer Characteristics

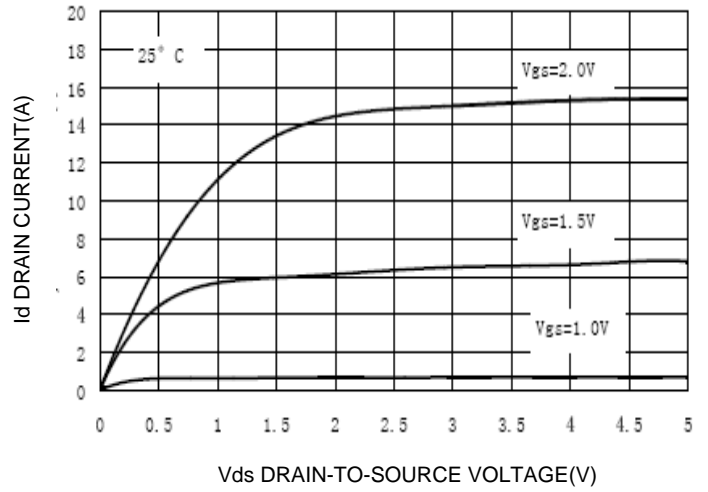


Figure 2. On-Region Characteristics

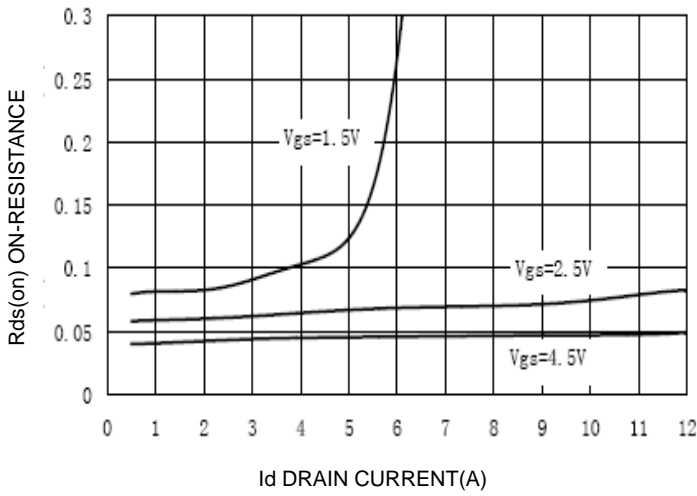


Figure 3. On-Resistance versus Drain Current

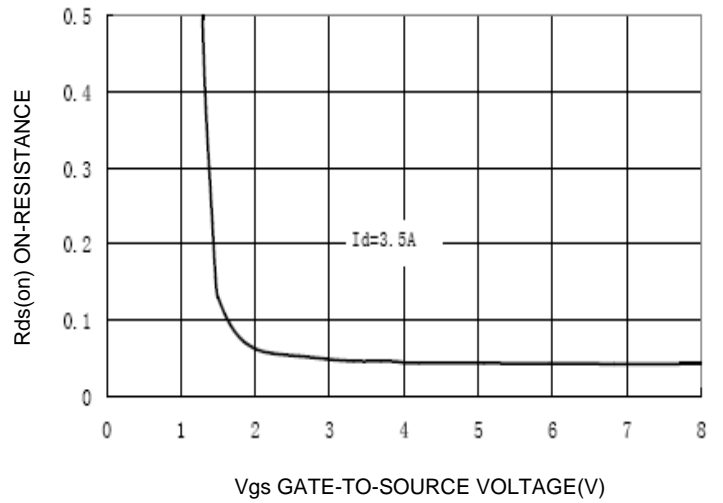


Figure 4. On-Resistance vs. Gate-to-Source Voltage

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TYPICAL ELECTRICAL CHARACTERISTICS

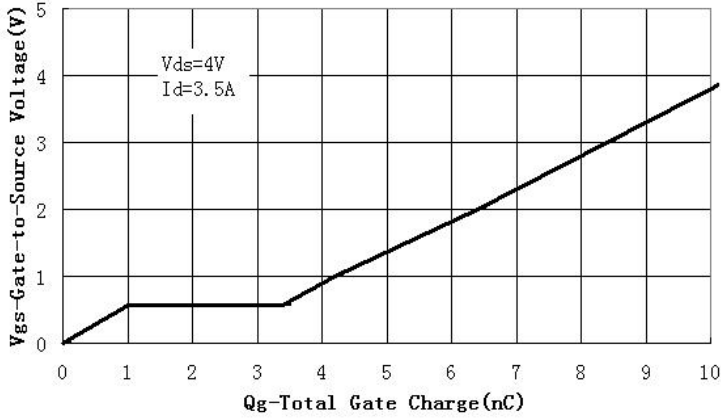


Figure 5. Gate Charge

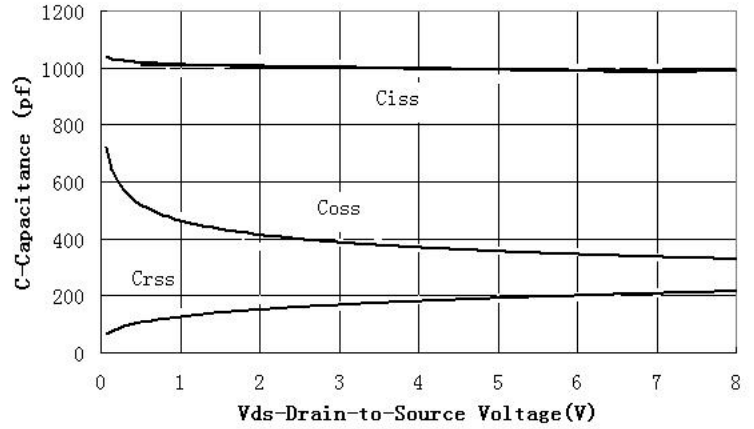


Figure 6. Capacitance

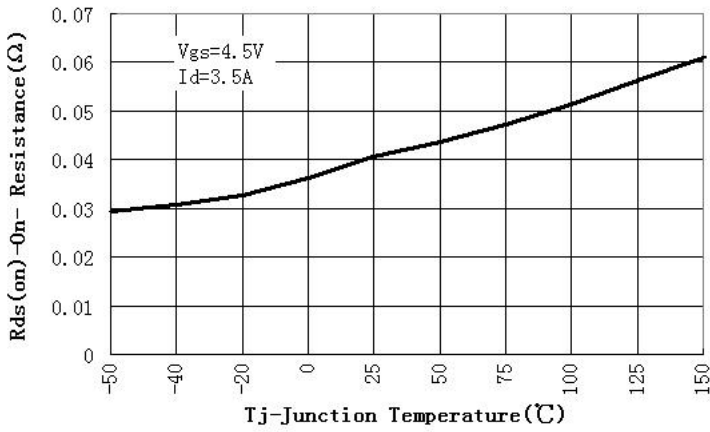


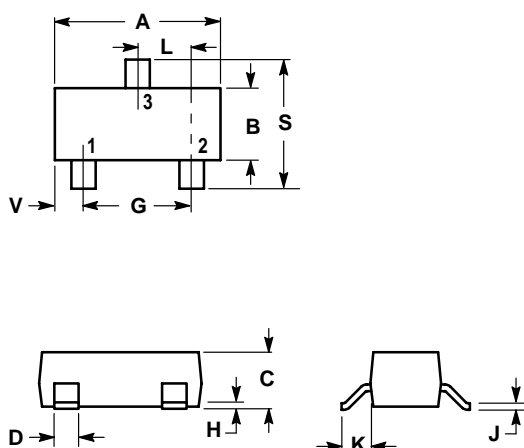
Figure 7. On-Resistance Vs. Junction Temperature

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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

