

N-Channel 1.8-V (G-S) MOSFET

LSI1012N3T5G
S-LSI1012N3T5G

FEATURES

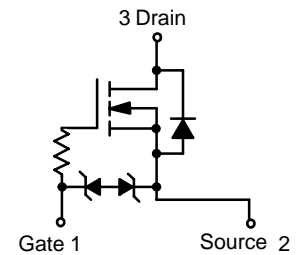
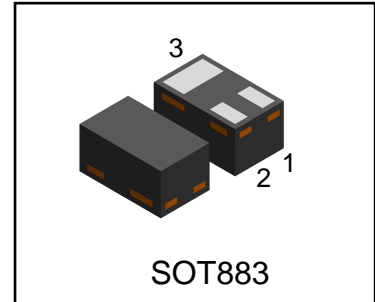
- TrenchFET® Power MOSFET: 1.8-V Rated
- Gate-Source ESD Protected: 2000 V
- High-Side Switching
- Low On-Resistance: 0.7 Ω
- Low Threshold: 0.8 V (typ)
- Fast Switching Speed: 10 ns
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers



ORDERING INFORMATION

Device	Marking	Shipping
LSI1012N3T5G S-LSI1012N3T5G	A2	10000/Tape&Reel

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	20		V
Gate-Source Voltage		V _{GS}	±6		
Continuous Drain Current (T _J = 150°C) ^b	T _A = 25°C	I _D	600	500	mA
	T _A = 85°C		400	350	
Pulsed Drain Current ^a		I _{DM}	1000		
Continuous Source Current (diode conduction) ^b		I _S	275	250	
Maximum Power Dissipation ^b	T _A = 25°C	P _D		250	mW
Thermal Resistance, Junction to Ambient		R _{θJA}		500	°C/W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000		V

a. Pulse width limited by maximum junction temperature.
b. Surface Mounted on FR4 Board.

LSI1012N3T5G , S-LSI1012N3T5G

SPECIFICATIONS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.45		0.9	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±4.5 V		±0.5	±1.0	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V		0.3	100	nA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 85 °C			5	μA
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	700			mA
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 600 mA		0.41	0.70	Ω
		V _{GS} = 2.5 V, I _D = 500 mA		0.53	0.85	
		V _{GS} = 1.8 V, I _D = 350 mA		0.70	1.25	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 400 mA		1.0		S
Diode Forward Voltage ^a	V _{SD}	I _S = 150 mA, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 250 mA		750		pC
Gate-Source Charge	Q _{gs}			75		
Gate-Drain Charge	Q _{gd}			225		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 47 Ω I _D ≅ 200 mA, V _{GEN} = 4.5 V, R _G = 10 Ω		5		ns
Rise Time	t _r			5		
Turn-Off Delay Time	t _{d(off)}			25		
Fall Time	t _f			11		

Notes

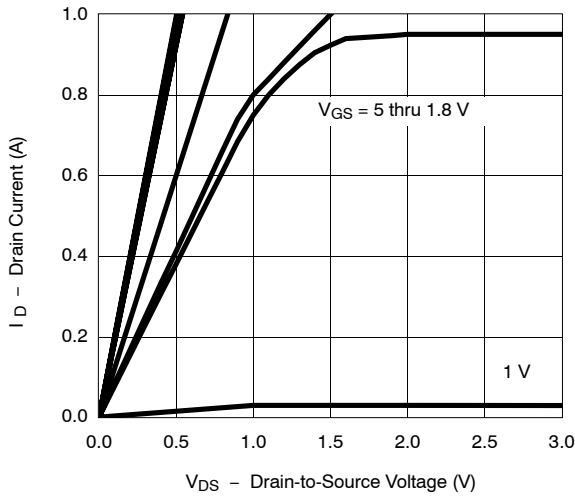
- c. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- d. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

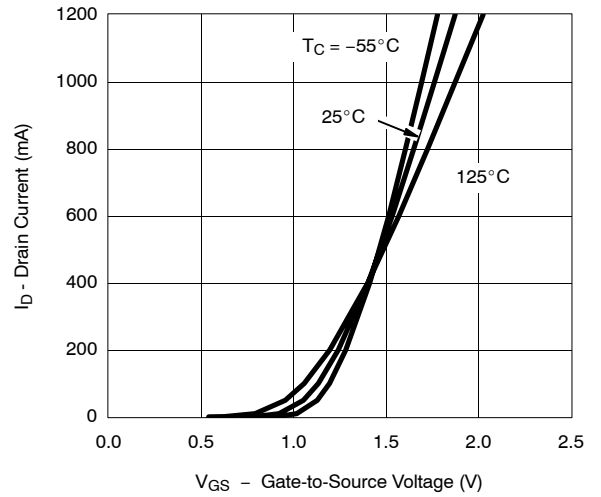
LSI1012N3T5G , S-LSI1012N3T5G

TYPICAL CHARACTERISTICS (T_A = 25 °C UNLESS NOTED)

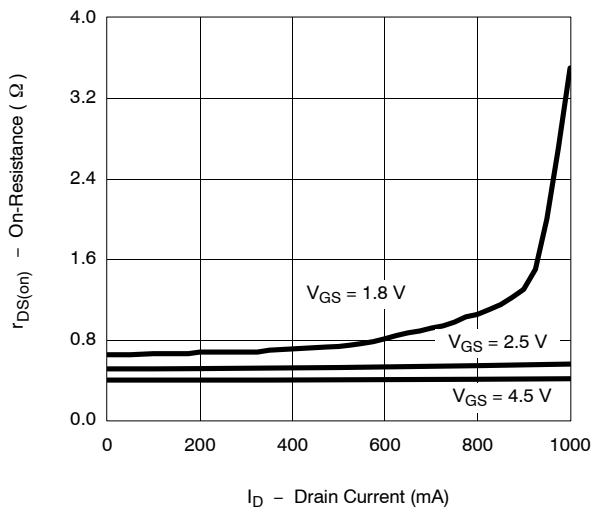
Output Characteristics



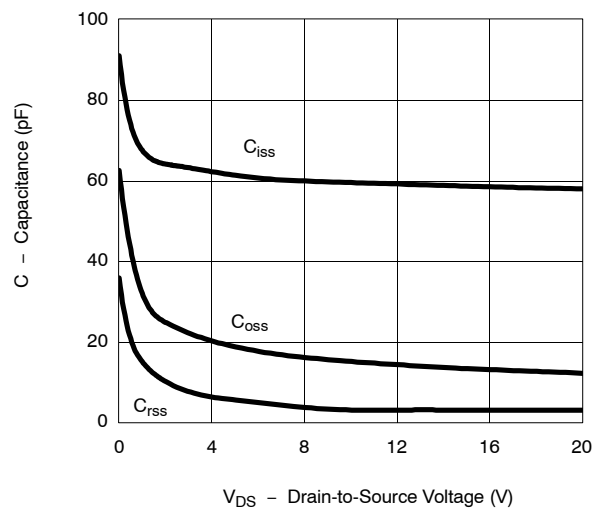
Transfer Characteristics



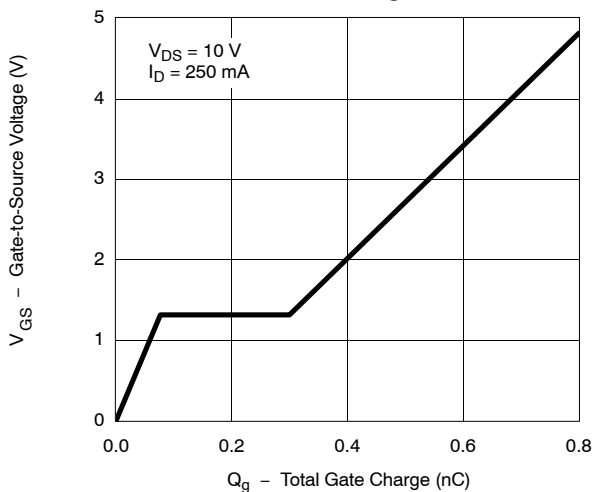
On-Resistance vs. Drain Current



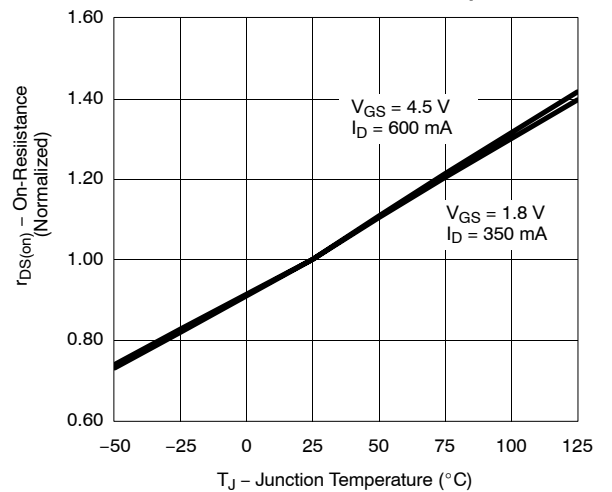
Capacitance



Gate Charge



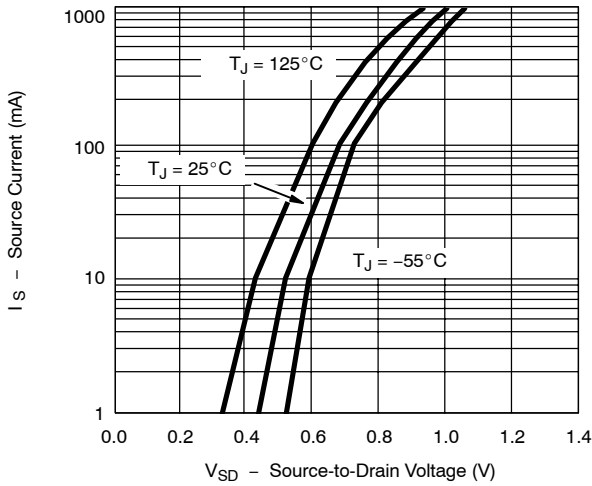
On-Resistance vs. Junction Temperature



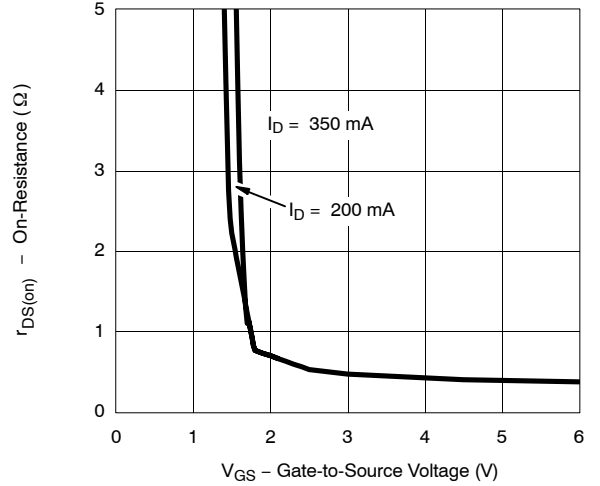
LSI1012N3T5G , S-LSI1012N3T5G

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS NOTED)

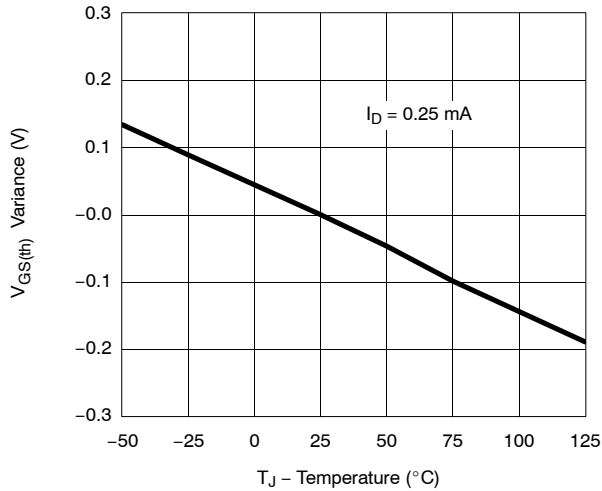
Source-Drain Diode Forward Voltage



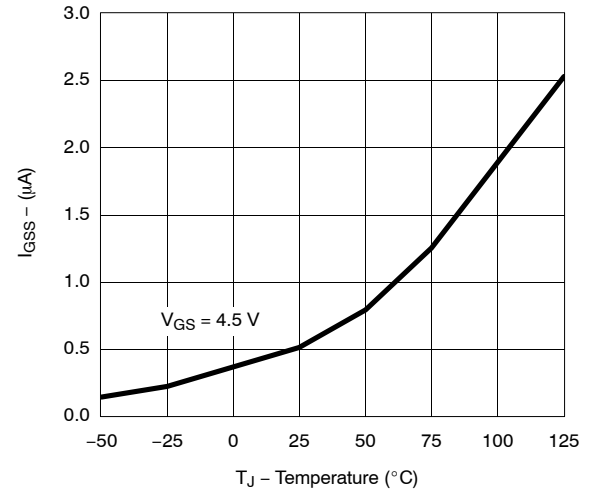
On-Resistance vs. Gate-to-Source Voltage



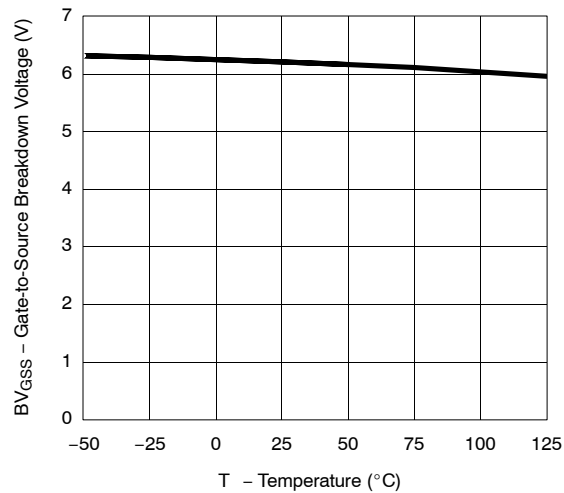
Threshold Voltage Variance vs. Temperature



IGSS vs. Temperature



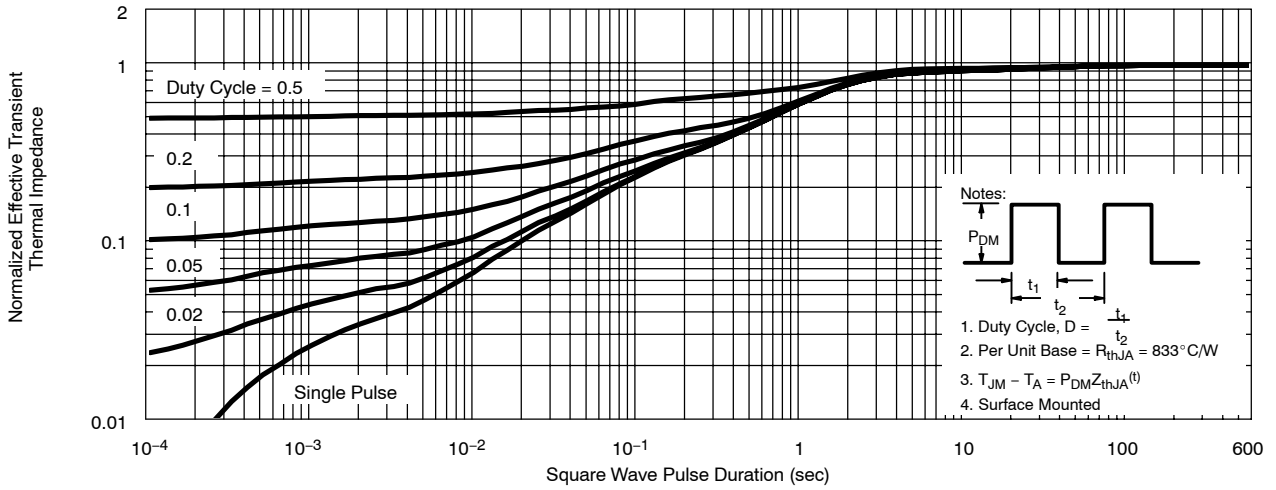
BV_{GSS} vs. Temperature



LSI1012N3T5G , S-LSI1012N3T5G

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Ambient (SC-75A)



Normalized Thermal Transient Impedance, Junction-to-Foot

