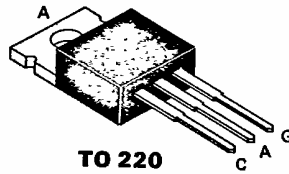


**S1210BH –  
S1210NH SCR'S****12 A 200–800 V 10–25 mA**

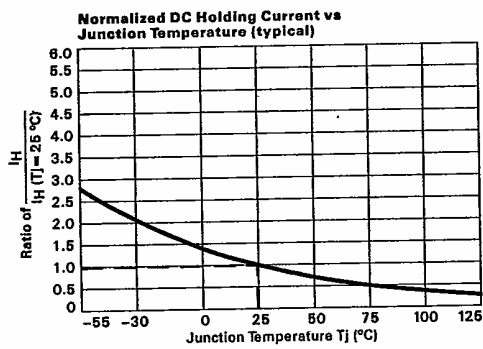
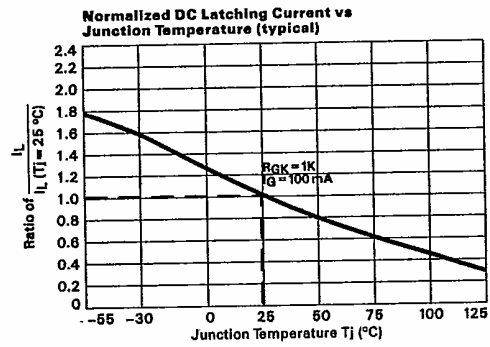
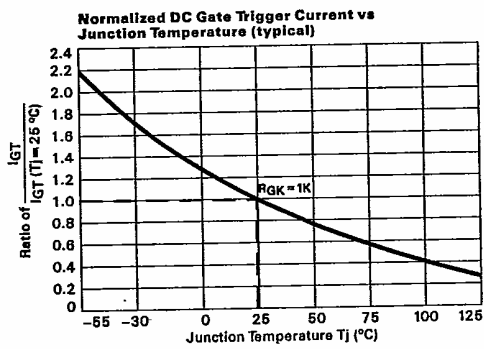
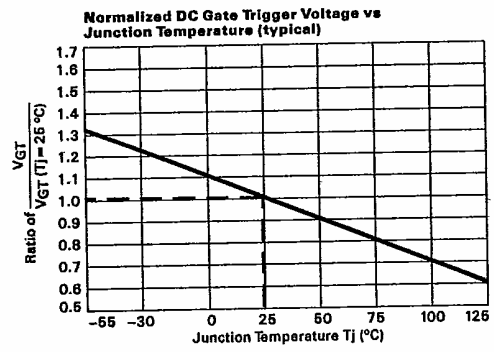
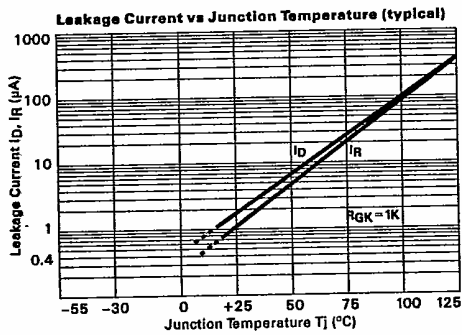
The S1210 series silicon controlled rectifiers are high performance glass passivated PNP devices. These parts are intended for general purpose high current applications where moderate gate insensitivity is required.

**TO 220****Absolute Maximum Ratings**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	<b>S1210BH</b> <b>S1210DH</b> <b>S1210MH</b> <b>S1210NH</b>	[ $V_{DRM}$ ] [ $V_{RRM}$ ]	200 400 600 800		V	[ $T_j = -40^\circ\text{C}$ to $125^\circ\text{C}$ ] [ $R_{GK} = 1\text{K}\Omega$ ]
On-State Current		$I_T(\text{RMS})$	12		A	All Conduction Angles $T_C = 85^\circ\text{C}$
Average On-State Current		$I_T(\text{AV})$	7.6		A	Half Cycle, $\Theta = 180^\circ$ , $T_C = 85^\circ\text{C}$
Nonrept. On-State Current		$I_{TSM}$	132		A	Half Cycle, 60 Hz
Nonrept. On-State Current		$I_{TSM}$	120		A	Half Cycle, 50 Hz
Fusing Current		$I^2t$	72		$\text{A}^2\text{s}$	$t = 10\text{ ms}$ , Half Cycle
Peak Gate Current		$I_{GM}$	4		A	$10\mu\text{s}$ max.
Peak Gate Dissipation		$P_{GM}$	10		W	$10\mu\text{s}$ max.
Gate Dissipation		$P_{G(\text{AV})}$	1		W	20 ms max.
Operating Temperature		$T_j$	-40	125	$^\circ\text{C}$	
Storage Temperature		$T_{stg}$	-40	125	$^\circ\text{C}$	
Soldering Temperature		$T_{sld}$		250	$^\circ\text{C}$	1.6 mm from case, 10 s max.

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	$I_{DRM}/I_{RRM}$	1.5		mA	@ $V_{DRM} + V_{RRM}$ , $R_{GK} = 1\text{K}\Omega$ , $T_j = 125^\circ\text{C}$
Off-State Leakage Current	$I_{DRM}/I_{RRM}$	5		$\mu\text{A}$	@ $V_{DRM} + V_{RRM}$ , $R_{GK} = 1\text{K}\Omega$ , $T_j = 25^\circ\text{C}$
On-State Voltage	$V_T$	1.80		V	at $I_T = 24\text{ A}$ , $T_j = 25^\circ\text{C}$
On-State Threshold Voltage	$V_{T(\text{TO})}$	1.0		V	$T_j = 125^\circ\text{C}$
On-State Slope Resistance	$r_T$		36	$\text{m}\Omega$	$T_j = 125^\circ\text{C}$
Gate Trigger Current	$I_{GT}$	10	25	mA	$V_D = 7\text{ V}$
Gate Trigger Voltage	$V_{GT}$		2.0	V	$V_D = 7\text{ V}$
Holding Current	$I_H$		38	mA	$R_{GK} = 1\text{K}\Omega$
Latching Current	$I_L$		75	mA	$R_{GK} = 1\text{K}\Omega$
Critical Rate of Voltage Rise	$dv/dt$	200		$\text{V}/\mu\text{s}$	$V_D = .67 \times V_{DRM}$ , $R_{GK} = 1\text{K}\Omega$ , $T_j = 125^\circ\text{C}$
Critical Rate of Current Rise	$di/dt$	100		$\text{A}/\mu\text{s}$	$I_G = 125\text{ mA}$ , $di_G/dt = 1.25\text{ A}/\mu\text{s}$ , $T_j = 125^\circ\text{C}$
Gate Controlled Delay Time	$t_{gd}$		500	ns	$I_G = 125\text{ mA}$ , $di_G/dt = 1.25\text{ A}/\mu\text{s}$
Commutated Turn-Off Time	$t_q$		50	$\mu\text{s}$	$T_C = 85^\circ\text{C}$ , $V_D = .67 \times V_{DRM}$ , $V_R = 35\text{ V}$ , $I_T = I_T(\text{AV})$
Thermal Resistance junc. to case	$R_{\theta jc}$		3	K/W	
Thermal Resistance junc. to amb.	$R_{\theta ja}$		60	K/W	



## Typical Characteristics S12 - Packaged Parts

