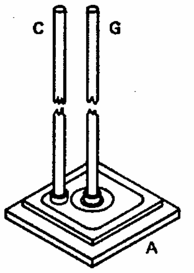
TAG SEMICONDUCTORS LTD

S1210BS –
S1210MS SCR'S

12 A 200–600 V 10–25 mA

The S1210 series silicon controlled rectifiers are high performance glass passivated PNPN devices. These parts are intended for hybrid applications.



SUB MINI

Absolute Maximum Ratings $T_A = 25\,°C$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	**S1210BS**	$\begin{bmatrix} V_{DRM} \\ V_{RRM} \end{bmatrix}$	200		V	$\begin{bmatrix} T_j = -40\,°C \text{ to } 125\,°C \\ R_{GK} = 1\,K\Omega \end{bmatrix}$
	S1210DS		400		V	
	S1210MS		600		V	
On-State Current		$I_{T(RMS)}$	12		A	All Conduction Angles $T_C = 85\,°C$
Average On-State Current		$I_{T(AV)}$	7.6		A	Half Cycle, $\Theta = 180°$, $T_C = 85\,°C$
Nonrept. On-State Current		I_{TSM}	132		A	Half Cycle, 60 Hz
Nonrept. On-State Current		I_{TSM}	120		A	Half Cycle, 50 Hz
Fusing Current		I^2t	72		A^2s	t = 10 ms, Half Cycle
Peak Gate Current		I_{GM}	4		A	10µs max.
Peak Gate Dissipation		P_{GM}	10		W	10µs max.
Gate Dissipation		$P_{G(AV)}$	1		W	20 ms max.
Operating Temperature		Tj	−40	125	°C	
Storage Temperature		T_{stg}	−40	150	°C	
Case Temperature		T_C			°C	Temperature measured on the substrate immediately adjacent to the Chip

Electrical Characteristics $T_A = 25\,°C$ unless otherwise noted

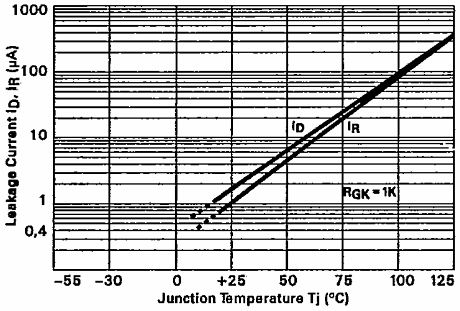
Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}/I_{RRM}		1.5	mA	@$V_{DRM} + V_{RRM}$, $R_{GK} = 1\,K\Omega$, $T_j = 125\,°C$
Off-State Leakage Current	I_{DRM}/I_{RRM}		5.0	µA	@$V_{DRM} + V_{RRM}$, $R_{GK} = 1\,K\Omega$, $T_j = 25\,°C$
On-State Voltage	V_T		1.80	V	at $I_T = 24\,A$, $T_j = 25\,°C$
On-State Threshold Voltage	$V_{T(TO)}$		1.0	V	$T_j = 125\,°C$
On-State Slope Resistance	r_T		36	mΩ	$T_j = 125\,°C$
Gate Trigger Current	I_{GT}	10	25	mA	$V_D = 7\,V$
Gate Trigger Voltage	V_{GT}		2.0	V	$V_D = 7\,V$
Holding Current	I_H		38	mA	$R_{GK} = 1\,K\Omega$
Latching Current	I_L		75	mA	$R_{GK} = 1\,K\Omega$
Critical Rate of Voltage Rise	dv/dt	200		V/µs	$V_D = .67 x V_{DRM}$ $R_{GK} = 1\,K\Omega$ $T_j = 125\,°C$
Critical Rate of Current Rise	di/dt	100		A/µs	$I_G = 125\,mA$ $di_G/dt = 1.25\,A/µs$ $T_j = 125\,°C$
Gate Controlled Delay Time	t_{gd}		500	ns	$I_G = 125\,mA$ $di_G/dt = 1.25\,A/µs$
Commutated Turn-Off Time	t_q		50	µs	$T_C = 85\,°C$ $V_D = .67 x V_{DRM}$ $V_R = 35\,V$ $I_T = I_T(AV)$
Thermal Resistance junc. to case	$R_{\Theta jc}$		1.2	K/W	50 micron solder on backside of Chip

Parts are 100% tested in Chip form with visual inspection after assembly.

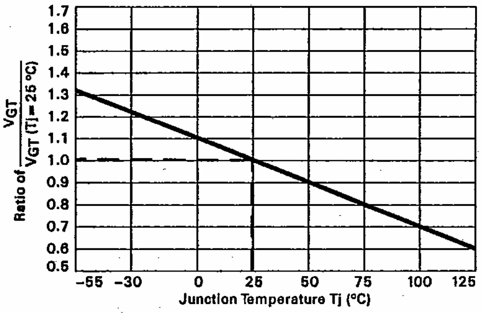
Per MIL-STD-105-D, parts will pass AQL 4.0 income inspection.

Typical Characteristics
S12 – Chips

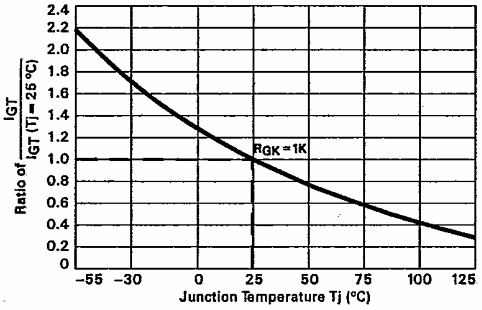
Leakage Current vs Junction Temperature (typical)



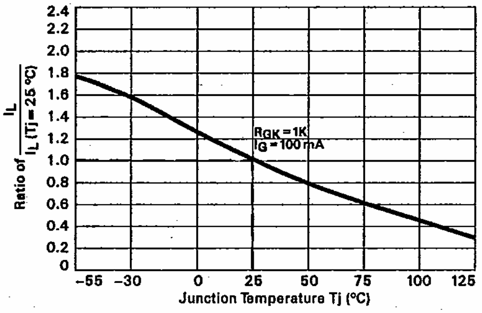
Normalized DC Gate Trigger Voltage vs Junction Temperature (typical)



Normalized DC Gate Trigger Current vs Junction Temperature (typical)



Normalized DC Latching Current vs Junction Temperature (typical)



Normalized DC Holding Current vs Junction Temperature (typical)