

## Description

The S19233 10 GbE/FC/SONET/SDH/FEC dual Clock Data Recovery (CDR) is one of the latest additions to the AMCC product family. S19233 device contains dual CDRs that provide fully integrated clock recovery signal conditioning capabilities for low power 10 Gbps applications. The device performs all necessary clock and data recovery/clock clean-up functions in conformance with SONET/SDH, 10GbE, 10 Gbps FC and G.709 transmission standards. The S19233 is primarily designed to be used in the XFP MSA module. The standard operating range is from 9.95 Gbps to 11.3 Gbps. Figure 1, *System Block Diagram*, shows a typical network application.

## Overview

The S19233 can be used to implement the front end of SONET/SDH/FEC/10GbE/10GFC equipment which consists primarily of the serial transmit interface and the serial receive interface.

The system circuitry consists of a high-speed phase detector, clock dividers, and equalization circuitry. The device utilizes on-chip clock recovery/clock clean-up PLL components that allow the use of a slower external clock reference, 155.52 MHz (or equivalent FEC/10GbE/10 Gbps FC rates), in support of existing system clocking schemes.

An equalizer is integrated in the receive front end of the TX side and it reshapes the data after transmission over a standard FR-4 material. This enables low bit error rate and transmission over longer distances. The device would allow users to meet the maximum dispersion penalty per ITU LR 2a, b, & c specifications with margin. Integrated in the S19233 on the receive optical side is an adjustable filter (DispersionXX™), offset cancellation circuitry to improve sensitivity, limiting amp with threshold Adjust, and a CDR with phase adjust.

The low-jitter, 1-bit, CML interfaces guarantee compliance with the bit-error rate requirements of the Telcordia and ITU-T standards. The high speed serial input and output can be connected to the AMCC SerDes (S19235 or S19237) or others across 24 inches of standard FR-4 with one connector.

The S19233 is packaged in a 6 mm X 6 mm package, offering designers a small package outline.

## - At a Glance -

### General Features

- Complies with ITU-T specifications, 2.7 mUI<sub>rms</sub> max. jitter generation (50 KHz - 80 MHz)
- Complies with XFP MSA Specifications
- 9.95 to 11.3 Gbps operation
- Optimized for up to 100 Km SMF
- Dual CDR - Typical Power 0.6 W
- Optical and Electrical Loopbacks
- Threshold & Phase Adjust
- CML serial input sensitivity at 10 mV pk-pk Differential
- Offset Cancellation Circuit
- RSSI - Receive Signal Strength Indicator
- LOS - Loss of Signal detect
- Termination and Biasing for AC coupling
- Power Down CDR Mode
- Reference clocks range 155 - 176 MHz
- Equalization on the Electrical Receive Side
- Lock detect indication
- -40 to 85 °C operation
- 1.8/3.3 Volt Power Supply
- I<sup>2</sup>C serial Interface

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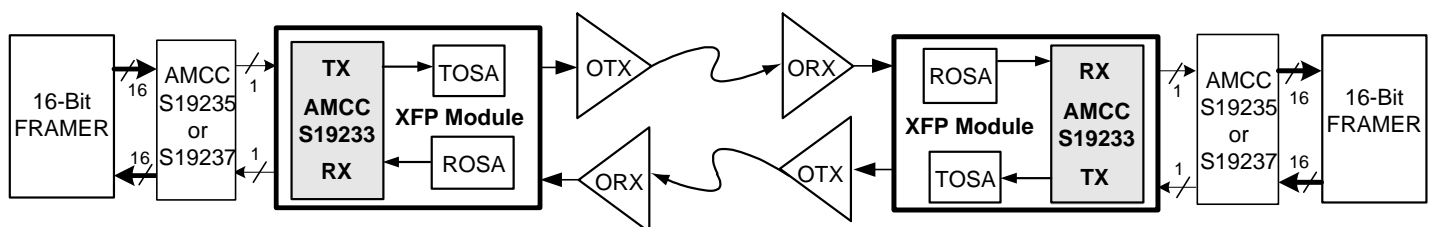


Figure 1. System Block Diagram

The sequence of operations is as follows:

**Transmitter Operations**

1. 1-bit serial data input
2. Equalization to compensate for 24+ inches of FR-4
3. Clock recovery
4. Data retiming
5. Serial data output

**Receiver Operations**

1. Serial input to post amp
2. Equalization adjust
3. 10 mV input sensitivity (differential)
4. Threshold adjustment
5. Lock detect
6. Clock and Data recovery
7. Serial data output

Internal clocking and control functions are transparent to the user.

**AMCC Suggested Interface Devices**

S19235	SONET/SDH STS-192/10 Gig Ethernet CMOS Transceiver with ISI compensation
S19237	SONET/SDH STS-192/10 Gig Ethernet CMOS Transceiver with ISI compensation
S3390	OC-192 Transimpedance Amplifier
S3095	OC-192 Transimpedance with Automatic Gain Control

- Serial interface polarity swap (per input)
- 6 mm x 6 mm, 49 pin PBGA package with 0.8 mm pitch

**Applications**

- XFP MSA Modules
- 10 GbE and 10G FC Designs
- SONET/SDH Based Transmission Equipment
- SONET/SDH Test Equipment
- SONET/SDH/FEC DWDM Equipment

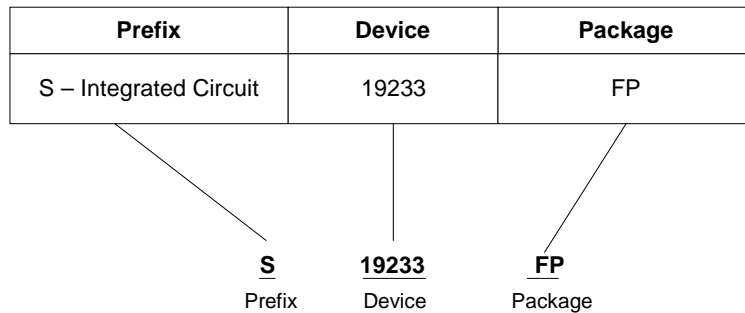


Figure 2. S19233 Ordering Information

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