## GENERAL DESCRIPTION

16–SOP–225

THE OUTLINE OF RDS(RADIO DATA SYSTEM)

Since 1988 most European national broadcaststations transmit RDS-code beside their audio signals. RDS means Radio Data System and was originally intended to give people in their cars additional information about the weather or traffic(jams). But RDS has grown out to one big channel of information. Radiostations send their name, the time (with DCF-77 accuracy), their type of music (format) and even more. The digital data of RDS are multiplexed into an FM radio wave using a sub-carrier of 57kHz. The transmission rate of RDS data is 1.1875kbit/sec.

The transmission rate of RDS data is 1.1875kbit/sec, and RDS data are encoded by differential encoding method. Then the encoded RDS data are modulated by BPSK using a clock of 1.1875kHz. The modulated RDS data is are modulated by carrier suppressed amplitude modulation using a sub-carrier of 57kHz. And that signal are multiplexed into an FM radio wave.

•RDS data are obtained by demodulating the received RDS modulation signal in RDS demodulator. First, the RDS modulation signal is extracted from an FM radio wave using a band pass filter. The BPSK signal is obtained from extracted RDS modulation signal by a 57kHz carrier recovery circuit. Then the bit rate clock of RDS data is extracted from the BPSK signal, and the BPSK signal is demodulated using the extracted clock signal. Then the RDS data are decoded by a differential decoding method using the demodulated BPSK signal.
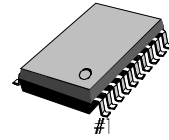
FEATURES

- Low Current

- Two Stage Anti-aliasing Filter

- 8'th 57kHz Switched Capacitor Bandpass Filter

- DSB Demodulation (Carrier Recovery)

- Clock Recovery Circuit

- Biphase Decoder & Differential Decoder

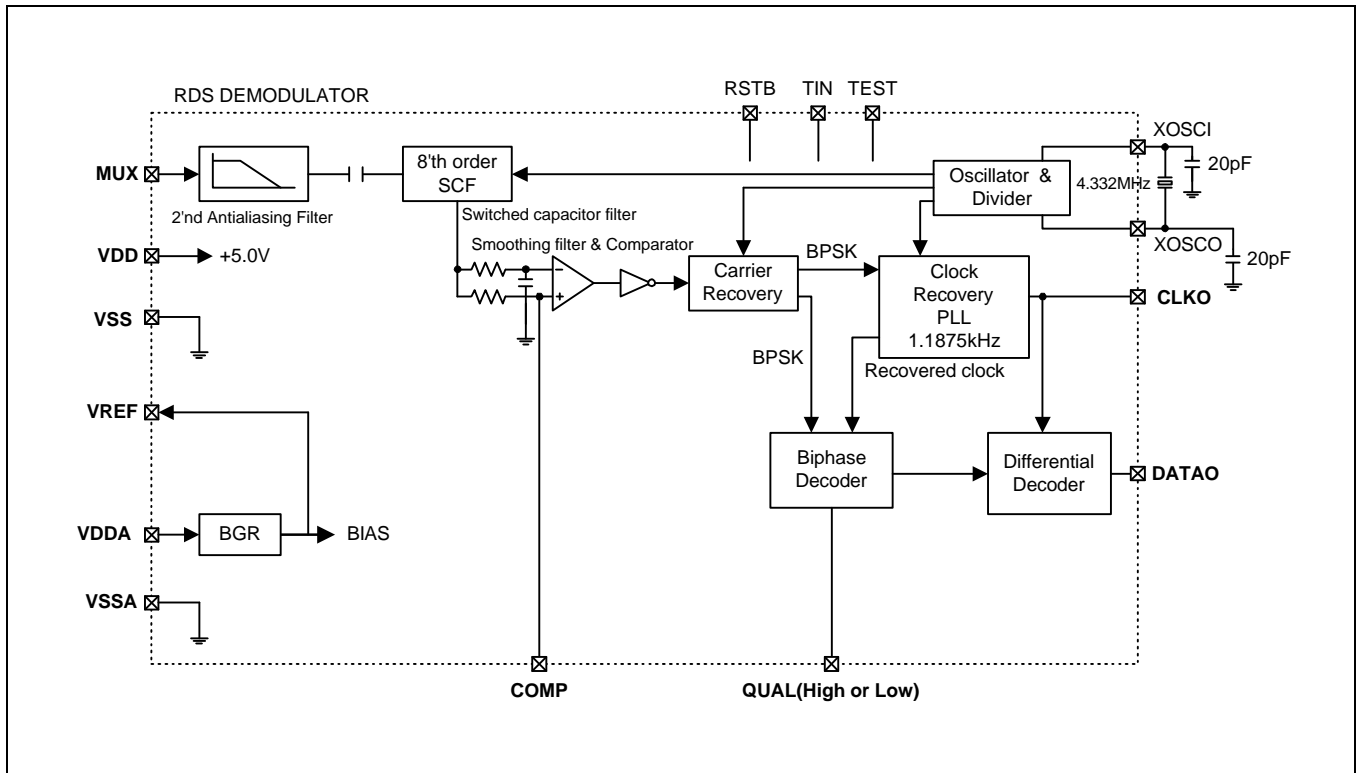- Quality Indication Output for Demodulated Data

ORDERING INFORMATION

DEVICE	PACKAGE	OPERATING TEMP.
S1A0905-S0B0	16-SOP-225	-40 − +85

DESCRIPTIONS

The S1A0905 is a RDS demodulator. It recovers the RDS data which is transmitted by FM radio broadcasting. The device operates in accordance with the EBU(European Broadcasting Union) specifications.

The IC includes a two stage antialiasing filter, a 57kHz switched capacitor bandpass filter, a comparator, a 57kHz carrier recovery circuit, a bit rate clock recovery circuit, BPSK decoder, differential decoding circuit, and RDS signal quality output.

BLOCK DIAGRAM

SAMSUNG
ELECTRONICS

PIN CONFIGURATION

16 SOP
(TOP VIEW)

```
         ┌───────────────┐
QUAL  [1]│ O             │[16] CLKO
DATAO [2]│               │[15] RSTB
VREF  [3]│      SEC      │[14] XOSCO
MUX   [4]│  S1A0905X01   │[13] XOSCI
VDDA  [5]│               │[12] VDD
VSSA  [6]│               │[11] VSS
SGND  [7]│               │[10] TIN
COMP  [8]│               │[9]  TEST
         └───────────────┘
```
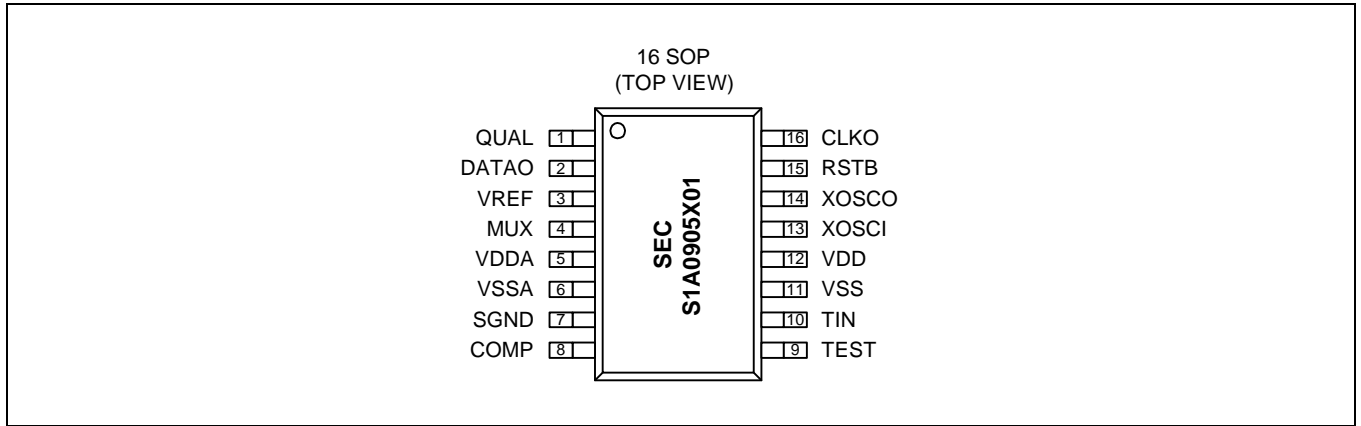
PIN DESCRIPTIONS

Pin	Name	I/O	Description
1	QUAL	O	Output for data quality indication (High = good data Low = bad data)
2	DATAO	O	RDS data output
3	VREF	O	System reference voltage output (2.5V)
4	MUX	I	Composite signal input
5	VDDA	P	Analog power (+5.0V)
6	VSSA	P	
7	SGND	P	System ground
8	COMP	O	Bandpass filter output
9	TEST	I	Test enable selecton pin (High = Test mode, Low = Normal mode)
10	TIN	I	Input signal for Test mode (Normally ground or open)
11	VSS	P	Digital power(+5.0V)
12	VDD	P	
13	XOSCI	I	Xtal oscillator input
14	XOSCO	O	Xtal oscillator output
15	RSTB	I	Input for system reset (High = active mode, Low = reset mode)
16	CLKO	O	RDS clock output (1187.5Hz)

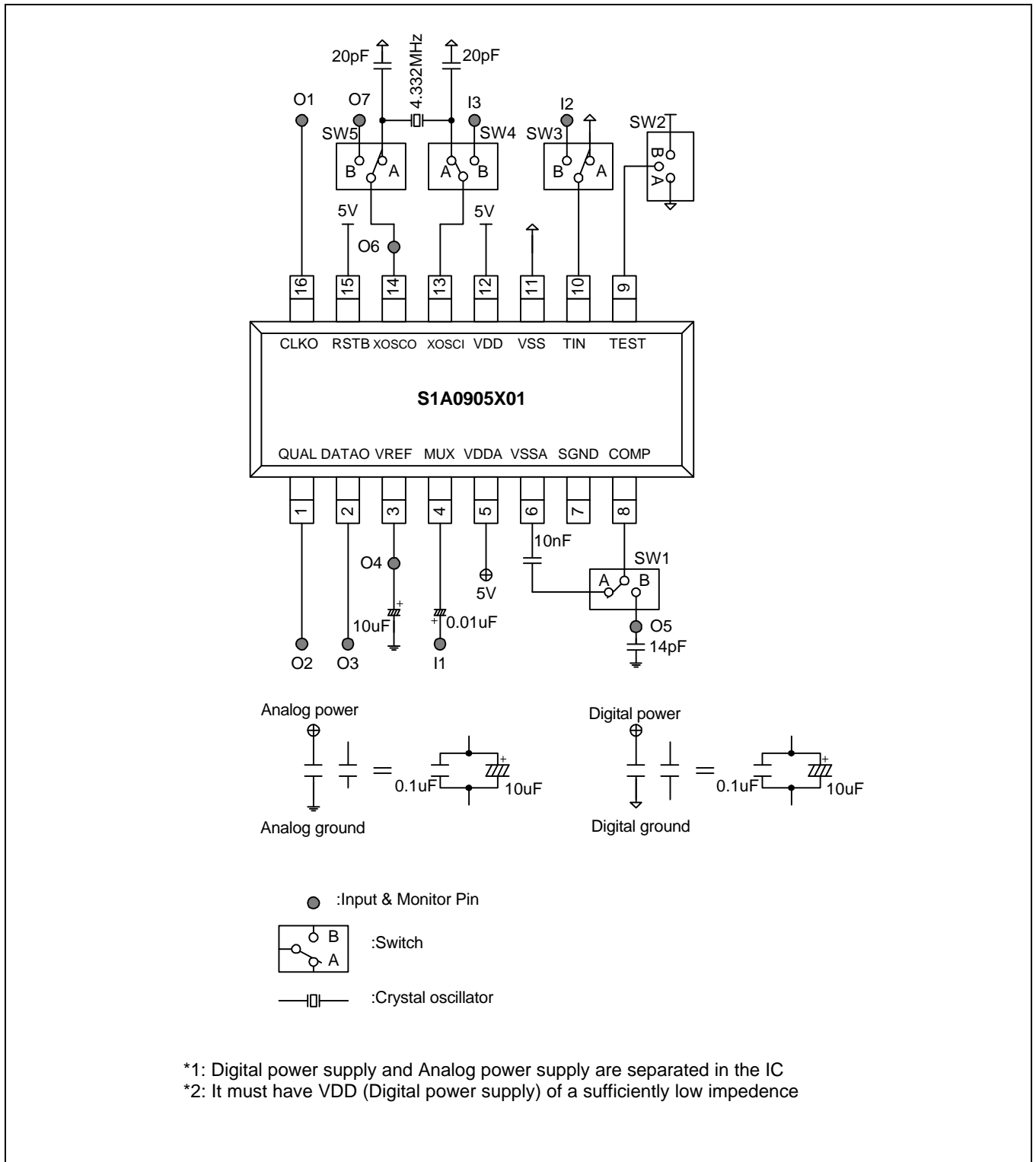I: Input pin, O: Output pin, P: Power pin

ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage1	VDDA	4.5	5.0	5.5	V	Analog power
Power supply voltage2	VDD	4.5	5.0	5.5	V	Digital power

Electrical Characteristics (VDDA = 5.0V, Ta = 25°C, fosc = 4.332MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating current	Isum	-	3.5	4.0	mA	i(VDDA)+i(VDD)
Reference voltage	VREF	2.4	2.5	2.6	V	
Ouput high level	Voh	VDDA-1.0	VDDA-0.3	-	V	CLKO,DATAO,QUAL
Output low level	Vol	-	0.2	1.0	V	CLKO,DATAO,QUAL
<Filter block>						
Center frequency	Fc	56.5	57	57.5	kHz	
Gain	GA	23	26	29	dB	Fc=57kHz, MUXFILO
Attenuation1	ATT1	-18	-22	-	dB	57.0kHz4kHz
Attenuation2	ATT2	-65	-80	-	dB	38kHz
Attenuation3	ATT3	-35	-50	-	dB	67kHz
S/N ratio	SN	30	40	-	dB	57kHz Vin=3mVrms
Input level	Vin	1	-	500	mVrms	
<Demodulator block>						
RDS detecter sensitivity	SRDS	-	0.5	1.0	mVrms	
RDS input level	VRDS	-	-	300	mVrms	
DATA rate	DRATE	-	1187.5	-	Hz	
Clock transient vs. DATA	CT	-	4.3	-	us	
Lockup time(RDS)	TL	-	100	200	ms	
<Oscillator block>						
XTAL frequency	Fosc	-	4.332	-	MHz	
Clock input high level	Xosci	4.0	-	-	V	
Clock input low level	Xosco	-	-	1.0	V	
Output Amplitude	Xosc	-	4.5	-	Vpp	
Load capacitance	CL	-	20	-	pF	

SAMSUNG
ELECTRONICS

TEST APPLICATION

*1: Digital power supply and Analog power supply are separated in the IC
*2: It must have VDD (Digital power supply) of a sufficiently low impedence

NOTES