EPSON

S1C63567

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Original Architecture Core CPU
- Low Current Consumption
- Wide-range Operating Voltage (2.2V to 5.5V)
- High Speed Operation in Low Voltage (0.56µsec/3.58MHz)

■ DESCRIPTION

The S1C63567 is a microcomputer which has a high-performance 4-bit CPU S1C63000 as the core CPU, ROM (16,384 words × 13 bits), RAM (5,120 words × 4 bits), serial interface, watchdog timer, programmable timer, time base counters (2 systems), SVD circuit, a dot-matrix LCD driver that can drive a maximum 60 segments × 17 commons, DTMF/DP generator and sound generator built-in. The S1C63567 features high speed operation and low current consumption in an operating voltage range (2.2 V to 5.5 V), this makes it suitable for applications working with batteries. It is also suitable for caller ID and portable data bank systems because it has a large capacity of RAM built-in.

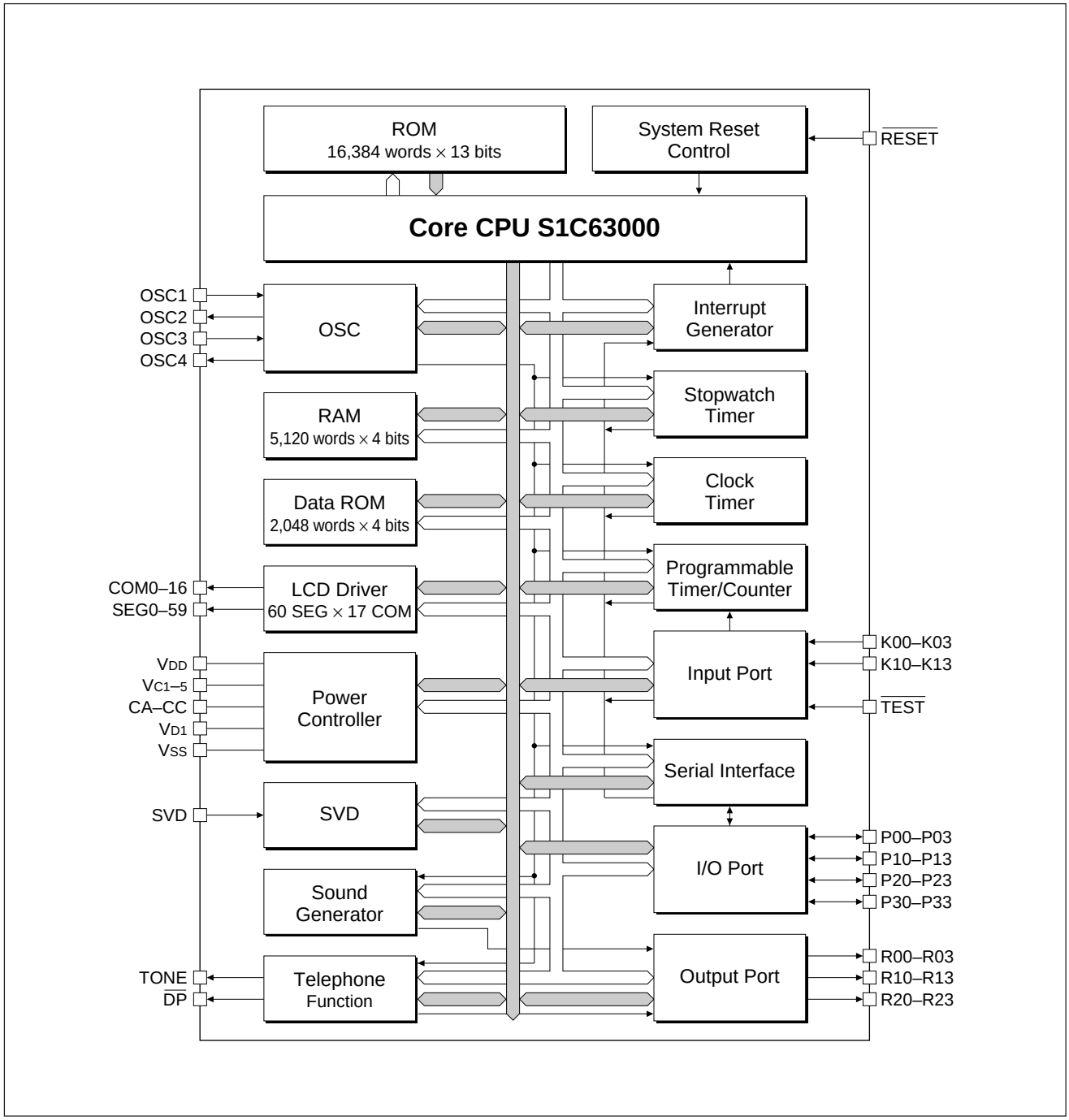
■ FEATURES

- OSC1 oscillation circuit ..... 32.768 kHz (Typ.) crystal or 60 kHz (Typ.) CR oscillation circuit (∗1)
- OSC3 oscillation circuit ..... 3.58 MHz (Typ.) ceramic or 1.8 MHz (Typ.) CR oscillation circuit (∗1)
- Instruction set ..... Basic instruction: 46 types (411 instructions with all)
  Addressing mode: 8 types
- Instruction execution time ..... During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec
  During operation at 3.58 MHz: 0.56 µsec 1.12 µsec 1.68 µsec
- ROM capacity ..... Code ROM: 16,384 words × 13 bits
  Data ROM: 2,048 words × 4 bits (= 8K bits)
- RAM capacity ..... Data memory: 5,120 words × 4 bits
  Display memory: 1,020 bits (240 words × 4 bits + 60 × 1 bit)
- Input port ..... 8 bits (Pull-up resistors may be supplemented ∗1)
- Output port ..... 12 bits (It is possible to switch the 8 bits to special output ∗2)
- I/O port ..... 16 bits (It is possible to switch the 2 bits to special output and the 4 bits to serial I/F input/output ∗2)
- Serial interface ..... Built-in (8-bit clock synchronous or asynchronous system is selectable)
- LCD driver ..... 60 segments × 8, 16 or 17 commons (∗2)
- Time base counter ..... 2 systems (Clock timer, stopwatch timer)
- Programmable timer ..... Built-in, 2 inputs × 8 bits, with event counter function
- Watchdog timer ..... Built-in
- DTMF generator ..... Built-in
- DP generator ..... Built-in
- Sound generator ..... With envelope and 1-shot output functions
- Supply voltage detection (SVD) circuit ... 12 values, programmable (2.20 V to 3.30 V)
  (It is possible to switch 1 value to the external voltage detection ∗1)
- External interrupt ..... Input port interrupt: 2 systems
- Internal interrupt ..... Clock timer interrupt: 4 systems
  Stopwatch timer interrupt: 2 systems
  Programmable timer interrupt: 2 systems
  Serial interface interrupt: 3 systems
  Dialer interrupt: 1 system
- Power supply voltage ..... 2.2 V to 5.5 V

- Operating temperature range ..... -20°C to 70°C
- Current consumption (Typ.) ..... Low-speed operation (OSC1: crystal oscillation):
  - During HALT (32 kHz) 3.0 V (LCD power OFF) 1.5 µA
  - 3.0 V (LCD power ON) 4 µA
  - During operation (32 kHz) 3.0 V (LCD power ON) 10 µA
  - High-speed operation (OSC3: ceramic oscillation):
  - During operation (3.58 MHz) 3.0 V (LCD power ON) 600 µA
- Package ..... QFP8-144pin (plastic) or chip

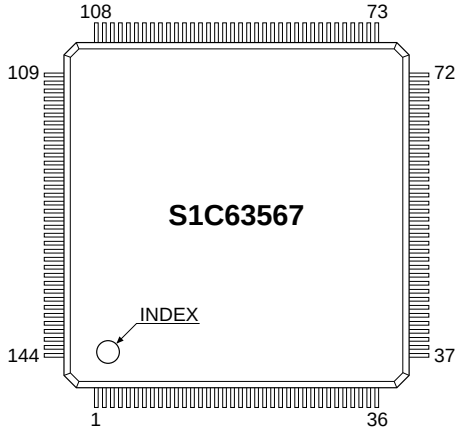
∗1: Can be selected with mask option ∗2: Can be selected with software

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP8-144pin



No.	Name	No.	Name	No.	Name	No.	Name
1	N.C.	37	N.C.	73	N.C.	109	N.C.
2	SEG16	38	N.C.	74	K11	110	N.C.
3	SEG15	39	$\overline{DP}$	75	K10	111	N.C.
4	SEG14	40	R23	76	K03	112	SEG47
5	SEG13	41	R22	77	K02	113	SEG46
6	SEG12	42	R21	78	K01	114	SEG45
7	SEG11	43	R20	79	K00	115	SEG44
8	SEG10	44	R13	80	SVD	116	SEG43
9	SEG9	45	R12	81	V_{C1}	117	SEG42
10	SEG8	46	R11	82	V_{C23}	118	SEG41
11	SEG7	47	R10	83	V_{C4}	119	SEG40
12	SEG6	48	R03	84	V_{C5}	120	SEG39
13	SEG5	49	R02	85	CC	121	SEG38
14	SEG4	50	R01	86	CB	122	SEG37
15	SEG3	51	R00	87	CA	123	SEG36
16	SEG2	52	P33	88	COM8	124	SEG35
17	SEG1	53	P32	89	COM9	125	SEG34
18	SEG0	54	P31	90	COM10	126	SEG33
19	COM7	55	P30	91	COM11	127	SEG32
20	COM6	56	P23	92	COM12	128	SEG31
21	COM5	57	P22	93	COM13	129	SEG30
22	COM4	58	P21	94	COM14	130	SEG29
23	COM3	59	P20	95	COM15	131	SEG28
24	COM2	60	P13	96	COM16	132	SEG27
25	COM1	61	P12	97	SEG59	133	SEG26
26	COM0	62	P11	98	SEG58	134	SEG25
27	V_{SS}	63	P10	99	SEG57	135	SEG24
28	OSC1	64	P03	100	SEG56	136	SEG23
29	OSC2	65	P02	101	SEG55	137	SEG22
30	V_{D1}	66	P01	102	SEG54	138	SEG21
31	OSC3	67	P00	103	SEG53	139	SEG20
32	OSC4	68	K13	104	SEG52	140	SEG19
33	V_{DD}	69	K12	105	SEG51	141	SEG18
34	$\overline{RESET}$	70	N.C.	106	SEG50	142	SEG17
35	$\overline{TEST}$	71	N.C.	107	SEG49	143	N.C.
36	TONE	72	N.C.	108	SEG48	144	N.C.

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	I/O	Function
V_{DD}	33	–	Power (+) supply pin
V_{SS}	27	–	Power (–) supply pin
V_{D1}	30	–	Oscillation system regulated voltage output pin
V_{C1}–V_{C5}	81–84	–	LCD system power supply pin (1/4 bias generated internally)
CA–CC	87–85	–	LCD system boosting/reducing capacitor connecting pin
OSC1	28	I	Crystal oscillation input pin
OSC2	29	O	Crystal oscillation output pin
OSC3	31	I	Ceramic oscillation input pin
OSC4	32	O	Ceramic oscillation output pin
K00–K03	79–76	I	Input port
K10–K13	75, 74, 69, 68	I	Input port
P00–P03	67–64	I/O	I/O port
P10–P13	63–60	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20	59	I/O	I/O port
P21	58	I/O	I/O port
P22	57	I/O	I/O port (switching to CL signal output is possible by software)
P23	56	I/O	I/O port (switching to FR signal output is possible by software)
P30–P33	55–52	I/O	I/O port
R00	51	O	Output port (switching to XBZ signal output is possible by software)
R01	50	O	Output port (switching to BZ signal output is possible by software)
R02	49	O	Output port (switching to TOUT signal output is possible by software)
R03	48	O	Output port (switching to FOUT signal output is possible by software)
R10	47	O	Output port (switching to XTMUTE signal output is possible by software)
R11	46	O	Output port (switching to XRMUTE signal output is possible by software)
R12	45	O	Output port (switching to HDO signal output is possible by software)
R13	44	O	Output port (switching to HFO signal output is possible by software)
R20–R23	43–40	O	Output port
COM0–COM16	26–19, 88–96	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
SEG0–SEG59	18–2, 142–112, 108–97	O	LCD segment output pin
SVD	80	I	SVD external voltage input pin
$\overline{DP}$	39	O	Dial pulse output pin
TONE	36	O	DTMF output pin
$\overline{RESET}$	34	I	Initial reset input pin
$\overline{TEST}$	35	I	Testing input pin

■ OPTION LIST

1 OSC1 SYSTEM CLOCK
- ☐ 1. Crystal
- ☐ 2. CR

2 OSC3 SYSTEM CLOCK
- ☐ 1. Ceramic
- ☐ 2. CR

3 MULTIPLE KEY ENTRY RESET COMBINATION
- ☐ 1. Not Use
- ☐ 2. Use (K00, K01, K02, K03)
- ☐ 3. Use (K00, K01, K02)
- ☐ 4. Use (K00, K01)

4 MULTIPLE KEY ENTRY RESET TIME AUTHORIZE
- ☐ 1. Not Use
- ☐ 2. Use

5 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• K11	☐ 1. With Resistor	☐ 2. Gate Direct
• K12	☐ 1. With Resistor	☐ 2. Gate Direct
• K13	☐ 1. With Resistor	☐ 2. Gate Direct

6 OUTPUT PORT OUTPUT SPECIFICATION

• R00	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R01	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R02	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R03	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R10	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R11	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R12	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R13	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R20	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R21	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R22	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R23	☐ 1. Complementary	☐ 2. Nch-OpenDrain

7 I/O PORT OUTPUT SPECIFICATION

• P00	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P01	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P02	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P03	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P10	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P11	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P12	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P13	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P20	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P21	☐ 1. Complementary	☐ 2. Nch-OpenDrain

- P22 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P23 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P30 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P31 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P32 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P33 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain

8 I/O PORT PULL UP RESISTOR

- P0x ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P1x ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P20 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P21 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P22 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P23 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P3x ..... ☐ 1. With Resistor ☐ 2. Gate Direct

9 DP PORT OUTPUT SPECIFICATION

☐ 1. Complementary
☐ 2. Nch-OpenDrain

10 SVD EXTERNAL VOLTAGE DETECTION

☐ 1. Not Use
☐ 2. Use

11 DTMF "DTS"

☐ 1. Not Use
☐ 2. Use

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package (QFP8-144pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	2.2	3.0	5.5	V
Oscillation frequency	f_{OSC1}	Crystal oscillation	–	32.768	–	kHz
		CR oscillation	40	60	80	kHz
	f_{OSC3}	CR oscillation		1,800	2,250	kHz
		Ceramic oscillation	–	3.58	–	MHz
SVD terminal input voltage	SVD	SVD≤V_{DD}, V_{SS}=0V	0		5.5	V

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C23}/V_{C4}/V_{C5} are internal voltage, C_1–C_7=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23, P30–33	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		P00–03, P10–13, P20–23, P30–33	0		0.4	V
Low level input voltage (3)	V_{IL3}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-16	-10	-6	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R02, R03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33			-0.6	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	R00, R01			-0.6	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R02, R03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33	1.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	R00, R01	1.5			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C23}/V_{C4}/V_{C5} are internal voltage, C_1–C_7=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23, P30–33	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		P00–03, P10–13, P20–23, P30–33	0		0.4	V
Low level input voltage (3)	V_{IL3}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=5.0V	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-25	-15	-10	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R02, R03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	R00, R01			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R02, R03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33	3.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	R00, R01	3.5			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C23}/V_{C4}/V_{C5} are internal voltage, C_1–C_7=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2·V_{C23} -0.1		1/2·V_{C23} ×0.95	V
	V_{C23}	Connect 1 MΩ load resistor between V_{SS} and V_{C23} (without panel load)	LC0–3="0"		1.95		
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"	Typ.	2.16	Typ.	V
			LC0–3="8"	×0.88	2.19	×1.12	
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		3/2·V_{C23} ×0.95		3/2·V_{C23}	V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)		2·V_{C23} ×0.95		2·V_{C23}	V
SVD voltage (Ta=25°C)	V_{SVD1}	SVDS0–3="0" (internal)			2.20		
		SVDS0–3="1"			2.20		
		SVDS0–3="2"			2.20		
		SVDS0–3="3"			2.20		
		SVDS0–3="4"			2.20		
		SVDS0–3="5"			2.30		
		SVDS0–3="6"			2.40		
		SVDS0–3="7"		Typ.	2.50	Typ.	V
		SVDS0–3="8"		×0.93	2.60	×1.07	
		SVDS0–3="9"			2.70		
		SVDS0–3="10"			2.80		
		SVDS0–3="11"			2.90		
		SVDS0–3="12"			3.00		
		SVDS0–3="13"			3.10		
		SVDS0–3="14"			3.20		
		SVDS0–3="15"			3.30		
SVD voltage (external) *3	V_{SVD2}	SVDS0–3="0" (external), Ta = 25°C		0.85	0.95	1.05	V
SVD circuit response time	t_{SVD}	Ta = 25°C				100	µS
Current consumption (Ta=25°C)	I_{OP}	During HALT (32 kHz crystal oscillation)	LCD power OFF *1, *2		1.5	3	µA
			LCD power ON *1, *2		4	8	µA
		During execution (32 kHz crystal oscillation)	LCD power ON *1, *2		10	19	µA
		During execution 60 kHz CR oscillation)	LCD power ON *1, *2		45	80	µA
		During execution (1,800 kHz CR oscillation)	LCD power ON *1		800	1,000	µA
		During HALT (3.58 MHz ceramic oscillation)	LCD power ON *1		150	300	µA
		During execution (3.58 MHz ceramic oscillation)	LCD power ON *1		600	800	µA
		SVD circuit current (during supply voltage detection) V_{DD}=2.2 to 5.5 V		1		15	µA
		SVD circuit current (during external voltage detection) V_{DD}=2.2 to 5.5 V		0.5		6	µA

*1: Without panel load. The SVD circuit is OFF.

*2: OSCC = "0"

*3: Please input the voltage, which is within the range between V_{SS} and V_{DD}, into the SVD terminal.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})	2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	Δf/ΔV	V_{DD}=2.2 to 5.5V			10	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	10	20		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})	5.5			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}	200			MΩ

OSC1 CR Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR1}=600kΩ, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	60kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 5.5V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 3.58MHz, C_{GC}=C_{DC}=30pF, Ta=-20 to 70°C)

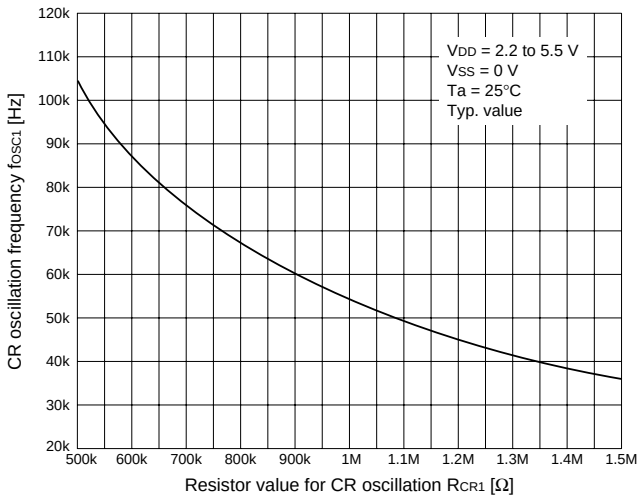
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 5.5V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 CR Oscillation Circuit

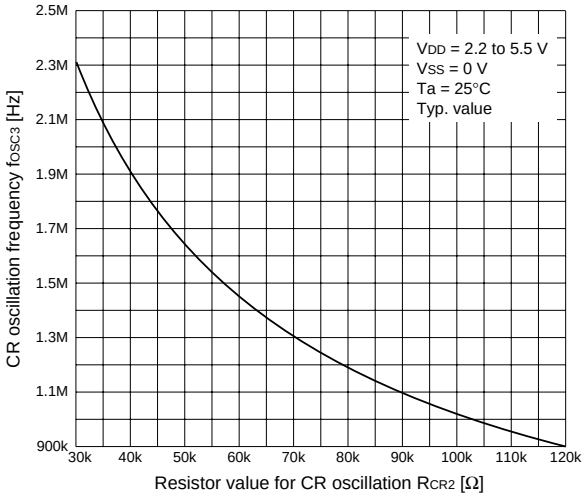
(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR2}=47kΩ, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-25	1,800kHz	25	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 5.5V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

- **OSC1 CR oscillation frequency-resistance characteristic**



- **OSC3 CR oscillation frequency-resistance characteristic**



● Serial Interface AC Characteristics

Clock Synchronous Master Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

Clock Synchronous Slave Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

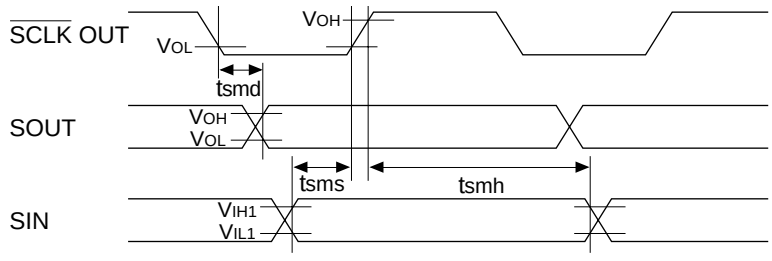
• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

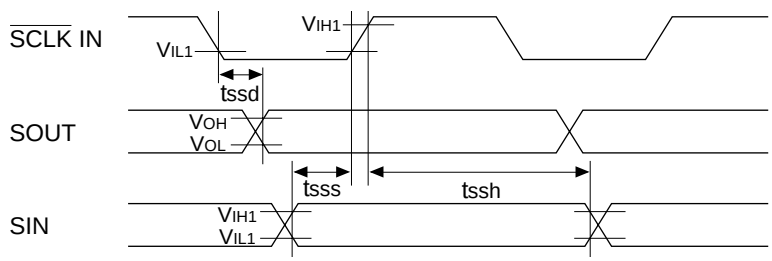
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>



<Slave mode>



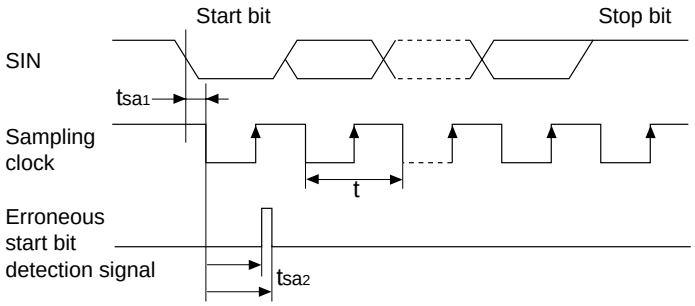
Asynchronous System

(Condition: V_{DD}=2.2 to 5.5V, V_{SS}=0V, Ta=-20 to 70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Start bit detection error time *1	t_{sa1}	0		t/16	S
Erroneous start bit detection range time *2	t_{sa2}	9t/16		10t/16	S

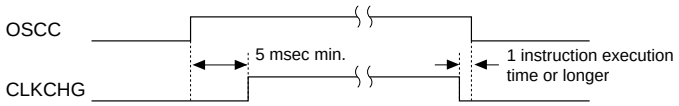
*1: Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

*2: Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started. When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)



● Timing Chart

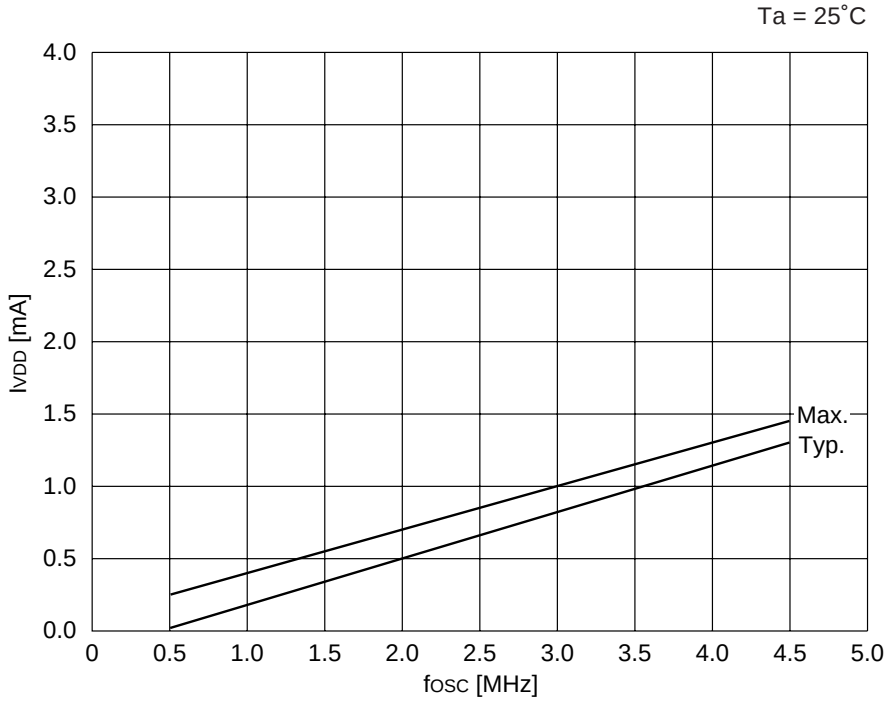
System clock switching



● Characteristic Curves (reference value)

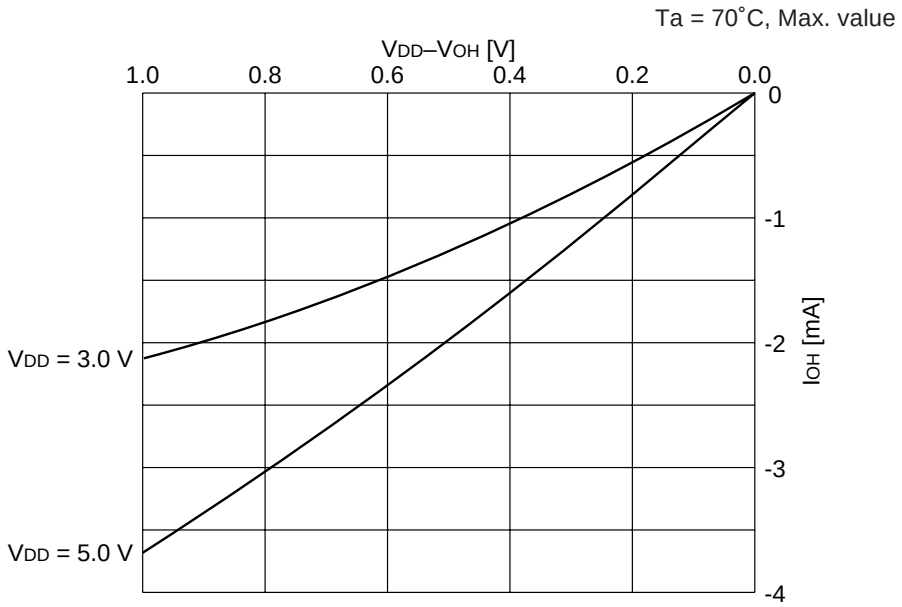
Power current - frequency characteristics

• Ceramic oscillation (during operation)

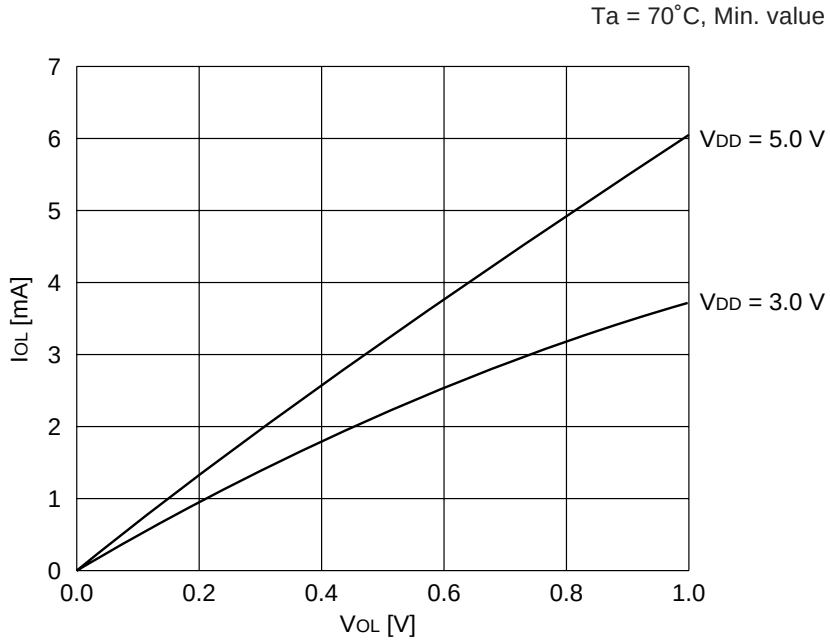


Output current characteristics

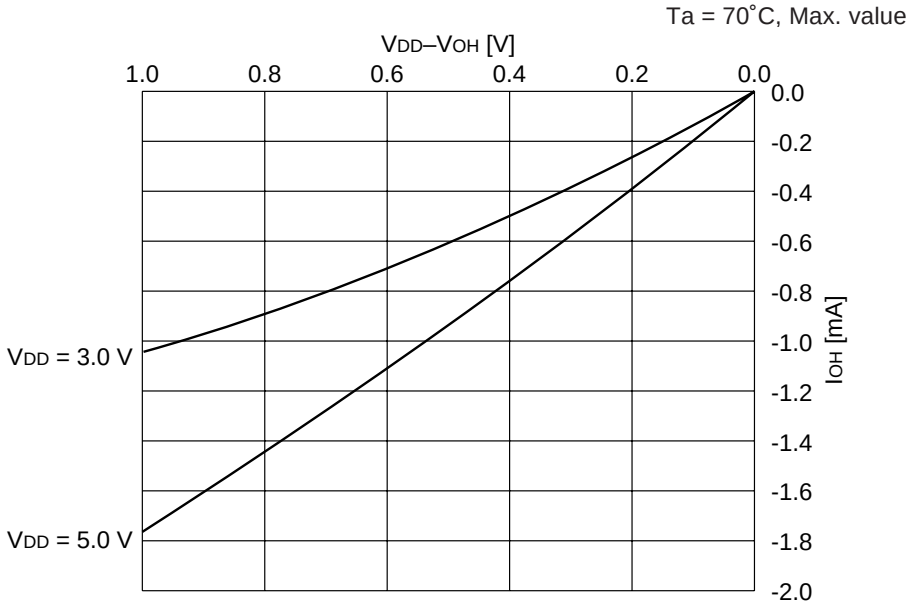
• High level output current (Pxx, Rxx, BZ)



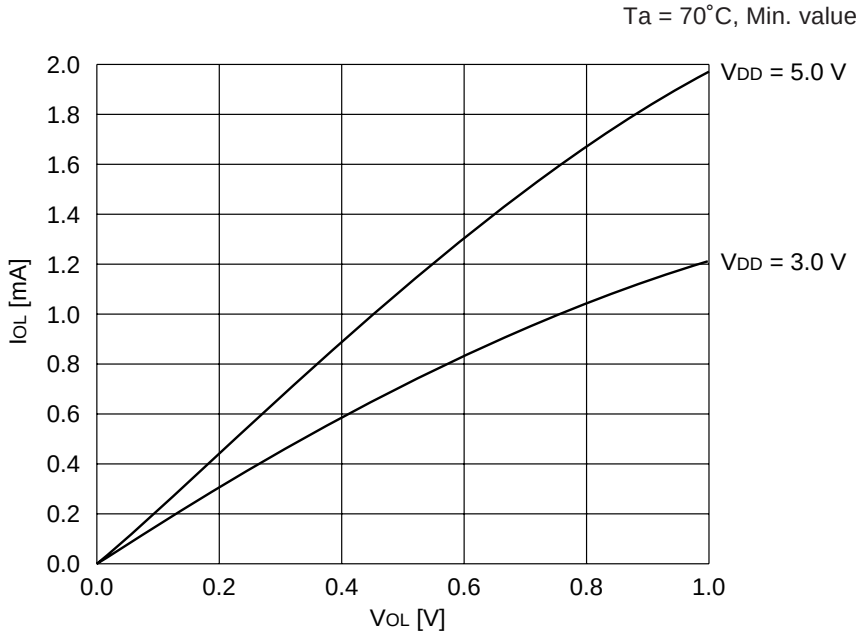
• Low level output current (Pxx, Rxx, BZ)



• **High level output current (SEGxx)**

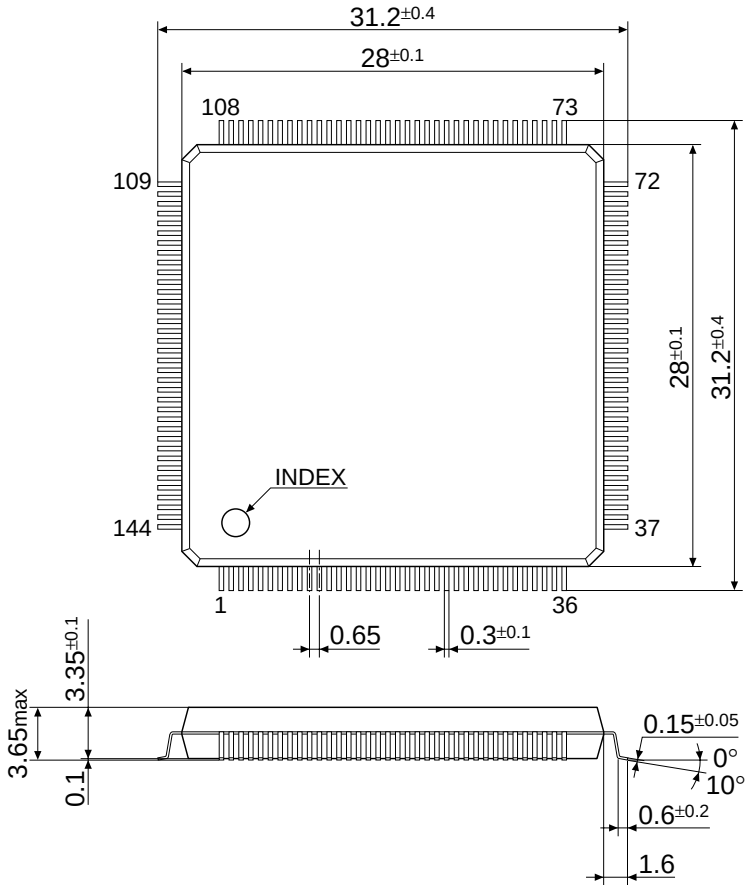


• **Low level output current (SEGxx)**



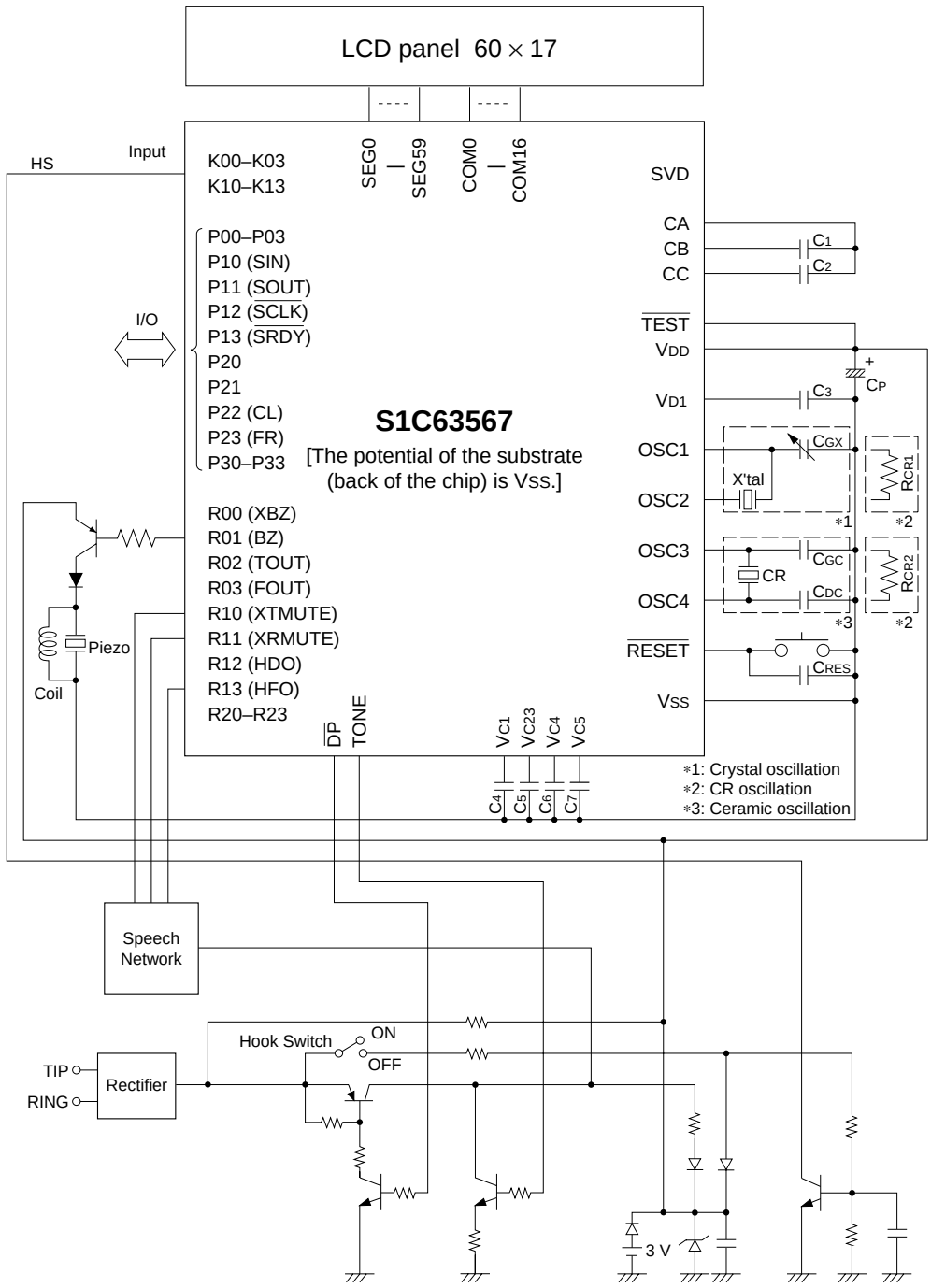
■ PACKAGE DIMENSIONS

Plastic QFP8-144pin



Unit: mm

■ BASIC EXTERNAL CONNECTION DIAGRAM

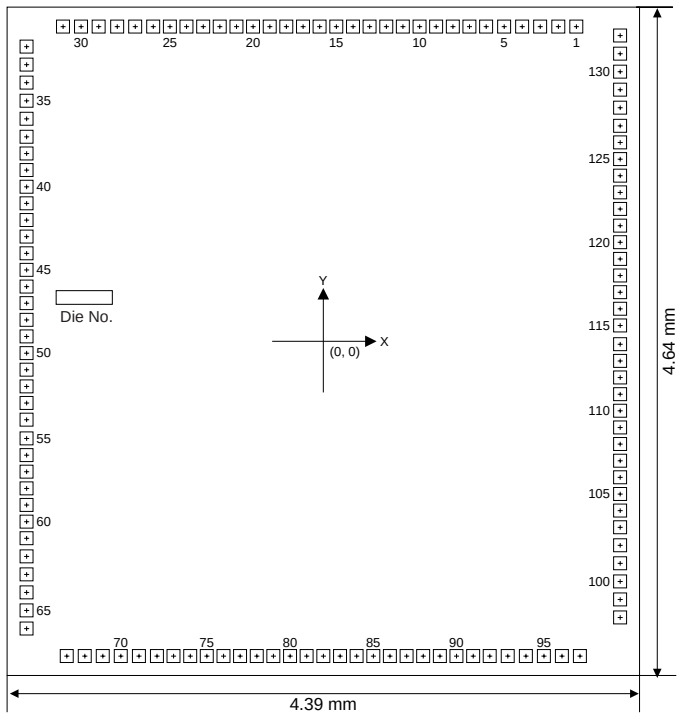


X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
RCR1	Resistor for OSC1 CR oscillation	600 kΩ (60 kHz)
CR	Ceramic oscillator	3.58 MHz (3.0 V)
CGC	Gate capacitor	30 pF
CDC	Drain capacitor	30 pF
RCR2	Resistor for OSC3 CR oscillation	47 kΩ (1.8 MHz)
C1–C7	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	$\overline{\text{RESET}}$ terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

■ PAD LAYOUT

● Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 100 µm

● Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	$\overline{DP}$	1756	2185	32	K11	-2060	2046	67	SEG47	-1781	-2185	98	SEG16	2060	-1917
2	R23	1631	2185	33	K10	-2060	1921	68	SEG46	-1656	-2185	99	SEG15	2060	-1792
3	R22	1505	2185	34	K03	-2060	1796	69	SEG45	-1531	-2185	100	SEG14	2060	-1667
4	R21	1380	2185	35	K02	-2060	1670	70	SEG44	-1406	-2185	101	SEG13	2060	-1541
5	R20	1255	2185	36	K01	-2060	1545	71	SEG43	-1280	-2185	102	SEG12	2060	-1416
6	R13	1130	2185	37	K00	-2060	1420	72	SEG42	-1155	-2185	103	SEG11	2060	-1291
7	R12	1014	2185	38	SVD	-2060	1304	73	SEG41	-1040	-2185	104	SEG10	2060	-1175
8	R11	899	2185	39	V_{C1}	-2060	1189	74	SEG40	-924	-2185	105	SEG09	2060	-1060
9	R10	783	2185	40	V_{C23}	-2060	1073	75	SEG39	-809	-2185	106	SEG08	2060	-944
10	R03	668	2185	41	V_{C4}	-2060	958	76	SEG38	-693	-2185	107	SEG07	2060	-829
11	R02	552	2185	42	V_{C5}	-2060	842	77	SEG37	-578	-2185	108	SEG06	2060	-713
12	R01	437	2185	43	CC	-2060	727	78	SEG36	-462	-2185	109	SEG05	2060	-598
13	R00	321	2185	44	CB	-2060	611	79	SEG35	-347	-2185	110	SEG04	2060	-482
14	P33	206	2185	45	CA	-2060	496	80	SEG34	-231	-2185	111	SEG03	2060	-367
15	P32	90	2185	46	COM8	-2060	380	81	SEG33	-116	-2185	112	SEG02	2060	-251
16	P31	-26	2185	47	COM9	-2060	265	82	SEG32	0	-2185	113	SEG01	2060	-136
17	P30	-141	2185	48	COM10	-2060	149	83	SEG31	116	-2185	114	SEG00	2060	-20
18	P23	-257	2185	49	COM11	-2060	34	84	SEG30	231	-2185	115	COM7	2060	110
19	P22	-372	2185	50	COM12	-2060	-82	85	SEG29	347	-2185	116	COM6	2060	226
20	P21	-488	2185	51	COM13	-2060	-197	86	SEG28	462	-2185	117	COM5	2060	341
21	P20	-603	2185	52	COM14	-2060	-313	87	SEG27	578	-2185	118	COM4	2060	457
22	P13	-719	2185	53	COM15	-2060	-428	88	SEG26	693	-2185	119	COM3	2060	572
23	P12	-834	2185	54	COM16	-2060	-544	89	SEG25	809	-2185	120	COM2	2060	688
24	P11	-950	2185	55	SEG59	-2060	-674	90	SEG24	924	-2185	121	COM1	2060	803
25	P10	-1065	2185	56	SEG58	-2060	-790	91	SEG23	1040	-2185	122	COM0	2060	919
26	P03	-1181	2185	57	SEG57	-2060	-905	92	SEG22	1155	-2185	123	V_{SS}	2060	1034
27	P02	-1306	2185	58	SEG56	-2060	-1021	93	SEG21	1280	-2185	124	OSC1	2060	1150
28	P01	-1431	2185	59	SEG55	-2060	-1136	94	SEG20	1406	-2185	125	OSC2	2060	1265
29	P00	-1556	2185	60	SEG54	-2060	-1252	95	SEG19	1531	-2185	126	V_{D1}	2060	1381
30	K13	-1682	2185	61	SEG53	-2060	-1367	96	SEG18	1656	-2185	127	OSC3	2060	1496
31	K12	-1807	2185	62	SEG52	-2060	-1493	97	SEG17	1781	-2185	128	OSC4	2060	1622
				63	SEG51	-2060	-1618					129	V_{DD}	2060	1747
				64	SEG50	-2060	-1743					130	$\overline{RESET}$	2060	1872
				65	SEG49	-2060	-1868					131	$\overline{TEST}$	2060	1997
				66	SEG48	-2060	-1994					132	TONE	2060	2123

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