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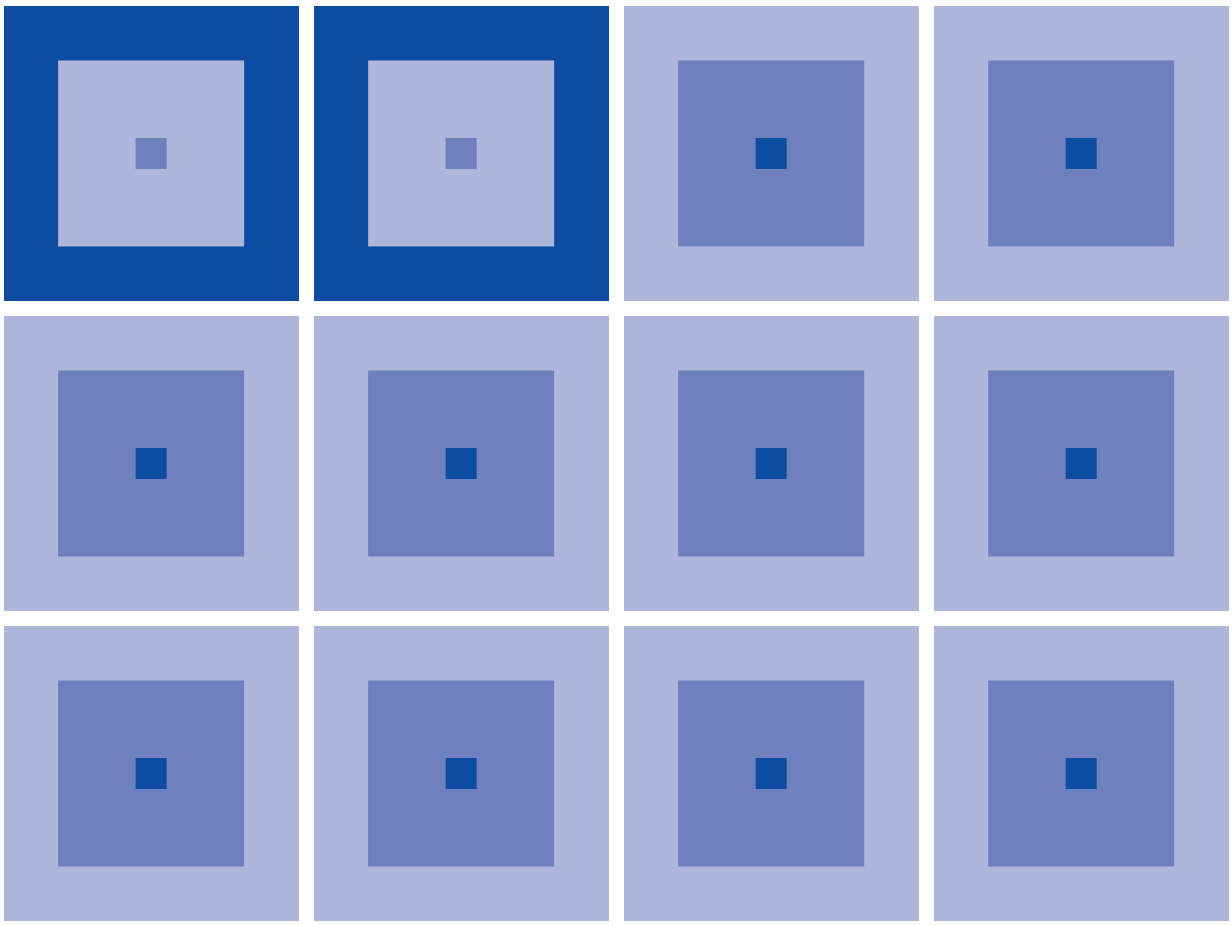
CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

S1C8F626

Technical Manual



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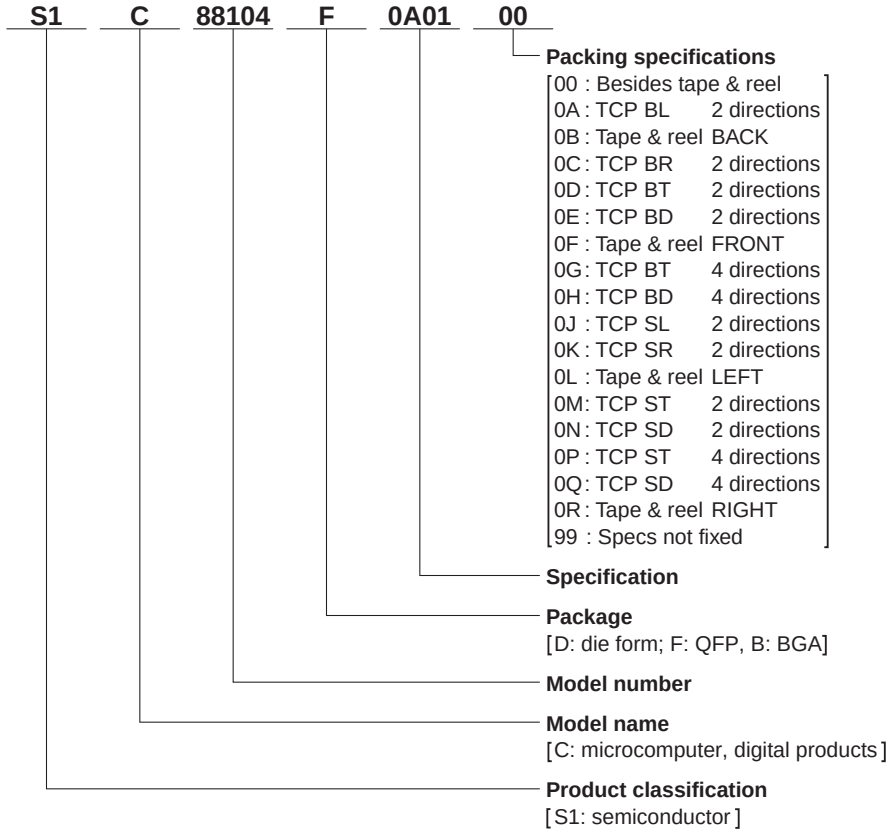
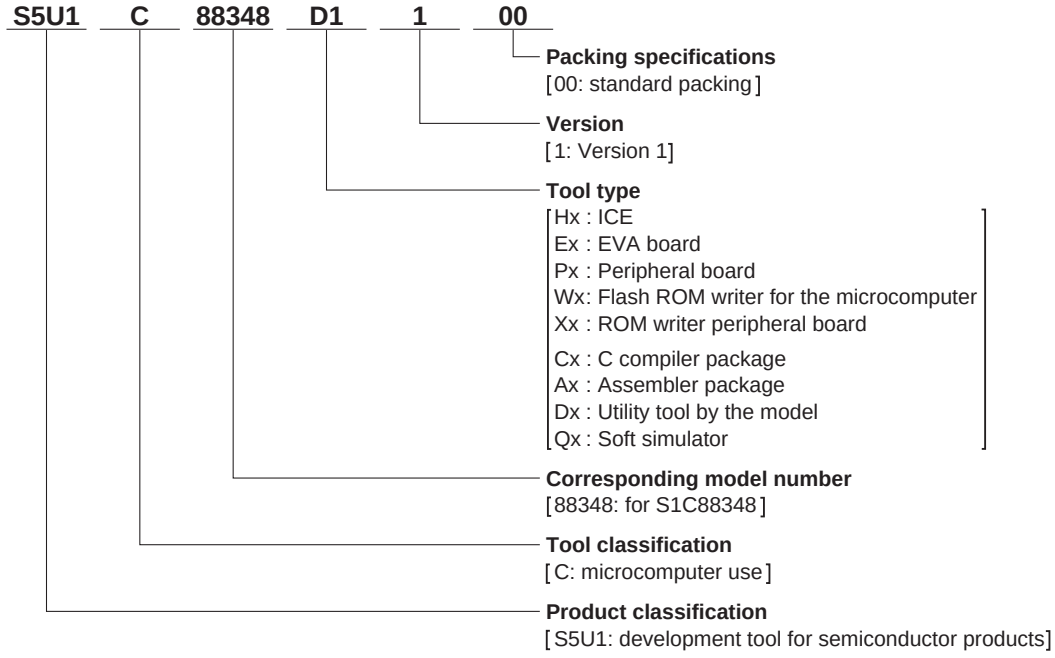
Configuration of product number

Devices



Development tools



Contents

1 INTRODUCTION

The S1C8F626 is a microcomputer which has a built-in 8-bit CPU S1C88 (MODEL3) as the core CPU, 48K-byte and 192K-byte Flash EEPROMs, 8K-byte RAM, 16-bit programmable timers (PWM), serial interface, watchdog timer, stopwatch timer, an LCD driver that can drive a maximum 96 segments × 32 commons and a supply voltage detection circuit.
This microcomputer features low-voltage (1.8 V) and high-speed (8.2 MHz) operations as well as low-current consumption (2.5 µA in HALT mode).
Furthermore, the S1C8F626 allows the user to program (erase, program, verify) the internal ROM even if it is mounted on the target board. The S1C8F626 Flash EEPROM can be used for storing a 11 × 12-dot kanji font data that contains JIS level-1 and level-2 kanji sets, other characters and user-defined characters, this makes it possible to display kanji characters without any external kanji font ROM (refer to Appendix B, "USING KANJI FONT").
The S1C8F626 is suitable for various battery driven controllers.

1.1 Features

Table 1.1.1 lists the features of the S1C8F626.

Table 1.1.1 Main features

Core CPU	S1C88 (MODEL3) CMOS 8-bit core CPU
Main (OSC3) oscillation circuit	Crystal oscillation circuit/ceramic oscillation circuit 8.2 MHz (Max.), or CR oscillation circuit 2.2 MHz (Max.)
Sub (OSC1) oscillation circuit	Crystal oscillation circuit 32.768 kHz (Typ.)
Instruction set	608 types (usable for multiplication and division instructions)
Min. instruction execution time	0.244 µsec/8.2 MHz (2 clock)
Internal ROM capacity (Flash EEPROM)	48K bytes: Program ROM 192K bytes: Program and data (font) ROM Can be programmed using the On Board Writer. (Supports various security settings.) Supports self-programming by the user program.
Internal RAM capacity	8K bytes: RAM 576 bytes: Display memory (4608 bits/display area × 2)
Input port	8 bits (4 bits can be used as the source clock inputs for PWM timers.)
I/O port	24 bits (Shard with serial interface, FOUT and TOUT terminals.)
Serial interface	2 ch (Supports clock synchronous system, asynchronous system and IrDA1.0 interface.)
Timer	Programmable timer: 16 bits (8 bits × 2) 4 ch (with PWM function) Clock timer: 1 ch Stopwatch timer: 1 ch
LCD driver	Dot matrix type (supports 16 × 16/5 × 8 or 12 × 12 dot font) 96 segments × 32, 16 or 8 commons (1/5 bias) Built-in LCD power supply circuit (booster type, 5 potentials)
Watchdog timer	Built-in
Supply voltage detection (SVD) circuit	13 value programmable (1.8–2.7 V)
Interrupt	External interrupt: Input interrupt 1 system (8 types) Internal interrupt: Timer interrupt 6 systems (23 types) Serial interface interrupt 2 systems (6 types)
Supply voltage	1.8–3.6 V (for running, internal operating voltage V_{D1} = 1.8 V) 2.7–3.6 V (for Flash programming, internal operating voltage V_{D1} = 2.5 V)
Current consumption	SLEEP mode: 1 µA (Typ.) HALT mode: 2.5 µA (Typ.) 32 kHz crystal, LCD OFF 7.5 µA (Typ.) 32 kHz crystal, LCD ON*, V_{DD} = 2.5–3.6 V Run state: 10 µA (Typ.) 32 kHz crystal, LCD OFF 1.8 mA (Typ.) 8 MHz ceramic, LCD OFF 700 µA (Typ.) 2 MHz CR, LCD OFF 15 µA (Typ.) 32 kHz crystal, LCD ON*, V_{DD} = 2.5–3.6 V 28 µA (Typ.) 32 kHz crystal, LCD ON*, V_{DD} = 1.8–2.5 V, Power voltage booster ON 15 µA (Typ.) 32 kHz crystal, SVD ON
Supply form	Chip, VFBGA10H-240pin or QFP21-216pin package

* The current consumption with LCD ON listed above is the value under the conditions of LCDCx = "11 (all on)", LCx = "0FH" and "No panel load". Current consumption increases according to the display contents and panel load.

1.2 Block Diagram

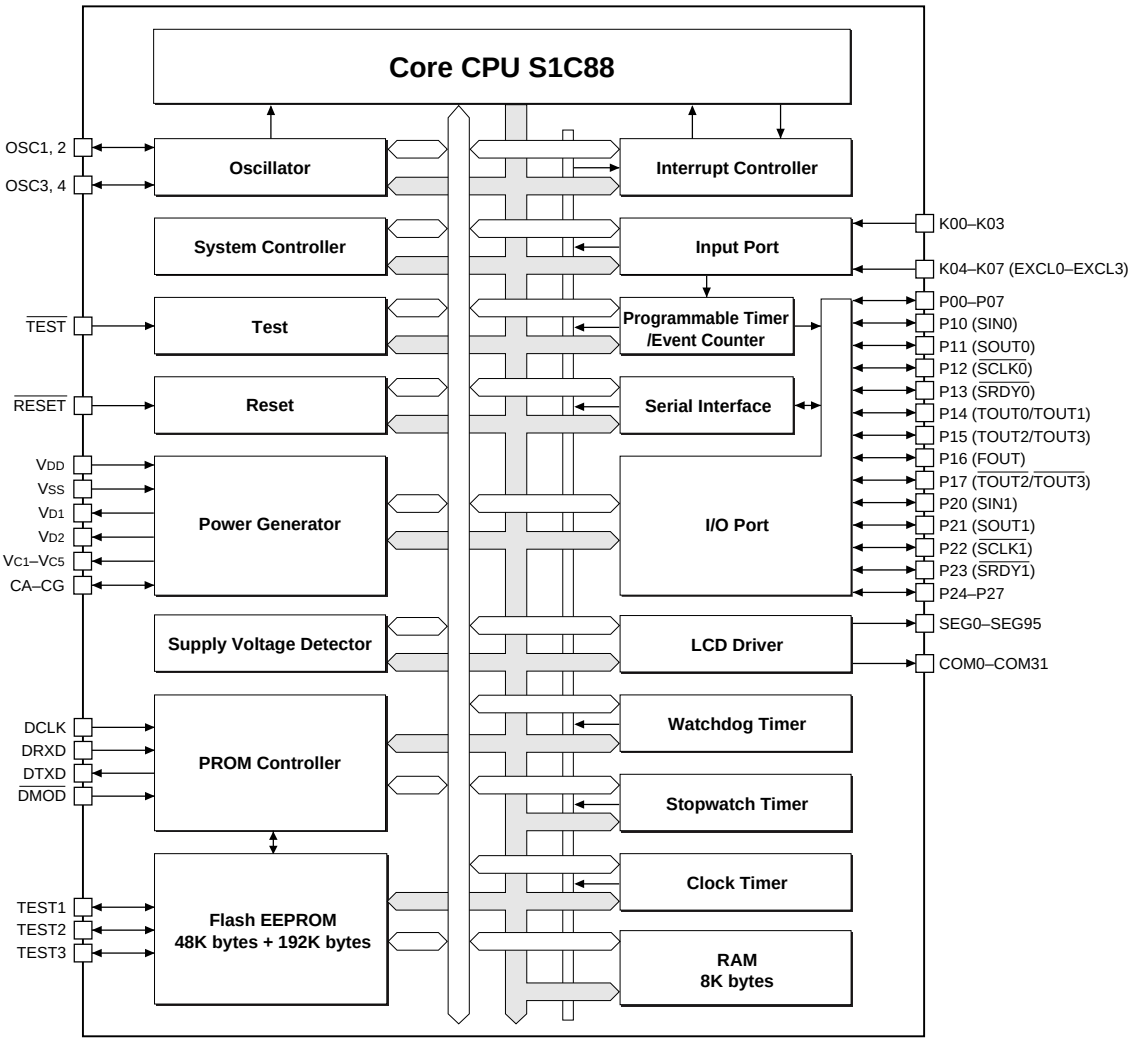
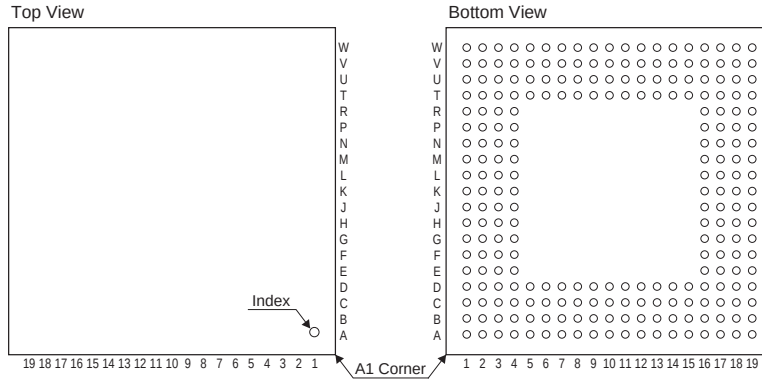


Fig. 1.2.1 S1C8F626 block diagram

1.3 Pins

1.3.1 Pin layout diagram

VFBGA10H-240pin

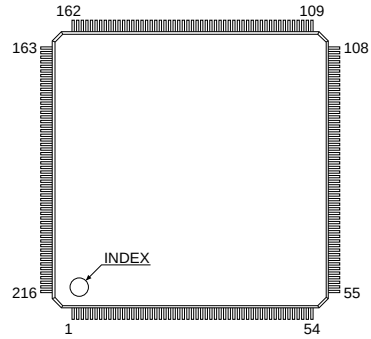


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	N.C.	N.C.	**VC3**	**CA**	**CD**	**CG**	**TEST3**	**COM16**	**COM20**	**COM24**	**COM28**	**SEG95**	**SEG91**	**SEG88**	**SEG85**	**SEG82**	N.C.	N.C.	N.C.	A
B	N.C.	N.C.	**VC2**	**VC5**	**CC**	**CF**	**VD2**	**VSS**	**COM19**	**COM23**	**COM27**	**COM31**	**SEG92**	**SEG89**	**SEG86**	**SEG83**	**SEG81**	N.C.	N.C.	B
C	N.C.	**VDD**	**VC1**	**VC4**	**CB**	**CE**	N.C.	**TEST1**	**COM18**	**COM22**	**COM26**	**COM30**	**SEG93**	**SEG90**	**SEG87**	**SEG84**	N.C.	**SEG80**	**SEG79**	C
D	**OSC3**	**OSC4**	N.C.	N.C.	N.C.	N.C.	N.C.	**TEST2**	**COM17**	**COM21**	**COM25**	**COM29**	**SEG94**	N.C.	N.C.	N.C.	**SEG78**	**SEG77**	**SEG76**	D
E	**VSS**	**VD1**	N.C.	N.C.												N.C.	**SEG75**	**SEG74**	**SEG73**	E
F	**OSC1**	**OSC2**	**$\overline{\text{TEST}}$**	**$\overline{\text{RESET}}$**												**SEG72**	**SEG71**	**SEG70**	**SEG69**	F
G	**$\overline{\text{DMOD}}$**	**DRXD**	**DTXD**	N.C.												**SEG68**	**SEG67**	**SEG66**	**SEG65**	G
H	**DCLK**	**K07** (EXCL3)	**K06** (EXCL2)	**K05** (EXCL1)												**SEG64**	**SEG63**	**SEG62**	**SEG61**	H
J	**K04** (EXCL0)	**K03**	**K02**	**K01**												**SEG60**	**SEG59**	**SEG58**	**SEG57**	J
K	**K00**	**P27**	**P26**	**P25**												**SEG56**	**SEG55**	**SEG54**	**SEG53**	K
L	**P24**	**P23** (SRDY1)	**P22** (SCLK1)	**P21** (SOUT1)												**SEG52**	**SEG51**	**SEG50**	**SEG49**	L
M	**P20** (SIN1)	**P17** (TOUT2/ TOUT3)	**P16** (FOUT)	**P15** (TOUT2/ TOUT3)												**SEG48**	**SEG47**	**SEG46**	**SEG45**	M
N	**P14** (TOUT0/ TOUT1)	**P13** (SRDY0)	**P12** (SCLK0)	**P11** (SOUT0)												N.C.	**SEG44**	**SEG43**	**SEG42**	N
P	**P10** (SIN0)	**P07**	**P06**	**P05**												N.C.	**SEG41**	**SEG40**	**SEG39**	P
R	**P04**	**P03**	**P02**	N.C.												N.C.	**SEG38**	**SEG37**	**SEG36**	R
T	**P01**	**P00**	N.C.	N.C.	N.C.	N.C.	**COM12**	**SEG0**	**SEG4**	**SEG8**	**SEG12**	**SEG16**	**SEG20**	**SEG24**	N.C.	N.C.	**SEG35**	**SEG34**	**SEG33**	T
U	**VDD**	**VSS**	N.C.	**COM2**	**COM5**	**COM8**	**COM11**	**COM15**	**SEG3**	**SEG7**	**SEG11**	**SEG15**	**SEG19**	**SEG23**	**SEG27**	N.C.	N.C.	**SEG32**	N.C.	U
V	N.C.	N.C.	N.C.	**COM1**	**COM4**	**COM7**	**COM10**	**COM14**	**SEG2**	**SEG6**	**SEG10**	**SEG14**	**SEG18**	**SEG22**	**SEG26**	**SEG29**	**SEG31**	N.C.	N.C.	V
W	N.C.	N.C.	N.C.	**COM0**	**COM3**	**COM6**	**COM9**	**COM13**	**SEG1**	**SEG5**	**SEG9**	**SEG13**	**SEG17**	**SEG21**	**SEG25**	**SEG28**	**SEG30**	N.C.	N.C.	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Top View

Fig. 1.3.1.1 S1C8F626 pin layout (VFBGA10H-240pin)

QFP21-216pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	–	55	–	109	–	163	–
2	–	56	–	110	–	164	–
3	–	57	–	111	–	165	–
4	SEG32	58	SEG81	112	V_{DD}	166	COM0
5	SEG33	59	SEG82	113	OSC3	167	COM1
6	SEG34	60	SEG83	114	OSC4	168	COM2
7	SEG35	61	SEG84	115	V_{SS}	169	COM3
8	SEG36	62	SEG85	116	V_{D1}	170	COM4
9	SEG37	63	SEG86	117	OSC1	171	COM5
10	SEG38	64	SEG87	118	OSC2	172	COM6
11	SEG39	65	SEG88	119	$\overline{TEST}$	173	COM7
12	SEG40	66	SEG89	120	$\overline{RESET}$	174	COM8
13	SEG41	67	SEG90	121	$\overline{DMOD}$	175	COM9
14	SEG42	68	SEG91	122	DRXD	176	COM10
15	SEG43	69	SEG92	123	DTXD	177	COM11
16	SEG44	70	SEG93	124	DCLK	178	COM12
17	SEG45	71	SEG94	125	K07/EXCL3	179	COM13
18	SEG46	72	SEG95	126	K06/EXCL2	180	COM14
19	SEG47	73	COM31	127	K05/EXCL1	181	COM15
20	SEG48	74	COM30	128	K04/EXCL0	182	SEG0
21	SEG49	75	COM29	129	K03	183	SEG1
22	SEG50	76	COM28	130	K02	184	SEG2
23	SEG51	77	COM27	131	K01	185	SEG3
24	SEG52	78	COM26	132	K00	186	SEG4
25	SEG53	79	COM25	133	P27	187	SEG5
26	SEG54	80	COM24	134	P26	188	SEG6
27	SEG55	81	COM23	135	P25	189	SEG7
28	SEG56	82	COM22	136	P24	190	SEG8
29	SEG57	83	COM21	137	P23/$\overline{SRDY1}$	191	SEG9
30	SEG58	84	COM20	138	P22/$\overline{SCLK1}$	192	SEG10
31	SEG59	85	COM19	139	P21/SOUT1	193	SEG11
32	SEG60	86	COM18	140	P20/SIN1	194	SEG12
33	SEG61	87	COM17	141	P17/$\overline{TOUT2}$/$\overline{TOUT3}$	195	SEG13
34	SEG62	88	COM16	142	P16/FOUT	196	SEG14
35	SEG63	89	V_{SS}	143	P15/TOUT2/TOUT3	197	SEG15
36	SEG64	90	TEST1	144	P14/TOUT0/TOUT1	198	SEG16
37	SEG65	91	TEST2	145	P13/$\overline{SRDY0}$	199	SEG17
38	SEG66	92	TEST3	146	P12/$\overline{SCLK0}$	200	SEG18
39	SEG67	93	V_{D2}	147	P11/SOUT0	201	SEG19
40	SEG68	94	CG	148	P10/SIN0	202	SEG20
41	SEG69	95	CF	149	P07	203	SEG21
42	SEG70	96	CE	150	P06	204	SEG22
43	SEG71	97	CD	151	P05	205	SEG23
44	SEG72	98	CC	152	P04	206	SEG24
45	SEG73	99	CB	153	P03	207	SEG25
46	SEG74	100	CA	154	P02	208	SEG26
47	SEG75	101	V_{C5}	155	P01	209	SEG27
48	SEG76	102	V_{C4}	156	P00	210	SEG28
49	SEG77	103	V_{C3}	157	V_{DD}	211	SEG29
50	SEG78	104	V_{C2}	158	V_{SS}	212	SEG30
51	SEG79	105	V_{C1}	159	–	213	SEG31
52	SEG80	106	–	160	–	214	–
53	–	107	–	161	–	215	–
54	–	108	–	162	–	216	–

Fig. 1.3.1.2 S1C8F626 pin layout (QFP21-216pin)

1.3.2 Pin description

Table 1.3.2.1 S1C8F626 pin description

Pin name	Pin No. (VFBGA)	Pin No. (QFP)	I/O	Initial status*3	Function
V_{DD}	C2, U1	112, 157	–	–	Power supply (+) terminal
V_{SS}	B8, E1, U2	89, 115, 158	–	–	Power supply (GND) terminal
V_{D1}	E2	116	–	–	Internal logic system and oscillation system voltage regulator output terminals
V_{D2}	B7	93	–	–	LCD circuit power voltage booster output terminal
V_{C1}–V_{C5}	C3, B3, A3, C4, B4	105–101	–	–	LCD drive voltage output terminals
CA–CG	A4, C5, B5, A5, C6, B6, A6	100–94	–	–	LCD and power voltage booster capacitor connection terminals
OSC1	F1	117	I	I	OSC1 oscillation input terminal (crystal oscillation)
OSC2	F2	118	O	O	OSC1 oscillation output terminal
OSC3	D1	113	I	I	OSC3 oscillation input terminal (crystal/ceramic or CR oscillation)
OSC4	D2	114	O	O	OSC3 oscillation output terminal
K00–K03	K1, J4, J3, J2	132–129	I	I (Pull-up)	Input port terminals
K04 (EXCL0)	J1	128	I (I)	I (Pull-up)	Input port terminal (Programmable timer external clock input terminal)
K05 (EXCL1)	H4	127	I (I)	I (Pull-up)	Input port terminal (Programmable timer external clock input terminal)
K06 (EXCL2)	H3	126	I (I)	I (Pull-up)	Input port terminal (Programmable timer external clock input terminal)
K07 (EXCL3)	H2	125	I (I)	I (Pull-up)	Input port terminal (Programmable timer external clock input terminal)
P00–P07	T2, T1, R3, R2, R1, P4, P3, P2	156–149	I/O	I (Pull-up)	I/O port terminals
P10 (SIN0)	P1	148	I/O (I)	I (Pull-up)	I/O port terminal (Serial I/F Ch. 0 data input terminal)
P11 (SOUT0)	N4	147	I/O (O)	I (Pull-up)	I/O port terminal (Serial I/F Ch. 0 data output terminal)
P12 ($\overline{SCLK0}$)	N3	146	I/O (I/O)	I (Pull-up)	I/O port terminal (Serial I/F Ch. 0 clock I/O terminal)
P13 ($\overline{SRDY0}$)	N2	145	I/O (O)	I (Pull-up)	I/O port terminal (Serial I/F Ch. 0 ready signal output terminal)
P14 (TOUT0/TOUT1)	N1	144	I/O (O)	I (Pull-up)	I/O port terminal (Programmable timer 0/1 output terminal)
P15 (TOUT2/TOUT3)	M4	143	I/O (O)	I (Pull-up)	I/O port terminal (Programmable timer 2/3 output terminal)
P16 (FOUT)	M3	142	I/O (O)	I (Pull-up)	I/O port terminal (FOUT clock output terminal)
P17 ($\overline{TOUT2}$/$\overline{TOUT3}$)	M2	141	I/O (O)	I (Pull-up)	I/O port terminal (Programmable timer 2/3 inverted output terminal)
P20 (SIN1)	M1	140	I/O (I)	I (Pull-up)	I/O port terminal (Serial I/F Ch. 1 data input terminal)
P21 (SOUT1)	L4	139	I/O (O)	I (Pull-up)	I/O port terminal (Serial I/F Ch. 1 data output terminal)
P22 ($\overline{SCLK1}$)	L3	138	I/O (I/O)	I (Pull-up)	I/O port terminal (Serial I/F Ch. 1 clock I/O terminal)
P23 ($\overline{SRDY1}$)	L2	137	I/O (O)	I (Pull-up)	I/O port terminal (Serial I/F Ch. 1 ready signal output terminal)
P24–P27	L1, K4, K3, K2	136–133	I/O	I (Pull-up)	I/O port terminals
COM0–COM31	*1	166–181, 88–73	O	O (L)	LCD common output terminals
SEG0–SEG95	*2	182–213, 4–52, 58–72	O	O (L)	LCD segment output terminals
$\overline{DMOD}$	G1	121	I	I (Pull-up)	PROM programming control terminal
DCLK	H1	124	I	I (Pull-up)	Clock input terminal for PROM programming
DRXD	G2	122	I	I (Pull-up)	Serial data input terminal for PROM programming
DTXD	G3	123	O	O (H)	Serial data output terminal for PROM programming
$\overline{RESET}$	F4	120	I	I (Pull-up)	Initial reset input terminal
$\overline{TEST}$	F3	119	I	I (Pull-up)	Test input terminal
TEST1–TEST3	C8, D8, A7	90–92	I/O	–	Test terminals (open TEST1 and TEST3, and connect TEST2 to V_{DD} during normal operation)

*1 COM0–COM31: W4, V4, U4, W5, V5, U5, W6, V6, U6, W7, V7, U7, T7, W8, V8, U8, A8, D9, C9, B9, A9, D10, C10, B10, A10, D11, C11, B11, A11, D12, C12, B12

*2 SEG0–SEG95: T8, W9, V9, U9, T9, W10, V10, U10, T10, W11, V11, U11, T11, W12, V12, U12, T12, W13, V13, U13, T13, W14, V14, U14, T14, W15, V15, U15, W16, V16, W17, V17, U18, T19, T18, T17, R19, R18, R17, P19, P18, P17, N19, N18, N17, M19, M18, M17, M16, L19, L18, L17, L16, K19, K18, K17, K16, J19, J18, J17, J16, H19, H18, H17, H16, G19, G18, G17, G16, F19, F18, F17, F16, E19, E18, E17, D19, D18, D17, C19, C18, B17, A16, B16, C16, A15, B15, C15, A14, B14, C14, A13, B13, C13, D13, A12

*3 (Pull-up): pulled up, (H): high-level output, (L): low-level output

Note: In the S1C8F626, the port configured for output cannot be set in high-impedance status.

1.4 Mask Option

The S1C8F626 has two optional configurations (Configuration 1 and Configuration 2) as shown in Table 1.4.1 allowing oscillation circuit selection of the built-in oscillator types.

Table 1.4.1 S1C8F626 optional configurations

Option	OSC1 oscillation circuit	OSC3 oscillation circuit
Configuration 1	Crystal	Crystal/Ceramic
Configuration 2	Crystal	CR

To perform debugging with the ICE (S5U1C88000H5) and Peripheral Circuit Boards (S5U1C88000P1&S5U1C88655P2), it is necessary to create an option data file by selecting two options shown in Table 1.4.2 using the function option generator winfog. These options allow selection of the OSC1 and OSC3 clocks on the Peripheral Circuit Boards from either the internal clock or user clock. When the user clock is selected, supply an operating clock to the OSC1 / OSC3 pin in the Peripheral Circuit Board connector. When the internal clock is selected, the clock is generated on the board according to the selected IC option. These options do not affect the actual IC operation. Refer to Appendix in this manual for details of the Peripheral Circuit Boards and the "S5U1C88000C Manual II" for winfog.

Table 1.4.2 Peripheral Circuit Board option

Item	Option
OSC1 oscillation circuit (OSC1 SYSTEM CLOCK)	☐ 1. Internal clock ☐ 2. User clock
OSC3 oscillation circuit (OSC3 SYSTEM CLOCK)	☐ 1. Internal clock ☐ 2. User clock

2 POWER SUPPLY

This section explains the operating voltage and the configuration of the internal power supply circuit of the S1C8F626.

2.1 Operating Voltage

The S1C8F626 operating power voltage is as follows:

Normal operation mode: 1.8 V to 3.6 V
Flash programming mode: 2.7 V to 3.6 V

2.2 Internal Power Supply Circuit

The S1C8F626 incorporates the power supply circuit shown in Figure 2.2.1. When voltage within the range described above is supplied to VDD (+) and VSS (GND), all the voltages needed for the internal circuit are generated internally in the IC. Roughly speaking, the power supply circuit is divided into three sections.

Table 2.2.1 Power supply circuit

Circuit	Power supply circuit	Output voltage
Oscillation circuits, Internal circuits	Internal logic voltage regulator	VD1
LCD system voltage regulator	Power voltage booster	VDD or VD2
LCD driver	LCD system voltage regulator	VC1–VC5

The internal logic voltage regulator generates the operating voltage <VD1> for driving the internal logic circuits and the oscillation circuit.
The VD1 voltage value can be switched in program; it should be set to 1.8 V in normal operation mode or 2.5 V in Flash programming mode. Refer to Section 5.4, "Oscillation Circuits and Operating Mode", for how to switch the VD1 voltage.

The power voltage booster generates the operating voltage <VD2> for the LCD system voltage regulator. Either <VDD> or <VD2> can be selected as the power source for the LCD system voltage regulator according to the <VDD> power supply voltage level.

Table 2.2.2 Power source for LCD system voltage regulator

Supply voltage VDD	Power source for LCD system voltage regulator
1.8–2.5 V	VD2
2.5–3.6 V	VDD

The VD2 voltage is about double the VDD voltage level. Refer to Chapter 9, "ELECTRICAL CHARACTERISTICS", for details.

The LCD system voltage regulator generates the 1/5-bias LCD drive voltages <VC1>, <VC2>, <VC3>, <VC4> and <VC5>. See Chapter 9, "ELECTRICAL CHARACTERISTICS" for the voltage values.

In the S1C8F626, the LCD drive voltage is supplied to the built-in LCD driver which drives the LCD panel connected to the SEG and COM terminals.

Notes:
- *Under no circumstances should VD1, VD2, VC1, VC2, VC3, VC4 and VC5, terminal output be used to drive external circuit.*
- *If VDD is used as the power source for the LCD system voltage regulator when VDD is 2.5 V or less, the VC1 to VC5 voltages cannot be generated within specifications.*

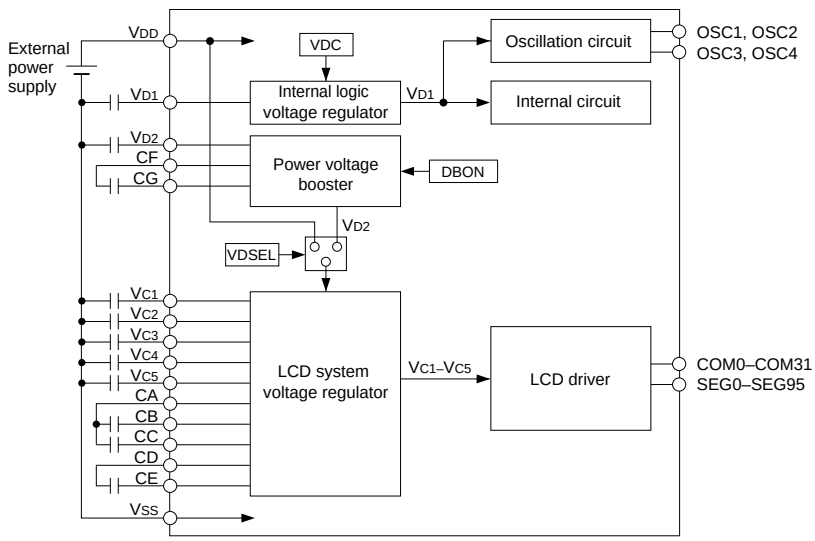


Fig. 2.2.1 Configuration of power supply circuit

3 CPU

In this section, we will explain the CPU and operating mode.

3.1 CPU

The S1C8F626 utilize the S1C88 8-bit core CPU whose register configuration, command set, etc. are virtually identical to other units in the family of processors incorporating the S1C88.

See the "S1C88 Core CPU Manual" for the S1C88.

Specifically, the S1C8F626 employs the Model 3 S1C88 CPU.

3.2 Internal Memory

The S1C8F626 is equipped with internal Flash EEPROM and RAM as shown in Figure 3.2.1.

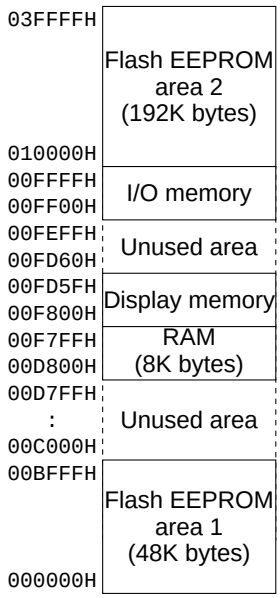


Fig. 3.2.1 Internal memory map

3.2.1 Flash EEPROM

The S1C8F626 has a built-in Flash EEPROM that supports two programming methods: PROM programmer mode to program / erase the Flash EEPROM using the exclusive PROM programmer and self programming mode to program / erase the Flash EEPROM in the user program. The Flash EEPROM is divided into two areas as shown below.

Area 1: 000000H to 00BFFFH, 48K bytes
This area is used as a program ROM.

Area 2: 010000H to 03FFFFH, 192K bytes
This area is used for storing font data. Furthermore, programs and data can be stored to the entire area when no font data is stored or to areas unused for font data.

3.2.2 RAM

The internal RAM capacity is 8K bytes and is allocated to 00D800H–00F7FFH.

3.2.3 I/O memory

A memory mapped I / O method is employed in the S1C8F626 for interfacing with internal peripheral circuit. Peripheral circuit control bits and data register are arranged in data memory space. Control and data exchange are conducted via normal memory access. I / O memory is arranged in page 0: 00FF00H–00FFFFH area.
See Section 5.1, "I / O Memory Map", for details of the I / O memory.

3.2.4 Display memory

The S1C8F626 is equipped with an internal display memory which stores a display data for LCD driver.
Display memory is arranged in page 0: 00Fx00H–00Fx5FH (x = 8–DH) in the data memory area. See Section 5.11, "LCD Driver", for details of the display memory.

3.3 Exception Processing Vectors

000000H–000051H in the program area of the S1C8F626 is assigned as exception processing vectors. Furthermore, from 000054H to 0000FFH, software interrupt vectors are assignable to any two bytes which begin with an even address.
Table 3.3.1 lists the vector addresses and the exception processing factors to which they correspond.

Table 3.3.1 Exception processing vector table

Vector address	Exception processing factor	Priority
000000H	Reset	High ↑
000002H	Zero division	
000004H	Watchdog timer ($\overline{\text{NMI}}$)	
000006H	K07 input interrupt	
000008H	K06 input interrupt	
00000AH	K05 input interrupt	
00000CH	K04 input interrupt	
00000EH	K03 input interrupt	
000010H	K02 input interrupt	
000012H	K01 input interrupt	
000014H	K00 input interrupt	
000016H	PTM 0 underflow interrupt	
000018H	PTM 0 compare match interrupt	
00001AH	PTM 1 underflow interrupt	
00001CH	PTM 1 compare match interrupt	
00001EH	PTM 2 underflow interrupt	
000020H	PTM 2 compare match interrupt	
000022H	PTM 3 underflow interrupt	
000024H	PTM 3 compare match interrupt	
000026H	System reserved (cannot be used)	
000028H	Serial I/F 0 error interrupt	
00002AH	Serial I/F 0 receiving complete interrupt	
00002CH	Serial I/F 0 transmitting complete interrupt	
00002EH	Stopwatch timer 100 Hz interrupt	
000030H	Stopwatch timer 10 Hz interrupt	
000032H	Stopwatch timer 1 Hz interrupt	
000034H	Clock timer 32 Hz interrupt	
000036H	Clock timer 8 Hz interrupt	
000038H	Clock timer 2 Hz interrupt	
00003AH	Clock timer 1 Hz interrupt	
00003CH	PTM 4 underflow interrupt	
00003EH	PTM 4 compare match interrupt	
000040H	PTM 5 underflow interrupt	
000042H	PTM 5 compare match interrupt	
000044H	PTM 6 underflow interrupt	
000046H	PTM 6 compare match interrupt	
000048H	PTM 7 underflow interrupt	
00004AH	PTM 7 compare match interrupt	
00004CH	Serial I/F 1 error interrupt	
00004EH	Serial I/F 1 receiving complete interrupt	↓
000050H	Serial I/F 1 transmitting complete interrupt	Low
000052H	System reserved (cannot be used)	No priority rating
000054H : 0000FEH	Software interrupt	

For each vector address and the address after it, the start address of the exception processing routine is written into the subordinate and super ordinate sequence. When an exception processing factor is generated, the exception processing routine is executed starting from the recorded address.
When multiple exception processing factors are generated at the same time, execution starts with the highest priority item.
The priority sequence shown in Table 3.3.1 assumes that the interrupt priority levels are all the same. The interrupt priority levels can be set by software in each system. (See Section 5.14, "Interrupt and Standby Status".)

Note: For exception processing other than reset, SC (system condition flag) and PC (program counter) are evacuated to the stack and branches to the exception processing routines. Consequently, when returning to the main routine from exception processing routines, please use the RETE instruction.

See the "S1C88 Core CPU Manual" for information on CPU operations when an exception processing factor is generated.

3.4 CC (Customized Condition Flag)

The S1C8F626 does not use the customized condition flag (CC) in the core CPU. Accordingly, it cannot be used as a branching condition for the conditional branching instruction (JRS, CARS).

3.5 CPU Mode

The CPU allows software to select its operating mode from two types shown below according to the programming area size.

■ **Minimum mode**
The program area is configured within 64K bytes in Bank 0 + any one-bank. However, the bank to be used must be specified in the CB register and cannot be changed after an initialization. This mode does not push the CB register contents onto the stack when a subroutine is called. It makes it possible to economize on stack area usage. This mode is suitable for small- to mid-scale program memory and large-scale data memory systems.

■ **Maximum mode**
The program area can be configured exceeding 64K bytes. However the CB register must be setup when the program exceeds a bank boundary every 64K bytes. This mode pushes the CB register contents when a subroutine is called. This mode is suitable for large-scale program and data memory systems.

4 INITIAL RESET

Initial reset in the S1C8F626 is required in order to initialize circuits. This section of the Manual contains a description of initial reset factors and the initial settings for internal registers, etc.

4.1 Initial Reset Factors

There are two initial reset factors for the S1C8F626 as shown below.

(1) External initial reset by the $\overline{\text{RESET}}$ terminal
(2) External initial reset by the simultaneous LOW level input at input port terminals K00–K03 (software selectable)

Figure 4.1.1 shows the configuration of the initial reset circuit.
The CPU and peripheral circuits are initialized by means of initial reset factors. When the factor is canceled, the CPU commences reset exception processing. (See the "S1C88 Core CPU Manual".) When this occurs, the reset exception processing vector, Bank 0, 000000H–000001H from program memory is read out and the program (initialization routine) which begins at the readout address is executed.

4.1.1 $\overline{\text{RESET}}$ terminal

Initial reset can be done by externally inputting a LOW level to the $\overline{\text{RESET}}$ terminal.
Be sure to maintain the $\overline{\text{RESET}}$ terminal at LOW level for the regulation time after the power on to assure the initial reset. (See Section 9.6, "AC Characteristics".)
The $\overline{\text{RESET}}$ terminal is equipped with a pull-up resistor.

4.1.2 Simultaneous LOW level input at input port terminals K00–K03

Another way of executing initial reset externally is to input a LOW level simultaneously to the input ports (K00–K03) selected with software. Since there is a built-in time authorize circuit, be sure to maintain the designated input port terminal at LOW level for 65536 / f_{OSC1} seconds (two seconds when the oscillation frequency is f_{OSC1} = 32.768 kHz) or more to perform the initial reset by means of this function. The combination of input ports (K00–K03) that can be selected with software (KEYR0–KEYR1 registers) are as follows:

Multiple key entry reset	
• Not use	(KEYR0–KEYR1 = 0)
• K00 & K01	(KEYR0–KEYR1 = 1)
• K00 & K01 & K02	(KEYR0–KEYR1 = 2)
• K00 & K01 & K02 & K03	(KEYR0–KEYR1 = 3)

For instance, let's say that "K00 & K01 & K02 & K03" is selected, when the input level at input ports K00–K03 is simultaneously LOW, initial reset will take place. Refer to Section 5.5, "Input Ports", for details of the KEYR0–KEYR1 registers.

Notes:
- *When using the multiple-key entry reset function, make sure that the designated input ports do not simultaneously switch to LOW level while the system is in normal operation.*
- *The multiple-key entry reset function cannot be used for power-on reset as it must be enabled with software.*
- *The multiple-key entry reset function cannot be used in SLEEP mode.*

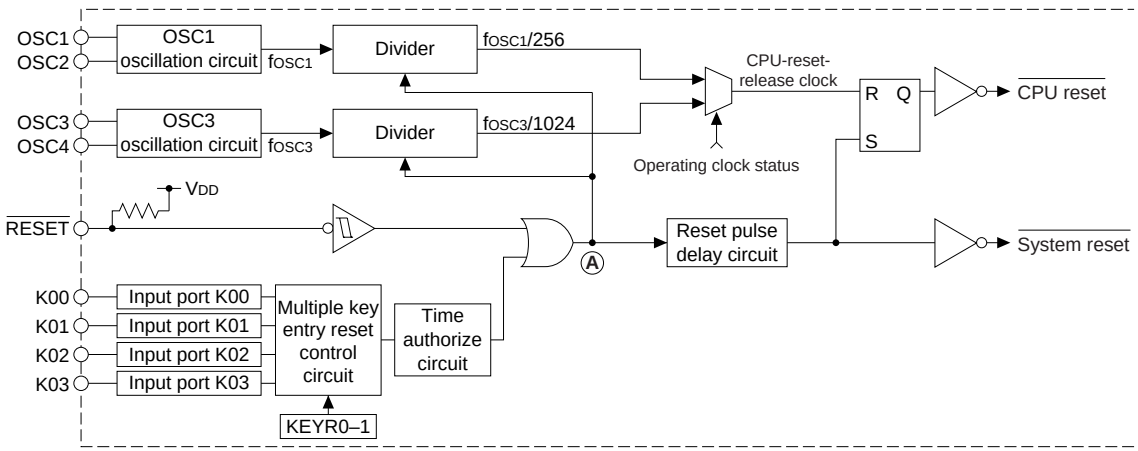


Fig. 4.1.1 Configuration of initial reset circuit

4.1.3 Initial reset sequence

Even if the $\overline{\text{RESET}}$ terminal input negates the reset signal after power is turned on, the CPU's reset status continues (or the CPU does not starts up) until the oscillation stabilization waiting time (512 / fOSC3 sec.) has elapsed.
Figure 4.1.3.1 shows the operating sequence following initial reset release.
The CPU starts operating in synchronization with the OSC3 clock after reset status is released.

Note: The oscillation stabilization time described in this section does not include oscillation start time. Therefore the time interval until the CPU starts executing instructions after power is turned on or SLEEP status is cancelled may be longer than that indicated in the figure below.

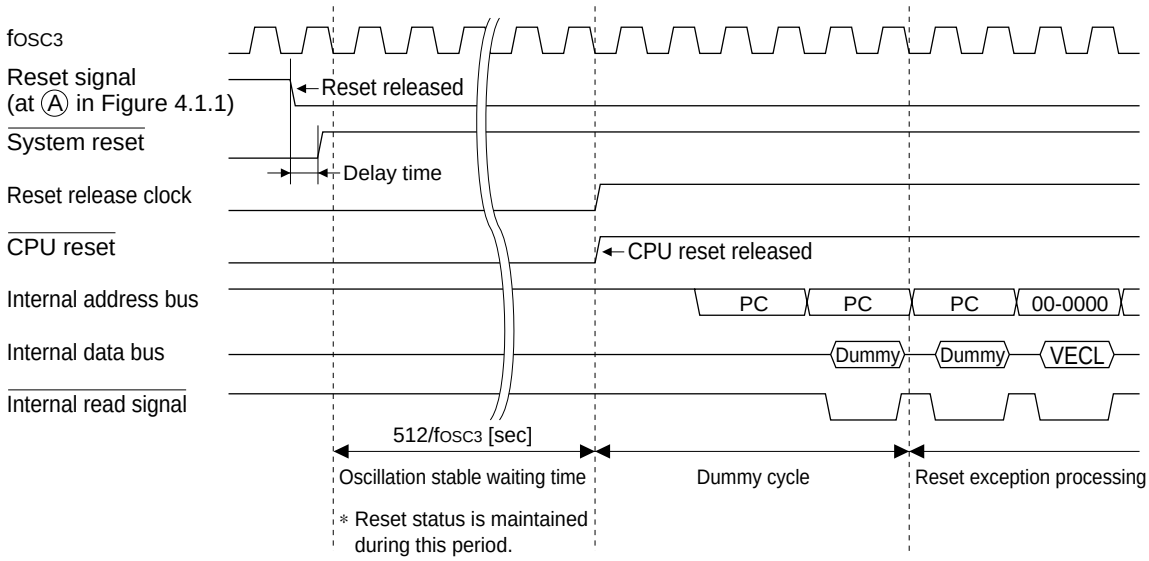


Fig. 4.1.3.1 Initial reset sequence

4.2 Initial Settings After Initial Reset

The CPU internal registers are initialized as follows during initial reset.

Table 4.2.1 Initial settings

Register name	Code	Bit length	Setting value
Data register A	A	8	Undefined
Data register B	B	8	Undefined
Index (data) register L	L	8	Undefined
Index (data) register H	H	8	Undefined
Index register IX	IX	16	Undefined
Index register IY	IY	16	Undefined
Program counter	PC	16	Undefined*
Stack pointer	SP	16	Undefined
Base register	BR	8	Undefined
Zero flag	Z	1	0
Carry flag	C	1	0
Overflow flag	V	1	0
Negative flag	N	1	0
Decimal flag	D	1	0
Unpack flag	U	1	0
Interrupt flag 0	I0	1	1
Interrupt flag 1	I1	1	1
New code bank register	NB	8	01H
Code bank register	CB	8	Undefined*
Expand page register	EP	8	00H
Expand page register for IX	XP	8	00H
Expand page register for IY	YP	8	00H

* Reset exception processing loads the preset values stored in 0 bank, 0000H–0001H into the PC. At the same time, 01H of the NB initial value is loaded into CB.

Initialize the registers which are not initialized at initial reset using software.

Since the internal RAM and display memory are not initialized at initial reset, be sure to initialize using software.

The respectively stipulated initializations are done for internal peripheral circuits. If necessary, the initialization should be done using software.
For initial value at initial reset, see the sections on the I/O memory map and peripheral circuit descriptions in the following chapter of this manual.

5 PERIPHERAL CIRCUITS AND THEIR OPERATION

The peripheral circuits of the S1C8F626 is interfaced with the CPU by means of the memory mapped I/O method. For this reason, just as with other memory access operations, peripheral circuits can be controlled by manipulating I/O memory. Below is a description of the operation and control method for each individual peripheral circuit.

5.1 I/O Memory Map

Table 5.1.1(a) I/O Memory map (00FF00H–00FF10H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00	D7	–	–	–	–	–		"0" when being read
	D6	CPUMOD	CPU mode	Maximum	Minimum	0	R/W	
	D5	–	–	–	–	–		Constantly "0" when
	D4	–	–	–	–	–		being read
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF01	D7	SPP7	Stack pointer page address (MSB)	1	0	0	R/W	
	D6	SPP6		1	0	0	R/W	
	D5	SPP5		1	0	0	R/W	
	D4	SPP4		1	0	0	R/W	
	D3	SPP3		1	0	0	R/W	
	D2	SPP2		1	0	0	R/W	
	D1	SPP1		1	0	0	R/W	
	D0	SPP0	(LSB)	1	0	0	R/W	
00FF02	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	1	R/W	
	D2	SOSC3	OSC3 oscillation On/Off control	On	Off	1	R/W	
	D1	–	–	–	–	–		"0" when being read
	D0	VDC	Operating mode selection	V_{D1} = 2.5 V	V_{D1} = 1.8 V	0	R/W	
00FF03	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	VDSEL	Power source select for LCD voltage regulator	V_{D2}	V_{DD}	0	R/W	
	D0	DBON	Power voltage booster On/Off control	On	Off	0	R/W	
00FF10	D7	HLMOD	Heavy load protection mode	On	Off	0	R/W	
	D6	SEGREV	Reverse SEG assignment	Reverse	Normal	0	R/W	
	D5	–	R/W register	1	0	0	R/W	Reserved register
	D4	–	R/W register	1	0	0	R/W	
	D3	–	R/W register	1	0	0	R/W	
	D2	DTFNT	LCD dot font selection	12×12	16×16/5×8	0	R/W	
	D1	LDUTY1	LCD drive duty selection			1	R/W	
			LDUTY1 LDUTY0 Duty					
			1 1 Not allowed					
	D0	LDUTY0	1 0 1/16			0	R/W	
			0 1 1/32					
			0 0 1/8					

Note: All the interrupts including $\overline{NMI}$ are disabled, until you write the optional value into both the 00FF00H and 00FF01H addresses.

Table 5.1.1(b) I/O Memory map (00FF11H–00FF15H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF11	D7	FRMCS	LCD frame signal source clock selection	PTM	f_{OSC1}	0	R/W	
	D6	DSPAR	LCD display memory area selection	Display area 1	Display area 0	0	R/W	
	D5	LCDC1	LCD display control LCDC1 LCDC0 LCD display 1 1 All LCDs lit 1 0 All LCDs out 0 1 Normal display 0 0 Drive off			0	R/W	These bits are reset to (0, 0) when SLP instruction is executed.
	D4	LCDC0				0	R/W	
	D3	LC3	LCD contrast adjustment LC3 LC2 LC1 LC0 Contrast 1 1 1 1 Dark 1 1 1 0 : : : : : : 0 0 0 0 Light			0	R/W	
	D2	LC2				0	R/W	
	D1	LC1				0	R/W	
	D0	LC0				0	R/W	
00FF12	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	SVDDT	SVD detection data	Low	Normal	0	R	
	D4	SVDON	SVD circuit On/Off	On	Off	0	R/W	
	D3	SVDS3	SVD criteria voltage setting SVDS3 SVDS2 SVDS1 SVDS0 Voltage (V) 1 1 1 1 2.7 1 1 1 0 2.6 1 1 0 1 2.5 : : : : : 0 0 1 1 1.8			0	R/W	
	D2	SVDS2				0	R/W	
	D1	SVDS1				0	R/W	
	D0	SVDS0				0	R/W	
00FF14	D7	PRPRT1	Programmable timer 1 clock control	On	Off	0	R/W	
	D6	PST12	Programmable timer 1 division ratio PST12 PST11 PST10 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 64 f_{OSC1} / 16 0 1 1 f_{OSC3} / 32 f_{OSC1} / 8 0 1 0 f_{OSC3} / 8 f_{OSC1} / 4 0 0 1 f_{OSC3} / 2 f_{OSC1} / 2 0 0 0 f_{OSC3} / 1 f_{OSC1} / 1			0	R/W	
	D5	PST11				0	R/W	
	D4	PST10				0	R/W	
	D3	PRPRT0	Programmable timer 0 clock control	On	Off	0	R/W	
	D2	PST02	Programmable timer 0 division ratio PST02 PST01 PST00 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 64 f_{OSC1} / 16 0 1 1 f_{OSC3} / 32 f_{OSC1} / 8 0 1 0 f_{OSC3} / 8 f_{OSC1} / 4 0 0 1 f_{OSC3} / 2 f_{OSC1} / 2 0 0 0 f_{OSC3} / 1 f_{OSC1} / 1			0	R/W	
	D1	PST01				0	R/W	
	D0	PST00				0	R/W	
00FF15	D7	PRPRT3	Programmable timer 3 clock control	On	Off	0	R/W	
	D6	PST32	Programmable timer 3 division ratio PST32 PST31 PST30 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 64 f_{OSC1} / 16 0 1 1 f_{OSC3} / 32 f_{OSC1} / 8 0 1 0 f_{OSC3} / 8 f_{OSC1} / 4 0 0 1 f_{OSC3} / 2 f_{OSC1} / 2 0 0 0 f_{OSC3} / 1 f_{OSC1} / 1			0	R/W	
	D5	PST31				0	R/W	
	D4	PST30				0	R/W	
	D3	PRPRT2	Programmable timer 2 clock control	On	Off	0	R/W	
	D2	PST22	Programmable timer 2 division ratio PST22 PST21 PST20 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 64 f_{OSC1} / 16 0 1 1 f_{OSC3} / 32 f_{OSC1} / 8 0 1 0 f_{OSC3} / 8 f_{OSC1} / 4 0 0 1 f_{OSC3} / 2 f_{OSC1} / 2 0 0 0 f_{OSC3} / 1 f_{OSC1} / 1			0	R/W	
	D1	PST21				0	R/W	
	D0	PST20				0	R/W	

Table 5.1.1(c) I/O Memory map (00FF17H–00FF1BH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF17	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PRTF3	Programmable timer 3 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D2	PRTF2	Programmable timer 2 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D1	PRTF1	Programmable timer 1 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D0	PRTF0	Programmable timer 0 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
00FF18	D7	PRPRT5	Programmable timer 5 clock control	On	Off	0	R/W	
	D6	PST52	Programmable timer 5 division ratio			0	R/W	
	D5	PST51	PST52 PST51 PST50 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 64 f_{OSC1} / 16 0 1 1 f_{OSC3} / 32 f_{OSC1} / 8 0 1 0 f_{OSC3} / 8 f_{OSC1} / 4 0 0 1 f_{OSC3} / 2 f_{OSC1} / 2 0 0 0 f_{OSC3} / 1 f_{OSC1} / 1			0	R/W	
	D4	PST50				0	R/W	
	D3	PRPRT4	Programmable timer 4 clock control	On	Off	0	R/W	
	D2	PST42	Programmable timer 4 division ratio PST42 PST41 PST40 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 64 f_{OSC1} / 16 0 1 1 f_{OSC3} / 32 f_{OSC1} / 8 0 1 0 f_{OSC3} / 8 f_{OSC1} / 4 0 0 1 f_{OSC3} / 2 f_{OSC1} / 2 0 0 0 f_{OSC3} / 1 f_{OSC1} / 1			0	R/W	
	D1	PST41				0	R/W	
	D0	PST40				0	R/W	
00FF19	D7	PRPRT7	Programmable timer 7 clock control	On	Off	0	R/W	
	D6	PST72	Programmable timer 7 division ratio PST72 PST71 PST70 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 64 f_{OSC1} / 16 0 1 1 f_{OSC3} / 32 f_{OSC1} / 8 0 1 0 f_{OSC3} / 8 f_{OSC1} / 4 0 0 1 f_{OSC3} / 2 f_{OSC1} / 2 0 0 0 f_{OSC3} / 1 f_{OSC1} / 1			0	R/W	
	D5	PST71				0	R/W	
	D4	PST70				0	R/W	
	D3	PRPRT6	Programmable timer 6 clock control	On	Off	0	R/W	
	D2	PST62	Programmable timer 6 division ratio PST62 PST61 PST60 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 64 f_{OSC1} / 16 0 1 1 f_{OSC3} / 32 f_{OSC1} / 8 0 1 0 f_{OSC3} / 8 f_{OSC1} / 4 0 0 1 f_{OSC3} / 2 f_{OSC1} / 2 0 0 0 f_{OSC3} / 1 f_{OSC1} / 1			0	R/W	
	D1	PST61				0	R/W	
	D0	PST60				0	R/W	
00FF1B	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PRTF7	Programmable timer 7 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D2	PRTF6	Programmable timer 6 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D1	PRTF5	Programmable timer 5 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D0	PRTF4	Programmable timer 4 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	

Table 5.1.1(d) I/O Memory map (00FF20H–00FF25H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF01 PSIF00 PSW1 PSW0 PTM1 PTM0	Priority level Level 3 Level 2 Level 1 Level 0	0	R/W	
	D6	PK00		1 1 1 0 0 1 0 0				
	D5	PSIF01	Serial interface 0 interrupt priority register			0	R/W	
	D4	PSIF00						
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0						
00FF21	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	PPT3	Programmable timer 3–2 interrupt priority register	PPT3 PPT2 PPT1 PPT0 PSIF11 PSIF10 1 1 1 0 0 1 0 0	Priority level Level 3 Level 2 Level 1 Level 0	0	R/W	
	D4	PPT2						
	D3	PPT1	Programmable timer 1–0 interrupt priority register			0	R/W	
	D2	PPT0						
	D1	PSIF11	Serial interface 1 interrupt priority register			0	R/W	
	D0	PSIF10						
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register					
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register					
	D3	ETM32	Clock timer 32 Hz interrupt enable register					
	D2	ETM8	Clock timer 8 Hz interrupt enable register					
	D1	ETM2	Clock timer 2 Hz interrupt enable register					
	D0	ETM1	Clock timer 1 Hz interrupt enable register					
00FF23	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	ESERR1	Serial I/F 1 (error) interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D4	ESREC1	Serial I/F 1 (receiving) interrupt enable register					
	D3	ESTRA1	Serial I/F 1 (transmitting) interrupt enable register					
	D2	ESERR0	Serial I/F 0 (error) interrupt enable register					
	D1	ESREC0	Serial I/F 0 (receiving) interrupt enable register					
	D0	ESTRA0	Serial I/F 0 (transmitting) interrupt enable register					
00FF24	D7	EK07	K07 interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	EK06	K06 interrupt enable					
	D5	EK05	K05 interrupt enable					
	D4	EK04	K04 interrupt enable					
	D3	EK03	K03 interrupt enable					
	D2	EK02	K02 interrupt enable					
	D1	EK01	K01 interrupt enable					
	D0	EK00	K00 interrupt enable					
00FF25	D7	ETC3	PTM3 compare match interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	ETU3	PTM3 underflow interrupt enable					
	D5	ETC2	PTM2 compare match interrupt enable					
	D4	ETU2	PTM2 underflow interrupt enable					
	D3	ETC1	PTM1 compare match interrupt enable					
	D2	ETU1	PTM1 underflow interrupt enable					
	D1	ETC0	PTM0 compare match interrupt enable					
	D0	ETU0	PTM0 underflow interrupt enable					

Table 5.1.1(e) I/O Memory map (00FF26H–00FF2CH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF26	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag					
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag					
	D3	FTM32	Clock timer 32 Hz interrupt factor flag					
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag					
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					
00FF27	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	FSERR1	Serial I/F 1 (error) interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D4	FSREC1	Serial I/F 1 (receiving) interrupt factor flag					
	D3	FSTRA1	Serial I/F 1 (transmitting) interrupt factor flag					
	D2	FSERR0	Serial I/F 0 (error) interrupt factor flag					
	D1	FSREC0	Serial I/F 0 (receiving) interrupt factor flag					
	D0	FSTRA0	Serial I/F 0 (transmitting) interrupt factor flag					
00FF28	D7	FK07	K07 interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D6	FK06	K06 interrupt factor flag					
	D5	FK05	K05 interrupt factor flag					
	D4	FK04	K04 interrupt factor flag					
	D3	FK03	K03 interrupt factor flag					
	D2	FK02	K02 interrupt factor flag					
	D1	FK01	K01 interrupt factor flag					
	D0	FK00	K00 interrupt factor flag					
00FF29	D7	FTC3	PTM3 compare match interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D6	FTU3	PTM3 underflow interrupt factor flag					
	D5	FTC2	PTM2 compare match interrupt factor flag					
	D4	FTU2	PTM2 underflow interrupt factor flag					
	D3	FTC1	PTM1 compare match interrupt factor flag					
	D2	FTU1	PTM1 underflow interrupt factor flag					
	D1	FTC0	PTM0 compare match interrupt factor flag					
	D0	FTU0	PTM0 underflow interrupt factor flag					
00FF2A	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT7	Programmable timer 7–6 interrupt priority register	PPT7 PPT6 Priority level PPT5 PPT4 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D2	PPT6						
	D1	PPT5	Programmable timer 5–4 interrupt priority register			0	R/W	
	D0	PPT4						
00FF2C	D7	ETC7	PTM7 compare match interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	ETU7	PTM7 underflow interrupt enable					
	D5	ETC6	PTM6 compare match interrupt enable					
	D4	ETU6	PTM6 underflow interrupt enable					
	D3	ETC5	PTM5 compare match interrupt enable					
	D2	ETU5	PTM5 underflow interrupt enable					
	D1	ETC4	PTM4 compare match interrupt enable					
	D0	ETU4	PTM4 underflow interrupt enable					

Table 5.1.1(f) I/O Memory map (00FF2EH–00FF34H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF2E	D7	FTC7	PTM7 compare match interrupt factor flag	(R)	(R)			
	D6	FTU7	PTM7 underflow interrupt factor flag	Interrupt	No interrupt			
	D5	FTC6	PTM6 compare match interrupt factor flag	factor is	factor is			
	D4	FTU6	PTM6 underflow interrupt factor flag	generated	generated			
	D3	FTC5	PTM5 compare match interrupt factor flag			0	R/W	
	D2	FTU5	PTM5 underflow interrupt factor flag	(W)	(W)			
	D1	FTC4	PTM4 compare match interrupt factor flag	Reset	No operation			
	D0	FTU4	PTM4 underflow interrupt factor flag					
00FF30	D7	MODE16_A	PTM0–1 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_A	External clock 0 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT0	PTM0 clock output control	On	Off	0	R/W	
	D2	PTRUN0	PTM0 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET0	PTM0 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL0	PTM0 input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT1	PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	PTM1 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET1	PTM1 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL1	PTM1 input clock selection	External clock	Internal clock	0	R/W	
00FF32	D7	RDR07	PTM0 reload data D7 (MSB)					
	D6	RDR06	PTM0 reload data D6					
	D5	RDR05	PTM0 reload data D5					
	D4	RDR04	PTM0 reload data D4					
	D3	RDR03	PTM0 reload data D3	High	Low	1	R/W	
	D2	RDR02	PTM0 reload data D2					
	D1	RDR01	PTM0 reload data D1					
	D0	RDR00	PTM0 reload data D0 (LSB)					
00FF33	D7	RDR17	PTM1 reload data D7 (MSB)					
	D6	RDR16	PTM1 reload data D6					
	D5	RDR15	PTM1 reload data D5					
	D4	RDR14	PTM1 reload data D4					
	D3	RDR13	PTM1 reload data D3	High	Low	1	R/W	
	D2	RDR12	PTM1 reload data D2					
	D1	RDR11	PTM1 reload data D1					
	D0	RDR10	PTM1 reload data D0 (LSB)					
00FF34	D7	CDR07	PTM0 compare data D7 (MSB)					
	D6	CDR06	PTM0 compare data D6					
	D5	CDR05	PTM0 compare data D5					
	D4	CDR04	PTM0 compare data D4					
	D3	CDR03	PTM0 compare data D3	High	Low	0	R/W	
	D2	CDR02	PTM0 compare data D2					
	D1	CDR01	PTM0 compare data D1					
	D0	CDR00	PTM0 compare data D0 (LSB)					

Table 5.1.1(g) I/O Memory map (00FF35H–00FF3AH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF35	D7	CDR17	PTM1 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR16	PTM1 compare data D6					
	D5	CDR15	PTM1 compare data D5					
	D4	CDR14	PTM1 compare data D4					
	D3	CDR13	PTM1 compare data D3					
	D2	CDR12	PTM1 compare data D2					
	D1	CDR11	PTM1 compare data D1					
	D0	CDR10	PTM1 compare data D0 (LSB)					
00FF36	D7	PTM07	PTM0 data D7 (MSB)	High	Low	1	R	
	D6	PTM06	PTM0 data D6					
	D5	PTM05	PTM0 data D5					
	D4	PTM04	PTM0 data D4					
	D3	PTM03	PTM0 data D3					
	D2	PTM02	PTM0 data D2					
	D1	PTM01	PTM0 data D1					
	D0	PTM00	PTM0 data D0 (LSB)					
00FF37	D7	PTM17	PTM1 data D7 (MSB)	High	Low	1	R	
	D6	PTM16	PTM1 data D6					
	D5	PTM15	PTM1 data D5					
	D4	PTM14	PTM1 data D4					
	D3	PTM13	PTM1 data D3					
	D2	PTM12	PTM1 data D2					
	D1	PTM11	PTM1 data D1					
	D0	PTM10	PTM1 data D0 (LSB)					
00FF38	D7	MODE16_B	PTM2–3 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_B	External clock 1 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	RPTOUT2	PTM2 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT2	PTM2 clock output control	On	Off	0	R/W	
	D2	PTRUN2	PTM2 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET2	PTM2 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL2	PTM2 input clock selection	External clock	Internal clock	0	R/W	
00FF39	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	RPTOUT3	PTM3 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT3	PTM3 clock output control	On	Off	0	R/W	
	D2	PTRUN3	PTM3 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET3	PTM3 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL3	PTM3 input clock selection	External clock	Internal clock	0	R/W	
00FF3A	D7	RDR27	PTM2 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR26	PTM2 reload data D6					
	D5	RDR25	PTM2 reload data D5					
	D4	RDR24	PTM2 reload data D4					
	D3	RDR23	PTM2 reload data D3					
	D2	RDR22	PTM2 reload data D2					
	D1	RDR21	PTM2 reload data D1					
	D0	RDR20	PTM2 reload data D0 (LSB)					

Table 5.1.1(h) I/O Memory map (00FF3BH–00FF40H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF3B	D7	RDR37	PTM3 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR36	PTM3 reload data D6					
	D5	RDR35	PTM3 reload data D5					
	D4	RDR34	PTM3 reload data D4					
	D3	RDR33	PTM3 reload data D3					
	D2	RDR32	PTM3 reload data D2					
	D1	RDR31	PTM3 reload data D1					
	D0	RDR30	PTM3 reload data D0 (LSB)					
00FF3C	D7	CDR27	PTM2 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR26	PTM2 compare data D6					
	D5	CDR25	PTM2 compare data D5					
	D4	CDR24	PTM2 compare data D4					
	D3	CDR23	PTM2 compare data D3					
	D2	CDR22	PTM2 compare data D2					
	D1	CDR21	PTM2 compare data D1					
	D0	CDR20	PTM2 compare data D0 (LSB)					
00FF3D	D7	CDR37	PTM3 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR36	PTM3 compare data D6					
	D5	CDR35	PTM3 compare data D5					
	D4	CDR34	PTM3 compare data D4					
	D3	CDR33	PTM3 compare data D3					
	D2	CDR32	PTM3 compare data D2					
	D1	CDR31	PTM3 compare data D1					
	D0	CDR30	PTM3 compare data D0 (LSB)					
00FF3E	D7	PTM27	PTM2 data D7 (MSB)	High	Low	1	R	
	D6	PTM26	PTM2 data D6					
	D5	PTM25	PTM2 data D5					
	D4	PTM24	PTM2 data D4					
	D3	PTM23	PTM2 data D3					
	D2	PTM22	PTM2 data D2					
	D1	PTM21	PTM2 data D1					
	D0	PTM20	PTM2 data D0 (LSB)					
00FF3F	D7	PTM37	PTM3 data D7 (MSB)	High	Low	1	R	
	D6	PTM36	PTM3 data D6					
	D5	PTM35	PTM3 data D5					
	D4	PTM34	PTM3 data D4					
	D3	PTM33	PTM3 data D3					
	D2	PTM32	PTM3 data D2					
	D1	PTM31	PTM3 data D1					
	D0	PTM30	PTM3 data D0 (LSB)					
00FF40	D7	WDEN	Watchdog timer enable	Enable	Disable	1	R/W	
	D6	FOUT2	FOUT frequency selection			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	

FOUT2	FOUT1	FOUT0	Frequency
1	1	1	f_{OSC3} / 8
1	1	0	f_{OSC3} / 4
1	0	1	f_{OSC3} / 2
1	0	0	f_{OSC3} / 1
0	1	1	f_{OSC1} / 8
0	1	0	f_{OSC1} / 4
0	0	1	f_{OSC1} / 2
0	0	0	f_{OSC1} / 1

Table 5.1.1(i) I/O Memory map (00FF41H–00FF49H)

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF41	D7	TMD7	Clock timer data 1 Hz		High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz						
	D5	TMD5	Clock timer data 4 Hz						
	D4	TMD4	Clock timer data 8 Hz						
	D3	TMD3	Clock timer data 16 Hz						
	D2	TMD2	Clock timer data 32 Hz						
	D1	TMD1	Clock timer data 64 Hz						
	D0	TMD0	Clock timer data 128 Hz						
00FF42	D7	–	–		–	–	–		Constantly "0" when being read
	D6	–	–		–	–	–		
	D5	–	–		–	–	–		
	D4	–	–		–	–	–		
	D3	–	–		–	–	–		
	D2	–	–		–	–	–		
	D1	SWRST	Stopwatch timer reset		Reset	No operation	–	W	
	D0	SWRUN	Stopwatch timer Run/Stop control		Run	Stop	0	R/W	
00FF43	D7	SWD7	Stopwatch timer data				0	R	
	D6	SWD6							
	D5	SWD5	BCD (1/10 sec)						
	D4	SWD4							
	D3	SWD3	Stopwatch timer data						
	D2	SWD2							
	D1	SWD1	BCD (1/100 sec)						
	D0	SWD0							
00FF48	D7	–	–		–	–	–		"0" when being read
	D6	EPR0	Serial I/F 0 parity enable register		With parity	Non parity	0	R/W	Only for asynchronous mode
	D5	PMD0	Serial I/F 0 parity mode selection		Odd	Even	0	R/W	
	D4	SCS01	Serial I/F 0 clock source selection				0	R/W	In the clock synchronous slave mode, external clock is selected.
			SCS01 SCS00 Clock source						
			1 1 Programmable timer 1						
	D3	SCS00	1 0 f_{OSC3} / 4				0	R/W	
			0 1 f_{OSC3} / 8						
			0 0 f_{OSC3} / 16						
	D2	SMD01	Serial I/F 0 mode selection				0	R/W	
			SMD01 SMD00 Mode						
			1 1 Asynchronous 8-bit						
	D1	SMD00	1 0 Asynchronous 7-bit				0	R/W	
			0 1 Clock synchronous slave						
			0 0 Clock synchronous master						
	D0	ESIF0	Serial I/F 0 enable register		Serial I/F	I/O port	0	R/W	
00FF49	D7	–	–		–	–	–		"0" when being read
	D6	FER0	Serial I/F 0 framing error flag	R	Error	No error	0	R/W	Only for asynchronous mode
				W	Reset (0)	No operation			
	D5	PER0	Serial I/F 0 parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER0	Serial I/F 0 overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG0	Serial I/F 0 receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN0	Serial I/F 0 receive enable		Enable	Disable	0	R/W	
	D1	TXTRG0	Serial I/F 0 transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN0	Serial I/F 0 transmit enable		Enable	Disable	0	R/W	

Table 5.1.1(j) I/O Memory map (00FF4AH–00FF4EH)

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF4A	D7	TRXD07	Serial I/F 0 transmit/Receive data D7 (MSB)		High	Low	X	R/W	Reading: Receive data Writing: Transmit data
	D6	TRXD06	Serial I/F 0 transmit/Receive data D6				X	R/W	
	D5	TRXD05	Serial I/F 0 transmit/Receive data D5				X	R/W	
	D4	TRXD04	Serial I/F 0 transmit/Receive data D4				X	R/W	
	D3	TRXD03	Serial I/F 0 transmit/Receive data D3				X	R/W	
	D2	TRXD02	Serial I/F 0 transmit/Receive data D2				X	R/W	
	D1	TRXD01	Serial I/F 0 transmit/Receive data D1				X	R/W	
	D0	TRXD00	Serial I/F 0 transmit/Receive data D0 (LSB)				X	R/W	
00FF4B	D7	IRTL0	Serial I/F 0 IrDA I/F output logic inverse		Inverse	Direct	0	R/W	
	D6	IRIL0	Serial I/F 0 IrDA I/F input logic inverse		Inverse	Direct	0	R/W	
	D5	–	–		–	–	–		"0" when being read
	D4	IRST0	Serial I/F 0 IrDA interface enable		IrDA	Normal	0	R/W	
	D3	–	–		–	–	–		Constantly "0" when being read
	D2	–	–		–	–	–		
	D1	STPB0	Serial I/F 0 stop bit selection		2 bits	1 bit	0	R/W	
	D0	SDP0	Serial I/F 0 data input/output permutation selection		MSB first	LSB first	0	R/W	
00FF4C	D7	–	–		–	–	–		"0" when being read
	D6	EPR1	Serial I/F 1 parity enable register		With parity	Non parity	0	R/W	Only for asynchronous mode
	D5	PMD1	Serial I/F 1 parity mode selection		Odd	Even	0	R/W	
	D4	SCS11	Serial I/F 1 clock source selection SCS11 SCS10 Clock source 1 1 Programmable timer 7				0	R/W	In the clock synchronous slave mode, external clock is selected.
	D3	SCS10	1 0 f_{OSC3} / 4 0 1 f_{OSC3} / 8 0 0 f_{OSC3} / 16				0	R/W	
	D2	SMD11	Serial I/F 1 mode selection SMD11 SMD10 Mode 1 1 Asynchronous 8-bit				0	R/W	
	D1	SMD10	1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master				0	R/W	
	D0	ESIF1	Serial I/F 1 enable register		Serial I/F	I/O port	0	R/W	
00FF4D	D7	–	–		–	–	–		"0" when being read
	D6	FER1	Serial I/F 1 framing error flag	R	Error	No error	0	R/W	Only for asynchronous mode
				W	Reset (0)	No operation			
	D5	PER1	Serial I/F 1 parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER1	Serial I/F 1 overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG1	Serial I/F 1 receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN1	Serial I/F 1 receive enable		Enable	Disable	0	R/W	
	D1	TXTRG1	Serial I/F 1 transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN1	Serial I/F 1 transmit enable		Enable	Disable	0	R/W	
00FF4E	D7	TRXD17	Serial I/F 1 transmit/Receive data D7 (MSB)		High	Low	X	R/W	Reading: Receive data Writing: Transmit data
	D6	TRXD16	Serial I/F 1 transmit/Receive data D6				X	R/W	
	D5	TRXD15	Serial I/F 1 transmit/Receive data D5				X	R/W	
	D4	TRXD14	Serial I/F 1 transmit/Receive data D4				X	R/W	
	D3	TRXD13	Serial I/F 1 transmit/Receive data D3				X	R/W	
	D2	TRXD12	Serial I/F 1 transmit/Receive data D2				X	R/W	
	D1	TRXD11	Serial I/F 1 transmit/Receive data D1				X	R/W	
	D0	TRXD10	Serial I/F 1 transmit/Receive data D0 (LSB)				X	R/W	

Table 5.1.1(k) I/O Memory map (00FF4FH–00FF58H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF4F	D7	IRTL1	Serial I/F 1 IrDA I/F output logic inverse	Inverse	Direct	0	R/W	
	D6	IRIL1	Serial I/F 1 IrDA I/F input logic inverse	Inverse	Direct	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	IRST1	Serial I/F 1 IrDA interface enable	IrDA	Normal	0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	STPB1	Serial I/F 1 stop bit selection	2 bits	1 bit	0	R/W	
	D0	SDP1	Serial I/F 1 data input/output permutation selection	MSB first	LSB first	0	R/W	
00FF52	D7	KCP07	K07 input comparison register	Interrupt generated at falling edge	Interrupt generated at rising edge	1	R/W	
	D6	KCP06	K06 input comparison register					
	D5	KCP05	K05 input comparison register					
	D4	KCP04	K04 input comparison register					
	D3	KCP03	K03 input comparison register					
	D2	KCP02	K02 input comparison register					
	D1	KCP01	K01 input comparison register					
	D0	KCP00	K00 input comparison register					
00FF54	D7	K07D	K07 input port data	High level input	Low level input	–	R	
	D6	K06D	K06 input port data					
	D5	K05D	K05 input port data					
	D4	K04D	K04 input port data					
	D3	K03D	K03 input port data					
	D2	K02D	K02 input port data					
	D1	K01D	K01 input port data					
	D0	K00D	K00 input port data					
00FF56	D7	PULK07	K07 pull-up control register	On	Off	1	R/W	
	D6	PULK06	K06 pull-up control register					
	D5	PULK05	K05 pull-up control register					
	D4	PULK04	K04 pull-up control register					
	D3	PULK03	K03 pull-up control register					
	D2	PULK02	K02 pull-up control register					
	D1	PULK01	K01 pull-up control register					
	D0	PULK00	K00 pull-up control register					
00FF58	D7	–	–	–	–	–		"0" when being read
	D6	CTK02H	K04–K07 port chattering-eliminate setup (Input level check time)			0	R/W	
	D5	CTK01H				0	R/W	
	D4	CTK00H				0	R/W	
	D3	–	–	–	–	–		"0" when being read
	D2	CTK02L	K00–K03 port chattering-eliminate setup (Input level check time)			0	R/W	
	D1	CTK01L				0	R/W	
	D0	CTK00L				0	R/W	

CTK02H	CTK01H	CTK00H	Check time [sec]
1	1	1	4/f_{OSC3}
1	1	0	2/f_{OSC3}
1	0	1	1/f_{OSC3}
1	0	0	4096/f_{OSC1}
0	1	1	2048/f_{OSC1}
0	1	0	512/f_{OSC1}
0	0	1	128/f_{OSC1}
0	0	0	None

CTK02L	CTK01L	CTK00L	Check time [sec]
1	1	1	4/f_{OSC3}
1	1	0	2/f_{OSC3}
1	0	1	1/f_{OSC3}
1	0	0	4096/f_{OSC1}
0	1	1	2048/f_{OSC1}
0	1	0	512/f_{OSC1}
0	0	1	128/f_{OSC1}
0	0	0	None

Table 5.1.1(l) I/O Memory map (00FF5AH–00FF63H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF5A	D7	IFLK07	K07 input I/F level select register	CMOS Schmitt	CMOS level	0	R/W	
	D6	IFLK06	K06 input I/F level select register					
	D5	IFLK05	K05 input I/F level select register					
	D4	IFLK04	K04 input I/F level select register					
	D3	IFLK03	K03 input I/F level select register					
	D2	IFLK02	K02 input I/F level select register					
	D1	IFLK01	K01 input I/F level select register					
	D0	IFLK00	K00 input I/F level select register					
00FF5C	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	KEYR1	Multiple-key entry reset selection KEYR1 KEYR0 Ports used 1 1 K00–K03 1 0 K00–K02 0 1 K00–K01 0 0 Not used			0	R/W	
	D0	KEYR0				0	R/W	
00FF60	D7	IOC07	P07 I/O control register	Output	Input	0	R/W	
	D6	IOC06	P06 I/O control register					
	D5	IOC05	P05 I/O control register					
	D4	IOC04	P04 I/O control register					
	D3	IOC03	P03 I/O control register					
	D2	IOC02	P02 I/O control register					
	D1	IOC01	P01 I/O control register					
	D0	IOC00	P00 I/O control register					
00FF61	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register					
	D5	IOC15	P15 I/O control register					
	D4	IOC14	P14 I/O control register					
	D3	IOC13	P13 I/O control register					
	D2	IOC12	P12 I/O control register					
	D1	IOC11	P11 I/O control register					
	D0	IOC10	P10 I/O control register					
00FF62	D7	P07D	P07 I/O port data	High	Low	1	R/W	
	D6	P06D	P06 I/O port data					
	D5	P05D	P05 I/O port data					
	D4	P04D	P04 I/O port data					
	D3	P03D	P03 I/O port data					
	D2	P02D	P02 I/O port data					
	D1	P01D	P01 I/O port data					
	D0	P00D	P00 I/O port data					
00FF63	D7	P17D	P17 I/O port data	High	Low	1	R/W	
	D6	P16D	P16 I/O port data					
	D5	P15D	P15 I/O port data					
	D4	P14D	P14 I/O port data					
	D3	P13D	P13 I/O port data					
	D2	P12D	P12 I/O port data					
	D1	P11D	P11 I/O port data					
	D0	P10D	P10 I/O port data					

Table 5.1.1(m) I/O Memory map (00FF64H–00FF6CH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF64	D7	PULP07	P07 pull-up control register	On	Off	1	R/W	
	D6	PULP06	P06 pull-up control register					
	D5	PULP05	P05 pull-up control register					
	D4	PULP04	P04 pull-up control register					
	D3	PULP03	P03 pull-up control register					
	D2	PULP02	P02 pull-up control register					
	D1	PULP01	P01 pull-up control register					
	D0	PULP00	P00 pull-up control register					
00FF65	D7	PULP17	P17 pull-up control register	On	Off	1	R/W	
	D6	PULP16	P16 pull-up control register					
	D5	PULP15	P15 pull-up control register					
	D4	PULP14	P14 pull-up control register					
	D3	PULP13	P13 pull-up control register					
	D2	PULP12	P12 pull-up control register					
	D1	PULP11	P11 pull-up control register					
	D0	PULP10	P10 pull-up control register					
00FF67	D7	IFLP17	P17 input I/F level select register	CMOS Schmitt	CMOS level	0	R/W	
	D6	IFLP16	P16 input I/F level select register					
	D5	IFLP15	P15 input I/F level select register					
	D4	IFLP14	P14 input I/F level select register					
	D3	IFLP13	P13 input I/F level select register					
	D2	IFLP12	P12 input I/F level select register					
	D1	IFLP11	P11 input I/F level select register					
	D0	IFLP10	P10 input I/F level select register					
00FF68	D7	IOC27	P27 I/O control register	Output	Input	0	R/W	
	D6	IOC26	P26 I/O control register					
	D5	IOC25	P25 I/O control register					
	D4	IOC24	P24 I/O control register					
	D3	IOC23	P23 I/O control register					
	D2	IOC22	P22 I/O control register					
	D1	IOC21	P21 I/O control register					
	D0	IOC20	P20 I/O control register					
00FF6A	D7	P27D	P27 I/O port data	High	Low	1	R/W	
	D6	P26D	P26 I/O port data					
	D5	P25D	P25 I/O port data					
	D4	P24D	P24 I/O port data					
	D3	P23D	P23 I/O port data					
	D2	P22D	P22 I/O port data					
	D1	P21D	P21 I/O port data					
	D0	P20D	P20 I/O port data					
00FF6C	D7	PULP27	P27 pull-up control register	On	Off	1	R/W	
	D6	PULP26	P26 pull-up control register					
	D5	PULP25	P25 pull-up control register					
	D4	PULP24	P24 pull-up control register					
	D3	PULP23	P23 pull-up control register					
	D2	PULP22	P22 pull-up control register					
	D1	PULP21	P21 pull-up control register					
	D0	PULP20	P20 pull-up control register					

Table 5.1.1(n) I/O Memory map (00FF6EH–00FFB4H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF6E	D7	IFLP27	P27 input I/F level select register	CMOS Schmitt	CMOS level	0	R/W	
	D6	IFLP26	P26 input I/F level select register					
	D5	IFLP25	P25 input I/F level select register					
	D4	IFLP24	P24 input I/F level select register					
	D3	IFLP23	P23 input I/F level select register					
	D2	IFLP22	P22 input I/F level select register					
	D1	IFLP21	P21 input I/F level select register					
	D0	IFLP20	P20 input I/F level select register					
00FFB0	D7	MODE16_C	PTM4–5 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_C	External clock 2 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN4	PTM4 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET4	PTM4 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL4	PTM4 input clock selection	External clock	Internal clock	0	R/W	
00FFB1	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN5	PTM5 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET5	PTM5 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL5	PTM5 input clock selection	External clock	Internal clock	0	R/W	
00FFB2	D7	RDR47	PTM4 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR46	PTM4 reload data D6					
	D5	RDR45	PTM4 reload data D5					
	D4	RDR44	PTM4 reload data D4					
	D3	RDR43	PTM4 reload data D3					
	D2	RDR42	PTM4 reload data D2					
	D1	RDR41	PTM4 reload data D1					
	D0	RDR40	PTM4 reload data D0 (LSB)					
00FFB3	D7	RDR57	PTM5 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR56	PTM5 reload data D6					
	D5	RDR55	PTM5 reload data D5					
	D4	RDR54	PTM5 reload data D4					
	D3	RDR53	PTM5 reload data D3					
	D2	RDR52	PTM5 reload data D2					
	D1	RDR51	PTM5 reload data D1					
	D0	RDR50	PTM5 reload data D0 (LSB)					
00FFB4	D7	CDR47	PTM4 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR46	PTM4 compare data D6					
	D5	CDR45	PTM4 compare data D5					
	D4	CDR44	PTM4 compare data D4					
	D3	CDR43	PTM4 compare data D3					
	D2	CDR42	PTM4 compare data D2					
	D1	CDR41	PTM4 compare data D1					
	D0	CDR40	PTM4 compare data D0 (LSB)					

Table 5.1.1(o) I/O Memory map (00FFB5H–00FFBAH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FFB5	D7	CDR57	PTM5 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR56	PTM5 compare data D6					
	D5	CDR55	PTM5 compare data D5					
	D4	CDR54	PTM5 compare data D4					
	D3	CDR53	PTM5 compare data D3					
	D2	CDR52	PTM5 compare data D2					
	D1	CDR51	PTM5 compare data D1					
	D0	CDR50	PTM5 compare data D0 (LSB)					
00FFB6	D7	PTM47	PTM4 data D7 (MSB)	High	Low	1	R	
	D6	PTM46	PTM4 data D6					
	D5	PTM45	PTM4 data D5					
	D4	PTM44	PTM4 data D4					
	D3	PTM43	PTM4 data D3					
	D2	PTM42	PTM4 data D2					
	D1	PTM41	PTM4 data D1					
	D0	PTM40	PTM4 data D0 (LSB)					
00FFB7	D7	PTM57	PTM5 data D7 (MSB)	High	Low	1	R	
	D6	PTM56	PTM5 data D6					
	D5	PTM55	PTM5 data D5					
	D4	PTM54	PTM5 data D4					
	D3	PTM53	PTM5 data D3					
	D2	PTM52	PTM5 data D2					
	D1	PTM51	PTM5 data D1					
	D0	PTM50	PTM5 data D0 (LSB)					
00FFB8	D7	MODE16_D	PTM6–7 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_D	External clock 3 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN6	PTM6 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET6	PTM6 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL6	PTM6 input clock selection	External clock	Internal clock	0	R/W	
00FFB9	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN7	PTM7 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET7	PTM7 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL7	PTM7 input clock selection	External clock	Internal clock	0	R/W	
00FFBA	D7	RDR67	PTM6 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR66	PTM6 reload data D6					
	D5	RDR65	PTM6 reload data D5					
	D4	RDR64	PTM6 reload data D4					
	D3	RDR63	PTM6 reload data D3					
	D2	RDR62	PTM6 reload data D2					
	D1	RDR61	PTM6 reload data D1					
	D0	RDR60	PTM6 reload data D0 (LSB)					

Table 5.1.1(p) I/O Memory map (00FFBBH–00FFBFH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FFBB	D7	RDR77	PTM7 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR76	PTM7 reload data D6					
	D5	RDR75	PTM7 reload data D5					
	D4	RDR74	PTM7 reload data D4					
	D3	RDR73	PTM7 reload data D3					
	D2	RDR72	PTM7 reload data D2					
	D1	RDR71	PTM7 reload data D1					
	D0	RDR70	PTM7 reload data D0 (LSB)					
00FFBC	D7	CDR67	PTM6 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR66	PTM6 compare data D6					
	D5	CDR65	PTM6 compare data D5					
	D4	CDR64	PTM6 compare data D4					
	D3	CDR63	PTM6 compare data D3					
	D2	CDR62	PTM6 compare data D2					
	D1	CDR61	PTM6 compare data D1					
	D0	CDR60	PTM6 compare data D0 (LSB)					
00FFBD	D7	CDR77	PTM7 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR76	PTM7 compare data D6					
	D5	CDR75	PTM7 compare data D5					
	D4	CDR74	PTM7 compare data D4					
	D3	CDR73	PTM7 compare data D3					
	D2	CDR72	PTM7 compare data D2					
	D1	CDR71	PTM7 compare data D1					
	D0	CDR70	PTM7 compare data D0 (LSB)					
00FFBE	D7	PTM67	PTM6 data D7 (MSB)	High	Low	1	R	
	D6	PTM66	PTM6 data D6					
	D5	PTM65	PTM6 data D5					
	D4	PTM64	PTM6 data D4					
	D3	PTM63	PTM6 data D3					
	D2	PTM62	PTM6 data D2					
	D1	PTM61	PTM6 data D1					
	D0	PTM60	PTM6 data D0 (LSB)					
00FFBF	D7	PTM77	PTM7 data D7 (MSB)	High	Low	1	R	
	D6	PTM76	PTM7 data D6					
	D5	PTM75	PTM7 data D5					
	D4	PTM74	PTM7 data D4					
	D3	PTM73	PTM7 data D3					
	D2	PTM72	PTM7 data D2					
	D1	PTM71	PTM7 data D1					
	D0	PTM70	PTM7 data D0 (LSB)					

5.2 System Controller

The system controller is a management unit that controls memory access according to the CPU mode. The following conditions must be set with software according to the program area size:

(1) CPU mode
(2) Page address of the stack pointer

Below is a description of the how these settings are to be made.

Note: It is not necessary to change the initialized values when the S1C8F626 is used in minimum CPU mode. However, to clear the interrupt mask that was set at initial reset to disable all interrupts, data must be written to the addresses (FF00H and FF01H) of the system controller registers.

5.2.1 Setting the CPU mode

The S1C8F626 has two CPU modes (minimum mode and maximum mode) and it should be set according to the program size using the CPUMOD register.

• Minimum mode (CPUMOD = "0")

Use the IC in minimum mode when the program size is less than 64K bytes and the program area described below is used.

Configuration 1: ROM area 1 (48K bytes from 0H to BFFFH) only is used

Bank 0 (0H to 7FFFH) and Bank 1 (8000H to BFFFH) are used in this configuration, so set 1 (Bank 1) to the CB register.

Configuration 2: Bank 0 in ROM area 1 (32K bytes from 0H to 7FFFH) and one bank (32K bytes) in ROM area 2 (10000H to 3FFFFH) are used

Set the bank number (one of 2 to 7) to be used as a program area to the CB register. In this configuration, Bank 1 (16K bytes in ROM area 1, 8000H to BFFFH) cannot be used as a program area.

This mode does not save the CB register contents on the stack when a subroutine is called. It makes it possible to economize on stack area usage.

• Maximum mode (CPUMOD = "1")

The entire ROM can be used as a program area in this mode, note, however, that the CB register must be modified every time the program sequence moves to another bank from the currently executed bank to access areas exceeding 64K bytes. The maximum mode saves the CB register contents on the stack when a subroutine is called.

5.2.2 Setting the stack page

By using the stack pointer SP, any area in the RAM can be allocated to the stack used to save register contents when subroutines are called. However, the stack page address must be set using the SPP0–SPP7 registers in the I/O memory.

The SPP0–SPP7 registers are set to "00H" (page 0) at initial reset and this IC does not need to change the address. However, write "00H" to these registers after an initial reset to clear interrupt mask.

To place the stack area at the end of the internal RAM, the stack pointer SP should be initialized to "F800H". (SP is pre-decremented.)

* A page is each recurrent 64K division of data memory beginning at address zero.

5.2.3 Control of system controller

Table 5.2.3.1 shows the control bits for the system controller.

Table 5.2.3.1 System controller control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00	D7	–	–	–	–	–		"0" when being read
	D6	CPUMOD	CPU mode	Maximum	Minimum	0	R/W	
	D5	–	–	–	–	–		Constantly "0" when being read
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF01	D7	SPP7	Stack pointer page address (MSB)	1	0	0	R/W	
	D6	SPP6		1	0	0	R/W	
	D5	SPP5		1	0	0	R/W	
	D4	SPP4		1	0	0	R/W	
	D3	SPP3		1	0	0	R/W	
	D2	SPP2		1	0	0	R/W	
	D1	SPP1		1	0	0	R/W	
	D0	SPP0	(LSB)	1	0	0	R/W	

CPUMOD: 00FF00H•D6

Sets the CPU mode.

When "1" is written: Maximum mode
When "0" is written: Minimum mode
Reading: Valid

Set the IC in minimum mode when the program size is 64K bytes or less, or maximum mode when the size exceeds 64K bytes.
At initial reset, this register is set to "0" (minimum mode).

SPP0–SPP7: 00FF01H

Sets the page address of stack area.
At initial reset, this register is set to "00H" (page 0).

Note: To avoid a malfunction from an interrupt generated before initialization, all interrupts including $\overline{NMI}$ are disabled, until data is written to addresses 00FF00H and 00FF01H. Furthermore, to avoid generating an interrupt while the stack area is being set, all interrupts including $\overline{NMI}$ are disabled in one instruction execution period after writing to address 00FF01H.

5.2.4 Programming note

All the interrupts including $\overline{NMI}$ are masked, until data is written to addresses 00FF00H and 00FF01H. Therefore, write data to these addresses in the initialize routine even if it is not necessary to change the contents (initial values).

5.3 Watchdog Timer

5.3.1 Configuration of watchdog timer

The S1C8F626 is equipped with a watchdog timer driven by OSC1 as source oscillation. The watchdog timer must be reset periodically in software, and if reset of more than 131072 / fOSC1 seconds (4 seconds when fOSC1 = 32.768 kHz) does not take place, a non-maskable interrupt signal is generated and output to the CPU. The watchdog timer starts operating after initial reset, however, it can be stopped by the software.

Figure 5.3.1.1 is a block diagram of the watchdog timer.

By running watchdog timer reset during the main routine of the program, it is possible to detect program runaway as if watchdog timer processing had not been applied. Normally, this routine is integrated at points that are regularly being processed.

The watchdog timer continues to operate during HALT and when a HALT state is continuous for longer than 131072 / fOSC1 seconds, the CPU shifts to exception processing.
During SLEEP, the watchdog timer is stopped.

5.3.2 Interrupt function

In cases where the watchdog timer is not periodically reset in software, the watchdog timer outputs an interrupt signal to the CPU's $\overline{\text{NMI}}$ (level 4) input. Unmaskable and taking priority over other interrupts, this interrupt triggers the generation of exception processing. See the "S1C88 Core CPU Manual" for more details on $\overline{\text{NMI}}$ exception processing.
This exception processing vector is set at 000004H.

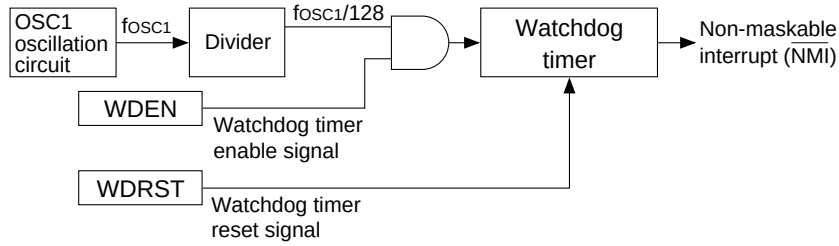


Fig. 5.3.1.1 Block diagram of watchdog timer

5.3.3 Control of watchdog timer

Table 5.3.3.1 shows the control bits for the watchdog timer.

Table 5.3.3.1 Watchdog timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	WDEN	Watchdog timer enable	Enable	Disable	1	R/W	
	D6	FOUT2	FOUT frequency selection			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	

FOUT2	FOUT1	FOUT0	Frequency
1	1	1	f_{OSC3} / 8
1	1	0	f_{OSC3} / 4
1	0	1	f_{OSC3} / 2
1	0	0	f_{OSC3} / 1
0	1	1	f_{OSC1} / 8
0	1	0	f_{OSC1} / 4
0	0	1	f_{OSC1} / 2
0	0	0	f_{OSC1} / 1

WDEN: 00FF40H•D7

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt ($\overline{NMI}$).
At initial reset, this register is set to "1".

WDRST: 00FF40H•D2

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" to WDRST, the watchdog timer is reset, after which it is immediately restarted.
Writing "0" will mean no operation.
Since WDRST is for writing only, it is constantly set to "0" during readout.

5.3.4 Programming notes

(1) When the watchdog timer is being used, the software must reset it within 4-second cycles (when f_{OSC1} is 32.768 kHz).

(2) Do not execute the SLP instruction for 2 msec after a $\overline{NMI}$ interrupt has occurred (when f_{OSC1} is 32.768 kHz).

(3) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt ($\overline{NMI}$) if it is not used.

5.4 Oscillation Circuits and Operating Mode

5.4.1 Configuration of oscillation circuits

The S1C8F626 is twin clock system with two internal oscillation circuits (OSC1 and OSC3). The OSC3 oscillation circuit generates the main-clock (Max. 8.2 MHz) to run the CPU and some peripheral circuits in high speed, and the OSC1 oscillation circuit generates the sub-clock (Typ. 32.768 kHz) for low-power operation.
Figure 5.4.1.1 shows the configuration of the oscillation circuit.

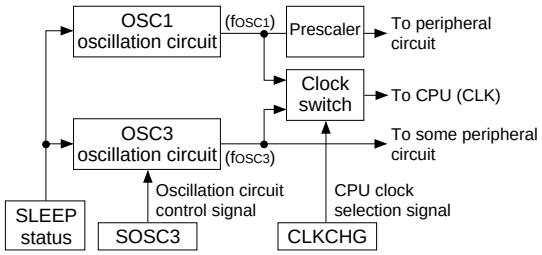


Fig. 5.4.1.1 Configuration of oscillation circuits

At initial reset, OSC3 oscillation circuit is selected for the CPU operating clock. ON / OFF switching of the OSC3 oscillation circuit and switching of the system clock between OSC3 and OSC1 are controlled in software. OSC3 circuit is utilized when high speed operation of the CPU and some peripheral circuits become necessary. Otherwise, OSC1 should be used to generate the operating clock and OSC3 circuit placed in a stopped state in order to reduce current consumption.

5.4.2 Mask option

The S1C8F626 has two optional configurations (Configuration 1 and Configuration 2) as shown in Table 5.4.2.1 allowing selection of oscillator types of the built-in oscillation circuit.

Table 5.4.2.1 S1C8F626 optional configurations

Option	OSC1 oscillation circuit	OSC3 oscillation circuit
Configuration 1	Crystal	Crystal/Ceramic
Configuration 2	Crystal	CR

5.4.3 OSC1 oscillation circuit

The OSC1 oscillation circuit generates the 32.768 kHz (Typ.) system clock which is utilized during low speed operation (low power mode) of the CPU and peripheral circuits. Furthermore, even when OSC3 is utilized as the system clock, OSC1 continues to generate the source clock for the clock timer and stopwatch timer.
This oscillation circuit stops when the SLP instruction is executed.
Figure 5.4.3.1 shows the configuration of the OSC1 oscillation circuit.

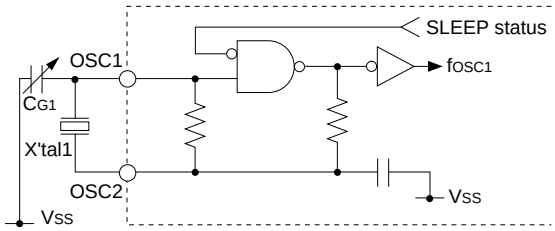
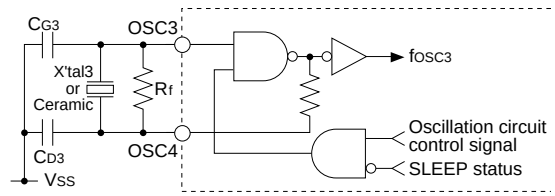


Fig. 5.4.3.1 OSC1 oscillation circuit (crystal oscillation)

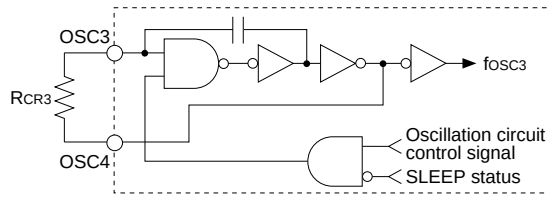
A crystal oscillation circuit can be easily formed by connecting a crystal oscillator X'tal1 (Typ. 32.768 kHz) between the OSC1 and OSC2 terminals along with a trimmer capacitor C_{G1} (0–25 pF) between the OSC1 terminal and V_{SS}.

5.4.4 OSC3 oscillation circuit

The OSC3 oscillation circuit generates the system clock when the CPU and some peripheral circuits are in high speed operation.
This oscillation circuit stops when the SLP instruction is executed, or the SOSC3 register is set to "0".
In terms of oscillation circuit types, either crystal / ceramic oscillation or CR oscillation can be selected by option.
Figure 5.4.4.1 shows the configuration of the OSC3 oscillation circuit.



(1) Crystal/Ceramic oscillation circuit



(2) CR oscillation circuit

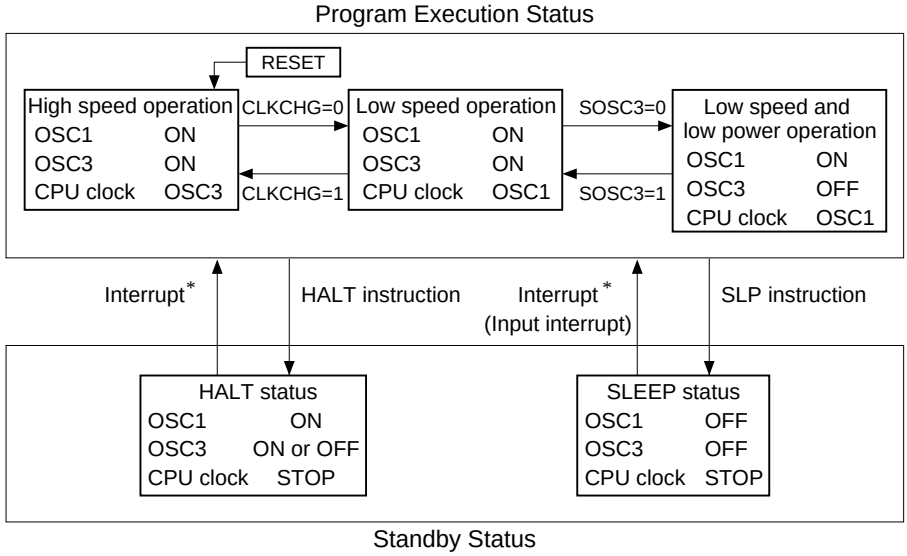
Fig. 5.4.4.1 OSC3 oscillation circuit

When crystal or ceramic oscillation circuit is selected, the crystal or ceramic oscillation circuit (Max. 8.2 MHz) are formed by connecting either a crystal oscillator (X'tal3) or a combination of ceramic oscillator (Ceramic) and feedback resistor (Rf) between OSC3 and OSC4 terminals and connecting two capacitors (C_{G3}, C_{D3}) between the OSC3 terminal and V_{SS}, and between the OSC4 terminal and V_{SS}, respectively.
When CR oscillation is selected, the CR oscillation circuit (Max. 2.2 MHz) is formed merely by connecting a resistor (R_{CR3}) between OSC3 and OSC4 terminals.

5.4.5 Switching the CPU clocks

You can use either OSC1 or OSC3 as the system clock for the CPU and you can switch over by means of software.
You can save power by turning the OSC3 oscillation circuit off while the CPU is operating in OSC1. When you must operate on OSC3, you can change to high speed operation by turning the OSC3 oscillation circuit ON and switching over the system clock.
In this case, since several tens of µsec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit ON, you should switch over the clock after stabilization time has elapsed.
When switching over from the OSC3 to the OSC1, turn the OSC3 oscillation circuit OFF immediately following the clock changeover.
When switching the system clock from OSC3 to OSC1 immediately after the power is turned on, it is necessary to wait for the OSC1 oscillation to stabilize before the clock can be switched. The OSC1 oscillation may take several tens of msec to several seconds until it has completely stabilized. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 9, "ELECTRICAL CHARACTERISTICS".)

Figure 5.4.5.1 indicates the status transition diagram for the clock changeover.



* The return destination from the standby status becomes the program execution status prior to shifting to the standby status.

Fig. 5.4.5.1 Status transition diagram for the clock changeover

5.4.6 Switching the operating mode

The S1C8F626 has two operating modes.

1. Normal operation mode
   This mode executes the program stored in the Flash EEPROM (normal operation).
   V_{DD} = 1.8 to 3.6 V,
   internal operating voltage V_{D1} = 1.8 V
2. Flash programming mode
   This mode is provided for erasing or programming the Flash EEPROM.
   V_{DD} = 2.7 to 3.6 V,
   internal operating voltage V_{D1} = 2.5 V

The internal operating voltage V_{D1} must be switched according to the mode as shown above using the VDC register. Normally the VDC register does not need to change from the default value "0" (V_{D1} = 1.8 V). Also control of the VDC register is unnecessary when the operating clock is switched. The VDC register must be set to "1" only when programming the Flash EEPROM.

Notes:
- *Before the Flash EEPROM can be programmed, a maximum 5 msec of wait time is required for the internal operating voltage to stabilize after switching the operating mode. Also when returning the IC to normal operation mode, be sure to take this wait time before setting the VDC register to "0".*
- *Setting the VDC register to "1" increases current consumption. Be sure to reset the VDC register to "0" after Flash EEPROM programming has finished.*

5.4.7 Control of oscillation circuit and operating mode

Table 5.4.7.1 shows the control bits for the oscillation circuit and operating mode.

SOSC3: 00FF02H•D2

Controls the ON and OFF settings of the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When the CPU and some peripheral circuits are to be operated at high speed, SOSC3 is to be set to "1". At all other times, it should be set to "0" in order to reduce current consumption.
At initial reset, SOSC3 is set to "1" (OSC3 oscillation ON).

CLKCHG: 00FF02H•D3

Selects the operating clock for the CPU.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

When the operating clock for the CPU is switched to OSC3, CLKCHG should be set to "1" and when the clock is switched to OSC1, CLKCHG should be set to "0".
At initial reset, CLKCHG is set to "1" (OSC3 clock).

VDC: 00FF02H•D0

Selects a V_{D1} internal operating voltage value (operating mode).

When "1" is written: 2.5 V (Flash programming mode)
When "0" is written: 1.8 V (Normal operation mode)
Reading: Valid

Set VDC to "0" (V_{D1} = 1.8 V) for normal operation. Before programming the Flash EEPROM, write "1" to VDC to set the V_{D1} voltage to 2.5 V.
At initial reset, this register is set to "0" (normal operation mode).

Table 5.4.7.1 Oscillation circuit and operating mode control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF02	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	1		
	D2	SOSC3	OSC3 oscillation On/Off control	On	Off	1		
	D1	–	–	–	–	–		"0" when being read
	D0	VDC	Operating mode selection	V_{D1} = 2.5 V	V_{D1} = 1.8 V	0		

5.4.8 Programming notes

(1) When the high speed CPU operation is not necessary, you should operate the peripheral circuits according to the setting outline indicate below.
- CPU operating clock OSC1
- OSC3 oscillation circuit OFF

(When the OSC3 clock is not necessary for some peripheral circuits.)

(2) Since several tens of µsec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit ON. Consequently, you should switch the CPU operating clock (OSC1 → OSC3) after allowing for a sufficient waiting time once the OSC3 oscillation goes ON. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 9, "ELECTRICAL CHARACTERISTICS".)

(3) When switching the clock from OSC3 to OSC1, be sure to switch OSC3 oscillation OFF with separate instructions. Using a single instruction to process simultaneously can cause a malfunction of the CPU.

(4) When switching the system clock from OSC3 to OSC1 immediately after the power is turned on, it is necessary to wait the OSC1 oscillation to stabilize before the clock can be switched. The OSC1 oscillation takes several tens of msec to several seconds until it has completely stabilized. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 9, "ELECTRICAL CHARACTERISTICS".)

(5) Before the Flash EEPROM can be programmed, a maximum 5 msec of wait time is required for the internal operating voltage to stabilize after switching the operating mode. Also when returning the IC to normal operation mode, be sure to take this wait time before setting the VDC register to "0".

(6) Setting the VDC register to "1" increases current consumption. Be sure to reset the VDC register to "0" after Flash EEPROM programming has finished.

5.5 Input Ports (K ports)

5.5.1 Configuration of input ports

The S1C8F626 is equipped with 8 input port bits (K00–K07) all of which are usable as general purpose input port terminals with interrupt function.
K04–K07 terminals doubles as the external clock (EXCL0–EXCL3) input terminal of the programmable timer (event counter) with input port functions sharing the input signal as is (see "5.10 Programmable Timer").
The K00–K03 input port can be used for multiple-key entry reset (see "4.1.2 Simultaneous LOW level input at input port terminals K00–K03"). When the multiple-key entry reset function is used, a port combination used for resetting can be selected with software.
Figure 5.5.1.1 shows the structure of the input port.

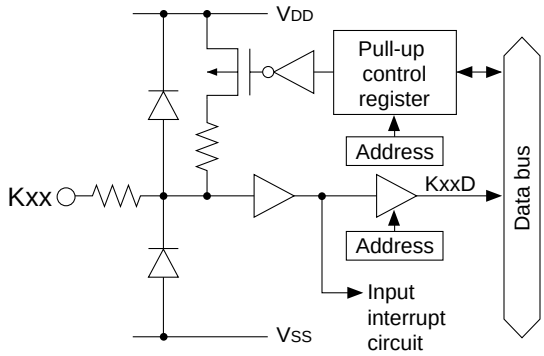


Fig. 5.5.1.1 Structure of input port

Each input port terminal is directly connected via a three-state buffer to the data bus. Furthermore, the input signal state at the instant of input port readout is read in that form as data.

5.5.2 Input interface level

The S1C8F626 input ports allow software to select an input interface level. When the input I/F level select register IFLK0x is set to "0", the corresponding input port is configured with a CMOS level interface. When IFLK0x is set to "1", the port is configured with a CMOS Schmitt level interface. At initial reset, all the ports are configured with a CMOS level interface.

5.5.3 Pull-up control

The S1C8F626 input ports have a built-in pull-up resistor and the resistor in each port is enabled or disabled with software.
The pull-up resistor becomes effective by writing "1" to the pull-up control register PULK0x that corresponds to each port, and the input line is pulled up. When "0" has been written, no pull-up is done.
At initial reset, the pull-up control register is set to "1" (pulled up).

The input port with a pull-up resistor suits input from the push switch and key matrix.

When changing the input terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an input port. In particular, special attention should be paid to key scan for key matrix formation. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

The input port without a pull-up resistor is suits for slide switch input and interfacing with other LSIs. In this case, take care that a floating state does not occur in input.

For unused ports, enable pull-up using the pull-up control registers.

5.5.4 Interrupt function and input comparison register

All the input ports (K00–K07) provide the interrupt functions. The conditions for issuing an interrupt can be set by the software.
When the interrupt generation condition set for a terminal is met, the interrupt factor flag FK00–FK07 corresponding to the terminal is set at "1" and an interrupt is generated.
Interrupt can be prohibited by setting the interrupt enable registers EK00–EK07 for the corresponding interrupt factor flags.
Furthermore, the priority level for input interrupt can be set at the desired level (0–3) using the interrupt priority registers PK00–PK01.
For details on the interrupt control registers for the above and on operations subsequent to interrupt generation, see "5.14 Interrupt and Standby Status".

The exception processing vectors for each interrupt factor are set as follows:

K07 input: 000006H	K03 input: 00000EH
K06 input: 000008H	K02 input: 000010H
K05 input: 00000AH	K01 input: 000012H
K04 input: 00000CH	K00 input: 000014H

Figure 5.5.4.1 shows the configuration of the input interrupt circuit. The input comparison register KCP selects whether the interrupt for each input port will be generated on the rising edge or the falling edge of input. When the K0x input signal changes to the status set by the input comparison register KCP0x, the interrupt factor flag FK0x is set to "1" and an interrupt occurs. The input port has a chattering-eliminate circuit that checks input level to avoid unnecessary interrupt generation due to chattering. There are two separate chattering-eliminate circuits for K00–K03 and K04–K07 and they can be set up individually. The CTK00x–CTK02x registers allow selection of signal level check time as shown in Table 5.5.4.1.

Table 5.5.4.1 Setting the input level check time

CTK02x	CTK01x	CTK00x	Check time (*)
1	1	1	4/fOSC3 (2 µs)
1	1	0	2/fOSC3 (1 µs)
1	0	1	1/fOSC3 (0.5 µs)
1	0	0	4096/fOSC1 (128 ms)
0	1	1	2048/fOSC1 (64 ms)
0	1	0	512/fOSC1 (16 ms)
0	0	1	128/fOSC1 (4 ms)
0	0	0	None –

*: When OSC1 = 32 kHz, OSC3 = 2 MHz

Notes:
- *Input interrupts cannot be accepted in SLEEP mode if the CPU enters SLEEP mode when the chattering-eliminate circuit is active. The chattering-eliminate circuit should be turned OFF (CTP2x = "000") before executing the SLP instruction.*
- *Be sure to disable interrupts before changing the contents of the CTK0x register. Unnecessary interrupts may occur if the register is changed when the corresponding input port interrupts have been enabled by the interrupt enable register EK0x.*
- *The chattering-eliminate check time means the maximum pulse width that can be eliminated. The valid interrupt input needs a pulse width of the set check time (minimum) to twice that of the check time (maximum).*
- *The internal signal may oscillate if the rise / fall time of the input signal is too long because the input signal level transition to the threshold level duration of time is too long. This causes the input interrupt to malfunction, therefore setup the input signal so that the rise/fall time is 25 nsec or less.*

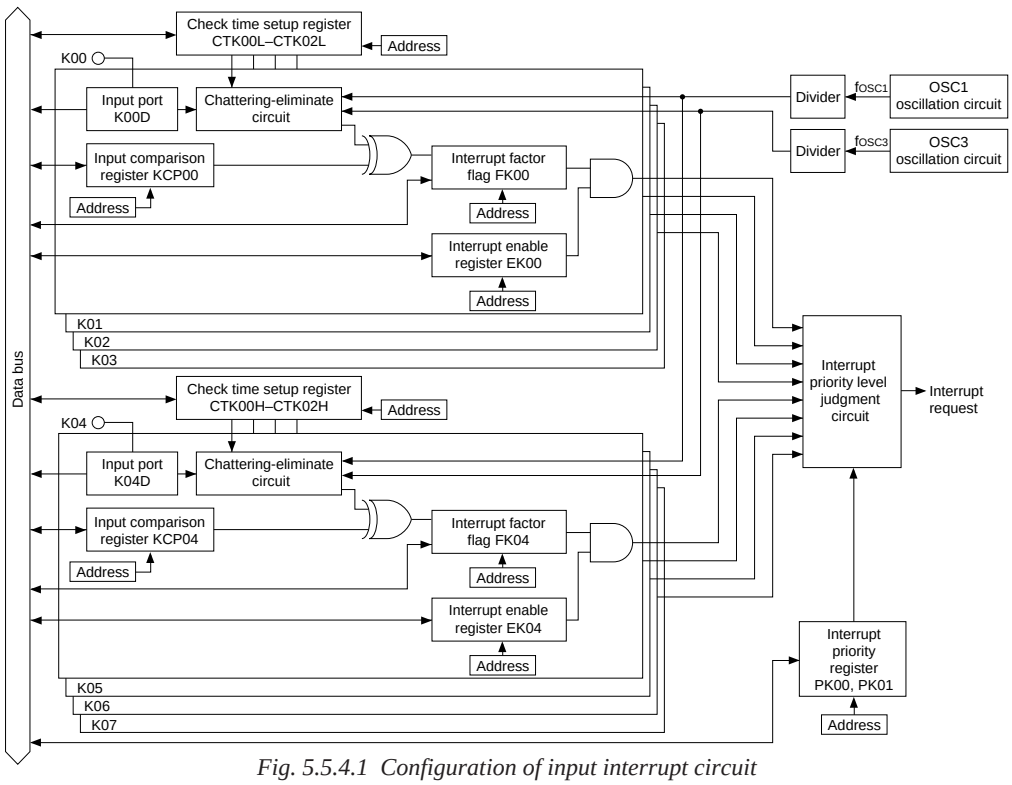


Fig. 5.5.4.1 Configuration of input interrupt circuit

5.5.5 Control of input ports

Table 5.5.5.1 shows the input port control bits.

Table 5.5.5.1(a) Input port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF52	D7	KCP07	K07 input comparison register	Interrupt generated at falling edge	Interrupt generated at rising edge	1	R/W	
	D6	KCP06	K06 input comparison register					
	D5	KCP05	K05 input comparison register					
	D4	KCP04	K04 input comparison register					
	D3	KCP03	K03 input comparison register					
	D2	KCP02	K02 input comparison register					
	D1	KCP01	K01 input comparison register					
	D0	KCP00	K00 input comparison register					
00FF54	D7	K07D	K07 input port data	High level input	Low level input	–	R	
	D6	K06D	K06 input port data					
	D5	K05D	K05 input port data					
	D4	K04D	K04 input port data					
	D3	K03D	K03 input port data					
	D2	K02D	K02 input port data					
	D1	K01D	K01 input port data					
	D0	K00D	K00 input port data					
00FF56	D7	PULK07	K07 pull-up control register	On	Off	1	R/W	
	D6	PULK06	K06 pull-up control register					
	D5	PULK05	K05 pull-up control register					
	D4	PULK04	K04 pull-up control register					
	D3	PULK03	K03 pull-up control register					
	D2	PULK02	K02 pull-up control register					
	D1	PULK01	K01 pull-up control register					
	D0	PULK00	K00 pull-up control register					
00FF58	D7	–	–	–	–	–		"0" when being read
	D6	CTK02H	K04–K07 port chattering-eliminate setup (Input level check time)			0	R/W	
	D5	CTK01H				0	R/W	
	D4	CTK00H				0	R/W	
	D3	–	–	–	–	–		"0" when being read
	D2	CTK02L	K00–K03 port chattering-eliminate setup (Input level check time)			0	R/W	
	D1	CTK01L				0	R/W	
	D0	CTK00L				0	R/W	

K04–K07 port chattering-eliminate setup (Input level check time)

CTK02H	CTK01H	CTK00H	Check time [sec]
1	1	1	4/f_{OSC3}
1	1	0	2/f_{OSC3}
1	0	1	1/f_{OSC3}
1	0	0	4096/f_{OSC1}
0	1	1	2048/f_{OSC1}
0	1	0	512/f_{OSC1}
0	0	1	128/f_{OSC1}
0	0	0	None

K00–K03 port chattering-eliminate setup (Input level check time)

CTK02L	CTK01L	CTK00L	Check time [sec]
1	1	1	4/f_{OSC3}
1	1	0	2/f_{OSC3}
1	0	1	1/f_{OSC3}
1	0	0	4096/f_{OSC1}
0	1	1	2048/f_{OSC1}
0	1	0	512/f_{OSC1}
0	0	1	128/f_{OSC1}
0	0	0	None

Table 5.5.5.1(b) Input port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF5A	D7	IFLK07	K07 input I/F level select register	CMOS Schmitt	CMOS level	0	R/W	
	D6	IFLK06	K06 input I/F level select register					
	D5	IFLK05	K05 input I/F level select register					
	D4	IFLK04	K04 input I/F level select register					
	D3	IFLK03	K03 input I/F level select register					
	D2	IFLK02	K02 input I/F level select register					
	D1	IFLK01	K01 input I/F level select register					
	D0	IFLK00	K00 input I/F level select register					
00FF5C	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	KEYR1	Multiple-key entry reset selection KEYR1 KEYR0 Ports used 1 1 K00–K03 1 0 K00–K02 0 1 K00–K01 0 0 Not used			0	R/W	
	D0	KEYR0				0	R/W	
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF01 PSIF00 PSW1 PSW0 PTM1 PTM0 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF01	Serial interface 0 interrupt priority register			0	R/W	
	D4	PSIF00						
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0						
00FF24	D7	EK07	K07 interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	EK06	K06 interrupt enable					
	D5	EK05	K05 interrupt enable					
	D4	EK04	K04 interrupt enable					
	D3	EK03	K03 interrupt enable					
	D2	EK02	K02 interrupt enable					
	D1	EK01	K01 interrupt enable					
	D0	EK00	K00 interrupt enable					
00FF28	D7	FK07	K07 interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D6	FK06	K06 interrupt factor flag					
	D5	FK05	K05 interrupt factor flag					
	D4	FK04	K04 interrupt factor flag					
	D3	FK03	K03 interrupt factor flag					
	D2	FK02	K02 interrupt factor flag					
	D1	FK01	K01 interrupt factor flag					
	D0	FK00	K00 interrupt factor flag					

K00D–K07D: 00FF54H

Input data of input port terminal K0x can be read out.

When "1" is read: HIGH level
When "0" is read: LOW level
Writing: Invalid

The terminal voltage of each of the input port K00–K07 can be directly read out as either a "1" for HIGH (V_{DD}) level or a "0" for LOW (V_{SS}) level. This bit is exclusively for readout and are not usable for write operations.

IFLK00–IFLK07: 00FF5AH

Selects an input interface level.

When "1" is written: CMOS Schmitt level
When "0" is written: CMOS level
Reading: Valid

IFLK0x is the input I/F level select register corresponding to each input port K0x.
When "1" is written to IFLK0x, the corresponding input port K0x is configured with a CMOS Schmitt level interface. When "0" is written, the port is configured with a CMOS level interface.
At initial reset, this register is set to "0" (CMOS level).

PULK00–PULK07: 00FF56H

Controls the input pull-up resistor.

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

PULK0x is the pull-up control register corresponding to the input port K0x that turns the pull-up resistor built into the input port ON and OFF.
When "1" is written to PULK0x, the corresponding input port K0x is pulled up to high. When "0" is written, the input port is not pulled up.
At initial reset, this register is set to "1" (Pull-up ON).

KCP00–KCP07: 00FF52H

Sets the interrupt generation condition (interrupt generation timing) for input port terminals K00–K07.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

KCP0x is the input comparison register which corresponds to the input port K0x. Interrupt in those ports which have been set to "1" is generated on the falling edge of the input and in those set to "0" on the rising edge.
At initial reset, this register is set to "1" (falling edge).

CTK00L–CTK02L: 00FF58H•D0–D2

Sets the input level check time of the chattering-eliminate circuit for the K00–K03 input port interrupts as shown in Table 5.5.5.2.

Table 5.5.5.2 Setting the input level check time

CTK02L	CTK01L	CTK00L	Input level check time [sec]
1	1	1	4/f_{OSC3}
1	1	0	2/f_{OSC3}
1	0	1	1/f_{OSC3}
1	0	0	4096/f_{OSC1}
0	1	1	2048/f_{OSC1}
0	1	0	512/f_{OSC1}
0	0	1	128/f_{OSC1}
0	0	0	None

Be sure to disable interrupts before changing the contents of this register. Unnecessary interrupts may occur if the register is changed when the corresponding input port interrupts have been enabled by the interrupt enable register EK0x.
At initial reset, this register is set to "0" (None).

CTK00H–CTK02H: 00FF58H•D4–D6

Sets the input level check time of the chattering-eliminate circuit for the K04–K07 input port interrupts as shown in Table 5.5.5.3.

Table 5.5.5.3 Setting the input level check time

CTK02H	CTK01H	CTK00H	Input level check time [sec]
1	1	1	4/f_{OSC3}
1	1	0	2/f_{OSC3}
1	0	1	1/f_{OSC3}
1	0	0	4096/f_{OSC1}
0	1	1	2048/f_{OSC1}
0	1	0	512/f_{OSC1}
0	0	1	128/f_{OSC1}
0	0	0	None

Be sure to disable interrupts before changing the contents of this register. Unnecessary interrupt may occur if the register is changed when the corresponding input port interrupts have been enabled by the interrupt enable register EK0x.
At initial reset, this register is set to "0" (None).

PK00, PK01: 00FF20H•D6, D7

Sets the input interrupt priority level. PK00 and PK01 are the interrupt priority registers corresponding to the input interrupts.
Table 5.5.5.4 shows the interrupt priority level which can be set by this register.

Table 5.5.5.4 Interrupt priority level settings

PK01	PK00	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EK00–EK07: 00FF24H

How interrupt generation to the CPU is permitted or prohibited.

When "1" is written: Interrupt permitted
When "0" is written: Interrupt prohibited
Reading: Valid

EK0x is the interrupt enable register which correspond to the input port K0x.
Interrupt is permitted in those terminals set to "1" and prohibited in those set to "0".
At initial reset, this register is set to "0" (interrupt prohibited).

FK00–FK07: 00FF28H

Indicates the generation state for an input interrupt.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Reset factor flag
When "0" is written: Invalid

The interrupt factor flag FK0x corresponds to K0x is set to "1" by the occurrence of an interrupt generation condition.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is all reset to "0".

KEYR0, KEYR1: 00FF5CH•D0, D1

Configures the multiple-key entry reset function.

Table 5.5.5.5 Multiple-key entry reset configuration

KEYR1	KEYR0	Port combination
1	1	K00 & K01 & K02 & K03
1	0	K00 & K01 & K02
0	1	K00 & K01
0	0	Not used

When "Not used" is selected, the multiple-key entry reset function is disabled. When a port combination is selected, the IC will be reset when the selected ports are set to LOW simultaneously.
At initial reset, this register is set to "0" (not used).

5.5.6 Programming notes

(1) When changing the input terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an input port. In particular, special attention should be paid to key scan for key matrix formation. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

(2) Be sure to disable interrupts before changing the contents of the CTK0x register. Unnecessary interrupts may occur if the register is changed when the corresponding input port interrupts have been enabled by the interrupt enable register EK0x.

5.6 I/O Ports (P ports)

5.6.1 Configuration of I/O ports

The S1C8F626 is equipped with 24 bits of I/O ports (P00–P07, P10–P17, P20–P27).
Figure 5.6.1.1 shows the structure of an I/O port.

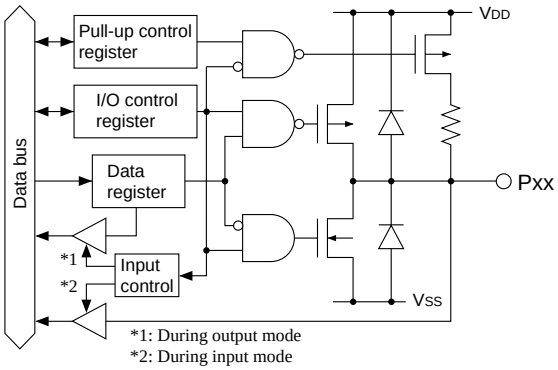


Fig. 5.6.1.1 Structure of I/O port

I/O port can be set for input or output mode in one bit unit. These settings are performed by writing data to the I/O control registers.

I/O port terminals P10–P13 and P20–P23 are shared with input/output terminals of serial interface Ch. 0 and Ch.1, respectively. The function of each terminal is switchable in software. With respect to serial interface see "5.7 Serial Interface".

The data registers and I/O control registers of I/O ports set for serial interface output terminals use are usable as general purpose registers with read/write capabilities which do not affect I/O activities of the terminal.
The same as above, the I/O control register of I/O port set for serial interface input terminal use is usable as general purpose register.

In addition to the general-purpose DC output, special output can be selected for the I/O ports P14–P17 with the software.

5.6.2 I/O control registers and I/O mode

I/O ports are set either to input or output modes by writing data to the I/O control registers IOCxx which correspond to each bit.
To set an I/O port to input mode, write "0" to the I/O control register.
An I/O port which is set to input mode will shift to a high impedance state and functions as an input port.
Readout in input mode consists simply of a direct readout of the input terminal state: the data being "1" when the input terminal is at HIGH (V_{DD}) level and "0" when it is at LOW (V_{SS}) level.
When the built-in pull-up resistor is enabled with the software, the port terminal will be pulled-up to high during input mode.
Even in input mode, data can be written to the data registers without affecting the terminal state.
To set an I/O port to output mode, write "1" to the I/O control register. An I/O port which is set to output mode functions as an output port.
When port output data is "1", a HIGH (V_{DD}) level is output and when it is "0", a LOW (V_{SS}) level is output. Readout in output mode consists of the contents of the data register.
At initial reset, I/O control registers are set to "0" (I/O ports are set to input mode).

5.6.3 Input interface level

The I/O ports P10–P17 and P20–P27 allow software to select an input interface level. When the input I/F level select register IFLPxx is set to "0", the corresponding port is configured with a CMOS level input interface. When IFLPxx is set to "1", the port is configured with a CMOS Schmitt level input interface. At initial reset, all the ports are configured with a CMOS level interface.

5.6.4 Pull-up control

The S1C8F626 I/O ports have a built-in pull-up resistor and the resistor in each port is enabled or disabled with software.
The pull-up resistor becomes effective by writing "1" to the pull-up control register PULPxx that corresponds to each port, and the Pxx terminal is pulled up during the input mode. When "0" has been written, no pull-up is done.
When the port is set in the output mode, the setting of the pull-up control register becomes invalid (no pull-up is done during output).
At initial reset, the pull-up control registers are set to "1" (pulled up).

When changing the port terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

For unused ports, enable pull-up using the pull-up control registers.

5.6.5 Special output

Besides general purpose DC input/output, I/O ports P14–P17 can also be assigned special output functions in software as shown in Table 5.6.5.1.

Table 5.6.5.1 Special output ports

Output port	Special output
P14	TOUT0/TOUT1 output
P15	TOUT2/TOUT3 output
P16	FOUT output
P17	$\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$ output

When using P14–P17 as a special output port, write "1" to the corresponding I/O control register (IOC14–IOC17) to set the port to the output mode.

■ TOUT output (P14, P15)

In order for the S1C8F626 to provide clock signal to an external device, the terminals P14 and P15 can be used to output a TOUTx signal (clock output by the programmable timer).

The output control for the TOUTx signals (x = 0–3) is done by the registers PTOUTx. When PTOUTx is set to "1", the TOUTx signal is output from the corresponding port terminal, when "0" is set, the port is set for DC output. When PTOUTx is "1", settings of the I/O control register IOC14/IOC15 and data register P14D/P15D become invalid.
The TOUT0–TOUT3 signals are generated from the underflow and compare-match signals of the programmable timers 0–3.
With respect to frequency control, see "5.10 Programmable Timer".
Since the TOUTx signals are generated asynchronously from the registers PTOUTx, when the signals are turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 5.6.5.1 shows the output waveform of the TOUT signal.

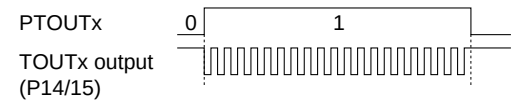


Fig. 5.6.5.1 Output waveform of TOUT signal

Note: If PTOUT0 and PTOUT1 are set to "1" at the same time, PTOUT1 is effective. Similarly, if PTOUT2 and PTOUT3 are set to "1", PTOUT3 is effective.

■ FOUT output (P16)

In order for the S1C8F626 to provide clock signal to an external device, a FOUT signal (oscillation clock fOSC1 or fOSC3 dividing clock) can be output from the P16 port terminal.
The output control for the FOUT signal is done by the register FOUTON. When FOUTON is set to "1", the FOUT signal is output from the P16 port terminal, when "0" is set, the port is set for DC output. When FOUTON is "1", settings of the I/O control register IOC16 and data register P16D become invalid.
The frequency of the FOUT signal can be selected in software by setting the registers FOUT0–FOUT2. The frequency is selected any one from among eight settings as shown in Table 5.6.5.2.

Table 5.6.5.2 FOUT frequency setting

FOUT2	FOUT1	FOUT0	FOUT frequency
1	1	1	fOSC3 / 8
1	1	0	fOSC3 / 4
1	0	1	fOSC3 / 2
1	0	0	fOSC3 / 1
0	1	1	fOSC1 / 8
0	1	0	fOSC1 / 4
0	0	1	fOSC1 / 2
0	0	0	fOSC1 / 1

fOSC1: OSC1 oscillation frequency
fOSC3: OSC3 oscillation frequency

When the FOUT frequency is made "fOSC3 / n", you must turn on the OSC3 oscillation circuit before outputting FOUT. A time interval of several tens of µsec to several tens of msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before turning outputting FOUT. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 9, "ELECTRICAL CHARACTERISTICS".)
Since the FOUT signal is generated asynchronously from the register FOUTON, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 5.6.5.2 shows the output waveform of the FOUT signal.

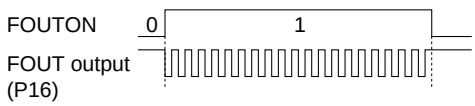


Fig. 5.6.5.2 Output waveform of FOUT signal

■ Inverted TOUT output (P17)

The S1C8F626 provides an output of the TOUT2 or TOUT3 inverted signal (programmable timer output clock) to supply a clock to external devices or to drive a buzzer.
By using this output with the TOUT2 or TOUT3 output from the P15 terminal, the bias level to be applied to the buzzer can be increased.
The output control for the $\overline{\text{TOUTx}}$ signals (x = 2 or 3) is done by the registers RPTOUTx. When RPTOUTx is set to "1", the $\overline{\text{TOUTx}}$ signal is output from the P17 port terminal, when "0" is set, the port is set for DC output. When RPTOUTx is "1", settings of the I/O control register IOC17 and data register P17D become invalid.
The $\overline{\text{TOUT2}}$ and $\overline{\text{TOUT3}}$ signals are generated from the underflow and compare-match signals of the programmable timers 2 and 3.
With respect to frequency control, see "5.10 Programmable Timer".
Since the $\overline{\text{TOUTx}}$ signals are generated asynchronously from the registers RPTOUTx, when the signals are turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 5.6.5.3 shows the output waveform of the $\overline{\text{TOUT}}$ signal.

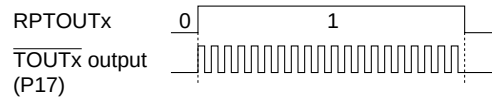


Fig. 5.6.5.3 Output waveform of $\overline{\text{TOUT}}$ signal

Note: If RPTOUT2 and RPTOUT3 are set to "1" at the same time, RPTOUT3 is effective.

5.6.6 Control of I/O ports

Table 5.6.6.1 shows the I/O port control bits.

Table 5.6.6.1(a) I/O port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF60	D7	IOC07	P07 I/O control register	Output	Input	0	R/W	
	D6	IOC06	P06 I/O control register					
	D5	IOC05	P05 I/O control register					
	D4	IOC04	P04 I/O control register					
	D3	IOC03	P03 I/O control register					
	D2	IOC02	P02 I/O control register					
	D1	IOC01	P01 I/O control register					
	D0	IOC00	P00 I/O control register					
00FF61	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register					
	D5	IOC15	P15 I/O control register					
	D4	IOC14	P14 I/O control register					
	D3	IOC13	P13 I/O control register					
	D2	IOC12	P12 I/O control register					
	D1	IOC11	P11 I/O control register					
	D0	IOC10	P10 I/O control register					
00FF62	D7	P07D	P07 I/O port data	High	Low	1	R/W	
	D6	P06D	P06 I/O port data					
	D5	P05D	P05 I/O port data					
	D4	P04D	P04 I/O port data					
	D3	P03D	P03 I/O port data					
	D2	P02D	P02 I/O port data					
	D1	P01D	P01 I/O port data					
	D0	P00D	P00 I/O port data					
00FF63	D7	P17D	P17 I/O port data	High	Low	1	R/W	
	D6	P16D	P16 I/O port data					
	D5	P15D	P15 I/O port data					
	D4	P14D	P14 I/O port data					
	D3	P13D	P13 I/O port data					
	D2	P12D	P12 I/O port data					
	D1	P11D	P11 I/O port data					
	D0	P10D	P10 I/O port data					
00FF64	D7	PULP07	P07 pull-up control register	On	Off	1	R/W	
	D6	PULP06	P06 pull-up control register					
	D5	PULP05	P05 pull-up control register					
	D4	PULP04	P04 pull-up control register					
	D3	PULP03	P03 pull-up control register					
	D2	PULP02	P02 pull-up control register					
	D1	PULP01	P01 pull-up control register					
	D0	PULP00	P00 pull-up control register					
00FF65	D7	PULP17	P17 pull-up control register	On	Off	1	R/W	
	D6	PULP16	P16 pull-up control register					
	D5	PULP15	P15 pull-up control register					
	D4	PULP14	P14 pull-up control register					
	D3	PULP13	P13 pull-up control register					
	D2	PULP12	P12 pull-up control register					
	D1	PULP11	P11 pull-up control register					
	D0	PULP10	P10 pull-up control register					

Table 5.6.6.1(b) I/O port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF67	D7	IFLP17	P17 input I/F level select register	CMOS Schmitt	CMOS level	0	R/W	
	D6	IFLP16	P16 input I/F level select register					
	D5	IFLP15	P15 input I/F level select register					
	D4	IFLP14	P14 input I/F level select register					
	D3	IFLP13	P13 input I/F level select register					
	D2	IFLP12	P12 input I/F level select register					
	D1	IFLP11	P11 input I/F level select register					
	D0	IFLP10	P10 input I/F level select register					
00FF68	D7	IOC27	P27 I/O control register	Output	Input	0	R/W	
	D6	IOC26	P26 I/O control register					
	D5	IOC25	P25 I/O control register					
	D4	IOC24	P24 I/O control register					
	D3	IOC23	P23 I/O control register					
	D2	IOC22	P22 I/O control register					
	D1	IOC21	P21 I/O control register					
	D0	IOC20	P20 I/O control register					
00FF6A	D7	P27D	P27 I/O port data	High	Low	1	R/W	
	D6	P26D	P26 I/O port data					
	D5	P25D	P25 I/O port data					
	D4	P24D	P24 I/O port data					
	D3	P23D	P23 I/O port data					
	D2	P22D	P22 I/O port data					
	D1	P21D	P21 I/O port data					
	D0	P20D	P20 I/O port data					
00FF6C	D7	PULP27	P27 pull-up control register	On	Off	1	R/W	
	D6	PULP26	P26 pull-up control register					
	D5	PULP25	P25 pull-up control register					
	D4	PULP24	P24 pull-up control register					
	D3	PULP23	P23 pull-up control register					
	D2	PULP22	P22 pull-up control register					
	D1	PULP21	P21 pull-up control register					
	D0	PULP20	P20 pull-up control register					
00FF6E	D7	IFLP27	P27 input I/F level select register	CMOS Schmitt	CMOS level	0	R/W	
	D6	IFLP26	P26 input I/F level select register					
	D5	IFLP25	P25 input I/F level select register					
	D4	IFLP24	P24 input I/F level select register					
	D3	IFLP23	P23 input I/F level select register					
	D2	IFLP22	P22 input I/F level select register					
	D1	IFLP21	P21 input I/F level select register					
	D0	IFLP20	P20 input I/F level select register					
00FF30	D7	MODE16_A	PTM0–1 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_A	External clock 0 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT0	PTM0 clock output control	On	Off	0	R/W	
	D2	PTRUN0	PTM0 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET0	PTM0 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL0	PTM0 input clock selection	External clock	Internal clock	0	R/W	

Table 5.6.6.1(c) I/O port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF31	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT1	PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	PTM1 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET1	PTM1 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL1	PTM1 input clock selection	External clock	Internal clock	0	R/W	
00FF38	D7	MODE16_B	PTM2–3 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_B	External clock 1 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	RPTOUT2	PTM2 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT2	PTM2 clock output control	On	Off	0	R/W	
	D2	PTRUN2	PTM2 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET2	PTM2 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL2	PTM2 input clock selection	External clock	Internal clock	0	R/W	
00FF39	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	RPTOUT3	PTM3 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT3	PTM3 clock output control	On	Off	0	R/W	
	D2	PTRUN3	PTM3 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET3	PTM3 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL3	PTM3 input clock selection	External clock	Internal clock	0	R/W	
00FF40	D7	WDEN	Watchdog timer enable	Enable	Disable	1	R/W	
	D6	FOUT2	FOUT frequency selection			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when being read
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	

FOUT2	FOUT1	FOUT0	Frequency
1	1	1	f_{OSC3} / 8
1	1	0	f_{OSC3} / 4
1	0	1	f_{OSC3} / 2
1	0	0	f_{OSC3} / 1
0	1	1	f_{OSC1} / 8
0	1	0	f_{OSC1} / 4
0	0	1	f_{OSC1} / 2
0	0	0	f_{OSC1} / 1

■ DC output control

P00D–P07D: 00FF62H
P10D–P17D: 00FF63H
P20D–P27D: 00FF6AH

How I/O port terminal Pxx data readout and output data settings are performed.

When writing data:

When "1" is written: HIGH level
When "0" is written: LOW level

When the I/O port is set to output mode, the data written is output as is to the I/O port terminal. In terms of port data, when "1" is written, the port terminal goes to HIGH (V_{DD}) level and when "0" is written to a LOW (V_{SS}) level.
Even when the port is in input mode, data can still be written in.

When reading out data:

When "1" is read: HIGH level ("1")
When "0" is read: LOW level ("0")

When an I/O port is in input mode, the voltage level being input to the port terminal is read out.
When terminal voltage is HIGH (V_{DD}), it is read as a "1", and when it is LOW (V_{SS}), it is read as a "0".
Furthermore, in output mode, the contents of the data register are read out.
At initial reset, this register is set to "1" (HIGH level).

Note: The data registers of the ports that are configured to the serial interface outputs and special outputs can be used as general purpose registers that do not affect the terminal inputs/outputs.

IOC00–IOC07: 00FF60H
IOC10–IOC17: 00FF61H
IOC20–IOC27: 00FF68H

Sets the I/O ports to input or output mode.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

IOCxx is the I/O control register which correspond to each I/O port in a bit unit.
Writing "1" to the IOCxx register will switch the corresponding I/O port Pxx to output mode, and writing "0" will switch it to input mode.
When the special output is used, "1" must always be set for the I/O control registers (IOC14–IOC17) of I/O ports which will become output terminals.
At initial reset, this register is set to "0" (input mode).

Note: The I/O control registers of the ports that are configured to the serial interface inputs/outputs and special outputs can be used as general purpose registers that do not affect the terminal inputs/outputs.

IFLP10–IFLP17: 00FF67H
IFLP20–IFLP27: 00FF6EH

Selects an input interface level.

When "1" is written: CMOS Schmitt level
When "0" is written: CMOS level
Reading: Valid

IFLPxx is the input I/F level select register corresponding to the I/O ports P10–P17 and P20–P27.
When "1" is written to IFLPxx, the corresponding I/O port Pxx is configured with a CMOS Schmitt level input interface. When "0" is written, the port is configured with a CMOS level input interface.
At initial reset, this register is set to "0" (CMOS level).

PULP00–PULP07: 00FF64H
PULP10–PULP17: 00FF65H
PULP20–PULP27: 00FF6CH

The pull-up during the input mode are set with these registers.

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

PULPxx is the pull-up control register corresponding to each I/O port (in bit units).
By writing "1" to the PULPxx register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull-up function OFF.
At initial reset, these registers are all set to "1", so the pull-up function is set to ON.

Note: The pull-up control registers of the ports that are configured to the serial interface outputs or special outputs can be used as general purpose registers that do not affect the pull-up control. The pull-up control registers of the port that are configured to the serial interface inputs function the same as the I/O port.

■ Special output control

PTOUT0: 00FF30H•D3
PTOUT1: 00FF31H•D3
PTOUT2: 00FF38H•D3
PTOUT3: 00FF39H•D3

Controls the TOUT (programmable timer output clock) signal output.

When "1" is written: TOUT signal output
When "0" is written: DC output
Reading: Valid

PTOUT0–PTOUT3 are the output control registers for the TOUT0–TOUT3 signals. When PTOUT0 (or PTOUT1) is set to "1", the TOUT0 (or TOUT1) signal is output from the P14 port terminal. When PTOUT2 (or PTOUT3) is set to "1", the TOUT2 (or TOUT3) signal is output from the P15 port terminal. When "0" is set, P14 / P15 is set for DC output.
At this time, settings of the I / O control register IOC14 / IOC15 and data register P14D / P15D become invalid.
At initial reset, PTOUT is set to "0" (DC output).

Note: If PTOUT0 and PTOUT1 are set to "1" at the same time, PTOUT1 is effective. Similarly, if PTOUT2 and PTOUT3 are set to "1", PTOUT3 is effective. Furthermore, if the programmable timer is set in 16-bit mode, the TOUT0 and TOUT2 signals cannot be output.

RPTOUT2: 00FF38H•D4
RPTOUT3: 00FF39H•D4

Controls the $\overline{\text{TOUT2}}$ / $\overline{\text{TOUT3}}$ (inverted TOUT2 / TOUT3) signal output.

When "1" is written: $\overline{\text{TOUT}}$ signal output
When "0" is written: DC output
Reading: Valid

RPTOUT2 and RPTOUT3 are the output control registers for the $\overline{\text{TOUT2}}$ and $\overline{\text{TOUT3}}$ signals, respectively. When RPTOUT2 (or RPTOUT3) is set to "1", the $\overline{\text{TOUT2}}$ (or $\overline{\text{TOUT3}}$) signal is output from the P17 port terminal. When "0" is set, P17 is set for DC output.
At this time, settings of the I / O control register IOC17 and data register P17D become invalid.
At initial reset, RPTOUT is set to "0" (DC output).

Note: If RPTOUT2 and RPTOUT3 are set to "1" at the same time, RPTOUT3 is effective. Furthermore, if the programmable timer is set in 16-bit mode, the $\overline{\text{TOUT2}}$ signal cannot be output.

FOUTON: 00FF40H•D3

Controls the FOUT (f_{OSC1} / f_{OSC3} dividing clock) signal output.

When "1" is written: FOUT signal output
When "0" is written: DC output
Reading: Valid

FOUTON is the output control register for FOUT signal. When "1" is set, the FOUT signal is output from the P16 port terminal and when "0" is set, P16 is set for DC output. At this time, settings of the I / O control register IOC16 and data register P16D become invalid.
At initial reset, FOUTON is set to "0" (DC output).

FOUT0–FOUT2: 00FF40H•D4–D6

FOUT signal frequency is set as shown in Table 5.6.6.2.

Table 5.6.6.2 FOUT frequency settings

FOUT2	FOUT1	FOUT0	FOUT frequency
1	1	1	f_{OSC3} / 8
1	1	0	f_{OSC3} / 4
1	0	1	f_{OSC3} / 2
1	0	0	f_{OSC3} / 1
0	1	1	f_{OSC1} / 8
0	1	0	f_{OSC1} / 4
0	0	1	f_{OSC1} / 2
0	0	0	f_{OSC1} / 1

f_{OSC1}: OSC1 oscillation frequency
f_{OSC3}: OSC3 oscillation frequency

At initial reset, this register is set to "0" (f_{OSC1} / 1).

5.6.7 Programming notes

(1) When changing the port terminal in which the pull-up resistor is enabled from LOW level to HIGH, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

(2) Since the special output signals (TOUT0–3, $\overline{TOUT2–3}$, and FOUT) are generated asynchronously from the output control registers (PTOUT0–3, RPTOUT2–3, and FOUTON), when the signals is turned ON or OFF by the output control register settings, a hazard of a 1/2 cycle or less is generated.

(3) When the FOUT frequency is made "f_{OSC3}/n", you must turn on the OSC3 oscillation circuit before outputting FOUT. A time interval of several tens of µsec to several tens of msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before turning outputting FOUT. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 9, "ELECTRICAL CHARACTERISTICS".)

(4) The SLP instruction has executed when the special output signals (TOUT0–3, $\overline{TOUT2–3}$, and FOUT) are in the enable status, an unstable clock is output for the special output at the time of return from the SLEEP state. Consequently, when shifting to the SLEEP state, you should set the special output signal to the disable status prior to executing the SLP instruction.

5.7 Serial Interface

5.7.1 Configuration of serial interface

The S1C8F626 incorporates two channels of full duplex serial interface ports (when asynchronous system is selected) that allow the user to select either clock synchronous system or asynchronous system.
The data transfer method can be selected in software.
When the clock synchronous system is selected, 8-bit data transfer is possible.
When the asynchronous system is selected, either 7-bit or 8-bit data transfer is possible, and a parity check of received data and the addition of a parity bit for transmitting data can automatically be done by selecting in software.
Figure 5.7.1.1 shows the configuration of the serial interface.

Note: Channels 0 and 1 of the serial interface are precisely identical, and the signal and register names are identified by the channel number (0 or 1) attached (e.g. the SIN0 terminal is for channel 0 and SIN1 terminal is for channel 1). This section explains the serial interface functions in common to both channels using common signal names with "x" attached as a substitute for the channel number (e.g. SIN0/SIN1 → SINx) except the part that needs distinction.

Serial interface Ch.0 input/output terminals, SIN0, SOUT0, $\overline{\text{SCLK0}}$ and $\overline{\text{SRDY0}}$ are shared with I/O ports P10–P13. Serial interface Ch.1 input/output terminals, SIN1, SOUT1, $\overline{\text{SCLK1}}$ and $\overline{\text{SRDY1}}$ are shared with I/O ports P20–P23. In order to utilize these terminals for the serial interface input/output terminals, "1" must be written to the ESIFx register.
At initial reset, these terminals are set as I/O port terminals.
The direction of I/O port terminals set for serial interface input/output terminals are determined by the signal and transfer mode for each terminal. Furthermore, the settings for the corresponding I/O control registers for the I/O ports become invalid.

Table 5.7.1.1 Configuration of input/output terminals

Terminal	When serial interface is selected
P10	SIN0
P11	SOUT0
P12	$\overline{\text{SCLK0}}$
P13	$\overline{\text{SRDY0}}$
P20	SIN1
P21	SOUT1
P22	$\overline{\text{SCLK1}}$
P23	$\overline{\text{SRDY1}}$

* The terminals used may vary depending on the transfer mode.

The serial interface terminals are configured according to the transfer mode set using the registers SMDx0 and SMDx1. SINx and SOUTx are serial data input and output terminals which function identically in clock synchronous system and asynchronous system. $\overline{\text{SCLKx}}$ is exclusively for use with clock synchronous system and functions as a synchronous clock input/output terminal. $\overline{\text{SRDYx}}$ is exclusively for use in clock synchronous slave mode and functions as a send-receive ready signal output terminal.
When asynchronous system is selected, since $\overline{\text{SCLKx}}$ and $\overline{\text{SRDYx}}$ are superfluous, the I/O port terminals P12/P22 and P13/P23 can be used as I/O ports.
In the same way, when clock synchronous master mode is selected, since $\overline{\text{SRDYx}}$ is superfluous, the I/O port terminal P13/P23 can be used as I/O port.

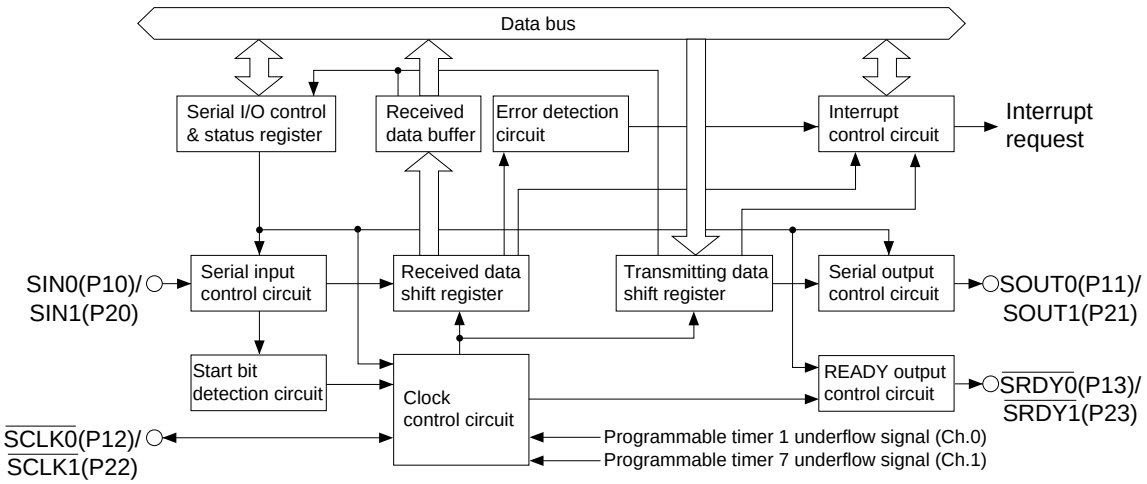


Fig. 5.7.1.1 Configuration of serial interface

5.7.2 I/O terminal specifications

The serial interface I/O terminals are shared with the I/O ports, so the terminal specifications are configured by setting the I/O port registers.

Each I/O port terminal has a built-in pull-up resistor that is enabled in input mode. Software can select whether the pull-up resistor is used or not in port (one bit) units. Use the PULPxx registers to configure pull-up for the P10 (SIN0), P12 ($\overline{SCLK0}$), P20 (SIN1) and P22 ($\overline{SCLK1}$) terminals. When the pull-up resistor is not used, make sure that the input terminal does not enter a floating state. Furthermore, the input interface level (CMOS level or CMOS Schmitt level) for these terminals can be selected using the IFLPxx registers of the I/O ports. Refer to Section 5.6, "I/O Ports", for controlling pull-up and input interface levels.

The output specification is fixed at complementary output. Open-drain output cannot be selected and the high-impedance control function is not provided.

5.7.3 Transfer modes

There are four transfer modes for the serial interface and mode selection is made by setting the two bits of the mode selection registers SMDx0 and SMDx1 as shown in the table below.

Table 5.7.3.1 Transfer modes

SMDx1	SMDx0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

Table 5.7.3.2 Terminal settings corresponding to each transfer mode

Mode	SINx	SOUTx	$\overline{SCLKx}$	$\overline{SRDYx}$
Asynchronous 8-bit	Input	Output	P12/P22	P13/P23
Asynchronous 7-bit	Input	Output	P12/P22	P13/P23
Clock synchronous slave	Input	Output	Input	Output
Clock synchronous master	Input	Output	Output	P13/P23

At initial reset, transfer mode is set to clock synchronous master mode.

■ Clock synchronous master mode

In this mode, the internal clock is utilized as a synchronous clock for the built-in shift registers, and clock synchronous 8-bit serial transfers can be performed with this serial interface as the master.
The synchronous clock is also output from the $\overline{SCLKx}$ terminal which enables control of the external (slave side) serial I/O device. Since the $\overline{SRDYx}$ terminal is not utilized in this mode, it can be used as an I/O port.
Figure 5.7.3.1(a) shows the connection example of input/output terminals in the clock synchronous master mode.

■ Clock synchronous slave mode

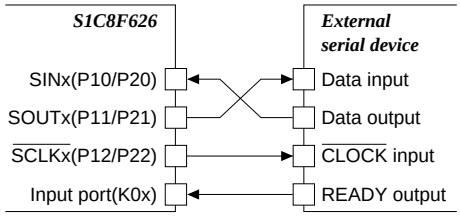
In this mode, a synchronous clock from the external (master side) serial input/output device is utilized and clock synchronous 8-bit serial transfers can be performed with this serial interface as the slave.
The synchronous clock is input to the $\overline{SCLKx}$ terminal and is utilized by this interface as the synchronous clock.
Furthermore, the $\overline{SRDYx}$ signal indicating the transmit-receive ready status is output from the $\overline{SRDYx}$ terminal in accordance with the serial interface operating status.
In the slave mode, the settings for registers SCSx0 and SCSx1 used to select the clock source are invalid.
Figure 5.7.3.1(b) shows the connection example of input/output terminals in the clock synchronous slave mode.

■ Asynchronous 7-bit mode

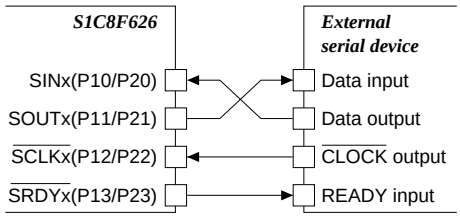
In this mode, asynchronous 7-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 7 bits with or without parity. Since this mode employs the internal clock, the $\overline{SCLKx}$ terminal is not used. Furthermore, since the $\overline{SRDYx}$ terminal is not utilized either, both of these terminals can be used as I/O ports.
Figure 5.7.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.

■ Asynchronous 8-bit mode

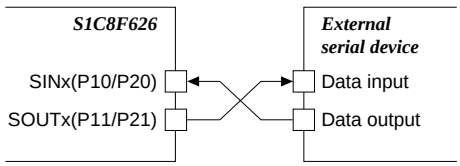
In this mode, asynchronous 8-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 8 bits with or without parity. Since this mode employs the internal clock, the $\overline{SCLKx}$ terminal is not used. Furthermore, since the $\overline{SRDYx}$ terminal is not utilized either, both of these terminals can be used as I/O ports.
Figure 5.7.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.



(a) Clock synchronous master mode



(b) Clock synchronous slave mode



(c) Asynchronous 7-bit/8-bit mode

Fig. 5.7.3.1 Connection examples of serial interface I/O terminals

5.7.4 Clock source

There are four clock sources and selection is made by setting the two bits of the clock source selection register SCSx0 and SCSx1 as shown in table below.

Table 5.7.4.1 Clock source

SCSx1	SCSx0	Clock source
1	1	Programmable timer 1 (Ch.0)
		Programmable timer 7 (Ch.1)
1	0	fOSC3 / 4
0	1	fOSC3 / 8
0	0	fOSC3 / 16

This register setting is invalid in clock synchronous slave mode and the external clock input from the SCLKx terminal is used.
When the "programmable timer" is selected, the programmable timer 1 (Ch.0) or timer 7 (Ch.1) underflow signal is divided by 2 and this signal is used as the clock source.
With respect to the transfer rate setting, see "5.10 Programmable Timer".
At initial reset, the synchronous clock is set to "fOSC3 / 16".
Whichever clock is selected, the signal is further divided by 16 and then used as the synchronous clock and the sampling clock.
Furthermore, external clock input is used as is for SCLKx in clock synchronous slave mode.
Table 5.7.4.2 shows an examples of transfer rates and OSC3 oscillation frequencies when the clock source is set to programmable timer.
When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several tens of µsec to several tens of msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 9, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

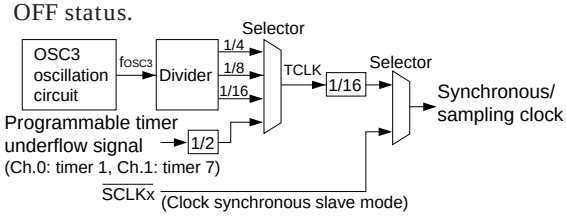


Fig. 5.7.4.1 Division of the synchronous clock

Table 5.7.4.2 OSC3 oscillation frequencies and transfer rates

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings					
	fOSC3 = 2.4576 MHz		fOSC3 = 3.0720 MHz		fOSC3 = 3.6864 MHz	
	PST1x/7x	RDR1x/7x	PST1x/7x	RDR1x/7x	PST1x/7x	RDR1x/7x
19,200	00H	03H	00H	04H	00H	05H
9,600	00H	07H	00H	09H	00H	0BH
4,800	00H	0FH	00H	13H	00H	17H
2,400	00H	1FH	00H	27H	00H	2FH
1,200	00H	3FH	00H	4FH	00H	5FH
600	00H	7FH	00H	9FH	00H	BFH
300	02H	1FH	03H	09H	01H	BFH
150	02H	3FH	03H	13H	02H	5FH

* Since the underflow signal only is used as the clock source, the CDR1x / 7x register value does not affect the transfer rates.

5.7.5 Transmit-receive control

Below is a description of the registers which handle transmit-receive control. With respect to transmit-receive control procedures and operations, please refer to the following sections in which these are discussed on a mode by mode basis.

■ Shift register and received data buffer

Exclusive shift registers for transmitting and receiving are installed in this serial interface. Consequently, duplex communication simultaneous transmit and receive is possible when the asynchronous system is selected.

Data being transmitted are written to TRXDx0–TRXDx7 and converted to serial through the shift register and is output from the SOUTx terminal.

In the reception section, a received data buffer is installed separate from the shift register.
Data being received are input to the SINx terminal and is converted to parallel through the shift register and written to the received data buffer. Since the received data buffer can be read even during serial input operation, the continuous data is received efficiently.
However, since buffer functions are not used in clock synchronous mode, be sure to read out data before the next data reception begins.

■ Transmit enable register and transmit control bit

For transmitting control, use the transmit enable register TXENx and transmit control bit TXTRGx.

The transmit enable register TXENx is used to set the transmitting enable / disable status. When "1" is written to this register to set the transmitting enable status, clock input to the shift register is enabled and the system is ready to transmit data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLKx}}$ terminal is also enabled.

The transmit control bit TXTRGx is used as the trigger to start transmitting data.
Data to be transmitted is written to the transmit data shift register, and when transmitting preparations a recomplete, "1" is written to TXTRGx whereupon data transmitting begins.
When interrupt has been enabled, an interrupt is generated when the transmission is completed. If there is subsequent data to be transmitted it can be sent using this interrupt.
In addition, TXTRGx can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
For details on timing, see the timing chart which gives the timing for each mode.

When not transmitting, set TXENx to "0" to disable transmitting status.

■ Receive enable register and receive control bit

For receiving control, use the receive enable register RXENx and receive control bit RXTRGx.
Receive enable register RXENx is used to set receiving enable / disable status. When "1" is written into this register to set the receiving enable status, clock input to the shift register is enabled and the system is ready to receive data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLKx}}$ terminal is also enabled.
With the above setting, receiving begins and serial data input from the SINx terminal goes to the shift register.
The operation of the receive control bit RXTRGx is slightly different depending on whether a clock synchronous system or an asynchronous system is being used.
In the clock synchronous system, the receive control bit RXTRGx is used as the trigger to start receiving data.
When received data has been read and the preparation for next data receiving is completed, write "1" into RXTRGx to start receiving. (When "1" is written to RXTRGx in slave mode, $\overline{\text{SRDYx}}$ switches to "0".)
In an asynchronous system, RXTRGx is used to prepare for next data receiving. After reading the received data from the received data buffer, write "1" into RXTRGx to signify that the received data buffer is empty. If "1" is not written into RXTRGx, the overrun error flag OERx will be set to "1" when the next receiving operation is completed. (An overrun error will be generated when receiving is completed between reading the received data and the writing of "1" to RXTRGx.)
In addition, RXTRGx can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRGx is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
For details on timing, see the timing chart which gives the timing for each mode.

When you do not receive, set RXENx to "0" to disable receiving status.

5.7.6 Operation of clock synchronous transfer

Clock synchronous transfer involves the transfer of 8-bit data by synchronizing it to eight clocks. The same synchronous clock is used by both the transmitting and receiving sides.
When the serial interface is used in the master mode, the clock signal selected using SCSx0 and SCSx1 is further divided by 1/16 and employed as the synchronous clock. This signal is then sent via the SCLKx terminal to the slave side (external serial I/O device).
When used in the slave mode, the clock input to the SCLKx terminal from the master side (external serial input/output device) is used as the synchronous clock.

In the clock synchronous mode, since one clock line (SCLKx) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)

The transfer data length is fixed at 8 bits. Data can be switched using a register whether it is transmitted/received from LSB (bit 0) or MSB (bit 7).

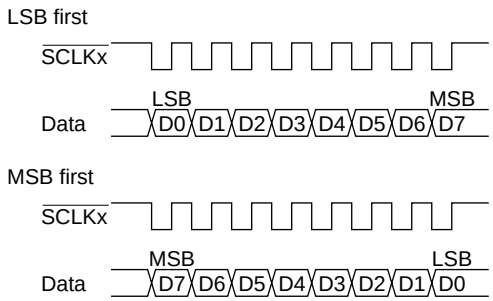


Fig. 5.7.6.1 Transfer data configuration using clock synchronous mode

Below is a description of initialization when performing clock synchronous transfer, transmit-receive control procedures and operations.
With respect to serial interface interrupt, see "5.7.9 Interrupt function".

■ Initialization of serial interface

When performing clock synchronous transfer, the following initial settings must be made.

(1) Setting of transmitting/receiving disable
To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXENx and the receive enable register RXENx. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection
Because serial interface input/output ports SINx, SOUTx, SCLKx and SRDYx are set as the I/O port terminals P10–P13 (channel 0)/P20–P23 (channel 1) at initial reset, "1" must be written to the serial interface enable register ESIFx in order to set these terminals for serial interface use.

(3) Setting of transfer mode
Select the clock synchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMDx0 and SMDx1.

Master mode: SMDx0 = "0", SMDx1 = "0"
Slave mode: SMDx0 = "1", SMDx1 = "0"

(4) Clock source selection
In the master mode, select the synchronous clock source by writing data to the two bits of the clock source selection registers SCSx0 and SCSx1. (See Table 5.7.4.1.)
This selection is not necessary in the slave mode.

Since all the registers mentioned in (2)–(4) are assigned to the same address, it's possible to set them all with one instruction. The parity enable register EPRx is also assigned to this address, however, since parity is not necessary in the clock synchronous mode, parity check will not take place regardless of how they are set.

(5) Clock source control
When the master mode is selected and programmable timer for the clock source is selected, set transfer rate on the programmable timer side. (See "5.10 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "5.4 Oscillation Circuits and Operating Mode".)

(6) Serial data input/output permutation
The S1C8F626 provides the data input/output permutation select register SDPx to select whether the serial data bits are transferred from the LSB or MSB. The SDPx register should be set before writing data to TRXDx0–TRXDx7.

■ Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXENx and the receive enable register RXENx to reset the serial interface.

(2) Write "1" in the transmit enable register TXENx to set into the transmitting enable status.

(3) Write the transmitting data into TRXDx0–TRXDx7.

(4) In case of the master mode, confirm the receive ready status on the slave side (external serial input / output device), if necessary. Wait until it reaches the receive ready status.

(5) Write "1" in the transmit control bit TXTRGx and start transmitting.

In the master mode, this control causes the synchronous clock to change to enable and to be provided to the shift register for transmitting and output from the $\overline{SCLKx}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLKx}$ terminal.
The transmitting data of the shift register shifts one bit at a time at each falling edge of the synchronous clock and is output from the SOUTx terminal. When the final bit (MSB when "LSB first" is selected, or LSB when "MSB first" is selected) is output, the SOUTx terminal is maintained at that level, until the next transmitting begins.

The transmitting complete interrupt factor flag FSTRAx is set to "1" at the point where the data transmitting of the shift register is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXENx, when the transmitting is completed.

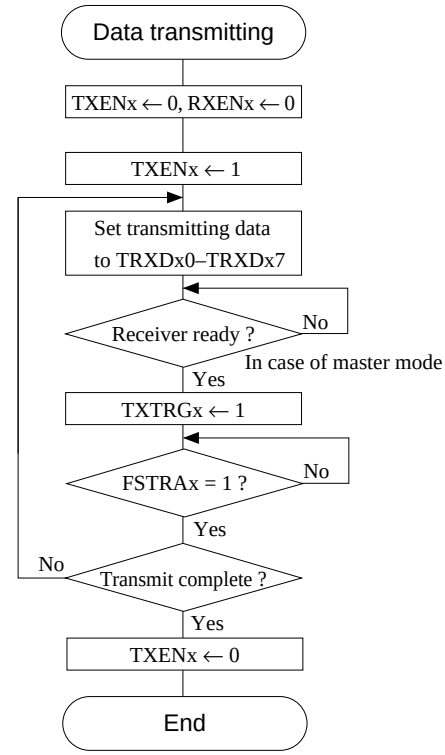


Fig. 5.7.6.2 Transmit procedure in clock synchronous mode

■ Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXENx and transmit enable register TXENx to reset the serial interface.

(2) Write "1" in the receive enable register RXENx to set into the receiving enable status.

(3) In case of the master mode, confirm the transmit ready status on the slave side (external serial input / output device), if necessary. Wait until it reaches the transmit ready status.

(4) Write "1" in the receive control bit RXTRGx and start receiving.

In the master mode, this control causes the synchronous clock to change to enable and is provided to the shift register for receiving and output from the $\overline{\text{SCLKx}}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{\text{SCLKx}}$ terminal. The received data input from the SINx terminal is successively incorporated into the shift register in synchronization with the rising edge of the synchronous clock.
At the point where the data of the 8th bit has been incorporated at the final (8th) rising edge of the synchronous clock, the content of the shift register is sent to the received data buffer and the receiving complete interrupt factor flag FSRECx is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point.

(5) Read the received data from TRXDx0–TRXDx7 using receiving complete interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXENx, when the receiving is completed.

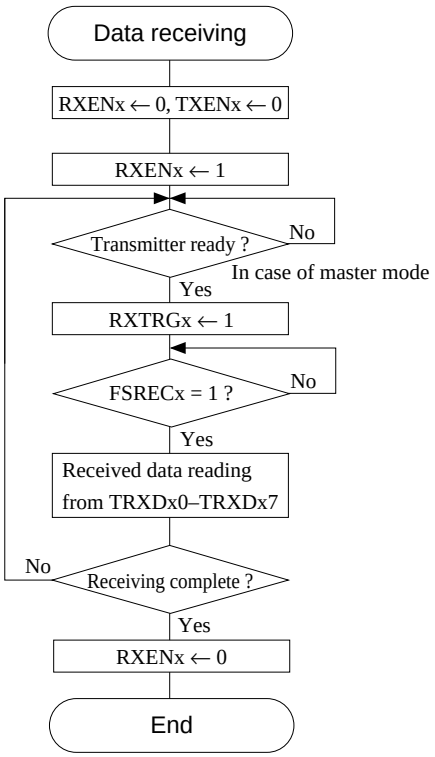


Fig. 5.7.6.3 Receiving procedure in clock synchronous mode

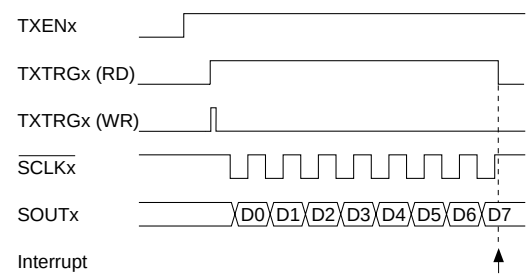
■ Transmit/receive ready (SRDYx) signal

When this serial interface is used in the clock synchronous slave mode (external clock input), an SRDYx signal is output to indicate whether or not this serial interface can transmit/receive to the master side (external serial input/output device). This signal is output from the SRDYx terminal and when this interface enters the transmit or receive enable (READY) status, it becomes "0" (LOW level) and becomes "1" (HIGH level) when there is a BUSY status, such as during transmit/receive operation.
The SRDYx signal changes the "1" to "0," immediately after writing "1" into the transmit control bit TXTRGx or the receive control bit RXTRGx and returns from "0" to "1", at the point where the first synchronous clock has been input (falling edge).

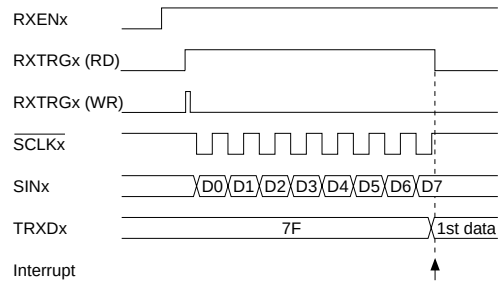
When you have set in the master mode, control the transfer by inputting the same signal from the slave side using the input port or I/O port. At this time, since the SRDYx terminal is not set and instead P13/P23 functions as the I/O port, you can apply this port for said control.

■ Timing chart

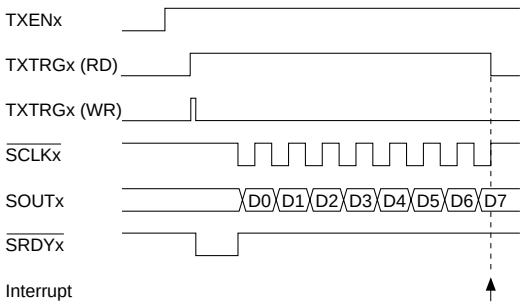
The timing chart for the clock synchronous system transmission is shown in Figure 5.7.6.4.



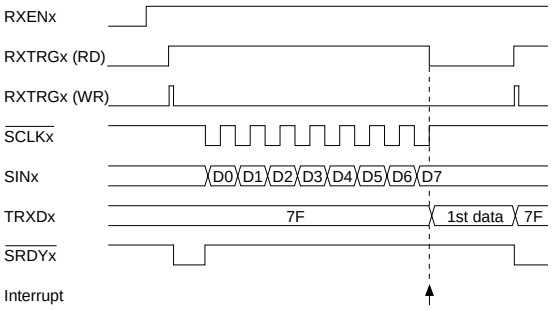
(a) Transmit timing for master mode



(c) Receive timing for master mode



(b) Transmit timing for slave mode

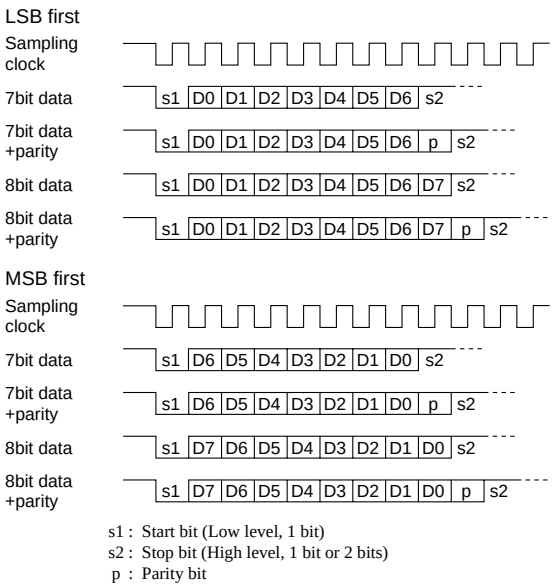


(d) Receive timing for slave mode

Fig. 5.7.6.4 Timing chart (clock synchronous system transmission, LSB first)

5.7.7 Operation of asynchronous transfer

Asynchronous transfer is a mode that transfers by adding a start bit and a stop bit to the front and the back of each piece of serial converted data. In this mode, there is no need to use a clock that is fully synchronized clock on the transmit side and the receive side, but rather transmission is done while adopting the synchronization at the start / stop bits that have attached before and after each piece of data. The RS-232C interface functions can be easily realized by selecting this transfer mode.
This interface has separate transmit and receive shift registers and is designed to permit full duplex transmission to be done simultaneously for transmitting and receiving.
The asynchronous mode supports a maximum 19200 bps of transfer rate in normal operating mode or a maximum 600 bps in low power operating mode.
For transfer data in the asynchronous 7-bit mode, either 7 bits data (no parity) or 7 bits data + parity bit can be selected. In the asynchronous 8-bit mode, either 8 bits data (no parity) or 8 bits data + parity bit can be selected.
Parity can be even or odd, and parity checking of received data and adding a party bit to transmitting data will be done automatically. Thereafter, it is not necessary to be conscious of parity itself in the program.
The start bit length is fixed at 1 bit. For the stop bit length, either 1 bit or 2 bits can be selected using the stop bit select register STPBx. Whether data is transmitted / received from LSB (bit 0) or MSB (bit 7) it can be switched using the data input / output permutation select register SDPx.



s1 : Start bit (Low level, 1 bit)
s2 : Stop bit (High level, 1 bit or 2 bits)
p : Parity bit

Fig. 5.7.7.1 Transfer data configuration for asynchronous system

Here following, we will explain the control sequence and operation for initialization and transmitting / receiving in case of asynchronous data transfer. See "5.7.9 Interrupt function" for the serial interface interrupts.

■ Initialization of serial interface

The below initialization must be done in cases of asynchronous system transfer.

(1) Setting of transmitting/receiving disable
To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXENx and the receive enable register RXENx. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection
Because serial interface input / output terminals SINx and SOUTx are set as I / O port terminals P10 / P20 and P11 / P21 at initial reset, "1" must be written to the serial interface enable register ESIFx in order to set these terminals for serial interface use.
$\overline{\text{SCLKx}}$ and $\overline{\text{SRDYx}}$ terminals set in the clock synchronous mode are not used in the asynchronous mode. These terminals function as I / O port terminals P12 / P22 and P13 / P23.

(3) Setting of transfer mode
Select the asynchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMDx0 and SMDx1.

7-bit mode: SMDx0 = "0", SMDx1 = "1"
8-bit mode: SMDx0 = "1", SMDx1 = "1"

(4) Parity bit selection
When checking and adding parity bits, write "1" into the parity enable register EPRx to set to "with parity check". As a result of this setting, in the asynchronous 7-bit mode, it has a 7 bits data + parity bit configuration and in the asynchronous 8-bit mode it has an 8 bits data + parity bit configuration. In this case, parity checking for receiving and adding a party bit for transmitting is done automatically in hardware. Moreover, when "with parity check" has been selected, "odd" or "even" parity must be further selected in the parity mode selection register PMDx.

When "0" is written to the EPRx register to select "without parity check" in the asynchronous 7-bit mode, data configuration is set to 7 bits data (no parity) and in the asynchronous 8-bit mode (no parity) it is set to 8 bits data (no parity) and parity checking and parity bit adding will not be done.

(5) Clock source selection
Select the clock source by writing data to the two bits of the clock source selection registers SCSx0 and SCSx1. (See Table 5.7.4.1.)

Since all the registers mentioned in (2)–(5) are assigned to the same address, it's possible to set them all with one instruction.

(6) Clock source control
When the programmable timer is selected for the clock source, set transfer rate on the programmable timer side. (See "5.10 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "5.4 Oscillation Circuits and Operating Mode".)

(7) Stop bit length selection
The stop bit length can be configured to 1 bit or 2 bits using the stop bit select register STPBx.

Table 5.7.7.1 Stop bit and parity bit settings

STPBx	EPRx	PMDx	Settings	
			Stop bit	Parity bit
1	1	1	2 bits	Odd
		0	2 bits	Even
	0	–	2 bits	Non parity
0	1	1	1 bit	Odd
		0	1 bit	Even
	0	–	1 bit	Non parity

(8) Serial data input/output permutation
The S1C8F626 provides the data input/output permutation select register SDPx to select whether the serial data bits are transferred from the LSB or MSB. The SDPx register should be set before writing data to TRXDx0–TRXDx7.

■ Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXENx to reset the serial interface.

(2) Write "1" in the transmit enable register TXENx to set into the transmitting enable status.

(3) Write the transmitting data into TRXDx0–TRXDx7.
Also, when 7-bit data is selected, the TRXDx7 data becomes invalid.

(4) Write "1" in the transmit control bit TXTRGx and start transmitting.
This control causes the shift clock to change to enable and a start bit (LOW) is output to the SOUTx terminal in synchronize to its falling edge. The transmitting data set to the shift register is shifted one bit at a time at each falling edge of the clock thereafter and is output from the SOUTx terminal. After the data output, it outputs a stop bit (HIGH) and HIGH level is maintained until the next start bit is output.

The transmitting complete interrupt factor flag FSTRAx is set to "1" at the point where the data transmitting is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(5) Repeat steps (3) to (4) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXENx, when the transmitting is completed.

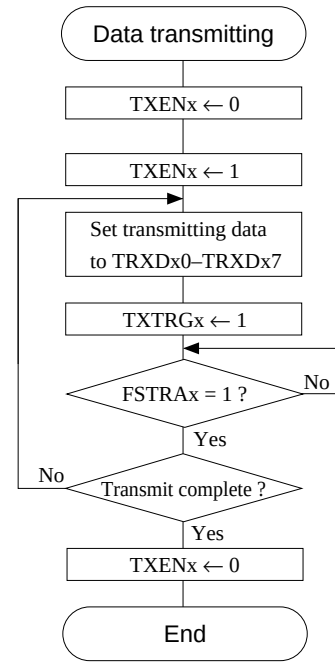


Fig. 5.7.7.2 Transmit procedure in asynchronous mode

■ Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXENx to set the receiving disable status and to reset the respective PERx, OERx, FERx flags that indicate parity, overrun and framing errors.

(2) Write "1" in the receive enable register RXENx to set into the receiving enable status.

(3) The shift clock will change to enable from the point where the start bit (LOW) has been input from the SINx terminal and the receive data will be synchronized to the rising edge following the second clock, and will thus be successively incorporated into the shift register.
After data bits have been incorporated, the stop bit is checked and, if it is not HIGH, it becomes a framing error and the error interrupt factor flag FSERRx is set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
When receiving is completed, data in the shift register is transferred to the received data buffer and the receiving complete interrupt flag FSRECx is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point. (When an overrun error is generated, the interrupt factor flag FSRECx is not set to "1" and a receiving complete interrupt is not generated.)
If "with parity check" has been selected, a parity check is executed when data is transferred into the received data buffer from the shift register and if a parity error is detected, the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error mentioned above.

(4) Read the received data from TRXDx0–TRXDx7 using receiving complete interrupt.

(5) Write "1" to the receive control bit RXTRGx to inform that the receive data has been read out. When the following data is received prior to writing "1" to RXTRGx, it is recognized as an overrun error and the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error and parity error mentioned above.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXENx, when the receiving is completed.

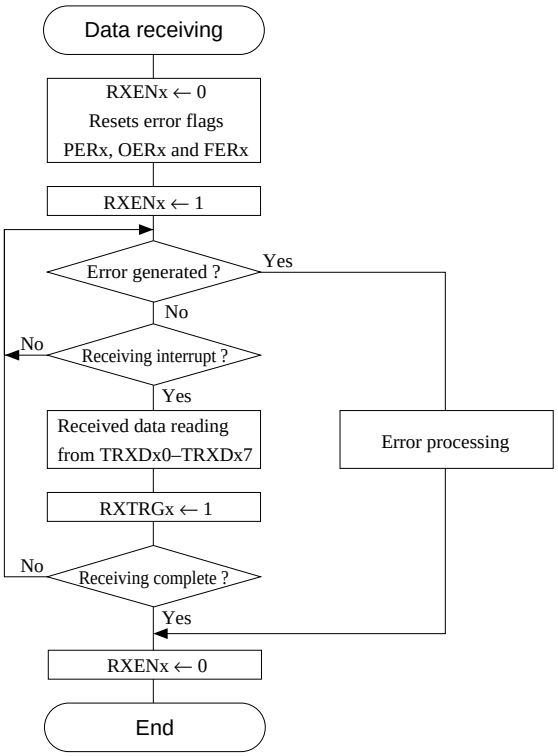


Fig. 5.7.7.3 Receiving procedure in asynchronous mode

■ Receive error

During receiving the following three types of errors can be detected by an interrupt.

(1) Parity error

When writing "1" to the EPRx register to select "with parity check", a parity check (vertical parity check) is executed during receiving. After each data bit is sent a parity check bit is sent. The parity check bit is a "0" or a "1". Even parity checking will cause the sum of the parity bit and the other bits to be even. Odd parity causes the sum to be odd. This is checked on the receiving side.

The parity check is performed when data received in the shift register is transferred to the received data buffer. It checks whether the parity check bit is a "1" or a "0" (the sum of the bits including the parity bit) and the parity set in the PMDx register match. When it does not match, it is recognized as an parity error and the parity error flag PERx and the error interrupt factor flag FSERRx are set to "1".

When interrupt has been enabled, an error interrupt is generated at this point.

The PERx flag is reset to "0" by writing "1".

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

The received data at this point cannot assured because of the parity error.

(2) Framing error

In asynchronous transfer, synchronization is adopted for each character at the start bit ("0") and the stop bit ("1"). When receiving has been done with the stop bit set at "0", the serial interface judges the synchronization to be off and a framing error is generated. When this error is generated, the framing error flag FERx and the error interrupt factor flag FSERRx are set to "1". When interrupt has been enabled, an error interrupt is generated at this point.

The FERx flag is reset to "0" by writing "1".

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receiving, such data cannot be assured.

(3) Overrun error

When the next data is received before "1" is written to RXTRGx, an overrun error will be generated, because the previous receive data will be overwritten. When this error is generated, the overrun error flag OERx and the error interrupt factor flag FSERRx are set to "1". When interrupt has been enabled, an error interrupt is generated at this point. The OERx flag is reset to "0" by writing "1" into it.

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

Furthermore, when the timing for writing "1" to RXTRGx and the timing for the received data transfer to the received data buffer overlap, it will be recognized as an overrun error.

■ Timing chart

Figure 5.7.7.4 show the asynchronous transfer timing chart.

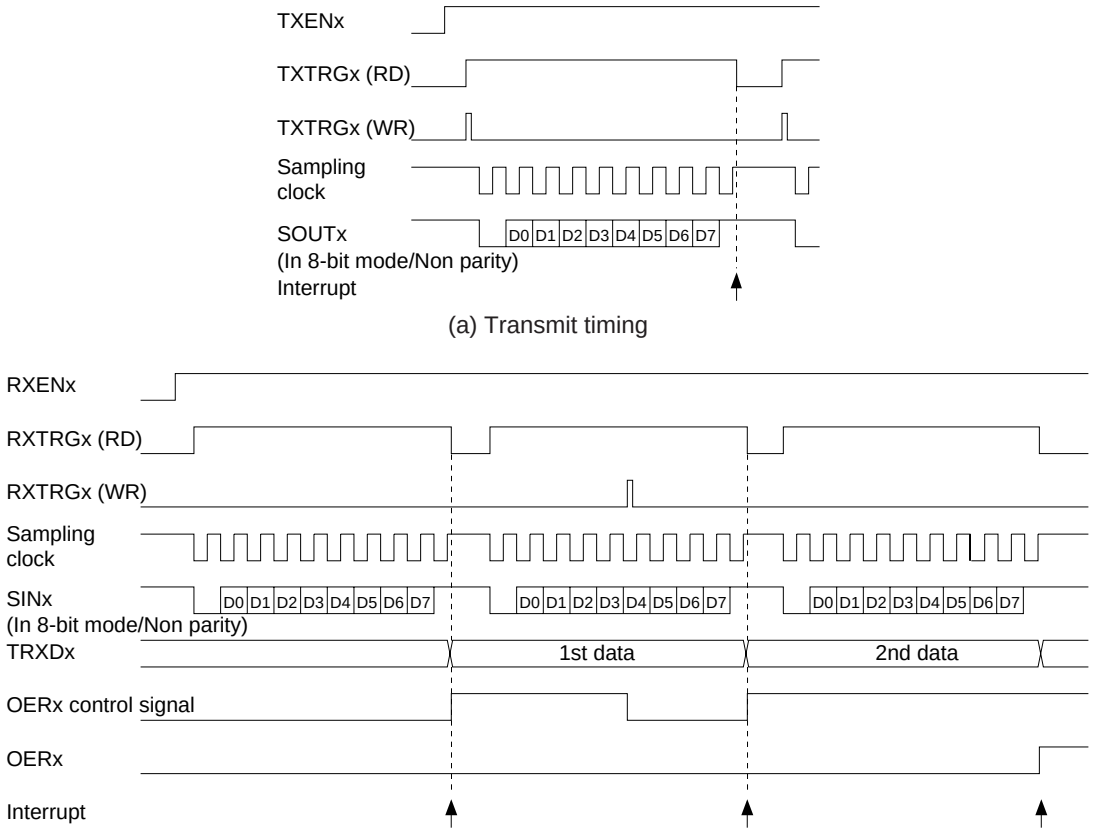


Fig. 5.7.7.4 Timing chart (asynchronous transfer, LSB first, stop bit = 1 bit)

5.7.8 IR (Infrared-ray) interface

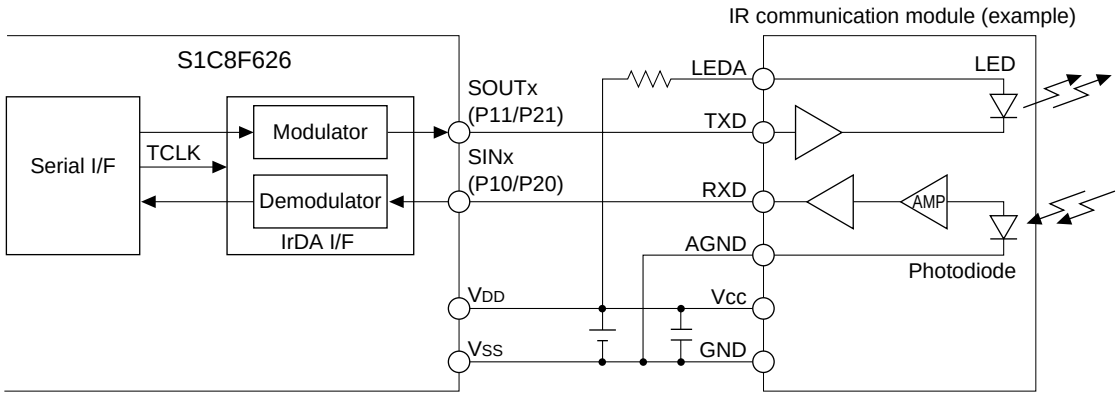


Fig. 5.7.8.1 Configuration example of IR interface

The serial interface has a built-in modulator / demodulator. Thus a circuit for infrared-ray communication based on IrDA (Infrared Data Association) standard can be configured by adding a simple external circuit.

■ Setting of IR interface

The modulator / demodulator is only available when the serial interface is set in asynchronous mode.
When using the IR interface, change the function of the serial interface using the IRSTx register. (See Table 5.7.8.1.)

Table 5.7.8.1 Setting of IR interface

IRSTx	Setting
1	IR interface is used
0	IR interface is not used (normal interface is set)

At initial reset, the serial interface is set as general interface.

When IR interface function is enabled, the serial interface can invert the logic polarity of the input / output signal according to the external infrared-ray communication module. It is negative logic usually. Invert the logic when inputting and outputting positive logic signal.
The logic of the SINx input and SOUTx output can be individually set by the IRILx register and the IRTLx register. (See Tables 5.7.8.2 and 5.7.8.3.)

At initial reset, both the IRILx register and IRTLx register are set to "0" (logic not inverted).

■ Control of IR interface

Figures 5.7.8.2 and 5.7.8.3 show the input / output signal conversion by the modulator / demodulator. The control procedure of data transfer is the same as in case of the asynchronous mode. Refer to Section 5.7.5, "Transmit-receive control".

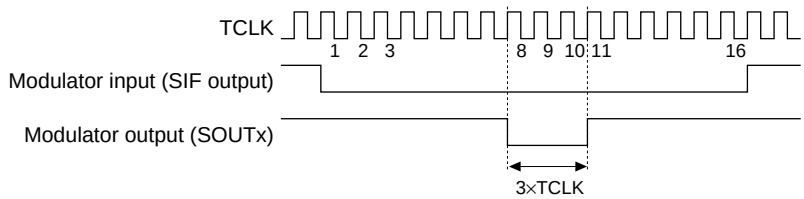


Fig. 5.7.8.2 Input/output signal (during transmission)

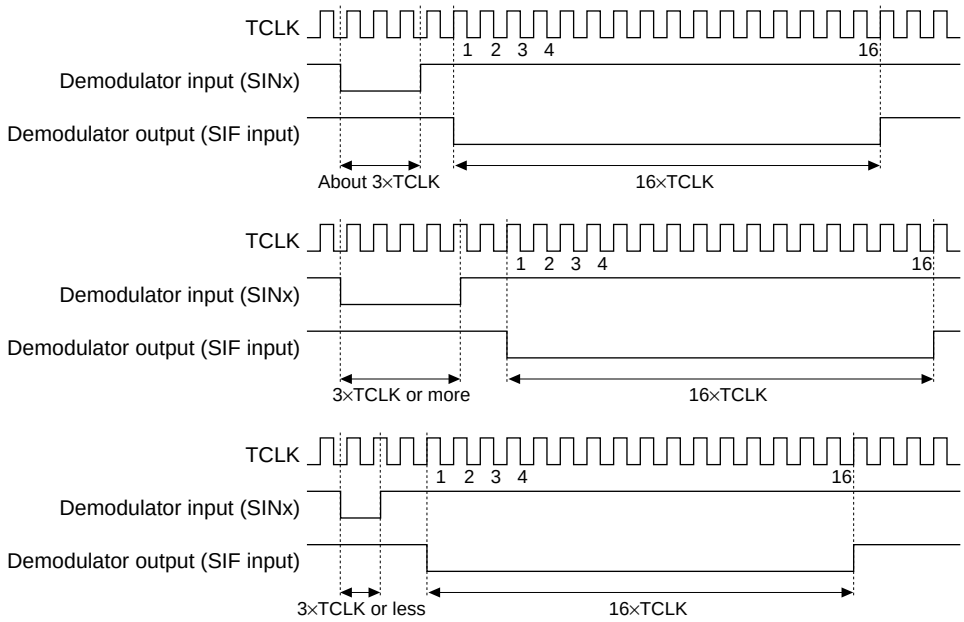


Fig. 5.7.8.3 Input/output signal (during receiving)

Input/output logic configuration examples

- 8-bit asynchronous mode
- LSB first
- Odd parity
- Two stop bit

Table 5.7.8.2 Input logic of IR interface

IRILx	Setting
1	SINx input logic is inverted (HIGH active)
0	SINx input logic is not inverted (LOW active)

Table 5.7.8.3 Output logic of IR interface

IRTLx	Setting
1	SOUTx output logic is inverted (HIGH active)
0	SOUTx output logic is not inverted (LOW active)

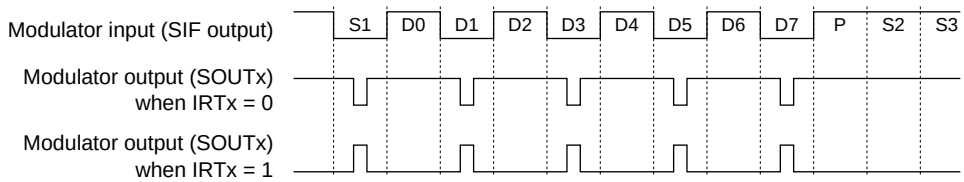


Fig. 5.7.8.4 Example of transmit signal waveform

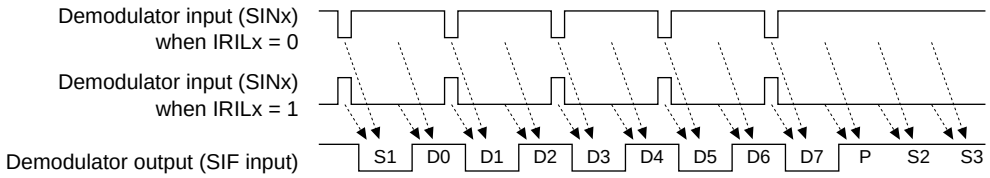


Fig. 5.7.8.5 Example of receive signal waveform

5.7.9 Interrupt function

This serial interface includes a function that generates the below indicated three types of interrupts.

- **Transmitting complete interrupt**
- **Receiving complete interrupt**
- **Error interrupt**

The interrupt factor flag FSxxx and the interrupt enable register ESxxx for the respective interrupt factors are provided and then the interrupt enable/disable can be selected by the software. In addition, a priority level of the serial interface interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PSIFx0 and PSIFx1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see "5.14 Interrupt and Standby Status".
Figure 5.7.9.1 shows the configuration of the serial interface interrupt circuit.

■ Transmitting complete interrupt

This interrupt factor is generated at the point where the sending of the data written into the shift register has been completed and sets the interrupt factor flag FSTRAx to "1". When set in this manner, if the corresponding interrupt enable register ESTRAx is set to "1" and the corresponding interrupt priority registers PSIFx0 and PSIFx1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. When "0" has been written into the interrupt enable register ESTRAx and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSTRAx is set to "1".
The interrupt factor flag FSTRAx is reset to "0" by writing "1".
The following transmitting data can be set and the transmitting start (writing "1" to TXTRGx) can be controlled by generation of this interrupt factor.

The exception processing vector address for each channel is set as follows:

Ch. 0 transmitting complete interrupt: 00002CH
Ch. 1 transmitting complete interrupt: 000050H

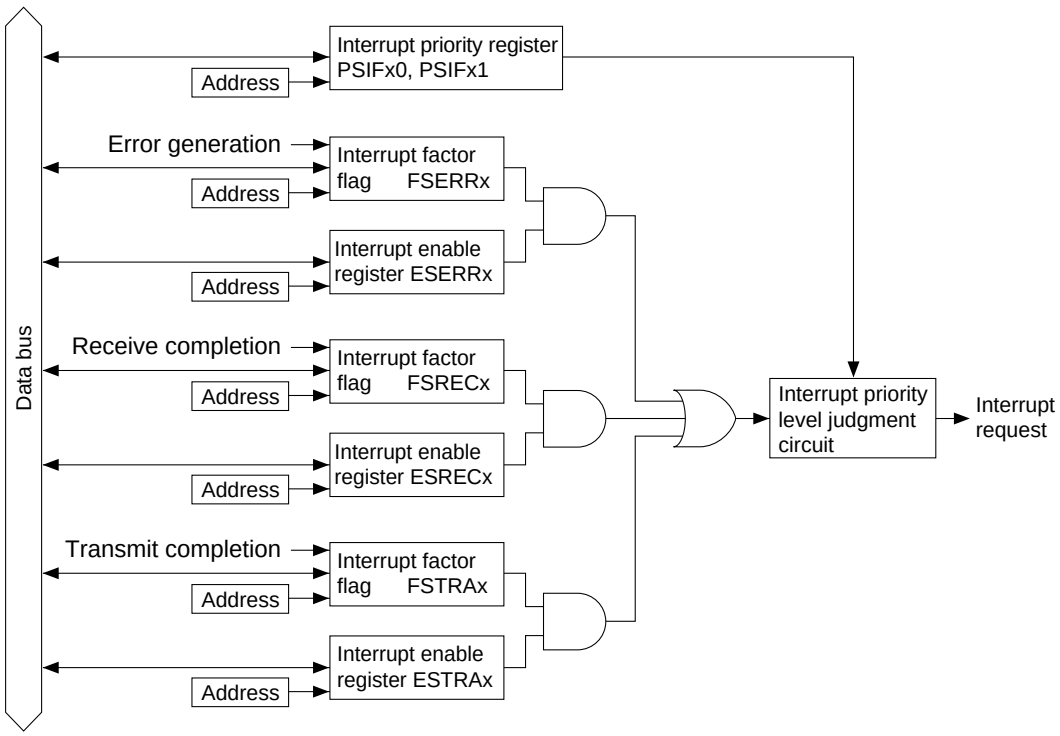


Fig. 5.7.9.1 Configuration of serial interface interrupt circuit

■ Receiving complete interrupt

This interrupt factor is generated at the point where receiving has been completed and the receive data incorporated into the shift register has been transferred into the received data buffer and it sets the interrupt factor flag FSRECx to "1". When set in this manner, if the corresponding interrupt enable register ESRECx is set to "1" and the corresponding interrupt priority registers PSIFx0 and PSIFx1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. When "0" has been written into the interrupt enable register ESRECx and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSRECx is set to "1".
The interrupt factor flag FSRECx is reset to "0" by writing "1".

The generation of this interrupt factor permits the received data to be read.

Also, the interrupt factor flag is set to "1" when a parity error or framing error is generated.

The exception processing vector address for each channel is set as follows:

Ch. 0 receiving complete interrupt: 00002AH
Ch. 1 receiving complete interrupt: 00004EH

■ Error interrupt

This interrupt factor is generated at the point where a parity error, framing error or overrun error is detected during receiving and it sets the interrupt factor flag FSERRx to "1". When set in this manner, if the corresponding interrupt enable register ESERRx is set to "1" and the corresponding interrupt priority registers PSIFx0 and PSIFx1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. When "0" has been written in the interrupt enable register ESERRx and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSERRx is set to "1".
The interrupt factor flag FSERRx is reset to "0" by writing "1".

Since all three types of errors result in the same interrupt factor, you should identify the error that has been generated by the error flags PERx (parity error), OERx (overrun error) and FERx (framing error).

The exception processing vector address for each channel is set as follows:

Ch. 0 receive error interrupt: 000028H
Ch. 1 receive error interrupt: 00004CH

5.7.10 Control of serial interface

Table 5.7.10.1 show the serial interface control bits.

Table 5.7.10.1(a) Serial interface control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF48	D7	–	–		–	–	–		"0" when being read
	D6	EPR0	Serial I/F 0 parity enable register		With parity	Non parity	0	R/W	Only for
	D5	PMD0	Serial I/F 0 parity mode selection		Odd	Even	0	R/W	asynchronous mode
	D4	SCS01	Serial I/F 0 clock source selection				0	R/W	In the clock synchro-
			SCS01 SCS00 Clock source						nous slave mode,
			1 1 Programmable timer 1						external clock is
	D3	SCS00	1 0 fOSC3 / 4				0	R/W	selected.
			0 1 fOSC3 / 8						
			0 0 fOSC3 / 16						
	D2	SMD01	Serial I/F 0 mode selection				0	R/W	
			SMD01 SMD00 Mode						
			1 1 Asynchronous 8-bit						
	D1	SMD00	1 0 Asynchronous 7-bit				0	R/W	
			0 1 Clock synchronous slave						
			0 0 Clock synchronous master						
	D0	ESIF0	Serial I/F 0 enable register		Serial I/F	I/O port	0	R/W	
00FF49	D7	–	–		–	–	–		"0" when being read
	D6	FER0	Serial I/F 0 framing error flag	R	Error	No error	0	R/W	Only for
				W	Reset (0)	No operation			asynchronous mode
	D5	PER0	Serial I/F 0 parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER0	Serial I/F 0 overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG0	Serial I/F 0 receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN0	Serial I/F 0 receive enable		Enable	Disable	0	R/W	
	D1	TXTRG0	Serial I/F 0 transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN0	Serial I/F 0 transmit enable		Enable	Disable	0	R/W	
00FF4A	D7	TRXD07	Serial I/F 0 transmit/Receive data D7 (MSB)		High	Low	X	R/W	Reading:
	D6	TRXD06	Serial I/F 0 transmit/Receive data D6				X	R/W	Receive data
	D5	TRXD05	Serial I/F 0 transmit/Receive data D5				X	R/W	Writing:
	D4	TRXD04	Serial I/F 0 transmit/Receive data D4				X	R/W	Transmit data
	D3	TRXD03	Serial I/F 0 transmit/Receive data D3				X	R/W	
	D2	TRXD02	Serial I/F 0 transmit/Receive data D2				X	R/W	
	D1	TRXD01	Serial I/F 0 transmit/Receive data D1				X	R/W	
	D0	TRXD00	Serial I/F 0 transmit/Receive data D0 (LSB)				X	R/W	
00FF4B	D7	IRTL0	Serial I/F 0 IrDA I/F output logic inverse		Inverse	Direct	0	R/W	
	D6	IRIL0	Serial I/F 0 IrDA I/F input logic inverse		Inverse	Direct	0	R/W	
	D5	–	–		–	–	–		"0" when being read
	D4	IRST0	Serial I/F 0 IrDA interface enable		IrDA	Normal	0	R/W	
	D3	–	–		–	–	–		Constantly "0" when
	D2	–	–		–	–	–		being read
	D1	STPB0	Serial I/F 0 stop bit selection		2 bits	1 bit	0	R/W	
	D0	SDP0	Serial I/F 0 data input/output permutation selection		MSB first	LSB first	0	R/W	

Table 5.7.10.1(b) Serial interface control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF4C	D7	–	–		–	–	–		"0" when being read
	D6	EPR1	Serial I/F 1 parity enable register		With parity	Non parity	0	R/W	Only for
	D5	PMD1	Serial I/F 1 parity mode selection		Odd	Even	0	R/W	asynchronous mode
	D4	SCS11	Serial I/F 1 clock source selection				0	R/W	In the clock synchro-
			SCS11 SCS10 Clock source						nous slave mode,
			1 1 Programmable timer 7						external clock is
	D3	SCS10	1 0 f_{OSC3} / 4				0	R/W	selected.
			0 1 f_{OSC3} / 8						
			0 0 f_{OSC3} / 16						
	D2	SMD11	Serial I/F 1 mode selection				0	R/W	
			SMD11 SMD10 Mode						
			1 1 Asynchronous 8-bit						
	D1	SMD10	1 0 Asynchronous 7-bit				0	R/W	
			0 1 Clock synchronous slave						
			0 0 Clock synchronous master						
	D0	ESIF1	Serial I/F 1 enable register		Serial I/F	I/O port	0	R/W	
00FF4D	D7	–	–		–	–	–		"0" when being read
	D6	FER1	Serial I/F 1 framing error flag	R	Error	No error	0	R/W	Only for
				W	Reset (0)	No operation			asynchronous mode
	D5	PER1	Serial I/F 1 parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER1	Serial I/F 1 overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG1	Serial I/F 1 receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN1	Serial I/F 1 receive enable		Enable	Disable	0	R/W	
	D1	TXTRG1	Serial I/F 1 transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN1	Serial I/F 1 transmit enable		Enable	Disable	0	R/W	
00FF4E	D7	TRXD17	Serial I/F 1 transmit/Receive data D7 (MSB)		High	Low	X	R/W	Reading:
	D6	TRXD16	Serial I/F 1 transmit/Receive data D6				X	R/W	Receive data
	D5	TRXD15	Serial I/F 1 transmit/Receive data D5				X	R/W	Writing:
	D4	TRXD14	Serial I/F 1 transmit/Receive data D4				X	R/W	Transmit data
	D3	TRXD13	Serial I/F 1 transmit/Receive data D3				X	R/W	
	D2	TRXD12	Serial I/F 1 transmit/Receive data D2				X	R/W	
	D1	TRXD11	Serial I/F 1 transmit/Receive data D1				X	R/W	
	D0	TRXD10	Serial I/F 1 transmit/Receive data D0 (LSB)				X	R/W	
00FF4F	D7	IRTL1	Serial I/F 1 IrDA I/F output logic inverse		Inverse	Direct	0	R/W	
	D6	IRIL1	Serial I/F 1 IrDA I/F input logic inverse		Inverse	Direct	0	R/W	
	D5	–	–		–	–	–		"0" when being read
	D4	IRST1	Serial I/F 1 IrDA interface enable		IrDA	Normal	0	R/W	
	D3	–	–		–	–	–		Constantly "0" when
	D2	–	–		–	–	–		being read
	D1	STPB1	Serial I/F 1 stop bit selection		2 bits	1 bit	0	R/W	
	D0	SDP1	Serial I/F 1 data input/output permutation selection		MSB first	LSB first	0	R/W	

Table 5.7.10.1(c) Serial interface control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF01 PSIF00 PSW1 PSW0 PTM1 PTM0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF01	Serial interface 0 interrupt priority register			0	R/W	
	D4	PSIF00						
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0						
00FF21	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	PPT3	Programmable timer 3–2 interrupt	PPT3 PPT2 PPT1 PPT0 PSIF11 PSIF10 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D4	PPT2	priority register					
	D3	PPT1	Programmable timer 1–0 interrupt			0	R/W	
	D2	PPT0	priority register					
	D1	PSIF11	Serial interface 1 interrupt priority register			0	R/W	
	D0	PSIF10						
00FF23	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	ESERR1	Serial I/F 1 (error) interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D4	ESREC1	Serial I/F 1 (receiving) interrupt enable register					
	D3	ESTRA1	Serial I/F 1 (transmitting) interrupt enable register					
	D2	ESERR0	Serial I/F 0 (error) interrupt enable register					
	D1	ESREC0	Serial I/F 0 (receiving) interrupt enable register					
	D0	ESTRA0	Serial I/F 0 (transmitting) interrupt enable register					
00FF27	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	FSERR1	Serial I/F 1 (error) interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D4	FSREC1	Serial I/F 1 (receiving) interrupt factor flag					
	D3	FSTRA1	Serial I/F 1 (transmitting) interrupt factor flag					
	D2	FSERR0	Serial I/F 0 (error) interrupt factor flag					
	D1	FSREC0	Serial I/F 0 (receiving) interrupt factor flag					
	D0	FSTRA0	Serial I/F 0 (transmitting) interrupt factor flag					

ESIF0: 00FF48H•D0
ESIF1: 00FF4CH•D0

Sets the serial interface terminals (P10–P13, P20–P23).

When "1" is written: Serial input/output terminal
When "0" is written: I/O port terminal
Reading: Valid

The ESIFx is the serial interface enable register and P10–P13/P20–P23 terminals become serial input/output terminals (SINx, SOUTx, $\overline{SCLKx}$, $\overline{SRDYx}$) when "1" is written, and they become I/O port terminals when "0" is written.
Also, see Table 5.7.3.2 for the terminal settings according to the transfer modes.
At initial reset, ESIFx is set to "0" (I/O port).

SMD00, SMD01: 00FF48H•D1, D2
SMD10, SMD11: 00FF4CH•D1, D2

Set the transfer modes according to Table 5.7.10.2.

Table 5.7.10.2 Transfer mode settings

SMDx1	SMDx0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

SMDx0 and SMDx1 can also read out.
At initial reset, this register is set to "0" (clock synchronous master mode).

SCS00, SCS01: 00FF48H•D3, D4
SCS10, SCS11: 00FF4CH•D3, D4

Select the clock source according to Table 5.7.10.3.

Table 5.7.10.3 Clock source selection

SCSx1	SCSx0	Clock source
1	1	Programmable timer 1 (Ch.0)
		Programmable timer 7 (Ch.1)
1	0	fOSC3 / 4
0	1	fOSC3 / 8
0	0	fOSC3 / 16

SCSx0 and SCSx1 can also be read out.
In the clock synchronous slave mode, setting of this register is invalid.
At initial reset, this register is set to "0" (fOSC3 / 16).

SDP0: 00FF4BH•D0
SDP1: 00FF4FH•D0

Selects the serial data input / output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input / output permutation will be MSB first or LSB first.
At initial reset, SDPx is set to "0" (LSB first).

STPB0: 00FF4BH•D1
STPB1: 00FF4FH•D1

Selects the stop bit length for asynchronous data transfer.

When "1" is written: 2 bits
When "0" is written: 1 bit
Reading: Valid

STPBx is the stop bit select register that is effective in asynchronous mode. When "1" is written to STPBx, the stop bit length is set to 2 bits, and when "0" is written, it is set to 1 bit.
In clock synchronous mode, no start / stop bits can be added to transfer data. Therefore, setting STPBx becomes invalid.
At initial reset, STPBx is set to "0" (1 bit).

EPR0: 00FF48H•D6
EPR1: 00FF4CH•D6

Selects the parity function.

When "1" is written: With parity
When "0" is written: Non parity
Reading: Valid

Selects whether or not to check parity of the received data and to add a parity bit to the transmitting data. When "1" is written to EPRx, the most significant bit of the received data is considered to be the parity bit and a parity check is executed. A parity bit is added to the transmitting data. When "0" is written, neither checking is done nor is a parity bit added.
Parity is valid only in asynchronous mode and the EPRx setting becomes invalid in the clock synchronous mode.
At initial reset, EPRx is set to "0" (non parity).

PMD0: 00FF48H•D5
PMD1: 00FF4CH•D5

Selects odd parity / even parity.

When "1" is written: Odd parity
When "0" is written: Even parity
Reading: Valid

When "1" is written to PMDx, odd parity is selected and even parity is selected when "0" is written. The parity check and addition of a parity bit is only valid when "1" has been written to EPRx. When "0" has been written to EPRx, the parity setting by PMDx becomes invalid.
At initial reset, PMDx is set to "0" (even parity).

TXEN0: 00FF49H•D0
TXEN1: 00FF4DH•D0

Sets the serial interface to the transmitting enable status.

When "1" is written: Transmitting enable
When "0" is written: Transmitting disable
Reading: Valid

When "1" is written to TXENx, the serial interface shifts to the transmitting enable status and shifts to the transmitting disable status when "0" is written. Set TXENx to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, TXENx is set to "0" (transmitting disable).

TXTRG0: 00FF49H•D1
TXTRG1: 00FF4DH•D1

Functions as the transmitting start trigger and the operation status indicator (transmitting / stop status).

When "1" is read: During transmitting
When "0" is read: During stop

When "1" is written: Transmitting start
When "0" is written: Invalid

Starts the transmitting when "1" is written to TXTRGx after writing the transmitting data.
TXTRGx can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
At initial reset, TXTRGx is set to "0" (during stop).

RXEN0: 00FF49H•D2
RXEN1: 00FF4DH•D2

Sets the serial interface to the receiving enable status.

When "1" is written: Receiving enable
When "0" is written: Receiving disable
Reading: Valid

When "1" is written to RXENx, the serial interface shifts to the receiving enable status and shifts to the receiving disable status when "0" is written.
Set RXENx to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, RXENx is set to "0" (receiving disable).

RXTRG0: 00FF49H•D3
RXTRG1: 00FF4DH•D3

Functions as the receiving start trigger or preparation for the following data receiving and the operation status indicator (during receiving / during stop).

When "1" is read: During receiving
When "0" is read: During stop

When "1" is written: Receiving start / following data receiving preparation
When "0" is written: Invalid

RXTRGx has a slightly different operation in the clock synchronous system and the asynchronous system.

The RXTRGx in the clock synchronous system, is used as the trigger for the receiving start.
Writes "1" into RXTRGx to start receiving at the point where the receive data has been read and the following receive preparation has been done. (In the slave mode, $\overline{\text{SRDY}}$x becomes "0" at the point where "1" has been written into the RXTRGx.)

RXTRGx is used in the asynchronous system for preparation of the following data receiving. Reads the received data located in the received data buffer and writes "1" into RXTRGx to inform that the received data buffer has shifted to empty. When "1" has not been written to RXTRGx, the overrun error flag OERx is set to "1" at the point where the following receiving has been completed. (When the receiving has been completed between the operation to read the received data and the operation to write "1" into RXTRGx, an overrun error occurs.)

In addition, RXTRGx can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRGx is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
At initial reset, RXTRGx is set to "0" (during stop).

TRXD00–TRXD07: 00FF4AH
TRXD10–TRXD17: 00FF4EH

During transmitting

Write the transmitting data into the transmit shift register.

When "1" is written: HIGH level
When "0" is written: LOW level

Write the transmitting data prior to starting transmitting.
In the case of continuous transmitting, wait for the transmitting complete interrupt, then write the data.
The TRXDx7 becomes invalid for the asynchronous 7-bit mode.
Converted serial data for which the bits set at "1" as HIGH (V_{DD}) level and for which the bits set at "0" as LOW (V_{SS}) level are output from the SOUTx terminal.

During receiving

Read the received data.

When "1" is read: HIGH level
When "0" is read: LOW level

The data from the received data buffer can be read out.
Since the sift register is provided separately from this buffer, reading can be done during the receive operation in the asynchronous mode. (The buffer function is not used in the clock synchronous mode.)
Read the data after waiting for the receiving complete interrupt.
When performing parity check in the asynchronous 7-bit mode, "0" is loaded into the 8th bit (TRXDx7) that corresponds to the parity bit.
The serial data input from the SINx terminal is level converted, making the HIGH (V_{DD}) level bit "1" and the LOW (V_{SS}) level bit "0" and is then loaded into this buffer.
At initial reset, the buffer content is undefined.

OER0: 00FF49H•D4
OER1: 00FF4DH•D4

Indicates the generation of an overrun error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

OERx is an error flag that indicates the generation of an overrun error and becomes "1" when an error has been generated.
An overrun error is generated when the receiving of data has been completed prior to the writing of "1" to RXTRGx in the asynchronous mode.
OERx is reset to "0" by writing "1".
At initial reset and when RXENx is "0", OERx is set to "0" (no error).

PER0: 00FF49H•D5
PER1: 00FF4DH•D5

Indicates the generation of a parity error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

PERx is an error flag that indicates the generation of a parity error and becomes "1" when an error has been generated.
When a parity check is performed in the asynchronous mode, if data that does not match the parity is received, a parity error is generated.
PERx is reset to "0" by writing "1".
At initial reset and when RXENx is "0", PERx is set to "0" (no error).

FER0: 00FF49H•D6
FER1: 00FF4DH•D6

Indicates the generation of a framing error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

FERx is an error flag that indicates the generation of a framing error and becomes "1" when an error has been generated.
When the stop bit for the receiving of the asynchronous mode has become "0", a framing error is generated.
FERx is reset to "0" by writing "1".
At initial reset and when RXENx is "0", FERx is set to "0" (no error).

IRST0: 00FF4BH•D4
IRST1: 00FF4FH•D4

Enables the IrDA interface function.

When "1" is written: IrDA interface
When "0" is written: Normal interface
Reading: Valid

Write "1" to IRSTx to use the IrDA interface function. Write "0" when the IrDA interface function is not used.
At initial reset, this register is set to "0" (normal interface).

IRTL0: 00FF4BH•D7
IRTL1: 00FF4FH•D7

Inverts the logic of the IrDA output signal.

When "1" is written: Inverted
When "0" is written: Not inverted
Reading: Valid

This register is used to configure the logic of the SOUTx output signal according to the external infrared-ray communication module when the IrDA interface function is used. When "1" is written to IRTLx, the SOUTx terminal is set so that it will output a HIGH pulse when the output data is "0" (the terminal maintains LOW when the output data is "1"). When "0" is written to IRTLx, the SOUTx terminal is set so that it will output a LOW pulse when the output data is "0" (the terminal maintains HIGH when the output data is "1").
At initial reset, this register is set to "0" (not inverted).

IRIL0: 00FF4BH•D6
IRIL1: 00FF4FH•D6

Inverts the logic of the IrDA input signal.

When "1" is written: Inverted
When "0" is written: Not inverted
Reading: Valid

This register is used to configure the logic of the input signal from the external infrared-ray communication module according to the built-in serial interface when the IrDA interface function is used. When "1" is written to IRILx, the serial interface inputs a HIGH pulse as data bit "0". When "0" is written to IRILx, the serial interface inputs a LOW pulse as data bit "0".
At initial reset, this register is set to "0" (not inverted).

PSIF00, PSIF01: 00FF21H•D0, D1
PSIF10, PSIF11: 00FF21H•D2, D3

Sets the priority level of the serial interface interrupt.
The two bits PSIFx0 and PSIFx1 are the interrupt priority register corresponding to the serial interface interrupt. Table 5.7.10.4 shows the interrupt priority level which can be set by this register.

Table 5.7.10.4 Interrupt priority level settings

PSIFx1	PSIFx0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ESTRA0, ESREC0, ESERR0: 00FF24H•D0, D1, D2
ESTRA1, ESREC1, ESERR1: 00FF24H•D4, D5, D6

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

ESTRAx, ESRECx and ESERRx are interrupt enable registers that respectively correspond to the interrupt factors for transmitting complete, receiving complete and receiving error. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FSTRA0, FSREC0, FSERR0: 00FF27H•D0, D1, D2
FSTRA1, FSREC1, FSERR1: 00FF27H•D4, D5, D6

Indicates the serial interface interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

FSTRAx, FSRECx and FSERRx are interrupt factor flags that respectively correspond to the interrupts for transmitting complete, receiving complete and receiving error and are set to "1" by generation of each factor.
Transmitting complete interrupt factor is generated at the point where the data transmitting of the shift register has been completed.
Receiving complete interrupt factor is generated at the point where the received data has been transferred into the received data buffer.
Receive error interrupt factor is generated when a parity error, framing error or overrun error has been detected during data receiving.

When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.7.11 Programming notes

(1) Be sure to initialize the serial interface mode in the transmitting / receiving disable status (TXENx = RXENx = "0").

(2) Do not perform double trigger (writing "1") to TXTRGx (RXTRGx) when the serial interface is in the transmitting (receiving) operation. Furthermore, do not execute the SLP instruction. (When executing the SLP instruction, set TXENx = RXENx = "0".)

(3) In the clock synchronous mode, since one clock line ($\overline{SCLKx}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.) Consequently, be sure not to write "1" to RXTRGx (TXTRGx) when TXTRGx (RXTRGx) is "1".

(4) When a parity error or framing error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag FSERRx is set to "1" prior to the receiving complete interrupt factor flag FSRECx for the time indicated in Table 5.7.11.1. Consequently, when an error is generated, you should reset the receiving complete interrupt factor flag FSRECx to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag FSRECx is not set to "1" and a receiving complete interrupt is not generated.

Table 5.7.11.1 Time difference between FSERRx and FSRECx on error generation

Clock source	Time difference
f_{OSC3} / n	1/2 cycles of f_{OSC3} / n
Programmable timer	1 cycle of timer 1/7 underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several tens of µsec to several tens of msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 9, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

5.8 Clock Timer

5.8.1 Configuration of clock timer

The S1C8F626 has built in a clock timer that uses the OSC1 oscillation circuit as clock source. The clock timer is composed of an 8-bit binary counter that uses the 256 Hz signal dividing fOSC1 as its input clock and can read the data of each bit (128–1 Hz) by software.
Normally, this clock timer is used for various timing functions such as clocks.
The configuration of the clock timer is shown in Figure 5.8.1.1.

5.8.2 Interrupt function

The clock timer can generate an interrupt by each of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals.
The configuration of the clock timer interrupt circuit is shown in Figure 5.8.2.1.

Interrupts are generated by respectively setting the corresponding interrupt factor flags FTM32, FTM8, FTM2 and FTM1 at the falling edge of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals to "1". Interrupt can be prohibited by the setting the interrupt enable registers ETM32, ETM8, ETM2 and ETM1 corresponding to each interrupt factor flag.
In addition, a priority level of the clock timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PTM0 and PTM1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see "5.14 Interrupt and Standby Status".

The exception processing vector addresses for each interrupt factor are respectively set as shown below.

32 Hz interrupt:	000034H
8 Hz interrupt:	000036H
2 Hz interrupt:	000038H
1 Hz interrupt:	00003AH

Figure 5.8.2.2 shows the timing chart for the clock timer.

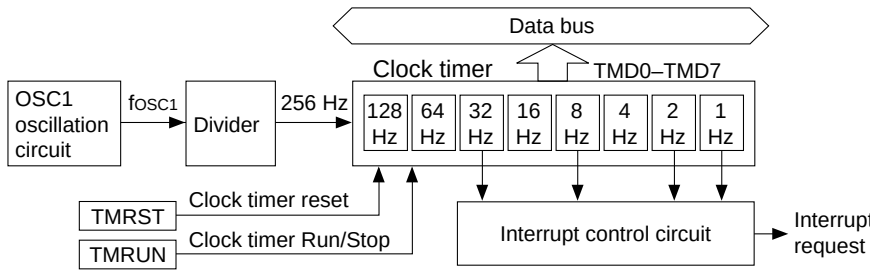


Fig. 5.8.1.1 Configuration of clock timer

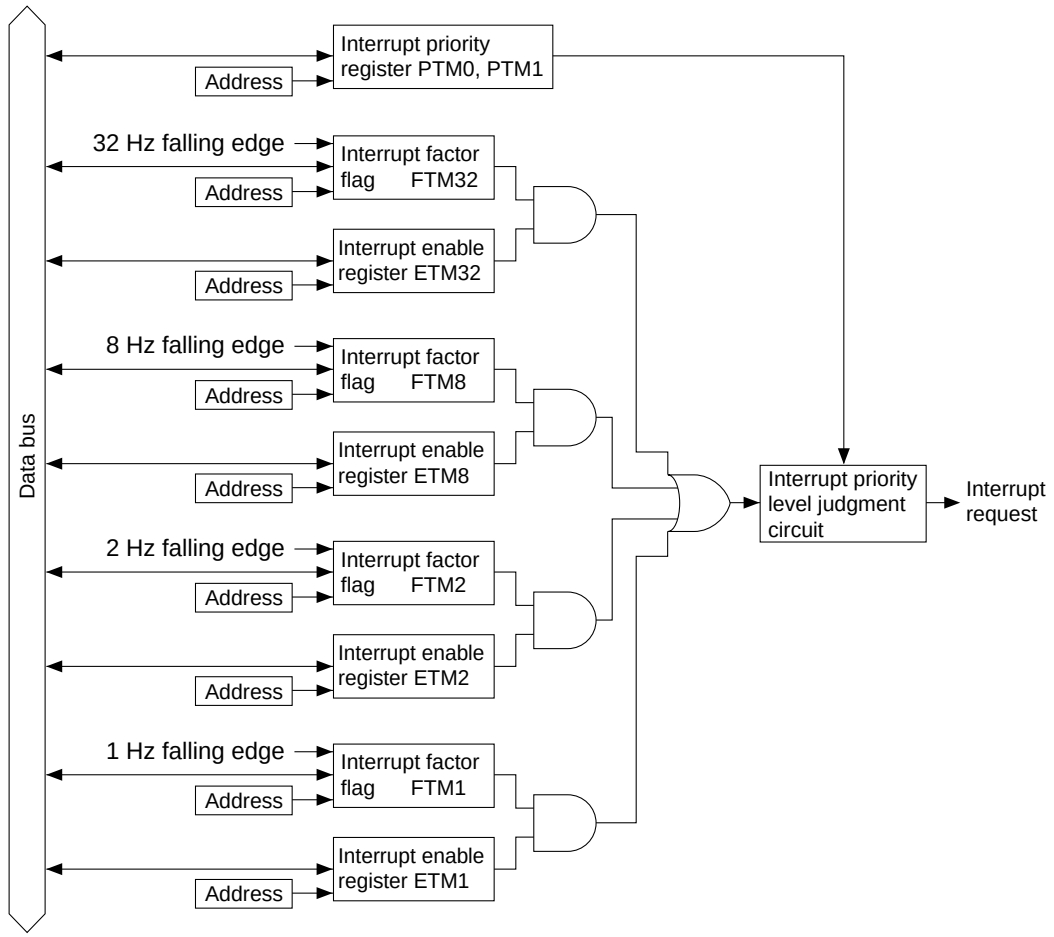


Fig. 5.8.2.1 Configuration of clock timer interrupt circuit

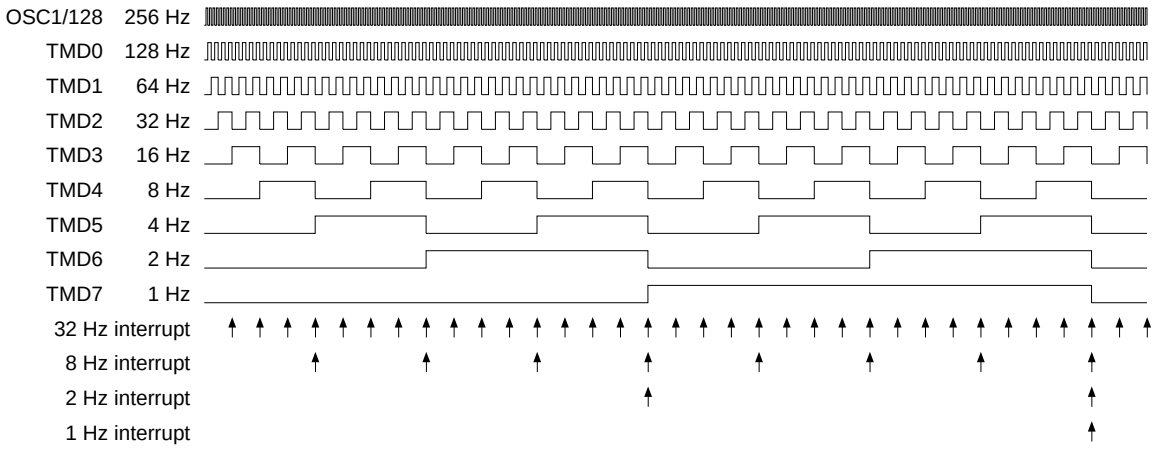


Fig. 5.8.2.2 Timing chart of clock timer

5.8.3 Control of clock timer

Table 5.8.3.1 shows the clock timer control bits.

Table 5.8.3.1 Clock timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	WDEN	Watchdog timer enable	Enable	Disable	1	R/W	
	D6	FOUT2	FOUT frequency selection FOUT2 FOUT1 FOUT0 Frequency 1 1 1 fOSC3 / 8 1 1 0 fOSC3 / 4 1 0 1 fOSC3 / 2 1 0 0 fOSC3 / 1 0 1 1 fOSC1 / 8 0 1 0 fOSC1 / 4 0 0 1 fOSC1 / 2 0 0 0 fOSC1 / 1			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when being read
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF41	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz					
	D5	TMD5	Clock timer data 4 Hz					
	D4	TMD4	Clock timer data 8 Hz					
	D3	TMD3	Clock timer data 16 Hz					
	D2	TMD2	Clock timer data 32 Hz					
	D1	TMD1	Clock timer data 64 Hz					
	D0	TMD0	Clock timer data 128 Hz					
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF01 PSIF00 PSW1 PSW0 Priority PTM1 PTM0 level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF01	Serial interface 0 interrupt priority register			0	R/W	
	D4	PSIF00						
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0						
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register					
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register					
	D3	ETM32	Clock timer 32 Hz interrupt enable register					
	D2	ETM8	Clock timer 8 Hz interrupt enable register					
	D1	ETM2	Clock timer 2 Hz interrupt enable register					
	D0	ETM1	Clock timer 1 Hz interrupt enable register					
00FF26	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag					
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag					
	D3	FTM32	Clock timer 32 Hz interrupt factor flag					
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag					
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					

TMD0–TMD7: 00FF41H

The clock timer data can be read out.
Each bit of TMD0–TMD7 and frequency correspondence are as follows:

TMD0:	128 Hz	TMD4:	8 Hz
TMD1:	64 Hz	TMD5:	4 Hz
TMD2:	32 Hz	TMD6:	2 Hz
TMD3:	16 Hz	TMD7:	1 Hz

Since the TMD0–TMD7 is exclusively for reading, the write operation is invalid.
At initial reset, the timer data is set to "00H".

TMRST: 00FF40H•D1

Resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

The clock timer is reset by writing "1" to the TMRST.
When the clock timer is reset in the RUN status, it restarts immediately after resetting. In the case of the STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to the TMRST.
Since the TMRST is exclusively for writing, it always becomes "0" during reading.

TMRUN: 00FF40H•D0

Controls RUN / STOP of the clock timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The clock timer starts up-counting by writing "1" to the TMRUN and stops by writing "0".
In the STOP status, the count data is maintained until it is reset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the TMRUN is set to "0" (STOP).

PTM0, PTM1: 00FF20H•D0, D1

Sets the priority level of the clock timer interrupt. The two bits PTM0 and PTM1 are the interrupt priority register corresponding to the clock timer interrupt. Table 5.8.3.2 shows the interrupt priority level which can be set by this register.

Table 5.8.3.2 Interrupt priority level settings

PTM1	PTM0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ETM1, ETM2, ETM8, ETM32: 00FF22H•D0–D3

Enables or disables the generation of an interrupt for the CPU.

When "1" is written:	Interrupt enabled
When "0" is written:	Interrupt disabled
Reading:	Valid

The ETM1, ETM2, ETM8 and ETM32 are interrupt enable registers that respectively correspond to the interrupt factors for 1 Hz, 2 Hz, 8 Hz and 32 Hz. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FTM1, FTM2, FTM8, FTM32: 00FF26H•D0–D3

Indicates the clock timer interrupt generation status.

When "1" is read:	Interrupt factor present
When "0" is read:	Interrupt factor not present
When "1" is written:	Resets factor flag
When "0" is written:	Invalid

The FTM1, FTM2, FTM8 and FTM32 are interrupt factor flags that respectively correspond to the interrupts for 1 Hz, 2 Hz, 8 Hz and 32 Hz and are set to "1" at the falling edge of each signal.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.8.4 Programming notes

(1) The clock timer is actually made to RUN / STOP in synchronization with the falling edge of the 256 Hz signal after writing to the TMRUN register. Consequently, when "0" is written to the TMRUN, the timer shifts to STOP status when the counter is incremented "1". The TMRUN maintains "1" for reading until the timer actually shifts to STOP status.
Figure 5.8.4.1 shows the timing chart of the RUN / STOP control.

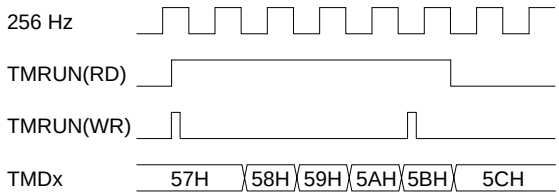


Fig. 5.8.4.1 Timing chart of RUN/STOP control

(2) The SLP instruction is executed when the clock timer is in the RUN status (TMRUN = "1"). The clock timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (TMRUN = "0") prior to executing the SLP instruction.

5.9 Stopwatch Timer

5.9.1 Configuration of stopwatch timer

The S1C8F626 has a built-in 1/100 sec and 1/10 sec stopwatch timer. The stopwatch timer is composed of a 4-bit 2 stage BCD counter (1/100 sec units and 1/10 sec units) that makes the 256 Hz signal that divides the fOSC1 the input clock and it can read the count data by software.
Figure 5.9.1.1 shows the configuration of the stopwatch timer.
The stopwatch timer can be used as a timer different from the clock timer and can easily realize stopwatch and other such functions by software.

5.9.2 Count up pattern

The stopwatch timer is respectively composed of the 4-bit BCD counters SWD0–SWD3 and SWD4–SWD7.

Figure 5.9.2.1 shows the count up pattern of the stopwatch timer.

The feedback dividing circuit generates an approximate 100 Hz signal at 2/256 sec and 3/256 sec intervals from a 256 Hz signal divided from fOSC1.

The 1/100 sec counter (SWD0–SWD3) generates an approximate 10 Hz signal at 25/256 sec and 26/256 sec intervals by counting the approximate 100 Hz signal generated by the feedback dividing circuit in 2/256 sec and 3/256 sec intervals. The count-up is made approximately 1/100 sec counting by the 2/256 sec and 3/256 sec intervals.

The 1/10 sec counter (SWD4–SWD7) generates a 1 Hz signal by counting the approximate 10 Hz signal generated by the 1/100 sec counter at 25/256 sec and 26/256 sec intervals in 4:6 ratios.

The count-up is made approximately 1/10 sec counting by 25/256 sec and 26/256 sec intervals.

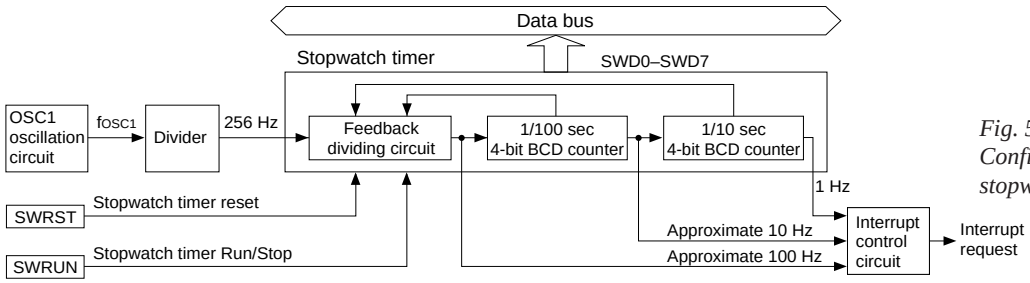


Fig. 5.9.1.1 Configuration of stopwatch timer

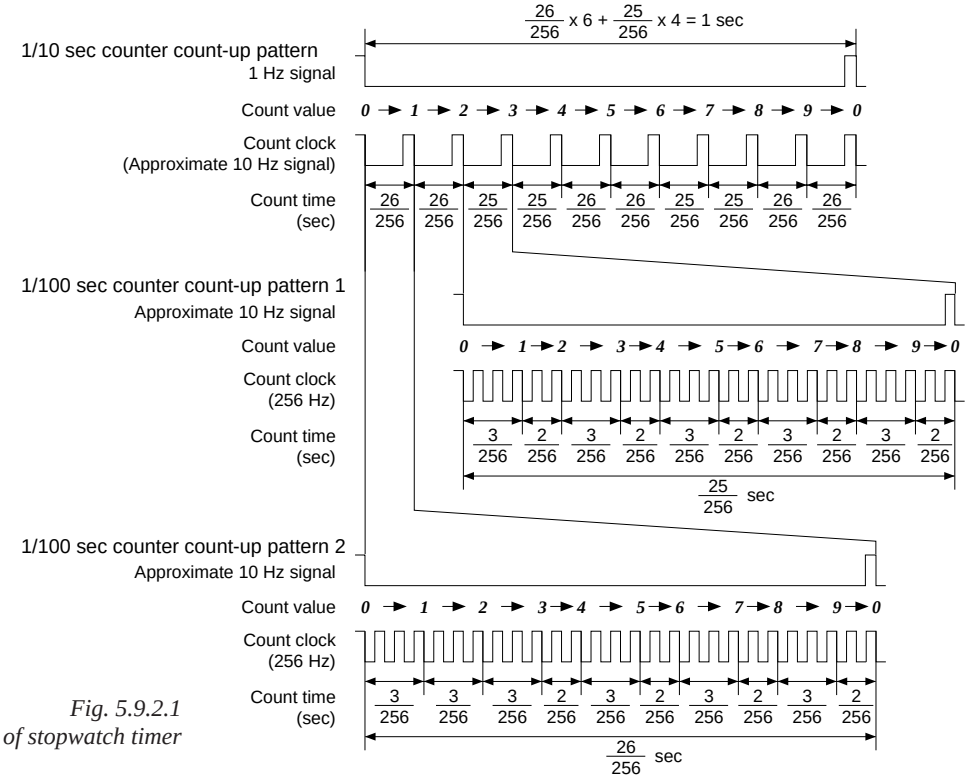


Fig. 5.9.2.1 Count-up pattern of stopwatch timer

5.9.3 Interrupt function

The stopwatch timer can generate an interrupt by each of the 100 Hz (approximately 100 Hz), 10 Hz (approximately 10 Hz) and 1 Hz signals.
Figure 5.9.3.1 shows the configuration of the stopwatch timer interrupt circuit.

The corresponding factor flags FSW100, FSW10 and FSW1 are respectively set to "1" at the falling edge of the 100 Hz, 10 Hz and 1 Hz signal and an interrupt is generated. Interrupt can be prohibited by the setting of the interrupt enable registers ESW100, ESW10 and ESW1 corresponding to each interrupt factor flag.

In addition, a priority level of the stopwatch timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PSW0 and PSW1.
For details on the above mentioned interrupt control registers and the operation following generation of an interrupt, see "5.14 Interrupt and Standby Status".
The exception processing vector addresses of each interrupt factor are respectively set as shown below.

100 Hz interrupt:	00002EH
10 Hz interrupt:	000030H
1 Hz interrupt:	000032H

Figure 5.9.3.2 shows the timing chart for the stopwatch timer.

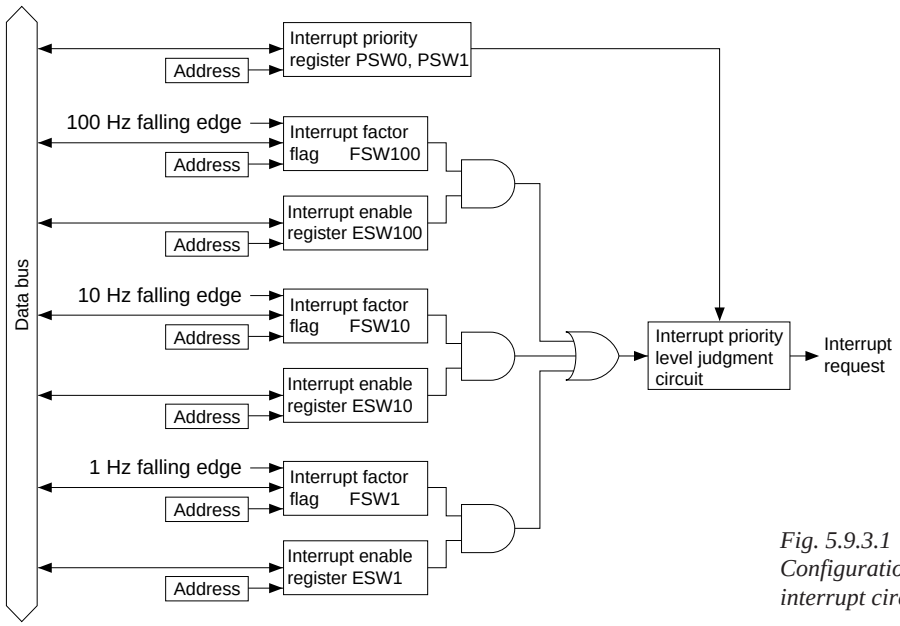


Fig. 5.9.3.1
Configuration of the stopwatch timer interrupt circuit

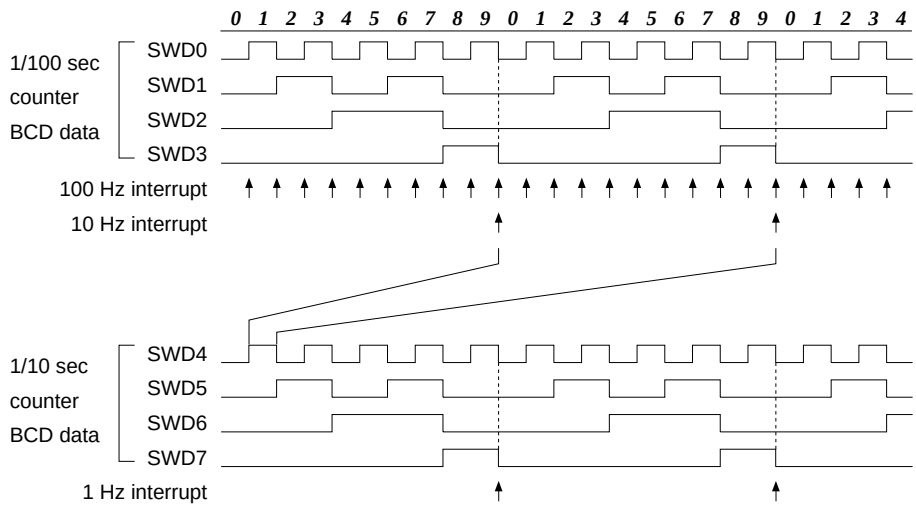


Fig. 5.9.3.2 Stopwatch timer timing chart

5.9.4 Control of stopwatch timer

Table 5.9.4.1 shows the stopwatch timer control bits.

Table 5.9.4.1 Stopwatch timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF42	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SWRST	Stopwatch timer reset	Reset	No operation	–	W	
	D0	SWRUN	Stopwatch timer Run/Stop control	Run	Stop	0	R/W	
00FF43	D7	SWD7	Stopwatch timer data BCD (1/10 sec)			0	R	
	D6	SWD6						
	D5	SWD5						
	D4	SWD4						
	D3	SWD3	Stopwatch timer data BCD (1/100 sec)					
	D2	SWD2						
	D1	SWD1						
	D0	SWD0						
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF01 PSIF00 PSW1 PSW0 PTM1 PTM0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF01	Serial interface 0 interrupt priority register			0	R/W	
	D4	PSIF00						
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0						
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register					
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register					
	D3	ETM32	Clock timer 32 Hz interrupt enable register					
	D2	ETM8	Clock timer 8 Hz interrupt enable register					
	D1	ETM2	Clock timer 2 Hz interrupt enable register					
	D0	ETM1	Clock timer 1 Hz interrupt enable register					
00FF26	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag					
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag					
	D3	FTM32	Clock timer 32 Hz interrupt factor flag					
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag					
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					

SWD0–SWD7: 00FF43H

The stopwatch timer data can be read out.
Higher and lower nibbles and BCD digit correspondence are as follows:

SWD0–SWD3:	BCD (1 / 100 sec)
SWD4–SWD7:	BCD (1 / 10 sec)

Since SWD0–SWD7 are exclusively for reading, the write operation is invalid.
At initial reset, the timer data is set to "00H".

SWRST: 00FF42H•D1

Resets the stopwatch timer.

When "1" is written:	Stopwatch timer reset
When "0" is written:	No operation
Reading:	Always "0"

The stopwatch timer is reset by writing "1" to the SWRST. When the stopwatch timer is reset in the RUN status, it restarts immediately after resetting. In the case of the STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to the SWRST.
Since the SWRST is exclusively for writing, it always becomes "0" during reading.

SWRUN: 00FF42H•D0

Controls RUN / STOP of the stopwatch timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The stopwatch timer starts up-counting by writing "1" to the SWRUN and stops by writing "0".
In the STOP status, the timer data is maintained until it is reset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the SWRUN is set at "0" (STOP).

PSW0, PSW1: 00FF20H•D2, D3

Sets the priority level of the stopwatch timer interrupt.
The two bits PSW0 and PSW1 are the interrupt priority register corresponding to the stopwatch timer interrupt. Table 5.9.4.2 shows the interrupt priority level which can be set by this register.

Table 5.9.4.2 Interrupt priority level settings

PSW1	PSW0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ESW1, ESW10, ESW100: 00FF22H•D4, D5, D6

Enables or disables the generation of an interrupt for the CPU.

When "1" is written:	Interrupt enabled
When "0" is written:	Interrupt disabled
Reading:	Valid

The ESW1, ESW10 and ESW100 are interrupt enable registers that respectively correspond to the interrupt factors for 1 Hz, 10 Hz and 100 Hz. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FSW1, FSW10, FSW100: 00FF26H•D4, D5, D6

Indicates the stopwatch timer interrupt generation status.

When "1" is read:	Interrupt factor present
When "0" is read:	Interrupt factor not present
When "1" is written:	Resets factor flag
When "0" is written:	Invalid

The FSW1, FSW10 and FSW100 are interrupt factor flags that respectively correspond to the interrupts for 1 Hz, 10 Hz and 100 Hz and are set to "1" in synchronization with the falling edge of each signal. When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.9.5 Programming notes

(1) The stopwatch timer is actually made to RUN / STOP in synchronization with the falling edge of the 256 Hz signal after writing to the SWRUN register. Consequently, when "0" is written to the SWRUN, the timer shifts to STOP status when the counter is incremented "1". The SWRUN maintains "1" for reading until the timer actually shifts to STOP status.
Figure 5.9.5.1 shows the timing chart of the RUN / STOP control.

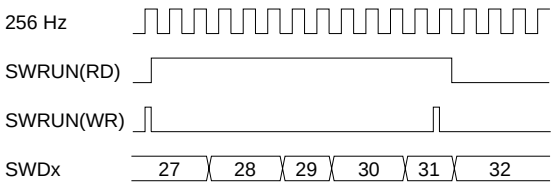


Fig. 5.9.5.1 Timing chart of RUN/STOP control

(2) The SLP instruction is executed when the stopwatch timer is in the RUN status (SWRUN = "1"). The stopwatch timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (SWRUN = "0") prior to executing the SLP instruction.

5.10 Programmable Timer

5.10.1 Configuration of programmable timer

The S1C8F626 has four built-in 16-bit programmable timer systems. Each system timer consists of a 16-bit presettable down counter, and can be used as 16-bit × 1 channel or 8-bit × 2 channels of programmable timer. Furthermore, they function as event counters using the input port terminal. Figures 5.10.1.1 and 5.10.1.2 show the configuration of the 16-bit programmable timers.

Two 8-bit down counters, the reload data register and compare data register corresponding to each down counter are arranged in the 16-bit programmable timer.
The reload data register is used to set an initial value to the down counter.
The compare data register stores data for comparison with the content of the down counter. By setting these registers, a PWM waveform is generated and it can be output to external devices as the TOUT0, 1, 2 or 3 signal. Furthermore, the serial interface clocks are generated from the Timer 1 and 7 underflow signals. The Timer 5 underflow signal can be used to set the frame frequency for the LCD driver.

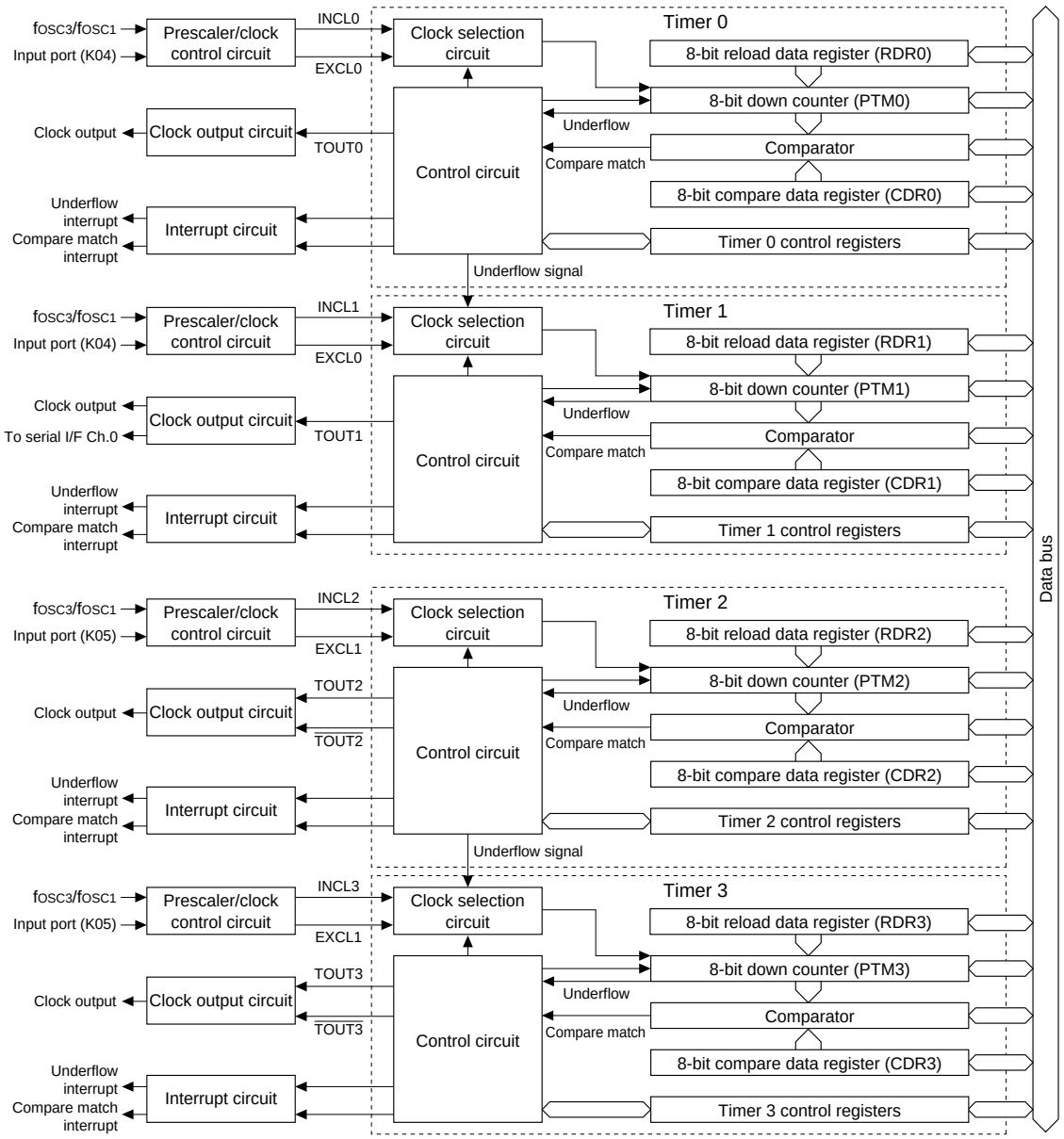


Fig. 5.10.1.1 Configuration of 16-bit programmable timer (Timers 0–3)

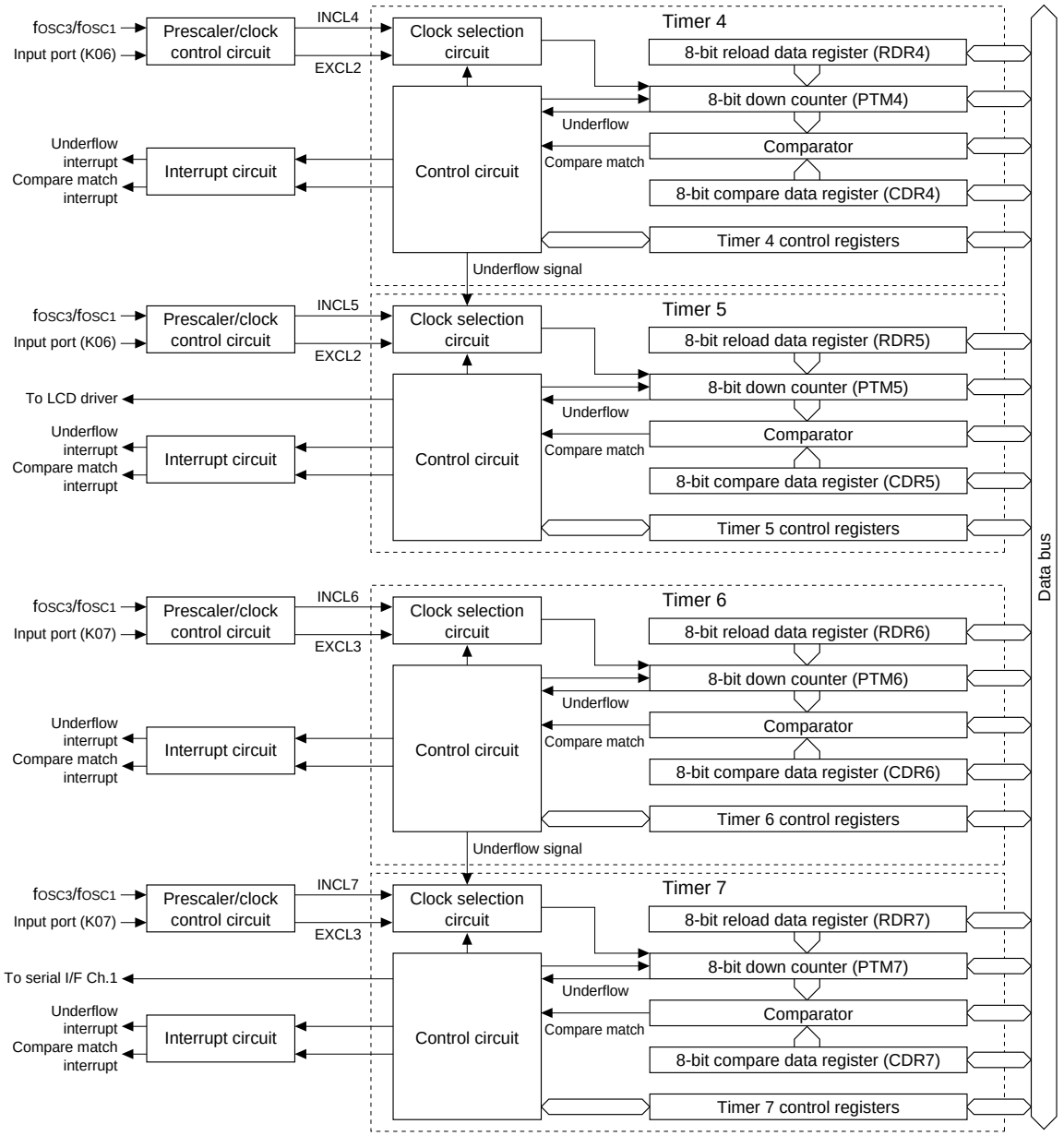


Fig. 5.10.1.2 Configuration of 16-bit programmable timer (Timers 4–7)

5.10.2 Operation mode

Timers 0 and 1, Timers 2 and 3, Timers 4 and 5, or Timers 6 and 7 can be used as two channels of 8-bit timers or one channel of 16-bit timer. Two kinds of operation modes are provided corresponding to this configuration, and it can be selected by the 8/16-bit mode selection registers MODE16_A (for Timer 0–1) through MODE16_D (for Timer 6–7). When "0" is set to the MODE16_A register, Timers 0 and 1 enter the 8-bit mode (8-bit × 2 channels) and when "1" is set, they enter the 16-bit mode (16-bit × 1 channel).

In the 8-bit mode, Timers 0 and 1 can be controlled individually.
In the 16-bit mode, the underflow signal of Timer 0 is used as the input clock of Timer 1 so that the down counters operate as a 16-bit counter.
The timer in the 16-bit mode is controlled with the control registers for Timer 0 except for the clock output.
MODE16_B through MODE16_D have the same function.

Figure 5.10.2.1 shows the timer configuration depending on the operation mode and Table 5.10.2.1 shows the configuration of the control registers.

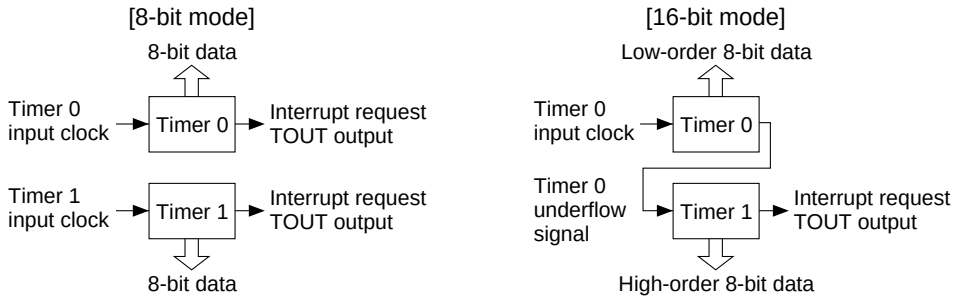


Fig. 5.10.2.1 Counter configuration in 8- and 16-bit mode (example of Timers 0 and 1)

Table 5.10.2.1(a) Control registers in 8-bit mode (example of Timers 0 and 1)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	MODE16_A	PTM0–1 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_A	External clock 0 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT0	PTM0 clock output control	On	Off	0	R/W	
	D2	PTRUN0	PTM0 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET0	PTM0 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL0	PTM0 input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT1	PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	PTM1 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET1	PTM1 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL1	PTM1 input clock selection	External clock	Internal clock	0	R/W	

Table 5.10.2.1(b) Control registers in 16-bit mode (example of Timers 0 and 1)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	MODE16_A	PTM0–1 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_A	External clock 0 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	–	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	Reserved register
	D3	PTOUT0	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	
	D2	PTRUN0	PTM0 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET0	PTM0 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL0	PTM0 input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT1	PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	
	D1	PSET1	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	W	"0" when being read
	D0	CKSEL1	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	

Note: The register names contain a timer number (0–7) to identify the timer to which the register belongs. The following explanation uses "x" instead of the timer number except when it is required. For example, PTRUNx represents PTRUN0 through PTRUN7. Furthermore, a pair of timers are described as Timer(L) and Timer(H) in explanations for 16-bit mode.
Timer(L) = Timer 0, Timer 2, Timer 4 or Timer 6
Timer(H) = Timer 1, Timer 3, Timer 5 or Timer 7

This is used for register names.

5.10.3 Setting of input clock

The clock to be input to the counter can be selected from either the internal clock or external clock by the input clock selection register (CKSEL) provided for each timer. The internal clock is an output of the prescaler. The external clock is used for the event counter function. A signal from the input port is used as the count clock.
Table 5.10.3.1 shows the input clock selection register and input clock of each timer.

Table 5.10.3.1 Input clock selection

Timer	Register setting	Input clock
Timer 0	CKSEL0 = "0"	INCL0 (Prescaler)
	CKSEL0 = "1"	EXCL0 (K04 input)
Timer 1	CKSEL1 = "0"	INCL1 (Prescaler)
	CKSEL1 = "1"	EXCL0 (K04 input)
Timer 2	CKSEL2 = "0"	INCL2 (Prescaler)
	CKSEL2 = "1"	EXCL1 (K05 input)
Timer 3	CKSEL3 = "0"	INCL3 (Prescaler)
	CKSEL3 = "1"	EXCL1 (K05 input)
Timer 4	CKSEL4 = "0"	INCL4 (Prescaler)
	CKSEL4 = "1"	EXCL2 (K06 input)
Timer 5	CKSEL5 = "0"	INCL5 (Prescaler)
	CKSEL5 = "1"	EXCL2 (K06 input)
Timer 6	CKSEL6 = "0"	INCL6 (Prescaler)
	CKSEL6 = "1"	EXCL3 (K07 input)
Timer 7	CKSEL7 = "0"	INCL7 (Prescaler)
	CKSEL7 = "1"	EXCL3 (K07 input)

When the external clock is selected, a signal from the input port is input to the programmable timer. An noise rejector is incorporated in the external clock input circuit and it can be enabled / disabled using the external clock noise rejector select registers PTNREN_A through PTNREN_D corresponding to the EXCL0 through EXCL3 inputs. Writing "1" to PTNREN_A (–D) enables the noise rejector for the external clock EXCL0 (–3). The noise rejector regards pulses less than a 16 / f_{OSC1} seconds in width as noise and rejects them (an external clock must have a pulse width at least double the rejected width). When PTNREN_A (–D) is "0", the external clock bypasses the noise rejector.

When the internal clock is used, select a source clock and a division ratio of the prescaler to set the clock frequency for each timer.
The source clock is specified using the source clock selection register PRTFx provided for each timer. When "1" is written to PRTFx, the OSC1 clock is selected as the source clock for Timer x. When "0" is written, the OSC3 clock is selected. The OSC3 oscillation circuit must be on before the OSC3 can be used. See "5.4 Oscillation Circuits and Operating Mode" for the controlling of the OSC3 oscillation circuit.

The prescaler provides the division ratio selection register PSTx0–PSTx2 for each timer. Note that the division ratio varies depending on the selected source clock.

Table 5.10.3.2 Division ratio and control registers

Register			Dividing ratio	
PSTx2	PSTx1	PSTx0	(OSC3)	(OSC1)
1	1	1	f_{OSC3}/4096	f_{OSC1}/128
1	1	0	f_{OSC3}/1024	f_{OSC1}/64
1	0	1	f_{OSC3}/256	f_{OSC1}/32
1	0	0	f_{OSC3}/64	f_{OSC1}/16
0	1	1	f_{OSC3}/32	f_{OSC1}/8
0	1	0	f_{OSC3}/8	f_{OSC1}/4
0	0	1	f_{OSC3}/2	f_{OSC1}/2
0	0	0	f_{OSC3}/1	f_{OSC1}/1

The set clock is output to Timer x by writing "1" to the clock control register PRPRTx.

When the 16-bit mode is selected, the programmable timer operates with the clock input to Timer(L), and Timer(H) inputs the Timer(L) underflow signal as the clock. Therefore, the setting of Timer(H) input clock is invalid.

5.10.4 Operation and control of timer

Reload data register and setting of initial value

The reload data register (RDRx) is used to set an initial value of the down counter.
In the 8-bit mode, RDRx is used as an 8-bit register separated for each timer.
In the 16-bit mode, the RDR(L) register is handled as low-order 8 bits of reload data, and the RDR(H) register is as high-order 8 bits.

The reload data register can be read and written, and all the registers are set to FFH at initial reset.

Data written in this register is loaded into the down counter, and a down counting starts from the value.
The down counter is preset, in the following two cases:

1) ***When software presets***
   The software preset can be done using the preset control bits PSETx corresponding to Timer x. When the preset control bit is set to "1", the content of the reload data register is loaded into the down counter at that point. In the 16-bit mode, a 16-bit reload data is loaded all at one time by setting PSET(L). In this case, writing to PSET(H) is invalid.

2) ***When down counter has underflowed during a count***
   Since the down counter presets the reload data by the underflow, the underflow period is decided according to the value set in the reload data register. This underflow generates an interrupt, and controls the clock (TOUTx signal) output.

Compare data register

The programmable timer has a built-in data comparator so that count data can be compared with an optional value. The compare data register (CDRx) is used to set the value to be compared.
In the 8-bit mode, CDRx is used as an 8-bit register separated for each timer.
In the 16-bit mode, the CDR(L) register is handled as low-order 8 bits of compare data, and the CDR(H) register is as high-order 8 bits.

The compare data register can be read and written, and all the registers are set to 00H at initial reset.

The programmable timer compares count data with the compare data register (CDRx), and generates a compare match signal when they become the same value. This compare match signal generates an interrupt, and controls the clock (TOUTx signal) output.

Timer operation

Timer is equipped with PTRUNx register which controls the RUN / STOP of the timer. Timer x starts down counting by writing "1" to the PTRUNx register. However, it is necessary to control the input clock and to preset the reload data before starting a count.

When "0" is written to PTRUNx register, clock input is prohibited, and the count stops.
This RUN / STOP control does not affect data in the counter. The data in the counter is maintained during count deactivation, so it is possible to resume counting from the data.

In the 8-bit mode, the timers can be controlled individually by the PTRUNx register.
In the 16-bit mode, the PTRUN(L) register controls a pair of timers as a 16-bit timer. In this case, control of the PTRUN(H) register is invalid.

The buffers PTMx is attached to the counter, and reading is possible in optional timing.

When the counter agrees with the data set in the compare data register during down counting, the timer generates a compare match interrupt.
And, when the counter underflows, an underflow interrupt is generated, and the initial value set in the reload data register is loaded to the counter. The interrupt generated does not stop the down counting.
After an underflow interrupt is generated, the counter continues counting from the initial value reloaded.

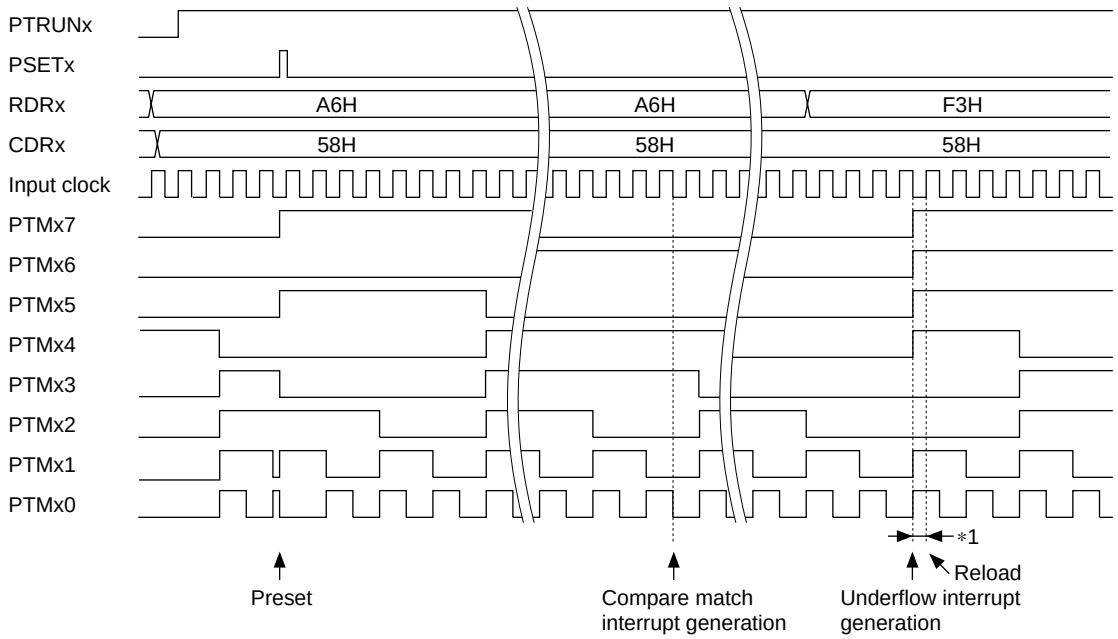


Fig. 5.10.4.1 Basic operation timing of counter (an example of 8-bit mode)

Note: The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ∗1 in the figure).
To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ∗1. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

5.10.5 Interrupt function

The 16-bit programmable timer can generate an interrupt with the compare match signal and underflow signal of each timer.
Figure 5.10.5.1 shows the configuration of the 16-bit programmable timer interrupt circuit.

The compare match signal and underflow signal of each timer set the corresponding interrupt factor flag to "1". At that point, the interrupt is generated. The interrupt can also be prohibited by setting the interrupt enable register to correspond with the interrupt factor flag.
Furthermore, the priority level of the interrupt for the CPU can be set to an optional level (0–3) using the interrupt priority register.
Table 5.10.5.1 shows the interrupt factor flags, interrupt enable registers and interrupt priority registers corresponding to the interrupt factors.

In the 8-bit mode, the compare match interrupt factor flag and underflow interrupt factor flag are individually set to "1" by the timers.

In the 16-bit mode, the interrupt factor flags of Timer(H) are set to "1" by the compare match and underflow in 16 bits.

Refer to Section 5.14, "Interrupt and Standby Status", for details of the interrupt control registers and operations subsequent to interrupt generation.

The exception processing vector addresses for the 16-bit programmable timer interrupt are set as follows:

Timer 0 underflow interrupt:	000016H
Timer 0 compare match interrupt:	000018H
Timer 1 underflow interrupt:	00001AH
Timer 1 compare match interrupt:	00001CH
Timer 2 underflow interrupt:	00001EH
Timer 2 compare match interrupt:	000020H
Timer 3 underflow interrupt:	000022H
Timer 3 compare match interrupt:	000024H
Timer 4 underflow interrupt:	00003CH
Timer 4 compare match interrupt:	00003EH
Timer 5 underflow interrupt:	000040H
Timer 5 compare match interrupt:	000042H
Timer 6 underflow interrupt:	000044H
Timer 6 compare match interrupt:	000046H
Timer 7 underflow interrupt:	000048H
Timer 7 compare match interrupt:	00004AH

Table 5.10.5.1 Interrupt control registers

Interrupt factor		Interrupt factor flag		Interrupt enable register		Interrupt priority register	
		Name	Address·Dx	Name	Address·Dx	Name	Address·Dx
Timer 0	Counter underflow	FTU0	00FF29H·D0	ETU0	00FF25H·D0	PPT0	00FF21H·D2
	Compare match	FTC0	00FF29H·D1	ETC0	00FF25H·D1	PPT1	00FF21H·D3
Timer 1	Counter underflow	FTU1	00FF29H·D2	ETU1	00FF25H·D2		
	Compare match	FTC1	00FF29H·D3	ETC1	00FF25H·D3		
Timer 2	Counter underflow	FTU2	00FF29H·D4	ETU2	00FF25H·D4	PPT2	00FF21H·D4
	Compare match	FTC2	00FF29H·D5	ETC2	00FF25H·D5	PPT3	00FF21H·D5
Timer 3	Counter underflow	FTU3	00FF29H·D6	ETU3	00FF25H·D6		
	Compare match	FTC3	00FF29H·D7	ETC3	00FF25H·D7		
Timer 4	Counter underflow	FTU4	00FF2EH·D0	ETU4	00FF2CH·D0	PPT4	00FF2AH·D0
	Compare match	FTC4	00FF2EH·D1	ETC4	00FF2CH·D1	PPT5	00FF2AH·D1
Timer 5	Counter underflow	FTU5	00FF2EH·D2	ETU5	00FF2CH·D2		
	Compare match	FTC5	00FF2EH·D3	ETC5	00FF2CH·D3		
Timer 6	Counter underflow	FTU6	00FF2EH·D4	ETU6	00FF2CH·D4	PPT6	00FF2AH·D2
	Compare match	FTC6	00FF2EH·D5	ETC6	00FF2CH·D5	PPT7	00FF2AH·D3
Timer 7	Counter underflow	FTU7	00FF2EH·D6	ETU7	00FF2CH·D6		
	Compare match	FTC7	00FF2EH·D7	ETC7	00FF2CH·D7		

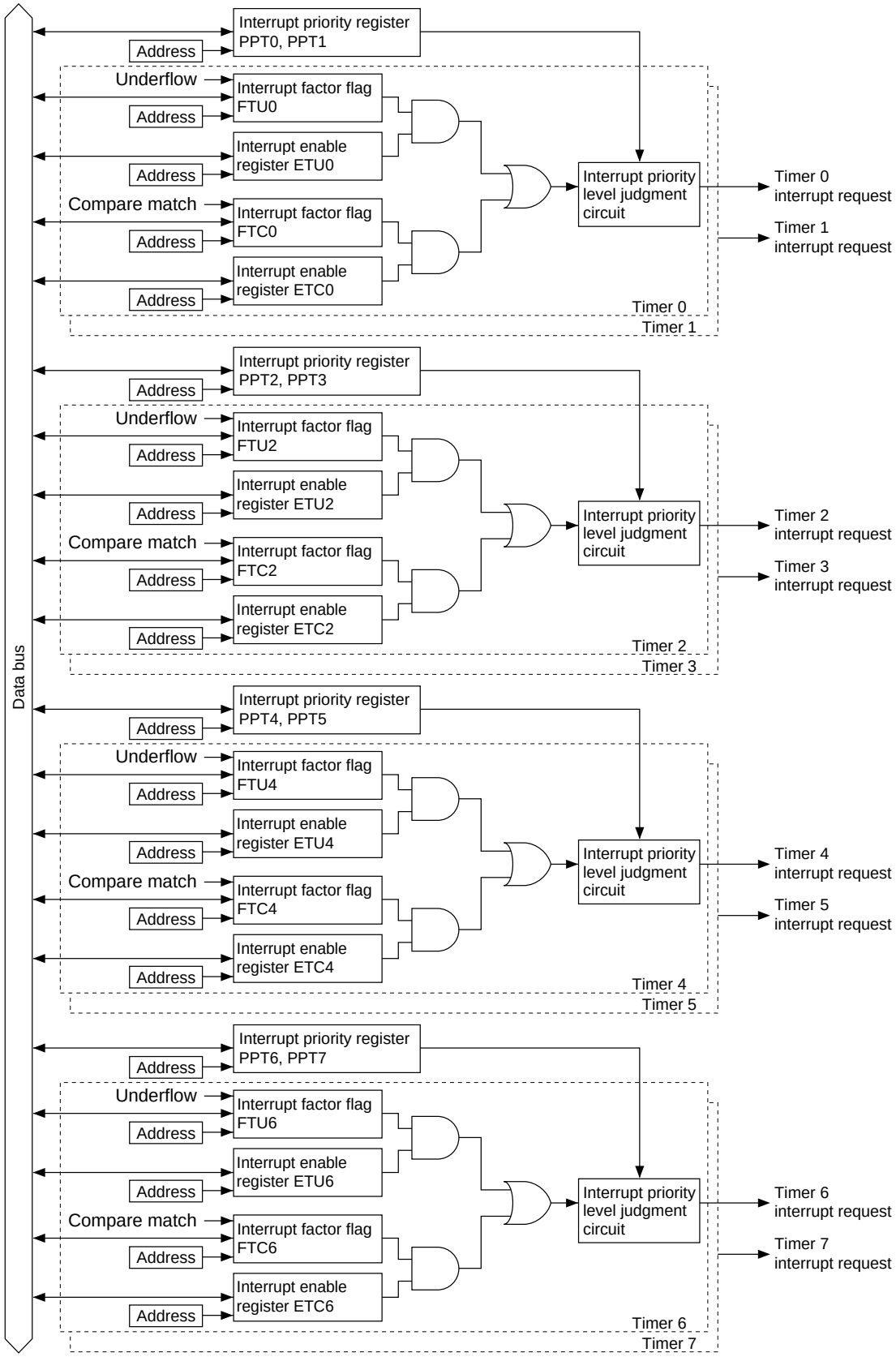


Fig. 5.10.5.1 Configuration of 16-bit programmable timer interrupt circuit

5.10.6 Setting of TOUT output

The 16-bit programmable timer can generate TOUT signals with the underflow and compare match signals of each timer. The TOUT signal generated in the 16-bit programmable timer can be output from the I/O port terminal shown in Table 5.10.6.1 so that a clock is supplied for external devices or it can be used as a PWM waveform output.

Table 5.10.6.1 TOUT output terminal

Timer	Output clock name	Output terminal
Timer 0	TOUT0	P14
Timer 1	TOUT1	P14
Timer 2	TOUT2	P15
	$\overline{\text{TOUT2}}$	P17
Timer 3	TOUT3	P15
	$\overline{\text{TOUT3}}$	P17

The TOUT signal rises at the falling edge of the underflow signal and falls at the falling edge of the compare match signal. $\overline{\text{TOUT}}$ is the inverted TOUT signal. Therefore, it is possible to change the frequency and duty ratio of the TOUT signal by setting the reload data register (RDR) and compare data register (CDR).

However, it needs a condition setting: RDR > CDR, CDR ≠ 0. In the case of RDR ≤ CDR, TOUT signal is fixed at "1".

The TOUT output can be controlled ON and OFF using the clock output control register PTOUTx of each timer and the $\overline{\text{TOUT}}$ output can be controlled using the inverted clock output control register RPTOUTx of Timer 2 or Timer 3.
When PTOUTx (RPTOUTx) is set to "1", the TOUTx ($\overline{\text{TOUTx}}$) signal is output from the corresponding port terminal, when "0" is set, the port is set for DC output. When PTOUTx (RPTOUTx) is "1", settings of the I/O control register IOC14/IOC15/IOC17 and data register P14D/P15D/P17D become invalid.

Note: If PTOUT0 and PTOUT1 are set to "1" at the same time, PTOUT1 is effective. Similarly, if PTOUT2 (RPTOUT2) and PTOUT3 (RPTOUT3) are set to "1", PTOUT3 (RPTOUT3) is effective.

In the 16-bit mode, the output is controlled by the control register PTOUT(H) for Timer(H). The clock is output from Timer(H).

Since the TOUTx ($\overline{\text{TOUTx}}$) signal is generated asynchronously from the register PTOUTx (RPTOUTx), when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 5.10.6.1 shows the output waveform of TOUT signal.

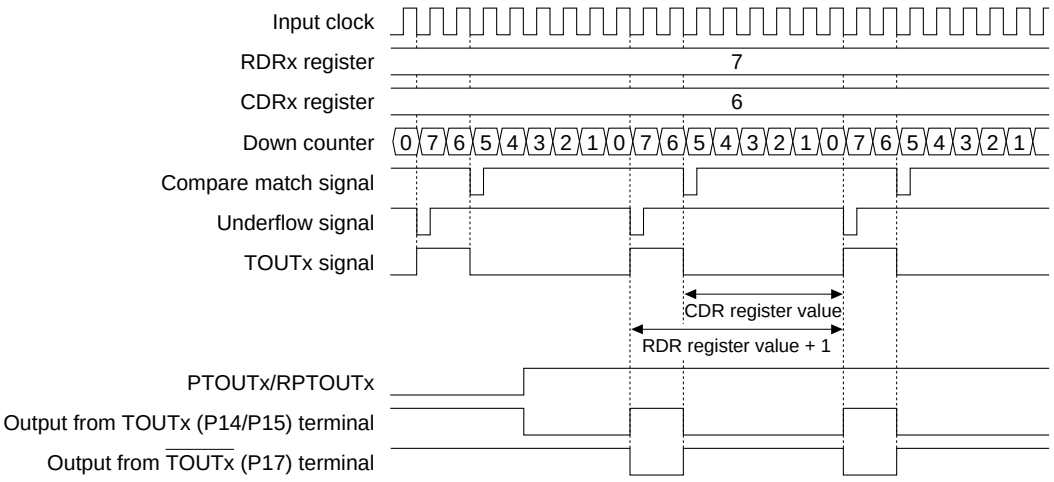


Fig. 5.10.6.1 Output waveform of TOUT signal

5.10.7 Transfer rate setting of serial interface

The underflow signal of Timer 1/Timer 7 can be used to clock the serial interface Ch.0/Ch.1.
The transfer rate setting in this case is made in the registers PST1x/PST7x and RDR1x/RDR7x (since only the underflow signal is used as the serial interface clock source, the CDR1x/CDR7x register value does not affect the transfer rates. It can be set to any value).

Since the underflow signal of the timer is divided by 32 in the serial interface, the value set in the register RDR1x/RDR7x which corresponds to the transfer rate is shown in the following expression:

$$RDR = \frac{fdiv}{32 \times bps} - 1$$

fdiv: Input clock frequency (setting of PST1x/PST7x)
bps: Transfer rate

Table 5.10.7.1 Example of transfer rate setting

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings					
	f_{OSC3} = 2.4576 MHz		f_{OSC3} = 3.0720 MHz		f_{OSC3} = 3.6864 MHz	
	PST1x/7x	RDR1x/7x	PST1x/7x	RDR1x/7x	PST1x/7x	RDR1x/7x
19,200	00H	03H	00H	04H	00H	05H
9,600	00H	07H	00H	09H	00H	0BH
4,800	00H	0FH	00H	13H	00H	17H
2,400	00H	1FH	00H	27H	00H	2FH
1,200	00H	3FH	00H	4FH	00H	5FH
600	00H	7FH	00H	9FH	00H	BFH
300	02H	1FH	03H	09H	01H	BFH
150	02H	3FH	03H	13H	02H	5FH

* Since the underflow signal only is used as the clock source, the CDR1x/CDR7x register value does not affect the transfer rates.

5.10.8 Setting frame frequency for LCD driver

The underflow signal of Timer 5 can be used as the source clock to generate the frame signal for the LCD driver.
The frame frequency is set up using the registers PST5x and RDR5x (since only the underflow signal is used as the source clock, the CDR5x register value does not affect the frame signal. It can be set to any value).
The Timer 5 underflow signal is divided by 128 (for 1/16 or 1/3 duty) or 256 (for 1/8 duty) in the LCD driver, so set a value represented by the following expressions to the register RDR5x.

(for 1/16 or 1/32 duty)

$$RDR5x = \frac{fdiv}{128 \times f_{FRM}} - 1$$

(for 1/8 duty)

$$RDR5x = \frac{fdiv}{256 \times f_{FRM}} - 1$$

fdiv: Input clock frequency (setting of PST5x)
f_{FRM}: Frame frequency (Hz)

5.10.9 Control of programmable timer

Table 5.10.9.1 shows the programmable timer control bits.

Table 5.10.9.1(a) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF14	D7	PRPRT1	Programmable timer 1 clock control	On	Off	0	R/W	
	D6	PST12	Programmable timer 1 division ratio			0	R/W	
	D5	PST11				0	R/W	
	D4	PST10				0	R/W	
	D3	PRPRT0	Programmable timer 0 clock control	On	Off	0	R/W	
	D2	PST02	Programmable timer 0 division ratio			0	R/W	
	D1	PST01				0	R/W	
	D0	PST00				0	R/W	
00FF15	D7	PRPRT3	Programmable timer 3 clock control	On	Off	0	R/W	
	D6	PST32	Programmable timer 3 division ratio			0	R/W	
	D5	PST31				0	R/W	
	D4	PST30				0	R/W	
	D3	PRPRT2	Programmable timer 2 clock control	On	Off	0	R/W	
	D2	PST22	Programmable timer 2 division ratio			0	R/W	
	D1	PST21				0	R/W	
	D0	PST20				0	R/W	
00FF18	D7	PRPRT5	Programmable timer 5 clock control	On	Off	0	R/W	
	D6	PST52	Programmable timer 5 division ratio			0	R/W	
	D5	PST51				0	R/W	
	D4	PST50				0	R/W	
	D3	PRPRT4	Programmable timer 4 clock control	On	Off	0	R/W	
	D2	PST42	Programmable timer 4 division ratio			0	R/W	
	D1	PST41				0	R/W	
	D0	PST40				0	R/W	

Programmable timer 1 division ratio

PST12	PST11	PST10	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Programmable timer 0 division ratio

PST02	PST01	PST00	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Programmable timer 3 division ratio

PST32	PST31	PST30	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Programmable timer 2 division ratio

PST22	PST21	PST20	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Programmable timer 5 division ratio

PST52	PST51	PST50	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Programmable timer 4 division ratio

PST42	PST41	PST40	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Table 5.10.9.1(b) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF19	D7	PRPRT7	Programmable timer 7 clock control	On	Off	0	R/W	
	D6	PST72	Programmable timer 7 division ratio PST72 PST71 PST70 (OSC3) (OSC1) 1 1 1 fosc3 / 4096 fosc1 / 128 1 1 0 fosc3 / 1024 fosc1 / 64 1 0 1 fosc3 / 256 fosc1 / 32 1 0 0 fosc3 / 64 fosc1 / 16 0 1 1 fosc3 / 32 fosc1 / 8 0 1 0 fosc3 / 8 fosc1 / 4 0 0 1 fosc3 / 2 fosc1 / 2 0 0 0 fosc3 / 1 fosc1 / 1			0	R/W	
	D5	PST71				0	R/W	
	D4	PST70				0	R/W	
	D3	PRPRT6	Programmable timer 6 clock control	On	Off	0	R/W	
	D2	PST62	Programmable timer 6 division ratio PST62 PST61 PST60 (OSC3) (OSC1) 1 1 1 fosc3 / 4096 fosc1 / 128 1 1 0 fosc3 / 1024 fosc1 / 64 1 0 1 fosc3 / 256 fosc1 / 32 1 0 0 fosc3 / 64 fosc1 / 16 0 1 1 fosc3 / 32 fosc1 / 8 0 1 0 fosc3 / 8 fosc1 / 4 0 0 1 fosc3 / 2 fosc1 / 2 0 0 0 fosc3 / 1 fosc1 / 1			0	R/W	
	D1	PST61				0	R/W	
	D0	PST60				0	R/W	
00FF17	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PRTF3	Programmable timer 3 source clock selection	fosc1	fosc3	0	R/W	
	D2	PRTF2	Programmable timer 2 source clock selection	fosc1	fosc3	0	R/W	
	D1	PRTF1	Programmable timer 1 source clock selection	fosc1	fosc3	0	R/W	
	D0	PRTF0	Programmable timer 0 source clock selection	fosc1	fosc3	0	R/W	
00FF1B	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PRTF7	Programmable timer 7 source clock selection	fosc1	fosc3	0	R/W	
	D2	PRTF6	Programmable timer 6 source clock selection	fosc1	fosc3	0	R/W	
	D1	PRTF5	Programmable timer 5 source clock selection	fosc1	fosc3	0	R/W	
	D0	PRTF4	Programmable timer 4 source clock selection	fosc1	fosc3	0	R/W	
00FF21	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	PPT3	Programmable timer 3–2 interrupt priority register PPT3 PPT2 PPT1 PPT0 Priority level PSIF11 PSIF10 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0			0	R/W	
	D4	PPT2						
	D3	PPT1	Programmable timer 1–0 interrupt priority register			0	R/W	
	D2	PPT0						
	D1	PSIF11	Serial interface 1 interrupt priority register			0	R/W	
	D0	PSIF10						
00FF2A	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT7	Programmable timer 7–6 interrupt priority register PPT7 PPT6 PPT5 PPT4 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0			0	R/W	
	D2	PPT6						
	D1	PPT5	Programmable timer 5–4 interrupt priority register			0	R/W	
	D0	PPT4						

Table 5.10.9.1(c) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF25	D7	ETC3	PTM3 compare match interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	ETU3	PTM3 underflow interrupt enable					
	D5	ETC2	PTM2 compare match interrupt enable					
	D4	ETU2	PTM2 underflow interrupt enable					
	D3	ETC1	PTM1 compare match interrupt enable					
	D2	ETU1	PTM1 underflow interrupt enable					
	D1	ETC0	PTM0 compare match interrupt enable					
	D0	ETU0	PTM0 underflow interrupt enable					
00FF29	D7	FTC3	PTM3 compare match interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D6	FTU3	PTM3 underflow interrupt factor flag					
	D5	FTC2	PTM2 compare match interrupt factor flag					
	D4	FTU2	PTM2 underflow interrupt factor flag					
	D3	FTC1	PTM1 compare match interrupt factor flag					
	D2	FTU1	PTM1 underflow interrupt factor flag					
	D1	FTC0	PTM0 compare match interrupt factor flag					
	D0	FTU0	PTM0 underflow interrupt factor flag					
00FF2C	D7	ETC7	PTM7 compare match interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	ETU7	PTM7 underflow interrupt enable					
	D5	ETC6	PTM6 compare match interrupt enable					
	D4	ETU6	PTM6 underflow interrupt enable					
	D3	ETC5	PTM5 compare match interrupt enable					
	D2	ETU5	PTM5 underflow interrupt enable					
	D1	ETC4	PTM4 compare match interrupt enable					
	D0	ETU4	PTM4 underflow interrupt enable					
00FF2E	D7	FTC7	PTM7 compare match interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D6	FTU7	PTM7 underflow interrupt factor flag					
	D5	FTC6	PTM6 compare match interrupt factor flag					
	D4	FTU6	PTM6 underflow interrupt factor flag					
	D3	FTC5	PTM5 compare match interrupt factor flag					
	D2	FTU5	PTM5 underflow interrupt factor flag					
	D1	FTC4	PTM4 compare match interrupt factor flag					
	D0	FTU4	PTM4 underflow interrupt factor flag					
00FF30	D7	MODE16_A	PTM0–1 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_A	External clock 0 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT0	PTM0 clock output control	On	Off	0	R/W	
	D2	PTRUN0	PTM0 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET0	PTM0 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL0	PTM0 input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT1	PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	PTM1 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET1	PTM1 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL1	PTM1 input clock selection	External clock	Internal clock	0	R/W	

Table 5.10.9.1(d) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF32	D7	RDR07	PTM0 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR06	PTM0 reload data D6					
	D5	RDR05	PTM0 reload data D5					
	D4	RDR04	PTM0 reload data D4					
	D3	RDR03	PTM0 reload data D3					
	D2	RDR02	PTM0 reload data D2					
	D1	RDR01	PTM0 reload data D1					
	D0	RDR00	PTM0 reload data D0 (LSB)					
00FF33	D7	RDR17	PTM1 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR16	PTM1 reload data D6					
	D5	RDR15	PTM1 reload data D5					
	D4	RDR14	PTM1 reload data D4					
	D3	RDR13	PTM1 reload data D3					
	D2	RDR12	PTM1 reload data D2					
	D1	RDR11	PTM1 reload data D1					
	D0	RDR10	PTM1 reload data D0 (LSB)					
00FF34	D7	CDR07	PTM0 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR06	PTM0 compare data D6					
	D5	CDR05	PTM0 compare data D5					
	D4	CDR04	PTM0 compare data D4					
	D3	CDR03	PTM0 compare data D3					
	D2	CDR02	PTM0 compare data D2					
	D1	CDR01	PTM0 compare data D1					
	D0	CDR00	PTM0 compare data D0 (LSB)					
00FF35	D7	CDR17	PTM1 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR16	PTM1 compare data D6					
	D5	CDR15	PTM1 compare data D5					
	D4	CDR14	PTM1 compare data D4					
	D3	CDR13	PTM1 compare data D3					
	D2	CDR12	PTM1 compare data D2					
	D1	CDR11	PTM1 compare data D1					
	D0	CDR10	PTM1 compare data D0 (LSB)					
00FF36	D7	PTM07	PTM0 data D7 (MSB)	High	Low	1	R	
	D6	PTM06	PTM0 data D6					
	D5	PTM05	PTM0 data D5					
	D4	PTM04	PTM0 data D4					
	D3	PTM03	PTM0 data D3					
	D2	PTM02	PTM0 data D2					
	D1	PTM01	PTM0 data D1					
	D0	PTM00	PTM0 data D0 (LSB)					
00FF37	D7	PTM17	PTM1 data D7 (MSB)	High	Low	1	R	
	D6	PTM16	PTM1 data D6					
	D5	PTM15	PTM1 data D5					
	D4	PTM14	PTM1 data D4					
	D3	PTM13	PTM1 data D3					
	D2	PTM12	PTM1 data D2					
	D1	PTM11	PTM1 data D1					
	D0	PTM10	PTM1 data D0 (LSB)					

Table 5.10.9.1(e) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF38	D7	MODE16_B	PTM2–3 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_B	External clock 1 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	RPTOUT2	PTM2 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT2	PTM2 clock output control	On	Off	0	R/W	
	D2	PTRUN2	PTM2 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET2	PTM2 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL2	PTM2 input clock selection	External clock	Internal clock	0	R/W	
00FF39	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	RPTOUT3	PTM3 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT3	PTM3 clock output control	On	Off	0	R/W	
	D2	PTRUN3	PTM3 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET3	PTM3 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL3	PTM3 input clock selection	External clock	Internal clock	0	R/W	
00FF3A	D7	RDR27	PTM2 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR26	PTM2 reload data D6					
	D5	RDR25	PTM2 reload data D5					
	D4	RDR24	PTM2 reload data D4					
	D3	RDR23	PTM2 reload data D3					
	D2	RDR22	PTM2 reload data D2					
	D1	RDR21	PTM2 reload data D1					
	D0	RDR20	PTM2 reload data D0 (LSB)					
00FF3B	D7	RDR37	PTM3 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR36	PTM3 reload data D6					
	D5	RDR35	PTM3 reload data D5					
	D4	RDR34	PTM3 reload data D4					
	D3	RDR33	PTM3 reload data D3					
	D2	RDR32	PTM3 reload data D2					
	D1	RDR31	PTM3 reload data D1					
	D0	RDR30	PTM3 reload data D0 (LSB)					
00FF3C	D7	CDR27	PTM2 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR26	PTM2 compare data D6					
	D5	CDR25	PTM2 compare data D5					
	D4	CDR24	PTM2 compare data D4					
	D3	CDR23	PTM2 compare data D3					
	D2	CDR22	PTM2 compare data D2					
	D1	CDR21	PTM2 compare data D1					
	D0	CDR20	PTM2 compare data D0 (LSB)					
00FF3D	D7	CDR37	PTM3 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR36	PTM3 compare data D6					
	D5	CDR35	PTM3 compare data D5					
	D4	CDR34	PTM3 compare data D4					
	D3	CDR33	PTM3 compare data D3					
	D2	CDR32	PTM3 compare data D2					
	D1	CDR31	PTM3 compare data D1					
	D0	CDR30	PTM3 compare data D0 (LSB)					

Table 5.10.9.1(f) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF3E	D7	PTM27	PTM2 data D7 (MSB)	High	Low	1	R	
	D6	PTM26	PTM2 data D6					
	D5	PTM25	PTM2 data D5					
	D4	PTM24	PTM2 data D4					
	D3	PTM23	PTM2 data D3					
	D2	PTM22	PTM2 data D2					
	D1	PTM21	PTM2 data D1					
	D0	PTM20	PTM2 data D0 (LSB)					
00FF3F	D7	PTM37	PTM3 data D7 (MSB)	High	Low	1	R	
	D6	PTM36	PTM3 data D6					
	D5	PTM35	PTM3 data D5					
	D4	PTM34	PTM3 data D4					
	D3	PTM33	PTM3 data D3					
	D2	PTM32	PTM3 data D2					
	D1	PTM31	PTM3 data D1					
	D0	PTM30	PTM3 data D0 (LSB)					
00FFB0	D7	MODE16_C	PTM4–5 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_C	External clock 2 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN4	PTM4 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET4	PTM4 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL4	PTM4 input clock selection	External clock	Internal clock	0	R/W	
00FFB1	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN5	PTM5 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET5	PTM5 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL5	PTM5 input clock selection	External clock	Internal clock	0	R/W	
00FFB2	D7	RDR47	PTM4 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR46	PTM4 reload data D6					
	D5	RDR45	PTM4 reload data D5					
	D4	RDR44	PTM4 reload data D4					
	D3	RDR43	PTM4 reload data D3					
	D2	RDR42	PTM4 reload data D2					
	D1	RDR41	PTM4 reload data D1					
	D0	RDR40	PTM4 reload data D0 (LSB)					
00FFB3	D7	RDR57	PTM5 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR56	PTM5 reload data D6					
	D5	RDR55	PTM5 reload data D5					
	D4	RDR54	PTM5 reload data D4					
	D3	RDR53	PTM5 reload data D3					
	D2	RDR52	PTM5 reload data D2					
	D1	RDR51	PTM5 reload data D1					
	D0	RDR50	PTM5 reload data D0 (LSB)					

Table 5.10.9.1(g) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FFB4	D7	CDR47	PTM4 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR46	PTM4 compare data D6					
	D5	CDR45	PTM4 compare data D5					
	D4	CDR44	PTM4 compare data D4					
	D3	CDR43	PTM4 compare data D3					
	D2	CDR42	PTM4 compare data D2					
	D1	CDR41	PTM4 compare data D1					
	D0	CDR40	PTM4 compare data D0 (LSB)					
00FFB5	D7	CDR57	PTM5 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR56	PTM5 compare data D6					
	D5	CDR55	PTM5 compare data D5					
	D4	CDR54	PTM5 compare data D4					
	D3	CDR53	PTM5 compare data D3					
	D2	CDR52	PTM5 compare data D2					
	D1	CDR51	PTM5 compare data D1					
	D0	CDR50	PTM5 compare data D0 (LSB)					
00FFB6	D7	PTM47	PTM4 data D7 (MSB)	High	Low	1	R	
	D6	PTM46	PTM4 data D6					
	D5	PTM45	PTM4 data D5					
	D4	PTM44	PTM4 data D4					
	D3	PTM43	PTM4 data D3					
	D2	PTM42	PTM4 data D2					
	D1	PTM41	PTM4 data D1					
	D0	PTM40	PTM4 data D0 (LSB)					
00FFB7	D7	PTM57	PTM5 data D7 (MSB)	High	Low	1	R	
	D6	PTM56	PTM5 data D6					
	D5	PTM55	PTM5 data D5					
	D4	PTM54	PTM5 data D4					
	D3	PTM53	PTM5 data D3					
	D2	PTM52	PTM5 data D2					
	D1	PTM51	PTM5 data D1					
	D0	PTM50	PTM5 data D0 (LSB)					
00FFB8	D7	MODE16_D	PTM6–7 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_D	External clock 3 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	–		"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN6	PTM6 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET6	PTM6 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL6	PTM6 input clock selection	External clock	Internal clock	0	R/W	
00FFB9	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN7	PTM7 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET7	PTM7 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL7	PTM7 input clock selection	External clock	Internal clock	0	R/W	

Table 5.10.9.1(h) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FFBA	D7	RDR67	PTM6 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR66	PTM6 reload data D6					
	D5	RDR65	PTM6 reload data D5					
	D4	RDR64	PTM6 reload data D4					
	D3	RDR63	PTM6 reload data D3					
	D2	RDR62	PTM6 reload data D2					
	D1	RDR61	PTM6 reload data D1					
	D0	RDR60	PTM6 reload data D0 (LSB)					
00FFBB	D7	RDR77	PTM7 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR76	PTM7 reload data D6					
	D5	RDR75	PTM7 reload data D5					
	D4	RDR74	PTM7 reload data D4					
	D3	RDR73	PTM7 reload data D3					
	D2	RDR72	PTM7 reload data D2					
	D1	RDR71	PTM7 reload data D1					
	D0	RDR70	PTM7 reload data D0 (LSB)					
00FFBC	D7	CDR67	PTM6 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR66	PTM6 compare data D6					
	D5	CDR65	PTM6 compare data D5					
	D4	CDR64	PTM6 compare data D4					
	D3	CDR63	PTM6 compare data D3					
	D2	CDR62	PTM6 compare data D2					
	D1	CDR61	PTM6 compare data D1					
	D0	CDR60	PTM6 compare data D0 (LSB)					
00FFBD	D7	CDR77	PTM7 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR76	PTM7 compare data D6					
	D5	CDR75	PTM7 compare data D5					
	D4	CDR74	PTM7 compare data D4					
	D3	CDR73	PTM7 compare data D3					
	D2	CDR72	PTM7 compare data D2					
	D1	CDR71	PTM7 compare data D1					
	D0	CDR70	PTM7 compare data D0 (LSB)					
00FFBE	D7	PTM67	PTM6 data D7 (MSB)	High	Low	1	R	
	D6	PTM66	PTM6 data D6					
	D5	PTM65	PTM6 data D5					
	D4	PTM64	PTM6 data D4					
	D3	PTM63	PTM6 data D3					
	D2	PTM62	PTM6 data D2					
	D1	PTM61	PTM6 data D1					
	D0	PTM60	PTM6 data D0 (LSB)					
00FFBF	D7	PTM77	PTM7 data D7 (MSB)	High	Low	1	R	
	D6	PTM76	PTM7 data D6					
	D5	PTM75	PTM7 data D5					
	D4	PTM74	PTM7 data D4					
	D3	PTM73	PTM7 data D3					
	D2	PTM72	PTM7 data D2					
	D1	PTM71	PTM7 data D1					
	D0	PTM70	PTM7 data D0 (LSB)					

MODE16_A: 00FF30H•D7
MODE16_B: 00FF38H•D7
MODE16_C: 00FFB0H•D7
MODE16_D: 00FFB8H•D7

Selects either the 8/16 bit mode.

When "1" is written: 16 bits × 1 channel
When "0" is written: 8 bits × 2 channels
Reading: Valid

MODE16_A, MODE16_B, MODE16_C and MODE16_D are the 8/16-bit mode selection registers corresponding to Timers 0 and 1, Timers 2 and 3, Timers 4 and 5, and Timers 6 and 7, respectively. Select whether Timer(L) and Timer(H) are used as 2 channels independent 8-bit timers or as 1 channel combined 16-bit timer.
When "0" is written to the MODE16_A (–D) register, 8-bit × 2 channels is selected and when "1" is written, 16-bit × 1 channel is selected.
At initial reset, this register is set to "0" (8-bit × 2 channels).

PTNREN_A: 00FF30H•D6
PTNREN_B: 00FF38H•D6
PTNREN_C: 00FFB0H•D6
PTNREN_D: 00FFB8H•D6

Enables/disables the noise rejector in the external clock input circuit.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

Writing "1" to PTNREN_A (–D) enables the noise rejector for the external clock EXCL0 (–3). The noise rejector regards pulses less than a 16/f_{OSC1} seconds in width as noise and rejects them.
When PTNREN_A (–D) is "0", the external clock bypasses the noise rejector.
At initial reset, this register is set to "0" (disabled).

CKSEL0: 00FF30H•D0
CKSEL1: 00FF31H•D0
CKSEL2: 00FF38H•D0
CKSEL3: 00FF39H•D0
CKSEL4: 00FFB0H•D0
CKSEL5: 00FFB1H•D0
CKSEL6: 00FFB8H•D0
CKSEL7: 00FFB9H•D0

Selects the input clock for each timer.

When "1" is written: External clock
When "0" is written: Internal clock
Reading: Valid

The clock to be input to each timer is selected from either the external clock (input signal of input port) or the internal clock (prescaler output clock).
When "0" is written to the CKSELx register, the internal clock (prescaler output INCLx) is selected as the input clock for Timer x.
When "1" is written, the external clock (EXCL0 (K04 input) for Timers 0 and 1, EXCL1 (K05 input) for Timers 2 and 3, EXCL2 (K06 input) for Timers 4 and 5, EXCL3 (K07 input) for Timers 6 and 7) is selected and the timer functions as an event counter.
In the 16-bit mode, the setting of the CKSEL(H) register is invalid.
At initial reset, this register is set to "0" (internal clock).

PRTF0: 00FF17H•D0
PRTF1: 00FF17H•D1
PRTF2: 00FF17H•D2
PRTF3: 00FF17H•D3
PRTF4: 00FF1BH•D0
PRTF5: 00FF1BH•D1
PRTF6: 00FF1BH•D2
PRTF7: 00FF1BH•D3

Selects the source clock for each timer (when internal clock is used).

When "1" is written: f_{OSC1}
When "0" is written: f_{OSC3}
Reading: Valid

When "1" is written to the PRTFx register, the OSC1 clock is selected as the source clock for Timer x.
When "0" is written, the OSC3 clock is selected.
At initial reset, this register is set to "0" (f_{OSC3}).

PST00–PST02: 00FF14H•D0–D2
PST10–PST12: 00FF14H•D4–D6
PST20–PST22: 00FF15H•D0–D2
PST30–PST32: 00FF15H•D4–D6
PST40–PST42: 00FF18H•D0–D2
PST50–PST52: 00FF18H•D4–D6
PST60–PST62: 00FF19H•D0–D2
PST70–PST72: 00FF19H•D4–D6

Selects the input clock for each timer (when internal clock is used).
It can be selected from 8 types of division ratio shown in Tables 5.10.9.1(a) and (b).
This register can also be read.
At initial reset, this register is set to "0".

PRPRT0: 00FF14H•D3
PRPRT1: 00FF14H•D7
PRPRT2: 00FF15H•D3
PRPRT3: 00FF15H•D7
PRPRT4: 00FF18H•D3
PRPRT5: 00FF18H•D7
PRPRT6: 00FF19H•D3
PRPRT7: 00FF19H•D7

Controls the clock supply of each timer (when internal clock is used).

When "1" is written:	ON
When "0" is written:	OFF
Reading:	Valid

By writing "1" to the PRPRTx register, the clock that is selected with the PSTx register is output to Timer x.
When "0" is written, the clock is not output.
At initial reset, the this register is set to "0" (OFF).

RDR00–RDR07: 00FF32H
RDR10–RDR17: 00FF33H
RDR20–RDR27: 00FF3AH
RDR30–RDR37: 00FF3BH
RDR40–RDR47: 00FFB2H
RDR50–RDR57: 00FFB3H
RDR60–RDR67: 00FFBAH
RDR70–RDR77: 00FFBBH

Sets the initial value for the counter of each timer.
Each counter loads the reload data set in this register and counts using it as the initial value.
The reload data set in this register is loaded into the counter when "1" is written to PSETx, or when a counter underflow occurs.
This register can also be read.
At initial reset, this register is set to "FFH".

CDR00–CDR07: 00FF34H
CDR10–CDR17: 00FF35H
CDR20–CDR27: 00FF3CH
CDR30–CDR37: 00FF3DH
CDR40–CDR47: 00FFB4H
CDR50–CDR57: 00FFB5H
CDR60–CDR67: 00FFBCH
CDR70–CDR77: 00FFBDH

Sets the compare data for each timer.
The timer compares the data set in this register with the corresponding counter data, and outputs the compare match signals when they are the same. The compare match signal controls the interrupt and the TOUT output waveform.
This register can also be read.
At initial reset, this register is set to "00H".

PTM00–PTM07: 00FF36H
PTM10–PTM17: 00FF37H
PTM20–PTM27: 00FF3EH
PTM30–PTM37: 00FF3FH
PTM40–PTM47: 00FFB6H
PTM50–PTM57: 00FFB7H
PTM60–PTM67: 00FFBEH
PTM70–PTM77: 00FFBFH

The counter data of each timer can be read.
Data can be read at any given time. However, in the 16-bit mode, reading PTM(L) does not latch the Timer(H) counter data in PTM(H). To avoid generating a borrow from Timer(L) to Timer(H), read the counter data after stopping the timer by writing "0" to PTRUN(L).
PTMx can only be read, so writing operation is invalid.
At initial reset, PTMx is set to "FFH".

PSET0: 00FF30H•D1
PSET1: 00FF31H•D1
PSET2: 00FF38H•D1
PSET3: 00FF39H•D1
PSET4: 00FFB0H•D1
PSET5: 00FFB1H•D1
PSET6: 00FFB8H•D1
PSET7: 00FFB9H•D1

Presets the reload data to the counter.

When "1" is written:	Preset
When "0" is written:	Invalid
Reading:	Always "0"

Writing "1" to PSETx presets the reload data in the RDRx register to the counter of Timer x. When the counter of Timer x is in RUN status, the counter restarts immediately after presetting.
In the case of STOP status, the counter maintains the preset data.
No operation results when "0" is written.
In the 16-bit mode, writing "1" to PSET(H) is invalid because 16-bit data is preset by PSET(L) only.
PSETx is only for writing, and it is always "0" during reading.

PTRUN0: 00FF30H•D2
PTRUN1: 00FF31H•D2
PTRUN2: 00FF38H•D2
PTRUN3: 00FF39H•D2
PTRUN4: 00FFB0H•D2
PTRUN5: 00FFB1H•D2
PTRUN6: 00FFB8H•D2
PTRUN7: 00FFB9H•D2

Controls the RUN / STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter of Timer x starts down-counting by writing "1" to the PTRUNx register and stops by writing "0".
In STOP status, the counter data is maintained until it is preset or the counter restarts. When STOP status changes to RUN status, the counter resumes counting from the data maintained.
In the 16-bit mode, the timers are controlled with the PTRUN(L) register, and the PTRUN(H) register is fixed at "0".
At initial reset, this register is set to "0" (STOP).

PTOUT0: 00FF30H•D3
PTOUT1: 00FF31H•D3
PTOUT2: 00FF38H•D3
PTOUT3: 00FF39H•D3

Controls the output of the TOUT signal.

When "1" is written: TOUT signal output
When "0" is written: DC output
Reading: Valid

The PTOUTx is the output control register for the TOUTx signal (Timer x output clock). When PTOUT0 or PTOUT1 is set to "1", the TOUT0 or TOUT1 signal is output from the P14 port terminal. When PTOUT2 or PTOUT3 is set to "1", the TOUT2 or TOUT3 signal is output from the P15 port terminal. When "0" is set, P14 / P15 is set for DC output.
At this time, settings of the I / O control register IOC14 / IOC15 and data register P14D / P15D become invalid.
In the 16-bit mode, the timers are controlled with the PTOUT(H) register, and the PTOUT(L) register is fixed at "0".
At initial reset, this register is set to "0" (DC output).

Note: If PTOUT0 and PTOUT1 are set to "1" at the same time, PTOUT1 is effective. Similarly, if PTOUT2 and PTOUT3 are set to "1", PTOUT3 is effective. Furthermore, if the programmable timer is set in 16-bit mode, the TOUT0 and TOUT2 signals cannot be output.

RPTOUT2: 00FF38H•D4
RPTOUT3: 00FF39H•D4

Controls the output of the $\overline{\text{TOUT}}$ signal.

When "1" is written: $\overline{\text{TOUT}}$ signal output
When "0" is written: DC output
Reading: Valid

The RPTOUTx is the output control register for the $\overline{\text{TOUTx}}$ signal (Timer x inverted output clock). When RPTOUT2 or RPTOUT3 is set to "1", the $\overline{\text{TOUT2}}$ or $\overline{\text{TOUT3}}$ signal is output from the P17 port terminal. When "0" is set, P17 is set for DC output.
At this time, settings of the I / O control register IOC17 and data register P17D become invalid.
In the 16-bit mode, the timers are controlled with the RPTOUT3 register, and the RPTOUT2 register is fixed at "0".
At initial reset, this register is set to "0" (DC output).

Note: If RPTOUT2 and RPTOUT3 are set to "1" at the same time, RPTOUT3 is effective.

PPT0, PPT1: 00FF21H•D2, D3
PPT2, PPT3: 00FF21H•D4, D5
PPT4, PPT5: 00FF2AH•D0, D1
PPT6, PPT7: 00FF2AH•D2, D3

Sets the priority level of the programmable timer interrupt.
PPT0–PPT1, PPT2–PPT3, PPT4–PPT5, and PPT6–PPT7 are the interrupt priority register corresponding to Timers 0–1, Timers 2–3, Timers 4–5, and Timers 6–7, respectively.
Table 5.10.9.2 shows the interrupt priority level which can be set by this register.

Table 5.10.9.2 Interrupt priority level settings

PPT7 PPT5 PPT3 PPT1	PPT6 PPT4 PPT2 PPT0	Interrupt priority level
1	1	Level 3 ($\overline{\text{IRQ3}}$)
1	0	Level 2 ($\overline{\text{IRQ2}}$)
0	1	Level 1 ($\overline{\text{IRQ1}}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ETU0: 00FF25H•D0
ETU1: 00FF25H•D2
ETU2: 00FF25H•D4
ETU3: 00FF25H•D6
ETU4: 00FF2CH•D0
ETU5: 00FF2CH•D2
ETU6: 00FF2CH•D4
ETU7: 00FF2CH•D6

Enables or disables the underflow interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The ETUx register is the interrupt enable register corresponding to the underflow interrupt factor of Timer x.
Interrupt in which the ETUx register is set to "1" is enabled, and the others in which the ETUx register is set to "0" are disabled.
In the 16-bit mode, the setting of the ETU(L) is invalid.
At initial reset, this register is set to "0" (interrupt is disabled).

ETC0: 00FF25H•D1
ETC1: 00FF25H•D3
ETC2: 00FF25H•D5
ETC3: 00FF25H•D7
ETC4: 00FF2CH•D1
ETC5: 00FF2CH•D3
ETC6: 00FF2CH•D5
ETC7: 00FF2CH•D7

Enables or disables the compare match interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The ETCx register is the interrupt enable register corresponding to the compare match interrupt factor of Timer x.
Interrupt in which the ETCx register is set to "1" is enabled, and the others in which the ETCx register is set to "0" are disabled.
In the 16-bit mode, the setting of the ETC(L) is invalid.
At initial reset, this register is set to "0" (interrupt is disabled).

FTU0: 00FF29H•D0
FTU1: 00FF29H•D2
FTU2: 00FF29H•D4
FTU3: 00FF29H•D6
FTU4: 00FF2EH•D0
FTU5: 00FF2EH•D2
FTU6: 00FF2EH•D4
FTU7: 00FF2EH•D6

Indicates the generation of underflow interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

FTUx is the interrupt factor flag corresponding to interrupt of Timer x, and is set to "1" due to the counter underflow.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
In the 16-bit mode, the interrupt factor flag FTU(L) is not set to "1" and Timer(L) interrupt is not generated. In this mode, the interrupt factor flag FTU(H) is set to "1" by the underflow of the 16-bit counter.
At initial reset, this flag is reset to "0".

FTC0: 00FF29H•D1
FTC1: 00FF29H•D3
FTC2: 00FF29H•D5
FTC3: 00FF29H•D7
FTC4: 00FF2EH•D1
FTC5: 00FF2EH•D3
FTC6: 00FF2EH•D5
FTC7: 00FF2EH•D7

Indicates the generation of compare match interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

FTCx is the interrupt factor flag corresponding to interrupt of Timer x, and is set to "1" with the compare match signal.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
In the 16-bit mode, the interrupt factor flag FTC(L) is not set to "1" and Timer(L) interrupt is not generated. In this mode, the interrupt factor flag FTC(H) is set to "1" by the compare match of the 16-bit counter.
At initial reset, this flag is reset to "0".

5.10.10 Programming notes

(1) The programmable timer actually enters into RUN or STOP status at the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to PTRUNx, the timer stops after counting once more (+1). PTRUNx is read as "1" until the timer actually stops.
Figure 5.10.10.1 shows the timing chart at the RUN / STOP control.

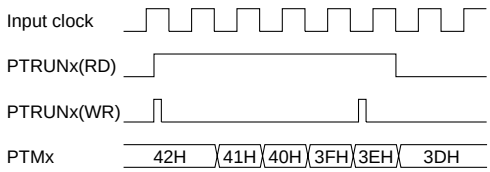


Fig. 5.10.10.1 Timing chart at RUN/STOP control

(2) When the SLP instruction is executed while the programmable timer is running (PTRUNx = "1"), the timer stops counting during SLEEP status. When SLEEP status is canceled, the timer starts counting. However, the operation becomes unstable immediately after SLEEP status is canceled. Therefore, when shifting to SLEEP status, stop the 16-bit programmable timer (PTRUNx = "0") prior to executing the SLP instruction.
Same as above, the TOUT signal output should be disabled (PTOUTx = "0") so that an unstable clock is not output to the clock output port terminal.

(3) In the 16-bit mode, reading PTM(L) does not latch the Timer(H) counter data in PTM(H). To avoid generating a borrow from Timer(L) to Timer(H), read the counter data after stopping the timer by writing "0" to PTRUN(L).

(4) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

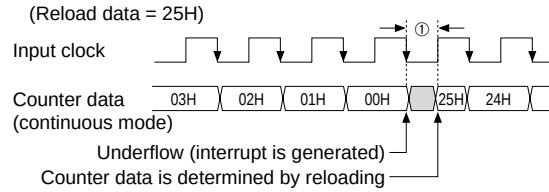


Fig. 5.10.10.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

5.11 LCD Driver

5.11.1 Configuration of LCD driver

The S1C8F626 has a built-in dot matrix LCD driver that can drive an LCD panel with a maximum of 3,072 dots (96 segments × 32 commons).
Figure 5.11.1.1 shows the configuration of the LCD driver and the drive power supply.

5.11.2 LCD power supply

The S1C8F626 generates the LCD drive voltages V_{C1} to V_{C5} using the internal power supply circuit. It is not necessary to apply an external voltage. Note that the internally generated voltage cannot be used for driving external loads.
The LCD system voltage regulator can be driven with V_{DD} or V_{D2} depending on the power supply voltage level. Use the LCD system voltage regulator power select register VDSEL for this switching. When VDSEL is set to "0", V_{DD} is selected and when VDSEL is set to "1", V_{D2} is selected. The V_{D2} voltage is generated by approximately doubling the V_{DD} voltage in the power voltage booster circuit. When using V_{D2}, write "1" to the power voltage booster circuit ON / OFF control register DBON to turn the power voltage booster circuit on. This must be done before the power source of the LCD system voltage regulator can be switched to V_{D2}.

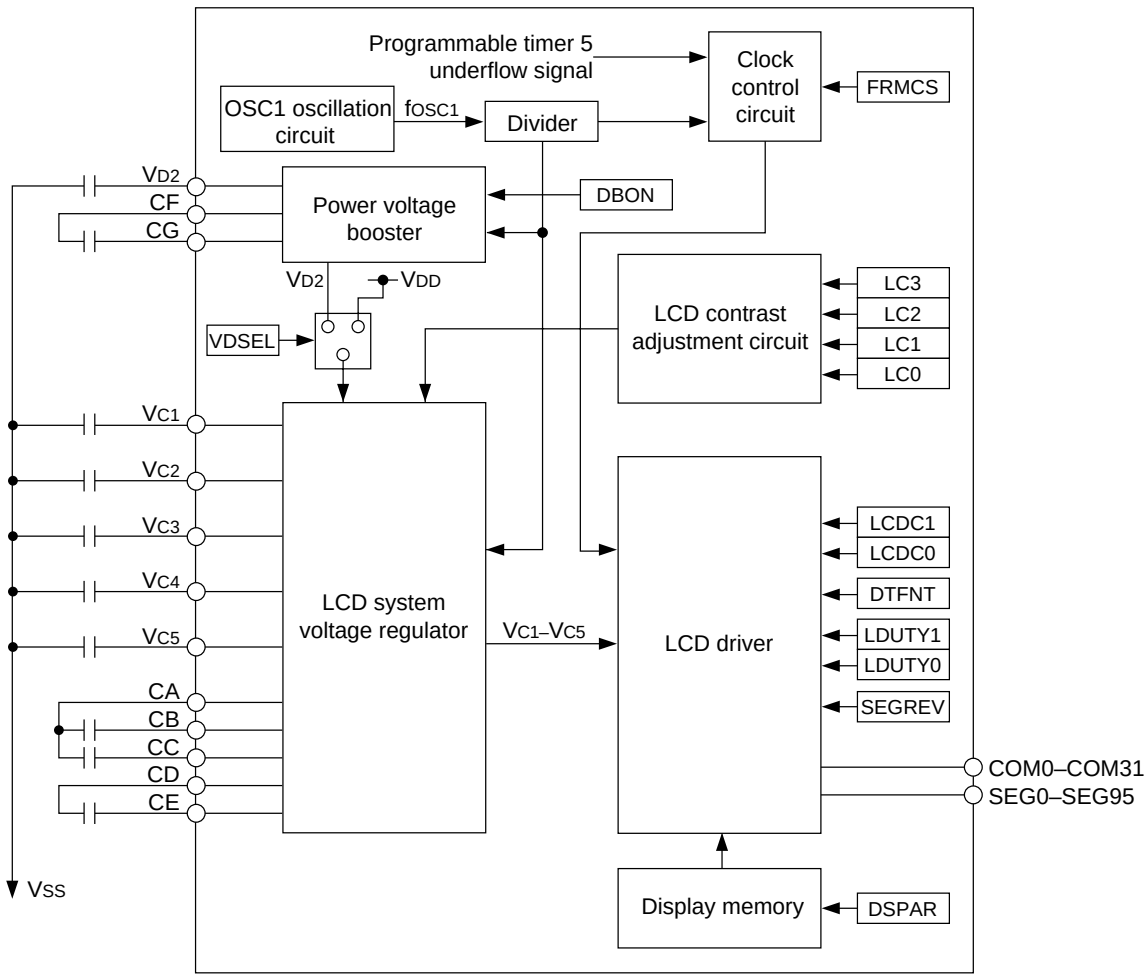


Fig. 5.11.1.1 Configuration of LCD driver and drive power supply

5.11.3 Frame frequency

This LCD driver allows selection of the source clock for generating the frame signal from the OSC1 oscillation clock (f_{OSC1}) and the programmable timer 5 underflow signal. By using programmable timer 5, flexible frame frequencies can be programmed. Refer to Section 5.10.8, "Setting frame frequency for LCD driver".
Use the LCD frame frequency source clock select register FRMCS to select the source clock. When FRMCS is set to "0", f_{OSC1} is selected, and when it is set to "1", programmable timer 5 is selected. The following shows the frame frequencies when f_{OSC1} is selected (f_{OSC1} = 32.768 kHz).
1/8 duty: 64 Hz
1/16 duty: 32 Hz
1/32 duty: 32 Hz

5.11.4 Switching drive duty

The S1C8F626 supports three types of LCD drive duty settings, 1/8, 1/16 and 1/32, and it can be switched using the LDUTY0 and LDUTY1 registers. Table 5.11.4.1 shows the relationship of the LDUTY setting, drive duty and the maximum number of displaying dots.
When 1/32 duty is selected, an LCD panel with 96 segments × 32 commons (maximum 3,072 dots) can be driven.
When 1/16 duty is selected, an LCD panel with 96 segments × 16 commons (maximum 1,536 dots) can be driven. The COM16–COM31 terminals become invalid, in that they always output an OFF signal.
When 1/8 duty is selected, an LCD panel with 96 segments × 8 commons (maximum 768 dots) can be driven. The COM8–COM31 terminals become invalid, in that they always output an OFF signal.

The drive bias is 1/5 (five potentials, V_{C1}, V_{C2}, V_{C3}, V_{C4} and V_{C5}) regardless of the drive duty selected. The respective drive waveforms are shown in Figures 5.11.4.1 to 5.11.4.3.

Table 5.11.4.1 Correspondence between drive duty and maximum number of displaying dots

LDUTY1	LDUTY0	Duty	Common terminal	Segment terminal	Maximum number of display dots
1	1	Not allowed	–	–	–
1	0	1/16	COM0–COM15	SEG0–SEG95	1,536 dots
0	1	1/32	COM0–COM31	SEG0–SEG95	3,072 dots
0	0	1/8	COM0–COM7	SEG0–SEG95	768 dots

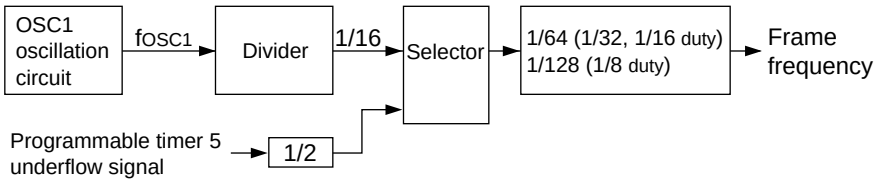
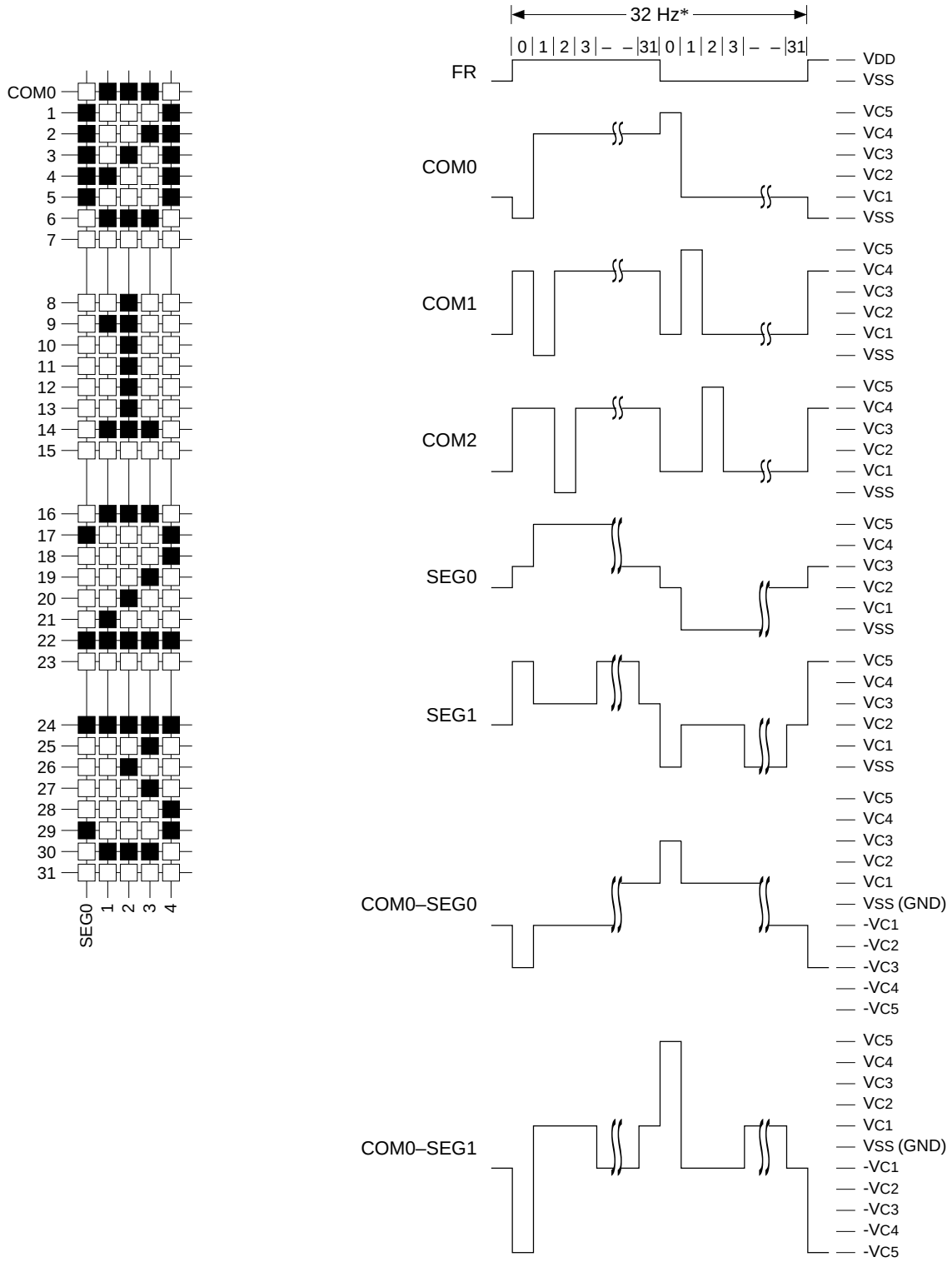
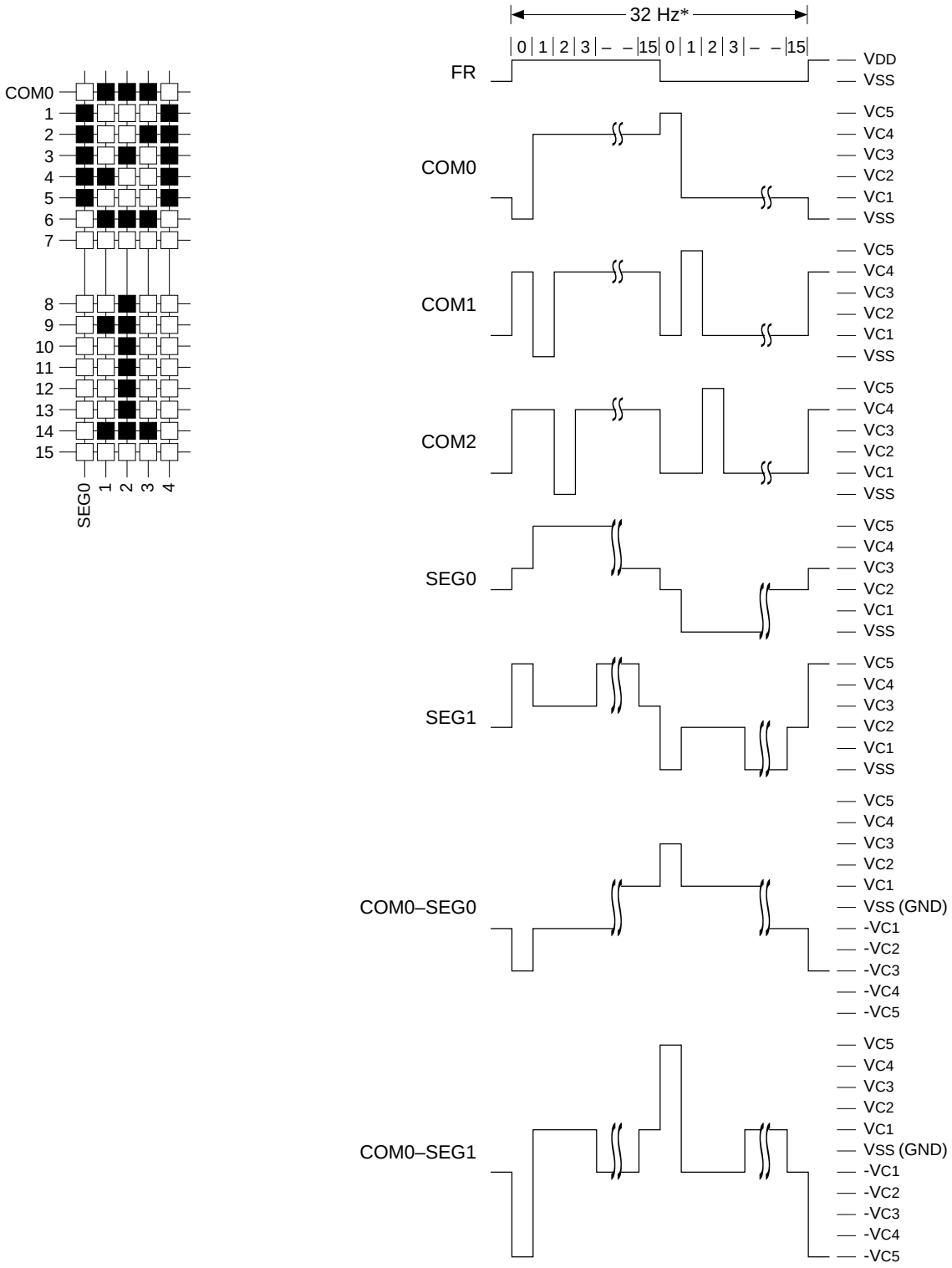


Fig. 5.11.3.1 Dividing the source clock to generate frame frequency



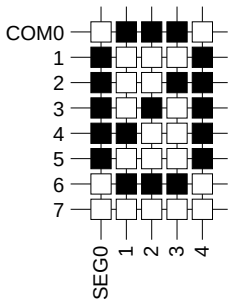
∗ when fOSC1 (32.768 kHz) is selected as the source clock (FRMCS = "0")

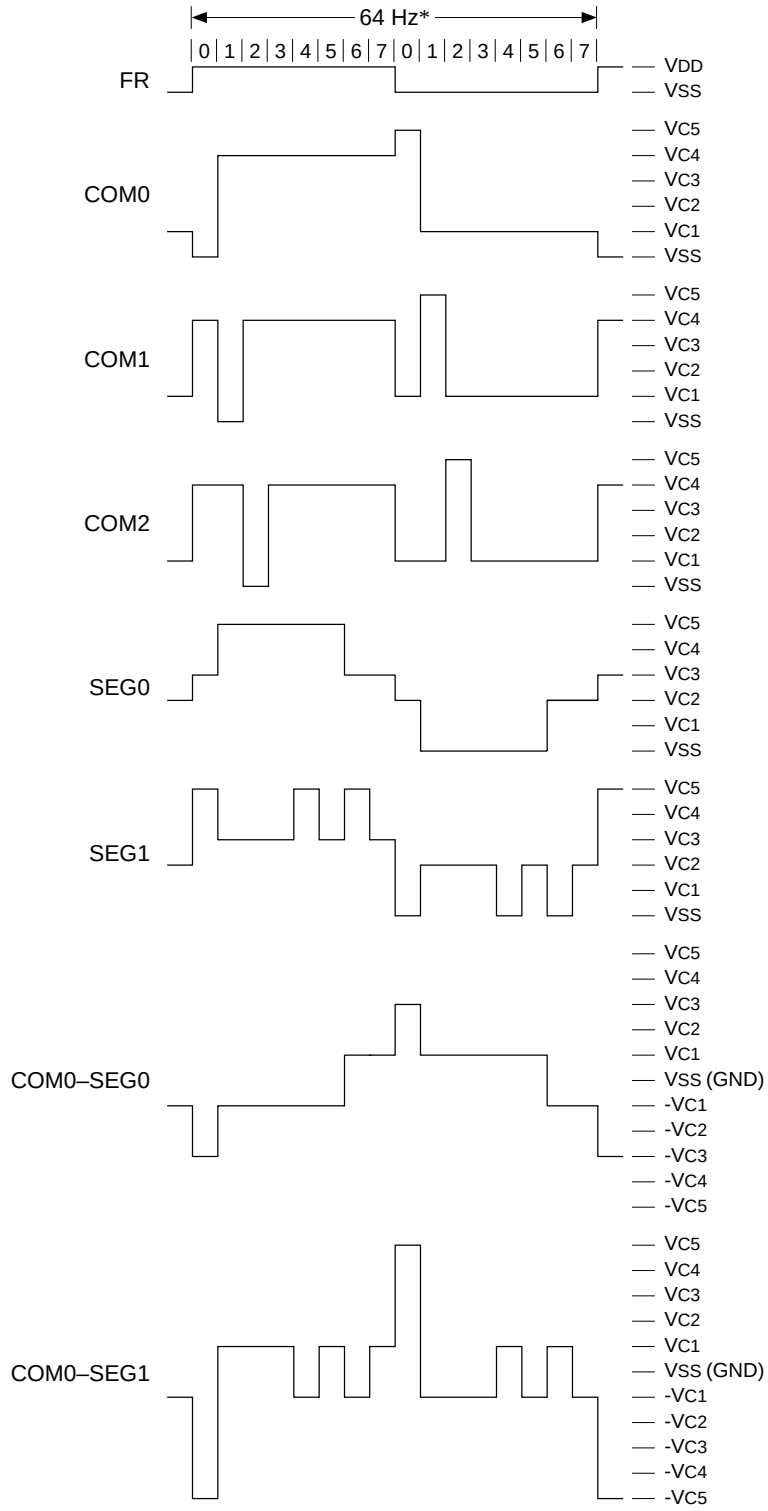
Fig. 5.11.4.1 Drive waveform for 1/32 duty



∗ when fOSC1 (32.768 kHz) is selected as the source clock (FRMCS = "0")

Fig. 5.11.4.2 Drive waveform for 1/16 duty





∗ when fosc1 (32.768 kHz) is selected as the source clock (FRMCS = "0")

Fig. 5.11.4.3 Drive waveform for 1/8 duty

5.11.5 Display memory

The S1C8F626 has a built-in 576-byte display memory. The display memory is allocated to address Fx00H–Fx5FH (x = 8–DH) and the correspondence between the memory bits and common / segment terminal is changed according to the selection status of the following items.

(1) Drive duty (1/32, 1/16 or 1/8 duty)
(2) Dot font (16 × 16/5 × 8 or 12 × 12 dots)
(3) SEG terminal assignment (normal or reverse)

When 1/16 or 1/8 duty is selected for the drive duty, two screen areas are reserved in the display memory and the area to be displayed can be selected by the display memory area select register DSPAR. When "0" is written to DSPAR, display area 0 is selected and when "1" is written, display area 1 is selected.
Furthermore, memory allocation for 16 × 16/5 × 8 dots and 12 × 12 dots can be selected in order to easily display 12 × 12-dot font characters on the LCD panel.
This selection can be done by the dot font selection register DTFNT: when "0" is written to DTFNT, 16 × 16/5 × 8 dots is selected and when "1" is written, 12 × 12 dots is selected.

The memory allocation for the SEG terminals can be reversed using the SEG assignment reverse register SEGREV.

Table 5.11.5.1 Selecting SEG assignment

SEGREV	Assignment	Fx00H	Fx5FH
1	Reverse	SEG95	SEG0
0	Normal	SEG0	SEG95

The correspondence between the display memory bits set according to the drive duty and font size, and the common / segment terminals are shown in Figures 5.11.5.1–5.11.5.6.
When "1" is written to the display memory bit corresponding to the dot on the LCD panel, the dot goes ON and when "0" is written, it goes OFF.
Since display memory is designed to permit reading / writing, it can be controlled in bit units by logical operation instructions and other means (read, modify and write instructions).
The display area bits which have not been assigned within the 576-byte display memory can be used as general purpose RAM with read / write capabilities.

Address / Data bit		0	1	2	3	4	5	COM
		0–F	0–F	0–F	0–F	0–F	0–F	
00F800H	D0	Display area						0
	D1							1
	D2							2
	D3							3
|	D4							4
	D5							5
00F85FH	D6							6
	D7							7
00F900H	D0	Display area						8
	D1							9
	D2							10
	D3							11
|	D4							12
	D5							13
00F95FH	D6							14
	D7							15
00FA00H	D0	Display area						16
	D1							17
	D2							18
	D3							19
|	D4							20
	D5							21
00FA5FH	D6							22
	D7							23
00FB00H	D0	Display area						24
	D1							25
	D2							26
	D3							27
|	D4							28
	D5							29
00FB5FH	D6							30
	D7							31
00FC00H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00FC5FH	D6							
	D7							
00FD00H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00FD5FH	D6							
	D7							
SEG (normal)*1		0–15	16–31	32–47	48–63	64–79	80–95	
SEG (reverse)*2		95–80	79–64	63–48	47–32	31–16	15–0	

∗1: SEGREV = "0" ∗2: SEGREV = "1"

Fig. 5.11.5.1 Display memory map for 1/32 duty and 16 × 16/5 × 8-dot font

Address / Data bit		0	1	2	3	4	5	COM
		0–F	0–F	0–F	0–F	0–F	0–F	
00F800H	D0	Display area						0
	D1							1
	D2							2
	D3							3
	D4							4
00F85FH	D5							5
	D6							6
	D7							7
00F900H	D0							8
	D1							9
	D2							10
	D3							11
	D4							
00F95FH	D5							
	D6							
	D7							
00FA00H	D0	Display area						12
	D1							13
	D2							14
	D3							15
	D4							
00FA5FH	D5							
	D6							
	D7							
00FB00H	D0	Display area						16
	D1							17
	D2							18
	D3							19
	D4							20
00FB5FH	D5							21
	D6							22
	D7							23
00FC00H	D0							24
	D1							25
	D2							26
	D3							27
	D4							
00FC5FH	D5							
	D6							
	D7							
00FD00H	D0	Display area						28
	D1							29
	D2							30
	D3							31
	D4							
00FD5FH	D5							
	D6							
	D7							
SEG (normal)*1		0–15	16–31	32–47	48–63	64–79	80–95	
SEG (reverse)*2		95–80	79–64	63–48	47–32	31–16	15–0	

∗1: SEGREV = "0" ∗2: SEGREV = "1"

Fig. 5.11.5.2 Display memory map for 1/32 duty and 12 × 12-dot font

Address / Data bit		0 0–F	1 0–F	2 0–F	3 0–F	4 0–F	5 0–F	COM
00F800H | 00F85FH	D0	Display area 0 (when DSPAR is set to "0")						0
	D1							1
	D2							2
	D3							3
	D4							4
	D5							5
	D6							6
	D7							7
00F900H | 00F95FH	D0	Display area 0 (when DSPAR is set to "0")						8
	D1							9
	D2							10
	D3							11
	D4							12
	D5							13
	D6							14
	D7							15
00FA00H | 00FA5FH	D0	Display area 1 (when DSPAR is set to "1")						0
	D1							1
	D2							2
	D3							3
	D4							4
	D5							5
	D6							6
	D7							7
00FB00H | 00FB5FH	D0	Display area 1 (when DSPAR is set to "1")						8
	D1							9
	D2							10
	D3							11
	D4							12
	D5							13
	D6							14
	D7							15
00FC00H | 00FC5FH	D0							
	D1							
	D2							
	D3							
	D4							
	D5							
	D6							
	D7							
00FD00H | 00FD5FH	D0							
	D1							
	D2							
	D3							
	D4							
	D5							
	D6							
	D7							
SEG (normal)*1		0–15	16–31	32–47	48–63	64–79	80–95	
SEG (reverse)*2		95–80	79–64	63–48	47–32	31–16	15–0	

∗1: SEGREV = "0" ∗2: SEGREV = "1"

Fig. 5.11.5.3 Display memory map for 1/16 duty and 16 × 16/5 × 8-dot font

Address / Data bit		0	1	2	3	4	5	COM
		0–F	0–F	0–F	0–F	0–F	0–F	
00F800H	D0	Display area 0 (when DSPAR is set to "0")						0
	D1							1
	D2							2
	D3							3
	D4							4
00F85FH	D5							5
	D6							6
	D7							7
00F900H	D0							8
	D1							9
	D2							10
	D3							11
	D4							
00F95FH	D5							
	D6							
	D7							
00FA00H	D0	Display area 0 (when DSPAR is set to "0")						12
	D1							13
	D2							14
	D3							15
	D4							
00FA5FH	D5							
	D6							
	D7							
00FB00H	D0	Display area 1 (when DSPAR is set to "1")						0
	D1							1
	D2							2
	D3							3
	D4							4
00FB5FH	D5							5
	D6							6
	D7							7
00FC00H	D0							8
	D1							9
	D2							10
	D3							11
	D4							
00FC5FH	D5							
	D6							
	D7							
00FD00H	D0	Display area 1 (when DSPAR is set to "1")						12
	D1							13
	D2							14
	D3							15
	D4							
00FD5FH	D5							
	D6							
	D7							
SEG (normal)*1		0–15	16–31	32–47	48–63	64–79	80–95	
SEG (reverse)*2		95–80	79–64	63–48	47–32	31–16	15–0	

∗1: SEGREV = "0" ∗2: SEGREV = "1"

Fig. 5.11.5.4 Display memory map for 1/16 duty and 12 × 12-dot font

Address / Data bit		0	1	2	3	4	5	COM
		0–F	0–F	0–F	0–F	0–F	0–F	
00F800H	D0	Display area 0 (when DSPAR is set to "0")						0
	D1							1
	D2							2
	D3							3
|	D4							4
	D5							5
00F85FH	D6							6
	D7							7
00F900H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00F95FH	D6							
	D7							
00FA00H	D0	Display area 1 (when DSPAR is set to "1")						0
	D1							1
	D2							2
	D3							3
|	D4							4
	D5							5
00FA5FH	D6							6
	D7							7
00FB00H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00FB5FH	D6							
	D7							
00FC00H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00FC5FH	D6							
	D7							
00FD00H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00FD5FH	D6							
	D7							
SEG (normal)*1		0–15	16–31	32–47	48–63	64–79	80–95	
SEG (reverse)*2		95–80	79–64	63–48	47–32	31–16	15–0	

∗1: SEGREV = "0" ∗2: SEGREV = "1"

Fig. 5.11.5.5 Display memory map for 1/8 duty and 5 × 8-dot font

Address / Data bit		0	1	2	3	4	5	COM
		0–F	0–F	0–F	0–F	0–F	0–F	
00F800H	D0	Display area 0 (when DSPAR is set to "0")						0
	D1							1
	D2							2
	D3							3
|	D4							4
	D5							5
00F85FH	D6							6
	D7							7
00F900H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00F95FH	D6							
	D7							
00FA00H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00FA5FH	D6							
	D7							
00FB00H	D0	Display area 1 (when DSPAR is set to "1")						0
	D1							1
	D2							2
	D3							3
|	D4							4
	D5							5
00FB5FH	D6							6
	D7							7
00FC00H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00FC5FH	D6							
	D7							
00FD00H	D0							
	D1							
	D2							
	D3							
|	D4							
	D5							
00FD5FH	D6							
	D7							
SEG (normal)*1		0–15	16–31	32–47	48–63	64–79	80–95	
SEG (reverse)*2		95–80	79–64	63–48	47–32	31–16	15–0	

∗1: SEGREV = "0" ∗2: SEGREV = "1"

Fig. 5.11.5.6 Display memory map for 1/8 duty and 12 × 12-dot font

5.11.6 Display control

The display status of the built-in LCD driver and the contrast adjustment can be controlled with the built-in LCD driver. The LCD display status can be selected by display control registers LCDC0 and LCDC1. Setting the value and display status are shown in Table 5.11.6.1.

Table 5.11.6.1 LCD display control

LCDC1	LCDC0	LCD display
1	1	All LCDs lit (Static)
1	0	All LCDs out (Dynamic)
0	1	Normal display
0	0	Drive OFF

All the dots in the LCD display can be turned on or off directly by the drive waveform output from the LCD driver, and data in the display memory is not changed. Also, since the common terminal at this time is set to static drive when all the dots are on and is set to dynamic drive when they are off, this function can be used as follows:

(1) Since all dots on is binary output (V_{C5} and V_{SS}) with static drive, the common / segment terminal can be used as a monitor terminal for the OSC1 oscillation frequency adjustment.

(2) Since all dots off is dynamic drive, you can brink the entire LCD display without changing display memory data.

Selecting LCD drive OFF turns the LCD drive power circuit OFF and all the V_{C1} to V_{C5} terminals go to V_{SS} level.
Furthermore, when the SLP instruction is executed, registers LCDC0 and LCDC1 are automatically reset to "0" (set to drive off) by hardware.

The LCD contrast can be adjusted in 16 stages. This adjustment is done by the contrast adjustment register LC0–LC3, and the setting values correspond to the contrast as shown in Table 5.11.6.2.

Table 5.11.6.2 LCD contrast adjustment

LC3	LC2	LC1	LC0	Contrast
1	1	1	1	Dark
1	1	1	0	↑
1	1	0	1	
:	:	:	:	
0	0	1	0	
0	0	0	1	↓
0	0	0	0	Light

5.11.7 Control of LCD driver

Table 5.11.7.1 shows the LCD driver control bits.

Table 5.11.7.1 LCD driver control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF03	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	VDSEL	Power source select for LCD voltage regulator	V_{D2}	V_{DD}	0	R/W	
	D0	DBON	Power voltage booster On/Off control	On	Off	0	R/W	
00FF10	D7	HLMOD	Heavy load protection mode	On	Off	0	R/W	
	D6	SEGREV	Reverse SEG assignment	Reverse	Normal	0	R/W	
	D5	–	R/W register	1	0	0	R/W	Reserved register
	D4	–	R/W register	1	0	0	R/W	
	D3	–	R/W register	1	0	0	R/W	
	D2	DTFNT	LCD dot font selection	12×12	16×16/5×8	0	R/W	
	D1	LDUTY1	LCD drive duty selection LDUTY1 LDUTY0 Duty 1 1 Not allowed 1 0 1/16 0 1 1/32 0 0 1/8			1	R/W	
	D0	LDUTY0				0	R/W	
00FF11	D7	FRMCS	LCD frame signal source clock selection	PTM	f_{OSC1}	0	R/W	
	D6	DSPAR	LCD display memory area selection	Display area 1	Display area 0	0	R/W	
	D5	LCDC1	LCD display control LCDC1 LCDC0 LCD display 1 1 All LCDs lit 1 0 All LCDs out 0 1 Normal display 0 0 Drive off			0	R/W	These bits are reset to (0, 0) when SLP instruction is executed.
	D4	LCDC0				0	R/W	
	D3	LC3	LCD contrast adjustment LC3 LC2 LC1 LC0 Contrast 1 1 1 1 Dark 1 1 1 0 : : : : : : 0 0 0 0 Light			0	R/W	
	D2	LC2				0	R/W	
	D1	LC1				0	R/W	
	D0	LC0				0	R/W	

LDUTY0, LDUTY1: 00FF10H•D0, D1

Selects the drive duty.

Table 5.11.7.2 Setting drive duty

LDUTY1	LDUTY0	Duty	Common terminal	Segment terminal	Maximum number of display dots
1	1	Not allowed	–	–	–
1	0	1/16	COM0–COM15	SEG0–SEG95	1,536 dots
0	1	1/32	COM0–COM31	SEG0–SEG95	3,072 dots
0	0	1/8	COM0–COM7	SEG0–SEG95	768 dots

At initial reset, LDUTY is set to "10" (1/16 duty).

DTFNT: 00FF10H•D2

Selects the dot font.

When "1" is written: 12 × 12 dots
When "0" is written: 16 × 16 / 5 × 8 dots
Reading: Valid

Select 16 × 16 / 5 × 8 dots or 12 × 12 dots type for the display memory area.
When "0" is written to DTFNT, 16 × 16 / 5 × 8 dots is selected and when "1" is written, 12 × 12 dots is selected.
The correspondence between the display memory bits set according to the dot font, and the common / segment terminals are shown in Figures 5.11.5.1–5.11.5.5.
At initial reset, DTFNT is set to "0" (16 × 16 / 5 × 8 dots).

SEGREV: 00FF10H•D6

Reverses the memory allocation for the SEG terminals.

Table 5.11.7.3 Selecting SEG assignment

SEGREV	Assignment	Fx00H	Fx5FH
1	Reverse	SEG95	SEG0
0	Normal	SEG0	SEG95

At initial reset, SEGREV is set to "0" (normal).

DSPAR: 00FF11H•D6

Selects the display area.

When "1" is written: Display area 1
When "0" is written: Display area 0
Reading: Valid

An area to be displayed is selected from two areas in the display memory.
When "0" is written to DSPAR, display area 0 is selected and when "1" is written, display area 1 is selected.
The correspondence between the display memory bits set according to the display area, and the common / segment terminals are shown in Figures 5.11.5.1–5.11.5.5.
At initial reset, DSPAR is set to "0" (display area 0).

LCDC0, LCDC1: 00FF11H•D4, D5

Controls the LCD display.

Table 5.11.7.4 LCD display control

LCDC1	LCDC0	LCD display
1	1	All LCDs lit (Static)
1	0	All LCDs out (Dynamic)
0	1	Normal display
0	0	Drive OFF

The four settings mentioned above can be made without changing the display memory data.
At initial reset and in the SLEEP status, this register is set to "0" (drive off).

LC0–LC3: 00FF11H•D0–D3

Adjusts the LCD contrast.

Table 5.11.7.5 LCD contract adjustment

LC3	LC2	LC1	LC0	Contrast
1	1	1	1	Dark
1	1	1	0	↑
1	1	0	1	
1	1	0	0	
1	0	1	1	
1	0	1	0	
1	0	0	1	
1	0	0	0	
0	1	1	1	
0	1	1	0	
0	1	0	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	↓
0	0	0	0	Light

The contrast can be adjusted in 16 stages as mentioned above. This adjustment changes the drive voltage on terminals V_{C1} to V_{C5}.
At initial reset, this register is set to "0".

FRMCS: 00FF11H•D7

Selects the source clock for generating the frame signal.

When "1" is written: Programmable timer 5
When "0" is written: f_{OSC1}
Reading: Valid

When "0" is written to FRMCS, f_{OSC1} is selected, and when "1" is written, programmable timer 5 is selected.
At initial reset, FRMCS is set to "0" (f_{OSC1}).

DBON: 00FF03H•D0

Control the power voltage booster circuit.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to DBON, the power voltage booster activates and almost doubles the V_{DD} voltage to generate the V_{D2} voltage. Turn the power voltage booster on when driving the LCD system voltage regulator with V_{D2}.
When "0" is written to DBON, the power voltage booster goes off. When driving the LCD system voltage regulator with V_{DD}, turn the power voltage booster off to reduce current consumption.
At initial reset, DBON is set to "0" (OFF).

VDSEL: 00FF03H•D1

Selects the power voltage for the LCD system voltage regulator.

When "1" is written: V_{D2}
When "0" is written: V_{DD}
Reading: Valid

When "1" is written to VDSEL, the LCD system voltage regulator is driven with V_{D2} generated by the power voltage booster. Before this setting is made, it is necessary to write "1" to DBON to turn on the power voltage booster. Furthermore, do not switch the power voltage to V_{D2} for at least 1 msec after the power voltage booster is turned on to allow V_{D2} stabilize.
When "0" is written to VDSEL, the LCD system voltage regulator is driven with V_{DD}.
At initial reset, VDSEL is set to "0" (V_{DD}).

5.11.8 Programming notes

(1) When the SLP instruction is executed, display control registers LCDC0 and LCDC1 are automatically reset to "0" by hardware.

(2) When driving the LCD system voltage regulator with V_{D2}, wait at least 1 msec for stabilization of the voltage before switching the power voltage for the LCD system voltage regulator to V_{D2} using VDSEL after the power voltage booster is turned on.

5.12 Supply Voltage Detection (SVD) Circuit

5.12.1 Configuration of SVD circuit

The S1C8F626 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON / OFF and the SVD criteria voltage setting can be done with software.
Figure 5.12.1.1 shows the configuration of the SVD circuit.

5.12.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (V_{DD}–V_{SS}) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be set for the 13 types shown in Table 5.12.2.1 by the SVDS3–SVDS0 registers.

Table 5.12.2.1 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
1	1	1	1	2.7
1	1	1	0	2.6
1	1	0	1	2.5
1	1	0	0	2.4
1	0	1	1	2.3
1	0	1	0	2.2
1	0	0	1	2.1
1	0	0	0	2.05
0	1	1	1	2.0
0	1	1	0	1.95
0	1	0	1	1.9
0	1	0	0	1.85
0	0	1	1	1.8
0	0	1	0	–
0	0	0	1	–
0	0	0	0	–

When the SVDON register is set to "1", source voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes OFF.
To obtain a stable detection result, the SVD circuit must be ON for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is ON, the IC draws a large current, so keep the SVD circuit off unless it is.

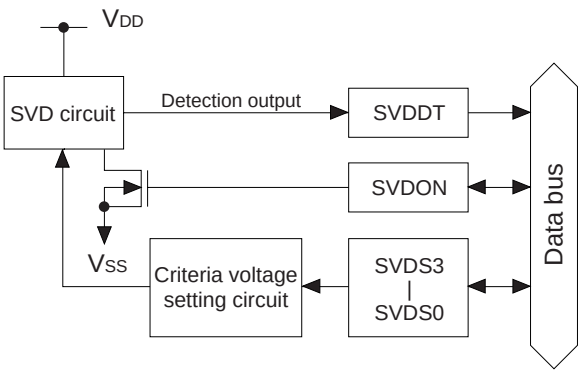


Fig. 5.12.1.1 Configuration of SVD circuit

5.12.3 Control of SVD circuit

Table 5.12.3.1 shows the SVD circuit control bits.

Table 5.12.3.1 SVD circuit control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF12	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	SVDDT	SVD detection data	Low	Normal	0	R	
	D4	SVDON	SVD circuit On/Off	On	Off	0	R/W	
	D3	SVDS3	SVD criteria voltage setting			0	R/W	
	D2	SVDS2	SVDS3 SVDS2 SVDS1 SVDS0 Voltage (V) 1 1 1 1 2.7 1 1 1 0 2.6 1 1 0 1 2.5 : : : : : 0 0 1 1 1.8			0	R/W	
	D1	SVDS1				0	R/W	
	D0	SVDS0				0	R/W	

SVDS3–SVDS0: 00FF12H•D3–D0

Criteria voltage for SVD is set as shown in Table 5.12.2.1.
At initial reset, this register is set to "0".

SVDON: 00FF12H•D4

Controls the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When the SVDON register is set to "1", a supply voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be ON for at least 500 µsec.
At initial reset, this register is set to "0".

SVDDT: 00FF12H•D5

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

5.12.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be ON for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

5.13 Heavy Load Protection Function

5.13.1 Outline of heavy load protection function

The S1C8F626 has a heavy load protection function to prevent malfunction due to a power voltage fluctuation caused by a heavy battery load such as when an external lamp is driven and while the IC is running in high-speed with the OSC3 clock. This function works when the IC enters the heavy load protection mode. Set the IC into the heavy load protection mode when there are inconsistencies in density on the LCD panel as well as when the IC is under one of the condition above.

The normal mode (heavy load protection function is off) changes to the heavy load protection mode (heavy load protection function is on) when the software changes the mode to the heavy load protection mode (HLMOD = "1").

Note: In the heavy load protection mode, more current is consumed than in the normal mode. Unless necessary, do not select the heavy load protection mode with the software.

5.13.2 Control of heavy load protection function

Table 5.13.2.1 shows the control bit for the heavy load protection function.

Table 5.13.2.1 Control bit for heavy load protection function

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF10	D7	HLMOD	Heavy load protection mode	On	Off	0	R/W	
	D6	SEGREV	Reverse SEG assignment	Reverse	Normal	0	R/W	
	D5	–	R/W register	1	0	0	R/W	Reserved register
	D4	–	R/W register	1	0	0	R/W	
	D3	–	R/W register	1	0	0	R/W	
	D2	DTFNT	LCD dot font selection	12×12	16×16/5×8	0	R/W	
	D1	LDUTY1	LCD drive duty selection LDUTY1 LDUTY0 Duty 1 1 Not allowed			1	R/W	
	D0	LDUTY0	1 0 1/16 0 1 1/32 0 0 1/8			0	R/W	

HLMOD: 00FF10H•D7

Controls the heavy load protection mode.

When "1" is written: Heavy load protection ON
When "0" is written: Heavy load protection OFF
Reading: Valid

The device enters the heavy load protection mode by writing "1" to HLMOD, and returns to the normal mode by writing "0". In the heavy load protection mode, the consumed current becomes larger. Unless necessary, do not select the heavy load protection mode with the software.
At initial reset, this register is set to "0".

5.13.3 Programming note

In the heavy load protection mode, more current is consumed than in the normal mode. Unless necessary, do not select the heavy load protection mode with the software.

5.14 Interrupt and Standby Status

■ Types of interrupts

5 systems and 37 types of interrupts have been provided for the S1C8F626.

External interrupt
- K00–K07 input interrupt (8 types)

Internal interrupt
- Clock timer interrupt (4 types)
- Stopwatch timer interrupt (3 types)
- Programmable timer interrupt (16 types)
- Serial interface interrupt (6 types)

An interrupt factor flag that indicates the generation of an interrupt factor and an interrupt enable register that sets enable / disable for interrupt requests have been provided for each interrupt and interrupt generation can be optionally set for each factor. In addition, an interrupt priority register has been provided for each system of interrupts and the priority of interrupt processing can be set to 3 levels in each system.
Figure 5.14.1 shows the configuration of the interrupt circuit.
Refer to the explanations of the respective peripheral circuits for details on each interrupt.

■ HALT status

By executing the program's HALT instruction, the S1C8F626 enters the HALT status.
Since CPU operation stops in the HALT status, power consumption can be reduced with only peripheral circuit operation.
Cancellation of the HALT status is done by initial reset or an optional interrupt request, and the CPU restarts program execution from an exception processing routine.
See the "S1C88 Core CPU Manual" for the HALT status and reactivation sequence.

■ SLEEP status

By executing the program's SLP instruction, the S1C8F626 enters the SLEEP status.
Since the operation of the CPU and peripheral circuits stop completely in the SLEEP status, power consumption can be reduced even more than in the HALT status.
Cancellation of the SLEEP status is done by initial reset or an input interrupt from the input port. The CPU reactivates after waiting 128 / f_{OSC1} or 512 / f_{OSC3} seconds of oscillation stabilization time (the oscillation stabilization time varies depending on the operating clock being used when the SLP instruction is executed). At this time, the CPU restarts program execution from an exception processing routine (input interrupt routine).

Note: The oscillation becomes unstable for a while after SLEEP status is cancelled, the wait time for restarting the CPU may be longer than 128/f_{OSC1} or 512/f_{OSC3} seconds.

5.14.1 Interrupt generation conditions

The interrupt factor flags that indicate the generation of their respective interrupt factors are provided for the previously indicated 5 systems and 37 types of interrupts and they will be set to "1" by the generation of a factor.
In addition, interrupt enable registers with a 1 to 1 correspondence to each of the interrupt factor flags are provided. An interrupt is enabled when "1" is written and interrupt is disabled when "0" is written.

The CPU manages the enable / disable of interrupt requests at the interrupt priority level. An interrupt priority register that sets the priority level is provided for each of the interrupts of the 5 systems and the CPU accepts only interrupts above the level that has been indicated with the interrupt flags (I0 and I1).
Consequently, the following three conditions are necessary for the CPU to accept the interrupt.

(1) The interrupt factor flag has been set to "1" by generation of an interrupt factor.

(2) The interrupt enable register corresponding to the above has been set to "1".

(3) The interrupt priority register corresponding to the above has been set to a priority level higher than the interrupt flag (I0 and I1) setting.

The CPU initially samples the interrupt for the first op-code fetch cycle of each instruction. Thereupon, the CPU shifts to the exception processing when the above mentioned conditions have been established.
See the "S1C88 Core CPU Manual" for the exception processing sequence.

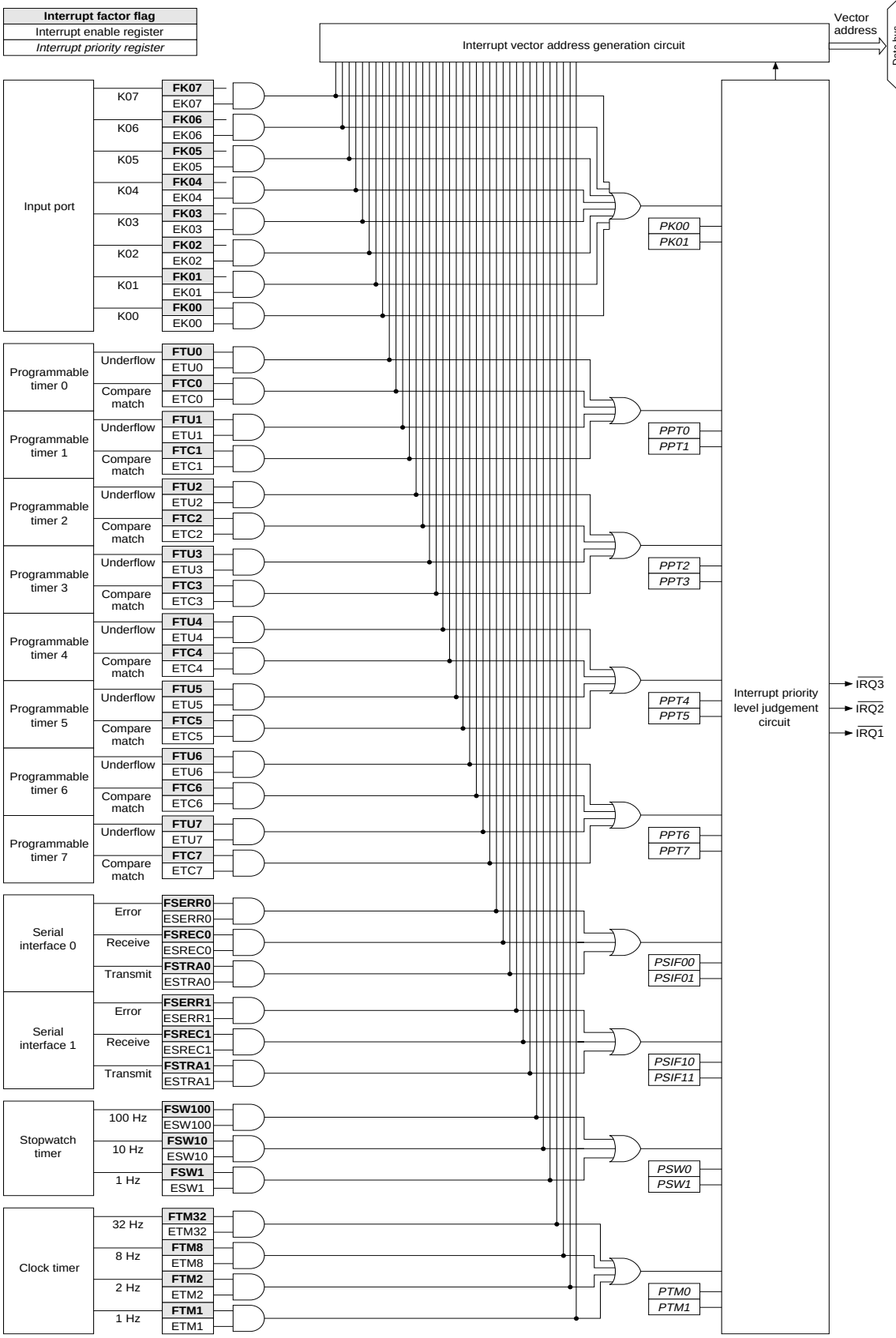


Fig. 5.14.1 Configuration of interrupt circuit

5.14.2 Interrupt factor flag

Table 5.14.2.1 shows the correspondence between the factors generating an interrupt and the interrupt factor flags.
The corresponding interrupt factor flags are set to "1" by generation of the respective interrupt factors. The corresponding interrupt factor can be confirmed by reading the flags through software.
Interrupt factor flag that has been set to "1" is reset to "0" by writing "1".
At initial reset, the interrupt factor flags are reset to "0".

Note: When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

Table 5.14.2.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
K07 input of falling edge or rising edge (instruction at KCP07)	FK07	00FF28H·D7
K06 input of falling edge or rising edge (instruction at KCP06)	FK06	00FF28H·D6
K05 input of falling edge or rising edge (instruction at KCP05)	FK05	00FF28H·D5
K04 input of falling edge or rising edge (instruction at KCP04)	FK04	00FF28H·D4
K03 input of falling edge or rising edge (instruction at KCP03)	FK03	00FF28H·D3
K02 input of falling edge or rising edge (instruction at KCP02)	FK02	00FF28H·D2
K01 input of falling edge or rising edge (instruction at KCP01)	FK01	00FF28H·D1
K00 input of falling edge or rising edge (instruction at KCP00)	FK00	00FF28H·D0
Programmable timer 0 underflow	FTU0	00FF29H·D0
Programmable timer 0 compare match	FTC0	00FF29H·D1
Programmable timer 1 underflow	FTU1	00FF29H·D2
Programmable timer 1 compare match	FTC1	00FF29H·D3
Programmable timer 2 underflow	FTU2	00FF29H·D4
Programmable timer 2 compare match	FTC2	00FF29H·D5
Programmable timer 3 underflow	FTU3	00FF29H·D6
Programmable timer 3 compare match	FTC3	00FF29H·D7
Programmable timer 4 underflow	FTU4	00FF2EH·D0
Programmable timer 4 compare match	FTC4	00FF2EH·D1
Programmable timer 5 underflow	FTU5	00FF2EH·D2
Programmable timer 5 compare match	FTC5	00FF2EH·D3
Programmable timer 6 underflow	FTU6	00FF2EH·D4
Programmable timer 6 compare match	FTC6	00FF2EH·D5
Programmable timer 7 underflow	FTU7	00FF2EH·D6
Programmable timer 7 compare match	FTC7	00FF2EH·D7
Serial interface 0 receiving error (in asynchronous mode)	FSERR0	00FF27H·D2
Serial interface 0 receiving completion	FSREC0	00FF27H·D1
Serial interface 0 transmitting completion	FSTRA0	00FF27H·D0
Serial interface 1 receiving error (in asynchronous mode)	FSERR1	00FF27H·D5
Serial interface 1 receiving completion	FSREC1	00FF27H·D4
Serial interface 1 transmitting completion	FSTRA1	00FF27H·D3
Falling edge of the stopwatch timer 100 Hz signal	FSW100	00FF26H·D6
Falling edge of the stopwatch timer 10 Hz signal	FSW10	00FF26H·D5
Falling edge of the stopwatch timer 1 Hz signal	FSW1	00FF26H·D4
Falling edge of the clock timer 32 Hz signal	FTM32	00FF26H·D3
Falling edge of the clock timer 8 Hz signal	FTM8	00FF26H·D2
Falling edge of the clock timer 2 Hz signal	FTM2	00FF26H·D1
Falling edge of the clock timer 1 Hz signal	FTM1	00FF26H·D0

5.14.3 Interrupt enable register

The interrupt enable register has a 1 to 1 correspondence with each interrupt factor flag and enable / disable of interrupt requests can be set.

When "1" is written to the interrupt enable register, an interrupt request is enabled, and is disabled when "0" is written.

This register also permits reading, thus making it possible to confirm that a status has been set.
At initial reset, the interrupt enable registers are set to "0" and shifts to the interrupt disable status.
Table 5.14.3.1 shows the correspondence between the interrupt enable registers and the interrupt factor flags.

Table 5.14.3.1 Interrupt enable registers and interrupt factor flags

Interrupt	Interrupt factor flag		Interrupt enable register	
K07 input	FK07	00FF28H·D7	EK07	00FF24H·D7
K06 input	FK06	00FF28H·D6	EK06	00FF24H·D6
K05 input	FK05	00FF28H·D5	EK05	00FF24H·D5
K04 input	FK04	00FF28H·D4	EK04	00FF24H·D4
K03 input	FK03	00FF28H·D3	EK03	00FF24H·D3
K02 input	FK02	00FF28H·D2	EK02	00FF24H·D2
K01 input	FK01	00FF28H·D1	EK01	00FF24H·D1
K00 input	FK00	00FF28H·D0	EK00	00FF24H·D0
Timer 0 underflow	FTU0	00FF29H·D0	ETU0	00FF25H·D0
Timer 0 compare match	FTC0	00FF29H·D1	ETC0	00FF25H·D1
Timer 1 underflow	FTU1	00FF29H·D2	ETU1	00FF25H·D2
Timer 1 compare match	FTC1	00FF29H·D3	ETC1	00FF25H·D3
Timer 2 underflow	FTU2	00FF29H·D4	ETU2	00FF25H·D4
Timer 2 compare match	FTC2	00FF29H·D5	ETC2	00FF25H·D5
Timer 3 underflow	FTU3	00FF29H·D6	ETU3	00FF25H·D6
Timer 3 compare match	FTC3	00FF29H·D7	ETC3	00FF25H·D7
Timer 4 underflow	FTU4	00FF2EH·D0	ETU4	00FF2CH·D0
Timer 4 compare match	FTC4	00FF2EH·D1	ETC4	00FF2CH·D1
Timer 5 underflow	FTU5	00FF2EH·D2	ETU5	00FF2CH·D2
Timer 5 compare match	FTC5	00FF2EH·D3	ETC5	00FF2CH·D3
Timer 6 underflow	FTU6	00FF2EH·D4	ETU6	00FF2CH·D4
Timer 6 compare match	FTC6	00FF2EH·D5	ETC6	00FF2CH·D5
Timer 7 underflow	FTU7	00FF2EH·D6	ETU7	00FF2CH·D6
Timer 7 compare match	FTC7	00FF2EH·D7	ETC7	00FF2CH·D7
Serial interface 0 receiving error	FSERR0	00FF27H·D2	ESERR0	00FF23H·D2
Serial interface 0 receiving completion	FSREC0	00FF27H·D1	ESREC0	00FF23H·D1
Serial interface 0 transmitting completion	FSTRA0	00FF27H·D0	ESTRA0	00FF23H·D0
Serial interface 1 receiving error	FSERR1	00FF27H·D5	ESERR1	00FF23H·D5
Serial interface 1 receiving completion	FSREC1	00FF27H·D4	ESREC1	00FF23H·D4
Serial interface 1 transmitting completion	FSTRA1	00FF27H·D3	ESTRA1	00FF23H·D3
Stopwatch timer 100 Hz	FSW100	00FF26H·D6	ESW100	00FF22H·D6
Stopwatch timer 10 Hz	FSW10	00FF26H·D5	ESW10	00FF22H·D5
Stopwatch timer 1 Hz	FSW1	00FF26H·D4	ESW1	00FF22H·D4
Clock timer 32 Hz	FTM32	00FF26H·D3	ETM32	00FF22H·D3
Clock timer 8 Hz	FTM8	00FF26H·D2	ETM8	00FF22H·D2
Clock timer 2 Hz	FTM2	00FF26H·D1	ETM2	00FF22H·D1
Clock timer 1 Hz	FTM1	00FF26H·D0	ETM1	00FF22H·D0

5.14.4 Interrupt priority register and interrupt priority level

Table 5.14.4.1 Interrupt priority register

Interrupt	Interrupt priority register	
K00–K07 input interrupt	PK00, PK01	00FF20·D6, D7
Programmable timer interrupt 1–0	PPT0, PPT1	00FF21·D2, D3
Programmable timer interrupt 3–2	PPT2, PPT3	00FF21·D4, D5
Programmable timer interrupt 5–4	PPT4, PPT5	00FF2A·D0, D1
Programmable timer interrupt 7–6	PPT6, PPT7	00FF2A·D2, D3
Serial interface 0 interrupt	PSIF00, PSIF01	00FF20·D4, D5
Serial interface 1 interrupt	PSIF10, PSIF11	00FF21·D0, D1
Stopwatch timer interrupt	PSW0, PSW1	00FF20·D2, D3
Clock timer interrupt	PTM0, PTM1	00FF20·D0, D1

The interrupt priority registers shown in Table 5.14.4.1 are set to each system of interrupts and the interrupt priority levels for the CPU can be set to the optional priority level (0–3). As a result, it is possible to have multiple interrupts that match the system's interrupt processing priority levels.

The interrupt priority level between each system can optionally be set to three levels by the interrupt priority register. However, when more than one system is set to the same priority level, they are processed according to the default priority level.

Table 5.14.4.2 Setting of interrupt priority level

P*1	P*0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, the interrupt priority registers are all set to "0" and each interrupt is set to level 0. Furthermore, the priority levels in each system have been previously decided and they cannot be changed.
The CPU can mask each interrupt by setting the interrupt flags (I0 and I1). The relation between the interrupt priority level of each system and interrupt flags is shown in Table 5.14.4.3, and the CPU accepts only interrupts above the level indicated by the interrupt flags.
The $\overline{NMI}$ (watchdog timer) that has level 4 priority, is always accepted regardless of the setting of the interrupt flags.

Table 5.14.4.3 Interrupt mask setting of CPU

I1	I0	Acceptable interrupt
1	1	Level 4 ($\overline{NMI}$)
1	0	Level 4, Level 3 ($\overline{IRQ3}$)
0	1	Level 4, Level 3, Level 2 ($\overline{IRQ2}$)
0	0	Level 4, Level 3, Level 2, Level 1 ($\overline{IRQ1}$)

After an interrupt has been accepted, the interrupt flags are written to the level of that interrupt. However, interrupt flags after an $\overline{NMI}$ has been accepted are written to level 3 (I0 = I1 = "1").

Table 5.14.4.4 Interrupt flags after acceptance of interrupt

Accepted interrupt priority level		I1	I0
Level 4	($\overline{NMI}$)	1	1
Level 3	($\overline{IRQ3}$)	1	1
Level 2	($\overline{IRQ2}$)	1	0
Level 1	($\overline{IRQ1}$)	0	1

The set interrupt flags are reset to their original value on return from the interrupt processing routine. Consequently, multiple interrupts up to 3 levels can be controlled by the initial settings of the interrupt priority registers alone. Additional multiplexing can be realized by rewriting the interrupt flags and interrupt enable register in the interrupt processing routine.

Note: Beware. If the interrupt flags have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

5.14.5 Exception processing vectors

When the CPU accepts an interrupt request, it starts exception processing following completion of the instruction being executed. In exception processing, the following operations branch the program.

(1) In the minimum mode, the program counter (PC) and system condition flag (SC) are moved to stack and in the maximum mode, the code bank register (CB), PC and SC are moved.

(2) The branch destination address is read from the exception processing vector corresponding to each exception processing (interrupt) factor and is placed in the PC.

An exception vector is 2 bytes of data in which the top address of each exception (interrupt) processing routine has been stored and the vector addresses correspond to the exception processing factors as shown in Table 5.14.5.1.

Note: An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the top portion of an exception processing routine must be described within the common area (000000H–007FFFH).

Table 5.14.5.1 Vector address and exception processing correspondence

Vector address	Exception processing factor	Priority
000000H	Reset	High ↑
000002H	Zero division	
000004H	Watchdog timer ($\overline{\text{NMI}}$)	
000006H	K07 input interrupt	
000008H	K06 input interrupt	
00000AH	K05 input interrupt	
00000CH	K04 input interrupt	
00000EH	K03 input interrupt	
000010H	K02 input interrupt	
000012H	K01 input interrupt	
000014H	K00 input interrupt	
000016H	PTM 0 underflow interrupt	
000018H	PTM 0 compare match interrupt	
00001AH	PTM 1 underflow interrupt	
00001CH	PTM 1 compare match interrupt	
00001EH	PTM 2 underflow interrupt	
000020H	PTM 2 compare match interrupt	
000022H	PTM 3 underflow interrupt	
000024H	PTM 3 compare match interrupt	
000026H	System reserved (cannot be used)	
000028H	Serial I/F 0 error interrupt	
00002AH	Serial I/F 0 receiving complete interrupt	
00002CH	Serial I/F 0 transmitting complete interrupt	
00002EH	Stopwatch timer 100 Hz interrupt	
000030H	Stopwatch timer 10 Hz interrupt	
000032H	Stopwatch timer 1 Hz interrupt	
000034H	Clock timer 32 Hz interrupt	
000036H	Clock timer 8 Hz interrupt	
000038H	Clock timer 2 Hz interrupt	
00003AH	Clock timer 1 Hz interrupt	
00003CH	PTM 4 underflow interrupt	
00003EH	PTM 4 compare match interrupt	
000040H	PTM 5 underflow interrupt	
000042H	PTM 5 compare match interrupt	
000044H	PTM 6 underflow interrupt	
000046H	PTM 6 compare match interrupt	
000048H	PTM 7 underflow interrupt	
00004AH	PTM 7 compare match interrupt	
00004CH	Serial I/F 1 error interrupt	
00004EH	Serial I/F 1 receiving complete interrupt	↓
000050H	Serial I/F 1 transmitting complete interrupt	Low
000052H	System reserved (cannot be used)	No priority rating
000054H : 0000FEH	Software interrupt	

5.14.6 Control of interrupt

Table 5.14.6.1 shows the interrupt control bits.

Table 5.14.6.1(a) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF01 PSIF00 PSW1 PSW0 PTM1 PTM0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF01	Serial interface 0 interrupt priority register			0	R/W	
	D4	PSIF00						
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0						
00FF21	D7	–	–	1	0	0	R/W	Reserved register
	D6	–	–	1	0	0	R/W	
	D5	PPT3	Programmable timer 3–2 interrupt priority register	PPT3 PPT2 PPT1 PPT0 PSIF11 PSIF10 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D4	PPT2						
	D3	PPT1	Programmable timer 1–0 interrupt priority register			0	R/W	
	D2	PPT0						
	D1	PSIF11	Serial interface 1 interrupt priority register			0	R/W	
	D0	PSIF10						
00FF2A	D7	–		–	–	–		Constantly "0" when being read
	D6	–		–	–	–		
	D5	–		–	–	–		
	D4	–		–	–	–		
	D3	PPT7		PPT7 PPT6 PPT5 PPT4 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D2	PPT6						
	D1	PPT5				0	R/W	
	D0	PPT4						
00FF22	D7	–	–	1	0	0	R/W	Reserved register
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register					
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register					
	D3	ETM32	Clock timer 32 Hz interrupt enable register					
	D2	ETM8	Clock timer 8 Hz interrupt enable register					
	D1	ETM2	Clock timer 2 Hz interrupt enable register					
	D0	ETM1	Clock timer 1 Hz interrupt enable register					
00FF23	D7	–	–	1	0	0	R/W	Reserved register
	D6	–	–	1	0	0	R/W	
	D5	ESERR1	Serial I/F 1 (error) interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D4	ESREC1	Serial I/F 1 (receiving) interrupt enable register					
	D3	ESTRA1	Serial I/F 1 (transmitting) interrupt enable register					
	D2	ESERR0	Serial I/F 0 (error) interrupt enable register					
	D1	ESREC0	Serial I/F 0 (receiving) interrupt enable register					
	D0	ESTRA0	Serial I/F 0 (transmitting) interrupt enable register					

Table 5.14.6.1(b) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF24	D7	EK07	K07 interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	EK06	K06 interrupt enable					
	D5	EK05	K05 interrupt enable					
	D4	EK04	K04 interrupt enable					
	D3	EK03	K03 interrupt enable					
	D2	EK02	K02 interrupt enable					
	D1	EK01	K01 interrupt enable					
	D0	EK00	K00 interrupt enable					
00FF25	D7	ETC3	PTM3 compare match interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	ETU3	PTM3 underflow interrupt enable					
	D5	ETC2	PTM2 compare match interrupt enable					
	D4	ETU2	PTM2 underflow interrupt enable					
	D3	ETC1	PTM1 compare match interrupt enable					
	D2	ETU1	PTM1 underflow interrupt enable					
	D1	ETC0	PTM0 compare match interrupt enable					
	D0	ETU0	PTM0 underflow interrupt enable					
00FF2C	D7	ETC7	PTM7 compare match interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	ETU7	PTM7 underflow interrupt enable					
	D5	ETC6	PTM6 compare match interrupt enable					
	D4	ETU6	PTM6 underflow interrupt enable					
	D3	ETC5	PTM5 compare match interrupt enable					
	D2	ETU5	PTM5 underflow interrupt enable					
	D1	ETC4	PTM4 compare match interrupt enable					
	D0	ETU4	PTM4 underflow interrupt enable					
00FF26	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag					
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag					
	D3	FTM32	Clock timer 32 Hz interrupt factor flag					
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag					
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					
00FF27	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	FSERR1	Serial I/F 1 (error) interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D4	FSREC1	Serial I/F 1 (receiving) interrupt factor flag					
	D3	FSTRA1	Serial I/F 1 (transmitting) interrupt factor flag					
	D2	FSERR0	Serial I/F 0 (error) interrupt factor flag					
	D1	FSREC0	Serial I/F 0 (receiving) interrupt factor flag					
	D0	FSTRA0	Serial I/F 0 (transmitting) interrupt factor flag					
00FF28	D7	FK07	K07 interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D6	FK06	K06 interrupt factor flag					
	D5	FK05	K05 interrupt factor flag					
	D4	FK04	K04 interrupt factor flag					
	D3	FK03	K03 interrupt factor flag					
	D2	FK02	K02 interrupt factor flag					
	D1	FK01	K01 interrupt factor flag					
	D0	FK00	K00 interrupt factor flag					

Table 5.14.6.1(c) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF29	D7	FTC3	PTM3 compare match interrupt factor flag	(R)	(R)			
	D6	FTU3	PTM3 underflow interrupt factor flag	Interrupt	No interrupt			
	D5	FTC2	PTM2 compare match interrupt factor flag	factor is	factor is			
	D4	FTU2	PTM2 underflow interrupt factor flag	generated	generated			
	D3	FTC1	PTM1 compare match interrupt factor flag			0	R/W	
	D2	FTU1	PTM1 underflow interrupt factor flag	(W)	(W)			
	D1	FTC0	PTM0 compare match interrupt factor flag	Reset	No operation			
	D0	FTU0	PTM0 underflow interrupt factor flag					
00FF2E	D7	FTC7	PTM7 compare match interrupt factor flag	(R)	(R)			
	D6	FTU7	PTM7 underflow interrupt factor flag	Interrupt	No interrupt			
	D5	FTC6	PTM6 compare match interrupt factor flag	factor is	factor is			
	D4	FTU6	PTM6 underflow interrupt factor flag	generated	generated			
	D3	FTC5	PTM5 compare match interrupt factor flag			0	R/W	
	D2	FTU5	PTM5 underflow interrupt factor flag	(W)	(W)			
	D1	FTC4	PTM4 compare match interrupt factor flag	Reset	No operation			
	D0	FTU4	PTM4 underflow interrupt factor flag					

Refer to the explanations on the respective peripheral circuits for the setting content and control method for each bit.

5.14.7 Programming notes

(1) When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

(2) Beware. If the interrupt flags (I0 and I1) have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

(3) An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the front portion of an exception processing routine must be described within the common area (000000H–007FFFH).

(4) Do not execute the SLP instruction for 2 msec after a $\overline{\text{NMI}}$ interrupt has occurred (when f_{OSC1} is 32.768 kHz).

6 FLASH EEPROM

The S1C8F626 has a built-in Flash EEPROM and supports ROM programming (erase / program / verify) on the target board with the S1C8F626 mounted.
Table 6.1 shows the Flash EEPROM specifications.

Table 6.1 Flash EEPROM specifications

Minimum erase unit	4K bytes
Minimum programming unit	1 byte
Programming count	10000 times (Typ.)*1
Data bit status after erasing	1
Program voltage range	V_{DD} = 2.7 to 3.6 V (VDC must be set to "1")
Security function	Programming/erasing protection, On Board Writer read protection*2

*1 The programming count assumes that "erasing + programming" or "programming only" is one count and the programmed data is guaranteed to be retained for 10 years.
*2 This protection can be set by the On Board Writer only.

Refer to Chapter 9, "ELECTRICAL CHARACTERISTICS", for other Flash EEPROM characteristics.

There are two ROM programming methods available, ROM programming with the On Board Writer (product name: S5U1C88000W3 / S5U1C88000W4) and self-programming controlled by the user program.

* This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

6.1 ROM Programming with On Board Writer

By connecting the target board to the On Board Writer using the 16-pin target-board connector as shown in Figure 6.1.1, ROM programming for the S1C8F626 can be controlled from the PC. During ROM programming, the S1C8F626 runs with the clock supplied from the On Board Writer. Consequently, the ROM programming function does not affect the OSC1 / OSC3 oscillation frequencies for normal operation.
The other terminals that are not connected to the On Board Writer retain the initial status set at initial reset.
Refer to Appendix C, "PROM Programming", for how to program the ROM using the On Board Writer.

Notes:
- *Be sure to leave the $\overline{DMOD}$, DTXD, DRXD and DCLK pins open in normal operation. Particularly, make sure that the $\overline{DMOD}$ pin is not pulled down to low from outside the IC, although the pin is pulled up with the internal resistor.*
- *The OSC1 and OSC3 oscillation circuits must be configured to enable oscillation when programming the Flash EEPROM using the On Board Writer.*

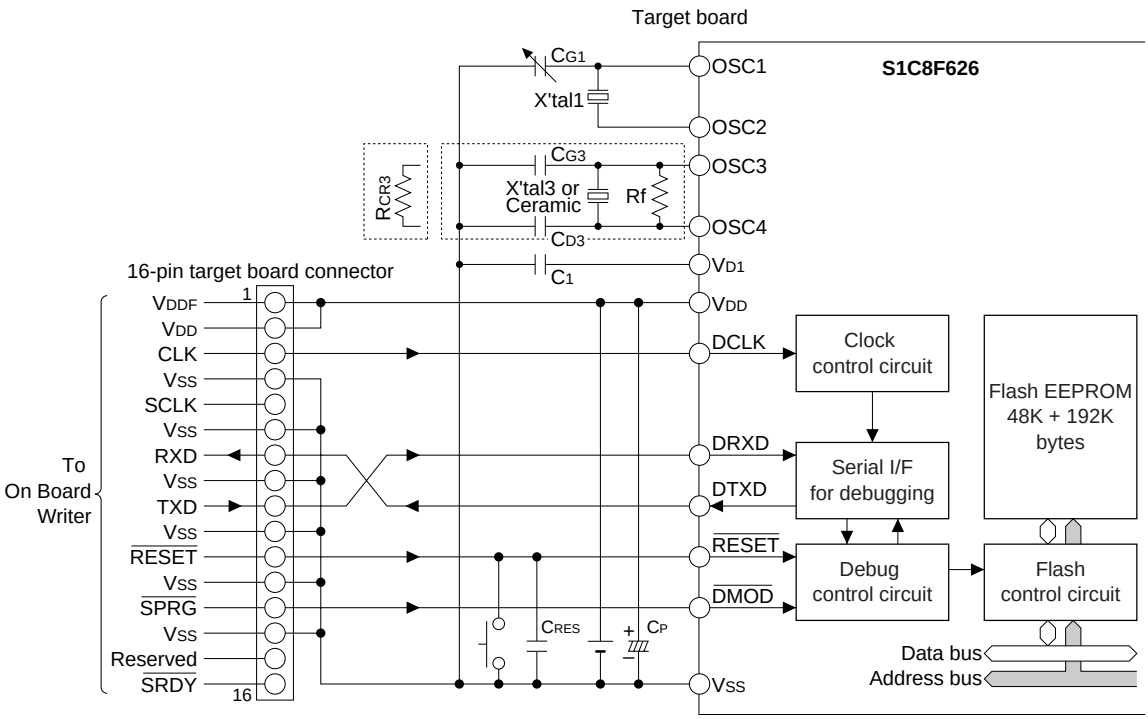


Fig. 6.1.1 ROM programming control circuit and connection example using 16-pin connector

6.2 ROM Programming from User Program

The S1C8F626 has a self-programming function that allows the user program being executed to erase and program the Flash EEPROM while the S1C8F626 is running on the target board.
For the S1C8F626, an object file that includes the functional routines for self-programming is provided as the self-programming package (S5U1C8F626Y4100).
By linking this object with the user application program, a self-programming function can be implemented easily. For details, refer to the manual supplied with the self-programming package.

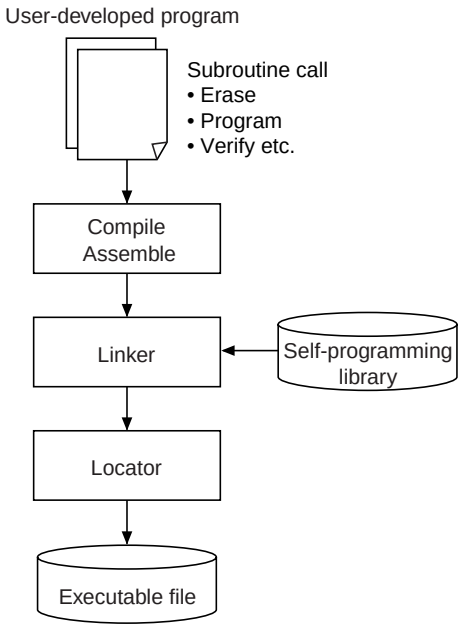


Fig. 6.2.1 Self-programming implement procedure

7 SUMMARY OF NOTES

7.1 Notes for Low Current Consumption

The S1C8F626 can turn circuits, which consume a large amount of power, ON or OFF by control registers.
You can reduce power consumption by creating a program that operates the minimum necessary circuits using these control registers.

Next, which circuit systems' operation can be controlled and their control registers (instructions) are explained. You should refer to these when programming.

See Chapter 9, "ELECTRICAL CHARACTERISTICS" for the current consumption.

Refer to "Programming notes" in each peripheral section for precautions of each peripheral circuit.

Table 7.1.1 Circuit systems and control registers

Circuit type	Control register (Instruction)	Status at time of initial resetting
CPU	HALT and SLP instructions	Operation status
Oscillation circuit	CLKCHG, SOSC3	OSC3 clock (CLKCHG = "1") OSC3 oscillation ON (SOSC3 = "1")
Power voltage booster	DBON	OFF status (DBON = "0")
LCD driver	LCDC0, LCDC1	Drive OFF (LCDC0 = LCDC1 = "0")
SVD circuit	SVDON	OFF status (SVDON = "0")
Heavy lord protection	HLMOD	OFF status (HLMOD = "0")
Internal logic voltage regulator	VDC	V_{D1} = 1.8 V (VDC = "0")

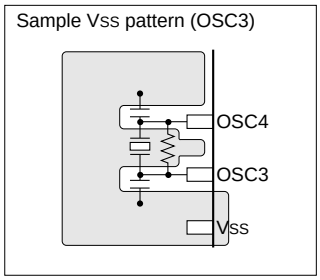
7.2 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.).
  In particular, when a ceramic or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals.
  Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

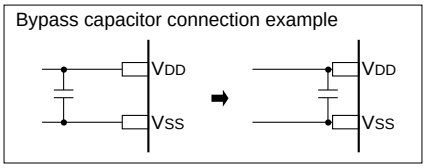
- The power-on reset signal which is input to the $\overline{\text{RESET}}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor of the $\overline{\text{RESET}}$ terminal is used, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{\text{RESET}}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD and VSS terminal with patterns as short and large as possible.

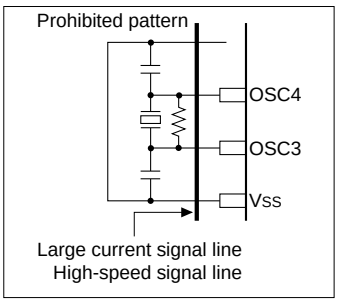
  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the VD1, VD2, VC1, VC2, VC3, VC4 and VC5 terminals, such as capacitors and resistors, should be connected in the shortest line.
  In particular, the VC1, VC2, VC3, VC4 and VC5 voltages affect the display quality.

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change electrical characteristics. It may cause the IC to malfunction or the nonvolatile memory data to be erased. When developing products, consider the following precautions to prevent malfunctions caused by visible radiation.

  (1) Design the product and bond the IC on the board so that it is shielded from visible radiation in actual use.

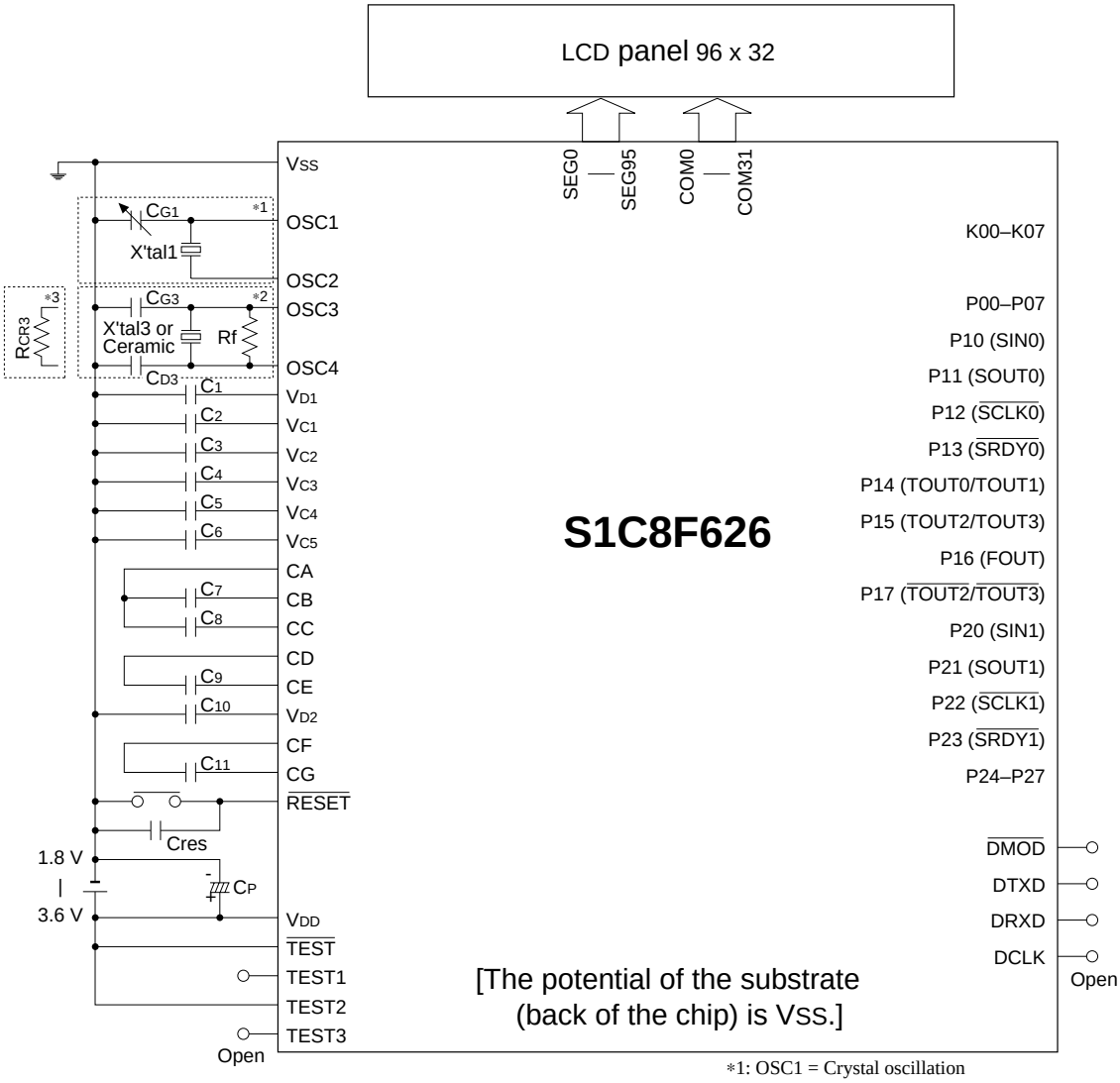
  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) Shield not only the face of the IC but the back and side as well.

  (4) After the shielded package has been opened, the IC chip should be bonded on the board within one week. If the IC chip must be stored after the package has been opened, be sure to shield the IC from visible radiation.

  (5) If there is a possibility that heat stress exceeding the reflow soldering condition is applied to the IC in the bonding process, perform enough evaluation of data stored in the nonvolatile memory before the product is shipped.

8 BASIC EXTERNAL WIRING DIAGRAM



*1: OSC1 = Crystal oscillation

*2: OSC3 = Crystal or Ceramic oscillation

*3: OSC3 = CR oscillation

Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz
C_{G1}	Trimmer capacitor	0–25 pF
X'tal3	Crystal oscillator	1–8 MHz
Ceramic	Ceramic oscillator	1–8 MHz
Rf	Feedback resistor	1 MΩ
C_{G3}	Gate capacitor	15 pF (Crystal oscillation)
		30 pF (Ceramic oscillation)
C_{D3}	Drain capacitor	15 pF (Crystal oscillation)
		30 pF (Ceramic oscillation)
R_{CR3}	Resistor for CR oscillation	30 kΩ

Symbol	Name	Recommended value
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7–C_9	Booster capacitors	0.1 µF
C_{10}	Capacitor between V_{SS} and V_{D2}	0.1 µF
C_{11}	Booster capacitor	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF

Note: The above table is simply an example, and is not guaranteed to work.

9 ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Rating

(V_{SS} = 0 V)

Item	Symbol	Condition	Rated value	Unit	Note
Power voltage	V_{DD}		-0.3 to +4.0	V	
Liquid crystal power voltage	V_{C5}		-0.3 to +6.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	1
Operating temperature	Topr		-20 to +70	°C	
Storage temperature	Tstg		-65 to +150	°C	
Soldering temperature / time	Tsol		260°C, 10 sec (lead section)	–	

Note) 1 In case of plastic package.

9.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage	V_{DD}	Normal operation mode	1.8		3.6	V	
		Flash programming mode	2.7		3.6	V	
Operating frequency	f_{OSC1}		30	32.768	200	kHz	
	f_{OSC3}	CR oscillation	0.03		2.2	MHz	
		Crystal/ceramic oscillation	0.03		8.2	MHz	
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{C1} and V_{SS}	C_2			0.1		µF	1
Capacitor between V_{C2} and V_{SS}	C_3			0.1		µF	1
Capacitor between V_{C3} and V_{SS}	C_4			0.1		µF	1
Capacitor between V_{C4} and V_{SS}	C_5			0.1		µF	1
Capacitor between V_{C5} and V_{SS}	C_6			0.1		µF	1
Capacitor between CA and CB	C_7			0.1		µF	1
Capacitor between CA and CC	C_8			0.1		µF	1
Capacitor between CD and CE	C_9			0.1		µF	1
Capacitor between V_{D2} and V_{SS}	C_{10}			0.1		µF	1
Capacitor between CF and CG	C_{11}			0.1		µF	1

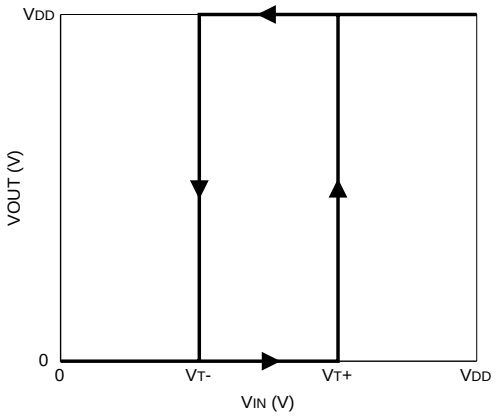
Note) 1 When LCD drive power is not used, the capacitor is not necessary.
In this case, leave the V_{C1} to V_{C5} and CA to CG terminals open.

9.3 DC Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = -20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage	V_{IH}	Kxx, Pxx	0.8V_{DD}		V_{DD}	V	
Low level input voltage	V_{IL}	Kxx, Pxx	0		0.2V_{DD}	V	
High level schmitt input voltage (1)	V_{T1+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage (1)	V_{T1-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
High level schmitt input voltage (2)	V_{T2+}	Kxx	0.5V_{DD}		0.9V_{DD}	V	1
Low level schmitt input voltage (2)	V_{T2-}	Kxx	0.1V_{DD}		0.5V_{DD}	V	1
High level output current	I_{OH}	Pxx, V_{OH} = 0.9 V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, V_{OL} = 0.1 V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$	-1		1	µA	
Output leak current	I_{LO}	Pxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$	100		500	kΩ	
Input terminal capacitance	C_{IN}	Kxx, Pxx V_{IN} = 0 V, f = 1 MHz, Ta = 25°C			15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1 V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1 V	5			µA	

Note) 1 When CMOS Schmitt level is selected.



9.4 Analog Circuit Characteristics

■ LCD drive circuit

The typical values in the following LCD driver characteristics varies depending on the panel load (panel size, number of display pixels and display contents), so evaluate them by connecting to the actually used LCD panel. Refer to Section 9.8, "Characteristics Curves" for the load characteristic.

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, C_1–C_{11} = 0.1 µF,
When a checker pattern is displayed, No panel load

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C1}	*1		0.18•V_{C5}		0.22•V_{C5}	V	
	V_{C2}	*2		0.39•V_{C5}		0.43•V_{C5}	V	
	V_{C3}	*3		0.59•V_{C5}		0.63•V_{C5}	V	
	V_{C4}	*4		0.79•V_{C5}		0.83•V_{C5}	V	
	V_{C5}	*5	LCx = 0H		4.20		V	
			LCx = 1H		4.30		V	
			LCx = 2H		4.40		V	
			LCx = 3H		4.50		V	
			LCx = 4H		4.60		V	
			LCx = 5H		4.70		V	
			LCx = 6H		4.80		V	
			LCx = 7H	Typ×0.94	4.90	Typ×1.06	V	
			LCx = 8H		5.00		V	
			LCx = 9H		5.10		V	
			LCx = AH		5.20		V	
			LCx = BH		5.30		V	
			LCx = CH		5.40		V	
			LCx = DH		5.50		V	
			LCx = EH		5.60		V	
			LCx = FH		5.70		V	

*1 Connects 1 MΩ load resistor between V_{SS} and V_{C1}.
*2 Connects 1 MΩ load resistor between V_{SS} and V_{C2}.
*3 Connects 1 MΩ load resistor between V_{SS} and V_{C3}.
*4 Connects 1 MΩ load resistor between V_{SS} and V_{C4}.
*5 Connects 1 MΩ load resistor between V_{SS} and V_{C5}.

■ SVD circuit

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	SVDS0–3 = "0"		–		V	
		SVDS0–3 = "1"		–		V	
		SVDS0–3 = "2"		–		V	
		SVDS0–3 = "3"		1.8		V	
		SVDS0–3 = "4"		1.85		V	
		SVDS0–3 = "5"		1.9		V	
		SVDS0–3 = "6"		1.95		V	
		SVDS0–3 = "7"		2.0		V	
		SVDS0–3 = "8"		2.05		V	
		SVDS0–3 = "9"	Typ×0.91	2.1	Typ×1.09	V	
		SVDS0–3 = "10"		2.2		V	
		SVDS0–3 = "11"		2.3		V	
		SVDS0–3 = "12"		2.4		V	
		SVDS0–3 = "13"		2.5		V	
		SVDS0–3 = "14"		2.6		V	
		SVDS0–3 = "15"		2.7		V	
SVD circuit response time	t_{SVD}				500	µs	

■ Flash EEPROM

Unless otherwise specified: V_{DD} = 2.7 to 3.6 V (VDC = "1"), V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Erase time	t_{SE}	When erasing 4K bytes			25	ms	1
Programming time	t_{BP}	When programming 1 byte			20	µs	1
Programming count	C_{FEP}		1000	10000		times	2

Note) 1 Data transfer and data verification are included and erase/program start control time is not included.
2 The programming count assumes that "erasing + programming" or "programming only" is one count and the programmed data is guaranteed to be retained for 10 years.

9.5 Power Current Consumption

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, C_1–C_{11} = 0.1 µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Current consumption in SLEEP mode	I_{SLP}	OSC1 = OFF, OSC3 = OFF, VDC = "0"		1	2.5	µA	
Current consumption in HALT mode	I_{HALT1}	OSC1 = 32kHz Crystal, OSC3 = OFF, VDC = "0"		2.5	5	µA	
	I_{HALT2}	OSC1 = 32kHz Crystal, OSC3 = 8MHz Ceramic, VDC = "0"		200	400	µA	
	I_{HALT3}	OSC1 = 32kHz Crystal, OSC3 = 2MHz CR, VDC = "0"		250	500	µA	
Current consumption during execution	I_{EXE1}	OSC1 = 32kHz Crystal, OSC3 = OFF, VDC = "0", CPU = OSC1		10	17	µA	
	I_{EXE2}	OSC1 = 32kHz Crystal, OSC3 = 8MHz Ceramic, VDC = "0", CPU = OSC3		1800	2700	µA	
	I_{EXE3}	OSC1 = 32kHz Crystal, OSC3 = 2MHz CR, VDC = "0", CPU = OSC3		700	1400	µA	
	I_{EXE11}	OSC1 = 32kHz Crystal, OSC3 = OFF, VDC = "1", CPU = OSC1		25	38	µA	
	I_{EXE21}	OSC1 = 32kHz Crystal, OSC3 = 8MHz Ceramic, VDC = "1", CPU = OSC3		3500	5000	µA	
	I_{EXE31}	OSC1 = 32kHz Crystal, OSC3 = 2MHz CR, VDC = "1", CPU = OSC3		1400	2800	µA	
Current consumption during execution in heavy load protection mode	I_{EXE1H}	OSC1 = 32kHz Crystal, OSC3 = OFF, VDC = "0", HLMOD = H		15	27	µA	
LCD circuit current	I_{LCD1}	LCDCx = All on, LCx = FH, f_{OSC1} = 32.768kHz, V_{DD} = 2.5 to 3.6V		5	10	µA	1
LCD circuit current in heavy load protection mode	I_{LCD1H}	LCDCx = All on, LCx = FH, f_{OSC1} = 32.768kHz, V_{DD} = 2.5 to 3.6V, HLMOD = H		18	30	µA	2
LCD circuit current when the power voltage booster is active	I_{LCD2}	LCDCx = All on, LCx = FH, f_{OSC1} = 32.768kHz, DBON = H, V_{DD} = 1.8 to 2.5V		10	20	µA	3
LCD circuit current in heavy load protection mode when the power voltage booster is active	I_{LCD2H}	LCDCx = All on, LCx = FH, f_{OSC1} = 32.768kHz, DBON = H, V_{DD} = 1.8 to 2.5V, HLMOD = H		40	60	µA	4
SVD circuit current	I_{SVD}	V_{DD} = 3.6V		5	10	µA	5
Flash EEPROM erasing current	I_{FERS}	When the CPU runs with 8MHz clock, VDC = "1"		4	8	mA	6
Flash EEPROM programming current	I_{FPRG}	When the CPU runs with 8MHz clock, VDC = "1"		4	8	mA	7

Note) 1 This value is added to the current consumption in HALT mode or current consumption during execution when the LCD circuit is active. Current consumption increases according to the display contents and panel load.
2 This value is added to the current consumption during execution in heavy load protection mode when the LCD circuit is active. Current consumption increases according to the display contents and panel load.
3 This value is added to the current consumption in HALT mode or current consumption during execution when the power voltage booster and the LCD circuit are active. Current consumption increases according to the display contents and panel load.
4 This value is added to the current consumption during execution in heavy load protection mode when the power voltage booster and the LCD circuit are active. Current consumption increases according to the display contents and panel load.
5 This value is added to the current consumption during execution or current consumption during execution in heavy load protection mode when the SVD circuit is active.
6 This value is added to the current consumption during execution when the Flash EEPROM is being erased in self-programming mode. Note that this is not the current value when the On Board Writer is connected.
7 This value is added to the current consumption during execution when the Flash EEPROM is being programmed in self-programming mode. Note that this is not the current value when the On Board Writer is connected.

9.6 AC Characteristics

■ Operating range

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = -20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating frequency	f_{OSC1}	V_{DD} = 1.8 to 3.6 V	30	32.768	200	kHz	
	f_{OSC3}		0.03		8.2	MHz	
Instruction execution time (during operation with OSC1 clock)	tcy	1-cycle instruction	10	61	67	µs	
		2-cycle instruction	20	122	133	µs	
		3-cycle instruction	30	183	200	µs	
		4-cycle instruction	40	244	267	µs	
		5-cycle instruction	50	305	333	µs	
		6-cycle instruction	60	366	400	µs	
Instruction execution time (during operation with OSC3 clock)	tcy	1-cycle instruction	0.24		66.7	µs	
		2-cycle instruction	0.49		133.3	µs	
		3-cycle instruction	0.73		200.0	µs	
		4-cycle instruction	0.98		266.7	µs	
		5-cycle instruction	1.22		333.3	µs	
		6-cycle instruction	1.46		400.0	µs	

■ Serial interface

• Clock synchronous master mode

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			100	ns	
Receiving data input set-up time	tsms	250			ns	
Receiving data input hold time	tsmh	100			ns	

• Clock synchronous slave mode

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			250	ns	
Receiving data input set-up time	tsss	100			ns	
Receiving data input hold time	tssh	100			ns	

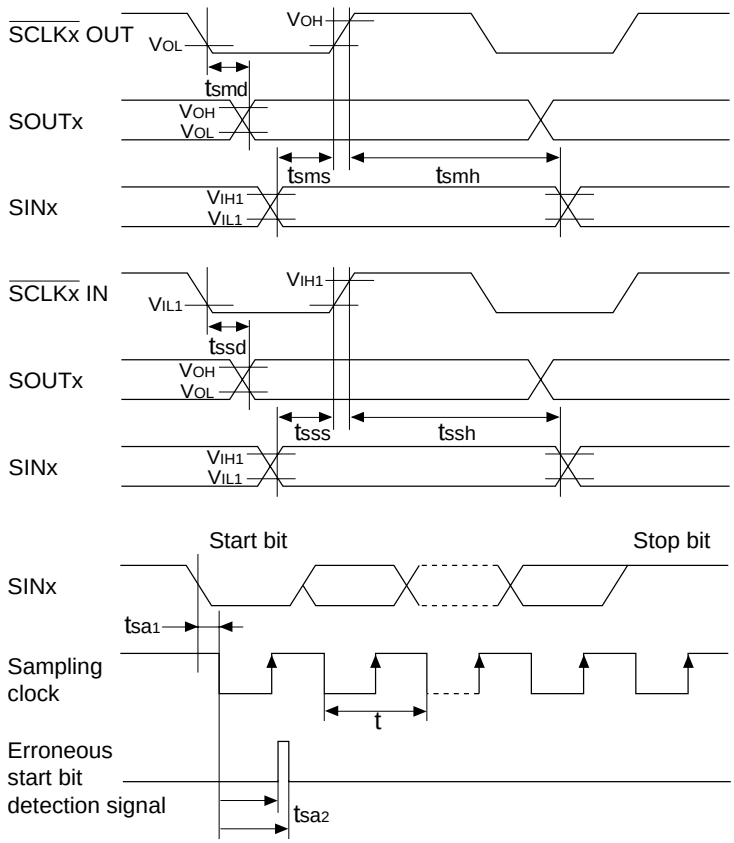
• Asynchronous system

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Start bit detection error time	t_{sa1}	0		t/16	s	1
Erroneous start bit detection range time	t_{sa2}	9t/16		10t/16	s	2

Note) 1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started.
When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)

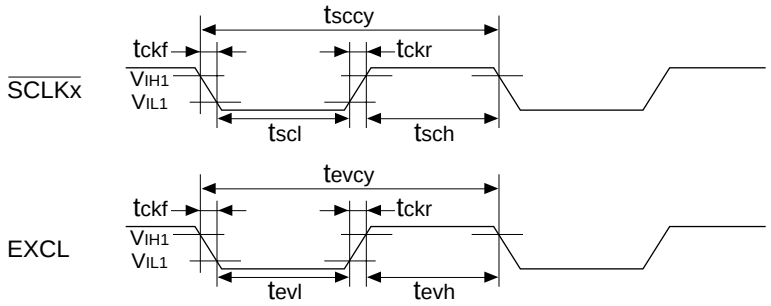


■ Input clock

• $\overline{\text{SCLKx}}$, EXCL input clock

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

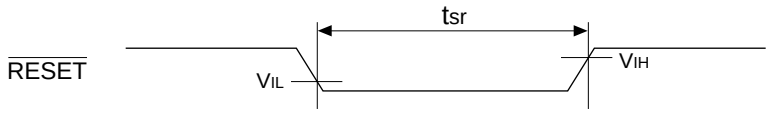
Item		Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{SCLKx}}$ input clock time	Cycle time	tsccy	2			µs	
	"H" pulse width	tsch	1			µs	
	"L" pulse width	tscl	1			µs	
EXCL input clock time (with noise rejector)	Cycle time	tevcy	64/f_{OSC1}			s	
	"H" pulse width	tevh	32/f_{OSC1}			s	
	"L" pulse width	tevl	32/f_{OSC1}			s	
EXCL input clock time (without noise rejector)	Cycle time	tevcy	2			µs	
	"H" pulse width	tevh	1			µs	
	"L" pulse width	tevl	1			µs	
Input clock rising time		tckr			25	ns	
Input clock falling time		tckf			25	ns	



• $\overline{\text{RESET}}$ input clock

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH} = 0.5V_{DD}, V_{IL} = 0.1V_{DD}

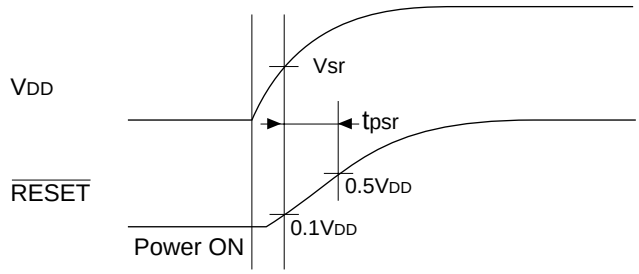
Item	Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{RESET}}$ input time	tsr	100			µs	

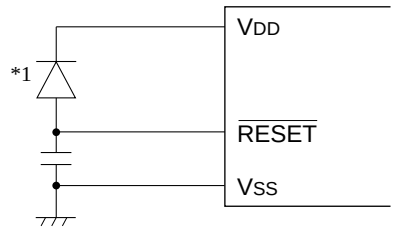


■ Power ON reset using an external capacitor

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Operating power voltage	Vsr	1.8			V	
$\overline{RESET}$ input time	tpsr	10			ms	





*1 Because the potential of the $\overline{RESET}$ terminal not reached V_{DD} level or higher.

9.7 Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator or crystal oscillator is used for OSC3, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance. The oscillation start time is important because it becomes the wait time when OSC3 clock is used. (If OSC3 is used as CPU clock before oscillation stabilizes, the CPU may malfunction.)

■ OSC1 (Crystal)

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C,

Crystal oscillator = C-002RX (R_1 = 30 kΩ (Typ.), C_L + 12.5 pF)*, C_{G1} = 25 pF, C_{D1} = Built-in

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	s	
External gate capacitance	C_{G1}	Including board capacitance	0		25	pF	
Built-in drain capacitance	C_{D1}	In case of the chip		10		pF	
Frequency/IC deviation	∂f/∂IC	V_{DD} = constant	-10		10	ppm	
Frequency/power voltage deviation	∂f/∂V				1	ppm/V	
Frequency adjustment range	∂f/∂C_G	V_{DD} = constant, C_G = 0 to 25 pF	25			ppm	

* C-002RX Made by Seiko Epson

■ OSC3 (Crystal)

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C,

Crystal oscillator = CA-301*, R_F = 1 MΩ, C_{G3} = C_{D3} = 15 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				10	ms	1

* CA-301 Made by Seiko Epson

Note) 1 The crystal oscillation start time changes by the crystal oscillator to be used, C_{G3} and C_{D3}.

■ OSC3 (Ceramic)

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C,

Ceramic oscillator = KBR-4.0MSB/KBR-8.0MSB*, R_F = 1 MΩ, C_{G3} = C_{D3} = 30 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				1	ms	1

* KBR-4.0MSB/KBR-8.0MSB Made by Kyocera

Note) 1 The ceramic oscillation start time changes by the ceramic oscillator to be used, C_{G3} and C_{D3}.

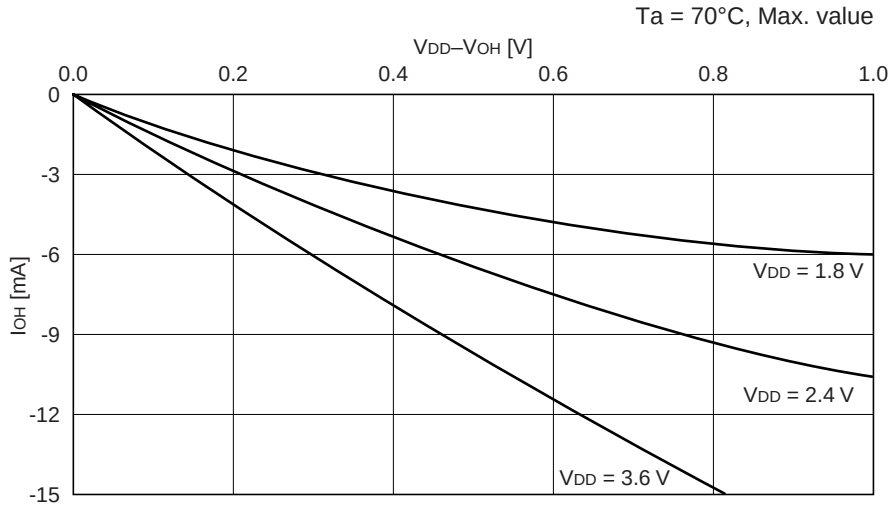
■ OSC3 (CR)

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C

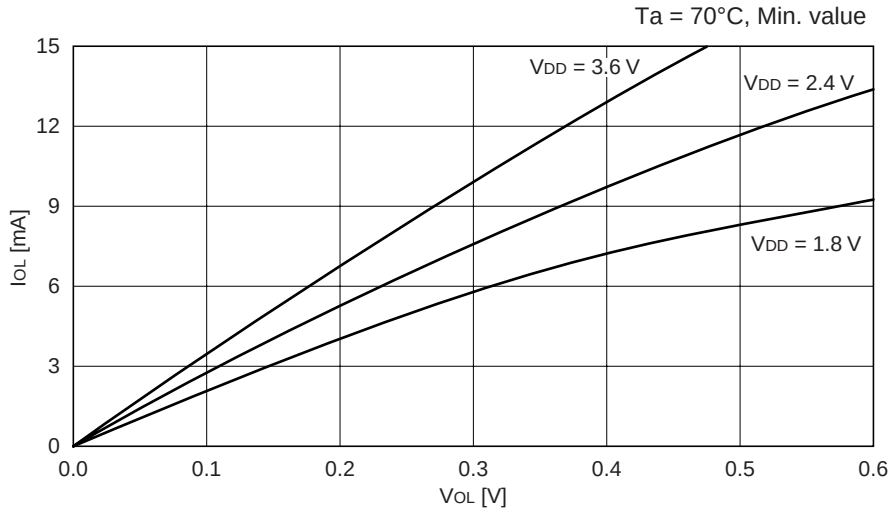
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				100	µs	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

9.8 Characteristics Curves (reference value)

■ High level output current-voltage characteristic



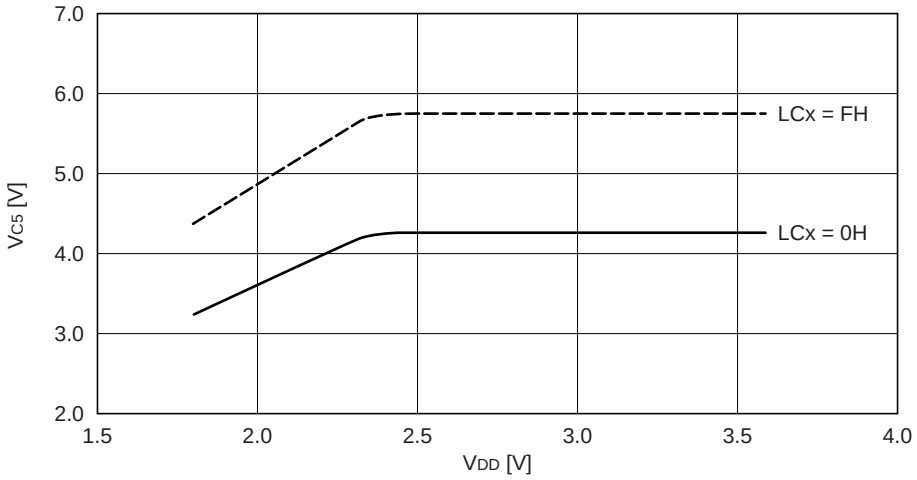
■ Low level output current-voltage characteristic



■ LCD drive voltage-supply voltage characteristic (when the power voltage booster is not used)

Connects 1 MΩ load resistor between V_{SS} and V_{C5}. (no panel load)

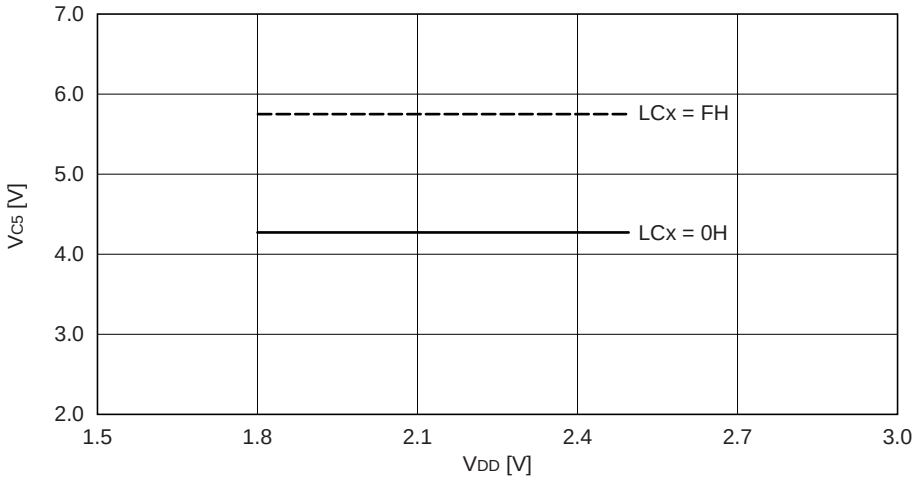
Ta = 25°C, Typ. value



■ LCD drive voltage-supply voltage characteristic (when the power voltage booster is used)

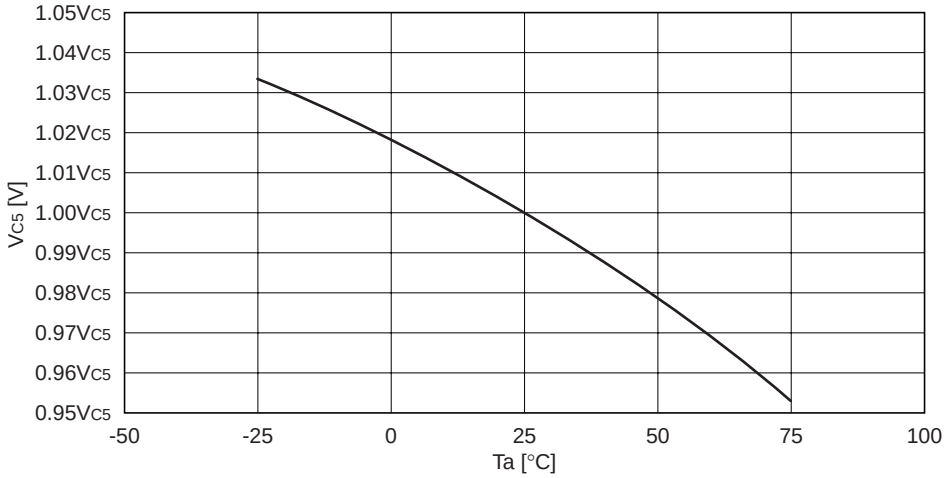
Connects 1 MΩ load resistor between V_{SS} and V_{C5}. (no panel load)

Ta = 25°C, Typ. value



■ LCD drive voltage-ambient temperature characteristic

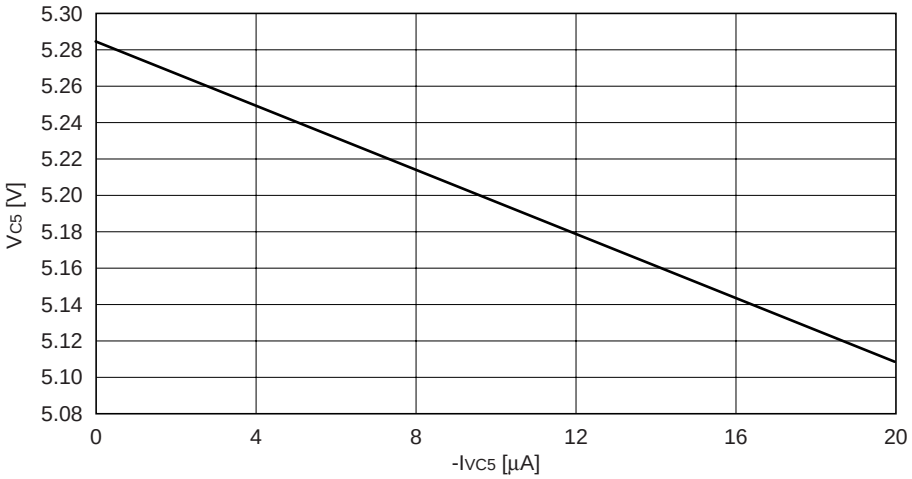
Typ. value



■ LCD drive voltage-load characteristic

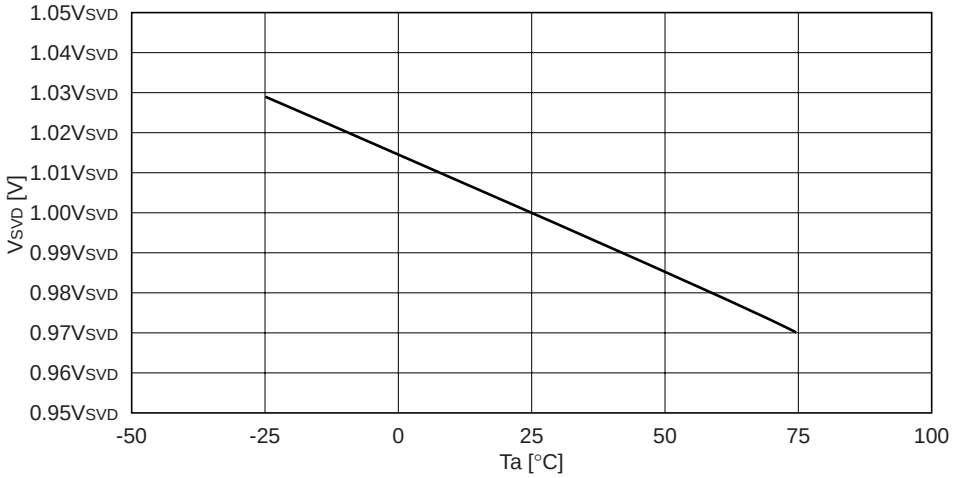
When a load is connected to the V_{C5} terminal only

Ta = 25°C, Typ. value, LCx = 8H

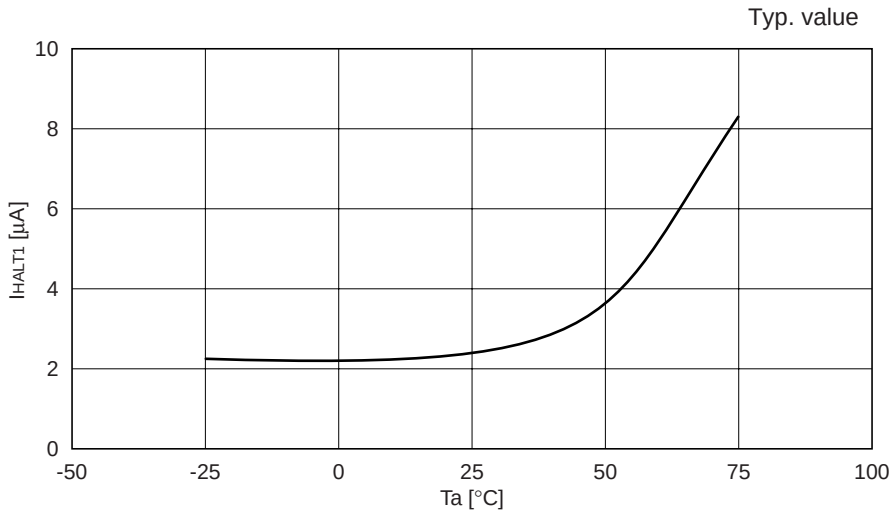


■ SVD voltage-ambient temperature characteristic

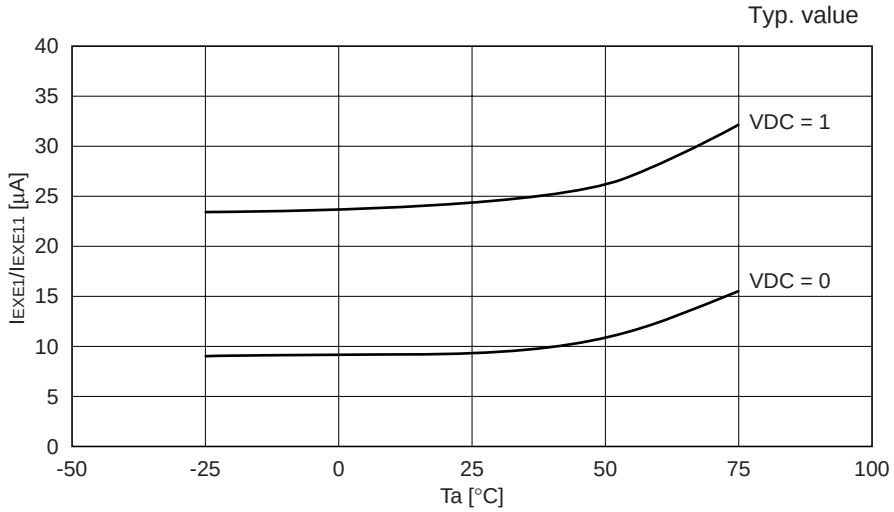
Typ. value, SVDSx = FH



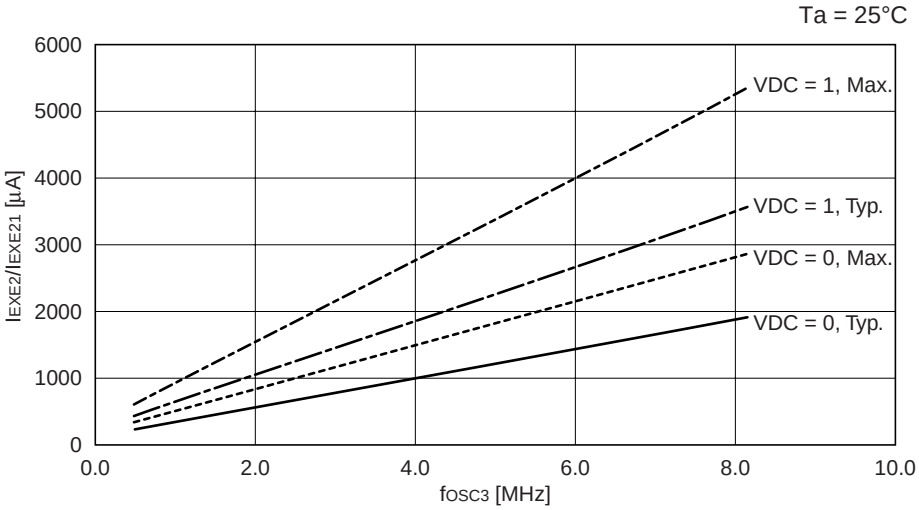
■ **In HALT status current consumption temperature characteristic (During operation with OSC1) <Crystal oscillation, f_{OSC1} = 32.768 kHz>**



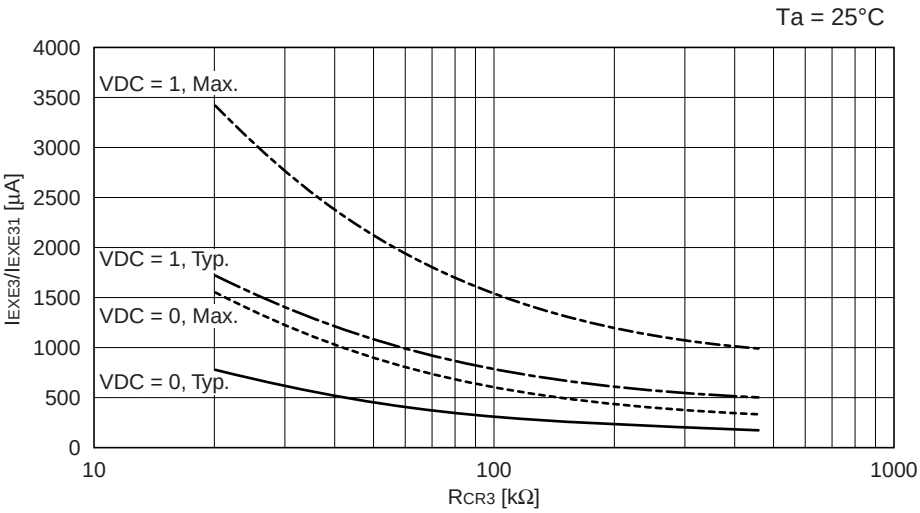
■ **In executed status current consumption temperature characteristic (During operation with OSC1) <Crystal oscillation, f_{OSC1} = 32.768 kHz>**



■ In executed status current consumption frequency characteristic (During operation with OSC3) <Crystal oscillation/Ceramic oscillation>

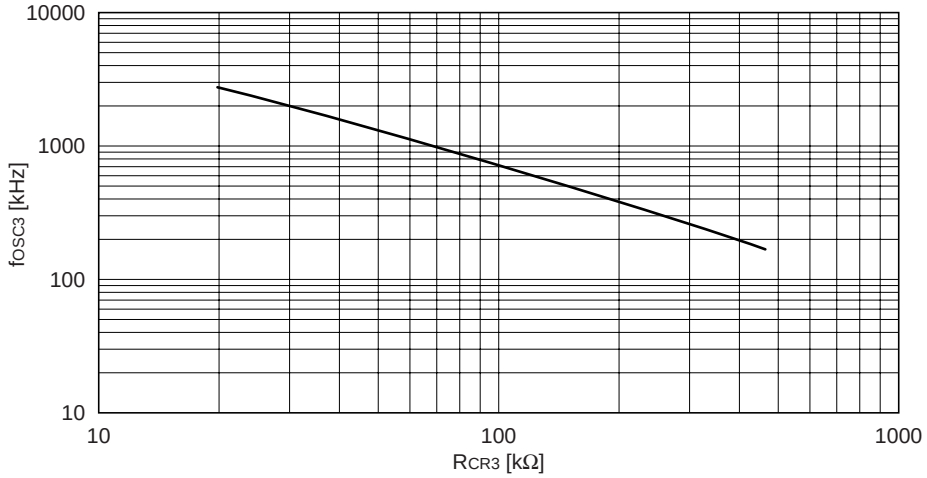


■ In executed status current consumption resistor characteristic (During operation with OSC3) <CR oscillation>



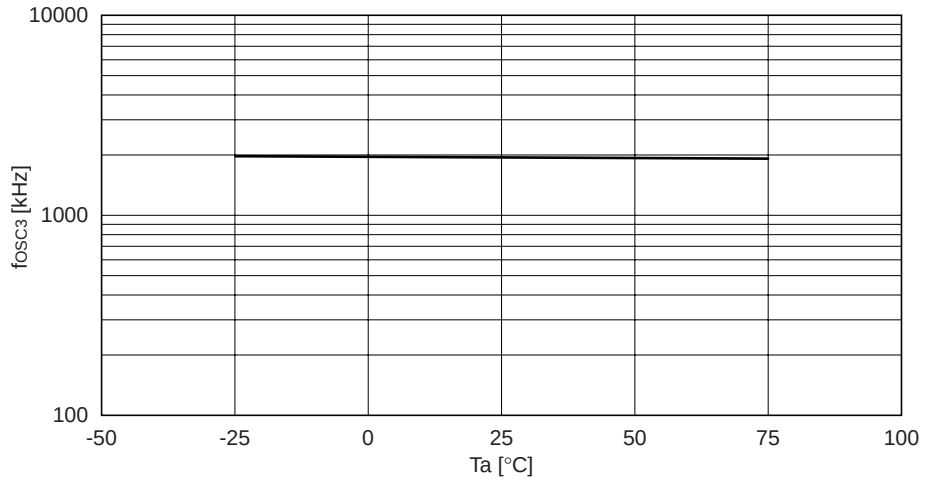
■ Oscillation frequency resistor characteristic (OSC3) <CR oscillation>

Ta = 25°C, Typ. value



■ Oscillation frequency temperature characteristic (OSC3) <CR oscillation>

Typ. value, RCR3 = 30 kΩ

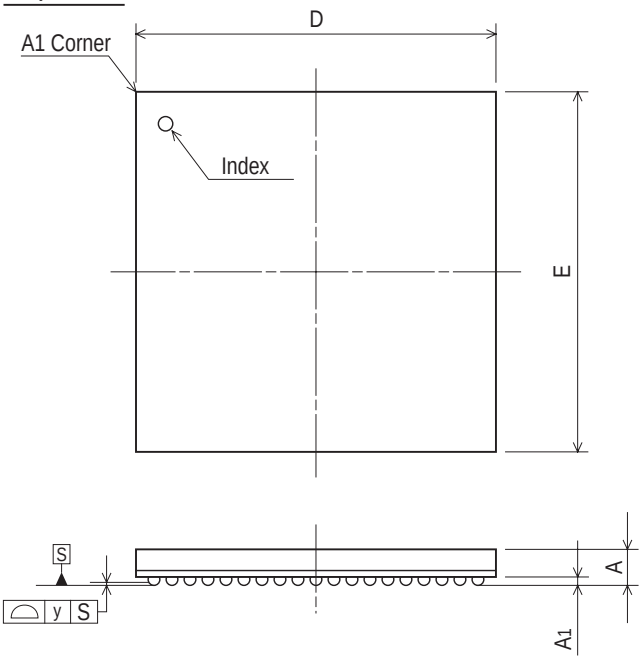


10 PACKAGE

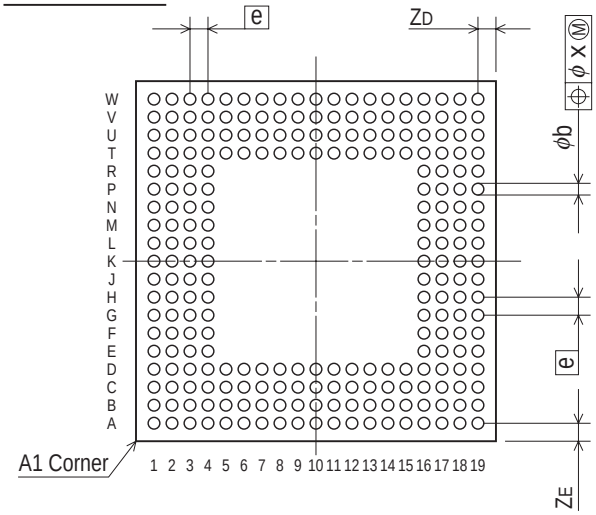
10.1 Plastic Package

VFBGA10H-240pin

Top View



Bottom View

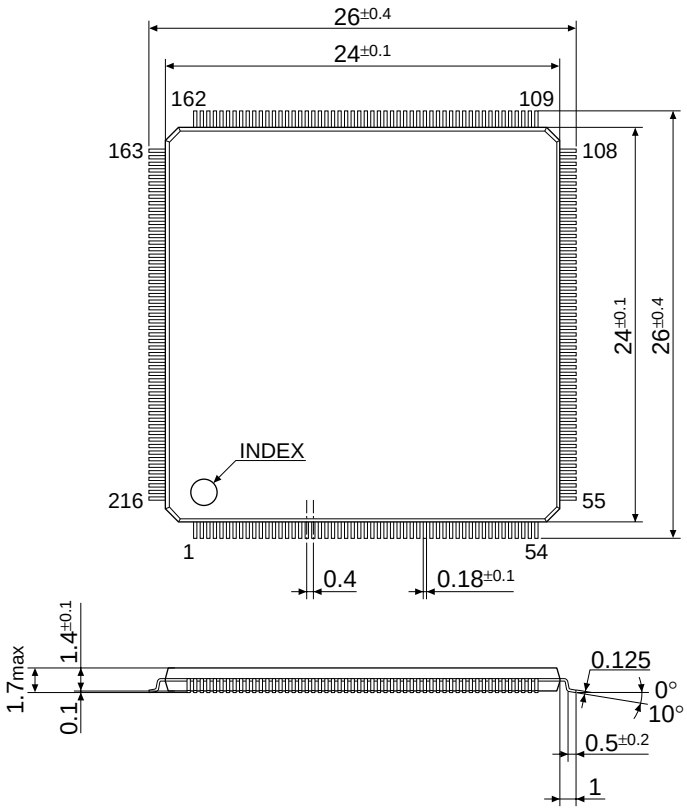


Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	–	10	–
E	–	10	–
A	–	–	1.0
A_1	–	0.23	–
e	–	0.5	–
b	0.26	–	0.36
x	–	–	0.08
y	–	–	0.1
Z_D	–	0.5	–
Z_E	–	0.5	–

1 = 1mm

QFP21-216pin

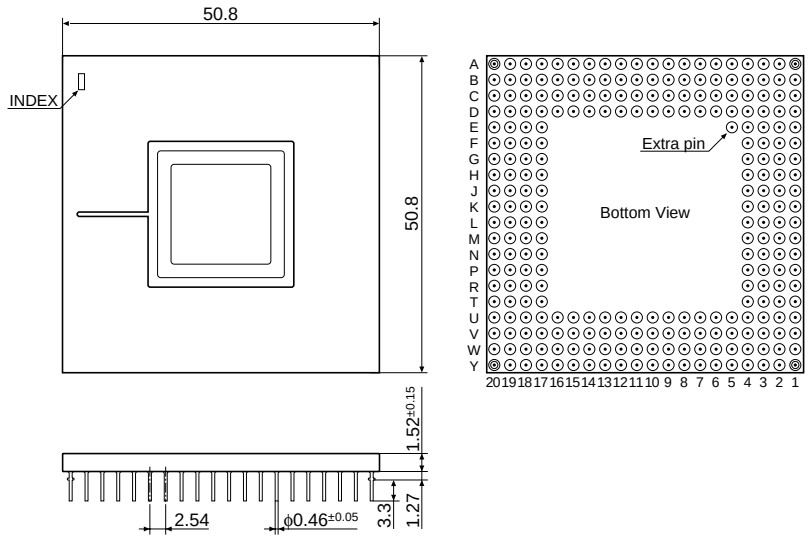
(Unit: mm)



10.2 Ceramic Package for Test Samples

PGA-256pin

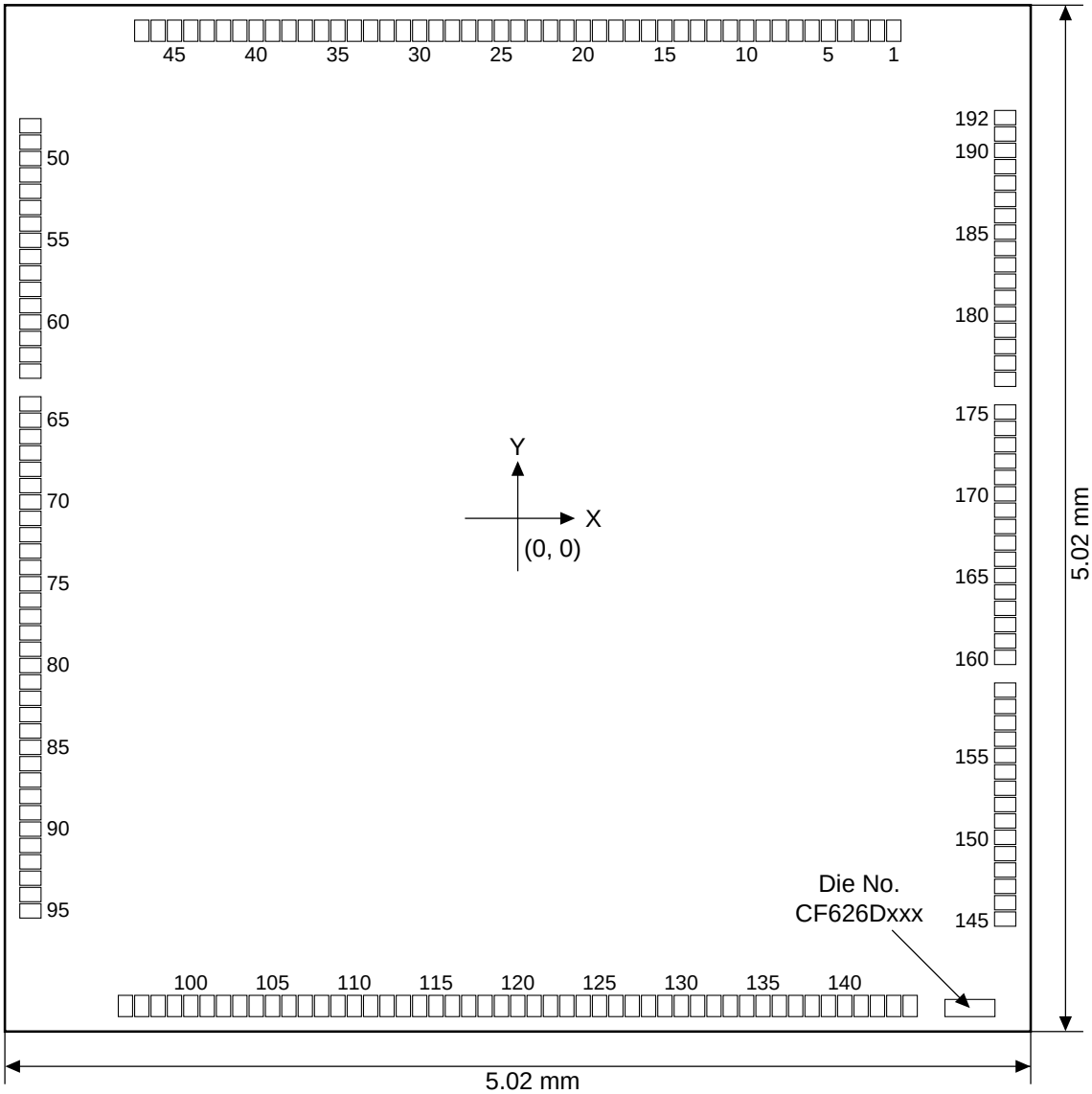
(Unit: mm)



Pin No.		Pin name	Pin No.		Pin name	Pin No.		Pin name	Pin No.		Pin name	Pin No.		Pin name
1	A1	N.C.	53	U1	V_{C4}	105	Y14	P14/TOUT0/TOUT1	157	M20	SEG3	209	A16	SEG40
2	D4	N.C.	54	P4	V_{C3}	106	U12	P13/$\overline{SRDY0}$	158	L17	SEG4	210	D13	SEG41
3	C2	N.C.	55	U2	V_{C2}	107	W14	P12/$\overline{SCLK0}$	159	L20	SEG5	211	B14	SEG42
4	D3	N.C.	56	T3	V_{C1}	108	V12	P11/SOUT0	160	L19	SEG6	212	C13	SEG43
5	B1	N.C.	57	V1	N.C.	109	Y15	P10/SIN0	161	K20	SEG7	213	A15	SEG44
6	E4	N.C.	58	R4	N.C.	110	V13	P07	162	K19	SEG8	214	C12	SEG45
7	D2	N.C.	59	V2	N.C.	111	W15	P06	163	J20	SEG9	215	B13	SEG46
8	E3	N.C.	60	U3	N.C.	112	U13	P05	164	K17	SEG10	216	D12	SEG47
9	C1	SEG81	61	W1	N.C.	113	Y16	P04	165	H20	SEG11	217	A14	SEG48
10	F4	SEG82	62	T4	N.C.	114	V14	P03	166	K18	SEG12	218	B12	SEG49
11	E2	SEG83	63	W2	N.C.	115	W16	P02	167	H19	SEG13	219	A13	SEG50
12	F3	SEG84	64	V3	N.C.	116	V15	P01	168	J19	SEG14	220	C11	SEG51
13	D1	SEG85	65	Y1	N.C.	117	Y17	P00	169	G20	SEG15	221	A12	SEG52
14	G4	SEG86	66	U4	N.C.	118	U14	V_{DD}	170	J17	SEG16	222	D11	SEG53
15	F2	SEG87	67	W3	N.C.	119	W17	V_{SS}	171	G19	SEG17	223	A11	SEG54
16	G3	SEG88	68	V4	N.C.	120	V16	N.C.	172	J18	SEG18	224	B11	SEG55
17	E1	SEG89	69	Y2	N.C.	121	Y18	N.C.	173	F20	SEG19	225	A10	SEG56
18	H4	SEG90	70	U5	N.C.	122	U15	N.C.	174	H18	SEG20	226	B10	SEG57
19	G2	SEG91	71	W4	N.C.	123	W18	N.C.	175	F19	SEG21	227	A9	SEG58
20	H3	SEG92	72	V5	N.C.	124	V17	N.C.	176	H17	SEG22	228	D10	SEG59
21	F1	SEG93	73	Y3	V_{DD}	125	Y19	N.C.	177	E20	SEG23	229	A8	SEG60
22	J3	SEG94	74	U6	OSC3	126	U16	N.C.	178	G18	SEG24	230	C10	SEG61
23	H2	SEG95	75	W5	OSC4	127	W19	N.C.	179	E19	SEG25	231	B8	SEG62
24	J4	COM31	76	V6	V_{SS}	128	V18	N.C.	180	F18	SEG26	232	B9	SEG63
25	G1	COM30	77	Y4	V_{D1}	129	Y20	N.C.	181	D20	SEG27	233	A7	SEG64
26	J2	COM29	78	U7	OSC1	130	U17	N.C.	182	G17	SEG28	234	D9	SEG65
27	H1	COM28	79	W6	OSC2	131	V19	N.C.	183	D19	SEG29	235	B7	SEG66
28	K3	COM27	80	V7	$\overline{TEST}$	132	U18	N.C.	184	E18	SEG30	236	C9	SEG67
29	J1	COM26	81	Y5	$\overline{RESET}$	133	W20	N.C.	185	C20	SEG31	237	A6	SEG68
30	K4	COM25	82	U8	$\overline{DMOD}$	134	T17	N.C.	186	F17	N.C.	238	C8	SEG69
31	K1	COM24	83	W7	DRXD	135	U19	N.C.	187	C19	N.C.	239	B6	SEG70
32	K2	COM23	84	V8	DTXD	136	T18	N.C.	188	D18	N.C.	240	D8	SEG71
33	L1	COM22	85	Y6	DCLK	137	V20	N.C.	189	B20	N.C.	241	A5	SEG72
34	L2	COM21	86	V9	K07/EXCL3	138	R17	COM0	190	E17	N.C.	242	C7	SEG73
35	M1	COM20	87	W8	K06/EXCL2	139	T19	COM1	191	B19	N.C.	243	B5	SEG74
36	L4	COM19	88	U9	K05/EXCL1	140	R18	COM2	192	C18	N.C.	244	C6	SEG75
37	N1	COM18	89	Y7	K04/EXCL0	141	U20	COM3	193	A20	N.C.	245	A4	SEG76
38	L3	COM17	90	W9	K03	142	P17	COM4	194	D17	N.C.	246	D7	SEG77
39	N2	COM16	91	Y8	K02	143	R19	COM5	195	B18	N.C.	247	B4	SEG78
40	M2	V_{SS}	92	V10	K01	144	P18	COM6	196	C17	N.C.	248	C5	SEG79
41	P1	TEST1	93	Y9	K00	145	T20	COM7	197	A19	N.C.	249	A3	SEG80
42	M4	TEST2	94	U10	P27	146	N17	COM8	198	D16	N.C.	250	D6	N.C.
43	P2	TEST3	95	Y10	P26	147	P19	COM9	199	B17	N.C.	251	B3	N.C.
44	M3	V_{D2}	96	W10	P25	148	N18	COM10	200	C16	N.C.	252	C4	N.C.
45	R1	CG	97	Y11	P24	149	R20	COM11	201	A18	SEG32	253	A2	N.C.
46	N3	CF	98	W11	P23/$\overline{SRDY1}$	150	M18	COM12	202	D15	SEG33	254	D5	N.C.
47	R2	CE	99	Y12	P22/$\overline{SCLK1}$	151	N19	COM13	203	B16	SEG34	255	B2	N.C.
48	N4	CD	100	U11	P21/SOUT1	152	M17	COM14	204	C15	SEG35	256	C3	N.C.
49	T1	CC	101	Y13	P20/SIN1	153	P20	COM15	205	A17	SEG36	–	–	–
50	P3	CB	102	V11	P17/$\overline{TOUT2}$/$\overline{TOUT3}$	154	M19	SEG0	206	D14	SEG37	–	–	–
51	T2	CA	103	W13	P16/FOUT	155	N20	SEG1	207	B15	SEG38	–	–	–
52	R3	V_{C5}	104	W12	P15/TOUT2/TOUT3	156	L18	SEG2	208	C14	SEG39	–	–	–

11 PAD LAYOUT

11.1 Diagram of Pad Layout



Pad opening) Pad No. 1–47, 96–144 : 70 × 104 µm
Pad No. 48–95, 145–192:104 × 70 µm
Chip thickness) 400 µm

11.2 Pad Coordinates

(Unit: mm)

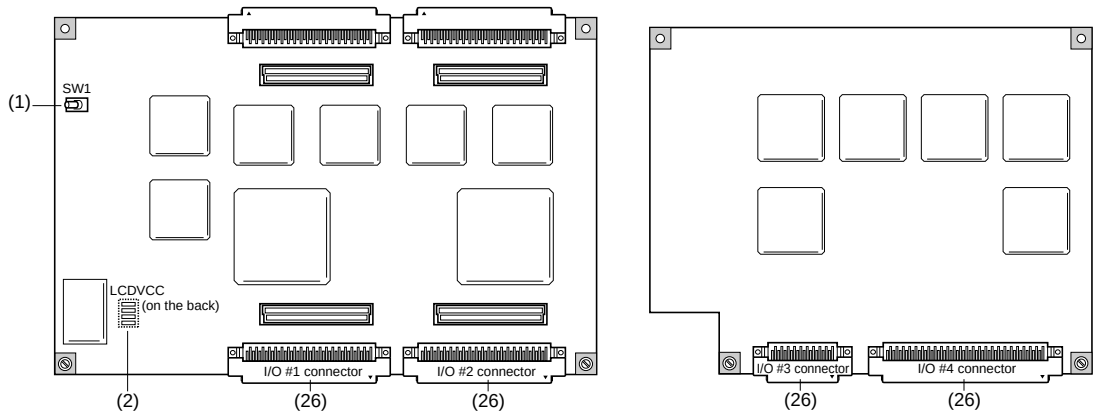
Pad		Coordinates		Pad		Coordinates		Pad		Coordinates		Pad		Coordinates	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	V_{DD}	1.840	2.385	49	COM1	-2.385	1.840	97	SEG33	-1.840	-2.385	145	SEG81	2.385	-1.960
2	OSC3	1.760	2.385	50	COM2	-2.385	1.760	98	SEG34	-1.760	-2.385	146	SEG82	2.385	-1.880
3	OSC4	1.680	2.385	51	COM3	-2.385	1.680	99	SEG35	-1.680	-2.385	147	SEG83	2.385	-1.800
4	V_{SS}	1.600	2.385	52	COM4	-2.385	1.600	100	SEG36	-1.600	-2.385	148	SEG84	2.385	-1.720
5	V_{D1}	1.520	2.385	53	COM5	-2.385	1.520	101	SEG37	-1.520	-2.385	149	SEG85	2.385	-1.640
6	OSC1	1.440	2.385	54	COM6	-2.385	1.440	102	SEG38	-1.440	-2.385	150	SEG86	2.385	-1.560
7	OSC2	1.360	2.385	55	COM7	-2.385	1.360	103	SEG39	-1.360	-2.385	151	SEG87	2.385	-1.480
8	$\overline{TEST}$	1.280	2.385	56	COM8	-2.385	1.280	104	SEG40	-1.280	-2.385	152	SEG88	2.385	-1.400
9	$\overline{RESET}$	1.200	2.385	57	COM9	-2.385	1.200	105	SEG41	-1.200	-2.385	153	SEG89	2.385	-1.320
10	$\overline{DMOD}$	1.120	2.385	58	COM10	-2.385	1.120	106	SEG42	-1.120	-2.385	154	SEG90	2.385	-1.240
11	DRXD	1.040	2.385	59	COM11	-2.385	1.040	107	SEG43	-1.040	-2.385	155	SEG91	2.385	-1.160
12	DTXD	0.960	2.385	60	COM12	-2.385	0.960	108	SEG44	-0.960	-2.385	156	SEG92	2.385	-1.080
13	DCLK	0.880	2.385	61	COM13	-2.385	0.880	109	SEG45	-0.880	-2.385	157	SEG93	2.385	-1.000
14	K07/EXCL3	0.800	2.385	62	COM14	-2.385	0.800	110	SEG46	-0.800	-2.385	158	SEG94	2.385	-0.920
15	K06/EXCL2	0.720	2.385	63	COM15	-2.385	0.720	111	SEG47	-0.720	-2.385	159	SEG95	2.385	-0.840
16	K05/EXCL1	0.640	2.385	64	SEG0	-2.385	0.560	112	SEG48	-0.640	-2.385	160	COM31	2.385	-0.680
17	K04/EXCL0	0.560	2.385	65	SEG1	-2.385	0.480	113	SEG49	-0.560	-2.385	161	COM30	2.385	-0.600
18	K03	0.480	2.385	66	SEG2	-2.385	0.400	114	SEG50	-0.480	-2.385	162	COM29	2.385	-0.520
19	K02	0.400	2.385	67	SEG3	-2.385	0.320	115	SEG51	-0.400	-2.385	163	COM28	2.385	-0.440
20	K01	0.320	2.385	68	SEG4	-2.385	0.240	116	SEG52	-0.320	-2.385	164	COM27	2.385	-0.360
21	K00	0.240	2.385	69	SEG5	-2.385	0.160	117	SEG53	-0.240	-2.385	165	COM26	2.385	-0.280
22	P27	0.160	2.385	70	SEG6	-2.385	0.080	118	SEG54	-0.160	-2.385	166	COM25	2.385	-0.200
23	P26	0.080	2.385	71	SEG7	-2.385	0.000	119	SEG55	-0.080	-2.385	167	COM24	2.385	-0.120
24	P25	0.000	2.385	72	SEG8	-2.385	-0.080	120	SEG56	0.000	-2.385	168	COM23	2.385	-0.040
25	P24	-0.080	2.385	73	SEG9	-2.385	-0.160	121	SEG57	0.080	-2.385	169	COM22	2.385	0.040
26	P23/$\overline{SRDY1}$	-0.160	2.385	74	SEG10	-2.385	-0.240	122	SEG58	0.160	-2.385	170	COM21	2.385	0.120
27	P22/$\overline{SCLK1}$	-0.240	2.385	75	SEG11	-2.385	-0.320	123	SEG59	0.240	-2.385	171	COM20	2.385	0.200
28	P21/SOUT1	-0.320	2.385	76	SEG12	-2.385	-0.400	124	SEG60	0.320	-2.385	172	COM19	2.385	0.280
29	P20/SIN1	-0.400	2.385	77	SEG13	-2.385	-0.480	125	SEG61	0.400	-2.385	173	COM18	2.385	0.360
30	P17/$\overline{TOUT2}$/$\overline{TOUT3}$	-0.480	2.385	78	SEG14	-2.385	-0.560	126	SEG62	0.480	-2.385	174	COM17	2.385	0.440
31	P16/FOUT	-0.560	2.385	79	SEG15	-2.385	-0.640	127	SEG63	0.560	-2.385	175	COM16	2.385	0.520
32	P15/TOUT2/TOUT3	-0.640	2.385	80	SEG16	-2.385	-0.720	128	SEG64	0.640	-2.385	176	V_{SS}	2.385	0.680
33	P14/TOUT0/TOUT1	-0.720	2.385	81	SEG17	-2.385	-0.800	129	SEG65	0.720	-2.385	177	TEST1	2.385	0.760
34	P13/$\overline{SRDY0}$	-0.800	2.385	82	SEG18	-2.385	-0.880	130	SEG66	0.800	-2.385	178	TEST2	2.385	0.840
35	P12/$\overline{SCLK0}$	-0.880	2.385	83	SEG19	-2.385	-0.960	131	SEG67	0.880	-2.385	179	TEST3	2.385	0.920
36	P11/SOUT0	-0.960	2.385	84	SEG20	-2.385	-1.040	132	SEG68	0.960	-2.385	180	V_{D2}	2.385	1.000
37	P10/SIN0	-1.040	2.385	85	SEG21	-2.385	-1.120	133	SEG69	1.040	-2.385	181	CG	2.385	1.080
38	P07	-1.120	2.385	86	SEG22	-2.385	-1.200	134	SEG70	1.120	-2.385	182	CF	2.385	1.160
39	P06	-1.200	2.385	87	SEG23	-2.385	-1.280	135	SEG71	1.200	-2.385	183	CE	2.385	1.240
40	P05	-1.280	2.385	88	SEG24	-2.385	-1.360	136	SEG72	1.280	-2.385	184	CD	2.385	1.320
41	P04	-1.360	2.385	89	SEG25	-2.385	-1.440	137	SEG73	1.360	-2.385	185	CC	2.385	1.400
42	P03	-1.440	2.385	90	SEG26	-2.385	-1.520	138	SEG74	1.440	-2.385	186	CB	2.385	1.480
43	P02	-1.520	2.385	91	SEG27	-2.385	-1.600	139	SEG75	1.520	-2.385	187	CA	2.385	1.560
44	P01	-1.600	2.385	92	SEG28	-2.385	-1.680	140	SEG76	1.600	-2.385	188	V_{C5}	2.385	1.640
45	P00	-1.680	2.385	93	SEG29	-2.385	-1.760	141	SEG77	1.680	-2.385	189	V_{C4}	2.385	1.720
46	V_{DD}	-1.760	2.385	94	SEG30	-2.385	-1.840	142	SEG78	1.760	-2.385	190	V_{C3}	2.385	1.800
47	V_{SS}	-1.840	2.385	95	SEG31	-2.385	-1.920	143	SEG79	1.840	-2.385	191	V_{C2}	2.385	1.880
48	COM0	-2.385	1.920	96	SEG32	-1.920	-2.385	144	SEG80	1.920	-2.385	192	V_{C1}	2.385	1.960

APPENDIX A S5U1C88000P1&S5U1C88655P2 MANUAL (Peripheral Circuit Board for S1C8F626)

This manual describes how to use the Peripheral Circuit Board for S1C8F626 (S5U1C88000P1&S5U1C88655P2). This circuit board is used to provide emulation functions when it is installed in the ICE (S5U1C88000H5), a debugging tool for the 8-bit Single Chip Microcomputer S1C88 Family.
The explanation assumes that the S1C8F626 circuit data has been downloaded into the S1C88 Family Peripheral Circuit Board (S5U1C88000P1).
For how to download circuit data into the S5U1C88000P1 and specifications of the boards, refer to Sections A.4 and A.6, respectively. For details on ICE functions and how to operate the debugger, refer to the separately prepared manuals.

A.1 Names and Functions of Each Part

The following explains the names and functions of each part of the S5U1C88000P1&S5U1C88655P2.



Main board (S5U1C88000P1) *Add-on board (S5U1C88655P2)*

Fig. A.1.1 Board layout

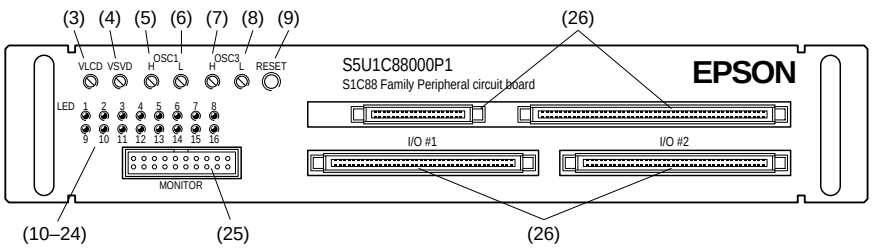


Fig. A.1.2 Panel layout (S5U1C88000P1)

(1) SW1

When downloading circuit data, set this switch to the "3" position. Otherwise, set to position "1".

(2) LCDVCC (on the back of the S5U1C88000P1 board)

The internal power voltage (V_{C5}) for the LCD driver can be varied using the DIP switch as shown in Table A.1.1. Be aware that the V_{C5} voltage level on this board is different from that of the actual IC.

Table A.1.1 Setting LCDVCC

LCDVCC				Setting
1	2	3	4	
ON	OFF	OFF	ON	V_{C5} = 6 V
OFF	ON	OFF	OFF	V_{C5} = 5.75 V
OFF	OFF	ON	OFF	V_{C5} = 5.5 V
OFF	OFF	OFF	ON	V_{C5} = 5 V
Other combinations				Not allowed

* The voltage value assumes that the LCD contrast adjustment register LC0–LC3 is 0FH. There is a need to allow for a maximum ±6% of error due to the characteristics of the parts used on this board.

(3) VLCD control

Unused.

(4) VSVD control

This control is used for varying the power supply voltage to confirm the supply voltage detection (SVD) function. (Refer to Section A.5.2, "Differences from Actual IC".)

(5) OSC1 H control

Unused.

(6) OSC1 L control

Unused.

(7) OSC3 H control

This control is used for coarse adjustment of the OSC3 CR oscillation frequency.

(8) OSC3 L control

This control is used for fine adjustment of the OSC3 CR oscillation frequency.

(9) RESET switch

This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.

(10) LED 1, LED 2 (Reserved)

Unused.

(11) LED 3 (CPUMOD)

Indicates the CPU mode.
Lit: Maximum (CPUMOD register = "1")
Not lit: Minimum (CPUMOD register = "0")

(12) LED 4 (CLKCHG)

Indicates the CPU operating clock.
Lit: OSC3 (CLKCHG register = "1")
Not lit: OSC1 (CLKCHG register = "0")

(13) LED 5 (SOSC3)

Indicates the OSC3 oscillation status.
Lit: OSC3 oscillation is on (SOSC3 register = "1")
Not lit: OSC3 oscillation is off (SOSC3 register = "0")

(14) LED 6 (SVDON)

Indicates the SVD circuit status.
Lit: SVD circuit is on (SVDON register = "1")
Not lit: SVD circuit is off (SVDON register = "0")

(15) LED 7 (LCDC)

Indicates the LCD circuit status.
Lit: LCD circuit is on (LCDC register = Not "00")
Not lit: LCD circuit is off (LCDC register = "00")

(16) LED 8 (HLMOD)

Indicates the heavy load protection status.
Lit: Heavy load protection mode (HLMOD register = "1")
Not lit: Normal mode (HLMOD register = "0")

(17) LED 9 (HALT/SLEEP)

Indicates the CPU status.
Lit: HALT or SLEEP
Not lit: RUN

(18) LED 10 (VDSEL)

Indicates the power voltage (V_{DD} or V_{D2}) selected for the LCD system voltage regulator.
Lit: V_{D2} (VDSEL register = "1")
Not lit: V_{DD} (VDSEL register = "0")

(19) LED 11 (DBON)

Indicates the status of the power voltage booster.
Lit: ON (DBON register = "1")
Not lit: OFF (DBON register = "0")

(20) LED 12 (SEGREV)

Indicates the SEG output assignment status.
Lit: Reverse (SEGREV register = "1")
Not lit: Normal (SEGREV register = "0")

(21) LED 13 (VDC)

Indicates the operating mode.
Lit: V_{D1} = 2.5 V (VDC register = "1")
Not lit: V_{D1} = 1.8 V (VDC register = "0")

(22) LED 14 (OSC1 operating clock)

The OSC1 operating clock is connected to this LED. The corresponding monitor pin (pin 14) can be used to check the OSC1 clock frequency.

(23) LED 15 (OSC3 operating clock)

The OSC3 operating clock is connected to this LED. The corresponding monitor pin (pin 15) can be used to check the OSC3 clock frequency.

(24) LED 16 (FPGA configuration)

If the FPGA on the S5U1C88000P1 includes circuit data, this LED lights when the power is turned on. If this LED does not light at power-up, a circuit data must be written to the FPGA before debugging can be started (turn the power on again after writing data).

(25) LED signal monitor connector

This connector provides the signals that drive the LEDs shown above for monitoring. The signals listed below are output from the connector pins. The signal level is high when the LED is lit and is low when the LED is not lit.

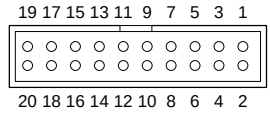


Fig. A.1.3 LED signal monitor connector

Pin 3: LED 3 (CPU mode)
Pin 4: LED 4 (CPU operating clock)
Pin 5: LED 5 (OSC3 oscillation status)
Pin 6: LED 6 (SVD circuit status)
Pin 7: LED 7 (LCD circuit status)
Pin 8: LED 8 (Heavy load protection status)
Pin 9: LED 9 (HALT/SLEEP, RUN status)
Pin 10: LED 10 (LCD voltage regulator power status)
Pin 11: LED 11 (Power voltage booster status)
Pin 12: LED 12 (SEG output assignment status)
Pin 13: LED 13 (Operating mode/VDC status)
Pin 14: LED 14 (OSC1 operating clock)
Pin 15: LED 15 (OSC3 operating clock)

Pin 19: OSC3 CR oscillation frequency monitor pin

Pins 1, 2, 17, 18 and 20 are not used.
The OSC3 CR oscillation clock is connected to pin 19. (The CR oscillation circuit on this board always operates even if crystal/ceramic oscillation is selected by option and regardless of the SOSC3 register status.) These pins can be used to monitor CR oscillation when adjusting the oscillation frequency.

(26) I/O #1, I/O #2, I/O #3, I/O #4 connectors

These are the connectors for connecting the I/O and LCD. The I/O cables (80-pin/40-pin × 2 flat type, 100-pin/50-pin × 2 flat type, 40-pin/20-pin × 2 flat type) are used to connect to the target system.

A.2 Installation

A.2.1 Installing S5U1C88655P2 to S5U1C88000P1

Aim the I/O connectors on the add-on board (S5U1C88655P2) at the front panel of the main board (S5U1C88000P1) and insert the four connectors on the back of the S5U1C88655P2 board into the corresponding connectors on the S5U1C88000P1 board.

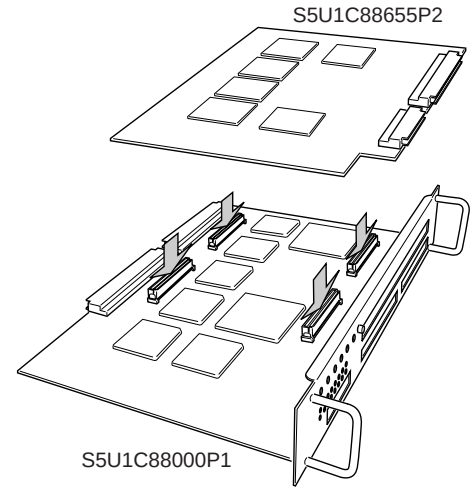


Fig. A.2.1.1 Installing S5U1C88655P2 to S5U1C88000P1

A.2.2 Installing into the ICE (S5U1C88000H5)

Insert the S5U1C88000P1 along by the lower guide rail of the ICE (S5U1C88000H5), until the connectors fit into the ICE back-panel connectors.

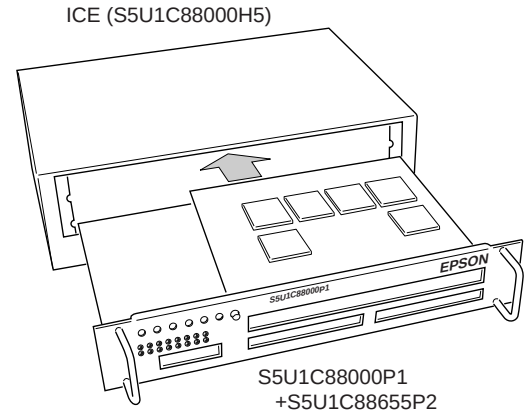


Fig. A.2.2.1 Installing into the ICE (S5U1C88000H5)

Note: The S5U1C88000P1 and S5U1C88655P2 may fail to operate if they are not adequately mounted, so be sure to mount them securely.

A.3 Connecting to the Target System

This section explains how to connect the S5U1C88000P1&S5U1C88655P2 to the target system.

Note: Turn the power of all equipment off before connecting or disconnecting cables.

Use the I/O cables (80-pin/40-pin × 2 flat type, 100-pin/50-pin × 2 flat type, 40-pin/20-pin × 2 flat type) to connect between the I/O #1 to I/O #4 connectors of the front panel and the target system.
Connect the 80-pin, 100-pin and 40-pin cable connectors to the I/O #1 to I/O #4 connectors, and the 40-pin × 2, 50-pin × 2 and 20-pin × 2 connectors to the target system. Be careful as power (V_{DD}) is supplied to I/O #1, I/O #2 and I/O #3 connectors.

The following shows the clock frequencies generated from the on-board crystal oscillation circuits:
OSC1 crystal oscillation circuit: 32.768 kHz
OSC3 crystal oscillation circuit: 4.9152 MHz

When CR oscillation is selected for OSC3, the oscillation frequency can be adjusted using the controls on the front panel (OSC3H and OSC3L). Use a frequency counter or other equipment to be connected to the OSC3 CR oscillation frequency monitor pin (pin 19) on the monitor connector for monitoring the frequency during adjustment. Be sure of the frequency when using this monitor pin because the CR oscillation frequency is initially undefined.

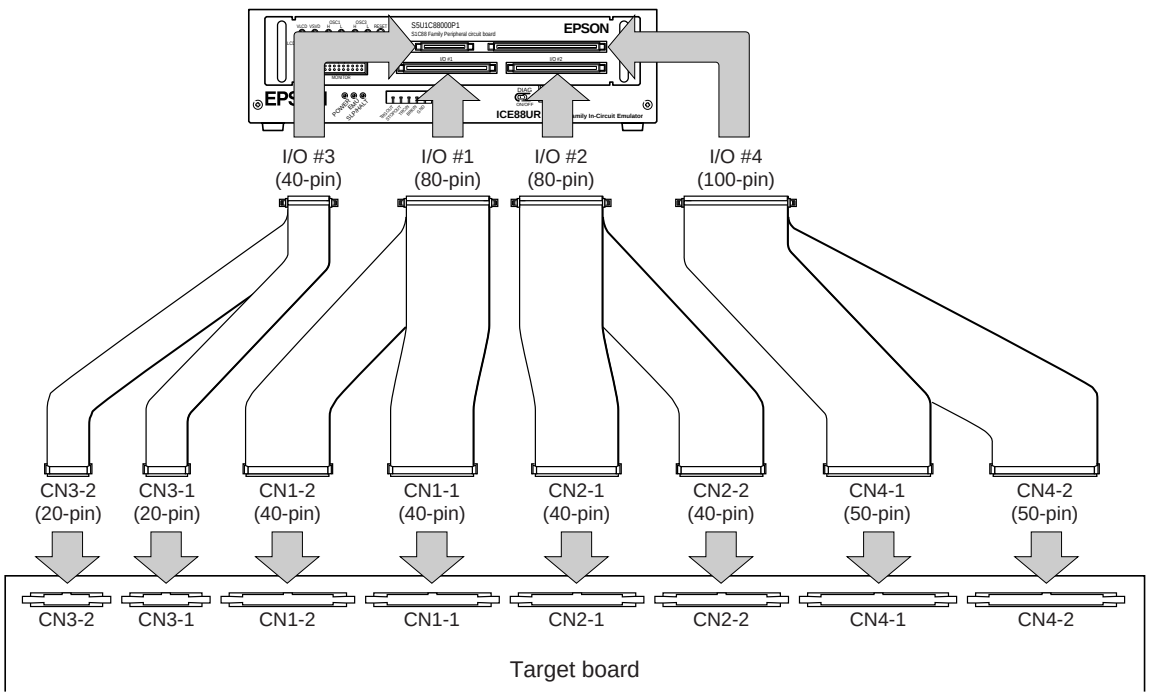


Fig. A.3.1 Connecting to the target system

I/O connector pin assignment

Table A.3.1 I/O #1 connector

40-pin CN1-1		40-pin CN1-2	
No.	Pin name	No.	Pin name
1	V_{DD} (3.3 V)	1	N.C.
2	V_{DD} (3.3 V)	2	N.C.
3	V_{SS}	3	N.C.
4	V_{SS}	4	N.C.
5	$\overline{DMOD}$	5	N.C.
6	DTXD	6	N.C.
7	DRXD	7	N.C.
8	DCLK	8	N.C.
9	N.C.	9	N.C.
10	N.C.	10	N.C.
11	N.C.	11	N.C.
12	N.C.	12	N.C.
13	N.C.	13	N.C.
14	N.C.	14	N.C.
15	N.C.	15	N.C.
16	N.C.	16	N.C.
17	N.C.	17	N.C.
18	N.C.	18	N.C.
19	N.C.	19	N.C.
20	N.C.	20	N.C.
21	N.C.	21	N.C.
22	N.C.	22	N.C.
23	N.C.	23	N.C.
24	N.C.	24	N.C.
25	N.C.	25	COM0
26	N.C.	26	COM1
27	N.C.	27	COM2
28	N.C.	28	COM3
29	N.C.	29	COM4
30	N.C.	30	COM5
31	N.C.	31	COM6
32	N.C.	32	COM7
33	N.C.	33	COM8
34	N.C.	34	COM9
35	N.C.	35	COM10
36	N.C.	36	COM11
37	N.C.	37	COM12
38	N.C.	38	COM13
39	N.C.	39	COM14
40	N.C.	40	COM15

Table A.3.2 I/O #2 connector

40-pin CN2-1		40-pin CN2-2	
No.	Pin name	No.	Pin name
1	V_{DD} (3.3 V)	1	SEG27
2	V_{DD} (3.3 V)	2	SEG28
3	V_{SS}	3	SEG29
4	V_{SS}	4	SEG30
5	$\overline{RESET}$	5	SEG31
6	N.C.	6	SEG32
7	OSC1EX	7	SEG33
8	OSC3EX	8	SEG34
9	V_{C1}	9	SEG35
10	V_{C2}	10	SEG36
11	V_{C3}	11	SEG37
12	V_{C4}	12	SEG38
13	V_{C5}	13	SEG39
14	SEG0	14	SEG40
15	SEG1	15	SEG41
16	SEG2	16	SEG42
17	SEG3	17	SEG43
18	SEG4	18	SEG44
19	SEG5	19	SEG45
20	SEG6	20	SEG46
21	SEG7	21	SEG47
22	SEG8	22	SEG48
23	SEG9	23	SEG49
24	SEG10	24	SEG50
25	SEG11	25	SEG51
26	SEG12	26	SEG52
27	SEG13	27	SEG53
28	SEG14	28	SEG54
29	SEG15	29	SEG55
30	SEG16	30	SEG56
31	SEG17	31	SEG57
32	SEG18	32	SEG58
33	SEG19	33	SEG59
34	SEG20	34	SEG60
35	SEG21	35	SEG61
36	SEG22	36	SEG62
37	SEG23	37	SEG63
38	SEG24	38	SEG64
39	SEG25	39	SEG65
40	SEG26	40	SEG66

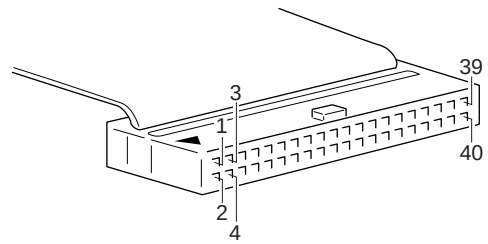


Fig. A.3.2 CN1-1/CN1-2 and CN2-1/CN2-2 pin layout

Table A.3.3 I/O #3 connector

20-pin CN3-1		20-pin CN3-2	
No.	Pin name	No.	Pin name
1	K00	1	VSS
2	K01	2	VSS
3	K02	3	P00
4	K03	4	P01
5	K04/EXCL0	5	P02
6	K05/EXCL1	6	P03
7	K06/EXCL2	7	P04
8	K07/EXCL3	8	P05
9	N.C.	9	P06
10	N.C.	10	P07
11	N.C.	11	VDD (3.3 V)
12	N.C.	12	VDD (3.3 V)
13	P20/SIN1	13	P10/SIN0
14	P21/SOUT1	14	P11/SOUT0
15	P22/$\overline{\text{SCLK1}}$	15	P12/$\overline{\text{SCLK0}}$
16	P23/$\overline{\text{SRDY1}}$	16	P13/$\overline{\text{SRDY0}}$
17	P24	17	P14/TOUT0/TOUT1
18	P25	18	P15/TOUT2/TOUT3
19	P26	19	P16/$\overline{\text{FOUT}}$
20	P27	20	P17/$\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$

Table A.3.4 I/O #4 connector

50-pin CN4-1		50-pin CN4-2	
No.	Pin name	No.	Pin name
1	SEG67	1	N.C.
2	SEG68	2	N.C.
3	SEG69	3	N.C.
4	SEG70	4	N.C.
5	SEG71	5	N.C.
6	SEG72	6	N.C.
7	SEG73	7	N.C.
8	SEG74	8	N.C.
9	SEG75	9	N.C.
10	SEG76	10	N.C.
11	SEG77	11	N.C.
12	SEG78	12	N.C.
13	SEG79	13	N.C.
14	SEG80	14	N.C.
15	SEG81	15	N.C.
16	SEG82	16	N.C.
17	SEG83	17	N.C.
18	SEG84	18	N.C.
19	SEG85	19	N.C.
20	SEG86	20	N.C.
21	SEG87	21	N.C.
22	SEG88	22	N.C.
23	SEG89	23	N.C.
24	SEG90	24	N.C.
25	SEG91	25	N.C.
26	SEG92	26	N.C.
27	SEG93	27	N.C.
28	SEG94	28	N.C.
29	SEG95	29	N.C.
30	N.C.	30	N.C.
31	N.C.	31	N.C.
32	N.C.	32	N.C.
33	N.C.	33	N.C.
34	N.C.	34	VSS
35	N.C.	35	COM16
36	N.C.	36	COM17
37	N.C.	37	COM18
38	N.C.	38	COM19
39	N.C.	39	COM20
40	N.C.	40	COM21
41	N.C.	41	COM22
42	N.C.	42	COM23
43	N.C.	43	COM24
44	N.C.	44	COM25
45	N.C.	45	COM26
46	N.C.	46	COM27
47	N.C.	47	COM28
48	N.C.	48	COM29
49	N.C.	49	COM30
50	N.C.	50	COM31

A.4 Downloading Circuit Data to the S5U1C88000P1

This board (S5U1C88000P1) comes with the FPGA that contains factory inspection data, therefore the circuit data for the model to be used should be downloaded. The following explains the downloading procedure.

1) Set the switch "SW1"*1 on this board to the "3" position.
2) Install this board to the ICE (S5U1C88000H5) as shown in Section A.2.2.
3) Connect the ICE to the host PC. Then turn the host PC and ICE on.
4) Invoke the debugger included in the ICE or assembler package. For how to use the ICE and debugger, refer to the manuals supplied with the ICE and assembler package.
5) Download the circuit data file (.mcs) corresponding to the model by entering the following commands in the command window.

`>XFER`		(erase all)
`>XFWR`	<*file name*>	(download the specified file)*2
`>XFCP`	<*file name*>	(compare the specified file and downloaded data)

6) Terminate the debugger and then turn the ICE off.
7) Remove this board from the ICE and set the switch "SW1" on the board to the "1" position.
8) Install this board to the ICE again.
9) Turn the ICE on and invoke the debugger again. Debugging can be started here.

*1 See Figure A.1.1, "Board layout", for the location of SW1.
*2 The downloading takes about 5 minutes.

A.5 Precautions

Take the following precautions when using the S5U1C88000P1&S5U1C88655P2.

A.5.1 Precaution for operation

(1) Turn the power of all equipment off before connecting or disconnecting cables.

(2) The mask option data must be loaded before debugging can be started.

A.5.2 Differences from actual IC

Caution is called for due to the following function and property related differences with the actual IC. If these precautions are overlooked, it may not operate on the actual IC, even if it operates on the ICE in which the S5U1C88000P1&S5U1C88655P2 has been installed.

(1) I/O differences

Interface power voltage

This board and target system interface voltage is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a level shifter or similar circuit on the target system side to accommodate the required interface voltage.

Drive capability of each output port

The drive capability of each output port on this board is higher than that of the actual IC. When designing the application system and software, refer to Chapter 9, "ELECTRICAL CHARACTERISTICS" to confirm the drive capability of each output port.

Input port characteristics

The AC characteristic of the input terminal is different from that of the actual IC and it affects the input interrupt function. Therefore, evaluate the operation in the actual IC if the rise/fall time of the input signal is long.

Protective diode of each port

All I/O ports incorporate a protective diode for V_{DD} and V_{SS}, and the interface signals between this board and the target system are set to +3.3 V. Therefore, this board and the target system cannot be interfaced with a voltage exceeding V_{DD} even if the output ports are configured with open-drain output.

Pull-up resistance value

The pull-up resistance values on this board are set to 300 kΩ which differ from those for the actual IC. For the resistance values on the actual IC, refer to Chapter 9, "ELECTRICAL CHARACTERISTICS".
Note that when using pull-up resistors to pull the input terminals high, the input terminals may require a certain period to reach a valid high level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since rise delay times on these input ports differ from those of the actual IC.

(2) Differences in current consumption

The amount of current consumed by this board differs significantly from that of the actual IC. Inspecting the LEDs on the S5U1C88000P1 front panel may help keep track of approximate current consumption. The following factors / components greatly affect device current consumption:

Those which can be verified by LEDs and monitor pins

a) Run and Halt execution ratio
(verified by LEDs and monitor pins on the ICE)
b) CPU operating clock change control
(LED 4: monitor pin 4)
c) OSC3 oscillation on / off control
(LED 5: monitor pin 5)
d) SVD circuit on / off control
(LED 6: monitor pin 6)
e) LCD power supply control
(LED 7: monitor pin 7)
f) Heavy load protection mode
(LED 8: monitor pin 8)
g) SLEEP and Halt execution ratio
(LED 9: monitor pin 9)
h) LCD voltage regulator power selection
(LED 10: monitor pin 10)
i) Power voltage booster
(LED 11: monitor pin 11)
j) Operating mode selected
(LED 13: monitor pin 13)
k) OSC1 operating clock
(LED 14: monitor pin 14)
l) OSC3 operating clock
(LED 15: monitor pin 15)

Those that can only be counteracted by system or software

m) Current consumed by the internal pull-up resistors
n) Input ports in a floating state

(3) Functional precautions

LCD circuit

- Pay attention to the output drive capability and output voltage of the LCD terminals (SEG, COM), since they are different from those of the actual IC. The system and the software should be designed in order to adjust the LCD contrast. The S5U1C88000P1 board allows switching of the LCD drive voltage with its switch on the back side. (Refer to Section A.1, "Names and Functions of Each Part")
- When the LCDC0 and LCDC1 registers are both set to "0" (LCD power control circuit is off), the SEG and COM terminal outputs of the actual IC are fixed at V_{SS} level. Note, however, that the COM outputs are fixed at V_{C4} level and the SEG outputs are fixed at V_{C3} level in this board.
- This board supports 16 × 16 / 5 × 8 dot font only and 12 × 12 dot font can not be used. (Writing and reading to / from DTFNT bit are enabled.)
- This board does not support reversing of the SEG assignment using the SEGREV bit. Check whether LED12 is lit or not to confirm the SEGREV status. (Writing and reading to / from SEGREV bit are enabled.)
- The actual IC outputs only COM0 to COM15 signals even if the display area is switched (DSPAR = "1") when the LCD driver is set to 1 / 16 (or 1 / 8) duty drive. This board outputs COM16 to COM31 signals with the same waveform as the COM0 to COM15. Therefore, if COM16 to COM31 along with COM0 to COM15 are connected to the LCD panel, the LCD panel displays the same contents twice to the upper half and lower half.

SVD circuit

- The SVD function is realized by artificially varying the power supply voltage using the VSVD control on the front panel of the S5U1C88000P1.
- There is a finite delay time from when the power to the SVD circuit turns on until actual detection of the voltage. The delay time on this board differs from that of the actual IC. Refer to Chapter 9, "ELECTRICAL CHARACTERISTICS" when setting the appropriate wait time for the actual IC.
- The evaluation voltages supported in this board are different from those of the actual IC. When debugging the SVD operation using this board, evaluate the SVD results as levels not voltages.

Oscillation circuit

- The OSC1 crystal oscillation frequency is fixed at 32.768 kHz.
- The OSC3 crystal oscillation frequency is fixed at 4.9152 MHz.
- The OSC3 CR oscillation frequency can be adjusted in the range of approx. 100 kHz to 8 MHz using the control on the S5U1C88000P1 front panel. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 9, "ELECTRICAL CHARACTERISTICS" to select the appropriate operating frequency.
- The S5U1C88000P1&S5U1C88655P2 does not include the OSC3 ceramic oscillation circuit. When ceramic oscillation circuit is selected by mask option, the S5U1C88655P2 uses the on-board crystal oscillation circuit.
- When using an external clock, adjust the external clock (amplitude: 3.3 V ±5%, duty: 50% ±10%) and input to the OSC1 or OSC3 terminal with Vss as GND.
- This board can operate normally even when the CPU clock is switched to OSC3 (CLKCHG = "1") immediately after the OSC3 oscillation control circuit is turned on (SOSC3 = "1") without a wait time inserted. In the actual IC, an oscillation stability wait time is required before switching the CPU clock after the OSC3 oscillation is turned on. Refer to Chapter 9, "ELECTRICAL CHARACTERISTICS" when setting the appropriate wait time for the actual IC.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If executed simultaneously with a single instruction, these operations, although good with this board, may not function properly with the actual IC.
- This board contains oscillation circuits for OSC1 and OSC3. Keep in mind that even though the actual IC may not have a resonator connected to its OSC3, this board can operate with the OSC3 circuit.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts on this board differs from that of the actual IC.

Access to undefined address space

If any undefined space in the S1C8F626's internal ROM / RAM or I / O is accessed for data read or write operations, the read / written value is indeterminate. Additionally, it is important to remain aware that the indeterminate state differs between this board and the actual IC.

Reset circuit

Keep in mind that the operation sequence from when the ICE with this board installed is powered on until the time at which the program starts running differs from the sequence of the actual IC. This is because this board becomes capable of operating as a debugging system after the user program and optional data are downloaded.

Internal power supply circuit

The LCD drive voltage on this board is different from that on the actual IC.

Input interface level

The actual IC allows selection of the K00–K07, P10–P17 and P20–P27 port input interface levels either COMS level or CMOS Schmitt level with software. This board supports CMOS level only and software selection does not affect the interface level of this board.

(4) Notes on model support

Parameter file

The ROM, RAM and I / O spaces in the ICE with this board installed are configured when the debugger on the personal computer starts up using the parameter file (8F626.par) provided for each model.

The parameter file allows the user to modify its contents according to the ROM and RAM spaces actually used. However, do not configure areas other than below.

ROM area: 0000H to BFFFH
10000H to 3FFFFH
RAM area: D800H to F7FFH
Stack area: D800H to F7FFH

Access disable area

When using this board for development of an S1C8F626 application, be sure not to read and write from / to I / O memory addresses FF16H and FF90H to FFADH.

Furthermore, do not change the initial values when writing to bit D4 of address FF17H.

A.6 Product Specifications

A.6.1 S5U1C88000P1 specifications

S5U1C88000P1

Dimensions (mm):
247.5 (wide) × 165 (depth) × 44.6 (height)
Weight:
Approx. 500 g
Power supply:
DC 5 V ± 5%, less than 1 A
(supplied from ICE main unit)

I/O connection cable (80-pin/40-pin x 2, 2 cables)

S5U1C88000P1 connector (80-pin):
KEL 8830E-080-170L, or equivalent
Cable connector (80-pin):
KEL 8822E-080-171 × 1
Cable connector (40-pin):
3M 7940-6500SC × 2
Cable:
40-pin flat cable × 2
Interface:
CMOS interface (3.3 V)
Length:
Approx. 40 cm

Monitor signal cable

S5U1C88000P1 connector:
3M 7610-5002SC, or equivalent
Cable connector (10-pin):
3M 7910-6500SC × 1
Interface:
CMOS interface (3.3 V)
Length:
Approx. 40 cm

Accessories

40-pin connector for the target system:
3M 3432-6002LCSC × 4

A.6.2 S5U1C88655P2 specifications

S5U1C88655P2

Dimensions (mm):
184 (W) × 152 (D) × 17 (H)

I/O cable (100-pin/50-pin x 2)

S5U1C88655P2 connector (100-pin):
KEL 8830E-100-170L
Cable connector (100-pin):
KEL 8822E-100-170L × 1
Cable connector (50-pin):
Connector 3M 7950-B500SC × 2
Strain relief 3M 3448-7950 × 2
Cable:
50-pin flat cable × 1
Interface:
CMOS interface (3.3 V)
Length:
Approx. 40 cm

I/O cable (40-pin/20-pin x 2)

S5U1C88655P2 connector (40-pin):
KEL 8830E-040-170L
Cable connector (40-pin):
KEL 8822E-040-170L × 1
Cable connector (20-pin):
Connector 3M 7920-B500SC × 2
Strain relief 3M 3448-7920 × 2
Cable:
20-pin flat cable × 1
Interface:
CMOS interface (3.3 V)
Length:
Approx. 40 cm

Accessories

50-pin connector for the target system:
3M 3433-6002LCSC × 2
20-pin connector for the target system:
3M 3428-6002LCSC × 2

APPENDIX B USING KANJI FONT

Use the S5U1C88000R1 (12 × 12-dot RIS 506 kanji font package) to display kanji font on an LCD in the S1C8F626 microcomputer.

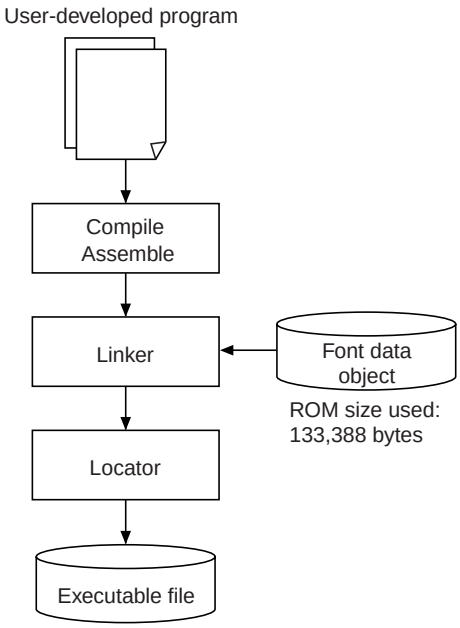
This package contains 12 × 12-dot-sized fonts (Seiko Epson original design[Note 1]) for the character codes conforming to the music shift-JIS kanji stipulated in the Recording Industry Association of Japan standard RIS 506-1996, which are supplied in the form of embeddable data for S1C88-Family microcomputer programs. The package also contains a sample program that runs on the S1C88-Family microcomputer to display this font data on an LCD, an application note for the sample program, and a bitmap utility that can be used to create custom font data.

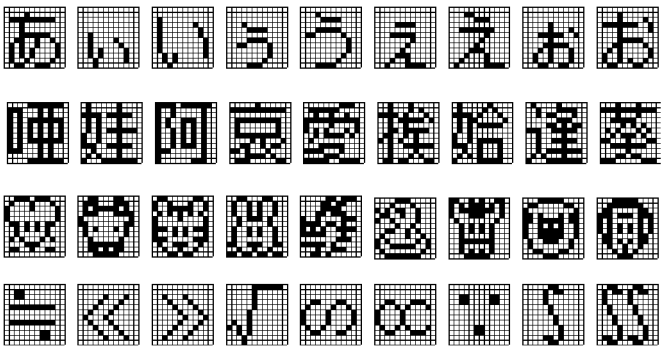
The kanji font data is supplied in an object file format (assembler output file identified by the extension .obj) to enable it to be embedded in the S1C88-Family microcomputer programs. Simply by linking this object file to the created application program, the kanji font data can be used easily.[Note 2]

See the "S5U1C88000R1 Manual" for details.

Notes 1 Before the kanji font data included with the package and the typefaces shown in the manual can be used, a contract for a license to use the typefaces must be concluded between Seiko Epson and the purchaser.

2 The programs necessary to obtain font data from the character codes and display the font data on an LCD must be created by the user.





Shown here is the typeface of an excerpted kanji font.

APPENDIX C PROM PROGRAMMING

C.1 Outline of PROM Programming Tools

The S1C8F626 Flash EEPROM programming tools are available for two interfaces: USB interface and RS-232C interface.
These PROM writers feature smaller size and weight and are operable with the same power supply as the microcomputer, this makes it possible to simply configure an on-board PROM programming environment.

USB interface type

- USB-Serial On Board Writer (product name: S5U1C88000W4)
- On Board Writer Control Software (OBPW88.EXE, RW8F626.INI) *
- USB-Serial conversion driver *

Operating voltage: 3.3 V ± 0.3 V (The power supply for the target can be used.)
PC interface: USB Ver. 1.1

Note: When using a USB hub to connect the USB-Serial On Board Writer to the PC, the USB hub should be driven with an external power supply. So use a USB hub that operates with an external power supply.

RS-232C interface type

- On Board Writer (product name: S5U1C88000W3)
- On Board Writer Control Software (OBPW88.EXE, RW8F626.INI) *

Operating voltage: 3.3 V ± 0.3 V (The power supply for the target can be used.)
PC interface: EIA-RS-232C

* The On Board Writer Control Software and USB-Serial conversion driver are included in the S1C88 Family Integrated Tool Package (S5U1C88000C1) Ver. 6 or later.
The On Board Writer Control Software (OBPW88.EXE, RW8F626.INI) supports both USB interface type and RS-232C interface type PROM writers.

C.2 How To Programming PROM

C.2.1 PROM programming environment

Prepare a personal computer system as a host computer and the data for programming the built-in Flash microcomputer.

(1) Personal computer

- IBM-PC / AT or compatible with a USB port or RS-232C port

(2) OS

- Windows 2000 / XP English or Japanese version

(3) PROM programming tools

- S5U1C88000W4 (USB interface type) package or S5U1C88000W3 (RS-232C interface type) package
- On Board Writer Control Software (OBPW88.EXE, RW8F626.INI) *
- USB-Serial conversion driver (required only when the USB-Serial On Board Writer is used) *

* The On Board Writer Control Software and USB-Serial conversion driver are included in the S1C88 Family Integrated Tool Package (S5U1C88000C1) Ver. 6 or later.

(4) User data (ROM data HEX file)

Execute the FIL88xxx to create the built-in ROM data HEX data file (C8F626xxx.PSA) from the program data HEX file (C8F626xxx.SA).
Refer to the S5U1C88000C Manual for details of the FIL88xxx.

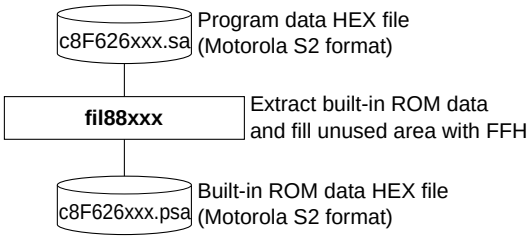


Fig. C.2.1.1 FIL88xxx execution flow

C.2.2 System connection for PROM programming

Below shows connection diagrams between the PC and the USB-Serial On Board Writer (S5U1C88000W4) with a target, and between the PC and the On Board Writer (S5U1C88000W3) with a target.

When the USB-Serial On Board Writer (S5U1C88000W4) is used

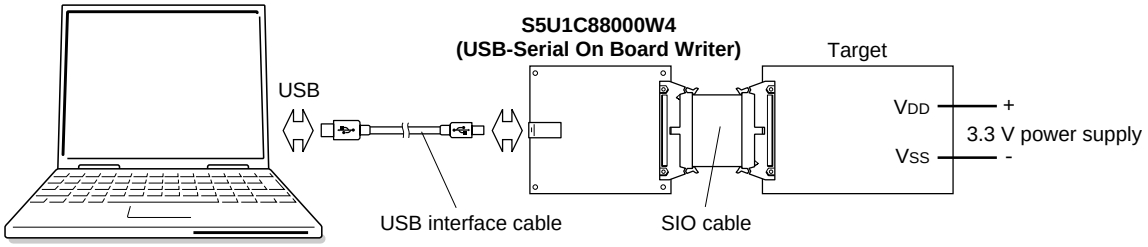


Fig. C.2.2.1 PROM programming system connection diagram (USB interface type)

When the On Board Writer (S5U1C88000W3) is used

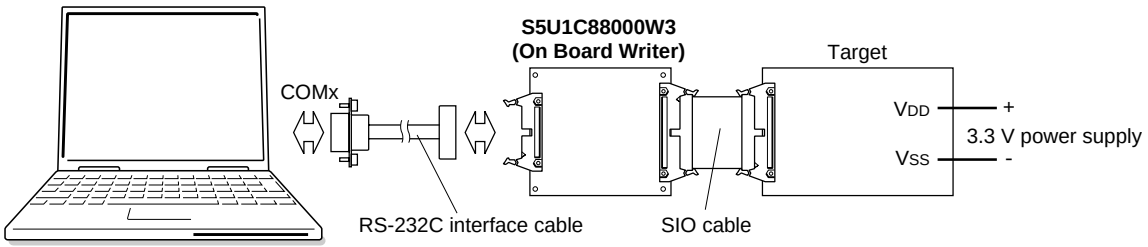


Fig. C.2.2.2 PROM programming system connection diagram (RS-232C interface type)

The system should be connected according to the following procedure.

(1) Make sure the power for the personal computer is switched off.

(2) As shown in the above figures, connect between the USB-Serial On Board Writer (S5U1C88000W4) or On Board Writer (S5U1C88000W3) and the PC using the interface cable included with the package.

Notes:
- *Turn the personal computer off before connecting and disconnecting the On Board Writer (S5U1C88000W3). The USB-Serial On Board Writer (S5U1C88000W4) can be connected after the PC is turned on.*
- *Secure the RS-232C cable with the connector screws to prevent malfunction.*

C.2.3 PROM programming procedure

(1) Connecting the system

Connect the system as shown in Section C.2.2, "System connection for PROM programming".

(2) Power on

Turn the personal computer on.

(3) Checking the serial port assignment

(Required only when the On Board Writer is used)

Check the serial port assignment on the personal computer. The On Board Writer uses the COM1 port by default setting.

(4) Installing the USB-Serial conversion driver

(Required only when the USB-Serial On Board Writer is used)

When the USB-Serial On Board Writer (S5U1C88000W4) is connected for the first time, a dialog box appears on the PC screen to prompt the user to install the driver. Install the USB-Serial conversion driver by following the prompts. The USB-Serial conversion driver was copied in the "\EPSON\S1C88\writer\driver" folder when the S1C88 Family Integrated Tool Package (S5U1C88000C1 Ver. 6 or later) was installed. Specify this folder as the driver location.

(5) Checking the serial port assignment

(Required only when the USB-Serial On Board Writer is used)

Open the Windows [Control Panel] → [System] → [Hardware] tab → [Device Manager] to check the COM port to which the USB-Serial port is assigned.

The USB-Serial conversion driver assigns a logical COM port to the physical USB port and transfers the COM port input/output to the USB input/output. Thus the On Board Writer Control Software can control the USB-Serial On Board Writer connected to the USB port through the assigned COM port.

(6) Preparing the On Board Writer Control Software

The On Board Writer Control Software was copied in the "\EPSON\S1C88\writer\OBPW" folder when the S1C88 Family Integrated Tool Package (S5U1C88000C1 Ver. 6 or later) was installed. When using the On Board Writer Control Software in another folder, the following two files should be copied from the OBPW folder.

- OBPW88.EXE
- RW8F626.INI

(7) Connecting the target board to the USB-Serial On Board Writer or On Board Writer

As Figure C.2.2.1 or C.2.2.2 shows, connect the target board to the USB-Serial On Board Writer (S5U1C88000W4) or On Board Writer (S5U1C88000W3) using the supplied SIO cable.

(8) Connecting the power supply for PROM programming

Connect the power supply for PROM programming (3.3 V) to the target board.

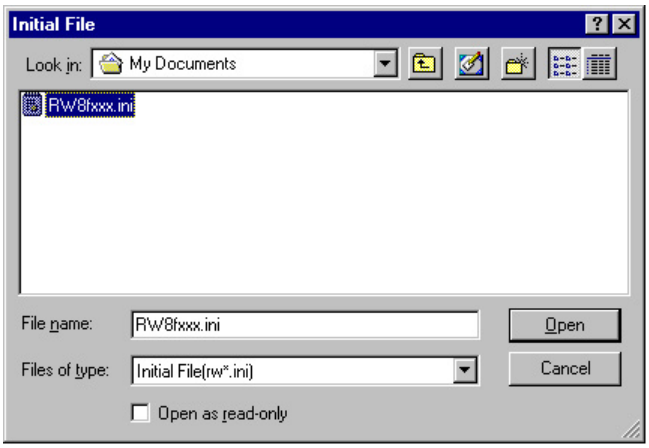
Notes:
- *Turn off the power of the target board except for the PROM programming power supply.*
- *Since PROM programming uses a 3.3-V power source, be careful of the voltage ratings of the parts on the target board.*

(9) Turning the PROM programming power on

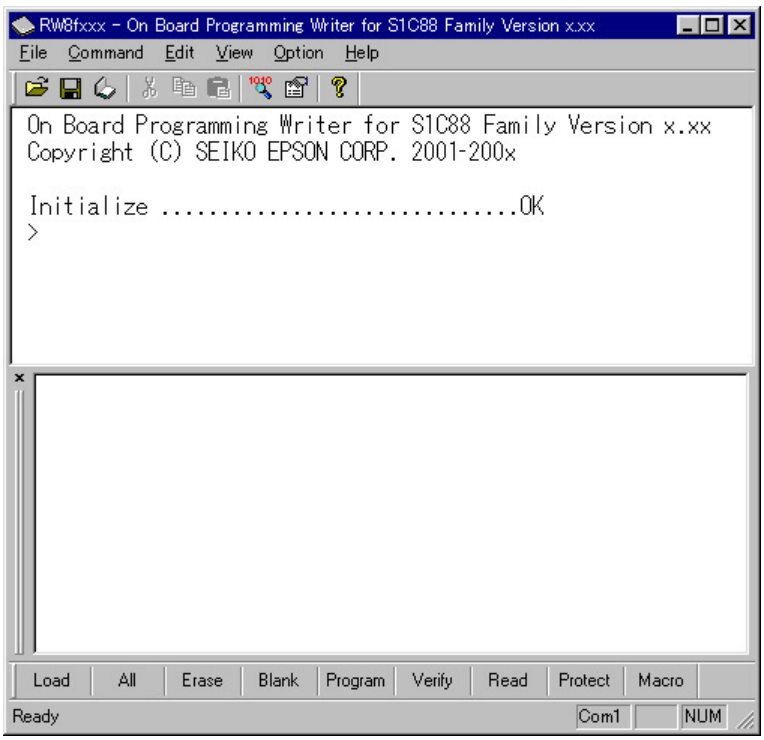
Turn the PROM programming power on. This also supplies the power to the USB-Serial On Board Writer (S5U1C88000W4) or On Board Writer (S5U1C88000W3) through the SIO cable.

(10) Starting up the On Board Writer Control Software

Double-click the OBPW88.EXE icon.
The [Initial File] dialog box shown below appears when the On Board Writer Control Software starts up.



Select the initial file with the same name as the microcomputer model.
RW*xxxxx*.ini *xxxxx*: microcomputer model name (e.g. 8f626 for the S1C8F626)
After an initial file is selected, the window shown below appears.



← Command window

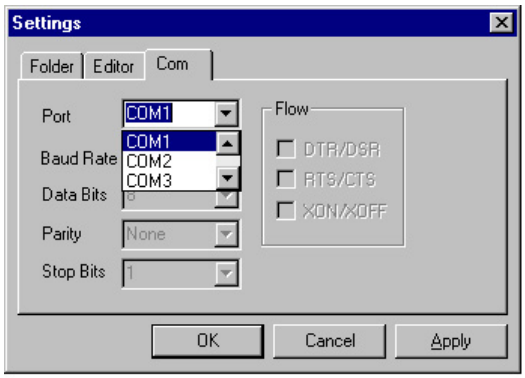
← Output window

(11) Selecting a serial port

Click the [Setting] button (or choose [Setting] from the [Option] menu) to display the [Settings] dialog box.

 *[Setting] button*

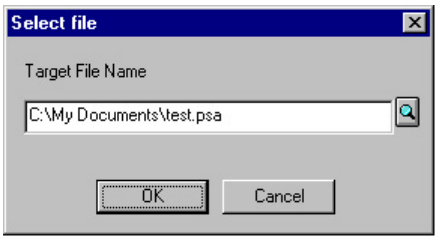
Click the [Com] tab to open the page shown below. When USB-Serial On Board Writer (USB interface type) is used, select the COM port that was determined in Step (5). When the On Board Writer (RS-232C interface type) is used, select the COM port to which the RS-232C cable has been connected.



(12) Loading user data to the personal computer

Click the [Load] button (or choose [Load] from the [Command] menu) to display the [Select file] dialog box.

 *[Load] button*



Choose the PSA file to be programmed to the PROM using the [Browse] button and then click [OK].

 *[Browse] button*

When data is loaded normally, "Complete" is displayed in the output window.

(13) Erasing PROM data

Click the [Erase] button (or choose [Erase] from the [Command] menu) to display an information dialog box. Clicking the [OK] button starts erasing the PROM data.

 *[Erase] button*

When the PROM is erased normally, "Complete" is displayed in the output window.

Notes: • *Inspection data is programmed in the PROM at shipment, so erase it once to initialize the contents.*

• *The PROM is protected against a read out when user data is programmed at Seiko Epson's factory. The protection is released after the contents have been erased by executing "Erasing PROM data".*

(14) Blank check after erasing

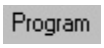
Click the [Blank] button (or choose [Blank Check] from the [Command] menu) starts process that checks if the PROM is completely erased.

 *[Blank] button*

When the blank check is finished normally, "Complete" is displayed in the output window.

(15) Programming user data

Click the [Program] button (or choose [Program] from the [Command] menu) to display an information dialog box. Clicking the [OK] button starts programming the PROM with the loaded data.



[Program] button

When programming is finished normally, "Complete" is displayed in the output window.

Note: Do not send the writer control window behind any other applications as it may cause a communication error.

(16) Verifying user data after programming

Click the [Verify] button (or choose [Verify] from the [Command] menu) starts verification of the PROM.

[Verify] button

When verification is finished without any error, "Complete" is displayed in the output window.

(17) Turning the PROM programming power off

Turn the PROM programming power off.

(18) Disconnecting the target board

Disconnect the target board after checking that programming has finished normally.

Note: Make sure that the PROM programming power is off before disconnecting and connecting the target board.

(19) Terminating the On Board Writer Control Software

Choose [Exit] from the [File] menu of the On Board Writer control window or click the close box to terminate the On Board Writer Control Software.
To continue programming, repeat from step (12) to step (18).

(20) Power off

Turn the personal computer off.

* Steps (13) to (15) can also be executed by clicking the [All] button only.

[All] button

Furthermore, the erase, erase check, program and verify commands allow specification of an address range when the command is entered from the keyboard. Refer to Section C.2.5.3, "Operating method", for details of the commands.

C.2.4 Connection diagram for PROM programming

The figures and tables below show the connection diagram on the target board and the signal specifications.

USB interface type: when the USB-Serial On Board Writer (S5U1C88000W4) is used

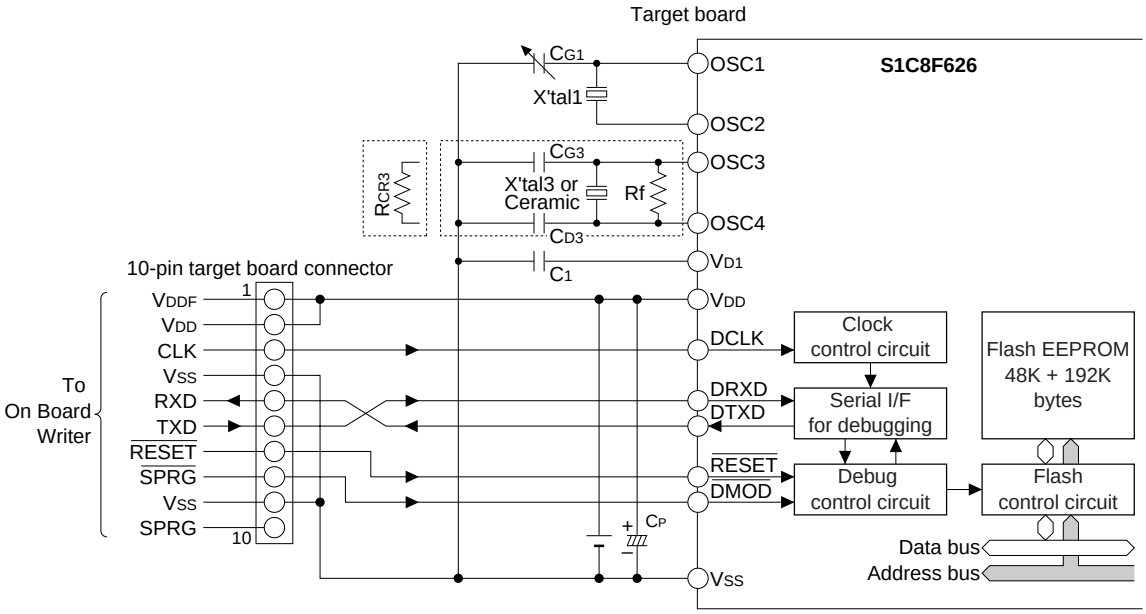


Fig. C.2.4.1 Connection diagram for on-board programming (USB interface type)

Table C.2.4.1 Signal specifications (USB interface type)

Connector pin No.	Signal name	Description	Microcomputer pin to be connected
1	V_{DDF}	Programming power supply pin	V_{DD} pin
2	V_{DD}	Power supply pin	V_{DD} pin
3	CLK	System clock output	DCLK pin
4	V_{SS}	Ground pin	V_{SS} pin
5	RXD	Serial I/F data input	DTXD pin
6	TXD	Serial I/F data output	DRXD pin
7	$\overline{\text{RESET}}$	Initial reset output	$\overline{\text{RESET}}$ pin
8	$\overline{\text{SPRG}}$	Programming mode setup output (for negative polarity I/O models)	$\overline{\text{DMOD}}$ pin
9	V_{SS}	Ground pin	V_{SS} pin
10	SPRG	Programming mode setup output (for positive polarity I/O models)	N.C.

Table C.2.4.2 Connectors for connecting On Board Writer (USB interface type)

Name	Model name	
Box header (male) [target side]	3662-6002LCPL (3M) or equivalent	
Socket connector (female) [SIO cable side]	Socket connector Strain relief or equivalent	7910-B500FL (3M) 3448-7910 (3M)

RS-232C interface type: when the On Board Writer (S5U1C88000W3) is used

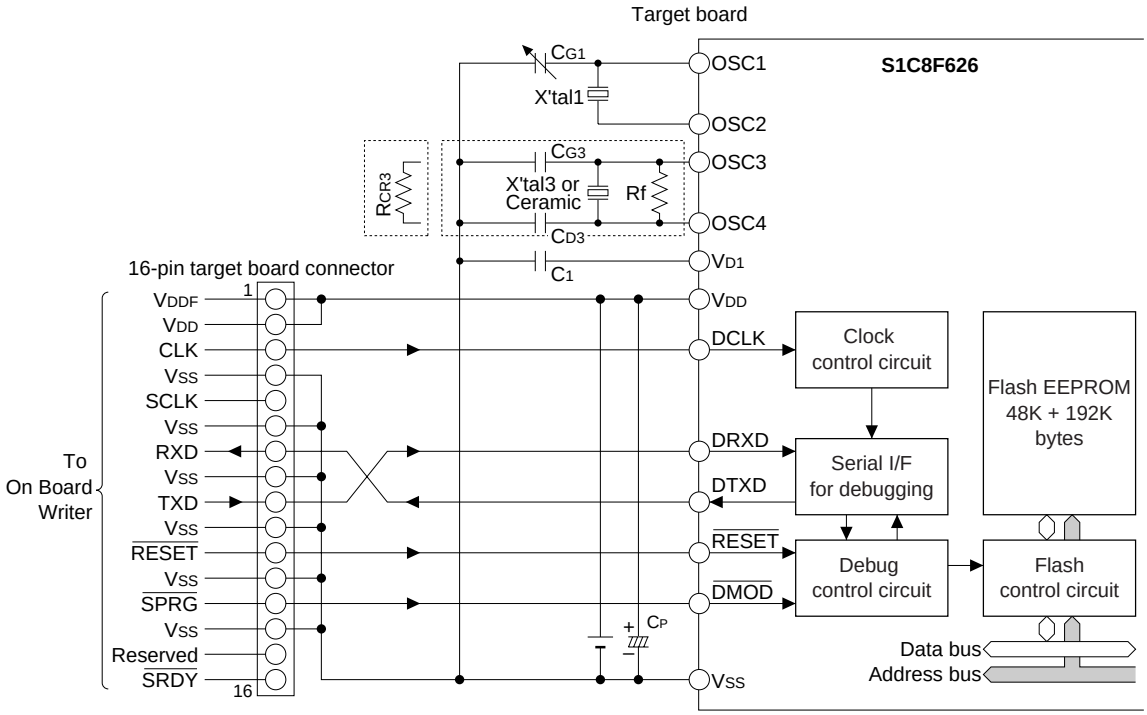


Fig. C.2.4.2 Connection diagram for on-board programming (RS-232C interface type)

Table C.2.4.3 Signal specifications (RS-232C interface type)

Connector pin No.	Signal name	Description	Microcomputer pin to be connected
1	VDDF	Programming power supply pin	VDD pin
2	VDD	Power supply pin	VDD pin
3	CLK	System clock output	DCLK pin
5	SCLK	Reserved	N.C.
7	RXD	Serial I/F data input	DTXD pin
9	TXD	Serial I/F data output	DRXD pin
11	$\overline{\text{RESET}}$	Initial reset output	$\overline{\text{RESET}}$ pin
13	$\overline{\text{SPRG}}$	Programming mode setup output (for negative polarity I/O models)	$\overline{\text{DMOD}}$ pin
15	SPRG	Programming mode setup output (for positive polarity I/O models)	N.C.
16	$\overline{\text{SRDY}}$	Reserved	N.C.
4, 6, 8, 10, 12, 14	Vss	Ground pin	Vss pin

Table C.2.4.4 Connectors for connecting On Board Writer (RS-232C interface type)

Name	Model name	
Box header (male) [target side]	3408-6002LCFL (3M) or equivalent	
Socket connector (female) [SIO cable side]	Socket connector Strain relief or equivalent	7916-B500FL (3M) 3448-7916 (3M)

Notes:
- *Prepare a 3.3-V power supply for PROM programming, since the power (3.3 V) of the On Board Writer must be supplied from the target board.*
- *Since PROM programming uses a 3.3-V power source, be careful of the voltage ratings of the parts on the target board.*

C.2.5 On Board Writer Control Software

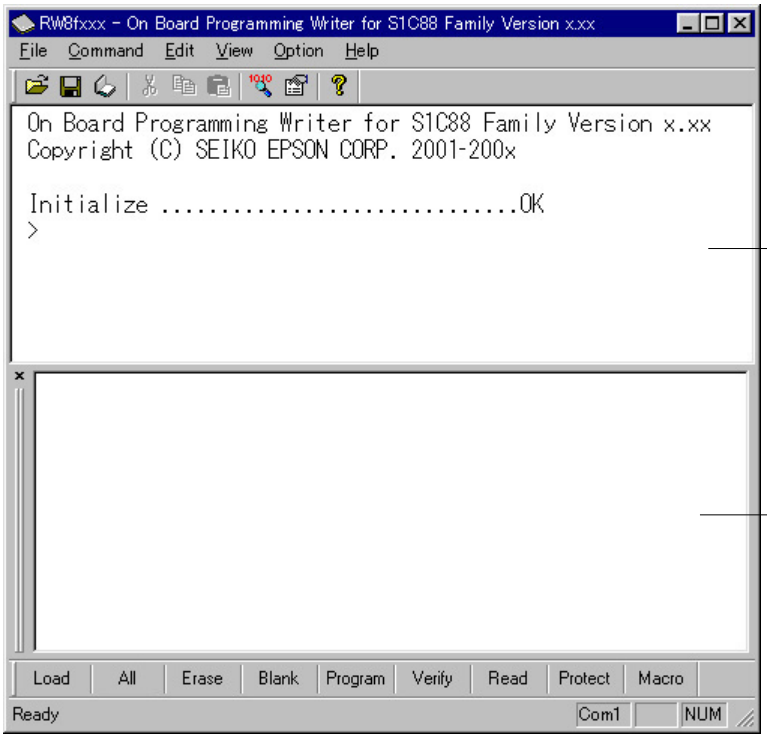
C.2.5.1 Starting up

Double-click the OBPW88.EXE icon to start up the On Board Writer system.

The dialog box shown below appears when the On Board Writer Control Software starts up.

Select the initial file with the same name as the microcomputer model.
RW*xxxxx*.ini *xxxxx*: microcomputer model name (e.g. 8f626 for the S1C8F626)

After an initial file is selected, the window shown below appears.



Command window
Accepts the commands input from the keyboard.

Output window
Displays the execution results.

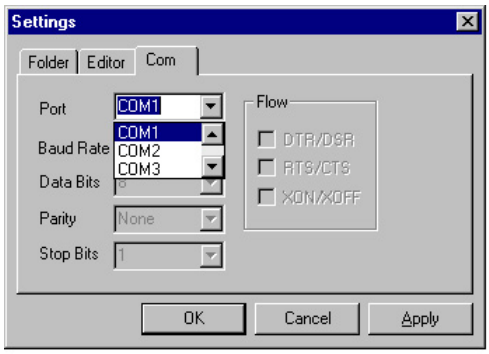
C.2.5.2 Setup

Click the [Setting] button (or choose [Setting] from the [Option] menu) to display the [Settings] dialog box.

 *[Setting] button*

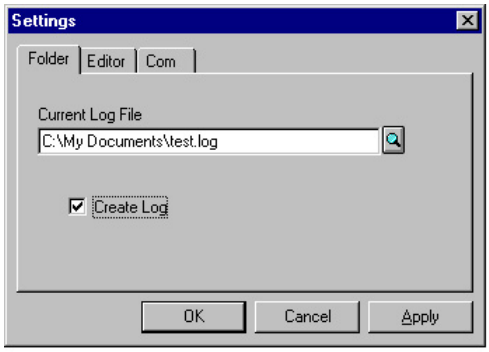
Selecting a serial port ([Com] tab)

When USB-Serial On Board Writer (USB interface type) is used, select the COM port that was assigned to the USB-Serial port (see Step (5) in Section C.2.3). When the On Board Writer (RS-232C interface type) is used, select the COM port to which the RS-232C cable has been connected.



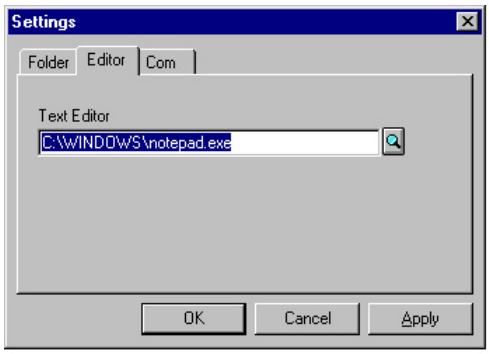
Specifying the log file ([Folder] tab)

When saving the execution results to a log file, enter (or choose) the log file name and place a check in the [Create Log] check box.
To disable logging, remove the check from the check box.



Specifying the editor path ([Editor] tab)

Specify the path to the editor used to open a log file from the On Board Writer Control Software. "notepad.exe" is used as the default editor unless specified.



C.2.5.3 Operating method

All the On Board Writer commands such as PROM programming can be executed using the buttons on the window.
This section explains the commands individually in the following manner.

Function: Shows the command function.

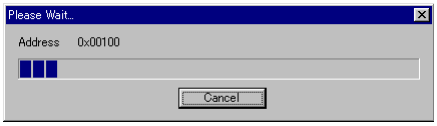
Usage:

Button	Program
Menu	[Command] menu - [Program]
Keyboard	>FW↵

Shows the button, menu command and typing command line to execute the command.

Description: Describes the operation and display contents after executing the command.

If "A progress window appears to show progress of the process." is described here, a progress window is displayed while the command is executing and the [Cancel] button on the window allows termination of the command being executed.



Note: Describes precautions.

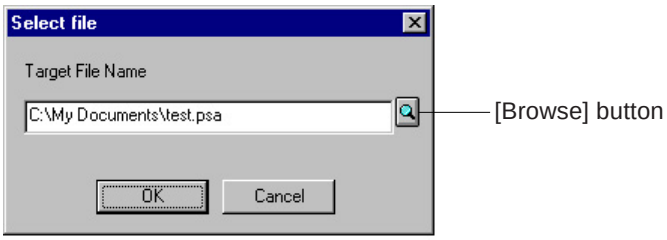
1 LOAD (PSA file)

Function: Loads user data files for PROM (xxxxxx.PSA) to the memory on the personal computer.

Usage:

Button	Load	
Menu	[Command] menu - [Load]	
Keyboard	>L *drive:* \ *folder* \ *file name*↵	*drive:* \ *folder* \ *file name*: PSA file name

Description: (1) The [Select file] dialog box appears.



(2) Clicking the [Browse] button displays the Windows standard file select dialog box. Choose the file to be loaded from the dialog box. Then click the [OK] button.

(3) When data is loaded normally, "Complete" is displayed in the output window.

Note: This command can load files in Motorola S2 format only.

2 ERASE

Function: Erases PROM data.

Usage:

Button	Erase	
Menu	[Command] menu - [Erase]	
Keyboard	>FERS↵	
	>FERS *startAddr endAddr*↵	*startAddr*: start address, hexadecimal
	>FERS *startAddr*↵	*endAddr*: end address, hexadecimal

Description:

(1) An information dialog box appears.

(2) Clicking the [OK] button starts erasing the PROM.

(3) A progress window appears to show progress of the process while the command is executing.
Clicking the [Cancel] button terminates the process.

(4) When the PROM is erased normally, "Complete" is displayed in the output window.

Note:

- When the process is terminated, the PROM must be erased before it can be programmed.
- To erase the PROM in sector units, enter the command with the start and end addresses from the keyboard.
  Erasing must be performed in 4K-byte sector units, therefore, specify a 4K-byte boundary address for the start address. The end address should be specified so that the specified area size will be a multiple of 4K bytes. Otherwise, the entered address is rounded off to a 4K-byte boundary address.
  Example: 2040H is entered → executed as 2000H

  When both the start and end addresses are omitted, the valid address range will be erased. When one address only is entered, it will be assumed as the start address and the range from the specified address to the last valid address will be erased.

3 BLANK CHECK

Function: Checks whether the PROM is completely erased or not.

Usage:

Button: Blank

Menu: [Command] menu - [Blank Check]

Keyboard:

```
>FE↵
>FE startAddr endAddr↵
>FE startAddr↵
```

startAddr: start address, hexadecimal
endAddr: end address, hexadecimal

Description:

(1) Starts a blank check.

(2) A progress window appears to show progress of the process.
Clicking the [Cancel] button terminates the process.

(3) When the check is finished without finding any address that is not erased, "Complete" is displayed in the output window.

(4) If error addresses that have not been erased are found, the address and data are displayed.
Example:

```
Address   READ
   0100   00
   0101   00
   0102   00
   0103   00
     :     :
```

Note:

- When an erase error is detected, the PROM must be erased before it can be programmed.
- To perform erase check for a specified address range, enter the command with the start and end addresses from the keyboard. When the start address only is entered, the range from the specified address to the last valid address will be checked.
  The erase check must be performed in 4K-byte units, therefore, specify a 4K-byte boundary address for the start address. The end address should be specified so that the specified area size will be a multiple of 4K bytes. Otherwise, the entered address is rounded off to a 4K-byte boundary address.
  Example: 2040H is entered → executed as 2000H

4 PROGRAM

Function: Programs the PROM with the data loaded by the [Load] command.

Usage:

Button	Program	
Menu	[Command] menu - [Program]	
Keyboard	>FW↵	
	>FW *startAddr endAddr*↵	*startAddr*: start address, hexadecimal
	>FW *startAddr*↵	*endAddr*: end address, hexadecimal

Description:

(1) An information dialog box appears.

(2) Clicking the [OK] button starts program process.

(3) A progress window appears to show progress of the process.
Clicking the [Cancel] button terminates the process.

(4) When programming is finished normally, "Complete" is displayed in the output window.

Note:

- Do not send the writer control window behind any other applications as it may cause a communication error.
- To program a specified address range, enter the command with the start and end addresses from the keyboard. When the start address only is entered, the range from the specified address to the last valid address will be programmed.
  The PROM programming must be performed in 4K-byte units, therefore, specify a 4K-byte boundary address for the start address. The end address should be specified so that the specified area size will be a multiple of 4K bytes. Otherwise, the entered address is rounded off to a 4K-byte boundary address.
  Example: 2040H is entered → executed as 2000H

5 VERIFY

Function: Compares the data loaded by the [Load] command and the data read from the PROM.

Usage:

Button — Verify

Menu — [Command] menu - [Verify]

Keyboard

>FV↵

>FV *startAddr endAddr*↵ — *startAddr*: start address, hexadecimal

>FV *startAddr*↵ — *endAddr*: end address, hexadecimal

Description:

(1) Starts verification process.

(2) A progress window appears to show progress of the process.
Clicking the [Cancel] button terminates the process.

(3) When both data are the same, "Complete" is displayed in the output window.

(4) When a verify error is detected, the error address and data are displayed.

Note: To verify data in a specified address range, enter the command with the start and end addresses from the keyboard. When the start address only is entered, the range from the specified address to the last valid address will be verified.
Verification must be performed in 4K-byte units, therefore, specify a 4K-byte boundary address for the start address. The end address should be specified so that the specified area size will be a multiple of 4K bytes. Otherwise, the entered address is rounded off to a 4K-byte boundary address.
Example: 2040H is entered → executed as 2000H

6 READ

Function: Reads the PROM data to the memory on the personal computer.

Usage:

Button	Read	
Menu	[Command] menu - [Read]	
Keyboard	>FR↵	
	>FR *startAddr endAddr*↵	*startAddr*: start address, hexadecimal
	>FR *startAddr*↵	*endAddr*: end address, hexadecimal

Description:

(1) An information dialog box appears.

(2) Clicking the [OK] button starts read process.

(3) A progress window appears to show progress of the process.
Clicking the [Cancel] button terminates the process.

(4) When data is read normally, "Complete" is displayed in the output window.

Note:

- The memory data on the personal computer is overwritten with the read data.
- To read data from a specified address range, enter the command with the start and end addresses from the keyboard. When the start address only is entered, data within the range from the specified address to the last valid address will be read.
  Reading must be performed in 4K-byte units, therefore, specify a 4K-byte boundary address for the start address. The end address should be specified so that the specified area size will be a multiple of 4K bytes. Otherwise, the entered address is rounded off to a 4K-byte boundary address.
  Example: 2040H is entered → executed as 2000H

7 PROTECT

Function: Protects the PROM from read out.

Usage:

	Button	Protect
	Menu	[Command] menu - [Protect]
	Keyboard	>FPROTECT↵

Description:
(1) An information dialog box appears.
(2) Clicking the [OK] button starts protect process.
(3) When the process is finished normally, "Complete" is displayed in the output window.

Note: When the PROM is protected, execution of all the commands except "Erase" are disabled.

8 MACRO

Function: Successively executes the commands described in a macro file.

Usage:

Button	Macro
Menu	[Command] menu - [Macro]
Keyboard	None

Description:

(1) A file-select dialog box appears.

(2) Select a macro file and then click the [OK] button. The macro file will be loaded and the described commands will be executed.

Macro file: Use a text editor to create macro files. ".CMD" is recommended for the file extension. Write the commands in order of execution and save as a text file. The command should be written one line by one line in the command line format listed at Usage: Keyboard. Any words following a ";" are regarded as a comment.

Example: Macro file <TEST.CMD>

```
L D:\WORK\C8Fxxx.PSA      Load PROM HEX file
FERS                      Erase PROM data
FE                        PROM blank check
FW                        Program PROM
FV                        PROM verify check
;--- PROTECT---           Comment
FPROTECT                  Read protect
```

9 ALL

Function: Erases PROM data, programs and sets protection sequentially.

Usage:

Button	All
Menu	None
Keyboard	None

Description:

(1) An information dialog box appears.

(2) Clicking the [OK] button starts the sequence of erasing, programming the PROM and setting protection.

(3) A progress window appears to show progress of the process while the command is executing. Clicking the [Cancel] button terminates the process.

(4) When the process is finished normally, "Complete" is displayed in the output window.

Note: When the process is terminated, execute the All or Erase command again.

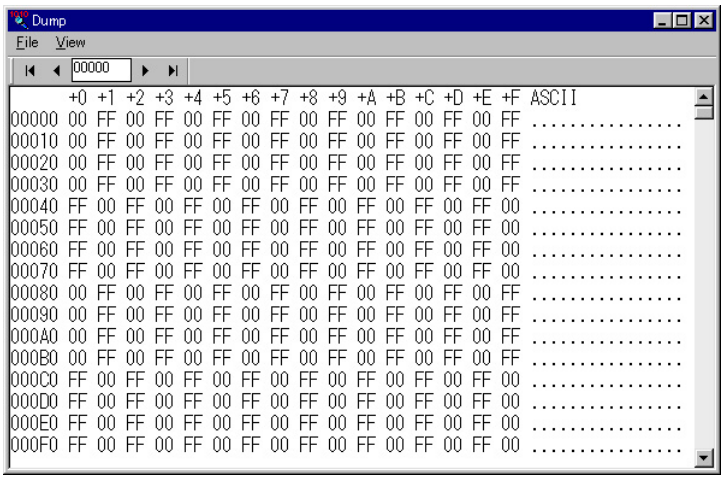
10 DUMP

Function: Displays the contents of the PC memory PROM area in hexadecimal numbers. The memory contents can be edited in the [Dump] window.

Usage:

Button	[Dump] button
Menu	[Command] menu - [Dump]
Keyboard	>D↵
	>D *address*↵ *address*: display start address

Description: (1) The [Dump] window appears.



Displays the last page.
Displays the next page.
Display start address is specified.
Displays the previous page.
Displays the top page.

(2) To edit the memory contents, enter a value after placing the cursor on the address to be edited.

11 OPEN LOG FILE

Function: Opens a log file.

Usage:

Button	 [Open Log file] button
Menu	[File] menu - [Open Log File]
Keyboard	None

Description: The specified editor starts up and opens the specified log file.
The editor and the log file must be specified beforehand in the [Editor] tab screen of the [Settings] dialog box and the [Folder] tab screen, respectively.

12 SAVE

Function: Saves the PROM data stored in the PC memory to a file.

Usage:

Button	 [Save] button
Menu	[File] menu - [Save to PSA]
Keyboard	>S *drive:**folder**file name*↵ (*drive:**folder**file name*: PSA file name)

Description:

(1) The Windows standard file select dialog box appears. Choose or enter the file name for saving data.

(2) The contents in the PC memory PROM area are saved to Motorola S2 format files (*.PSA).

C.2.6 List of commands

Table C.2.6.1 List of commands

No.	Command line	Menu	Button	Function
1	`L` *drive\folder\file name*↵	[Command]-[Load]	Load	Load PSA file
2	`FERS` (*startAddr* (*endAddr*))↵	[Command]-[Erase]	Erase	Erase PROM data
3	`FE` (*startAddr* (*endAddr*))↵	[Command]-[Blank Check]	Blank	PROM blank check
4	`FW` (*startAddr* (*endAddr*))↵	[Command]-[Program]	Program	Program PROM
5	`FV` (*startAddr* (*endAddr*))↵	[Command]-[Verify]	Verify	Verify PROM
6	`FR` (*startAddr* (*endAddr*))↵	[Command]-[Read]	Read	Read PROM data
7	`FPROTECT`↵	[Command]-[Protect]	Protect	Read-protect PROM
8	–	[Command]-[Macro]	Macro	Read/execute macro file
9	–	–	All	Erase/program/protect PROM
10	`D` (*address*)↵	[Command]-[Dump]		Dump PROM data
11	–	[File]-[Open Log File]		Open log file
12	`S` *drive\folder\file name*↵	[File]-[Save to PSA]		Save PROM data
13	`LOG`↵	–		Start logging
14	`LOG /E`↵	–		End logging

( ) indicates command options.

C.2.7 List of error messages

Table C.2.7.1 List of error messages

Error message	Description
Command timeout	Communication time out
Receive NAK	Communication error
Send error	Communication error
COM Port Open Error	Port open error
Invalid File Format	The file is not a Motorola S2 format file.
Data Size Over flow	The data size in the file exceeds the PROM size.
Verify Error	Verify error
Protected Error	The PROM has read-protected.
Abort by operator	The process is terminated.
Complete	The process is terminated normally.

APPENDIX D DIFFERENCES FROM S1C88649/650

The S1C8F626 is compatible with the major functions of the S1C88649 / 650. Table D.1 lists the differences from the S1C88649 / 650.

Table D.1 List of differences

Function	S1C88649	S1C88650	S1C8F626
Operating frequency	30 kHz to 4.2 MHz	30 kHz to 8.2 MHz	30 kHz to 8.2 MHz
Internal ROM capacity	48K + 192K bytes	48K + 896K bytes	48K + 192K bytes
Internal RAM capacity	8K bytes	8K bytes	8K bytes
Sound generator	Available	Not available (Can be substituted with Programmable timer)	Not available (Can be substituted with Programmable timer)
Programmable timer	1 ch. (PWM)	2 ch. (PWM)	2 ch. (PWM)
Stopwatch timer	Available	Not available	Available
Serial interface	1 ch.	1 ch. (2-bit parity, LSB/MSB first selectable)	2 ch. (2-bit parity, LSB/MSB first selectable)
IrDA interface	Not available	Not available	Available
Multiple-key entry reset	Mask option	Mask option	Register control
Watchdog timer reset period	Fixed at 3 to 4-second period	Mask option	Fixed at 4-second period
LCD driver	80 SEG × 16/8 COM	126 SEG × 32/16/8 COM	96 SEG × 32/16/8 COM
SEG assignment reverse function	Not available	Available	Available
12 × 12-dot font select function	Not available	Available	Available
LCD power supply	1/4 bias	1/5 bias (V_{DD} booster built in)	1/5 bias (V_{DD} booster built in)
Input interface level select function	P10–17 (Mask option)	K00–07, P10–17 (Mask option)	K00–07, P10–17, P20–27 (Register control)
Supporting OSC3 source clock by chattering elimination circuit	Not available (OSC1 source clock only)	Available	Available
K port	K00–07	K00–07	K00–07
P port	P00–07, P10–17	P00–07, P10–17	P00–07, P10–17, P20–27
R port	R00–07, R10–17, R20–24, R30–33	R00–07, R10–17, R20–24, R30–33	Not available
External bus	512K bytes × 4	1M bytes × 3	Not available
Shipping form	Chip	Chip, QFP22-256pin	Chip, VFBGA10H-240pin, QFP21-216pin
Current consumption			
SLEEP mode	1 µA (Typ.)	1 µA (Typ.)	1 µA (Typ.)
HALT mode (32 kHz crystal)	2.5 µA (Typ.)	2.5 µA (Typ.)	2.5 µA (Typ.)
Run state (32 kHz crystal)	7 µA (Typ.)	9 µA (Typ.)	10 µA (Typ.)
Run state (8 MHz ceramic)	670 µA@4 MHz (Typ.)	1700 µA (Typ.)	1800 µA (Typ.)

∗ The S1C8F626 is upwardly compatible with the S1C88649 and S1C88650.

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

HEADQUARTERS
2580 Orchard Parkway
San Jose, CA 95131, U.S.A.
Phone: +1-800-228-3964 Fax: +1-408-922-0238

SALES OFFICE
Northeast
301 Edgewater Place, Suite 210
Wakefield, MA 01880, U.S.A.
Phone: +1-800-922-7667 Fax: +1-781-246-5443

EUROPE

EPSON EUROPE ELECTRONICS GmbH

HEADQUARTERS
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-89-14005-0 Fax: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
23F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: +86-10-6410-6655 Fax: +86-10-6410-7320

SHANGHAI BRANCH
7F, High-Tech Bldg., 900, Yishan Road
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 Fax: +86-21-5423-5512

EPSON HONG KONG LTD.
20/F, Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON Electronic Technology Development (Shenzhen) LTD.
12/F, Dawning Mansion, Keji South 12th Road
Hi- Tech Park, Shenzhen
Phone: +86-755-2699-3828 Fax: +86-755-2699-3838

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road
Taipei 110
Phone: +886-2-8786-6688 Fax: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 Fax: +65-6271-3182

SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 Fax: +82-2-767-3677

GUMI OFFICE
2F, Grand B/D, 457-4 Songjeong-dong
Gumi-City, KOREA
Phone: +82-54-454-6027 Fax: +82-54-454-6093

SEIKO EPSON CORPORATION
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 Fax: +81-42-587-5117

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SEIKO EPSON CORPORATION
SEMICONDUCTOR OPERATIONS DIVISION

■ EPSON Electronic Devices Website

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