**EPSON**

## LCD Controller ICs
# S1D13305 Series
# Technical Manual

ENERGY SAVING EPSON

**SEIKO EPSON CORPORATION**

# The information of the product number change

Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

# Configuration of product number

● Devices

```
S1    D    13706    F    00A0    00
```
- Packing specification
- Specification
- Package (B: CSP, F: QFP)
- Corresponding model number
- Model name (D: driver, digital products)
- Product classification (S1: semiconductor)

● Evaluation Board

```
S5U    13705    P00C
```
- Specification
- Corresponding model number (13705: for S1D13705)
- Product classification (S5U: development tool for semiconductor)
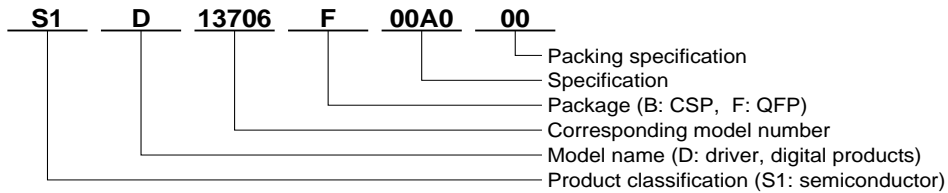
# Comparison table between new and previous number

• S1D13305 Series

| Previous No. | New No. |
|---|---|
| SED1335 Series | S1D13305 Series |
| SED1335D0A | S1D13305D00A |
| SED1335F0A | S1D13305F00A |
| SED1335F0B | S1D13305F00B |

• S1D1350x Series

| Previous No. | New No. |
|---|---|
| SED135x Series | S1D1350x Series |
| SED1353D0A | S1D13503D00A |
| SED1353F0A | S1D13503F00A |
| SED1353F1A | S1D13503F01A |
| SED1354F0A | S1D13504F00A |
| SED1354F1A | S1D13504F01A |
| SED1354F2A | S1D13504F02A |
| SED1355F0A | S1D13505F00A |
| SED1356F0A | S1D13506F00A |

• S1D1370x Series

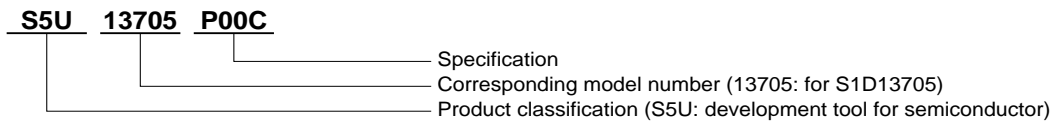| Previous No. | New No. |
|---|---|
| SED137x Series | S1D1370x Series |
| SED1374F0A | S1D13704F00A |
| SED1375F0A | S1D13705F00A |
| SED1376B0A | S1D13706B00A |
| SED1376F0A | S1D13706F00A |
| SED1378 Series | S1D13708 Series |

• S1D13A0x Series

| Previous No. | New No. |
|---|---|
| SED13Ax Series | S1D13A0x Series |
| SED13A3F0A | S1D13A03F00A |
| SED13A3B0B | S1D13A03B00B |
| SED13A4B0B | S1D13A04B00B |

• S1D1380x Series

| Previous No. | New No. |
|---|---|
| SED138x Series | S1D1380x Series |
| SED1386F0A | S1D13806F00A |

# Comparison table between new and previous number of Evaluation Boards

• S1D1350x Series

| Previous No. | New No. |
|---|---|
| SDU1353#0C | S5U13503P00C |
| SDU1354#0C | S5U13504P00C |
| SDU1355#0C | S5U13505P00C |
| SDU1356#0C | S5U13506P00C |

• S1D1370x Series

| Previous No. | New No. |
|---|---|
| SDU1374#0C | S5U13704P00C |
| SDU1375#0C | S5U13705P00C |
| SDU1376#0C | S5U13706P00C |
| SDU1376BVR | S5U13706B32R |
| SDU1378#0C | S5U13708P00C |

• S1D13A0x Series

| Previous No. | New No. |
|---|---|
| SDU13A3#0C | S5U13A03P00C |
| SDU13A4#0C | S5U13A04P00C |

• S1D1380x Series

| Previous No. | New No. |
|---|---|
| SDU1386#0C | S5U13806P00C |

# CONTENTS

# 1. OVERVIEW

The S1D13305 series is a controller IC that can display text and graphics on LCD panel.

The S1D13305 series can display layered text and graphics, scroll the display in any direction and partition the display into multiple screens.

The S1D13305 series stores text, character codes and bit-mapped graphics data in external frame buffer memory. Display controller functions include transferring data from the controlling microprocessor to the buffer memory, reading memory data, converting data to display pixels and generating timing signals for the buffer memory, LCD panel.

The S1D13305 series has an internal character generator with 160, $5 \times 7$ pixel characters in internal mask ROM. The character generators support up to 64, $8 \times 16$ pixel characters in external character generator RAM and up to 256, $8 \times 16$ pixel characters in external character generator ROM.

# 2. FEATURES

- Text, graphics and combined text/graphics display modes
- Three overlapping screens in graphics mode
- Up to $640 \times 256$ pixel LCD panel display resolution
- Programmable cursor control
- Smooth horizontal and vertical scrolling of all or part of the display
- 1/2-duty to 1/256-duty LCD drive
- Up to $640 \times 256$ pixel LCD panel display resolution memory
- 160, $5 \times 7$ pixel characters in internal mask-programmed character generator ROM
- Up to 64, $8 \times 16$ pixel characters in external character generator RAM
- Up to 256, $8 \times 16$ pixel characters in external character generator ROM
- 6800 and 8080 family microprocessor interfaces
- Low power consumption—3.5 mA operating current ($V_{DD} = 3.5V$), 0.05 µA standby current
- Package

| line-up | Package |
|---|---|
| S1D13305F00A | QFP5-60 pin |
| S1D13305F00B | QFP6-60 pin |

- 2.7 to 5.5 V (S1D13305F)

# 3. BLOCK DIAGRAM

**EPSON**
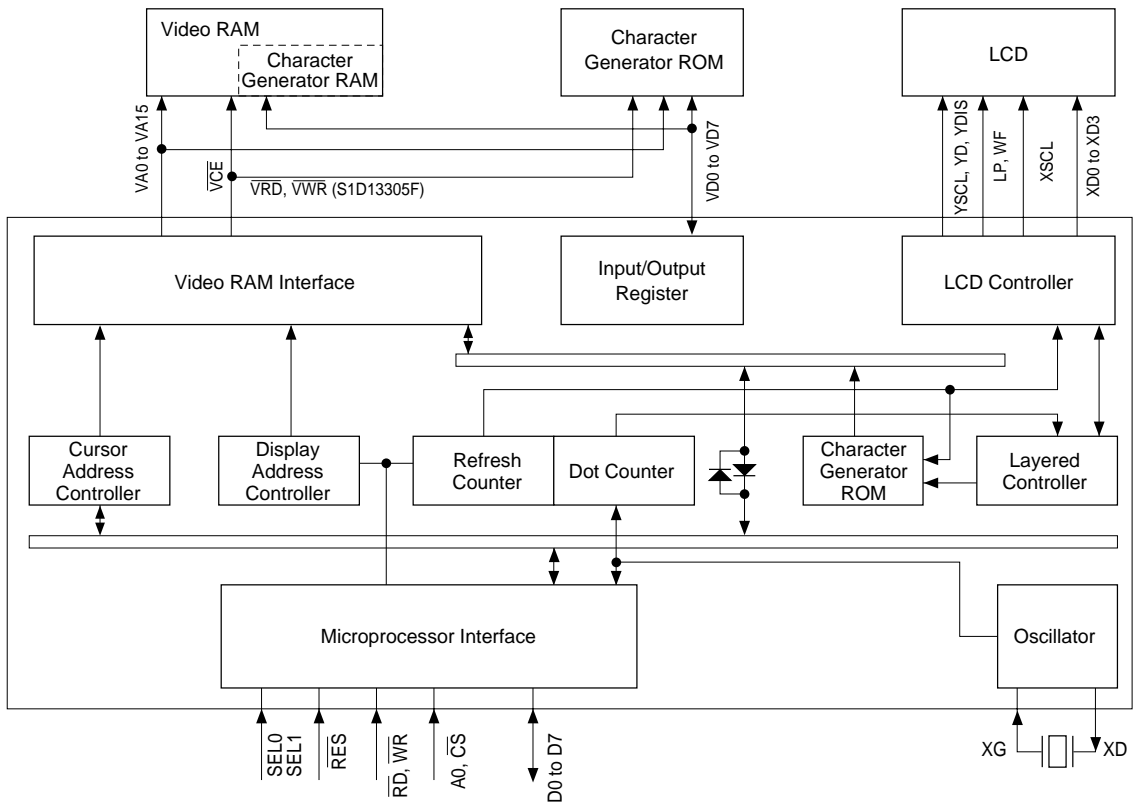
# 4.  PINOUTS
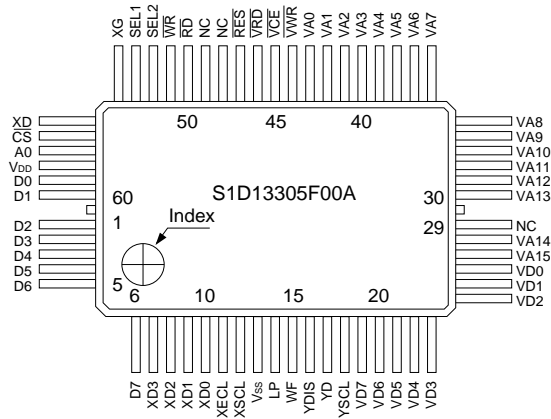
◊S1D13305F00A                                              ◊S1D13305F00B
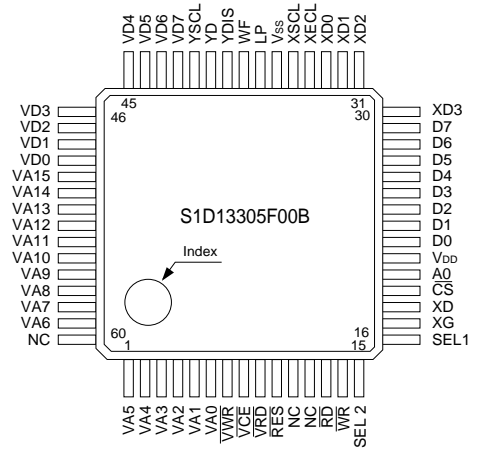
# 5. PIN DESCRIPTION
## 5.1. S1D13305F00A/00B Pin Summary

| Name | Number | | Type | Description |
| --- | --- | --- | --- | --- |
| | S1D13305F00A | S1D13305F00B | | |
| VA0 to VA15 | 27 to 28<br>30 to 43 | 1 to 6<br>50 to 59 | Output | VRAM address bus |
| $\overline{\text{VWR}}$ | 44 | 7 | Output | VRAM write signal |
| $\overline{\text{VCE}}$ | 45 | 8 | Output | Memory control signal |
| $\overline{\text{VRD}}$ | 46 | 9 | Output | VRAM read signal |
| $\overline{\text{RES}}$ | 47 | 10 | Input | Reset |
| NC | 28, 48, 49 | 11, 12, 60 | — | No connection |
| $\overline{\text{RD}}$ | 50 | 13 | Input | 8080 family: Read signal<br>6800 family: Enable clock (E) |
| $\overline{\text{WR}}$ | 51 | 14 | Input | 8080 family: Write signal<br>6800 family: R/$\overline{\text{W}}$ signal |
| SEL2 | 52 | 15 | Input | 8080 or 6800 family interface select |
| SEL1 | 53 | 16 | Input | 8080 or 6800 family interface select |
| XG | 54 | 17 | Input | Oscillator connection |
| XD | 55 | 18 | Output | Oscillator connection |
| $\overline{\text{CS}}$ | 56 | 19 | Input | Chip select |
| A0 | 57 | 20 | Input | Data type select |
| VDD | 58 | 21 | Supply | 2.7 to 5.5V supply |
| D0 to D7 | 59 to 60<br>1 to 6 | 22 to 29 | Input/output | Data bus |
| XD0 to XD3 | 7 to 10 | 30 to 33 | Output | X-driver data |
| XECL | 11 | 34 | Output | X-driver enable chain clock |
| XSCL | 12 | 35 | Output | X-driver data shift clock |
| VSS | 13 | 36 | Supply | Ground |
| LP | 14 | 37 | Output | Latch pulse |
| WF | 15 | 38 | Output | Frame signal |
| YDIS | 16 | 39 | Output | Power-down signal when display is blanked |
| YD | 17 | 40 | Output | Scan start pulse |
| YSCL | 18 | 41 | Output | Y-driver shift clock |
| VD0 to VD7 | 19 to 26 | 42 to 49 | Input/output | VRAM data bus |

## 5.2. Pin Functions

### 5.2.1. Power supply

| Pin Name | Function |
|---|---|
| VDD | 2.7 to 5.5V supply.<br>This may be the same supply as the controlling microprocessor. |
| VSS | Ground |

**Note:** The peak supply current drawn by the S1D13305 series may be up to ten times the average supply current. The power supply impedance must be kept as low as possible by ensuring that supply lines are sufficiently wide and by placing 0.47 μF decoupling capacitors that have good high-frequency response near the device's supply pins.

### 5.2.2. Oscillator

| Pin Name | Function |
|---|---|
| XG | Crystal connection for internal oscillator (See section 13). This pin can be driven by an external clock source that satisfies the timing specifications of the EXT $\phi$0 signal (See section 6.3.6). |
| XD | Crystal connection for internal oscillator. Leave this pin open when using an external clock source. |

### 5.2.3. Microprocessor interface

| Pin Name | Function |
|---|---|
| D0 to D7 | Tristate input/output pins. Connect these pins to an 8- or 16-bit microprocessor bus. |
| SEL1, SEL2 | Microprocessor interface select pin. The S1D13305 series supports both 8080 family processors (such as the 8085 and Z80®) and 6800 family processors (such as the 6802 and 6809). |

| SEL1 | SEL2* | Interface | A0 | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 8080 family | A0 | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ |
| 1 | 0 | 6800 family | A0 | E | R/$\overline{W}$ | $\overline{CS}$ |

**Note:** SEL1 should be tied directly to VDD or VSS to prevent noise. If noise does appear on SEL1, decouple it to ground using a capacitor placed as close to the pin as possible.

| Pin Name | Function | | | |
|---|---|---|---|---|
| A0 | **8080 family interface** | | | |
| | A0 | $\overline{\text{RD}}$ | $\overline{\text{WR}}$ | Function |
| | 0 | 0 | 1 | Status flag read |
| | 1 | 0 | 1 | Display data and cursor address read |
| | 0 | 1 | 0 | Display data and parameter write |
| | 1 | 1 | 0 | Command write |
| | **6800 family interface** | | | |
| | A0 | R/$\overline{\text{W}}$ | E | Function |
| | 0 | 1 | 1 | Status flag read |
| | 1 | 1 | 1 | Display data and cursor address read |
| | 0 | 0 | 1 | Display data and parameter write |
| | 1 | 0 | 1 | Command write |
| $\overline{\text{RD}}$ or E | When the 8080 family interface is selected, this signal acts as the active-LOW read strobe. The S1D13305 series output buffers are enabled when this signal is active. | | | |
| | When the 6800 family interface is selected, this signal acts as the active-HIGH enable clock. Data is read from or written to the S1D13305 series when this clock goes HIGH. | | | |
| $\overline{\text{WR}}$ or R/$\overline{\text{W}}$ | When the 8080 family interface is selected, this signal acts as the active-LOW write strobe. The bus data is latched on the rising edge of this signal. | | | |
| | When the 6800 family interface is selected, this signal acts as the read/write control signal. Data is read from the S1D13305 series if this signal is HIGH, and written to the S1D13305 series if it is LOW. | | | |
| $\overline{\text{CS}}$ | Chip select. This active-LOW input enables the S1D13305 series. It is usually connected to the output of an address decoder device that maps the S1D13305 series into the memory space of the controlling microprocessor. | | | |
| $\overline{\text{RES}}$ | This active-LOW input performs a hardware reset on the S1D13305 series. It is a Schmitt-trigger input for enhanced noise immunity; however, care should be taken to ensure that it is not triggered if the supply voltage is lowered. | | | |

## 5.2.4. Display memory control

The S1D13305 series can directly access static RAM and PROM. The designer may use a mixture of these two types of memory to achieve an optimum trade-off between low cost and low power consumption.

| Pin Name | Function |
|---|---|
| VA0 to VA15 | 16-bit display memory address. When accessing character generator RAM or ROM, VA0 to VA3, reflect the lower 4 bits of the S1D13305 series's row counter. |
| VD0 to VD7 | 8-bit tristate display memory data bus. These pins are enabled when VR/$\overline{\text{W}}$ is LOW. |
| $\overline{\text{VWR}}$ | Active-LOW display memory write control output. |
| $\overline{\text{VRD}}$ | Active-LOW display memory read control output. |
| $\overline{\text{VCE}}$ | Active-LOW static memory standby control signal. $\overline{\text{VCE}}$ can be used with $\overline{\text{CS}}$. |

### 5.2.5. LCD drive signals

In order to provide effective low-power drive for LCD matrixes, the S1D13305 series can directly control both the X- and Y-drivers using an enable chain.

| Pin Name | Function |
|---|---|
| XD0 to XD3 | 4-bit X-driver (column drive) data outputs. Connect these outputs to the inputs of the X-driver chips. |
| XSCL | The falling edge of XSCL latches the data on XD0 to XD3 into the input shift registers of the X-drivers. To conserve power, this clock halts between LP and the start of the following display line (See section 6.3.7). |
| XECL | The falling edge of XECL triggers the enable chain cascade for the X-drivers. Every 16th clock pulse is output to the next X-driver. |
| LP | LP latches the signal in the X-driver shift registers into the output data latches. LP is a falling-edge triggered signal, and pulses once every display line. Connect LP to the Y-driver shift clock on modules. |
| WF | LCD panel AC drive output. The WF period is selected to be one of two values with SYSTEM SET command. |
| YSCL | The falling edge of YSCL latches the data on YD into the input shift registers of the Y-drivers. YSCL is not used with driver ICs which use LP as the Y-driver shift clock. |
| YD | YD is the data pulse output for the Y drivers. It is active during the last line of each frame, and is shifted through the Y drivers one by one (by YSCL), to scan the display's common connections. |
| YDIS | Power-down output signal. YDIS is HIGH while the display drive outputs are active. YDIS goes LOW one or two frames after the sleep command is written to the S1D13305 series. All Y-driver outputs are forced to an intermediate level (de-selecting the display segments) to blank the display. In order to implement power-down operation in the LCD unit, the LCD power drive supplies must also be disabled when the display is disabled by YDIS. |

# 6. SPECIFICATIONS

## 6.1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{DD}$ | −0.3 to 7.0 | V |
| Input voltage range | $V_{IN}$ | −0.3 to $V_{DD}$ + 0.3 | V |
| Power dissipation | $P_D$ | 300 | mW |
| Operating temperature range | $T_{opg}$ | −20 to 75 | °C |
| Storage temperature range | $T_{stg}$ | −65 to 150 | °C |
| Soldering temperature (10 seconds). See note 1. | $T_{solder}$ | 260 | °C |

**Notes:**

1. The humidity resistance of the flat package may be reduced if the package is immersed in solder. Use a soldering technique that does not heatstress the package.

2. If the power supply has a high impedance, a large voltage differential can occur between the input and supply voltages. Take appropriate care with the power supply and the layout of the supply lines. (See section 6.2.)

3. All supply voltages are referenced to $V_{SS}$ = 0V.

## 6.2. S1D13305

$V_{DD}$ = 4.5 to 5.5V, $V_{SS}$ = 0V, $T_a$ = −20 to 75°C

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Supply voltage | $V_{DD}$ | | 4.5 | 5.0 | 5.5 | V |
| Register data retention voltage | $V_{OH}$ | | 2.0 | — | 6.0 | V |
| Input leakage current | $I_{LI}$ | $V_I = V_{DD}$. See note 5. | — | 0.05 | 2.0 | μA |
| Output leakage current | $I_{LO}$ | $V_I = V_{SS}$. See note 5. | — | 0.10 | 5.0 | μA |
| Operating supply current | $I_{opr}$ | See note 4. | — | 11 | 15 | mA |
| Quiescent supply current | $I_Q$ | Sleep mode, $V_{OSC1} = V_{\overline{CS}} = V_{\overline{RD}} = V_{DD}$ | — | 0.05 | 20.0 | μA |
| Oscillator frequency | $f_{OSC}$ | Measured at crystal, 47.5% duty cycle. See note 6. | 1.0 | — | 10.0 | MHz |
| External clock frequency | $f_{CL}$ | | 1.0 | — | 10.0 | MHz |
| Oscillator feedback resistance | $R_f$ | | 0.5 | 1.0 | 3.0 | MΩ |
| **TTL** | | | | | | |
| HIGH-level input voltage | $V_{IHT}$ | See note 1. | $0.5V_{DD}$ | — | $V_{DD}$ | V |
| LOW-level input voltage | $V_{ILT}$ | See note 1. | $V_{SS}$ | — | $0.2V_{DD}$ | V |
| HIGH-level output voltage | $V_{OHT}$ | $I_{OH}$ = −5.0 mA. See note 1. | 2.4 | — | — | V |
| LOW-level output voltage | $V_{OLT}$ | $I_{OL}$ = 5.0 mA. See note 1. | — | — | $V_{SS} + 0.4$ | V |
| **CMOS** | | | | | | |
| HIGH-level input voltage | $V_{IHC}$ | See note 2. | $0.8V_{DD}$ | — | $V_{DD}$ | V |
| LOW-level input voltage | $V_{ILC}$ | See note 2. | $V_{SS}$ | — | $0.2V_{DD}$ | V |
| HIGH-level output voltage | $V_{OHC}$ | $I_{OH}$ = −2.0 mA. See note 2. | $V_{DD} - 0.4$ | — | — | V |
| LOW-level output voltage | $V_{OLC}$ | $I_{OH}$ = 1.6 mA. See note 2. | — | — | $V_{SS} + 0.4$ | V |
| **Open-drain** | | | | | | |
| LOW-level output voltage | $V_{OLN}$ | $I_{OL}$ = 6.0 mA. | — | — | $V_{SS} + 0.4$ | V |
| **Schmitt-trigger** | | | | | | |
| Rising-edge threshold voltage | $V_{T+}$ | See note 3. | $0.5V_{DD}$ | $0.7V_{DD}$ | $0.8V_{DD}$ | V |
| Falling-edge threshold voltage | $V_{T-}$ | See note 3. | $0.2V_{DD}$ | $0.3V_{DD}$ | $0.5V_{DD}$ | V |

**Notes:**

1. D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, $\overline{VRD}$, $\overline{VWR}$ and $\overline{VCE}$ are TTL-level inputs.

2. SEL1 is CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS are CMOS-level outputs.

3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200 μs. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.

4. $f_{OSC}$ = 10 MHz, no load (no display memory), internal character generator, 256 × 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.

5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.

6. Because the oscillator circuit input bias current is in the order of μA, design the printed circuit board so as to reduce leakage currents.

$V_{DD}$ = 2.7 to 4.5 V, $V_{SS}$ = 0 V, Ta = –20 to 75°C unless otherwise noted

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Supply voltage | $V_{DD}$ | | 2.7 | 3.5 | 4.5 | V |
| Register data retention voltage | $V_{OH}$ | | 2.0 | — | 6.0 | V |
| Input leakage current | $I_{LI}$ | $V_I$ = $V_{DD}$. See note 5. | — | 0.05 | 2.0 | μA |
| Output leakage current | $I_{LO}$ | $V_I$ = $V_{SS}$. See note 5. | — | 0.10 | 5.0 | μA |
| Operating supply current | $I_{opr}$ | $V_{DD}$ = 3.5 V. See note 4. | — | 3.5 | — | mA |
| | | See note 4. | — | — | 7.0 | |
| Quiescent supply current | $I_Q$ | Sleep mode, $V_{OSC1}$ = $V_{\overline{CS}}$ = $V_{\overline{RD}}$ = $V_{DD}$ | — | 0.05 | 20.0 | μA |
| Oscillator frequency | $f_{OSC}$ | Measured at crystal, | 1.0 | — | 8.0 | MHz |
| External clock frequency | $f_{CL}$ | 47.5% duty cycle. | 1.0 | — | 8.0 | MHz |
| Oscillator feedback resistance | $R_f$ | See note 6. | 0.7 | — | 3.0 | MΩ |
| **TTL** | | | | | | |
| HIGH-level input voltage | $V_{IHT}$ | See note 1. | 0.5 $V_{DD}$ | — | $V_{DD}$ | V |
| LOW-level input voltage | $V_{ILT}$ | See note 1. | $V_{SS}$ | — | 0.2 $V_{DD}$ | V |
| HIGH-level output voltage | $V_{OHT}$ | $I_{OH}$ = –3.0 mA. See note 1. | 2.4 | — | — | V |
| LOW-level output voltage | $V_{OLT}$ | $I_{OL}$ = 3.0 mA. See note 1. | — | — | $V_{SS}$ + 0.4 | V |
| **CMOS** | | | | | | |
| HIGH-level input voltage | $V_{IHC}$ | See note 2. | 0.8 $V_{DD}$ | — | $V_{DD}$ | V |
| LOW-level input voltage | $V_{ILC}$ | See note 2. | $V_{SS}$ | — | 0.2 $V_{DD}$ | V |
| HIGH-level output voltage | $V_{OHC}$ | $I_{OH}$ = –2.0 mA. See note 2. | $V_{DD}$ – 0.4 | — | — | V |
| LOW-level output voltage | $V_{OLC}$ | $I_{OH}$ = 1.6 mA. See note 2. | — | — | $V_{SS}$ + 0.4 | V |
| **Open-drain** | | | | | | |
| LOW-level output voltage | $V_{OLN}$ | $I_{OL}$ = 6.0 mA. | — | — | $V_{SS}$ + 0.4 | V |
| **Schmitt-trigger** | | | | | | |
| Rising-edge threshold voltage | $V_{T+}$ | See note 3. | 0.5 $V_{DD}$ | 0.7 $V_{DD}$ | 0.8 $V_{DD}$ | V |
| Falling-edge threshold voltage | $V_{T-}$ | See note 3. | 0.2 $V_{DD}$ | 0.3 $V_{DD}$ | 0.5 $V_{DD}$ | V |

**Notes**

1. D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, $\overline{VRD}$, $\overline{VWR}$ and $\overline{VCE}$ are TTL-level inputs.

2. SEL1 is CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS are CMOS-level outputs.

3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200 μs. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.

4. $f_{OSC}$ = 10 MHz, no load (no display memory), internal character generator, 256 × 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.

5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.

6. Because the oscillator circuit input bias current is in the order of μA, design the printed circuit board so as to reduce leakage currents.

## 6.3. S1D13305F Timing Diagrams

### 6.3.1. 8080 family interface timing
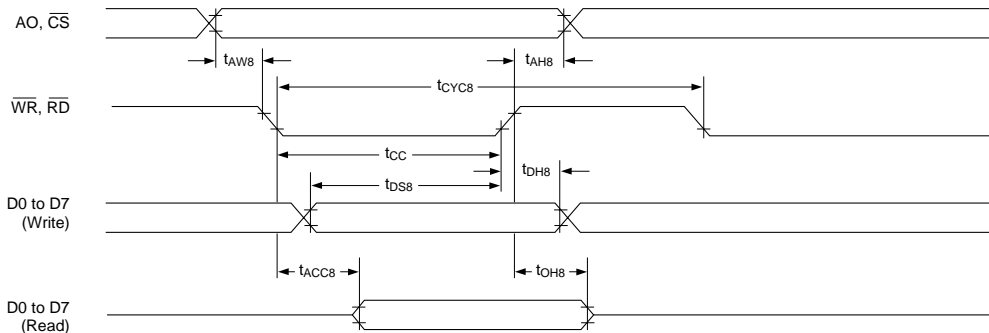


Ta = −20 to 75°C

| Signal | Symbol | Parameter | VDD = 4.5 to 5.5V | | VDD = 2.7 to 4.5V | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| A0, $\overline{CS}$ | tAH8 | Address hold time | 10 | — | 10 | — | ns | CL = 100pF |
| | tAW8 | Address setup time | 0 | — | 0 | — | ns | |
| $\overline{WR}$, $\overline{RD}$ | tCYC8 | System cycle time | See note. | — | See note. | — | ns | |
| | tCC | Strobe pulsewidth | 120 | — | 150 | — | ns | |
| D0 to D7 | tDS8 | Data setup time | 120 | — | 120 | — | ns | |
| | tDH8 | Data hold time | 5 | — | 5 | — | ns | |
| | tACC8 | $\overline{RD}$ access time | — | 50 | — | 80 | ns | |
| | tOH8 | Output disable time | 10 | 50 | 10 | 55 | ns | |

**Note:** For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

**EPSON**

## 6.3.2. 6800 family interface timing
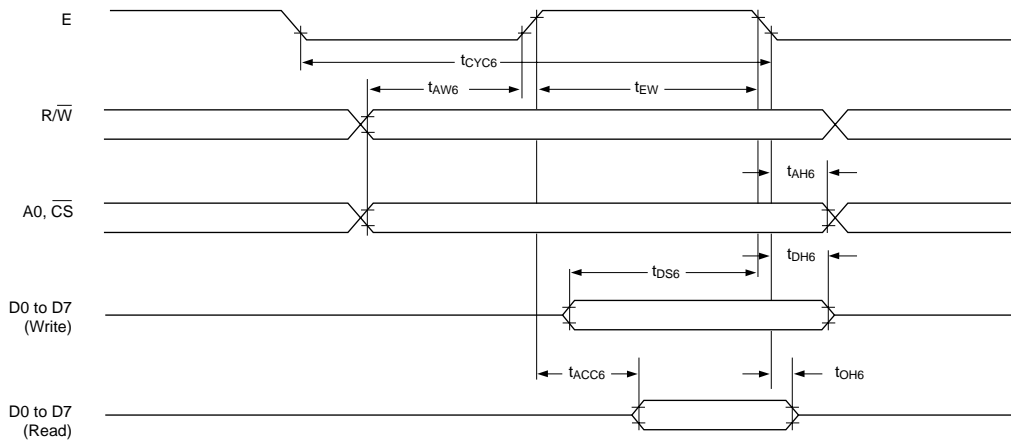


**Note:** $t_{CYC6}$ indicates the interval during which CS is LOW and E is HIGH.

$T_a = -20$ to $75°C$

| Signal | Symbol | Parameter | VDD = 4.5 to 5.5V | | VDD = 2.7 to 4.5V | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| A0, $\overline{CS}$, R/$\overline{W}$ | tCYC6 | System cycle time | See note. | — | See note. | — | ns | CL = 100 pF |
| | tAW6 | Address setup time | 0 | — | 10 | — | ns | |
| | tAH6 | Address hold time | 0 | — | 0 | — | ns | |
| D0 to D7 | tDS6 | Data setup time | 100 | — | 120 | — | ns | |
| | tDH6 | Data hold time | 0 | — | 0 | — | ns | |
| | tOH6 | Output disable time | 10 | 50 | 10 | 75 | ns | |
| | tACC6 | Access time | — | 85 | — | 130 | ns | |
| E | tEW | Enable pulsewidth | 120 | — | 150 | — | ns | |

**Note:** For memory control and system control commands:

$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

## 6.3.3. Display memory read timing



Ta = −20 to 75°C

| Signal | Symbol | Parameter | VDD = 4.5 to 5.5V | | VDD = 2.7 to 4.5V | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| EXT φ0 | tC | Clock period | 100 | — | 125 | — | ns | CL = 100 pF |
| $\overline{VCE}$ | tW | $\overline{VCE}$ HIGH-level pulsewidth | tC − 50 | — | tC − 50 | — | ns | |
| | tCE | $\overline{VCE}$ LOW-level pulsewidth | 2tC − 30 | — | 2tC − 30 | — | ns | |
| VA0 to VA15 | tCYR | Read cycle time | 3tC | — | 3tC | — | ns | |
| | tASC | Address setup time to falling edge of $\overline{VCE}$ | tC − 70 | — | tC − 100 | — | ns | |
| | tAHC | Address hold time from falling edge of $\overline{VCE}$ | 2tC − 30 | — | 2tC − 40 | — | ns | |
| $\overline{VRD}$ | tRCS | Read cycle setup time to falling edge of $\overline{VCE}$ | tC − 45 | — | tC − 60 | — | ns | |
| | tRCH | Read cycle hold time from rising edge of $\overline{VCE}$ | 0.5tC | — | 0.5tC | — | ns | |
| VD0 to VD7 | tACV | Address access time | — | 3tC − 100 | — | 3tC − 115 | ns | |
| | tCEA | $\overline{VCE}$ access time | — | 2tC − 80 | — | 2tC − 90 | ns | |
| | tOH2 | Output data hold time | 0 | — | 0 | — | ns | |
| | tCE3 | $\overline{VCE}$ to data off time | 0 | — | 0 | — | ns | |

### 6.3.4. Display memory write timing

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Ta = −20 to 75°C

| Signal | Symbol | Parameter | VDD = 4.5 to 5.5V | | VDD = 2.7 to 4.5V | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| EXT φ0 | tC | Clock period | 100 | — | 125 | — | ns | CL = 100 pF |
| $\overline{VCE}$ | tW | $\overline{VCE}$ HIGH-level pulsewidth | tC − 50 | — | tC − 50 | — | ns | |
| | tCE | $\overline{VCE}$ LOW-level pulsewidth | 2tC − 30 | — | 2tC − 30 | — | ns | |
| VA0 to VA15 | tCYW | Write cycle time | 3tC | — | 3tC | — | ns | |
| | tAHC | Address hold time from falling edge of $\overline{VCE}$ | 2tC − 30 | — | 2tC − 40 | — | ns | |
| | tASC | Address setup time to falling edge of $\overline{VCE}$ | tC − 70 | — | tC − 110 | — | ns | |
| | tCA | Address hold time from rising edge of $\overline{VCE}$ | 0 | — | 0 | — | ns | |
| | tAS | Address setup time to falling edge of $\overline{VWR}$ | 0 | — | 0 | — | ns | |
| | tAH2 | Address hold time from rising edge of $\overline{VWR}$ | 10 | — | 10 | — | ns | |
| $\overline{VWR}$ | tWSC | Write setup time to falling edge of $\overline{VCE}$ | tC − 80 | — | tC − 115 | — | ns | |
| | tWHC | Write hold time from falling edge of $\overline{VCE}$ | 2tC − 20 | — | 2tC − 20 | — | ns | |
| VD0 to VD7 | tDSC | Data input setup time to falling edge of $\overline{VCE}$ | tC − 85 | — | tC − 125 | — | ns | |
| | tDHC | Data input hold time from falling edge of $\overline{VCE}$ | 2tC − 30 | — | 2tC − 30 | — | ns | |
| | tDH2 | Data hold time from rising edge of $\overline{VWR}$ | 5 | 50 | 5 | 50 | ns | |

**Note:** VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

## 6.3.5.  SLEEP IN command timing
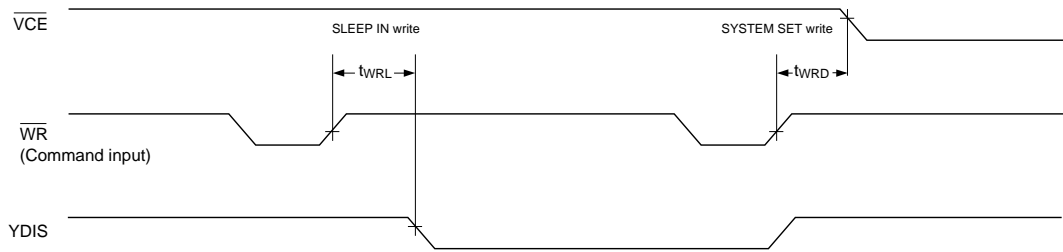


Ta = −20 to 75°C

| Signal | Symbol | Parameter | VDD = 4.5 to 5.5V | | VDD = 2.7 to 4.5V | | Unit | Condition |
|--------|--------|-----------|-------------------|------|-------------------|------|------|-----------|
| | | | Min. | Max. | Min. | Max. | | |
| $\overline{WR}$ | tWRD | $\overline{VCE}$ falling-edge delay time | See note 1. | — | See note 1. | — | ns | CL = 100 pF |
| | tWRL | YDIS falling-edge delay time | — | See note 2. | — | See note 2. | ns | |

**Notes:**

1.  $t_{WRD} = 18t_C + t_{OSS} + 40$   ($t_{OSS}$ is the time delay from the sleep state until stable operation)

2.  $t_{WRL} = 36t_C \times [TC/R] \times [L/F] + 70$

## 6.3.6. External oscillator signal timing
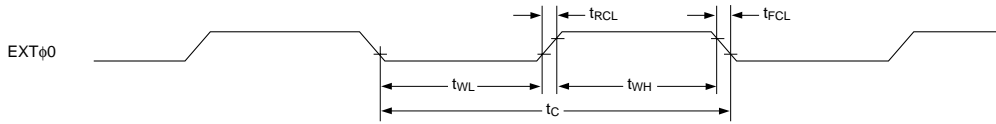


Ta = −20 to 75°C

| Signal | Symbol | Parameter | VDD = 4.5 to 5.5V | | VDD = 2.7 to 4.5V | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max | | |
| EXT φ0 | tRCL | External clock rise time | — | 15 | — | 15 | ns | |
| | tFCL | External clock fall time | — | 15 | — | 15 | ns | |
| | tWH | External clock HIGH-level pulsewidth | See note 1. | See note 2. | See note 1. | See note 2. | ns | |
| | tWL | External clock LOW-level pulsewidth | See note 1. | See note 2. | See note 1. | See note 2. | ns | |
| | tC | External clock period | 100 | — | 125 | — | ns | |

**Notes:**

1. $(t_C - t_{RCL} - t_{FCL}) \times \dfrac{475}{1000} < t_{WH}, t_{WL}$

2. $(t_C - t_{RCL} - t_{FCL}) \times \dfrac{525}{1000} > t_{WH}, t_{WL}$

### 6.3.7. LCD output timing

The following characteristics are for a 1/64 duty cycle.
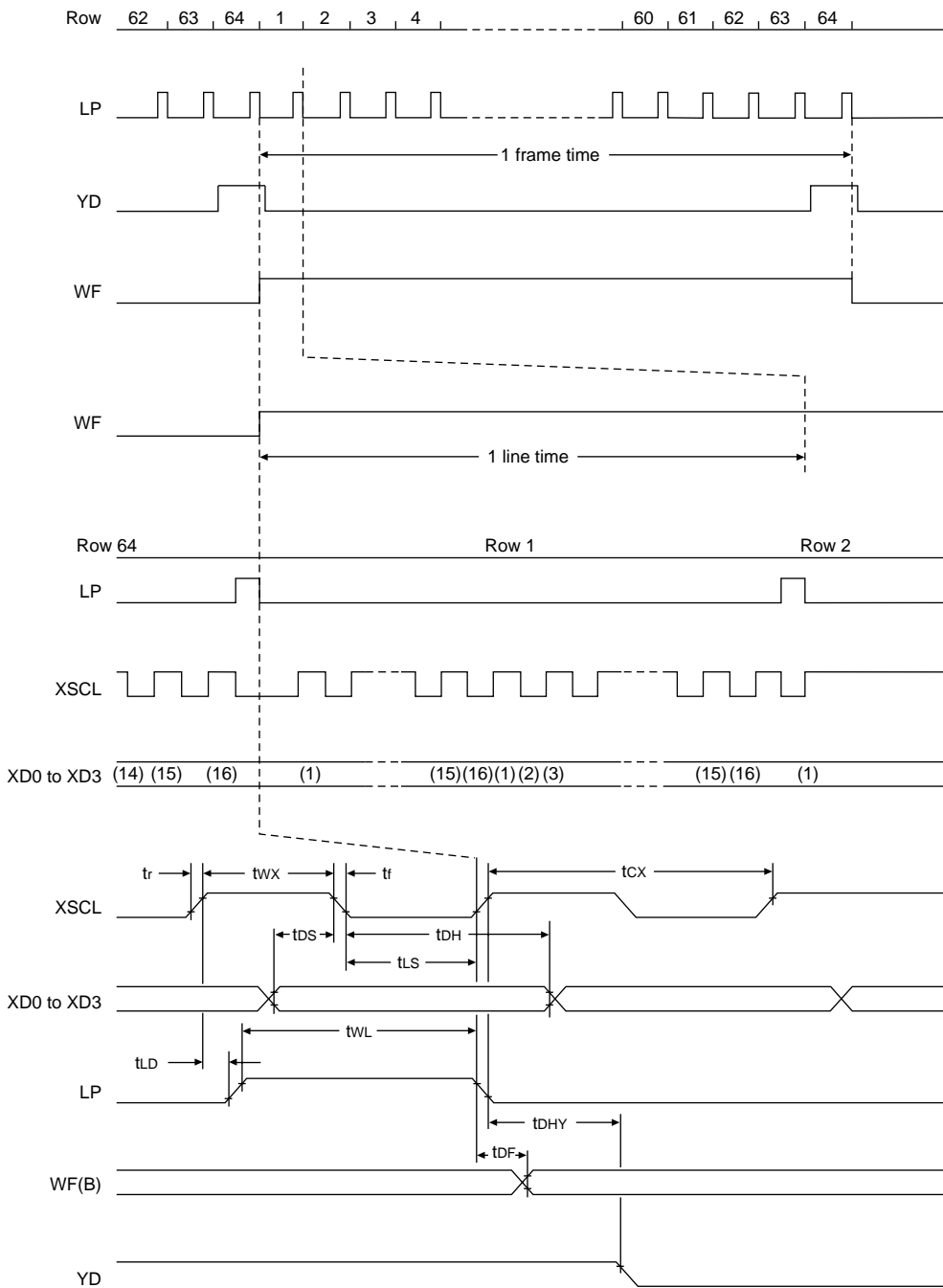
$T_a$ = −20 to 75°C

| Signal | Symbol | Parameter | $V_{DD}$ = 4.5 to 5.5V | | $V_{DD}$ = 2.7 to 4.5V | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max | | |
| | tr | Rise time | — | 30 | — | 40 | ns | CL = 100 pF |
| | tf | Fall time | — | 30 | — | 40 | ns | |
| XSCL | tCX | Shift clock cycle time | 4tC | — | 4tC | — | ns | |
| | tWX | XSCL clock pulsewidth | 2tc – 60 | — | 2tc – 60 | — | ns | |
| XD0 to XD3 | tDH | X data hold time | 2tc – 50 | — | 2tc – 50 | — | ns | |
| | tDS | X data setup time | 2tc – 100 | — | 2tc – 105 | — | ns | |
| LP | tLS | Latch data setup time | 2tc – 50 | — | 2tc – 50 | — | ns | |
| | tWL | LP pulsewidth | 4tc – 80 | — | 4tc – 120 | — | ns | |
| | tLD | LP delay time from XSCL | 0 | — | 0 | — | ns | |
| WF | tDF | Permitted WF delay | — | 50 | — | 50 | ns | |
| YD | tDHY | Y data hold time | 2tc – 20 | — | 2tc – 20 | — | ns | |

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# 7. PACKAGE DIMENSIONS

Unit: mm

## 7.1. S1D13305F00A

◊QFP5-60 pin
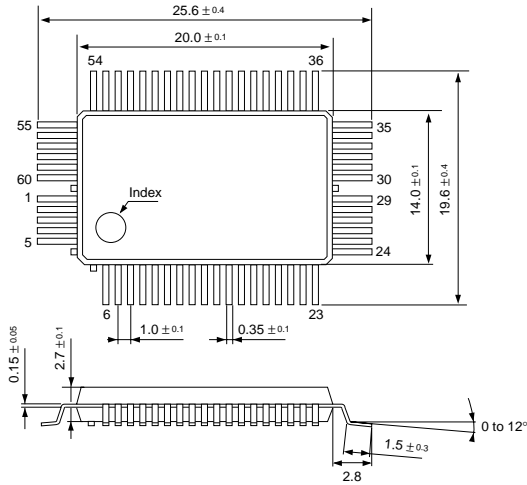


## 7.2. S1D13305F00B

◊QFP6-60 pin

# 8. INSTRUCTION SET

## 8.1. The Command Set

Table 1. Command set

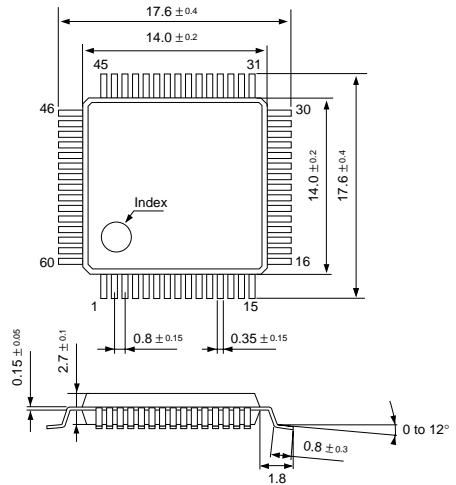| Class | Command | Code | | | | | | | | | | | Hex | Command Description | Command Read Parameters | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $\overline{RD}$ | $\overline{WR}$ | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | No. of Bytes | Sec-tion |
| System control | SYSTEM SET | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | Initialize device and display | 8 | 8.2.1 |
| | SLEEP IN | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 | Enter standby mode | 0 | 8.2.2 |
| Display control | DISP ON/OFF | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | D | 58, 59 | Enable and disable display and display flashing | 1 | 8.3.1 |
| | SCROLL | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 | Set display start address and display regions | 10 | 8.3.2 |
| | CSRFORM | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5D | Set cursor type | 2 | 8.3.3 |
| | CGRAM ADR | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 5C | Set start address of character generator RAM | 2 | 8.3.6 |
| | CSRDIR | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | CD1 | CD0 | 4C to 4F | Set direction of cursor movement | 0 | 8.3.4 |
| | HDOT SCR | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 5A | Set horizontal scroll position | 1 | 8.3.7 |
| | OVLAY | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5B | Set display overlay format | 1 | 8.3.5 |
| Drawing control | CSRW | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 46 | Set cursor address | 2 | 8.4.1 |
| | CSRR | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 47 | Read cursor address | 2 | 8.4.2 |
| Memory control | MWRITE | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | Write to display memory | — | 8.5.1 |
| | MREAD | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 43 | Read from display memory | — | 8.5.2 |

**Notes:**

1. In general, the internal registers of the S1D13305 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged.

   2-byte parameters (where two bytes are treated as 1 data item) are handled as follows:

   a. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.

   b. SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.

2. APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

## 8.2.   System Control Commands

### 8.2.1.   SYSTEM SET

Initializes the device, sets the window sizes, and selects the LCD interface format. Since this command sets the basic operating parameters of the S1D13305 series, an

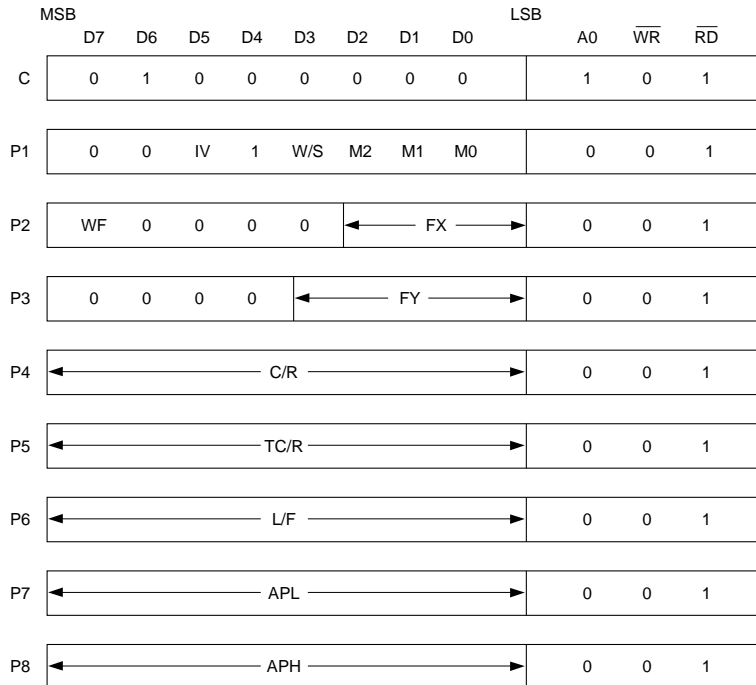incorrect SYSTEM SET command may cause other commands to operate incorrectly.

| | MSB | | | | | | | LSB | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A0 | $\overline{WR}$ | $\overline{RD}$ |
| C | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| P1 | 0 | 0 | IV | 1 | W/S | M2 | M1 | M0 | 0 | 0 | 1 |
| P2 | WF | 0 | 0 | 0 | 0 | ←—— FX ——→ | | | 0 | 0 | 1 |
| P3 | 0 | 0 | 0 | 0 | ←—— FY ——→ | | | | 0 | 0 | 1 |
| P4 | ←———————— C/R ————————→ | | | | | | | | 0 | 0 | 1 |
| P5 | ←———————— TC/R ———————→ | | | | | | | | 0 | 0 | 1 |
| P6 | ←———————— L/F ————————→ | | | | | | | | 0 | 0 | 1 |
| P7 | ←———————— APL ———————→ | | | | | | | | 0 | 0 | 1 |
| P8 | ←———————— APH ———————→ | | | | | | | | 0 | 0 | 1 |

Figure 1. SYSTEM SET instruction

### 8.2.1.1.   C

This control byte performs the following:
1.   Resets the internal timing generator
2.   Disables the display
3.   Cancels sleep mode
Parameters following P1 are not needed if only canceling sleep mode.

### 8.2.1.2.   M0

Selects the internal or external character generator ROM. The internal character generator ROM contains 160, 5 × 7 pixel characters, as shown in figure 70. These characters are fixed at fabrication by the metallization mask. The external character generator ROM, on the other hand, can contain up to 256 user-defined characters.
M0 = 0: Internal CG ROM
M0 = 1: External CG ROM

Note that if the CG ROM address space overlaps the display memory address space, that portion of the display memory cannot be written to.

### 8.2.1.3.   M1

Selects the memory configuration for user-definable characters. The CG RAM codes select one of the 64 codes shown in figure 46.
M1 = 0: No D6 correction.
The CG RAM1 and CG RAM2 address spaces are not contiguous, the CG RAM1 address space is treated as character generator RAM, and the CG RAM2 address space is treated as character generator ROM.
M1 = 1: D6 correction.
The CG RAM1 and CG RAM2 address spaces are contiguout and are both treated as character generator RAM.

### 8.2.1.4. M2

Selects the height of the character bitmaps. Characters more than 16 pixels high can be displayed by creating a bitmap for each portion of each character and using the S1D13305 series graphics mode to reposition them.

M2 = 0: 8-pixel character height (2716 or equivalent ROM)

M2 = 1: 16-pixel character height (2732 or equivalent ROM)

### 8.2.1.5. W/S

Selects the LCD drive method.
W/S = 0: Single-panel drive
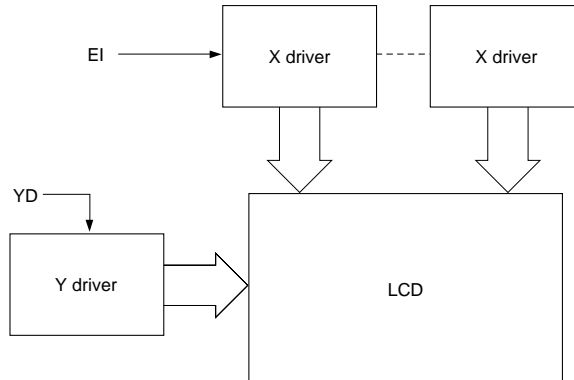W/S = 1: Dual-panel drive
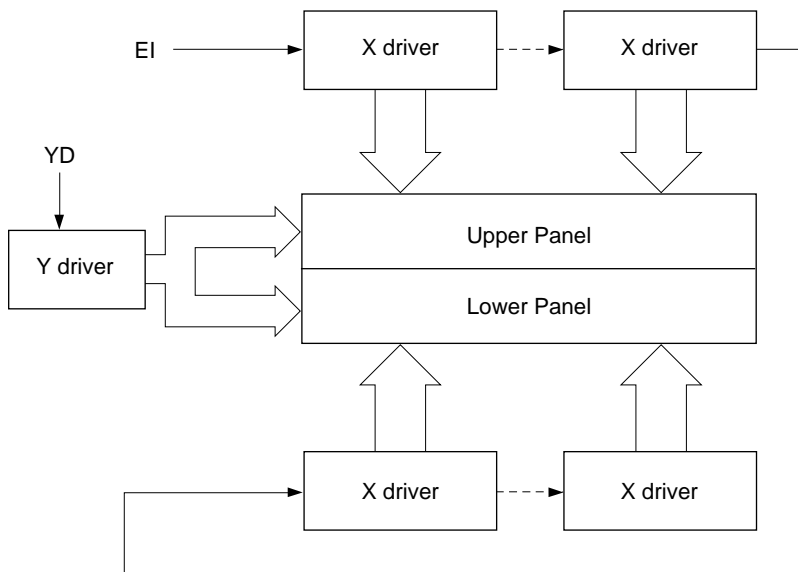
Figure 2.   Single-panel display
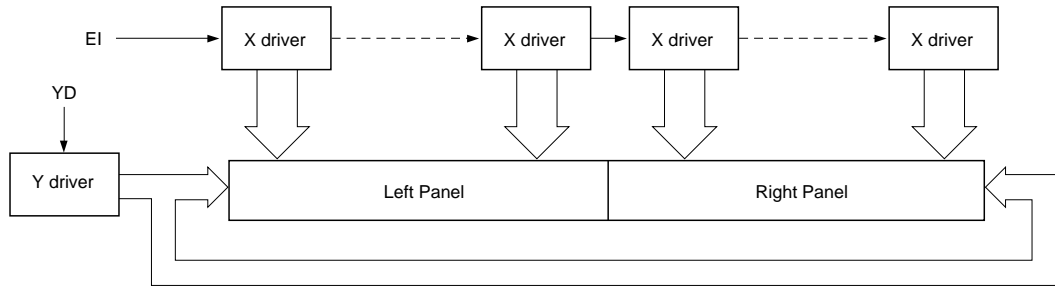
Figure 3.   Above and below two-panel display

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Figure 4.   Left-and-right two-panel display

**Note**
There are no Seiko Epson LCD units in the configuration shown in Figure 4.

Table 2.   LCD parameters

| Parameter | W/S = 0 | | W/S = 1 | |
|---|---|---|---|---|
| | IV = 1 | IV = 0 | IV = 1 | IV = 0 |
| C/R | C/R | C/R | C/R | C/R |
| TC/R | TC/R | TC/R (See note 1.) | TC/R | TC/R |
| L/F | L/F | L/F | L/F | L/F |
| SL1 | 00H to L/F | 00H to L/F + 1 (See note 2.) | (L/F) / 2 | (L/F) / 2 |
| SL2 | 00H to L/F | 00H to L/F + 1 (See note 2.) | (L/F) / 2 | (L/F) / 2 |
| SAD1 | First screen block | First screen block | First screen block | First screen block |
| SAD2 | Second screen block | Second screen block | Second screen block | Second screen block |
| SAD3 | Third screen block | Third screen block | Third screen block | Third screen block |
| SAD4 | Invalid | Invalid | Fourth screen block | Fourth screen block |
| Cursor movement range | Continuous movement over whole screen | | Above-and-below configuration: continuous movement over whole screen | |

**Notes:**

1. See table 26 for further details on setting the C/R and TC/R parameters when using the HDOT SCR command.

2. The value of SL when IV = 0 is equal to the value of SL when IV = 1, plus one.

### 8.2.1.6.   IV

Screen origin compensation for inverse display. IV is usually set to 1.
The best way of displaying inverted characters is to Exclusive-OR the text layer with the graphics background layer. However, inverted characters at the top or left of the screen are difficult to read as the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these characters.

The IV flag causes the S1D13305 series to offset the text screen against the graphics back layer by one vertical pixel. Use the horizontal pixel scroll function (HDOT SCR) to shift the text screen 1 to 7 pixels to the right. All characters will then have the necessary surrounding background pixels that ensure easy reading of the inverted characters.

See Section 10.5 for information on scrolling.

IV = 0: Screen top-line correction
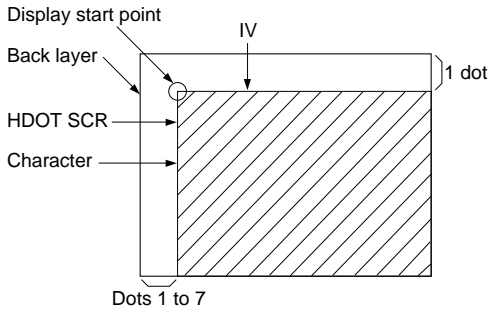IV = 1: No screen top-line correction



Figure 5.   IV and HDOT SCR adjustment

### 8.2.1.7.  FX

Define the horizontal character size. The character width in pixels is equal to FX + 1, where FX can range from 00 to 07H inclusive. If data bit 3 is set (FX is in the range 08 to 0FH) and an 8-pixel font is used, a space is inserted between characters.

Table 3.   Horizontal character size selection

| FX | | | | | [FX] character width (pixels) |
|---|---|---|---|---|---|
| HEX | D3 | D2 | D1 | D0 | |
| 00 | 0 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 1 | 2 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 07 | 0 | 1 | 1 | 1 | 8 |

Since the S1D13305 series handles display data in 8-bit units, characters larger than 8 pixels wide must be formed from 8-pixel segments. As Figure 6 shows, the remainder of the second eight bits are not displayed. This also applies to the second screen layer.

In graphics mode, the normal character field is also eight pixels. If a wider character field is used, any remainder in the second eight bits is not displayed.
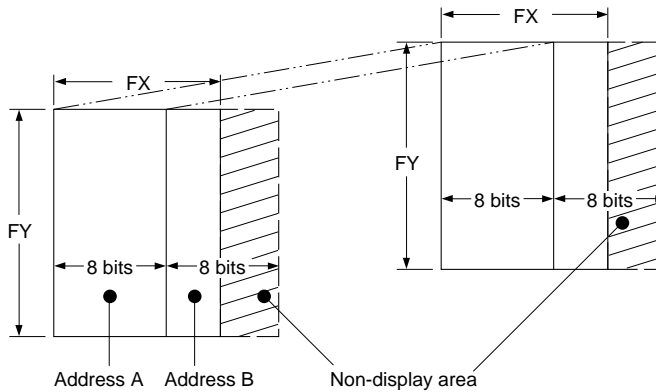


Figure 6.   FX and FY display addresses

#### 8.2.1.8.  WF

Selects the AC frame drive waveform period. WF is usually set to 1.

WF = 0: 16-line AC drive

WF = 1: two-frame AC drive

In two-frame AC drive, the WF period is twice the frame period.

In 16-line AC drive, WF inverts every 16 lines.

Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles.

#### 8.2.1.9.  FY

Sets the vertical character size. The height in pixels is equal to FY + 1.

FY can range from 00 to 0FH inclusive.

Set FY to zero (vertical size equals one) when in graphics mode.

#### 8.2.1.10.  C/R

Sets the address range covered by one display line, that is, the number of characters less one, multiplied by the number of horizontal bytes per character.

C/R can range from 0 to 239.

For example, if the character width is 10 pixels, then the address range is equal to twice the number of characters, less 2. See Section 16.1.1 for the calculation of C/R.

[C/R] cannot be set to a value greater than the address range. It can, however, be set smaller than the address range, in which case the excess display area is blank. The number of excess pixels must not exceed 64.

Table 4.   Vertical character size selection

| | FY | | | | [FY] character height (pixels) |
|---|---|---|---|---|---|
| HEX | D3 | D2 | D1 | D0 | |
| 00 | 0 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 1 | 2 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 07 | 0 | 1 | 1 | 1 | 8 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 0E | 1 | 1 | 1 | 0 | 15 |
| 0F | 1 | 1 | 1 | 1 | 16 |

Table 5.   Display line address range

| | C/R | | | | | | | | [C/R] bytes per display line |
|---|---|---|---|---|---|---|---|---|---|
| HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 4F | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 80 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| EE | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 239 |
| EF | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 240 |

### 8.2.1.11. TC/R

Sets the length, including horizontal blanking, of one line. The line length is equal to TC/R + 1, where TC/ R can range from 0 to 255.

TC/R must be greater than or equal to C/R + 4. Provided this condition is satisfied, [TC/R] can be set according to the equation given in section 16.1.1 in order to hold the frame period constant and minimize jitter for any given main oscillator frequency, $f_{OSC}$.

Table 6. Line length selection

| TC/R | | | | | | | | | [TC/R] line length (bytes) |
|---|---|---|---|---|---|---|---|---|---|
| HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 52 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 83 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| FE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 255 |
| FF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 256 |

### 8.2.1.12. L/F

Sets the height, in lines, of a frame. The height in lines is equal to L/F + 1, where L/F can range from 0 to 255.

Table 7. Frame height selection

| L/F | | | | | | | | | [L/F] lines per frame |
|---|---|---|---|---|---|---|---|---|---|
| HEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 7F | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| FE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 255 |
| FF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 256 |

If W/S is set to 1, selecting two-screen display, the number of lines must be even and L/F must, therefore, be an odd number.

### 8.2.1.13.  AP

Defines the horizontal address range of the virtual screen.
APL is the least significant byte of the address.

| APL | AP7 | AP6 | AP5 | AP4 | AP3 | AP2 | AP1 | AP0 |
|---|---|---|---|---|---|---|---|---|

| APH | AP15 | AP14 | AP13 | AP12 | AP11 | AP10 | AP9 | AP8 |
|---|---|---|---|---|---|---|---|---|

Figure 7.   AP parameters

Table 8.   Horizontal address range

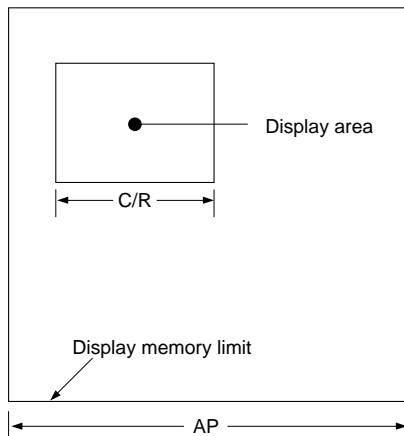| Hex code | | | | [AP] addresses per line |
|---|---|---|---|---|
| APH | | APL | | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| ↓ | ↓ | ↓ | ↓ | ↓ |
| 0 | 0 | 5 | 0 | 80 |
| ↓ | ↓ | ↓ | ↓ | ↓ |
| F | F | F | E | $2^{16} - 2$ |
| F | F | F | F | $2^{16} - 1$ |



Figure 8.   AP and C/R relationship

### 8.2.2.  SLEEP IN

Places the system in standby mode. This command has no parameter bytes. At least one blank frame after receiving this command, the S1D13305F halts all internal operations, including the oscillator, and enters the sleep state.

Blank data is sent to the X-drivers, and the Y-drivers have their bias supplies turned off by the YDIS signal. Using the YDIS signal to disable the Y-drivers guards against any spurious displays.

The internal registers of the S1D13305 series maintain their values during the sleep state. The display memory control pins maintain their logic levels to ensure that the display memory is not corrupted.

The S1D13305 series can be removed from the sleep state by sending the SYSTEM SET command with only the P1 parameter. The DISP ON command should be sent next to enable the display.

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| C | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

Figure 9.   SLEEP IN instruction

1.  The YDIS signal goes LOW between one and two frames after the SLEEP IN command is received. Since YDIS forces all display driver outputs to go to the deselected output voltage, YDIS can be used as a power-down signal for the LCD unit. This can be done by having YDIS turn off the relatively high-power LCD drive supplies at the same time as it blanks the display.

2.  Since all internal clocks in the S1D13305 series are halted while in the sleep state, a DC voltage will be applied to the LCD panel if the LCD drive supplies remain on.

    If reliability is a prime consideration, turn off the LCD drive supplies before issuing the SLEEP IN command.

3.  Note that, although the bus lines become high imped-ance in the sleep state, pull-up or pull-down resistors on the bus will force these lines to a known state.

## 8.3. Display Control Commands

### 8.3.1. DISP ON/OFF

Turns the whole display on or off. The single-byte parameter enables and disables the cursor and layered screens, and sets the cursor and screen flash rates. The cursor can be set to flash over one character or over a whole line.
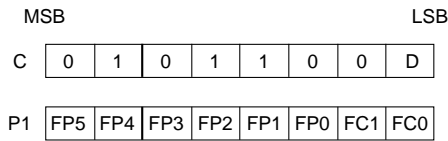
MSB                                                    LSB

| C | 0 | 1 | 0 | 1 | 1 | 0 | 0 | D |
|---|---|---|---|---|---|---|---|---|

| P1 | FP5 | FP4 | FP3 | FP2 | FP1 | FP0 | FC1 | FC0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|

Figure 10.   DISP ON/OFF parameters

#### 8.3.1.1. D

Turns the display ON or OFF. The D bit takes precedence over the FP bits in the parameter.
D = 0:  Display OFF
D = 1:  Display ON

#### 8.3.1.2. FC

Enables/disables the cursor and sets the flash rate. The cursor flashes with a 70% duty cycle (ON/OFF).

Table 9.   Cursor flash rate selection

| FC1 | FC0 | Cursor display | |
|-----|-----|----------------|--|
| 0 | 0 | OFF (blank) | |
| 0 | 1 | ON | No flashing |
| 1 | 0 | | Flash at $f_{FR}$/32 Hz (approx. 2 Hz) |
| 1 | 1 | | Flash at $f_{FR}$/64 Hz (approx. 1 Hz) |

**Note:** As the MWRITE command always enables the cursor, the cursor position can be checked even when performing consecutive writes to display memory while the cursor is flashing.

#### 8.3.1.3. FP

Each pair of bits in FP sets the attributes of one screen block, as follows.

The display attributes are as follows:

Table 10.   Screen block attribute selection

| FP1 | FP0 | First screen block (SAD1) | |
|-----|-----|---------------------------|--|
| FP3 | FP2 | Second screen block (SAD2, SAD4). See note. | |
| FP5 | FP4 | Third screen block (SAD3) | |
| 0 | 0 | OFF (blank) | |
| 0 | 1 | ON | No flashing |
| 1 | 0 | | Flash at $f_{FR}$/32 Hz (approx. 2 Hz) |
| 1 | 1 | | Flash at $f_{FR}$/4 Hz (approx. 16 Hz) |

**Note**
If SAD4 is enabled by setting W/S to 1, FP3 and FP2 control both SAD2 and SAD4. The attributes of SAD2 and SAD4 cannot be set independently.

### 8.3.2. SCROLL

#### 8.3.2.1. C

Sets the scroll start address and the number of lines per scroll block. Parameters P1 to P10 can be omitted if not required. The parameters must be entered sequentially as shown in Figure 11.
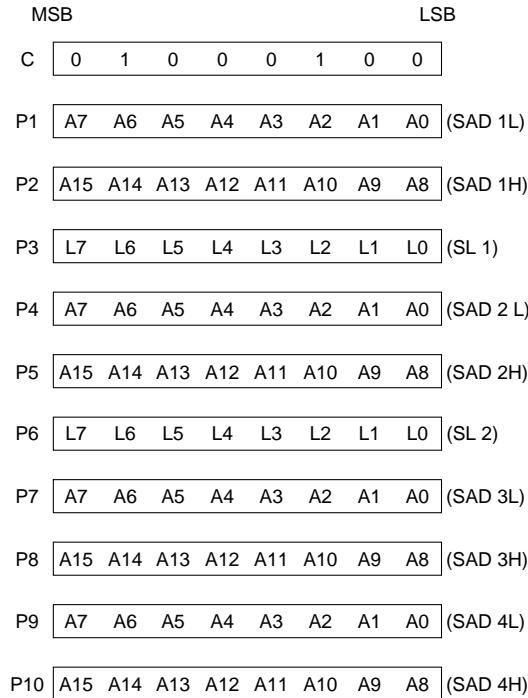
MSB                                                    LSB

| C   | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |

| P1  | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | (SAD 1L) |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| P2  | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | (SAD 1H) |
| P3  | L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 | (SL 1) |
| P4  | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | (SAD 2 L) |
| P5  | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | (SAD 2H) |
| P6  | L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 | (SL 2) |
| P7  | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | (SAD 3L) |
| P8  | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | (SAD 3H) |
| P9  | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | (SAD 4L) |
| P10 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | (SAD 4H) |

Figure 11.    SCROLL instruction parameters

**Note:** Set parameters P9 and P10 only if both two-screen drive (W/S = 1) and two-layer configuration are selected. SAD4 is the fourth screen block display start address.

Table 11.  Screen block start address selection

| | SL1, SL2 | | | | | | | | [SL] screen lines |
|---|---|---|---|---|---|---|---|---|---|
| HEX | L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 | |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 7F | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| FE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 255 |
| FF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 256 |

### 8.3.2.2.  SL1, SL2
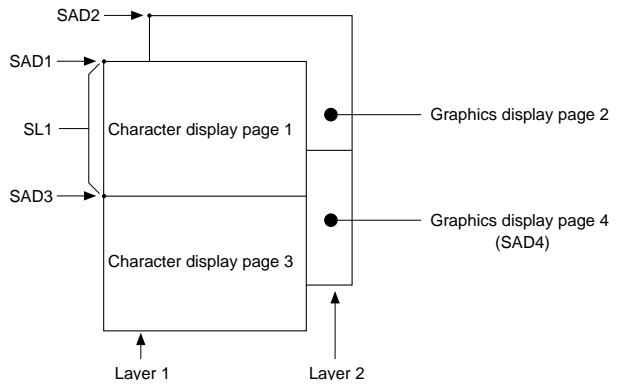
SL1 and SL2 set the number of lines per scrolling screen. The number of lines is SL1 or SL2 plus one. The relationship between SAD, SL and the display mode is described below.

Table 12.  Text display mode

| W/S | Screen | | First Layer | Second Layer |
|---|---|---|---|---|
| 0 | First screen block | | SAD1 | SAD2 |
| | Second screen block | | SL1 | SL2 |
| | Third screen block (partitioned screen) | | SAD3 (see note 1)<br>Set both SL1 and SL2 to L/F + 1<br>if not using a partitioned screen. | |
| | Screen configuration example:<br><br>SAD2<br>SAD1<br>SL1 — Character display page 1<br>SAD3<br>Character display page 3<br>SL2<br>Graphics display page 2<br>Layer 2<br>Layer 1 | | | |

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Table 12.   Text display mode (continued)

| W/S | Screen | First Layer | Second Layer |
|---|---|---|---|
| 1 | Upper screen | SAD1<br>SL1 | SAD2<br>SL2 |
| | Lower screen | SAD3<br>(See note 2.) | SAD4<br>(See note 2.) |
| | Set both SL1 and SL2 to ((L/F) / 2 + 1). | | |
| | Screen configuration example: | | |



**Notes:**

1. SAD3 has the same value as either SAD1 or SAD2, whichever has the least number of lines (set by SL1 and SL2).
2. Since the parameters corresponding to SL3 and SL4 are fixed by L/F, they do not have to be set in this mode.

Table 13.  Graphics display mode

| W/S | Screen | First Layer | Second Layer | Third Layer |
|---|---|---|---|---|
| 0 | Two-layer composition | SAD1<br>SL1 | SAD2<br>SL2 | — |
|  | Upper screen | SAD3 (see note 3.)<br>Set both SL1 and SL2 to<br>L/F + 1 if not using a<br>partitioned screen | | — |
|  | Screen configuration example:  | | | |
| 0 | Three-layer configuration | SAD1<br>SL1 = L/F + 1 | SAD2<br>SL2 = L/F + 1 | SAD3<br>— |
|  | Screen configuration example:  | | | |

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Table 13.   Graphics display mode (continued)

| W/S | Screen | First Layer | Second Layer | Third Layer |
|---|---|---|---|---|
| 1 | Upper screen | SAD1<br>SL1 | SAD2<br>SL2 | — |
| | Lower screen | SAD3<br>(See note 2.) | SAD4<br>(See note 2.) | — |
| | Set both SL1 and SL2 to ((L/F) / 2 + 1). | | | |
| | Screen configuration example (See note 3.):  | | | |

**Notes:**

1. SAD3 has the same value as either SAD1 or SAD2, whichever has the least number of lines (set by SL1 and SL2).

2. Since the parameters corresponding to SL3 and SL4 are fixed by L/F, they do not have to be set.

3. If, and only if, W/S = 1, the differences between SL1 and (L/F + 1) / 2, and between SL2 and (L/F + 1) / 2, are blanked.
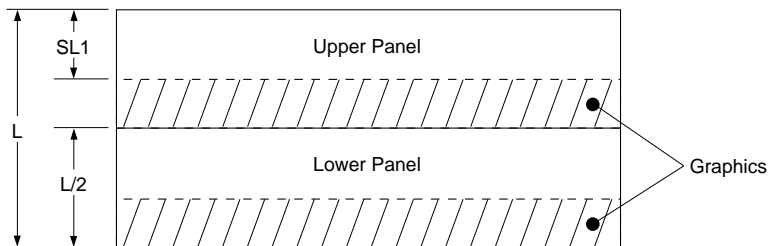


Figure 12.   Two-panel display height

### 8.3.3. CSRFORM

Sets the cursor size and shape. Although the cursor is normally only used in text displays, it may also be used in graphics displays when displaying special characters.
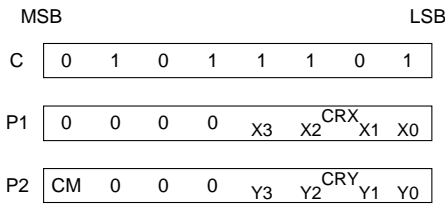
| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| C | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |

| | | | | | | CRX | | |
|---|---|---|---|---|---|---|---|---|
| P1 | 0 | 0 | 0 | 0 | X3 | X2 | X1 | X0 |

| | | | | | | CRY | | |
|---|---|---|---|---|---|---|---|---|
| P2 | CM | 0 | 0 | 0 | Y3 | Y2 | Y1 | Y0 |

Figure 13.   CSRFORM parameter bytes

#### 8.3.3.1. CRX

Sets the horizontal size of the cursor from the character origin. CRX is equal to the cursor size less one. CRX must be less than or equal to FX.

Table 14.   Horizontal cursor size selection

| CRX | | | | | [CRX] cursor width (pixels) |
|---|---|---|---|---|---|
| HEX | X3 | X2 | X1 | X0 | |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 2 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 4 | 0 | 1 | 0 | 0 | 9 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| E | 1 | 1 | 1 | 0 | 15 |
| F | 1 | 1 | 1 | 1 | 16 |

#### 8.3.3.2. CRY

Sets the location of an underscored cursor in lines, from the character origin. When using a block cursor, CRY sets the vertical size of the cursor from the character origin. CRY is equal to the number of lines less one.

Table 15.   Cursor height selection

| CRY | | | | | [CRY] cursor height (lines) |
|---|---|---|---|---|---|
| HEX | Y3 | Y2 | Y1 | Y0 | |
| 0 | 0 | 0 | 0 | 0 | Illegal |
| 1 | 0 | 0 | 0 | 1 | 2 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 8 | 1 | 0 | 0 | 0 | 9 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| E | 1 | 1 | 1 | 0 | 15 |
| F | 1 | 1 | 1 | 1 | 16 |

Character start point



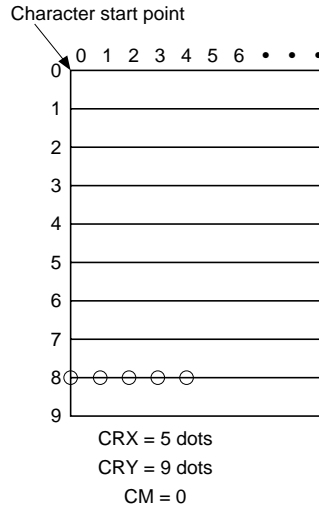CRX = 5 dots
CRY = 9 dots
CM = 0

Figure 14.   Cursor size and position

#### 8.3.3.3. CM

Sets the cursor shape. Always set CM to 1 when in graphics mode.
CM = 0:  Underscore cursor
CM = 1:  Block cursor

### 8.3.4. CSRDIR

Sets the direction of automatic cursor increment. The cursor can move left or right one character, or up or down by the number of bytes specified by the address pitch, AP. When reading from and writing to display memory, this automatic cursor increment controls the display memory address increment on each read or write.
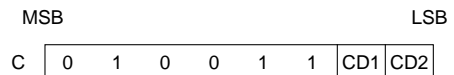
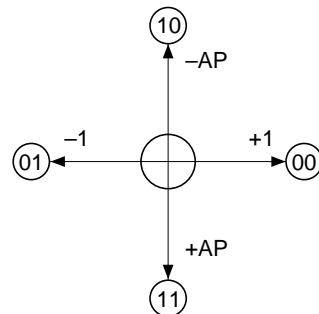| | MSB | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|
| C | 0 | 1 | 0 | 0 | 1 | 1 | CD1 | CD2 |

Figure 15.   CSRDIR parameters



Figure 16.   Cursor direction

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Table 16.   Cursor shift direction

| C | CD1 | CD0 | Shift direction |
|---|---|---|---|
| 4CH | 0 | 0 | Right |
| 4DH | 0 | 1 | Left |
| 4EH | 1 | 0 | Up |
| 4FH | 1 | 1 | Down |

**Note:**  Since the cursor moves in address units even if $FX \geq 9$, the cursor address increment must be preset for movement in character units. See Section 9.3.

## 8.3.5.   OVLAY

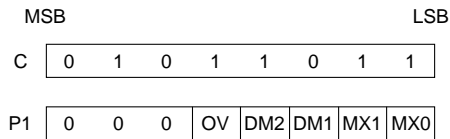Selects layered screen composition and screen text/ graphics mode.

MSB                                                    LSB

| C | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|

| P1 | 0 | 0 | 0 | OV | DM2 | DM1 | MX1 | MX0 |
|---|---|---|---|---|---|---|---|---|

Figure 17.   OVLAY parameters

### 8.3.5.1.   MX0, MX1

MX0 and MX1 set the layered screen composition method, which can be either OR, AND, Exclusive-OR or Priority-OR. Since the screen composition is organized in layers and not by screen blocks, when using a layer divided into two screen blocks, different composition methods cannot be specified for the individual screen blocks.

The Priority-OR mode is the same as the OR mode unless flashing of individual screens is used.

Table 17.   Composition method selection

| MX1 | MX0 | Function | Composition Method | Applications |
|---|---|---|---|---|
| 0 | 0 | $L1 \cup L2 \cup L3$ | OR | Underlining, rules, mixed text and graphics |
| 0 | 1 | $(L1 \oplus L2) \cup L3$ | Exclusive-OR | Inverted characters, flashing regions, underlining |
| 1 | 0 | $(L1 \cap L2) \cup L3$ | AND | Simple animation, three-dimensional appearance |
| 1 | 1 | $L1 > L2 > L3$ | Priority-OR | |

**Notes:**

L1:  First layer (text or graphics). If text is selected, layer L3 cannot be used.

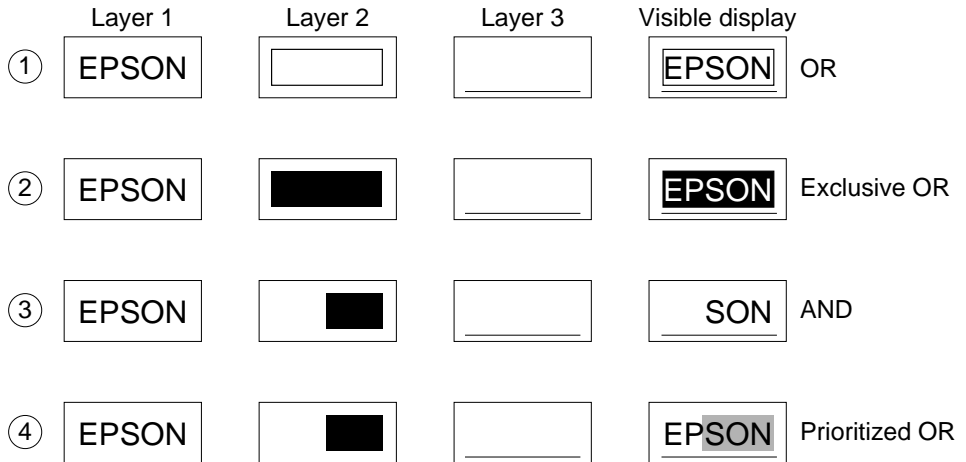L2:  Second layer (graphics only)

L3:  Third layer (graphics only)

Figure 18.   Combined layer display

**Notes:**

L1:  Not flashing

L2:  Flashing at 1 Hz

L3:  Flashing at 2 Hz

#### 8.3.5.2.  DM1, DM2

DM1 and DM2 specify the display mode of screen blocks 1 and 3, respectively.

DM1/2 = 0:  Text mode

DM1/2 = 1:  Graphics mode

Note 1: Screen blocks 2 and 4 can only display graphics.

Note 2: DM1 and DM2 must be the same, regardless of the setting of W/S.

#### 8.3.5.3.  OV

Specifies two- or three-layer composition in graphics mode.

OV = 0:  Two-layer composition

OV = 1:  Three-layer composition

Set OV to 0 for mixed text and graphics mode.

#### 8.3.6.  CGRAM ADR

Specifies the CG RAM start address.
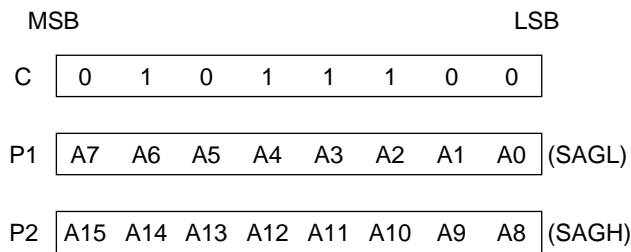


Figure 19.   CGRAM ADR parameters

**Note**

See section 10 for information on the SAG parameters.

### 8.3.7. HDOT SCR

While the SCROLL command only allows scrolling by characters, HDOT SCR allows the screen to be scrolled horizontally by pixels. HDOT SCR cannot be used on individual layers.
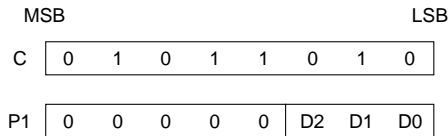
```
       MSB                           LSB

   C   | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |


   P1  | 0 | 0 | 0 | 0 | 0 | D2 | D1 | D0 |
```

Figure 20.  HDOT SCR parameters

#### 8.3.7.1.  D0 to D2

Specifies the number of pixels to scroll. The C/R parameter has to be set to one more than the number of horizontal characters before using HDOT SCR. Smooth scrolling can be simulated if the controlling microprocessor repeatedly issues the HDOT SCR command to the S1D13305 series. See Section 9.5 for more information on scrolling the display.

Table 18.  Scroll step selection (continued)

| P1 | | | | Number of pixels to scroll |
| --- | --- | --- | --- | --- |
| HEX | D2 | D1 | D0 | |
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 1 | 1 |
| 02 | 0 | 1 | 0 | 2 |
| ↓ | ↓ | ↓ | ↓ | ↓ |
| 06 | 1 | 1 | 0 | 6 |
| 07 | 1 | 1 | 1 | 7 |

M/N is the number of bits (dots) that parameter 1 (P1) is incremented/decremented by.
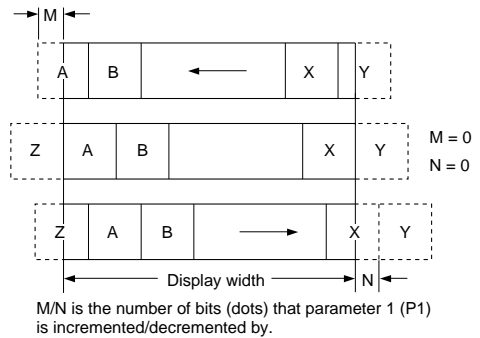
Figure 21.  Horizontal scrolling

## 8.4. Drawing Control Commands

### 8.4.1.  CSRW

The 16-bit cursor address register contains the display memory address of the data at the cursor position as shown in Figure 22.
Note that the microprocessor cannot directly access the display memory.

The MREAD and MWRITE commands use the address in this register.

```
       MSB                              LSB

   C   | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |


   P1  | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |  (CSRL)


   P2  | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |  (CSRH)
```
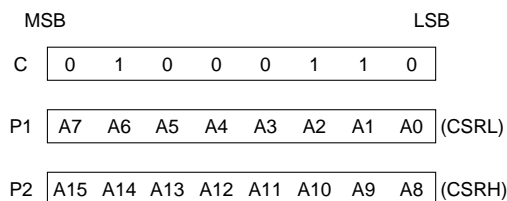
Figure 22.  CSRW parameters

The cursor address register can only be modified by the CSRW command, and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling.

If a new address is not set, display memory accesses will be from the last set address or the address after previous automatic increments.

### 8.4.2. CSRR

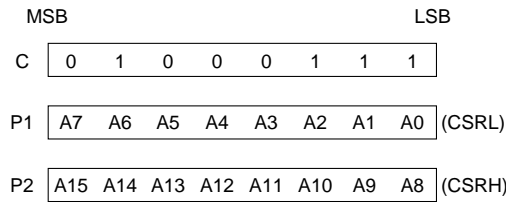Reads from the cursor address register. After issuing the command, the data read address is read twice, for the low byte and then the high byte of the register.

| | MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|
| C | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | |
| P1 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | (CSRL) |
| P2 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | (CSRH) |

Figure 23.   CSRR parameters

## 8.5.   Memory Control Commands

### 8.5.1.   MWRITE

The microprocessor may write a sequence of data bytes to display memory by issuing the MREAD command and then writing the bytes to the S1D13305 series. There is no need for further MWRITE commands or for the micro-processor to update the cursor address register after each byte as the cursor address is automatically incremented by the amount set with CSRDIR, in preparation for the next data write.
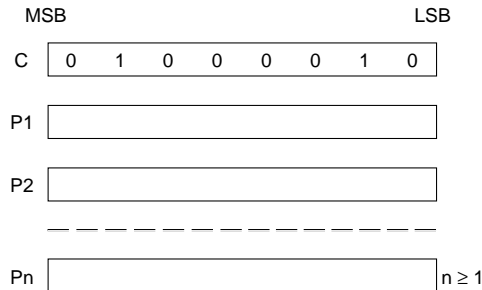
| | MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|
| C | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | |
| P1 | | | | | | | | | |
| P2 | | | | | | | | | |
| Pn | | | | | | | | | $n \geq 1$ |

Figure 24.   MWRITE parameters

**Note:**
P1, P2, ..., Pn: display data.

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### 8.5.2. MREAD

Puts the S1D13305 series into the data output state. Each time the microprocessor reads the buffer, the cursor address is incremented by the amount set by CSRDIR and the next data byte fetched from memory, so a sequence of data bytes may be read without further MREAD commands or by updating the cursor address register.

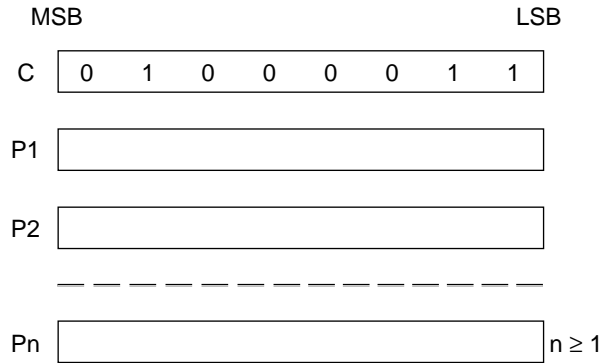If the cursor is displayed, the read data will be from two positions ahead of the cursor.

MSB LSB

| C | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |

P1

P2

Pn    n ≥ 1

Figure 25.   MREAD parameters

# 9. DISPLAY CONTROL FUNCTIONS

## 9.1. Character Configuration

The origin of each character bitmap is in the top left corner as shown in Figure 29. Adjacent bits in each byte are horizontally adjacent in the corresponding character image.

Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.
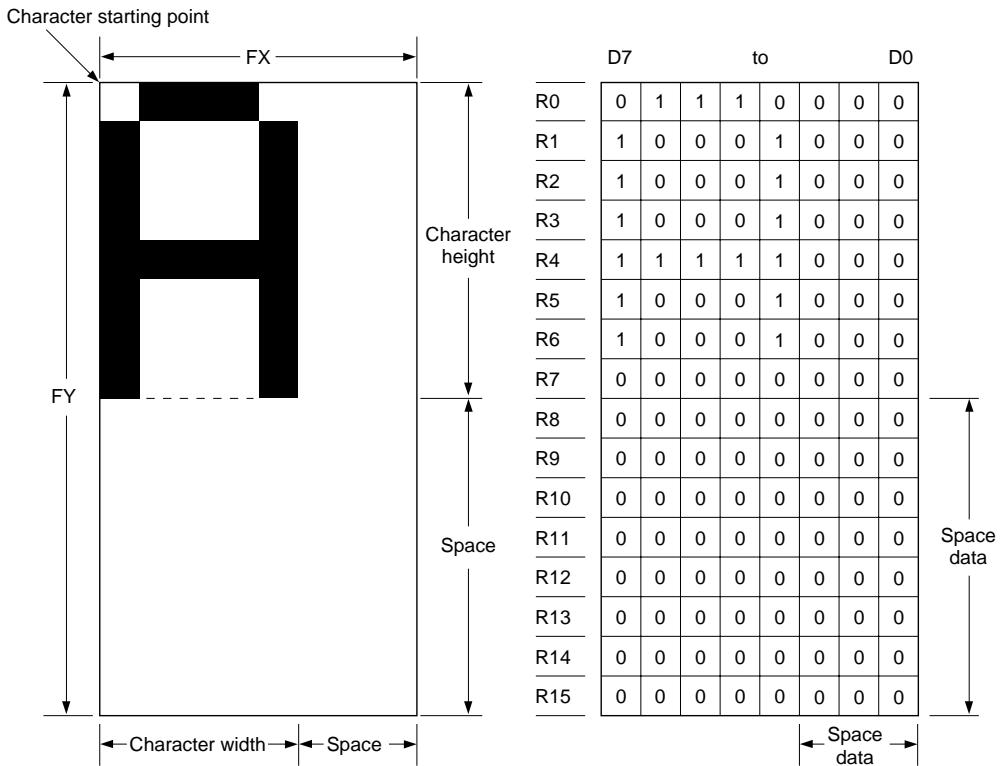


| | D7 | | | to | | | | D0 | |
|---|---|---|---|---|---|---|---|---|---|
| R0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | |
| R1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| R2 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| R3 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| R4 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | |
| R5 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| R6 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| R7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Space data |
| R12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R15 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Figure 26. Example of character display ([FX] ≤ 8) and generator bitmap

If the area outside the character bitmap contains only zeros, the displayed character size can easily be increased by increasing FX and FY, as the zeros ensure that the extra space between displayed characters is blank.

The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.
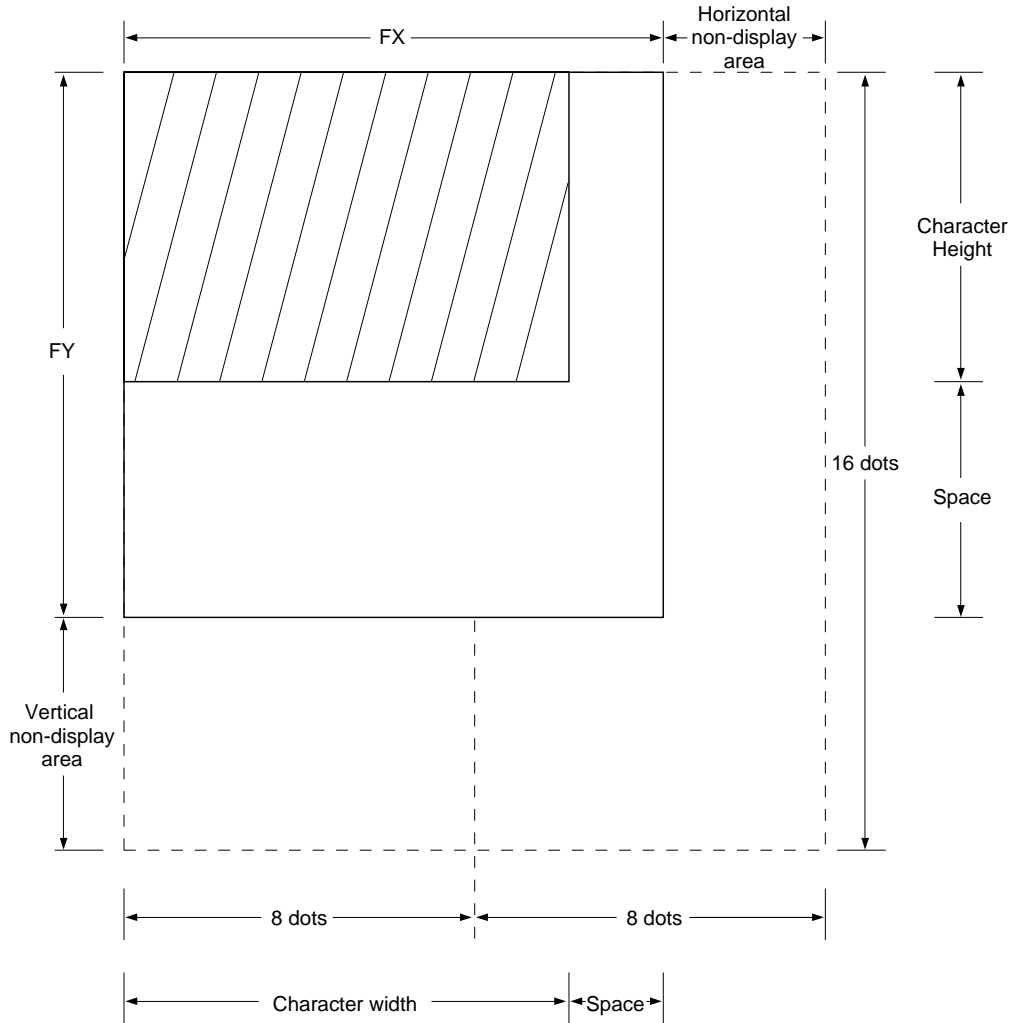
Figure 27.   Character width greater than one byte wide ([FX] = 9)

**Note:**  The S1D13305 series does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row, even though the character image requires only one.

## 9.2. Screen Configuration

### 9.2.1. Screen configuration

The basic screen configuration of the S1D13305 series is as a single text screen or as overlapping text and graphics screens. The graphics screen uses eight times as much display memory as the text screen.

Figure 28 shows the relationship between the virtual screens and the physical screen.
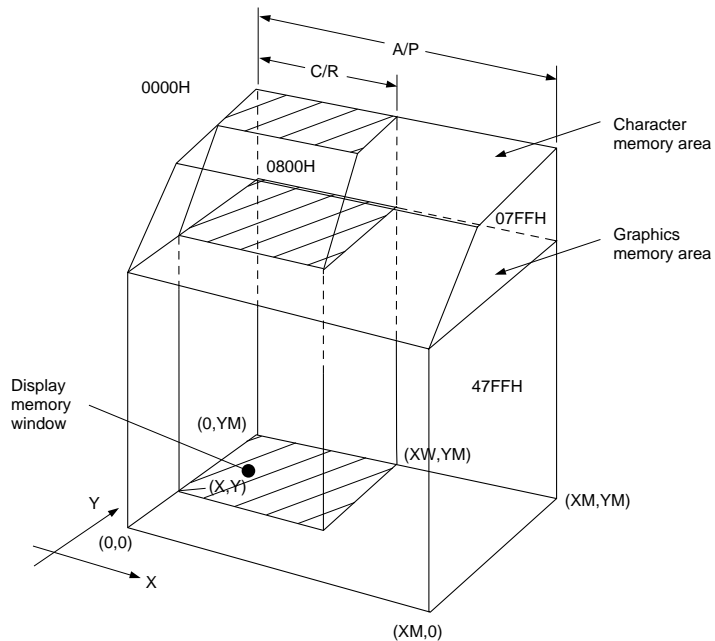


Figure 28. Virtual and physical screen relationship

### 9.2.2. Display address scanning

The S1D13305 series scans the display memory in the same way as a raster scan CRT screen. Each row is scanned from left to right until the address range equals C/R. Rows are scanned from top to bottom.

In graphics mode, at the start of each line, the address counter is set to the address at the start of the previous line plus the address pitch, AP.

In text mode, the address counter is set to the same start address, and the same character data is read, for each row in the character bitmap. However, a new row of the character generator output is used each time. Once all the rows in the character bitmap have been displayed, the address counter is set to the start address plus AP and the next line of text is displayed.

| 1 | SAD | SAD + 1 | SAD + 2 | | SAD + C/R |
|---|-----|---------|---------|--|-----------|
| 8 | | | | | |
| 9 | SAD + AP | SAD + AP + 1 | SAD + AP + 2 | | SAD + AP + C/R |
| 16 | | | | | |
| 17 | SAD + 2AP | | | | |
| 24 | | | | | |

$$\longleftarrow \text{C/R} \longrightarrow$$

W/S = 0, FX = 8, FY = 8
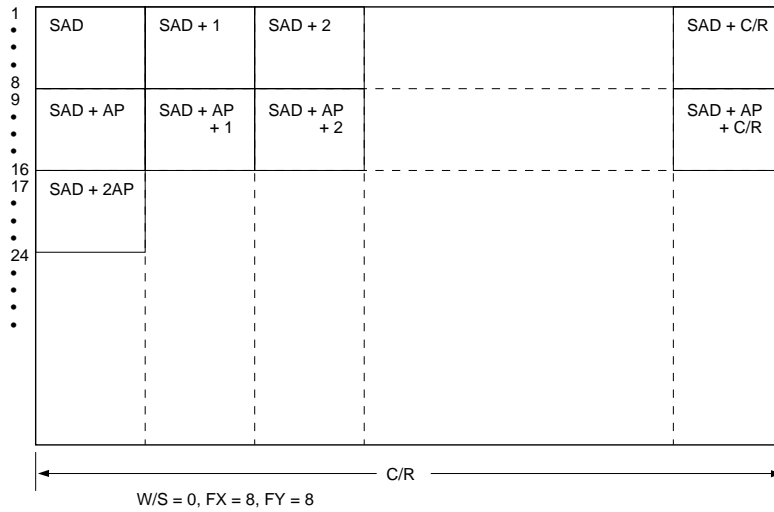
**Figure 29.   Character position parameters**

**Note:** One byte of display memory corresponds to one character.

| 1 | SAD | SAD +1 | SAD + 2 | | SAD + C/R |
|---|-----|--------|---------|--|-----------|
| 2 | SAD + AP | SAD + AP + 1 | SAD + AP + 2 | | SAD + AP + C/R |
| 3 | SAD + 2AP | | | | |

$$\longleftarrow \text{C/R} \longrightarrow$$

W/S = 0, FX = 8

Line 1
SAD
SAD +1
SAD + 2

SAD + C/R

AP

Line 2
SAD + AP
SAD + AP + 1

SAD + AP + C/R

AP

Line 3
SAD + 2AP
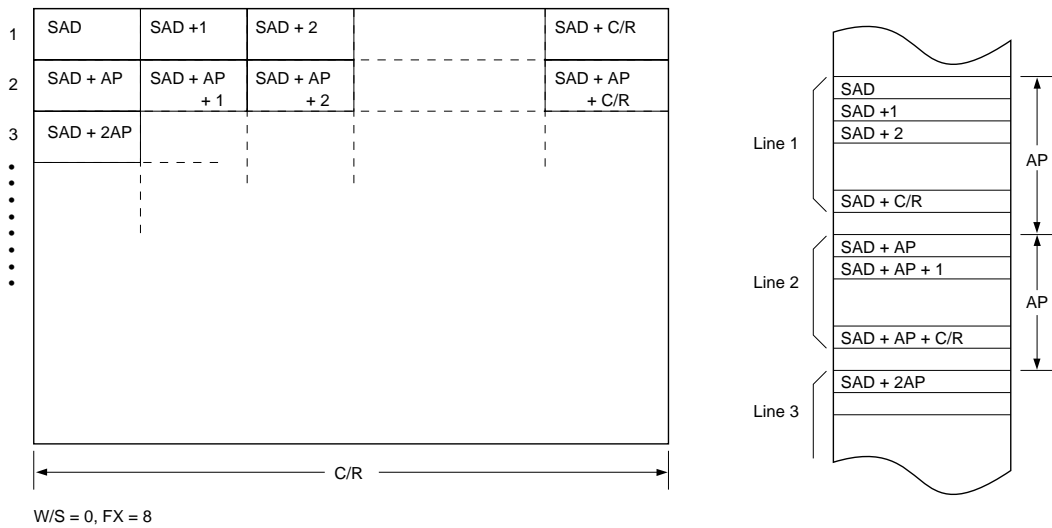
**Figure 30.   Character parameters vs. memory**

**Note:** One bit of display memory corresponds to one pixel.

| 1 | SAD1 | SAD1 + 1 | SAD1 + 2 | | SAD1 + C/R |
|---|---|---|---|---|---|
| • | | | | | |
| • | | | | | |
| • | | | | | |
| 8 | | | | | |
| 9 | SAD1 + AP | SAD1 + AP + 1 | SAD1 + AP + 2 | | SAD1 + AP + C/R |
| • | | | | | |
| • | | | | | |
| • | | | | | |
| 16 | | | | | |
| 17 | SAD1 + 2AP | | | | |
| • | | | | | |
| • | | | | | |
| • | | | | | |
| 24 | | | | | |
| 25 | | | | | |
| • | | | | | |
| • | | | | | |
| • | | | | | |
| (L/F)/2 = β | | | | | |
| β + 1 | SAD3 + 1 | | SAD3 + 2 | | SAD3 + C/R |
| • | | | | | |
| • | | | | | |
| β + 8 | | | | | |
| β + 9 | SAD3 + AP | SAD3 + AP + 1 | SAD3 + AP + 2 | | SAD3 + AP + C/R |
| • | | | | | |
| • | | | | | |
| β + 16 | | | | | |
| β + 17 | SAD3 + 2AP | | | | |
| • | | | | | |
| • | | | | | |
| • | | | | | |
| β + 24 | | | | | |
| β + 25 | | | | | |
| • | | | | | |
| • | | | | | |
| • | | | | | |
| (L/F) | | | | | |

C/R

W/S = 1, FX = 8, FY = 8
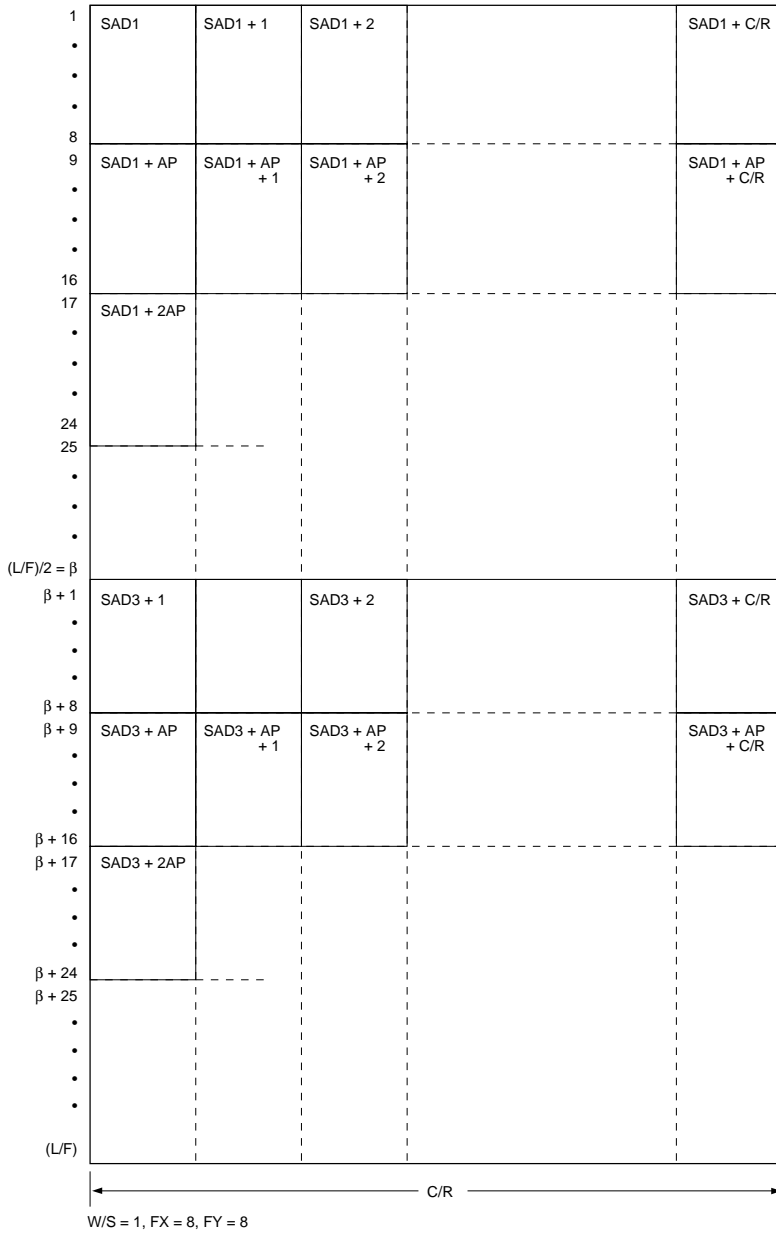
Figure 31.    Two-panel display address indexing

**Note**

In two-panel drive, the S1D13305 series reads line 1 and line β + 1 as one cycle.  The upper and lower panels are thus read alternately, one line at a time.

### 9.2.3. Display scan timing

Figure 32 shows the basic timing of the S1D13305 series. One display memory read cycle takes nine periods of the system clock, $\phi 0$ ($f_{OSC}$). This cycle repeats (C/R + 1) times per display line.

When reading, the display memory pauses at the end of each line for (TC/R - C/R) display memory read cycles, though the LCD drive signals are still generated. TC/R may be set to any value within the constraints imposed by C/R, $f_{OSC}$, $f_{FR}$, and the size of the LCD panel, and it may be used to fine tune the frame frequency. The microprocessor may also use this pause to access the display memory data.
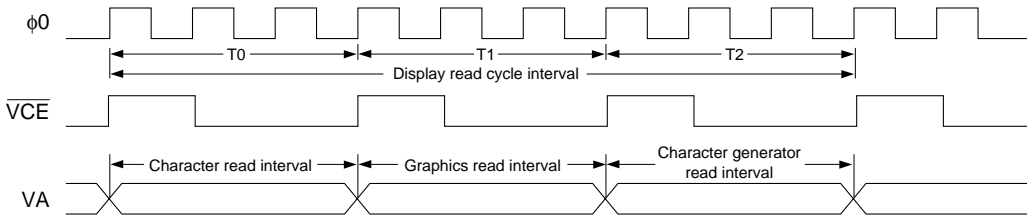
Figure 32.   Display memory basic read cycle
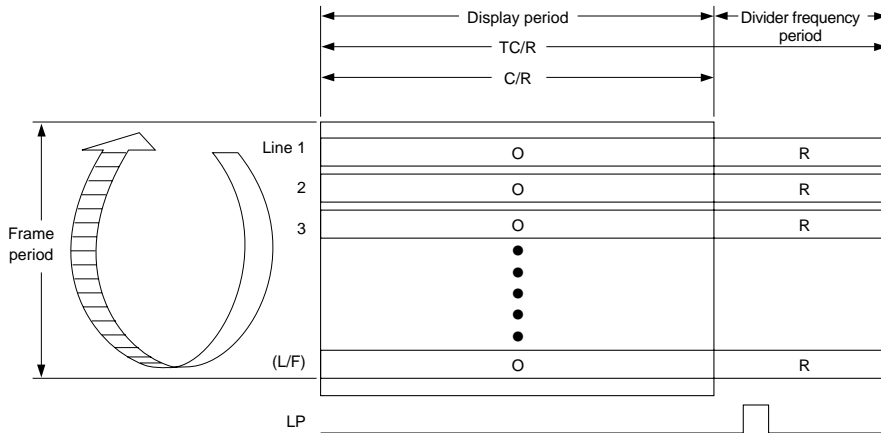
Figure 33.   Relationship between TC/R and C/R

**Note:** The divider adjustment interval (R) applies to both the upper and lower screens even if W/S = 1. In this case, LP is active only at the end of the lower screen's display interval.

## 9.3. Cursor Control

### 9.3.1. Cursor register function

The S1D13305 series cursor address register functions as both the displayed cursor position address register and the display memory access address register. When accessing display memory outside the actual screen memory, the address register must be saved before accessing the memory and restored after memory access is complete.
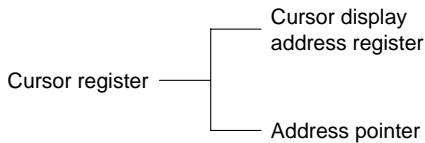
Figure 34. Cursor addressing

Note that the cursor may disappear from the display if the cursor address remains outside the displayed screen memory for more than a few hundred milliseconds.

### 9.3.2. Cursor movement

On each memory access, the cursor address register changes by the amount previously specified with CSRDIR, automatically moving the cursor to the desired location.

### 9.3.3. Cursor display layers

Although the S1D13305 series can display up to three layers, the cursor is displayed in only one of these layers:
Two-layer configuration: First layer (L1)
Three-layer configuration: Third layer (L3)
The cursor will not be displayed if it is moved outside the memory for its layer. Layers may be swapped or the cursor layer moved within the display memory if it is necessary to display the cursor on a layer other than the present cursor layer.

Although the cursor is normally displayed for character data, the S1D13305 series may also display a dummy cursor for graphical characters. This is only possible if the graphics screen is displayed, the text screen is turned off and the microprocessor generates the cursor control address.
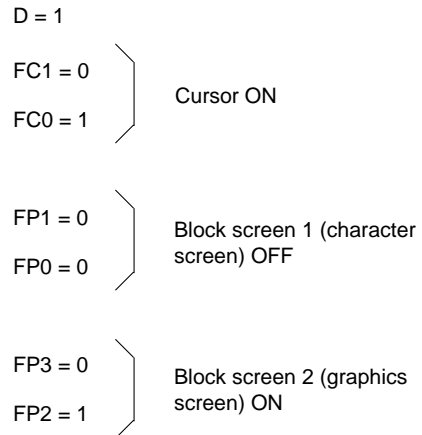
Figure 35. Cursor display layers

Consider the example of displaying Chinese characters on a graphics screen. To write the display data, the cursor address is set to the second screen block, but the cursor is not displayed. To display the cursor, the cursor address is set to an address within the blank text screen block.
Since the automatic cursor increment is in address units, not character units, the controlling microprocessor must set the cursor address register when moving the cursor over the graphical characters.
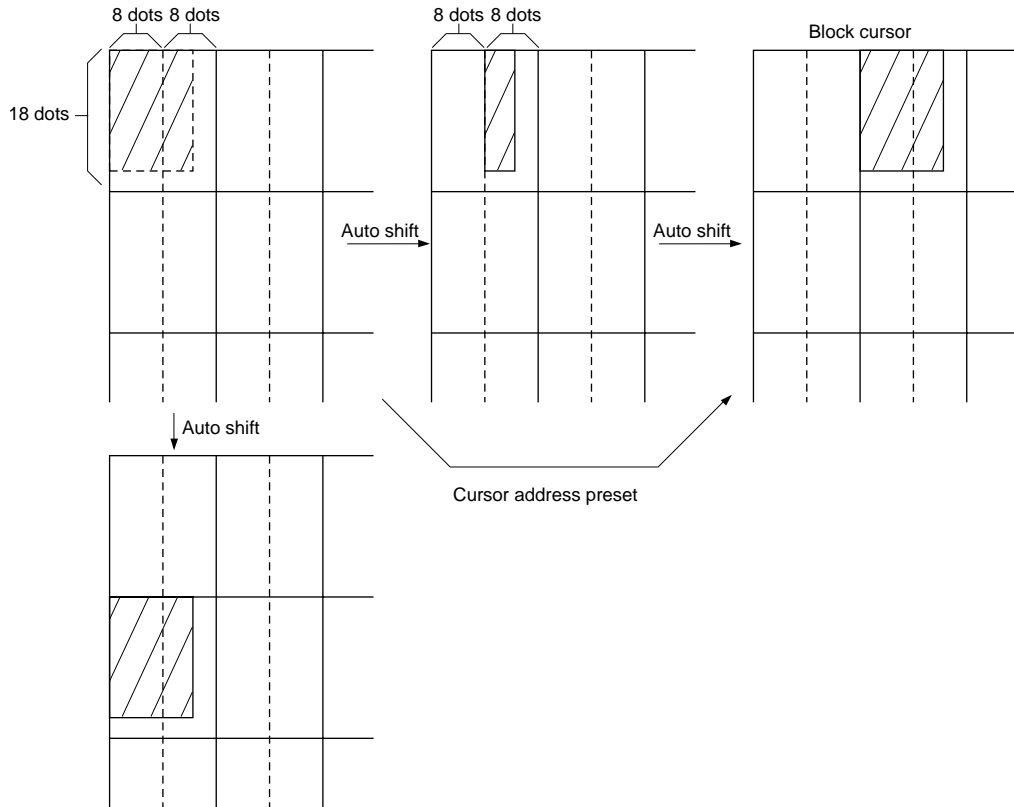
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Figure 36.   Cursor movement

If no text screen is displayed, only a bar cursor can be displayed at the cursor address.

If the first layer is a mixed text and graphics screen and the cursor shape is set to a block cursor, the S1D13305 series automatically decides which cursor shape to display. On the text screen it displays a block cursor, and on the graphics screen, a bar cursor.

## 9.4. Memory to Display Relationship

The S1D13305 series supports virtual screens that are larger than the physical size of the LCD panel address range, C/R. A layer of the S1D13305 series can be considered as a window in the larger virtual screen held in display memory. This window can be divided into two blocks, with each block able to display a different portion of the virtual screen.

This enables, for example, one block to dynamically scroll through a data area while the other acts as a status message display area. See Figure 37 and 38.



Figure 37.   Display layers and memory

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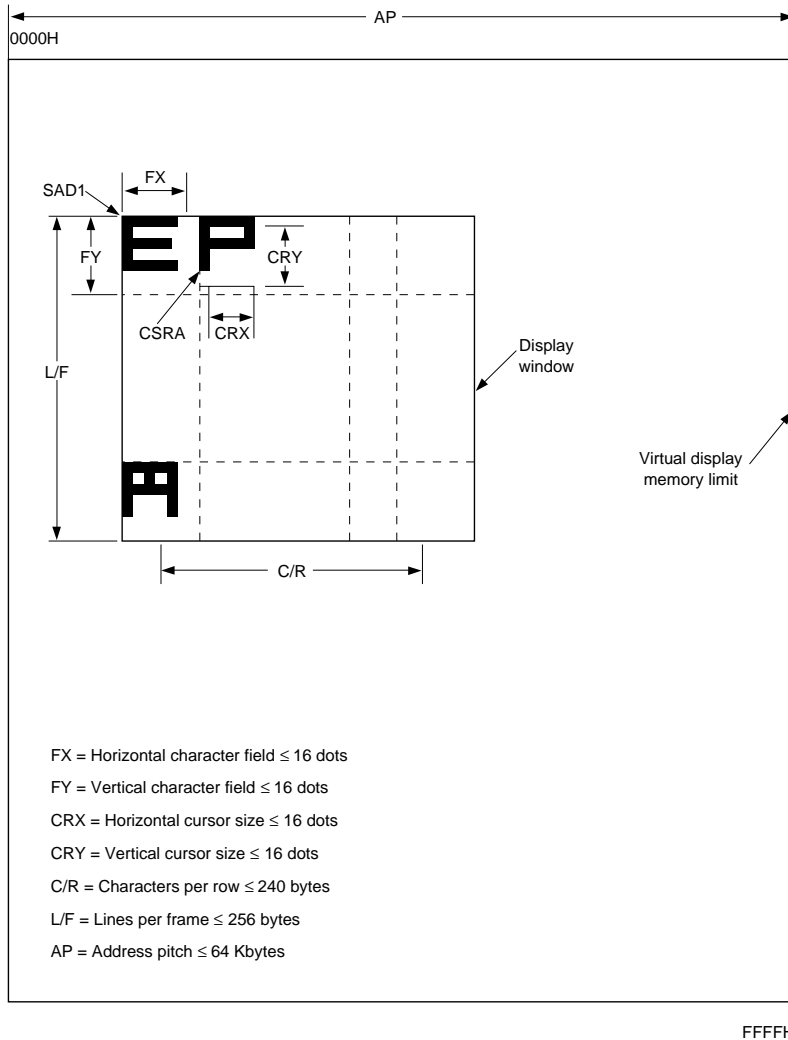
Figure 38.   Display window and memory

FX = Horizontal character field ≤ 16 dots

FY = Vertical character field ≤ 16 dots

CRX = Horizontal cursor size ≤ 16 dots

CRY = Vertical cursor size ≤ 16 dots

C/R = Characters per row ≤ 240 bytes

L/F = Lines per frame ≤ 256 bytes

AP = Address pitch ≤ 64 Kbytes
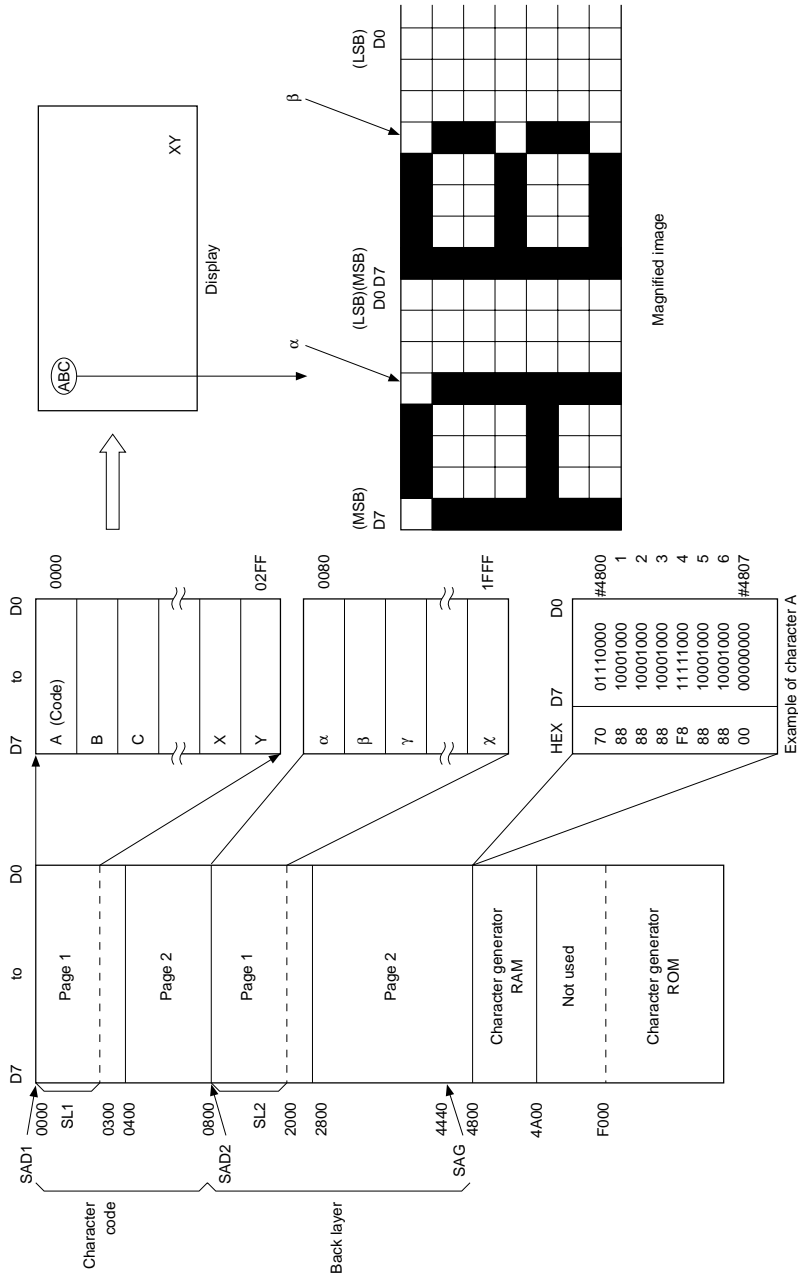
Figure 39.   Memory map and magnified characters

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## 9.5.  Scrolling

The controlling microprocessor can set the S1D13305 series scrolling modes by overwriting the scroll address registers SAD1 to SAD4, and by directly setting the scrolling mode and scrolling rate.

Since the S1D13305 series does not automatically erase the bottom line, it must be erased with blanking data when changing the scroll address register.

### 9.5.1.  On-page scrolling

The normal method of scrolling within a page is to move the whole display up one line and erase the bottom line.
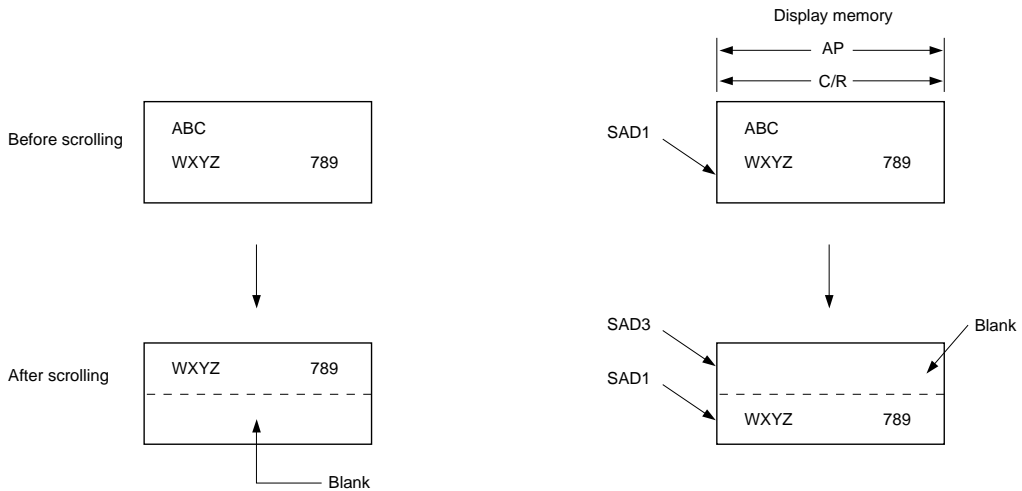
Figure 40.   On-page scrolling

### 9.5.2.  Inter-page scrolling

Scrolling between pages and page switching can be performed only if the display memory capacity is greater than one screen.
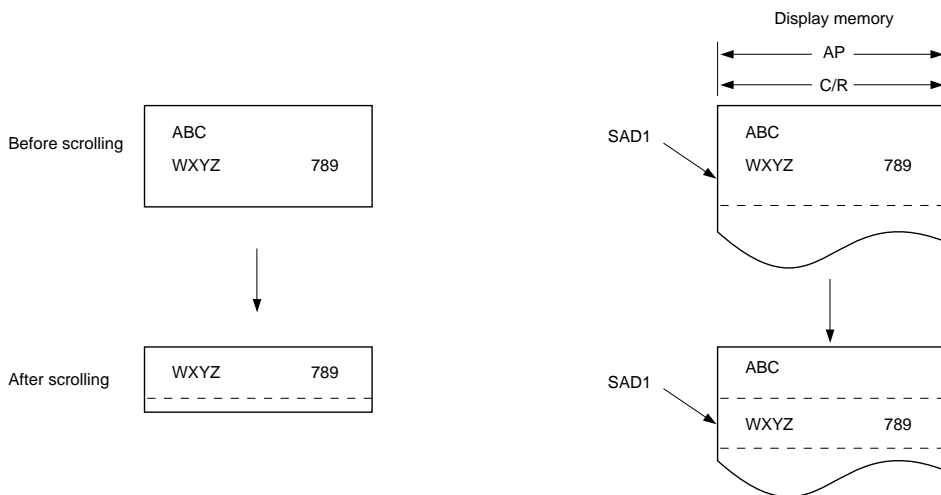
Figure 41.   Inter-page scrolling

### 9.5.3. Horizontal scrolling

The display can be scrolled horizontally in one-character
units, regardless of the display memory capacity.
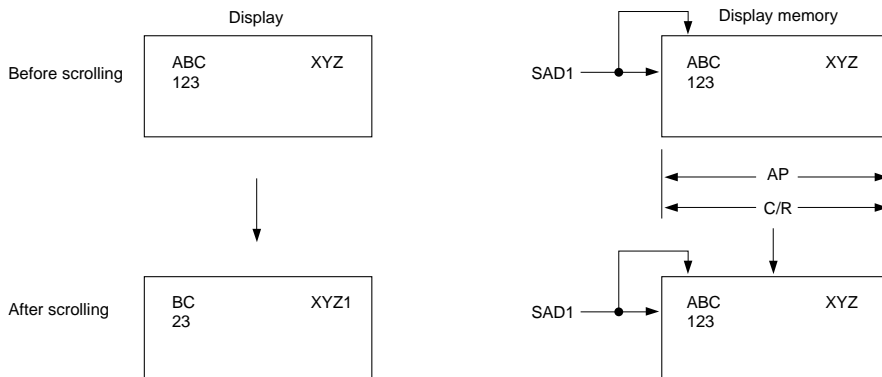


Figure 42. Horizontal wraparound scrolling

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## 9.5.4.  Bidirectional scrolling

Bidirectional scrolling can be performed only if the display memory is larger than the physical screen both horizontally and vertically. Although scrolling is normally done in single-character units, the HDOT SCR command can be used to scroll horizontally in pixel units. Single-pixel scrolling both horizontally and vertically can be performed by using the SCROLL and HDOT SCR commands. See Section 16.4
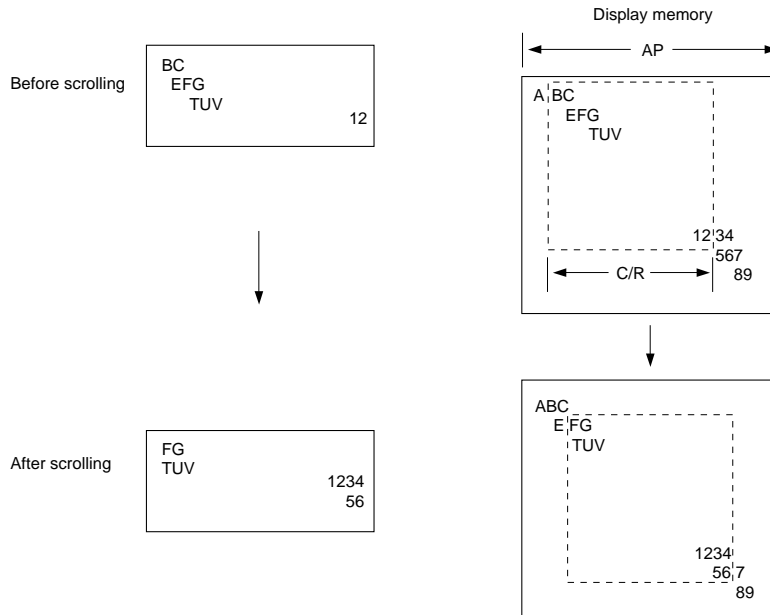


Figure 43.   Bidirectional scrolling

## 9.5.5.  Scroll units

Tale 19.   Scroll units

| Mode | Vertical | Horizontal |
|------|----------|------------|
| Text | Characters | Pixels or characters |
| Graphics | Pixels | Pixels |

Note that in a divided screen, each block cannot be independently scrolled horizontally in pixel units.

# 10. CHARACTER GENERATOR

## 10.1. CG Characteristics

### 10.1.1. Internal character generator

The internal character generator is recommended for minimum system configurations containing a S1D13305 series, display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator uses a CMOS mask ROM, it is also recommended for low-power applications.

- $5 \times 7$-pixel font (See Section 17.)
- 160 JIS standard characters
- Can be mixed with character generator RAM (maximum of 64 CG RAM characters)
- Can be automatically spaced out up to $8 \times 16$ pixels

### 10.1.2. External character generator ROM

The external CG ROM can be used when fonts other than those in the internal ROM are needed. Data is stored in the external ROM in the same format used in the internal ROM. (See Section 10.3.)

- Up to $8 \times 8$-pixel characters (M2 = 0) or $8 \times 16$-pixel characters (M2 = 1)
- Up to 256 characters (192 if used together with the internal ROM)
- Mapped into the display memory address space at F000H to F7FFH (M2 = 0) or F000H to FFFFH (M2 = 1)
- Characters can be up to $8 \times 16$-pixels; however, excess bits must be set to zero.

### 10.1.3. Character generator RAM

The user can freely use the character generator RAM for storing graphics characters. The character generator RAM can be mapped by the microprocessor anywhere in display memory, allowing effective use of unused address space.

- Up to $8 \times 8$-pixel characters (M2 = 0) or $8 \times 16$ characters (M2 = 1)
- Up to 256 characters if mapped at F000H to FFFFH (64 if used together with character generator ROM)
- Can be mapped anywhere in display memory address space if used with the character generator ROM
- Mapped into the display memory address space at F000H to F7FFH if not used with the character generator ROM (more than 64 characters are in the CG RAM). Set SAG0 to F000H and M1 to zero when defining characters number 193 upwards.

## 10.2.  CG Memory Allocation

Since the S1D13305 series uses 8-bit character codes, it can handle no more than 256 characters at a time. However, if a wider range of characters is required, character generator memory can be bank-switched using the CGRAM ADR command.
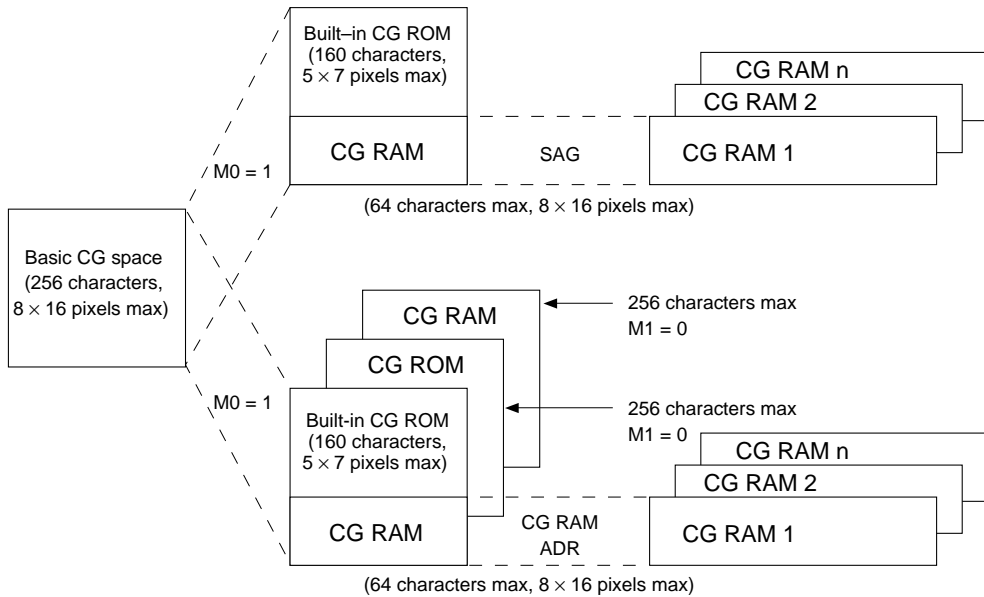


Figure 44.   Internal and external character mapping

Note that there can be no more than 64 characters per bank.

Table 20.   Character mapping

| Item | | Parameter | Remarks |
|---|---|---|---|
| Internal/external character generator selection | | M0 | |
| Character field height | 1 to 8 pixels | M2 = 0 | |
| | 9 to 16 pixels | M2 = 1 | |
| | Greater than 16 pixels | Graphics mode (8 bits × 1 line) | |
| Internal CG ROM/RAM select External CG ROM/RAM select | | Automatic | Determined by the character code |
| CG RAM bit 6 correction | | M1 | |
| CG RAM data storage address | | Specified with CG RAM ADR command | Can be moved anywhere in the display memory address space |
| External CG ROM address | 192 characters or less | Other than the area of Figure 49 | |
| | More than 192 characters | Set SAG to F000H and overly SAG and the CG ROM table | |

## 10.3.  Setting the Character Generator Address

The CG RAM addresses in the VRAM address space are not mapped directly from the address in the SAG register. The data to be displayed is at a CG RAM address calculated from SAG + character code + ROW select address. This mapping is shown in Table 21 and 22.

Table 21.  Character fonts, number of lines ≤ 8 (M2 = 0, M1 = 0)

| | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SAG | | | | | | | | | | | | | | | | |
| Character code | 0 | 0 | 0 | 0 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 0 | 0 | 0 |
| +ROW select address | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | R2 | R1 | R0 |
| CG RAM address | VA15 | VA14 | VA13 | VA12 | VA11 | VA10 | VA9 | VA8 | VA7 | VA6 | VA5 | VA4 | VA3 | VA2 | VA1 | VA0 |

Table 22.  Character fonts, 9 ≤ number of lines ≤ 16 (M2 = 1, M1 = 0)

| | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SAG | | | | | | | | | | | | | | | | |
| Character code | 0 | 0 | 0 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 0 | 0 | 0 | 0 |
| +ROW select address | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | R3 | R2 | R1 | R0 |
| CG RAM address | VA15 | VA14 | VA13 | VA12 | VA11 | VA10 | VA9 | VA8 | VA7 | VA6 | VA5 | VA4 | VA3 | VA2 | VA1 | VA0 |

| Row | R3 | R2 | R1 | R0 | |
|---|---|---|---|---|---|
| Row 0 | 0 | 0 | 0 | 0 | |
| Row 1 | 0 | 0 | 0 | 1 | |
| Row 2 | 0 | 0 | 1 | 0 | Line 1 |
| Row 7 | 0 | 1 | 1 | 1 | |
| Row 8 | 1 | 0 | 0 | 0 | Line 2 |
| Row 14 | 1 | 1 | 1 | 0 | |
| Row 15 | 1 | 1 | 1 | 1 | |
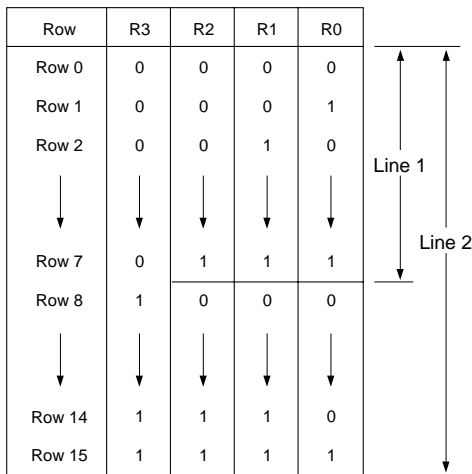
Figure 45.  Row select address

**Note:**  Lines = 1: lines in the character bitmap ≤ 8
Lines = 2: lines in the character bitmap ≥ 9

### 10.3.1.  M1 = 1

The S1D13305 series automatically converts all bits set in bit 6 of character code for CG RAM 2 to zero. Because of this, the CG RAM data areas become contiguous in display memory.

When writing data to CG RAM:
• Calculate the address as for M1 = 0.
• Change bit 6 of the character code from "1" to "0".

### 10.3.2.  CG RAM addressing example

- Define a pattern for the "A" in Figure 26.
- The CG RAM table start address is 4800H.
- The character code for the defined pattern is 80H (the first character code in the CG RAM area).

As the character code table in Figure 46 shows, codes 80H to 9FH and E0H to FFH are allocated to the CG RAM and can be used as desired. 80H is thus the first code for CG RAM. As characters cannot be used if only using graphics mode, there is no need to set the CG RAM data.

Table 23.   Character data example

| CGRAM AD | 5CH | Reverse the CG RAM address calculation to calculate SAG |
| P1 | 00H | |
| P2 | 40H | |
| CSRDIR | 4CH | Set cursor shift direction to right |
| CSRW | 46H | CG RAM start address is 4800H |
| P1 | 00H | |
| P2 | 48H | |
| MWRITE | 42H | |
| P | 70H | Write ROW 0 data |
| P2 | 88H | Write ROW 1 data |
| P3 | 88H | Write ROW 2 data |
| P4 | 88H | Write ROW 3 data |
| P5 | F8H | Write ROW 4 data |
| P6 | 88H | Write ROW 5 data |
| P7 | 88H | Write ROW 6 data |
| P8 | 00H | Write ROW 7 data |
| P8 | 00H | Write ROW 8 data |
| ↓ | ↓ | ↓ |
| P16 | 00H | Write ROW 15 data |

## 10.4. Character Codes

The following figure shows the character codes and the
codes allocated to CG RAM. All codes can be used by the
CG RAM if not using the internal ROM.

| Lower 4 bits | Upper 4 bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0 | | | | 0 | @ | P | ' | p | | | | | | | | |
| 1 | | | ! | 1 | A | Q | a | q | | | | | | | | |
| 2 | | | " | 2 | B | R | b | r | | | | | | | | |
| 3 | | | # | 3 | C | S | c | s | | | | | | | | |
| 4 | | | $ | 4 | D | T | d | t | | | | | | | | |
| 5 | | | % | 5 | E | U | e | u | | | | | | | | |
| 6 | | | & | 6 | F | V | f | v | | | | | | | | |
| 7 | | | ' | 7 | G | W | g | w | | | | | | | | |
| 8 | | | ( | 8 | H | X | h | x | | | | | | | | |
| 9 | | | ) | 9 | I | Y | i | y | | | | | | | | |
| A | | | * | : | J | Z | j | z | | | | | | | | |
| B | | | + | ; | K | [ | k | { | | | | | | | | |
| C | | | , | < | L | ¥ | l | ¦ | | | | | | | | |
| D | | | . | = | M | ] | m | } | | | | | | | | |
| E | | | - | > | N | ^ | n | $\rightarrow$ | | | | | | | | |
| F | | | / | ? | O | _ | o | $\leftarrow$ | | | | | | | | |

CG RAM1      CG RAM2

M1 = 0

M1 = 1

Figure 46.   On-chip character codes

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# 11. MICROPROCESSOR INTERFACE

## 11.1. System Bus Interface

SEL1, SEL2, A0, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the system address bus. SEL1 and SEL2 change the operation of the $\overline{RD}$ and $\overline{WR}$ pins to enable interfacing to either an 8080 or 6800 family bus, and should have a pull-up or pull-down resistor. With microprocessors using an 8080 family interface, the S1D13305 series is normally mapped into the I/O address space.

### 11.1.1. 8080 series

Table 24.   8080 series interface signals

| A0 | $\overline{RD}$ | $\overline{WR}$ | Function |
|----|----|----|---|
| 0 | 0 | 1 | Status flag read |
| 1 | 0 | 1 | Display data and cursor address read |
| 0 | 1 | 0 | Display data and parameter write |
| 1 | 1 | 0 | Command write |

### 11.1.2. 6800 series

Table 25.   6800 series interface signals

| A0 | R/$\overline{W}$ | E | Function |
|----|----|----|---|
| 0 | 1 | 1 | Status flag read |
| 1 | 1 | 1 | Display data and cursor address read |
| 0 | 0 | 1 | Display data and parameter write |
| 1 | 0 | 1 | Command write |

## 11.2. Microprocessor Synchronization

The S1D13305 series interface operates at full bus speed, completing the execution of each command within the cycle time, t$_{CYC}$. The controlling microprocessor's performance is thus not hampered by polling or handshaking when accessing the S1D13305 series.

Display flicker may occur if there is more than one consecutive access that cannot be ignored within a frame. The microprocessor can minimize this either by performing these accesses intermittently, or by continuously checking the status flag (D6) and waiting for it to become HIGH.

### 11.2.1. Display status indication output

When $\overline{CS}$, A0 and $\overline{RD}$ are LOW, D6 functions as the display status indication output. It is HIGH during the TV-mode vertical retrace period or the LCD-mode horizontal retrace period, and LOW, during the period the controller is writing to the display. By monitoring D6 and writing to the data memory only during retrace periods, the display can be updated without causing screen flicker.

### 11.2.2. Internal register access

The SYSTEM SET and SLEEP IN commands can be used to perform input/output to the S1D13305 series independently of the system clock frequency. These are the only commands that can be used while the S1D13305 series is in sleep mode.

### 11.2.3. Display memory access

The S1D13305 series supports a form of pipelined processing, in which the microprocessor synchronizes its processing to the S1D13305 series timing. When writing, the microprocessor first issues the MWRITE command. It then repeatedly writes display data to the S1D13305 series using the system bus timing. This ensures that the microprocessor is not slowed down even if the display memory access times are slower than the system bus access times. See Figure 47.

When reading, the microprocessor first issues the MREAD command, which causes the S1D13305 series to load the first read data into its output buffer. The microprocessor then reads data from the S1D13305 series using the system bus timing. With each read, the S1D13305 series reads the next data item from the display memory ready for the next read access. See Figure 48.
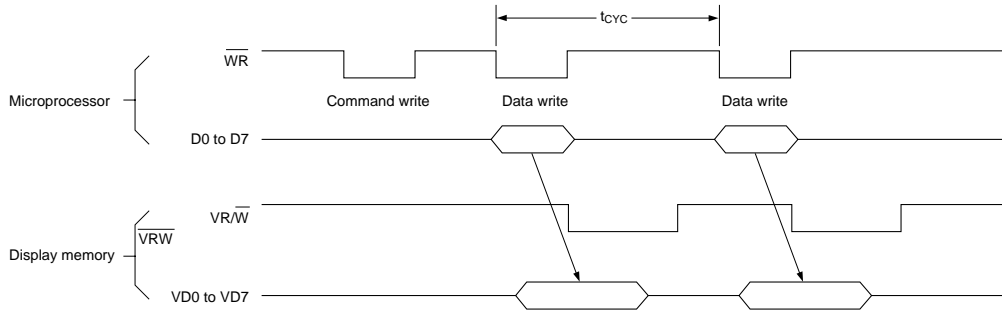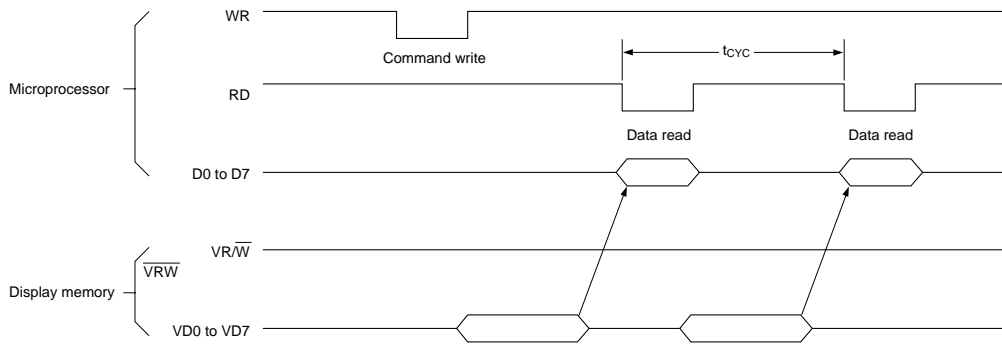
Figure 47.   Display memory write cycle



Figure 48.   Display memory read cycle

**Note**
A possible problem with the display memory read cycle is that the system bus access time, $t_{ACC}$, does not depend on the display memory access time, $t_{ACV}$.  The microprocessor may only make repeated reads if the read loop time exceeds the S1D13305 series cycle time, $t_{CYC}$.  If it does not, NOP instructions may be inserted in the program loop.  $t_{ACC}$, $t_{ACV}$ and $t_{CYC}$ limits are given in section 6.2.

## 11.3.  Interface Examples

### 11.3.1.  Z80 to S1D13305 series interface
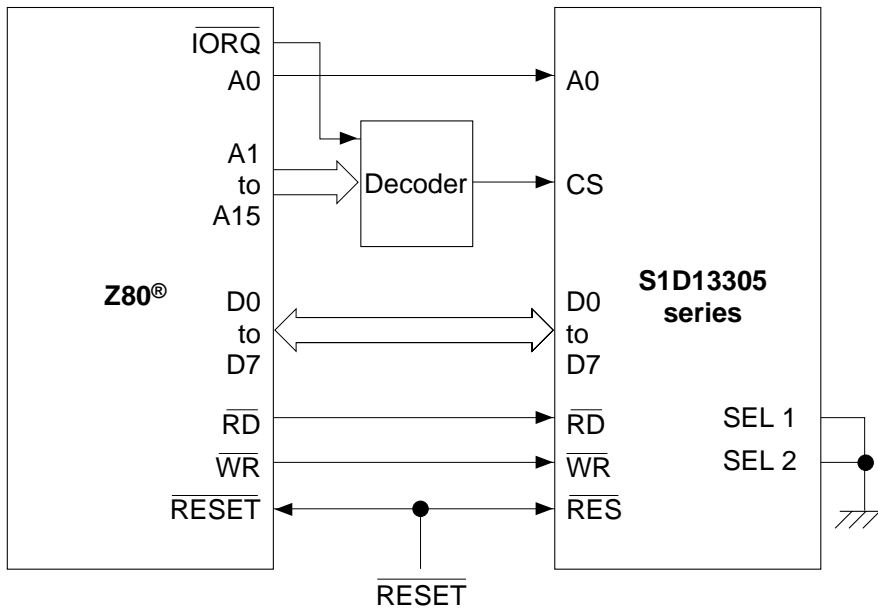


Figure 49.   Z80® to S1D13305 series interface

**Note:**  Z80® is a registered trademark of Zilog Corporation.

### 11.3.2.  6802 to S1D13305 series interface
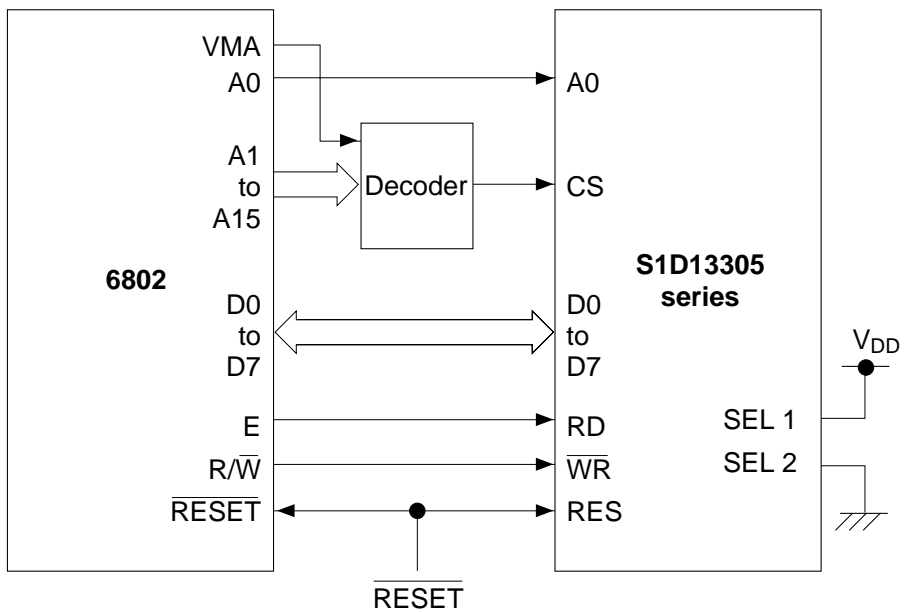


Figure 50.   6802 to S1D13305 series interface

# 12. DISPLAY MEMORY INTERFACE

## 12.1. Static RAM

The figure below shows the interface between an $8K \times 8$ static RAM and the S1D13305 series. Note that bus buffers are required if the bus is heavily loaded.

• S1D13305F
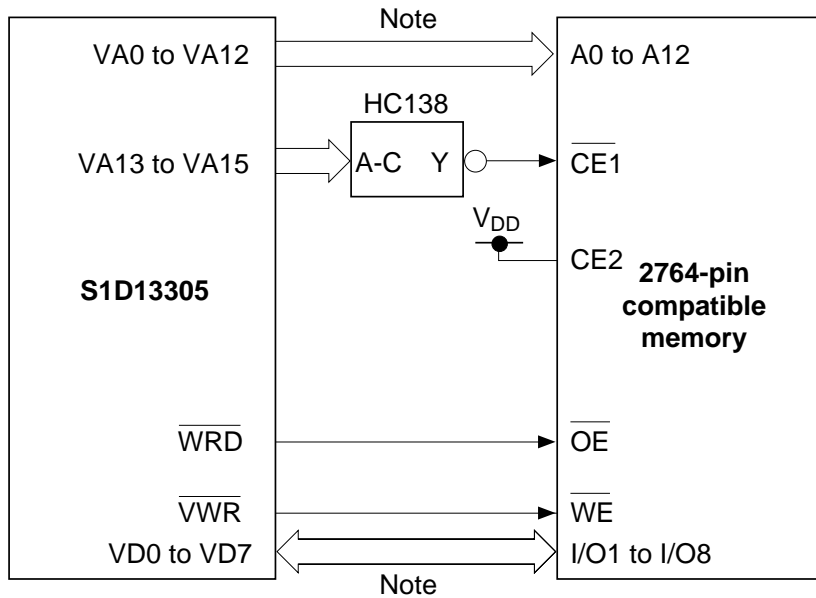


Figure 51. Static RAM interface

**Note**: If the bus load is too much, use a bus buffer.

**EPSON**

## 12.2.  Supply Current during Display Memory Access

The 24 address and data lines of the S1D13305 series cycle at one-third of the oscillator frequency, $f_{OSC}$. The charge and discharge current on these pins, $I_{VOP}$, is given by the equation below. When $I_{VOP}$ exceeds $I_{OPR}$, it can be estimated by:

$$I_{VOP} \propto C \, V \, f$$

where C is the capacitance of the display memory bus, V is the operating voltage, and f is the operating frequency.

If $V_{OPR} = 5.0V$, $f = 1.0\,MHz$, and the display memory bus capacitance is 1.0 pF per line:

$$I_{VOP} \leq 120\ \mu A\ /\ MHz \times pF$$

To reduce current flow during display memory accesses, it is important to use low-power memory, and to minimize both the number of devices and the parasitic capacitance.

# 13.  OSCILLATOR CIRCUIT

The S1D13305 series incorporates an oscillator circuit. A stable oscillator can be constructed simply by connecting an AT-cut crystal and two capacitors to XG and XD, as shown in the figure below. If the oscillator frequency is increased, $C_D$ and $C_G$ should be decreased proportionally.

Note that the circuit board lines to XG and XD must be as short as possible to prevent wiring capacitance from changing the oscillator frequency or increasing the power consumption.
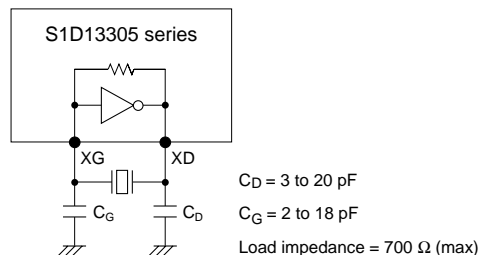


Figure 52.   Crystal oscillator

# 14.  STATUS FLAG

The S1D13305 series has a single bit status flag.
D6: X line standby
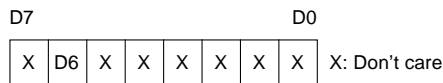


Figure 53.   Status flag

The D6 status flag is HIGH for the TC/R-C/R cycles at the end of each line where the S1D13305 series is not reading the display memory. The microprocessor may use this period to update display memory without affecting the display, however it is recommended that the display be turned off when refreshing the whole display.
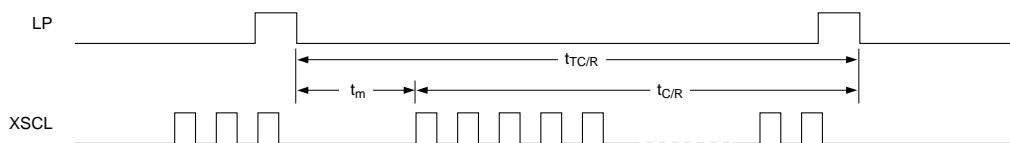


Figure 54.   C/R to TC/R time difference

| $\overline{CS}$ | A0 | $\overline{RD}$ | $D_6$ (flag) |
|---|---|---|---|
| 0 | 0 | 0 | 0:  Period of retrace lines<br>1:  Period of display |

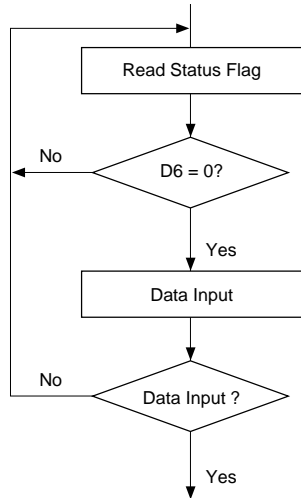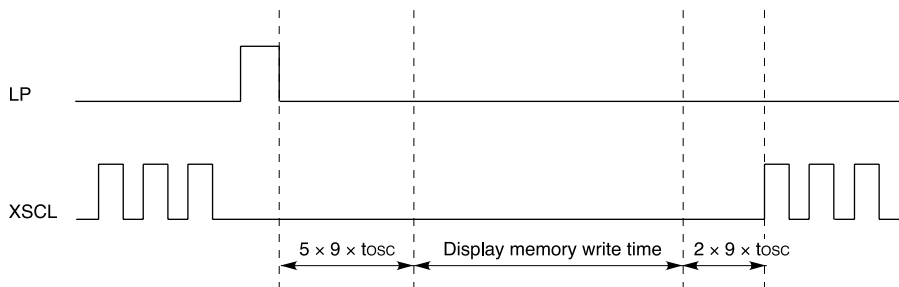Figure 55.   Flowchart for busy flag checking

## <Timing To Be Observed For Avoiding S1D 13305 Series Write Noise>

**• Precaution on the write timing to VRAM**



The allowable writing duration is since "$5 \times 9 \times t_{OSC}$" has elapsed ($t_{OSC} = 1/f_{OSC}$: a cycle of the oscillation frequency) from the positive going edge of LP up to $\{(TCR) - (C/R) - 7\} \times 9 \times t_{OSC}$.

Currently employed D6 status flag reading method does not identify the timing when the read D6 = Low took place.  Thus, negative going edge of LP should be used as the interrupt signal when implementing the writing in above timing.

If you try to access the display memory in other timing than the above, flickering of the display screen will result.

# 15. RESET
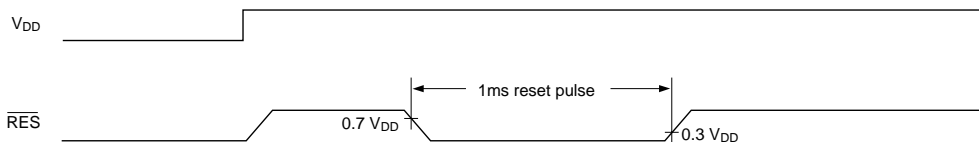


Figure 56.   Reset timing

The S1D13305 series requires a reset pulse at least 1 ms long after power-on in order to re-initialize its internal state.

For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the S1D13305 series is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse.

The S1D13305 series cannot receive commands while it is reset. Commands to initialize the internal registers should be issued soon after a reset.

During reset, the LCD drive signals XD, LP and FR are halted.

A delay of 3 ms (maximum) is required following the rising edges of both $\overline{\text{RES}}$ and $V_{DD}$ to allow for system stabilization.

# 16.   APPLICATION NOTES

## 16.1.   Initialization Parameters

The parameters for the initialization commands must be determined first. Square brackets around a parameter name indicate the number represented by the parameter, rather than the value written to the parameter register. For example, [FX] = FX + 1.

### 16.1.1.   SYSTEM SET instruction and parameters

❒ FX
The horizontal character field size is determined from the horizontal display size in pixels [VD] and the number of characters per line [VC].
$$[VD] / [VC] \le [FX]$$

❒ C/R
C/R can be determined from VC and FX.
$$[C/R] = RND ([FX] / 8) \times [VC]$$
where RND(x) denotes $x$ rounded up to the next highest integer. [C/R] is the number of bytes per line, not the number of characters.

❒ TC/R
TC/R must satisfy the condition $[TC/R] \ge [C/R] + 4$.

❒ $f_{OSC}$ and $f_{FR}$
Once TC/R has been set, the frame frequency, $f_{FR}$, and lines per frame [L/F] will also have been set. The lower limit on the oscillator frequency $f_{OSC}$ is given by:
$$f_{OSC} \ge ([TC/R] \times 9 + 1) \times [L/F] \times f_{FR}$$

❒ If no standard crystal close to the calculated value of $f_{OSC}$ exists, a higher frequency crystal can be used and the value of TC/R revised using the above equation.

❒ Symptoms of an incorrect TC/R setting are listed below. If any of these appears, check the value of TC/R and modify it if necessary.
  • Vertical scanning halts and a high-contrast horizontal line appears.
  • All pixels are on or off.
  • The LP output signal is absent or corrupted.
  • The display is unstable.

Table 26. Epson LCD unit example parameters

| Product name and resolution (X × Y) | [FX] | [FY] | [C/R] | TC/R | fosc (MHz) See Note 2. |
|---|---|---|---|---|---|
| 256 × 64 | [FX] = 6 pixels: 256 / 6 = 42 remainder 4 = 4 blank pixels | 8 or 16, depending on the screen | [C/R] = 42 = 2AH bytes: C/R = 29H. When using HDOT SCR, [C/R] = 43 bytes | 2DH | 1.85 |
| 512 × 64 | [FX] = 6 pixels: 512 / 6 = 85 remainder 2 = 2 blank pixels | 8 or 16, depending on the screen | [C/R] = 85 = 55H bytes: C/R = 54H. When using HDOT SCR, [C/R] = 86 bytes | 58H | 3.59 |
| 256 × 128 | [FX] = 8 pixels: 256 / 8 = 32 remainder 0 = no blank pixels | 8 or 16, depending on the screen | [C/R] = 32 = 20H bytes: C/R = 19H. When using HDOT SCR, [C/R] = 33 bytes | 22H | 2.90 |
| 512 × 128 | [FX] = 10 pixels: 512 / 10 = 51 remainder 2 = 2 blank pixels | 8 or 16, depending on the screen | [C/R] = 102 = 66H bytes: C/R = 65H. When using HDOT SCR, [C/R] = 103 bytes | 69H | 8.55 |

**Notes:**

1. The remainder pixels on the right-hand side of the display are automatically blanked by the S1D13305F. There is no need to zero the display memory corresponding to these pixels.

2. Assuming a frame frequency of 60 Hz.

## 16.1.2. Initialization example

The initialization example shown in Figure 57 is for a S1D13305 series with an 8-bit microprocessor interface bus and an Epson EG4810S-AR display unit (512 × 128 pixels).
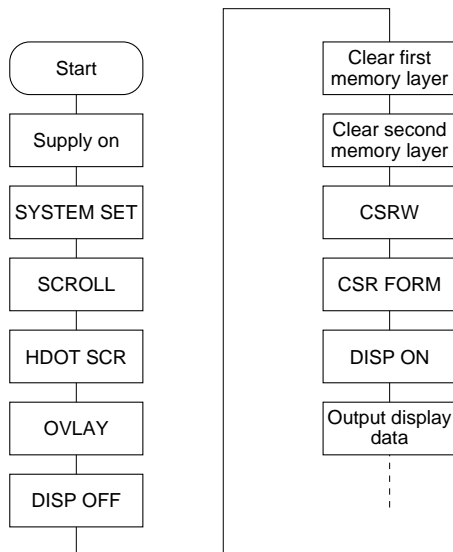


Figure 57. Initialization procedure

**Note:** Set the cursor address to the start of each screen's layer memory, and use MWRITE to fill the memory with space characters, 20H (text screen only) or 00H (graphics screen only). Determining which memory to clear is explained in section 16.1.3.

Table 27.  Initialization procedure

| No. | Command | Operation |
|-----|---------|-----------|
| 1 | Power-up | |
| 2 | Supply | |
| 3 | SYSTEM SET | |
| | C = 40H | |
| | P1 = 38H | M0: Internal CG ROM<br>M1: CG RAM is 32 characters maximum<br>M2: 8 lines per character<br>W/S: Two-panel drive<br>IV: No top-line compensation |
| | P2 = 87H | FX: Horizontal character size = 8 pixels<br>WF: Two-frame AC drive |
| | P3 = 07H | FY: Vertical character size = 8 pixels |
| | P4 = 3FH | C/R: 64 display addresses per line |
| | P5 = 49H | TC/R: Total address range per line = 90<br>$f_{OSC}$ = 6.0 MHz, $f_{FR}$ = 70 Hz |
| | P6 = 7FH | L/F: 128 display lines |
| | P7 = 80H<br>P8 = 00H | AP: Virtual screen horizontal size is 128 addresses |
| 4 | SCROLL | |
| | C = 44H | |
| | P1 = 00H<br>P2 = 00H | First screen block start address<br>Set to 0000H |
| | P3 = 40H | Display lines in first screen block = 64 |
| | P4 = 00H<br>P5 = 10H | Second screen block start address<br>Set to 1000H |
| | P6 = 40H | Display lines in second screen block = 64 |
| | P7 = 00H<br>P8 = 04H | Third screen block start address<br>Set to 0400H |
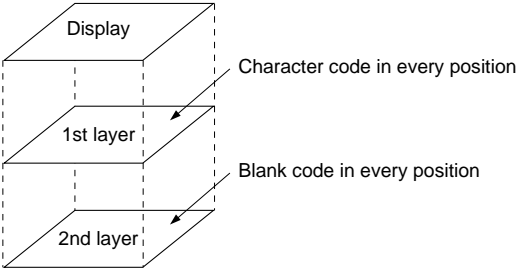
(continued)

Table 27. Initialization procedure (continued)

| No. | Command | Operation |
|---|---|---|
| | P9 = 00H | Fourth screen block start address |
| | P10 = 30H | Set to 3000H |
| | | Display memory |
| | | (SAD1) 0000H — 1st display memory page |
| | | (SAD3) 0400H — 2nd display memory page |
| | | 0800H |
| | | (SAD2) 1000H — 3rd display memory page |
| | | (SAD4) 3000H — 4th display memory page |
| | | 5000H |
| 5 | HDOT SCR | |
| | C = 5AH | |
| | P1 = 00H | Set horizontal pixel shift to zero |
| 6 | OVLAY | |
| | C = 5BH | |
| | P1 = 01H | MX 1, MX 0: Inverse video superposition |
| | | DM 1: First screen block is text mode |
| | | DM 2: Third screen block is text mode |
| 7 | DISP ON/OFF | |
| | C = 58H | D: Display OFF |
| | P1 = 56H | FC1, FC0: Flash cursor at 2 Hz |
| | | FP1, FP0: First screen block ON |
| | | FP3, FP2: Second and fourth screen blocks ON |
| | | FP5, FP4: Third screen block ON |
| 8 | Clear data in first layer | Fill first screen layer memory with 20H (space character) |

(continued)

Table 27.   Initialization procedure (continued)

| No. | Command | Operation |
|---|---|---|
| 9 | Clear data in second layer | Fill second screen layer memory with 00H (blank data)<br><br> |
| 10 | CSRW<br>C = 46H<br>P1 = 00H<br>P2 = 00H | Set cursor to start of first screen block |
| 11 | CSR FORM<br>C = 5DH<br>P1 = 04H<br>P2 = 86H | CRX: Horizontal cursor size = 5 pixels<br>CRY: Vertical cursor size = 7 pixels<br>CM: Block cursor |
| 12 | DISP ON/OFF<br>C = 59H | Display ON<br><br> |
| 13 | CSR DIR<br>C = 4CH | Set cursor shift direction to right |

(continued)

www.DataSheet4U.com
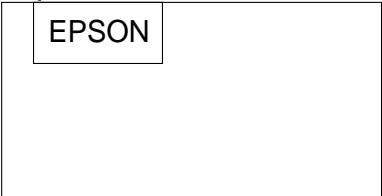
Table 27.   Initialization procedure (continued)

| No. | Command | Operation |
|-----|---------|-----------|
| 14 | MWRITE<br>C = 42H<br><br>P1 = 20H<br>P2 = 45H<br>P3 = 50H<br>P4 = 53H<br>P5 = 4FH<br>P6 = 4EH | <br><br>' '<br>'E'<br>'P'<br>'S'<br>'O'<br>'N'<br><br>EPSON■ |
| 15 | CSRW<br>C = 46H<br><br>P1 = 00H<br>P2 = 10H | <br><br>Set cursor to start of second screen block |
| 16 | CSR DIR<br>C = 4FH | <br>Set cursor shift direction to down |
| 17 | MWRITE<br>C = 42H<br><br>P1 = FFH<br>↓<br>P9 = FFH | <br><br>Fill in a square to the left of the 'E'<br><br>■EPSON |
| 18 | CSRW<br>C = 46H<br><br>P1 = 01H<br>P2 = 10H | <br><br>Set cursor address to 1001H |
| 19 | MWRITE<br>C = 42H | |

(continued)

Table 27. Initialization procedure (continued)

| No. | Command | Operation |
|---|---|---|
| | P1 = FFH | Fill in the second screen block in the second column of line 1 |
| | ↓ | |
| | P9 = FFH | |
| 20 | CSRW | Repeat operations 18 and 19 to fill in the background under 'EPSON' |
| ↓ | | |
| 29 | MWRITE | Inverse display <br><br> EPSON |
| 30 | CSRW | |
| | C = 46H | |
| | P1 = 00H | Set cursor to line three of the first screen block |
| | P2 = 01H | |
| 31 | CSR DIR | |
| | C = 4CH | Set cursor shift direction to right |
| 32 | MWRITE | |
| | C = 42H | |
| | P1 = 44H | 'D' |
| | P2 = 6FH | 'o' |
| | P3 = 74H | 't' |
| | P4 = 20H | ' ' Inverse display |
| | P5 = 4DH | 'M' |
| | P6 = 61H | 'a' EPSON |
| | P7 = 74H | 't' |
| | P8 = 72H | 'r' |
| | P9 = 69H | 'i' Dot matrix LCD |
| | P10 = 78H | 'x' |
| | P11 = 20H | ' ' |
| | P12 = 4CH | 'L' |
| | P13 = 43H | 'C' |
| | P14 = 44H | 'D' |

### 16.1.3. Display mode setting example 1: combining text and graphics

❒ Conditions
- 320 × 200 pixels, single-panel drive (1/200 duty cycle)
- First layer: text display
- Second layer: graphics display
- 8 × 8-pixel character font
- CG RAM not required

❒ Display memory allocation
- First layer (text): 320/8 = 40 characters per line, 200/8 = 25 lines. Required memory size = 40 × 25 = 1000 bytes.
- Second layer (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 40 × 200 = 8000 bytes.

```
                    03E8H
                    2nd graphics layer
                    (8000 bytes)

                                              2327H
        0000H
        1st character layer
        (1000 bytes)

                              03E7H
```
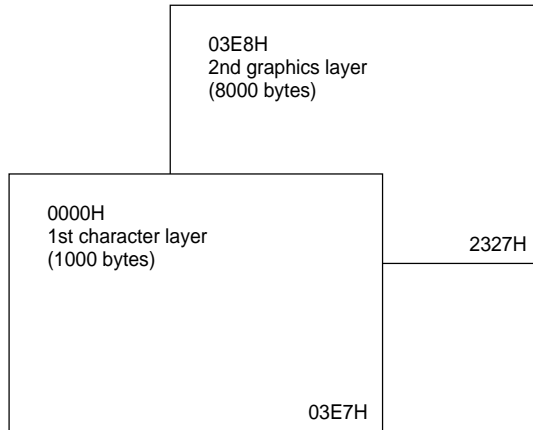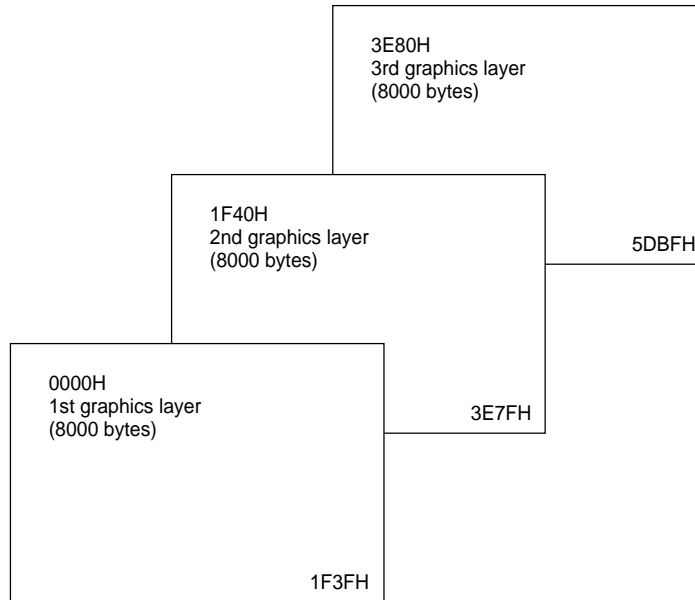
Figure 58.   Character over graphics layers

❒ Register setup procedure

SYSTEM SET   TC/R calculation
C =  40H
P1 = 30H     $f_{OSC}$ = 6 MHz
P2 = 87H     $f_{FR}$ = 70 Hz
P3 = 07H
P4 = 27H     (1/6) × 9 × [TC/R] × 200 = 1/70
P5 = 2FH     [TC/R] = 48, so TC/R = 2FH
P6 = C7H
P7 = 28H
P8 = 00H

SCROLL
C =  44H
P1 = 00H
P2 = 00H
P3 = C8H
P4 = E8H
P5 = 03H
P6 = C8H
P7 = XH
P8 = XH
P9 = XH
P10 = XH

**EPSON**

CSR FORM
C =    5DH
P1 =  04H
P2 =  86H

HDOT SCR
C =    5AH
P1 =  00H

OVLAY
C =    5BH
P1 =  00H

DISP ON/OFF
C =    59H
P1 =  16H

X =    Don't care

### 16.1.4.  Display mode setting example 2: combining graphics and graphics

❒ Conditions
  • $320 \times 200$ pixels, single-panel drive (1/ 200 duty cycle)
  • First layer: graphics display
  • Second layer: graphics display

❒ Display memory allocation
  • First layer (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 40 $\times$ 200 = 8000 bytes.
  • Second layer (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 8000 bytes.

1F40H
2nd graphics layer
(8000 bytes)

3E7FH

0000H
1st graphics layer
(8000 bytes)

1F3FH
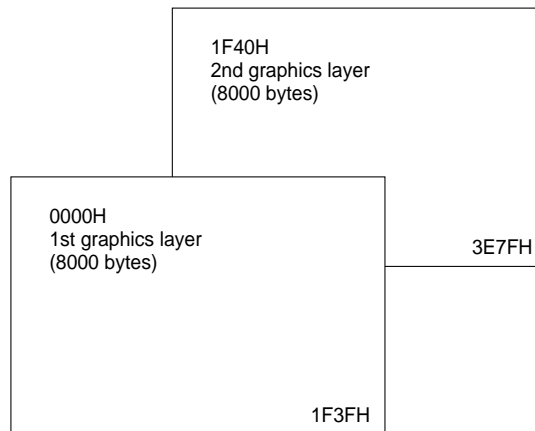
Figure 59.   Two-layer graphics

❐ Register setup procedure

SYSTEM SET   TC/R calculation

C =   40H
P1 =  30H       $f_{OSC}$ = 6 MHz
P2 =  87H       $f_{FR}$ = 70 Hz
P3 =  07H
P4 =  27H       $(1/6) \times 9 \times [TC/R] \times 200 = 1/70$
P5 =  2FH       [TC/R] = 48, so TC/R = 2FH
P6 =  C7H
P7 =  28H
P8 =  00H

SCROLL
C =   44H
P1 =  00H
P2 =  00H
P3 =  C8H
P4 =  40H
P5 =  1FH
P6 =  C8H
P7 =  XH
P8 =  XH
P9 =  XH
P10 = XH

CSR FORM
C =   5DH
P1 =  07H
P2 =  87H

HDOT SCR
C =   5AH
P1 =  00H

OVLAY
C =   5BH
P1 =  0CH

DISP ON/OFF
C =   59H
P1 =  16H

X = Don't care

## 16.1.5.   Display mode setting example 3: combining three graphics layers

❒ Conditions
  • 320 × 200 pixels, single-panel drive (1/200 duty cycle)
  • First layer: graphics display
  • Second layer: graphics display
  • Third layer: graphics display

❒ Display memory allocation
  • All layers (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 40 × 200 = 8000 bytes.



Figure 60.   Three-layer graphics

❒ Register setup procedure

SYSTEM SET  TC/R calculation

C  =  40H
P1 =  30H       $f_{OSC}$ = 6 MHz
P2 =  87H       $f_{FR}$ = 70 Hz
P3 =  07H
P4 =  27H       (1/6) × 9 × [TC/R] × 200 = 1/70
P5 =  2FH       [TC/R] = 48, so TC/R = 2FH
P6 =  C7H
P7 =  28H
P8 =  00H

SCROLL

C  =  44H
P1 =  00H
P2 =  00H
P3 =  C8H
P4 =  40H
P5 =  1FH
P6 =  C8H
P7 =  80H
P8 =  3EH
P9 =  XH
P10 = XH

CSR FORM
C =   5DH
P1 =  07H
P2 =  87H

HDOT SCR
C =   5AH
P1 =  00H

OVLAY
C =   5BH
P1 =  1CH

DISP ON/OFF
C =   59H
P1 =  16H

X = Don't care

## 16.2.  System Overview

Figure 61 shows the S1D13305 series in a typical system. The microprocessor issues instructions to the S1D13305 series, and the S1D13305 series drives the LCD panel and may have up to 64KB of display memory. Since all of the

LCD control circuits are integrated onto the S1D13305 series, few external components are required to construct a complete medium- resolution liquid crystal display.
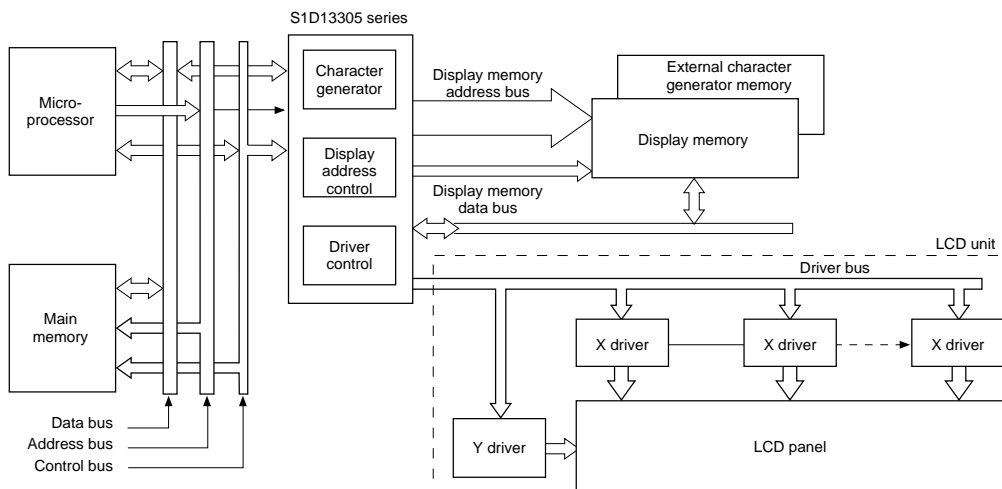


Figure 61.   System block diagram

## 16.3. System Interconnection

### 16.3.1. S1D13305F
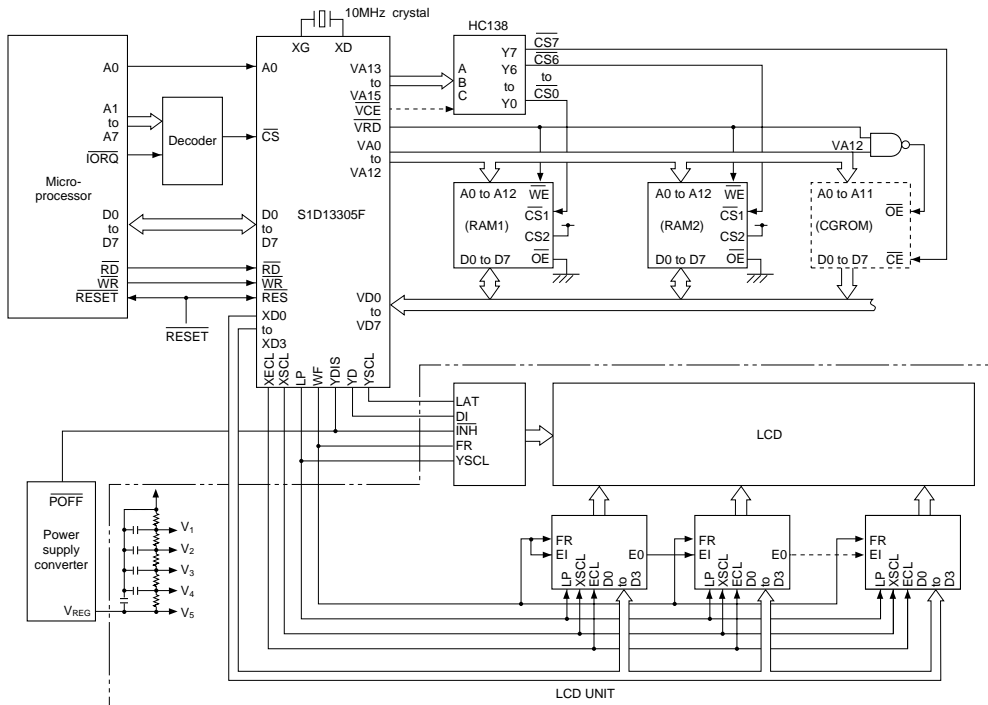


Figure 62. System interconnection diagram

The S1D13305 series layered screens and flexible scroll-ing facilities support a range of display functions and reduces the load on the controlling microprocessor when displaying underlining, inverse display, text overlaid on graphics or simple animation.

These facilities are supported by the S1D13305 series ability to divide display memory into up to four different areas.

❏ Character code table
- Contains character codes for text display
- Each character requires 8 bits
- Table mapping can be changed by using the scroll start function

❏ Graphics data table
- Contains graphics bitmaps
- Word length is 8 bits
- Table mapping can be changed

❏ CG RAM table
- Character generator memory can be modified by the external microprocessor
- Character sizes up to $8 \times 16$-pixels (16 bytes per character)
- Maximum of 64 characters
- Table mapping can be changed

❏ CG ROM table
- Used when the internal character generator is not adequate
- Can be used in conjunction with the internal char-acter generator and external character generator RAM
- Character sizes up to $8 \times 16$-pixels (16 bytes per character)
- Maximum of 256 characters
- Fixed mapping at F000H to FFFFH

## 16.4.  Smooth Horizontal Scrolling

Figure 63 illustrates smooth display scrolling to the left. When scrolling left, the screen is effectively moving to the right, over the larger virtual screen.

Instead of changing the display start address SAD and shifting the display by eight pixels, smooth scrolling is achieved by repeatedly changing the pixel-shift parameter of the HDOT SCR command. When the display has been scrolled seven pixels, the HDOT SCR pixel-shift parameter is reset to zero and SAD incremented by one. Repeating this operation at a suitable rate gives the appearance of smooth scrolling.

To scroll the display to the right, the reverse procedure is followed.

When the edge of the virtual screen is reached, the microprocessor must take appropriate steps so that the display is not corrupted. The scroll must be stopped or the display modified.

Note that the HDOT SCR command cannot be used to scroll individual layers.
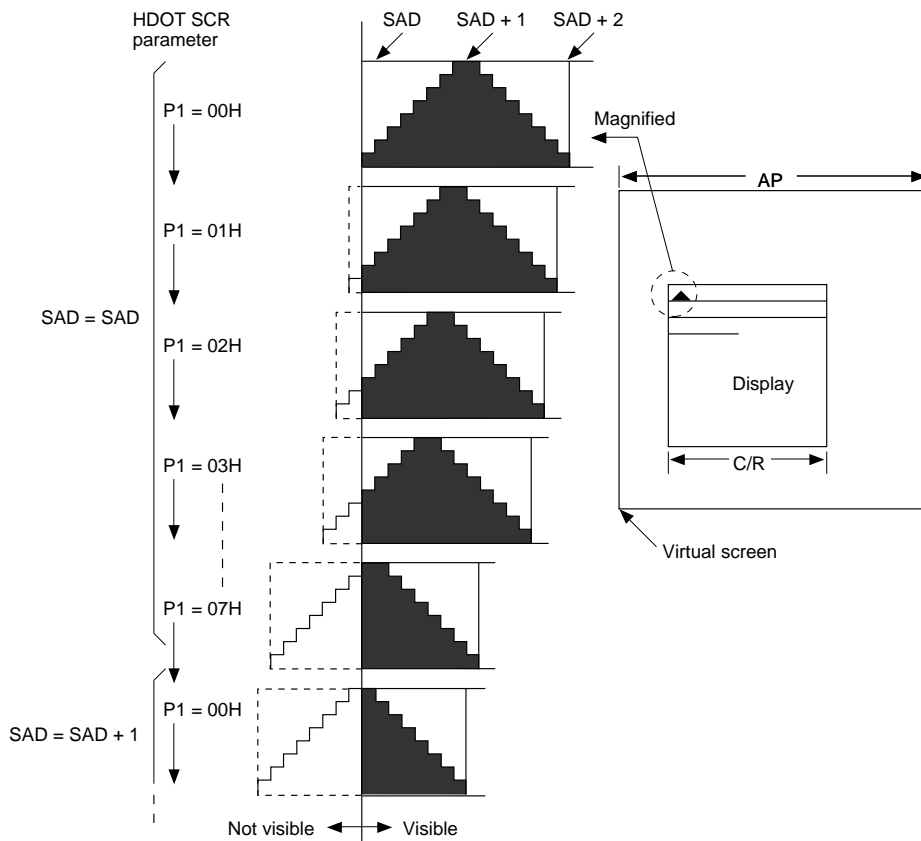
Figure 63.   HDOT SCR example

**Note:**  The response time of LCD panels changes considerably at low temperatures. Smooth scrolling under these conditions may make the display difficult to read.

## 16.5.  Layered Display Attributes

S1D13305 series incorporates a number of functions for enhanced displays using monochrome LCD panels. It allows the display of inverse characters, half-intensity menu pads and flashing of selected screen areas. These functions are controlled by the OVLAY and DISP ON/OFF commands.

| Attribute | MX1 | MX0 | Combined layer display | | 1st layer display | | 2ndt layer display |
|-----------|-----|-----|------------------------|---|-------------------|---|---------------------|
| Reverse | 0<br>1 | 1<br>1 | IV | EPSON | IV | EPSON | ///// |
| Half-tone | 0<br>1 | 0<br>1 | ME | Yes, No | ME | Yes, No | ///// |
| Local flashing | 0<br>0 | 0<br>1 | BL | Error | BL | | Error |
| Ruled line | 0<br>0<br>1 | 0<br>1<br>1 | RL | LINE<br>LINE | RL | LINE<br>LINE | LINE |

Figure 64.   Layer synthesis

A number of means can be used to achieve these effects, depending on the display configuration. These are listed below. Note, however, that not all of these can be used in the one layer at the same time.

### 16.5.1.  Inverse display

The first layer is text, the second layer is graphics.

1.  CSRW, CSDIR, MWRITE
    Write is into the graphics screen at the area to be inverted.

2.  OVLAY: MX0 = 1, MX1 = 0
    Set the combination of the two layers to Exclusive-OR.

3.  DISP ON/OFF: FP0 = FP1 = 1, FP1 = FP3 = 0.
    Turn on layers 1 and 2.

### 16.5.2.  Half-tone display

The FP parameter can be used to generate half-intensity display by flashing the display at 17 Hz. Note that this mode of operation may cause flicker problems with certain LCD panels.

#### 16.5.2.1.  Menu pad display

Turn flashing off for the first layer, on at 17 Hz for the second layer, and combine the screens using the OR function.
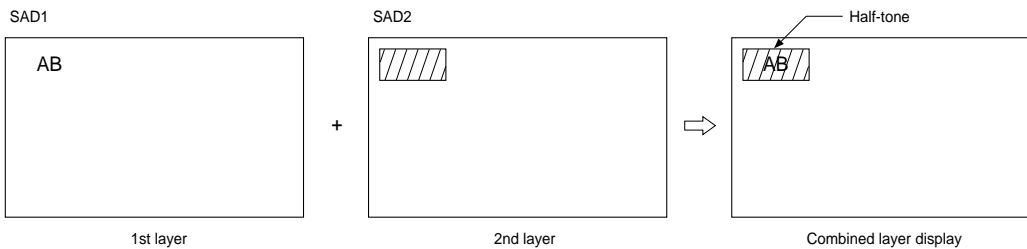1.  OVLAY: P1 = 00H
2.  DISP ON/OFF: P1 = 34H

Figure 65.   Half-tone character and graphics

### 16.5.2.2. Graph display

To present two overlaid graphs on the screen, configure the display as for the menu bar display and put one graph on each screen layer. The difference in contrast between the half- and full-intensity displays will make it easy to distinguish between the two graphs and help create an attractive display.

1. OVLAY: P1 = 00H
2. DISP ON/OFF: P1 = 34H

## 16.5.3. Flashing areas

### 16.5.3.1 Small area

To flash selected characters, the MPU can alternately write the characters as character codes and blank characters at intervals of 0.5 to 1.0 seconds.

### 16.5.3.2. Large area

Divide both layer 1 and layer 2 into two screen blocks each, layer 2 being divided into the area to be flashed and the remainder of the screen. Flash the layer 2 screen block at 2 Hz for the area to be flashed and combine the layers using the OR function.
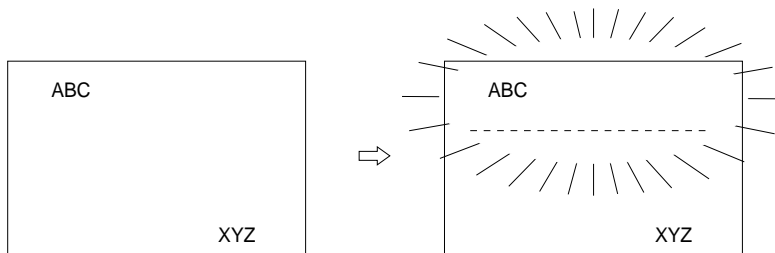


Figure 66. Localized flashing

## 16.6. 16 × 16-dot Graphic Display

### 16.6.1. Command usage

This example shows how to display 16 × 16-pixel characters. The command sequence is as follows:

CSRW      Set the cursor address.
CSRDIR    Set the cursor auto-increment direction.
MWRITE    Write to the display memory.

### 16.6.2. Kanji character display

The program for writing large characters operates as follows:

1. The microprocessor reads the character data from its ROM.
2. The microprocessor sets the display address and writes to the VRAM. The flowchart is shown in Figure 69.
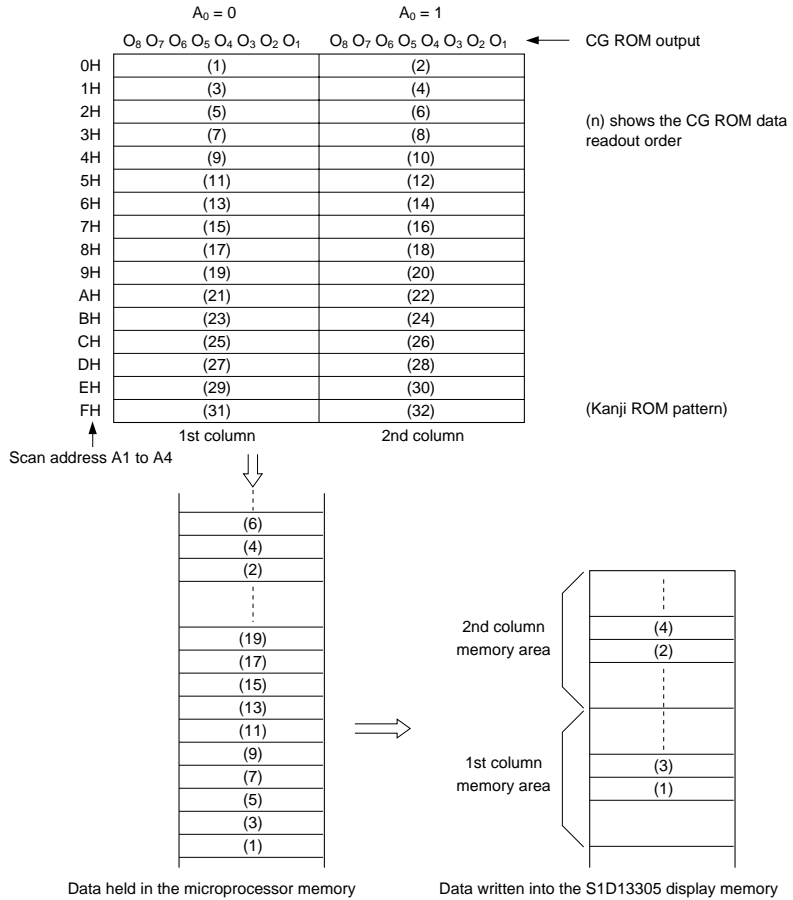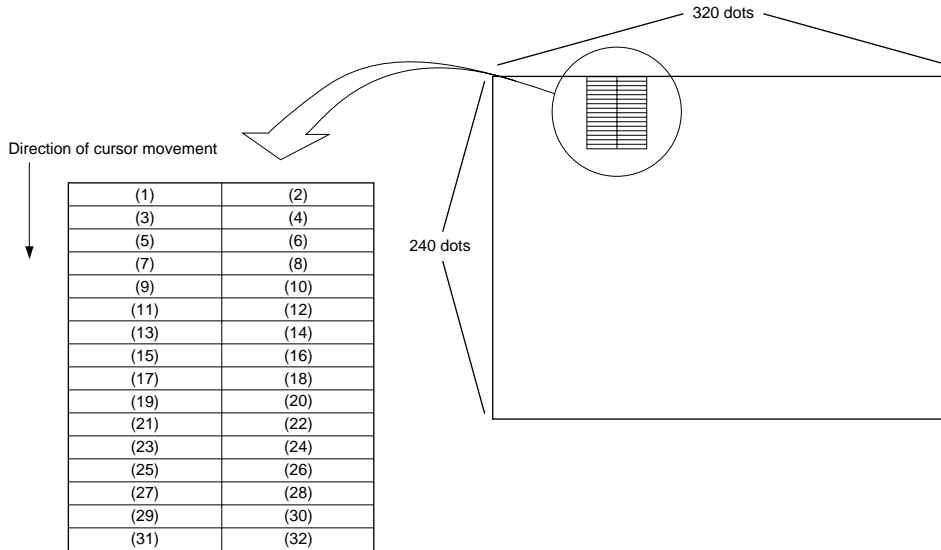
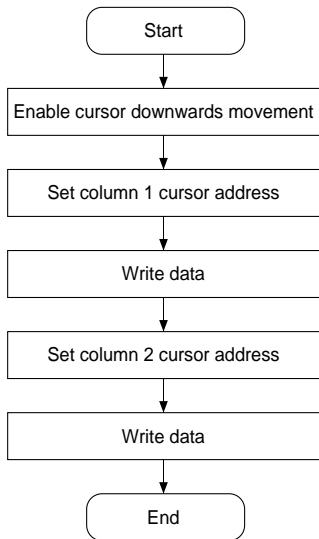Figure 67.   Graphics address indexing

**EPSON**

Figure 68.   Graphics bit map



Figure 69.   16 × 16-dot display flowchart

Using an external character generator ROM, and $8 \times 16$-pixel font can be used, allowing a $16 \times 16$-pixel character to be displayed in two segments. The external CG ROM EPROM data format is described in Section 9.1. This will allow the display of up to 128, $16 \times 16$-pixel characters. If CG RAM is also used, 96 fixed characters and 32 bank-switchable characters can also be supported.

## 17. INTERNAL CHARACTER GENERATOR FONT



Figure 70. On-chip character set

**Note**

The shaded positions indicate characters that have the whole $6 \times 8$ bitmap blackened.

# 18.  GLOSSARY OF TERMS

| | |
|---|---|
| A | Address |
| AP | Address pitch parameter |
| C | Character display mode |
| CD | Cursor direction of movement parameter |
| CG | Character generator |
| CGRAM ADR | Character generator memory address |
| CM | Cursor display shape parameter |
| C/R | Characters per row parameter |
| CRX | Horizontal cursor size parameter |
| CRY | Vertical cursor size parameter |
| CSR DIR | Cursor direction of movement instruction |
| CSR FORM | Cursor size, position and type instruction |
| CSRR | Read cursor address register instruction |
| CSRW | Write cursor address register instruction |
| DM | Display mode parameter |
| FC | Flashing cursor parameter |
| $f_{FR}$ | Frame frequency |
| $f_{OSC}$ | Oscillator frequency |
| FP | Screen flashing parameter |
| FX | Horizontal character size parameter |
| FY | Vertical character size parameter |
| G | Graphics display mode |
| GLC | Graphic line control unit |
| HDOT SCR | Horizontal scrolling by pixels instruction |
| IV | Screen origin compensation for inverse display |
| L/F | Lines per frame instruction |
| MREAD | Display memory read instruction |
| MWRITE | Display memory write instruction |
| MX | Screen composition mode |
| OV | Graphics layer select parameter |
| OVLAY | Screen layer mode instruction |
| P | Parameter |
| R | Row |
| RAM | Random access memory |
| ROM | Read only memory |
| SAD | Display scrolling start address parameter |
| SL | Display scrolling length parameter |
| TC/R | Length, including horizontal blanking, of one screen line |
| VRAM | Display memory |
| WF | Display drive waveform parameter |
| W/S | Windows per screen parameter |

**Request for Information on S1D13305 Series**

Dated:_____, 19____

Company: _____  Name of the inquiring person: _____

| The phenomenon occurred on: | Desired date of receiving the reply: _____ |
|---|---|

Device name:   S1D13305F00A/  S1D13305F00B          (Lot No.                    )

| Number of units of the device causing the phenomenon: __units<br><br>(Scope of occurrence:  ___ / ___ ) | Applications: |
|---|---|
| Your address:<br><br>Your phone number:         -        -        FAX:        -        - | Documents in your current possession: |

Image plane size:  ____ dots × ____ dots (single-plane drive/2-plane drive)

Using LCD module (manufacturer):      Frame frequency:                    Hz.

Display mode (circle either one)

(1)  First layer: Characters   Two-part plane,     Second layer: Graphics   Single plane
(2)  First layer: Characters   Single plane,       Second layer: Graphics   Single plane        < (1)' >
(3)  First layer: Characters   Two-part plane,     Second layer: Graphics   Two-part plane
(4)  First layer: Graphics     Two-part plane,     Second layer: Graphics   Single plane
(5)  First layer: Graphics     Single plane,       Second layer: Graphics   Single plane        < (4)' >
(6)  First layer: Graphics     Single plane,       Second layer: Graphics   Single plane,   Third layer: Graphics   Single plane
(7)  First layer: Graphics     Two-part plane,     Second layer: Graphics   Two-part plane

Initialization parameter: Give in decimals or duodecimals.

| System setting | Scroll | HDOT SCR | CSRFORM |
|---|---|---|---|
| P1(IV, W/S, M2, M1, M0)  = | P1(SADIL)  = | P1      = | P1     = |
| P2(W/F, FX)  = | P2(SADIH)  = | OVLAY | P2     = |
| P3(FY)  = | P3(SL1)  = | P1      = |  |
| P4(C/R)  = | P4(SAD2L)  = | DISP ON/OFF |  |
| P5(TC/R)  = | P5(SAD2H)  = | P1      = |  |
| P6(L/F)  = | P6(SL2)  = | CSRW |  |
| P7(APL)  = | P7(SAD3L)  = | P1      = |  |
| P8(APH)  = | P8(SAD3H)  = | P2      = |  |
|  | P9(SAD4L)  = | CSR DIR |  |
|  | P10(SAD4H) = | C      = |  |

Oscillation frequency:                    MHz.     (internal/external)

CPU:                              CPU clock:                    MHz.

Frame memory capacity:                    Kb.     (using memory IC:                , access time:                    nsec.)

Descriptions of your inquiry (Give details such as what type of display is being sought for and which phenomenon is occurring.)

Attached documents (circuit diagram, timing chart, program list, or others)

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assists in creating the products of our customers' dreams.
**Epson IS energy savings.**

# S1D13305 Series
## Technical Manual

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ELECTRONIC DEVICES MARKETING DIVISION

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