EPSON

S1D13505F00A

Embedded RAMDAC LCD/CRT Controller

■ DESCRIPTION

The S1D13505 is a color/monochrome LCD/CRT graphics controller interfacing to a wide range of CPUs and display devices. The S1D13505 architecture is designed to meet the low cost, low power requirements of the embedded markets, such as Mobile Communications, Hand-Held PCs, and Office Automation.

The S1D13505 supports multiple CPUs, all LCD panel types, CRT, and additionally provides a number of differentiating features. Products requiring a “Portrait” mode display can take advantage of the SwivelView™ feature. Simultaneous, Virtual and Split Screen Display are just some of the display modes supported, while the Hardware Cursor, Ink Layer, and the Memory Enhancement Registers offer substantial performance benefits. These features, combined with the S1D13505's Operating System independence, make it an ideal display solution for a wide variety of applications.

■ FEATURES

◆ Memory Interface

- 16-bit DRAM interface:
  - EDO-DRAM up to 40MHz data rate (80M bytes per second).
  - FPM-DRAM up to 25MHz data rate (50M bytes per second).
- Memory size options:
  - 512K bytes using one 256K x 16 device.
  - 2M bytes using one 1M x 16 device.
- Performance Enhancement Register to tailor the memory control output timing for the DRAM device.

◆ CPU Interface

- Supports the following interfaces:
  - 8/16-bit SH-4 bus interface.
  - 8/16-bit SH-3 bus interface.
  - 8/16-bit interface to 8/16/32-bit MC68000 microprocessors/microcontrollers.
  - 8/16-bit interface to 8/16/32-bit MC68030 microprocessors/microcontrollers.
  - Philips PR31500/PR31700 (MIPS).
  - Toshiba TX3912 (MIPS).
  - Philips PR31500/PR31700.
  - 16-bit Power PC (MPC821) microprocessor.
  - 16-bit Epson E0C33 microprocessor.
  - PC Card (PCMCIA).
  - StrongARM (PC Card).
  - NEC VR41xx (MIPS).
  - ISA bus.
- Supports the following interface with external logic:
  - GX486 microprocessor.
- One-stage write buffer for minimum wait-state CPU writes.
- Registers are memory-mapped - the M/R# pin selects between the display buffer and register address space.
- The complete 2M byte display buffer address space is addressable as a single linear address space through the 21-bit address bus.

◆ Display Support

- 4/8-bit monochrome passive LCD interface.
- 4/8/16-bit color passive LCD interface.
- Single-panel, single-drive displays.
- Dual-panel, dual-drive displays.
- Direct support for 9/12-bit TFT/D-TFD; 18-bit TFT/D-TFD is supported up to 64K color depth (16-bit data).
- Embedded RAMDAC (DAC)with direct analog CRT drive.
- Simultaneous display of CRT and passive or TFT/D-TFD panels.

◆ Display Modes

- 1/2/4/8/15/16 bit-per-pixel (bpp) support on LCD/CRT.
- Up to 16 shades of gray using FRM on monochrome passive LCD panels.
- Up to 4096 colors on passive LCD panels; three 256x4 Look-Up Tables (LUT) are used to map 1/2/4/8 bpp modes into these colors, 15/16 bpp modes are mapped directly using the 4 most significant bits of the red, green and blue colors.
- Up to 64K colors on TFT/D-TFD LCD panels and CRT; three 256x4 Look-Up Tables are used to map 1/2/4/8 bpp modes into 4096 colors, 15/16 bpp modes are mapped directly.

◆ Display Features

- SwivelView™: direct hardware 90˚ rotation of display image for “portrait” mode display.
- Split Screen Display: allows two different images to be simultaneously viewed on the same display.
- Virtual Display Support: displays images larger than the display size through the use of panning.
- Double Buffering/multi-pages: provides smooth animation and instantaneous screen update.
- Acceleration of screen updates by allocating full display memory bandwidth to CPU (see REG[23h] bit 7).
- Hardware 64x64 pixel 2-bit cursor or full screen 2-bit ink layer.
- Simultaneous display of CRT and passive panel or TFT/D-TFD panel.
- Normal mode for cases where LCD and CRT screen sizes are identical.
- Line-doubling for simultaneous display of 240-line images on 240-line LCD and 480-line CRT.
- Even-scan or interlace modes for simultaneous display of 480-line images on 240-line LCD and 480-line CRT.

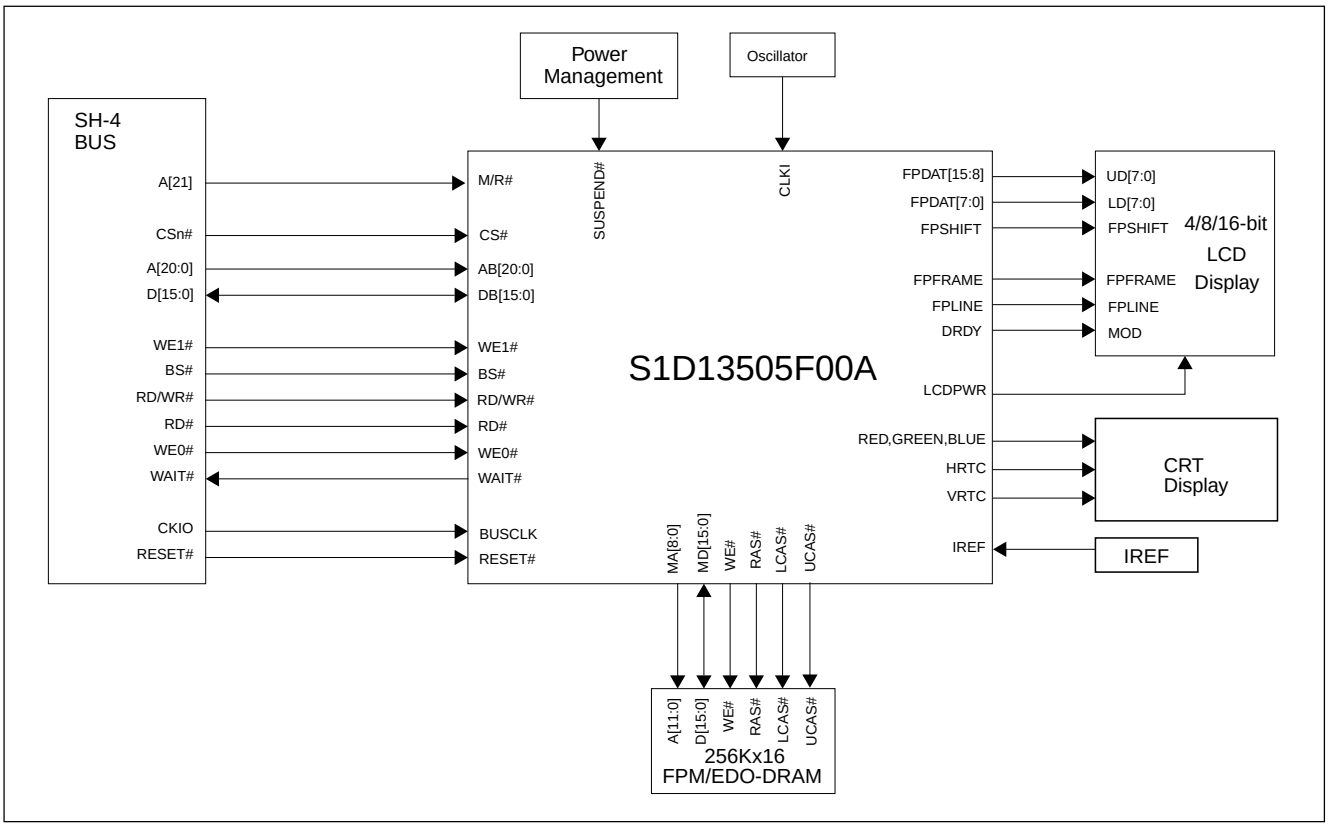
◆ Clock Source

- Single clock input for both the pixel and memory clocks.
- Memory clock can be input clock or (input clock/2), providing flexibility to use CPU bus clock as input.
- Pixel clock can be the memory clock, (memory clock/2), (memory clock/3) or (memory clock/4).

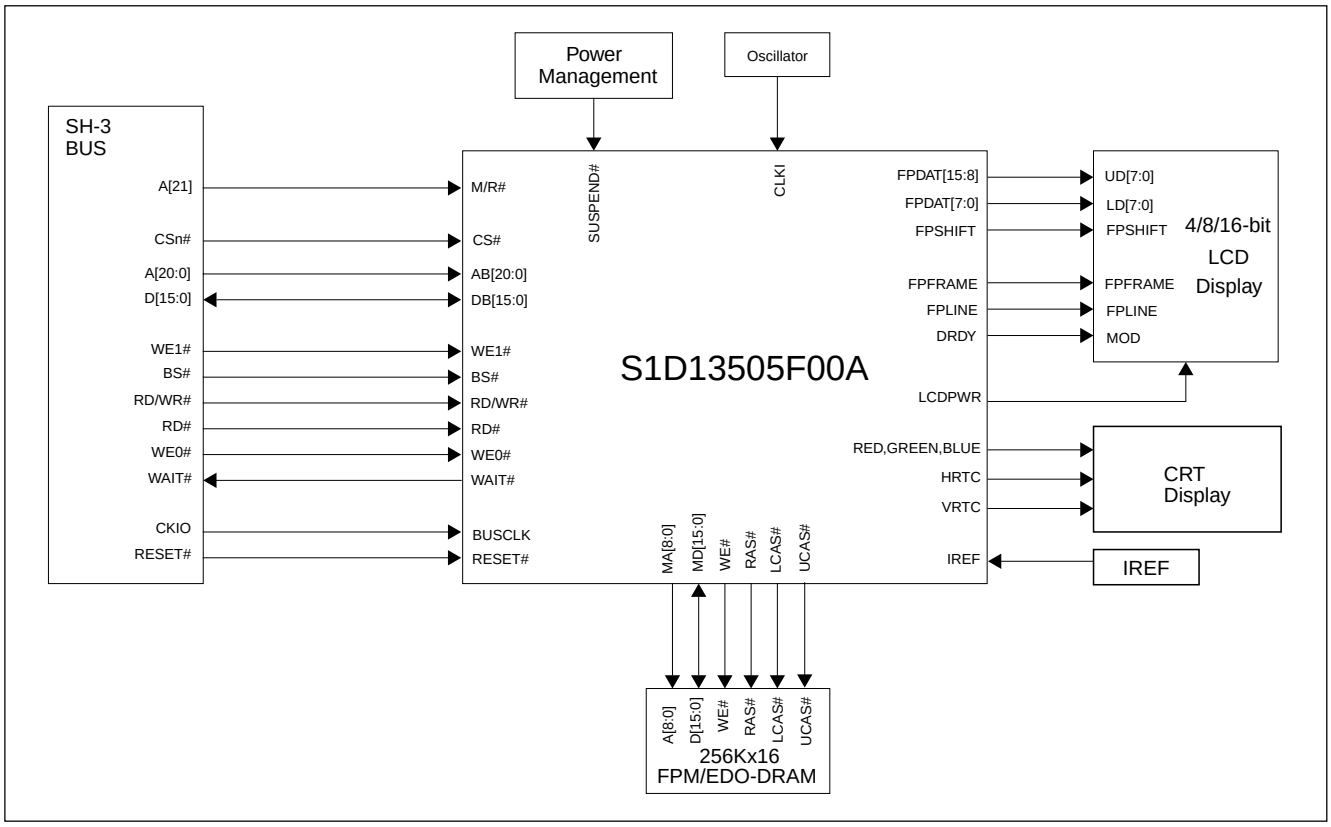
◆ Miscellaneous

- The memory data bus, MD[15:0], is used to configure the chip at power-on.
- Three General Purpose Input/Output pins, GPIO[3:1], are available if the upper Memory Address pins are not required for asymmetric DRAM support.
- Suspend power save mode can be initiated by either hardware or software.
- The SUSPEND# pin is used either as an input to initiate Suspend mode, or as a General Purpose Output that can be used to control the LCD backlight. Power-on polarity is selected by an MD configuration pin.
- Operating voltages from 2.7 volts to 5.5 volts are supported
- 128-pin QFP15 surface mount package

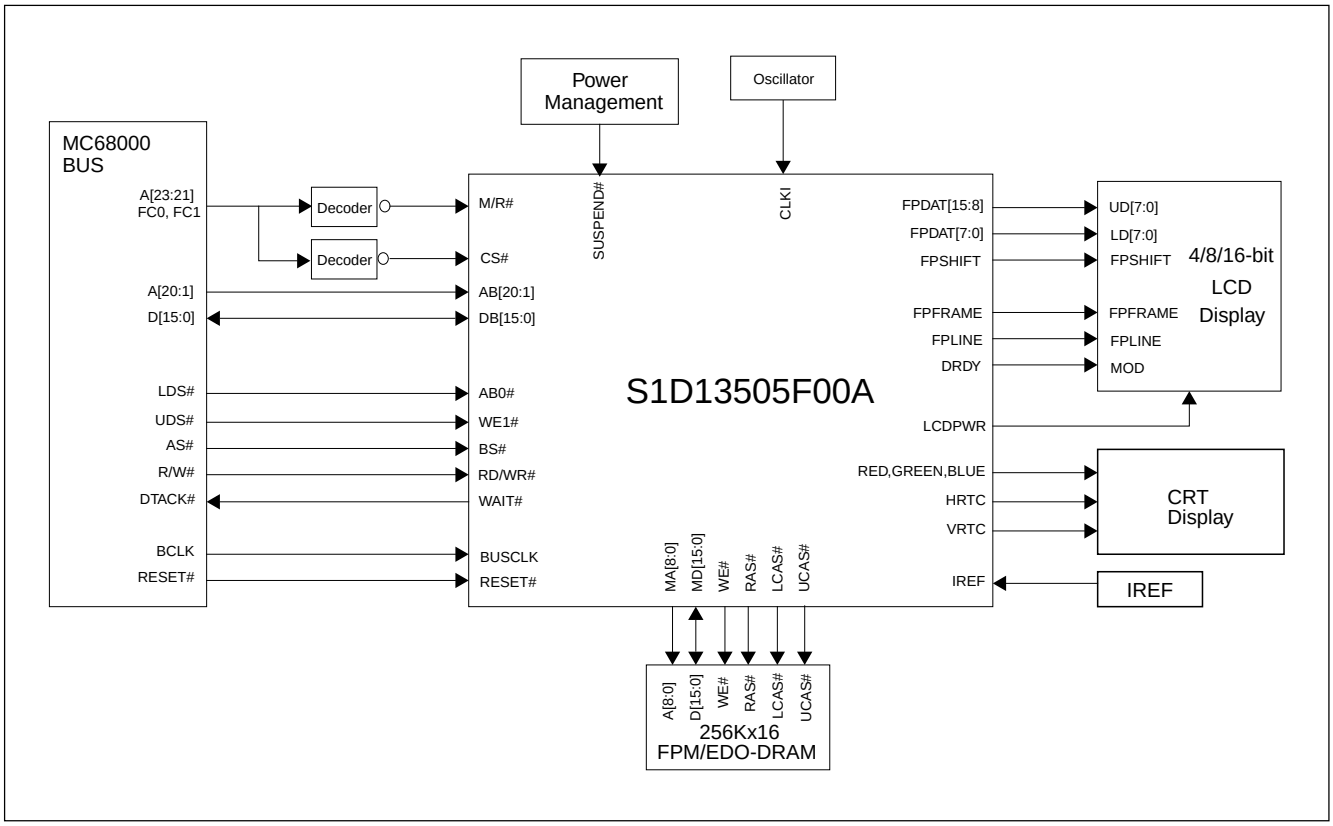
■ TYPICAL SYSTEM IMPLEMENTATION DIAGRAMS



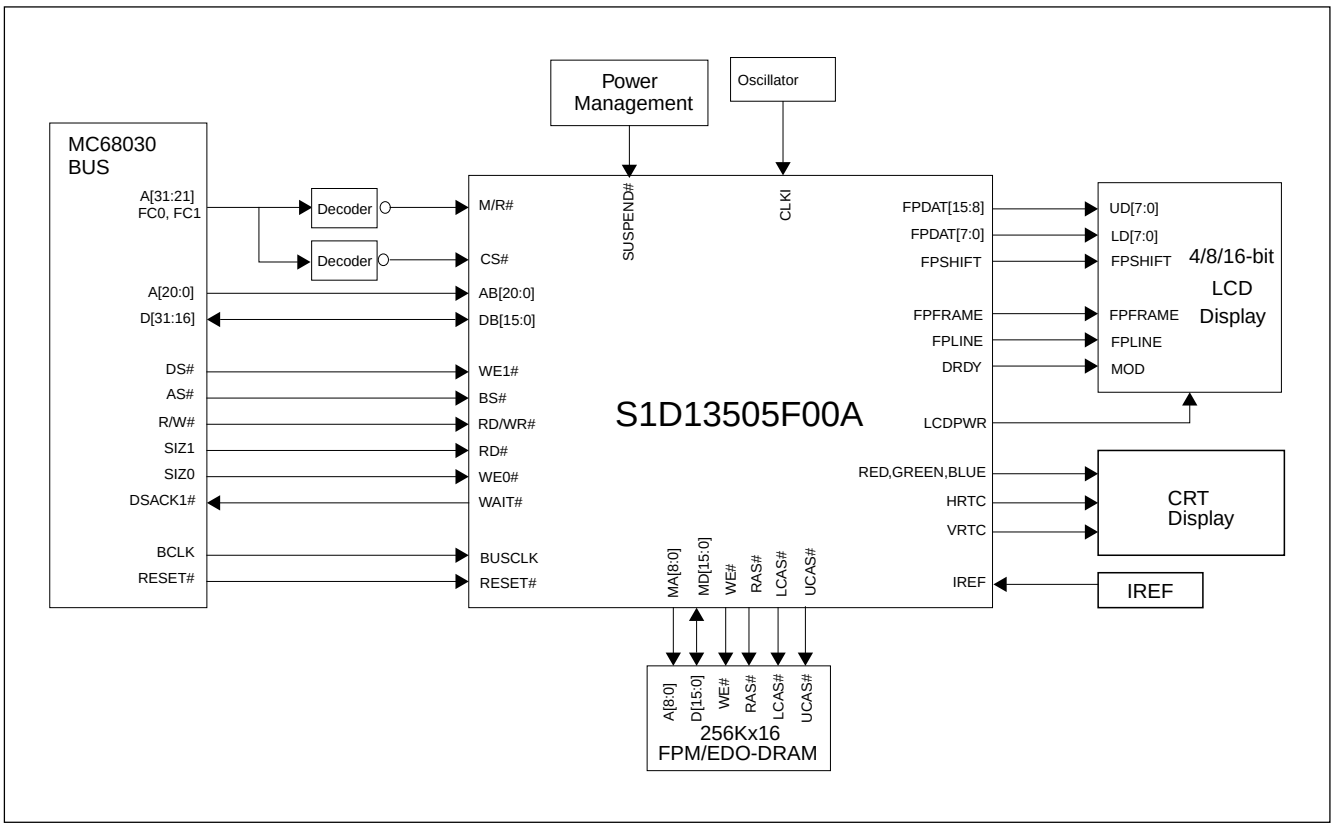
Typical System Diagram (SH-4 Bus, 256Kx16 FPM/EDO-DRAM)



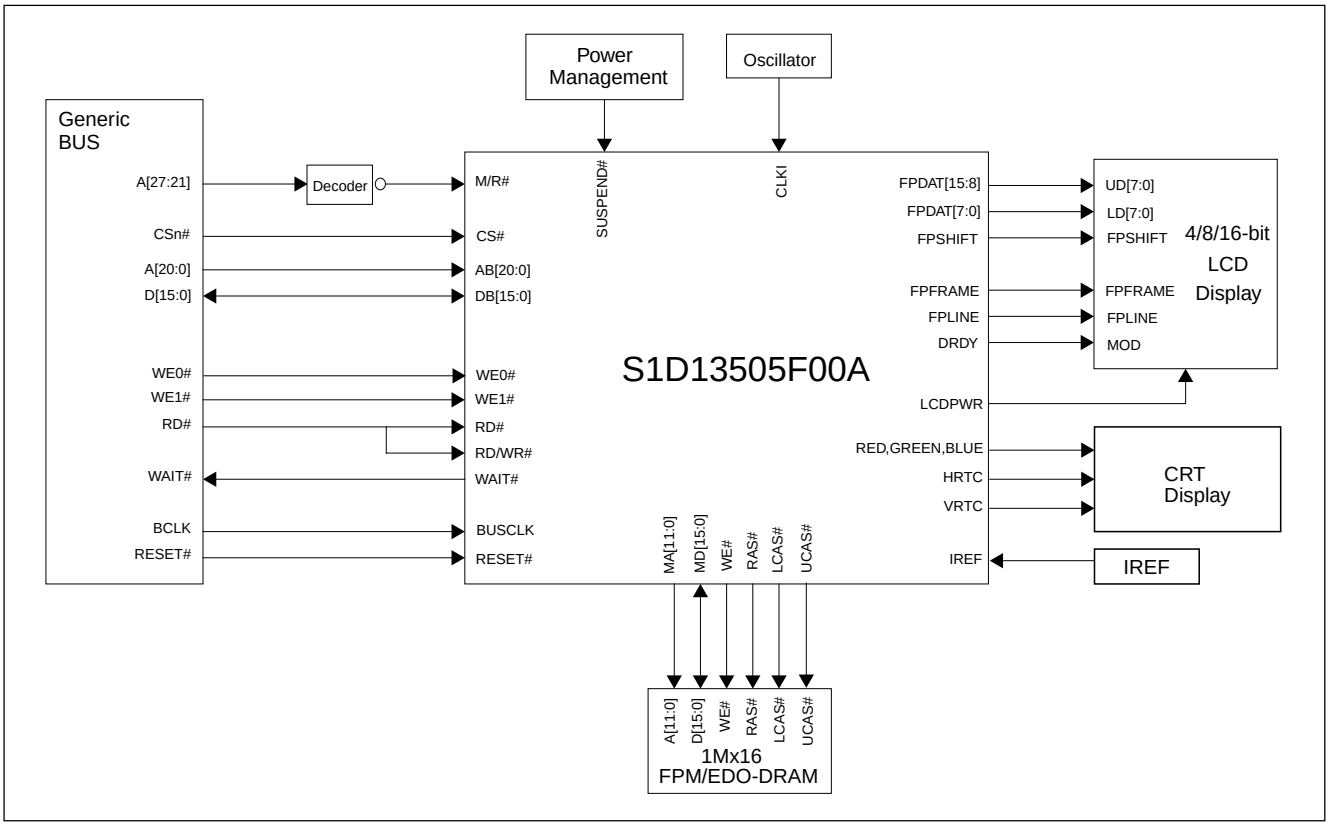
Typical System Diagram (SH-3 Bus, 256Kx16 FPM/EDO-DRAM)



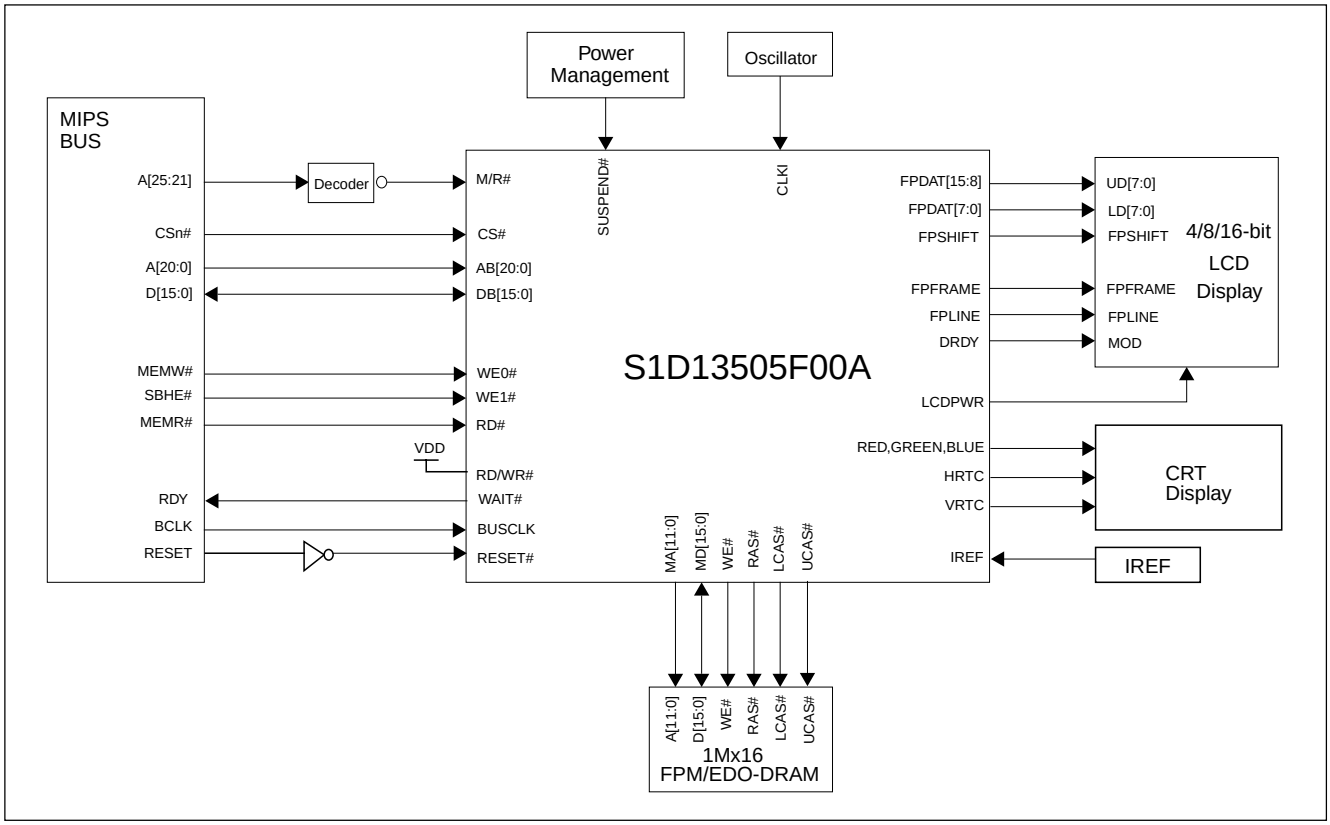
Typical System Diagram (MC68K Bus 1, 16-Bit 68000, 256Kx16 FPM/EDO-DRAM)



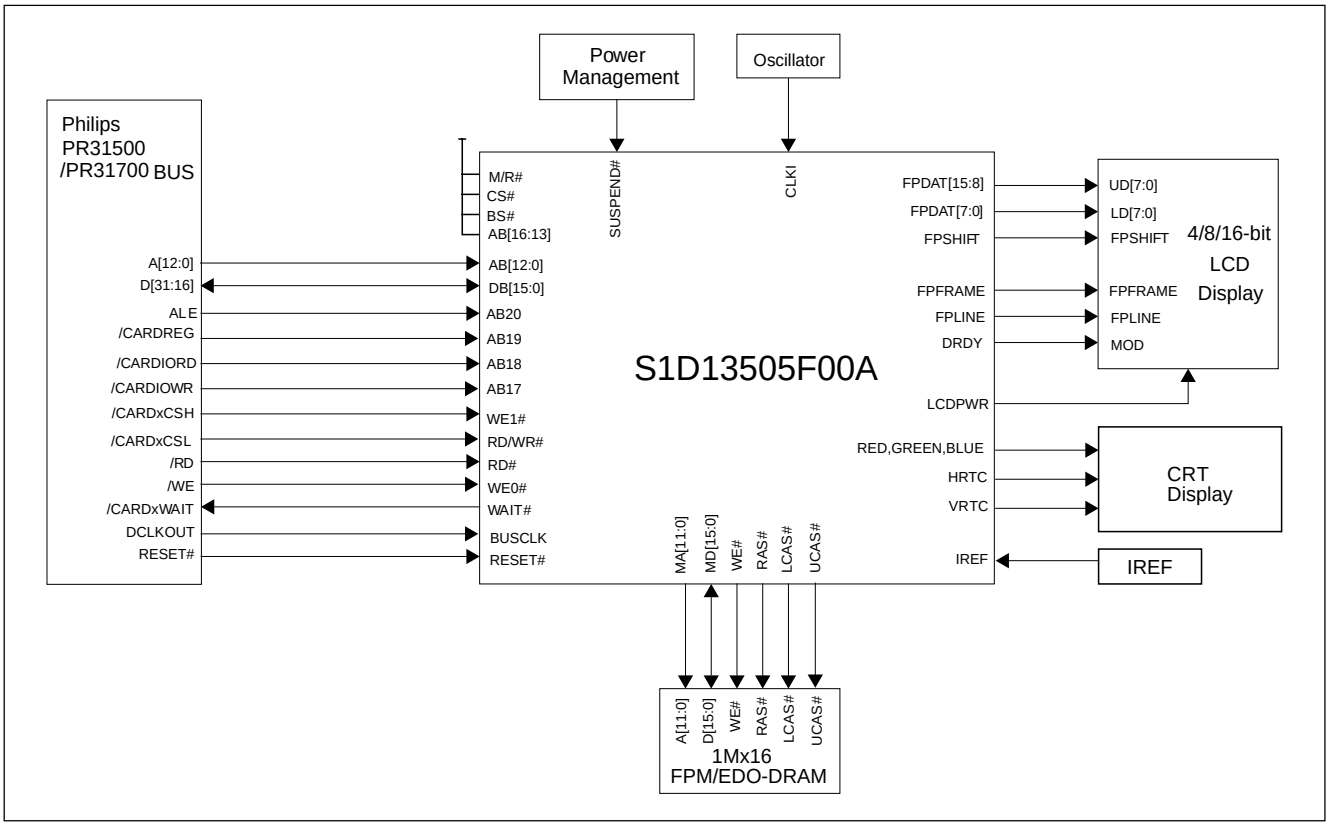
Typical System Diagram (MC68K Bus 2, 32-Bit 68030, 256Kx16 FPM/EDO-DRAM)



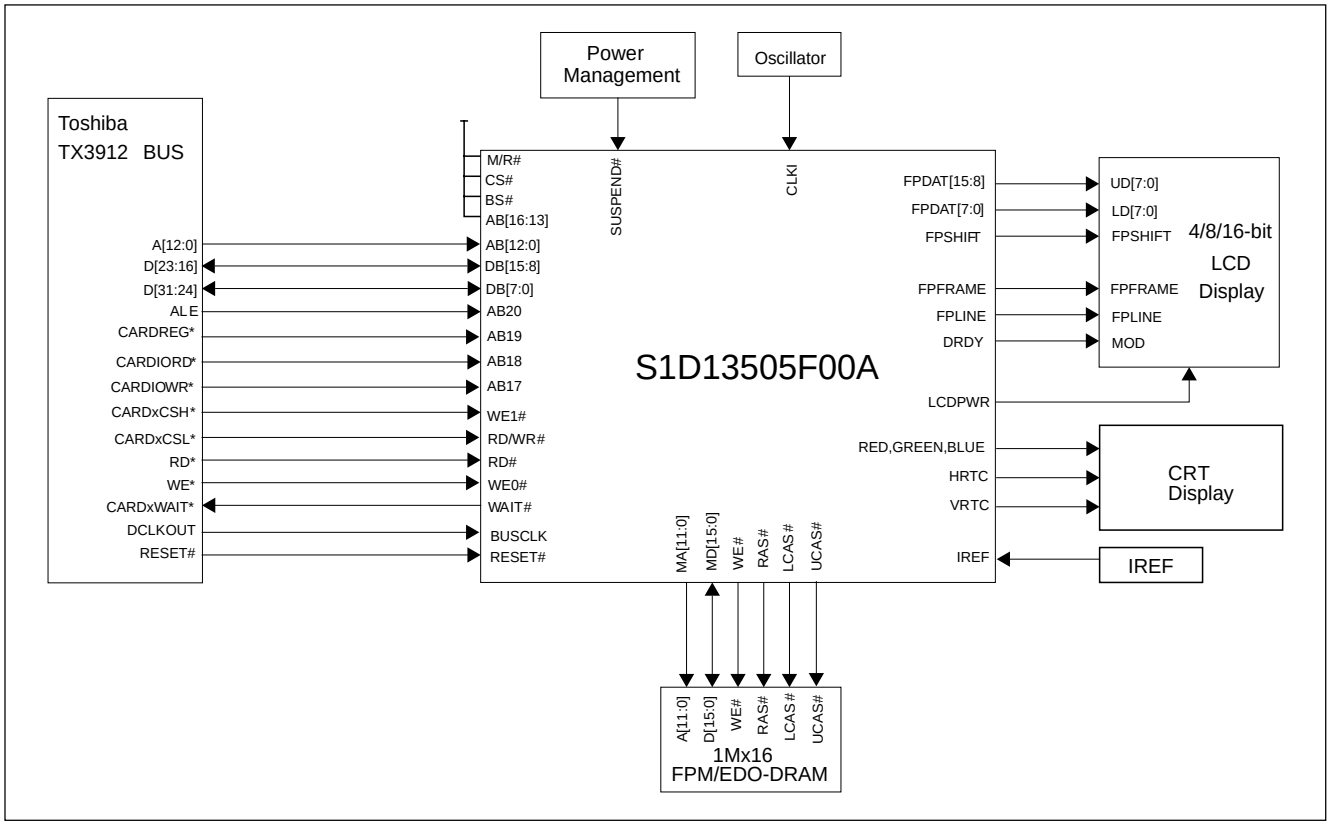
Typical System Diagram (Generic Bus, 1Mx16 FPM/EDO-DRAM)



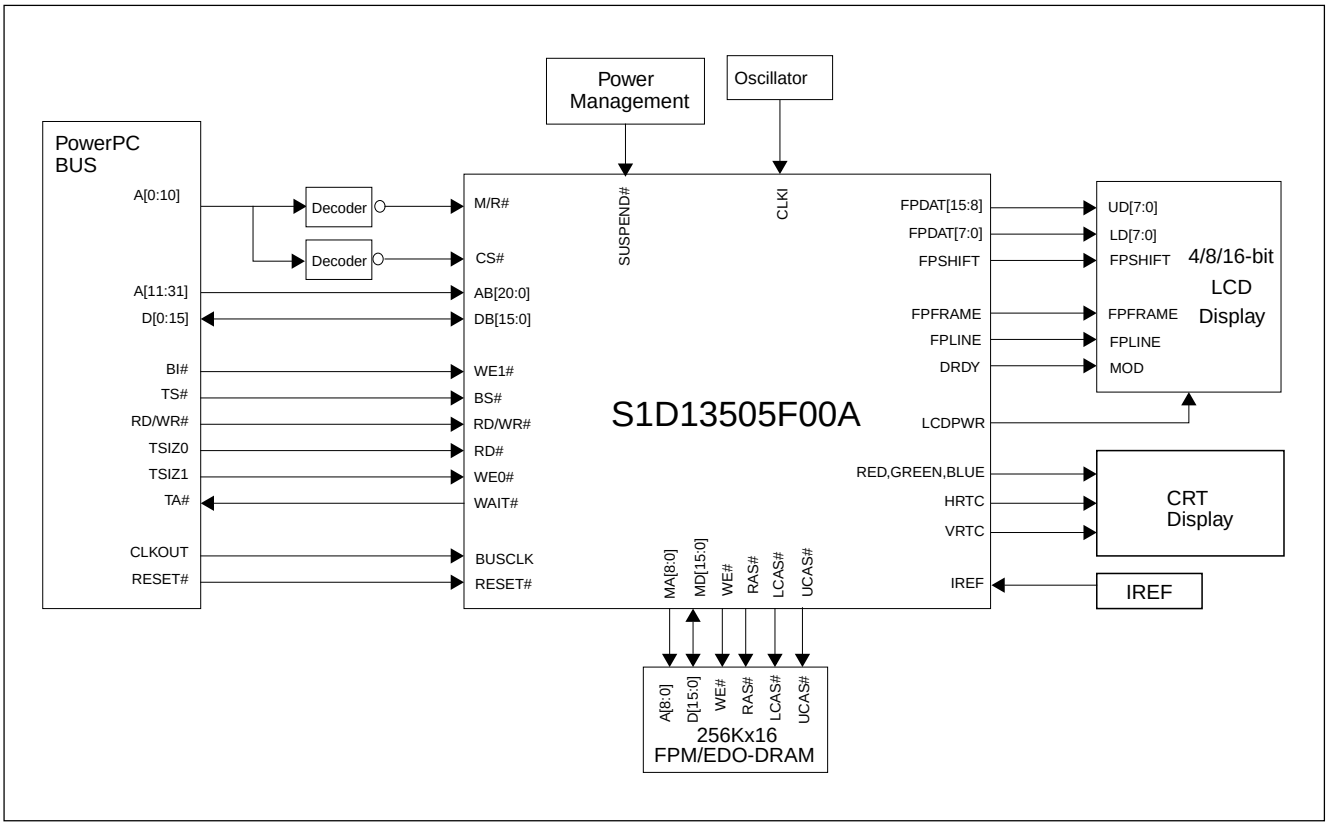
Typical System Diagram (NEC VR41xx (MIPS) Bus, 1Mx16 FPM/EDO-DRAM)



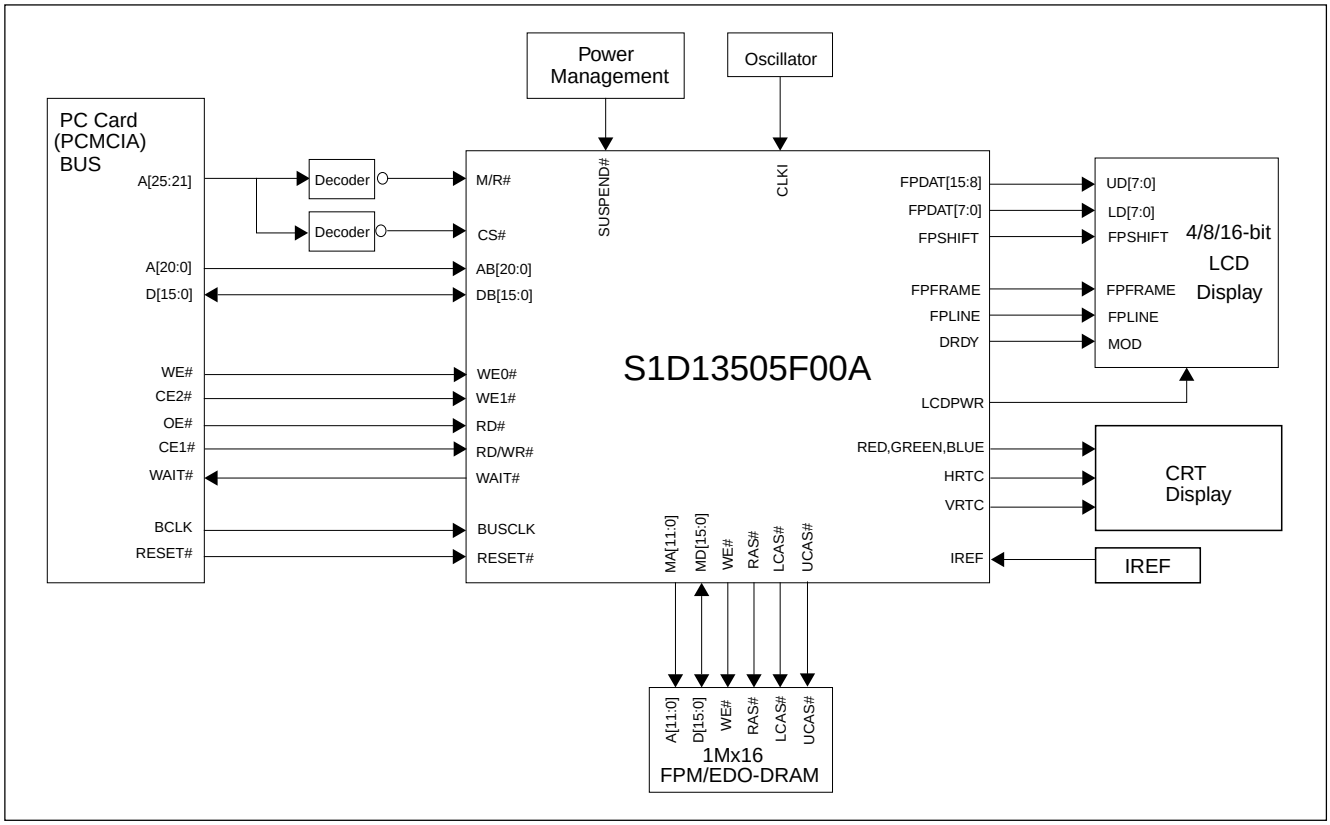
Typical System Diagram (Philips PR31500/PR31700 Bus, 1Mx16 FPM/EDO-DRAM)



Typical System Diagram (Toshiba TX3912 Bus, 1Mx16 FPM/EDO-DRAM)



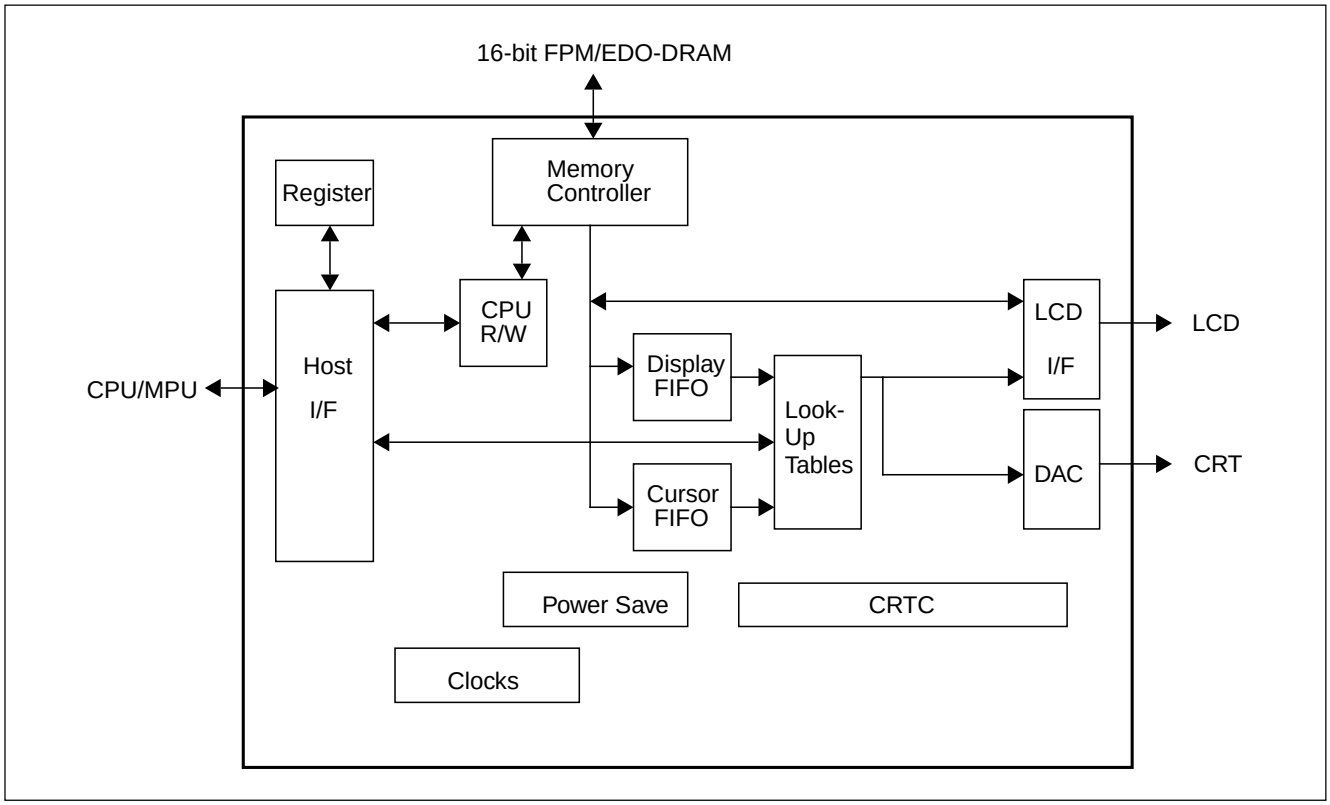
Typical System Diagram (Power PC Bus, 256Kx16 FPM/EDO-DRAM)



Typical System Diagram (PC Card (PCMCIA) Bus, 1Mx16 FPM/EDO-DRAM)

■ INTERNAL DESCRIPTION

◆ Block Diagram Showing Datapaths



System Block Diagram Showing Datapaths

◆ Block Descriptions

Register

The Register block contains all the register latches.

Host Interface

The Host Interface (I/F) block provides the means for the CPU/MPU to communicate with the display buffer and internal registers via one of the supported bus interfaces.

CPU R/W

The CPU R/W block synchronizes the CPU requests for display buffer access. If SwivelView™ is enabled, the data is rotated in this block.

Memory Controller

The Memory Controller block arbitrates between CPU accesses and display refresh accesses as well as generates the necessary signals to interface to one of the supported 16-bit memory devices (FPM-DRAM or EDO-DRAM).

Display FIFO

The Display FIFO block fetches display data from the Memory Controller for display refresh.

Cursor FIFO

The Cursor FIFO block fetches Cursor/ink data from the Memory Controller for display refresh.

Look-Up Tables

The Look-Up Tables block contains three 256x4 Look-Up Tables (LUT), one for each primary color. In monochrome mode, only the green LUT is selected and used. This block contains anti-sparkle circuitry. The cursor/ink and display data are merged in this block.

CRTC

The CRTC generates the sync timing for the LCD and CRT, defining the vertical and horizontal display periods.

LCD Interface

The LCD Interface block performs Frame Rate Modulation (FRM) for passive LCD panels and generates the correct data format and timing control signals for various LCD and TFT/D-TFD panels.

DAC

The DAC is the Digital to Analog converter for analog CRT support.

Power Save

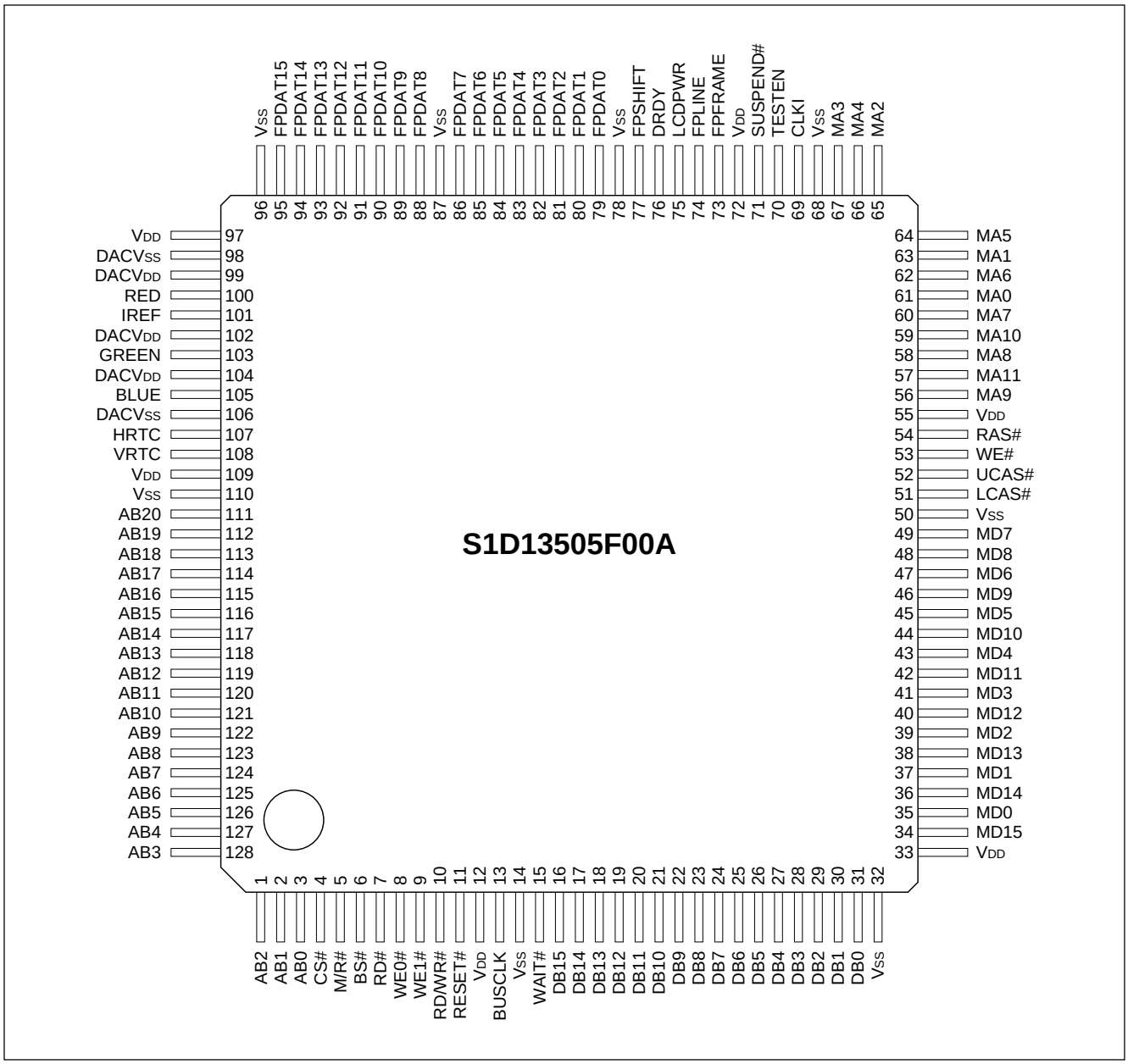
The Power Save block contains the power save mode circuitry.

Clocks

The Clocks module is the source of all clocks in the chip.

■ PIN OUT

◆ Pinout Diagram



Pinout Diagram

128-pin QFP15 surface mount package

◆ Pin Description

Key:

I	=	Input
O	=	Output
I/O	=	Bi-Directional (Input/Output)
A	=	Analog
P	=	Power pin
C	=	CMOS level input
CD	=	CMOS level input with pull down resistor (typical values of 100KΩ/180KΩ at 5V/3.3V respectively)
CS	=	CMOS level Schmitt input
COx	=	CMOS output driver, x denotes driver type (see tables “Electrical Characteristics for V_{DD} = 5.0V Typical,” “Electrical Characteristics for V_{DD} = 3.3V Typical,” “Electrical Characteristics for V_{DD} = 3.0V Typical” for details)
TSx	=	Tri-state CMOS output driver, x denotes driver type (see tables “Electrical Characteristics for V_{DD} = 5.0V Typical,” “Electrical Characteristics for V_{DD} = 3.3V Typical,” “Electrical Characteristics for V_{DD} = 3.0V Typical” for details)
TSxD	=	Tri-state CMOS output driver with pull down resistor (typical values of 100KW/180KW at 5V/ 3.3V respectively), x denotes driver type (see tables “Electrical Characteristics for V_{DD} = 5.0V Typical,” “Electrical Characteristics for V_{DD} = 3.3V Typical,” “Electrical Characteristics for V_{DD} = 3.0V Typical” for details)
CNx	=	CMOS low-noise output driver, x denotes driver type (see tables “Electrical Characteristics for V_{DD} = 5.0V Typical,” “Electrical Characteristics for V_{DD} = 3.3V Typical,” “Electrical Characteristics for V_{DD} = 3.0V Typical” for details)

● Host Interface

Host Interface Pin Descriptions

Pin Name	Type	Pin #	Driver	Reset# State	Description
AB0	I	3	CS	Hi-Z	• For SH-3/SH-4 Bus, this pin inputs system address bit 0 (A0). • For MC68K Bus 1, this pin inputs the lower data strobe (LDS#). • For MC68K Bus 2, this pin inputs system address bit 0 (A0). • For Generic Bus, this pin inputs system address bit 0 (A0). • For MIPS/ISA Bus, this pin inputs system address bit 0 (SA0). • For Philips PR31500/31700 Bus, this pin inputs system address bit 0 (A0). • For Toshiba TX3912 Bus, this pin inputs system address bit 0 (A0). • For PowerPC Bus, this pin inputs system address bit 31 (A31). • For PC Card (PCMCIA) Bus, this pin inputs system address bit 0 (A0). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
AB[12:1]	I	119–128, 1, 2	C	Hi-Z	• For PowerPC Bus, these pins input the system address bits 19 through 30 (A[19:30]). • For all other busses, these pins input the system address bits 12 through 1 (A[12:1]). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
AB[16:13]	I	115-118	C	Hi-Z	• For Philips PR31500/31700 Bus, these pins are connected to V_{DD}. • For Toshiba TX3912 Bus, these pins are connected to V_{DD}. • For PowerPC Bus, these pins input the system address bits 15 through 18 (A[15:18]). • For all other busses, these pins input the system address bits 16 through 13 (A[16:13]). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
AB17#	I	114	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the I/O write command (/CARDIOWR). • For Toshiba TX3912 Bus, this pin inputs the I/O write command (CAR-DIOWR*). • For PowerPC Bus, this pin inputs the system address bit 14 (A14). • For all other busses, this pin inputs the system address bit 17 (A17). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
AB18	I	113	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the I/O read command (/CARDIORD). • For Toshiba TX3912 Bus, this pin inputs the I/O read command (CAR-DIORD*). • For PowerPC Bus, this pin inputs the system address bit 13 (A13). • For all other busses, this pin inputs the system address bit 18 (A18). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
AB19	I	112	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the card control register access (/CARDREG). • For Toshiba TX3912 Bus, this pin inputs the card control register (CAR-DREG*). • For PowerPC Bus, this pin inputs the system address bit 12 (A12). • For all other busses, this pin inputs the system address bit 19 (A19). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.

Host Interface Pin Descriptions (Continue)

Pin Name	Type	Pin #	Driver	Reset# State	Description
AB20	I	111	C	Hi-Z	• For the MIPS/ISA Bus, this pin inputs system address bit 20. Note that for the ISA Bus, the unlatched LA20 must first be latched before input to AB20. • For Philips PR31500/31700 Bus, this pin inputs the address latch enable (ALE). • For Toshiba TX3912 Bus, this pin inputs the address latch enable (ALE). • For PowerPC Bus, this pin inputs the system address bit 11 (A11). • For all other busses, this pin inputs the system address bit 20 (A20). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
DB[15:0]	IO	16–31	C/TS2	Hi-Z	These pins are the system data bus. For 8-bit bus modes, unused data pins should be tied to V_{DD}. • For SH-3/SH-4 Bus, these pins are connected to D[15:0]. • For MC68K Bus 1, these pins are connected to D[15:0]. • For MC68K Bus 2, these pins are connected to D[31:16] for 32-bit devices (e.g. MC68030) or D[15:0] for 16-bit devices (e.g. MC68340). • For Generic Bus, these pins are connected to D[15:0]. • For MIPS/ISA Bus, these pins are connected to SD[15:0]. • For Philips PR31500/31700 Bus, these pins are connected to D[31:16]. • For Toshiba TX3912 Bus, pins [15:8] are connected to D[23:16] and pins [7:0] are connected to D[31:24]. • For PowerPC Bus, these pins are connected to D[0:15]. • For PC Card (PCMCIA) Bus, these pins are connected to D[15:0]. See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
WE1#	IO	9	CS/TS2	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the write enable signal for the upper data byte (WE1#). • For MC68K Bus 1, this pin inputs the upper data strobe (UDS#). • For MC68K Bus 2, this pin inputs the data strobe (DS#). • For Generic Bus, this pin inputs the write enable signal for the upper data byte (WE1#). • For MIPS/ISA Bus, this pin inputs the system byte high enable signal (SBHE#). • For Philips PR31500/31700 Bus, this pin inputs the odd byte access enable signal (/CARDxCSH). • For Toshiba TX3912 Bus, this pin inputs the odd byte access enable signal (CARDxCSH*). • For PowerPC Bus, this pin outputs the burst inhibit signal (BI#). • For PC Card (PCMCIA) Bus, this pin inputs the card enable 2 signal (-CE2). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
M/R#	I	5	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For Toshiba TX3912 Bus, this pin is connected to V_{DD}. • For all busses, this input pin is used to select between the display buffer and register address spaces of the S1D13505. M/R# is set high to access the display buffer and low to access the registers. See Register Mapping. See Table “CPU Interface Pin Mapping” on page 18.
CS#	I	4	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For Toshiba TX3912 Bus, this pin is connected to V_{DD}. • For all busses, this is the Chip Select input. See Table “CPU Interface Pin Mapping” on page 18. See the respective AC Timing diagram for detailed functionality

Host Interface Pin Descriptions (Continue)

Pin Name	Type	Pin #	Driver	Reset# State	Description
BUSCLK	I	13	C	Hi-Z	This pin inputs the system bus clock. It is possible to apply a 2x clock and divide it by 2 internally - see MD12 in Summary of Configuration Options. • For SH-3/SH-4 Bus, this pin is connected to CKIO. • For MC68K Bus 1, this pin is connected to CLK. • For MC68K Bus 2, this pin is connected to CLK. • For Generic Bus, this pin is connected to BCLK. • For MIPS/ISA Bus, this pin is connected to CLK. • For Philips PR31500/31700 Bus, this pin is connected to DCLKOUT. • For Toshiba TX3912 Bus, this pin is connected to DCLKOUT. • For PowerPC Bus, this pin is connected to CLKOUT. • For PC Card (PCMCIA) Bus, this pin is connected to the input clock (CLKI, pin 69). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
BS#	I	6	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the bus start signal (BS#). • For MC68K Bus 1, this pin inputs the address strobe (AS#). • For MC68K Bus 2, this pin inputs the address strobe (AS#). • For Generic Bus, this pin is connected to V_{DD}. • For MIPS/ISA Bus, this pin is connected to V_{DD}. • For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For Toshiba TX3912 Bus, this pin is connected to V_{DD}. • For PowerPC Bus, this pin inputs the Transfer Start signal (TS#). • For PC Card (PCMCIA) Bus, this pin is connected to V_{DD}. See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
RD/WR#	I	10	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the read write signal (RD/WR#). The S1D13505 needs this signal for early decode of the bus cycle. • For MC68K Bus 1, this pin inputs the read write signal (R/W#). • For MC68K Bus 2, this pin inputs the read write signal (R/W#). • For Generic Bus, this pin inputs the read command for the upper data byte (RD1#). • For MIPS/ISA Bus, this pin is connected to V_{DD}. • For Philips PR31500/31700 Bus, this pin inputs the even byte access enable signal (/CARDxCSL). • For Toshiba TX3912 Bus, this pin inputs the even byte access enable signal (CARDxCSL*). • For PowerPC Bus, this pin inputs the read write signal (RD/WR#). • For PC Card (PCMCIA) Bus, this pin inputs the card enable 1 signal (-CE1). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
RD#	I	7	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the read signal (RD#). • For MC68K Bus 1, this pin is connected to V_{DD}. • For MC68K Bus 2, this pin inputs the bus size bit 1 (SIZ1). • For Generic Bus, this pin inputs the read command for the lower data byte (RD0#). • For MIPS/ISA Bus, this pin inputs the memory read signal (MEMR#). • For Philips PR31500/31700 Bus, this pin inputs the memory read command (/RD). • For Toshiba TX3912 Bus, this pin inputs the memory read command (RD*). • For PowerPC Bus, this pin inputs the transfer size 0 signal (TSIZ0). • For PC Card (PCMCIA) Bus, this pin inputs the output enable signal (-OE). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.

Host Interface Pin Descriptions (Continue)

Pin Name	Type	Pin #	Driver	Reset# State	Description
WE0#	I	8	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the write enable signal for the lower data byte (WE0#). • For MC68K Bus 1, this pin must be connected to V_{DD} • For MC68K Bus 2, this pin inputs the bus size bit 0 (SIZ0). • For Generic Bus, this pin inputs the write enable signal for the lower data byte (WE0#). • For MIPS/ISA Bus, this pin inputs the memory write signal (MEMW#). • For Philips PR31500/31700 Bus, this pin inputs the memory write command (/WE). • For Toshiba TX3912 Bus, this pin inputs the memory write command (WE*). • For PowerPC Bus, this pin inputs the Transfer Size 1 signal (TSIZ1). • For PC Card (PCMCIA) Bus, this pin inputs the write enable signal (-WE). See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
WAIT#	O	15	TS2	Hi-Z	The active polarity of the WAIT# output is configurable; the state of MD5 on the rising edge of RESET# defines the active polarity of WAIT# - see “Summary of Configuration Options.” • For SH-3 Bus, this pin outputs the wait request signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. • For SH-4 Bus, this pin outputs the ready signal (RDY#); MD5 must be pulled high during reset by an external pull-up resistor. • For MC68K Bus 1, this pin outputs the data transfer acknowledge signal (DTACK#); MD5 must be pulled high during reset by an external pull-up resistor. • For MC68K Bus 2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#); MD5 must be pulled high during reset by an external pull-up resistor. • For Generic Bus, this pin outputs the wait signal (WAIT#); MD5 must be pulled high during reset by an external pull-up resistor. • For MIPS/ISA Bus, this pin outputs the IO channel ready signal (IOCHRDY); MD5 must be pulled low during reset by the internal pull-down resistor. • For Philips PR31500/31700 Bus, this pin outputs the wait state signal (/CARDxWAIT); MD5 must be pulled low during reset by the internal pull-down resistor. • For Toshiba TX3912 Bus, this pin outputs the wait state signal (CARDx-WAIT*); MD5 must be pulled low during reset by the internal pull-down resistor. • For PowerPC Bus, this pin outputs the transfer acknowledge signal (TA#); MD5 must be pulled high during reset by an external pull-up resistor. • For PC Card (PCMCIA) Bus, this pin outputs the wait signal (-WAIT); MD5 must be pulled low during reset by the internal pull-down resistor. See Table “CPU Interface Pin Mapping” for summary. See the respective AC Timing diagram for detailed functionality.
RESET#	I	11	CS	–	Active low input that clears all internal registers and forces all outputs to their inactive states. Note that active high RESET signals must be inverted before input to this pin.

● Memory Interface

Memory Interface Pin Descriptions

Pin Name	Type	Pin #	Driver	Reset# State	Description
LCAS#	O	51	CO1	1	• For dual-CAS# DRAM, this is the column address strobe for the lower byte (LCAS#). • For single-CAS# DRAM, this is the column address strobe (CAS#). See Table “Memory Interface Pin Mapping” for summary. See Memory Interface Timing for detailed functionality.
UCAS#	O	52	CO1	1	This is a multi-purpose pin: • For dual-CAS# DRAM, this is the column address strobe for the upper byte (UCAS#). • For single-CAS# DRAM, this is the write enable signal for the upper byte (UWE#). See Table “Memory Interface Pin Mapping” for summary. See Memory Interface Timing for detailed functionality.
WE#	O	53	CO1	1	• For dual-CAS# DRAM, this is the write enable signal (WE#). • For single-CAS# DRAM, this is the write enable signal for the lower byte (LWE#). See Table “Memory Interface Pin Mapping” for summary. See Memory Interface Timing for detailed functionality
RAS#	O	54	CO1	1	Row address strobe - see Memory Interface Timing for detailed functionality.
MD[15:0]	IO	34, 36, 38, 40, 42, 44, 46, 48, 49, 47, 45, 43, 41, 39, 37, 35	C/TS1D	Hi-Z	• Bi-Directional memory data bus. • During reset, these pins are inputs and their states at the rising edge of RESET# are used to configure the chip - see “Summary of Configuration Options.” Internal pull-down resistors (typical values of 100KΩ/180KΩ at 5V/3.3V respectively) pull the reset states to 0. External pull-up resistors can be used to pull the reset states to 1. See Memory Interface Timing for detailed functionality.
MA[8:0]	O	58, 60, 62, 64, 66, 67, 65, 63, 61	CO1	Output	Multiplexed memory address - see Memory Interface Timing for functionality.
MA9	IO	56	C/TS1	Output	This is a multi-purpose pin: • For 2M byte DRAM, this is memory address bit 9 (MA9). • For asymmetrical 512K byte DRAM, this is memory address bit 9 (MA9). • For symmetrical 512K byte DRAM, this pin can be used as general purpose IO pin 3 (GPIO3). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See Table “Memory Interface Pin Mapping” for summary. See Memory Interface Timing for detailed functionality.
MA10	IO	59	C/TS1	Output	This is a multi-purpose pin: • For asymmetrical 2M byte DRAM this is memory address bit 10 (MA10). • For symmetrical 2M byte DRAM and all 512K byte DRAM this pin can be used as general purpose IO pin 1 (GPIO1). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See Table “Memory Interface Pin Mapping” for summary. See Memory Interface Timing for detailed functionality.
MA11	IO	57	C/TS1	Output	This is a multi-purpose pin: • For asymmetrical 2M byte DRAM this is memory address bit 11 (MA11). • For symmetrical 2M byte DRAM and all 512K byte DRAM this pin can be used as general purpose IO pin 2 (GPIO2). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See Table “Memory Interface Pin Mapping” for summary. See Memory Interface Timing for detailed functionality.

● LCD Interface

LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
FPDAT[15:0]	O	95–88, 86–79	CN3	Output	Panel data bus. Not all pins are used for some panels - see Table “LCD Interface Pin Mapping” for details. Unused pins are driven low.
FPFRAME	O	73	CN3	Output	Frame pulse
FPLINE	O	74	CN3	Output	Line pulse
FPSHIFT	O	77	CN3	Output	Shift clock
LCDPWR	O	75	CO1	Output if MD[10]=0 1 if MD[10]=1	LCD power control output. The active polarity of this output is selected by the state of MD10 at the rising edge of RESET# - see “Summary of Configuration Options.” This output is controlled by the power save mode circuitry.
DRDY	O	76	CN3	Output	This is a multi-purpose pin: • For TFT/D-TFD panels this is the display enable output (DRDY). • For passive LCD with Format 1 interface this is the 2nd Shift Clock (FPSHIFT2). • For all other LCD panels this is the LCD backplane bias signal (MOD). See Table “LCD Interface Pin Mapping” and REG[02h] for details.

● CRT Interface

Clock Input Pin Description

Pin Name	Type	Pin #	Cell	RESET# State	Description
HRTC	IO	107	CN3	Output	Horizontal retrace signal for CRT
VRTC	IO	108	CN3	Output	Vertical retrace signal for CRT
RED	O	100	A		Analog output for CRT color Red
GREEN	O	103	A		Analog output for CRT color Green
BLUE	O	105	A		Analog output for CRT color Blue
IREF	I	101	A		Current reference for DAC - see Analog Pins. This pin must be left unconnected if the DAC is not needed.

● Miscellaneous

Miscellaneous Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
SUSPEND#	IO	71	CS/TS1	Hi-Z if MD[9]=0 High if MD[10:9]=01 Low if MD[10:9]=11	This pin can be used as a power-down input (SUSPEND#) or as an output possibly used for controlling the LCD backlight power: • When MD9 = 0 at rising edge of RESET#, this pin is an activelow Schmitt input used to put the S1D13505 into Hardware suspend mode. • When MD[10:9] = 01 at rising edge of RESET#, this pin is an output (GPO) with a reset state of 1. Its state is controlled by REG[21h] bit 7. • When MD[10:9] = 11 at rising edge of RESET#, this pin is an output (GPO) with a reset state of 0. Its state is controlled by REG[21h] bit 7.
CLKI	I	69	C		Input clock for the internal pixel clock (PCLK) and memory clock (MCLK). PCLK and MCLK are derived from CLKI - see REG[19h] for details.
TESTEN	I	70	CD	Hi-Z	Test Enable. This pin should be connected to V_{SS} for normal operation.
V_{DD}	P	12, 33, 55, 72, 97, 109	P		V_{DD}
DACV_{DD}	P	99, 102, 104	P		DAC V_{DD}
V_{SS}	P	14, 32, 50, 68, 78, 87, 96, 110	P		V_{SS}
DACV_{SS}	P	98, 106	P		DAC V_{SS}

◆ Summary of Configuration Options

Summary of Power On / Reset Options

Pin Name	Value on this pin at rising edge of RESET# is used to configure: (1/0)	
	1	0
MD0	8-bit host bus interface	16-bit host bus interface
MD[3:1]	Select host bus interface:MD[11] = 0: 000 = SH-3/SH-4 bus interface 001 = MC68K Bus1 010 = MC68K Bus2 011 = Generic 100 = Reserved 101 = MIPS/ISA 110 = PowerPC 111 = PC Card (when MD11 = 1Philips PR31500/PR31700 or ToshibaTX3912 Bus)	
MD4	Little Endian	Big Endian
MD5	WAIT# is active high (1 = insert wait state)	WAIT# is active low (0 = insert wait state)
MD[7:6]	Memory Address/GPIO configuration: 00 = symmetrical 256K x16 DRAM. MA[8:0] = DRAM address. MA[11:9] = GPIO2,1,3 pins. 01 = symmetrical 1M x16 DRAM. MA[9:0] = DRAM address. MA[10:11] = GPIO2,1 pins. 10 = asymmetrical 256K x16 DRAM. MA[9:0] = DRAM address. MA[10:11] = GPIO2,1 pins. 11 = asymmetrical 1M x16 DRAM. MA[11:0] = DRAM address.	
MD8	Not used	
MD9	SUSPEND# pin configured as GPO output	SUSPEND# pin configured as SUSPEND# input
MD10	Active low LCDPWR and GPO polarities	Active high LCDPWR and GPO polarities
MD11	Alternate Host Bus Interface Selected	Primary Host Bus Interface Selected
MD12	BUSCLK input divided by 2	BUSCLK input not divided
MD[15:13]	Not used	

◆ Multiple Function Pin Mapping

CPU Interface Pin Mapping

S1D13505 Pin Name	SH-3	SH-4	MC68K Bus 1	MC68K Bus 2	Generic	MIPS/ISA	Philips PR31500 /PR31700	Toshiba TX3912	PowerPC	PC Card (PCMCIA)
AB20	A20	A20	A20	A20	A20	LatchA20	ALE	ALE	A11	A20
AB19	A19	A19	A19	A19	A19	SA19	/CAR-DREG	CAR-DREG*	A12	A19
AB18	A18	A18	A18	A18	A18	SA18	/CAR-DIORD	CAR-DIORD*	A13	A18
AB17	A17	A17	A17	A17	A17	SA17	/CAR-DIOWR	CAR-DIOWR*	A14	A17
AB[16:13]	A[16:13]	A[16:13]	A[16:13]	A[16:13]	A[16:13]	SA[16:13]	VDD	VDD	A[15:18]	A[16:13]
AB[12:1]	A[12:1]	A[12:1]	A[12:1]	A[12:1]	A[12:1]	SA[12:1]	A[12:1]	A[12:1]	A[19:30]	A[12:1]
AB0	A0	A0	LDS#	A0	A0	SA0	A0	A0	A31	A0
DB[15:8]	D[15:8]	D[15:8]	D[15:8]	D[31:24]	D[15:8]	SD[15:8]	D[31:24]	D[31:24]	D[0:7]	D[15:8]
DB[7:0]	D[7:0]	D[7:0]	D[7:0]	D[23:16]	D[7:0]	SD[7:0]	D[23:16]	D[23:16]	D[8:15]	D[7:0]
WE1#	WE1#	WE1#	UDS#	DS#	WE1#	SBHE#	/CARDxCSH	CARDxCSH*	BI#	-CE2
M/R#	External Decode						VDD		External Decode	
CS#	External Decode						VDD		External Decode	
BUSCLK	CKIO	CKIO	CLK	CLK	BCLK	CLK	DCLK-OUT	DCLK-OUT	CLKOUT	CLKI
BS#	BS#	BS#	AS#	AS#	VDD	VDD	VDD	VDD	TS#	VDD
RD/WR#	RD/WR#	RD/WR#	R/W#	R/W#	RD1#	VDD	/CARDxCSL	CARDxCSL*	RD/WR#	-CE1
RD#	RD#	RD#	VDD	SIZ1	RD0#	MEMR#	/RD	RD*	TSIZ0	-OE
WE0#	WE0#	WE0#	VDD	SIZ0	WE0#	MEMW#	/WE	WE*	TSIZ1	-WE
WAIT#	WAIT#	RDY	DTACK#	DSACK1#	WAIT#	IOCHRDY	/CARD x WAIT	CARD x WAIT*	TA#	-WAIT
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	inverted RESET	RESET#	PON*	RESET#	inverted RESET

Memory Interface Pin Mapping

S1D13505 Pin Name	FPM/EDO-DRA M							
	Sym 256Kx16		Asym 256Kx16		Sym 1Mx16		Asym 1Mx16	
	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#
MD[15:0]	D[15:0]							
MA[8:0]	A[8:0]							
MA9	GPIO3		A9				A9	
MA10	GPIO1						A10	
MA11	GPIO2						A11	
UCAS#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#
LCAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#
WE#	WE#	LWE#	WE#	LWE#	WE#	LWE#	WE#	LWE#
RAS#	RAS#							

Notes: • All GPIO pins default to input on reset and unless programmed otherwise, should be connected to either V_{SS} or IO V_{DD} if not used.

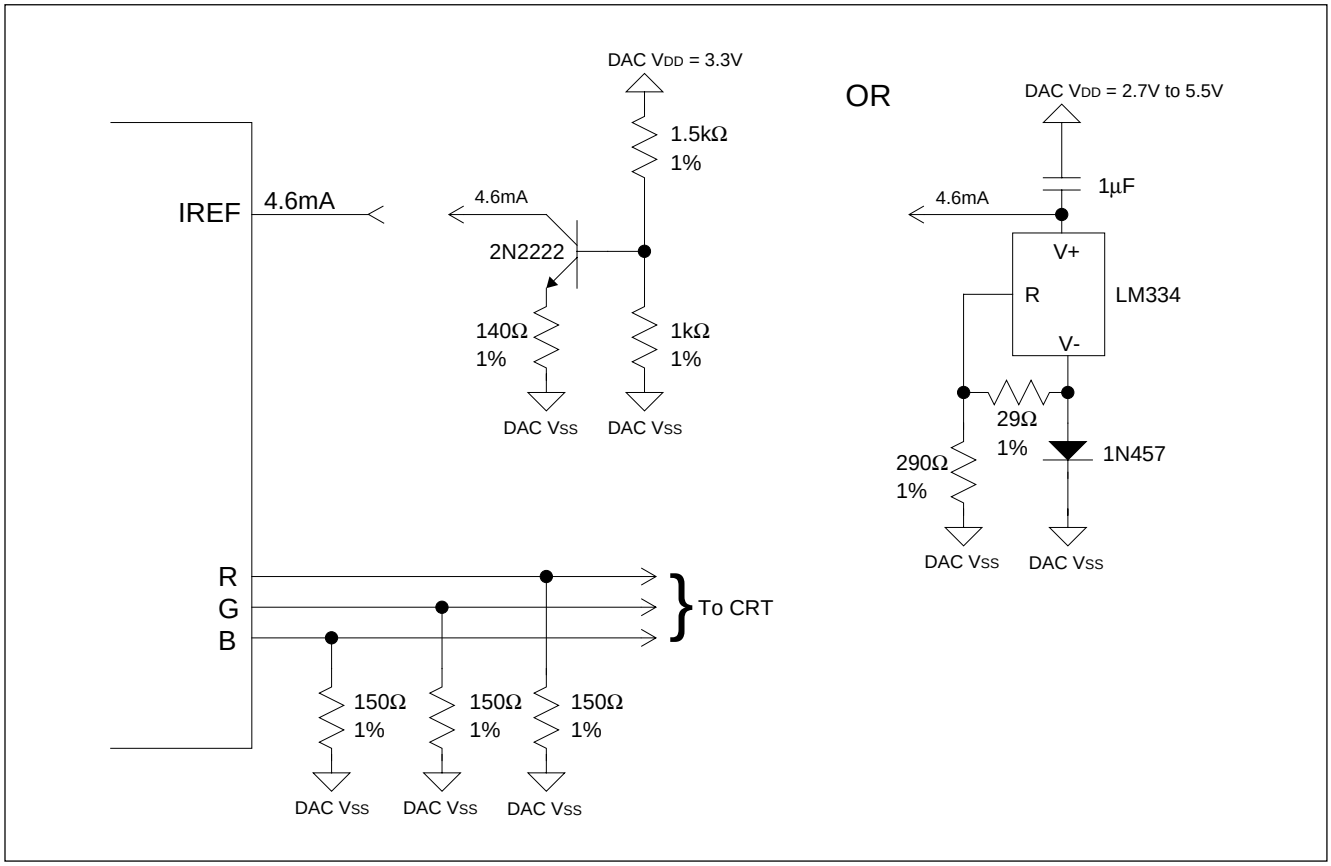
• The bus signal A0 is not used by the S1D13505 internally.

LCD Interface Pin Mapping

S1D13505 Pin Name	Monochrome Passive Panel			Color Passive Panel						Color TFT/D-TFD Panel		
	Single		Dual	Single	Single Format 1	Single Format 2	Single	Dual				
	4-bit	8-bit	8-bit	4-bit	8-bit	8-bit	16-bit	8-bit	16-bit	9-bit	12-bit	18-bit
FPFRAME	FPFRAME											
FPLINE	FPLINE											
FPSHIFT	FPSHIFT											
DRDY	MOD				FPSHIFT 2	MOD				DRDY		
FPDAT0	driven 0	D0	LD0	driven 0	D0	D0	D0	LD0	LD0	R2	R3	R5
FPDAT1	driven 0	D1	LD1	driven 0	D1	D1	D1	LD1	LD1	R1	R2	R4
FPDAT2	driven 0	D2	LD2	driven 0	D2	D2	D2	LD2	LD2	R0	R1	R3
FPDAT3	driven 0	D3	LD3	driven 0	D3	D3	D3	LD3	LD3	G2	G3	G5
FPDAT4	D0	D4	UD0	D0	D4	D4	D4	UD0	UD0	G1	G2	G4
FPDAT5	D1	D5	UD1	D1	D5	D5	D5	UD1	UD1	G0	G1	G3
FPDAT6	D2	D6	UD2	D2	D6	D6	D6	UD2	UD2	B2	B3	B5
FPDAT7	D3	D7	UD3	D3	D7	D7	D7	UD3	UD3	B1	B2	B4
FPDAT8	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D8	driven 0	LD4	B0	B1	B3
FPDAT9	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D9	driven 0	LD5	driven 0	R0	R2
FPDAT10	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D10	driven 0	LD6	driven 0	driven 0	R1
FPDAT11	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D11	driven 0	LD7	driven 0	G0	G2
FPDAT12	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D12	driven 0	UD4	driven 0	driven 0	G1
FPDAT13	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D13	driven 0	UD5	driven 0	driven 0	G0
FPDAT14	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D14	driven 0	UD6	driven 0	B0	B2
FPDAT15	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D15	driven 0	UD7	driven 0	driven 0	B1

◆ CRT Interface

The following figure shows the external circuitry for the CRT interface.



External Circuitry for CRT Interface

■ D.C. CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
DAC V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	˚C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	˚C

Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	V_{SS} = 0V	2.7	3.0/3.3/5.0	5.5	V
V_{IN}	Input Voltage		V_{SS}		V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	˚C

Electrical Characteristics for V_{DD} = 5.0V Typical

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			400	µA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	V_{DD} = min I_{OL} = -4mA (Type1), -8mA (Type2), -12mA (Type3)	V_{DD} - 0.4			V
V_{OL}	Low Level Output Voltage	V_{DD} = min I_{OL} = 4mA (Type1), 8mA (Type2), 12mA (Type3)			0.4	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = max	3.5			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = min			1.0	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 5.0V			4.0	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 5.0V	0.8			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 5.0V	0.3			V
R_{PD}	Pull Down Resistance	V_I = V_{DD}	50	100	200	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

Electrical Characteristics for V_{DD} = 3.3V Typical

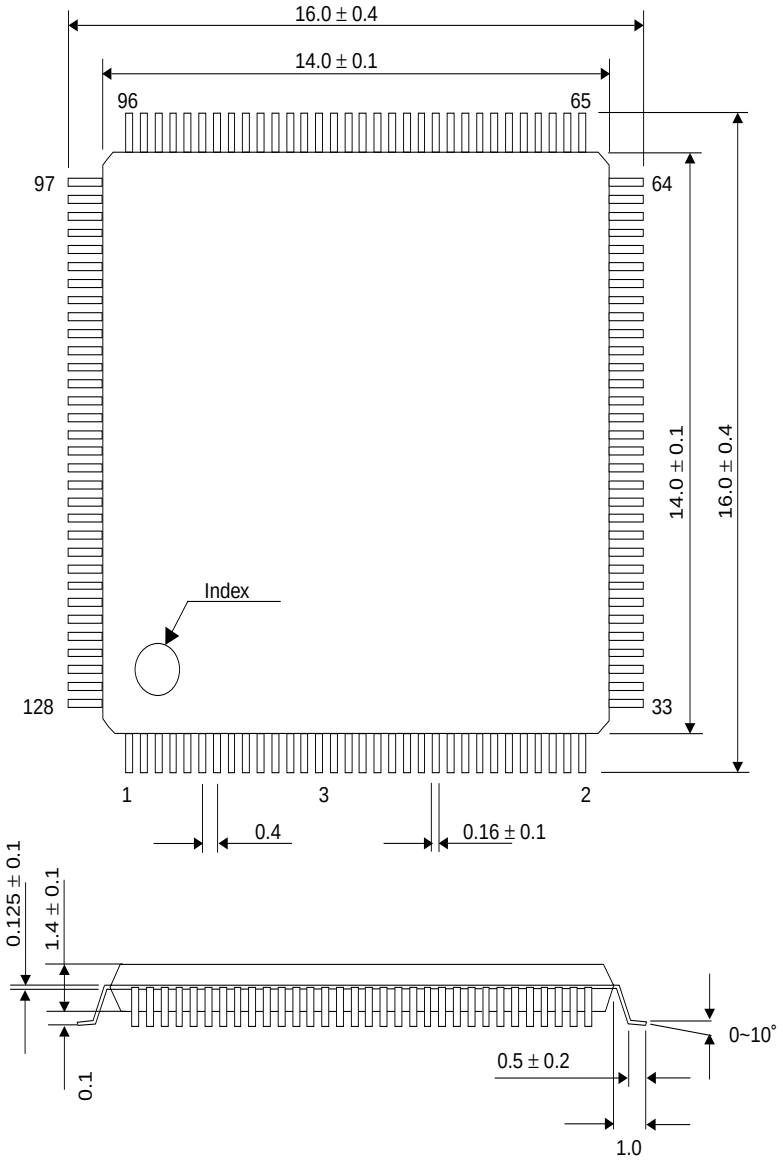
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			290	µA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	V_{DD} = min I_{OL} = -2mA (Type1), -4mA (Type2), -6mA (Type3)	V_{DD} - 0.3			V
V_{OL}	Low Level Output Voltage	V_{DD} = min I_{OL} = 2mA (Type1), 4mA (Type2), 6mA (Type3)			0.3	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = max	2.2			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = min			0.8	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 3.3V			2.4	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 3.3V	0.6			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 3.3V	0.1			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	90	180	360	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

Electrical Characteristics for V_{DD} = 3.0V Typical

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			260	µA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	V_{DD} = min I_{OL} = -1.8mA (Type1), -3.5mA (Type2), -5mA (Type3)	V_{DD} - 0.3			V
V_{OL}	Low Level Output Voltage	V_{DD} = min I_{OL} = 1.8mA (Type1), 3.5mA (Type2), 5mA (Type3)			0.3	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = max	2.0			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = min			0.8	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 3.0V			2.3	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 3.0V	0.5			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 3.0V	0.1			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	100	200	400	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

■ MECHANICAL DATA

128-pin QFP15 surface mount package



Mechanical Drawing QFP15

S1D13505F00A

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