Preliminary

S1D15104 Series Technical Manual

S1D15104D00B000

Rev.0.1

- This specification is a preliminary version.
- All values in this specification are tentative and may change in the later.

Evaluation board/kit and Development tool important notice

1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purposes. It is not intended to meet the requirements of design for finished products.
2. This evaluation board/kit or development tool is intended for use by an electronics engineer and is not a consumer product. The user should use it properly and in a safe manner. Seiko Epson dose not assume any responsibility or liability of any kind of damage and/or fire coursed by the use of it. The user should cease to use it when any abnormal issue occurs even during proper and safe use.
3. The part used for this evaluation board/kit or development tool may be changed without any notice.

NOTICE

Table of Contents

1. Description

The S1D15104 series (hereinafter referred to as “S1D15104”) is an LCD driver designed for segment type LCD display system and can be connected directly to the bus of the microcomputer. The S1D15104 stores serial display data transmitted by the microcomputer to the built-in display data RAM, and all LCD drive signals are generated by this IC independently from the microcomputer.
The S1D15104 contains the display data RAM with a capacity of 120 × 4 × 2 bits, 120 segment output circuits and 4 common output circuits. The maximum display resolution of S1D15104 is 480 pixels and there is a one-to-one correspondence between each of the bits in the display data RAM and each of the pixels on the LCD panel. In addition, multiple chips can be cascaded as a master/slave connection to extend larger LCD displays.
The S1D15104 features a built-in oscillation circuit and an LCD bias generating circuit that can be comprised of a display system with minimized number of external components.

2. Features

- Serial Interface (Selectable by pin setting)
  - 4-wire (SPI)
  - 2-wire (I2C compliant)
- Display Data RAM
  - Capacity: 120 x 4 x 2 = 960 bits
- LCD Driver
  - Segment: 120 outputs
  - Common: 4 outputs
- LCD Drive Duty Configuration
  - 1/4, 1/3, 1/2, 1/1(Static drive)
    Applicable for +1H Dummy ON/OFF
- LCD Drive Bias Configuration
  - 1/3, 1/2, 1/1(Static drive)
- Built-in Power Supply Circuit for LCD Drive
  - VLCD voltage generating circuit
    - Electronic volume
    - Voltage regulator circuit for booster (VDC regulator)
    - Booster circuit with built-in capacitor
  - Bias voltages (V1, V2, V3, V4) generating circuit
  - Applicable for external power supply
- Built-in Oscillation Circuit
  - Adjustable frame frequency by command setting (Max. 381Hz)
  - Applicable for external clock input
- A Variety of Command Functions
- Read Function for IC Revision and Lot Number (Only for 4-wire serial interface)
- Power-on Reset Function
- Extendable Display Capacity by comprising of Master/Slave Connection
- Operating Power Supply Voltages
  - LCD Drive VLCD : 2.7V (*1) to 8.0V (*2)
    **1: min. 4.5V (TBD) in case of 1/3 and 1/2 bias*
    **2: max. 7.0V in case of using VLCD voltage generating circuit*
  - Booster : VDD2 : 2.7V to 5.5V
  - Logic : VDD : 2.7V to 5.5V
- Shipping Form
  - Au bump chip
- Operating Temperature Range
  - -40 to +105℃
- AEC-Q100 Corresponsive
- This IC is not designed to comply with radiation- or light- protected design. Refer to the description in section “13. Precautions”.

3. Block Diagram

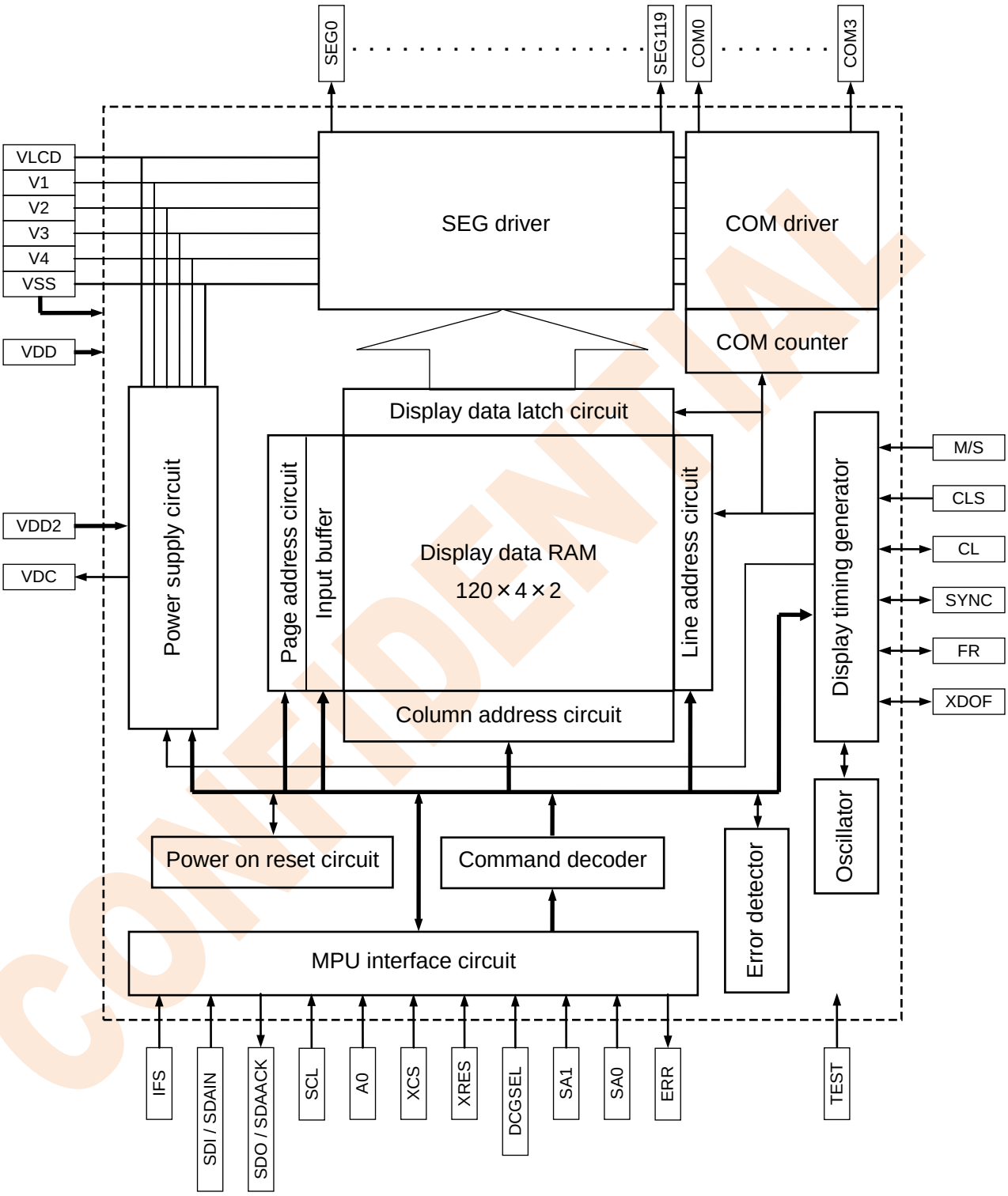


Figure 3 Block Diagram of S1D15104

4. Pin Assignment

4.1 Chip Specifications

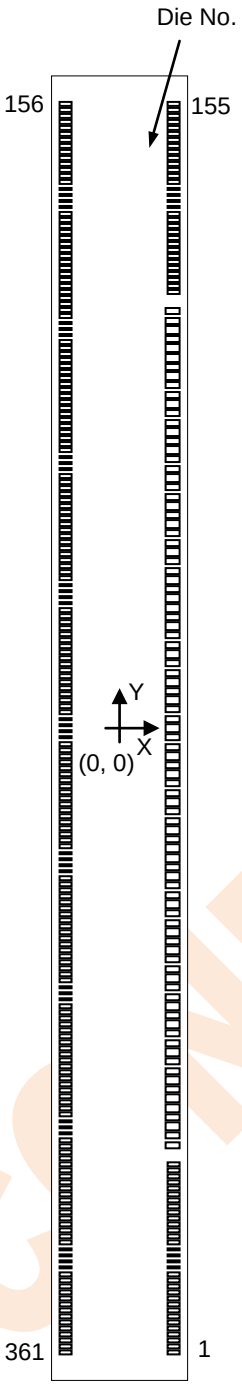
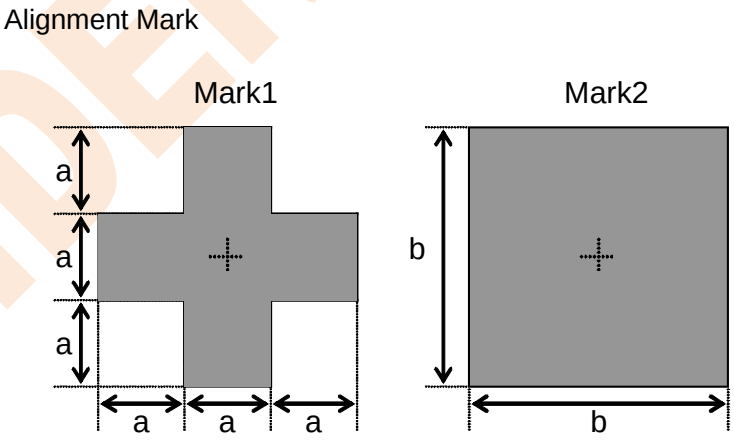


Table 4.1 Chip Specifications

Parameter		Dimensions X	Dimensions Y	Unit
Chip Size		1.109	10.703	mm
Chip Thickness		300		μm
Bump Pitch		min. 50		μm
Bump Size	No. 1 to 32	95	30	μm
	No. 33 to 123	111	56	μm
	No. 124 to 361	95	30	μm
Bump Height		12		μm
Bump Area Total		1335156		μm^2
Linear Coefficient of Thermal Expansion		2.6×10^{-6}		/℃

Note: These values are provided for reference only and not guaranteed.



Alignment Mark Center Coordinates (Unit: μm)
Mark1 (452.5, -5249.5)
Mark2 (452.5, 5249.5)

Size
a=15μm, b=45μm

Figure 4.1 Bump Assignment Drawing

4.2 Bump Center Coordinates

Table 4.2 Bump Center Coordinates

BUMP No.	Pin Name	X (µm)	Y (µm)
1	NC	445.0	-5125.0
2	NC	445.0	-5075.0
3	NC	445.0	-5025.0
4	NC	445.0	-4975.0
5	NC	445.0	-4925.0
6	NC	445.0	-4875.0
7	NC	445.0	-4825.0
8	NC	445.0	-4775.0
9	NC	445.0	-4725.0
10	NC	445.0	-4675.0
11	NC	445.0	-4625.0
12	NC	445.0	-4575.0
13	NC	445.0	-4525.0
14	NC	445.0	-4475.0
15	NC	445.0	-4425.0
16	NC	445.0	-4375.0
17	NC	445.0	-4325.0
18	NC	445.0	-4275.0
19	NC	445.0	-4225.0
20	NC	445.0	-4175.0
21	NC	445.0	-4125.0
22	NC	445.0	-4075.0
23	NC	445.0	-4025.0
24	NC	445.0	-3975.0
25	NC	445.0	-3925.0
26	NC	445.0	-3875.0
27	NC	445.0	-3825.0
28	COM0	445.0	-3775.0
29	COM1	445.0	-3725.0
30	COM2	445.0	-3675.0
31	COM3	445.0	-3625.0
32	NC	445.0	-3575.0
33	NC	437.0	-3420.0
34	V4	437.0	-3344.0
35	V4	437.0	-3268.0
36	V4	437.0	-3192.0
37	V4	437.0	-3116.0
38	V3	437.0	-3040.0
39	V3	437.0	-2964.0
40	V3	437.0	-2888.0

BUMP No.	Pin Name	X (µm)	Y (µm)
41	V3	437.0	-2812.0
42	NC	437.0	-2736.0
43	V2	437.0	-2660.0
44	V2	437.0	-2584.0
45	V2	437.0	-2508.0
46	V2	437.0	-2432.0
47	V1	437.0	-2356.0
48	V1	437.0	-2280.0
49	V1	437.0	-2204.0
50	V1	437.0	-2128.0
51	VLCD	437.0	-2052.0
52	VLCD	437.0	-1976.0
53	VLCD	437.0	-1900.0
54	VLCD	437.0	-1824.0
55	VLCD	437.0	-1748.0
56	VLCD	437.0	-1672.0
57	VLCD	437.0	-1596.0
58	VLCD	437.0	-1520.0
59	VLCD	437.0	-1444.0
60	VLCD	437.0	-1368.0
61	NC	437.0	-1292.0
62	VDC	437.0	-1216.0
63	VDD2	437.0	-1140.0
64	VDD2	437.0	-1064.0
65	VDD2	437.0	-988.0
66	VDD2	437.0	-912.0
67	VDD2	437.0	-836.0
68	VDD2	437.0	-760.0
69	VDD	437.0	-684.0
70	VDD	437.0	-608.0
71	VDD	437.0	-532.0
72	VDD	437.0	-456.0
73	VDD	437.0	-380.0
74	VDD	437.0	-304.0
75	IFS	437.0	-228.0
76	SA0	437.0	-152.0
77	VSS	437.0	-76.0
78	SA1	437.0	0.0
79	VDD	437.0	76.0
80	M/S	437.0	152.0

Table 4.2 Bump Center Coordinates (continued)

BUMP No.	Pin Name	X (μm)	Y (μm)
81	CLS	437.0	228.0
82	TEST1	437.0	304.0
83	TEST2	437.0	380.0
84	TEST3	437.0	456.0
85	TEST4	437.0	532.0
86	TEST5	437.0	608.0
87	VSS	437.0	684.0
88	VSS	437.0	760.0
89	VSS	437.0	836.0
90	VSS	437.0	912.0
91	VSS	437.0	988.0
92	VSS	437.0	1064.0
93	TEST11	437.0	1140.0
94	TEST12	437.0	1216.0
95	TEST13	437.0	1292.0
96	VSS	437.0	1368.0
97	VSS	437.0	1444.0
98	VSS	437.0	1520.0
99	VSS	437.0	1596.0
100	VSS	437.0	1672.0
101	TEST6	437.0	1748.0
102	TEST7	437.0	1824.0
103	TEST8	437.0	1900.0
104	TEST9	437.0	1976.0
105	TEST10	437.0	2052.0
106	DCGSEL	437.0	2128.0
107	VDD	437.0	2204.0
108	XRES	437.0	2280.0
109	XCS	437.0	2356.0
110	A0	437.0	2432.0
111	VSS	437.0	2508.0
112	SDI/SDAIN	437.0	2584.0
113	SDI/SDAIN	437.0	2660.0
114	SDO/SDAACK	437.0	2736.0
115	SDO/SDAACK	437.0	2812.0
116	SCL	437.0	2888.0
117	SCL	437.0	2964.0
118	ERR	437.0	3040.0
119	CL	437.0	3116.0
120	SYNC	437.0	3192.0
121	FR	437.0	3268.0
122	XDOF	437.0	3344.0
123	NC	437.0	3420.0
124	NC	445.0	3575.0
125	COM3	445.0	3625.0
126	COM2	445.0	3675.0
127	COM1	445.0	3725.0
128	COM0	445.0	3775.0
129	NC	445.0	3825.0
130	NC	445.0	3875.0
131	NC	445.0	3925.0
132	NC	445.0	3975.0
133	NC	445.0	4025.0
134	NC	445.0	4075.0
135	NC	445.0	4125.0
136	NC	445.0	4175.0
137	NC	445.0	4225.0
138	NC	445.0	4275.0
139	NC	445.0	4325.0
140	NC	445.0	4375.0
141	NC	445.0	4425.0
142	NC	445.0	4475.0
143	NC	445.0	4525.0
144	NC	445.0	4575.0
145	NC	445.0	4625.0
146	NC	445.0	4675.0
147	NC	445.0	4725.0
148	NC	445.0	4775.0
149	NC	445.0	4825.0
150	NC	445.0	4875.0
151	NC	445.0	4925.0
152	NC	445.0	4975.0
153	NC	445.0	5025.0
154	NC	445.0	5075.0
155	NC	445.0	5125.0
156	NC	-445.0	5125.0
157	NC	-445.0	5075.0
158	NC	-445.0	5025.0
159	NC	-445.0	4975.0
160	NC	-445.0	4925.0

Table 4.2 Bump Center Coordinates (continued)

BUMP No.	Pin Name	X (μm)	Y (μm)
161	NC	-445.0	4875.0
162	NC	-445.0	4825.0
163	NC	-445.0	4775.0
164	NC	-445.0	4725.0
165	NC	-445.0	4675.0
166	NC	-445.0	4625.0
167	NC	-445.0	4575.0
168	NC	-445.0	4525.0
169	NC	-445.0	4475.0
170	NC	-445.0	4425.0
171	NC	-445.0	4375.0
172	NC	-445.0	4325.0
173	NC	-445.0	4275.0
174	NC	-445.0	4225.0
175	NC	-445.0	4175.0
176	NC	-445.0	4125.0
177	NC	-445.0	4075.0
178	NC	-445.0	4025.0
179	NC	-445.0	3975.0
180	NC	-445.0	3925.0
181	NC	-445.0	3875.0
182	NC	-445.0	3825.0
183	NC	-445.0	3775.0
184	NC	-445.0	3725.0
185	NC	-445.0	3675.0
186	NC	-445.0	3625.0
187	NC	-445.0	3575.0
188	NC	-445.0	3525.0
189	NC	-445.0	3475.0
190	NC	-445.0	3425.0
191	NC	-445.0	3375.0
192	NC	-445.0	3325.0
193	NC	-445.0	3275.0
194	SEG0	-445.0	3225.0
195	SEG1	-445.0	3175.0
196	SEG2	-445.0	3125.0
197	SEG3	-445.0	3075.0
198	SEG4	-445.0	3025.0
199	SEG5	-445.0	2975.0
200	SEG6	-445.0	2925.0

BUMP No.	Pin Name	X (μm)	Y (μm)
201	SEG7	-445.0	2875.0
202	SEG8	-445.0	2825.0
203	SEG9	-445.0	2775.0
204	SEG10	-445.0	2725.0
205	SEG11	-445.0	2675.0
206	SEG12	-445.0	2625.0
207	SEG13	-445.0	2575.0
208	SEG14	-445.0	2525.0
209	SEG15	-445.0	2475.0
210	SEG16	-445.0	2425.0
211	SEG17	-445.0	2375.0
212	SEG18	-445.0	2325.0
213	SEG19	-445.0	2275.0
214	SEG20	-445.0	2225.0
215	SEG21	-445.0	2175.0
216	SEG22	-445.0	2125.0
217	SEG23	-445.0	2075.0
218	SEG24	-445.0	2025.0
219	SEG25	-445.0	1975.0
220	SEG26	-445.0	1925.0
221	SEG27	-445.0	1875.0
222	SEG28	-445.0	1825.0
223	SEG29	-445.0	1775.0
224	SEG30	-445.0	1725.0
225	SEG31	-445.0	1675.0
226	SEG32	-445.0	1625.0
227	SEG33	-445.0	1575.0
228	SEG34	-445.0	1525.0
229	SEG35	-445.0	1475.0
230	SEG36	-445.0	1425.0
231	SEG37	-445.0	1375.0
232	SEG38	-445.0	1325.0
233	SEG39	-445.0	1275.0
234	SEG40	-445.0	1225.0
235	SEG41	-445.0	1175.0
236	SEG42	-445.0	1125.0
237	SEG43	-445.0	1075.0
238	SEG44	-445.0	1025.0
239	SEG45	-445.0	975.0
240	SEG46	-445.0	925.0

Table 4.2 Bump Center Coordinates (continued)

BUMP No.	Pin Name	X (μm)	Y (μm)
241	SEG47	-445.0	875.0
242	SEG48	-445.0	825.0
243	SEG49	-445.0	775.0
244	SEG50	-445.0	725.0
245	SEG51	-445.0	675.0
246	SEG52	-445.0	625.0
247	SEG53	-445.0	575.0
248	SEG54	-445.0	525.0
249	SEG55	-445.0	475.0
250	SEG56	-445.0	425.0
251	SEG57	-445.0	375.0
252	SEG58	-445.0	325.0
253	SEG59	-445.0	275.0
254	NC	-445.0	225.0
255	COM0	-445.0	175.0
256	COM1	-445.0	125.0
257	COM2	-445.0	75.0
258	COM3	-445.0	25.0
259	NC	-445.0	-25.0
260	NC	-445.0	-75.0
261	NC	-445.0	-125.0
262	NC	-445.0	-175.0
263	NC	-445.0	-225.0
264	SEG60	-445.0	-275.0
265	SEG61	-445.0	-325.0
266	SEG62	-445.0	-375.0
267	SEG63	-445.0	-425.0
268	SEG64	-445.0	-475.0
269	SEG65	-445.0	-525.0
270	SEG66	-445.0	-575.0
271	SEG67	-445.0	-625.0
272	SEG68	-445.0	-675.0
273	SEG69	-445.0	-725.0
274	SEG70	-445.0	-775.0
275	SEG71	-445.0	-825.0
276	SEG72	-445.0	-875.0
277	SEG73	-445.0	-925.0
278	SEG74	-445.0	-975.0
279	SEG75	-445.0	-1025.0
280	SEG76	-445.0	-1075.0
281	SEG77	-445.0	-1125.0
282	SEG78	-445.0	-1175.0
283	SEG79	-445.0	-1225.0
284	SEG80	-445.0	-1275.0
285	SEG81	-445.0	-1325.0
286	SEG82	-445.0	-1375.0
287	SEG83	-445.0	-1425.0
288	SEG84	-445.0	-1475.0
289	SEG85	-445.0	-1525.0
290	SEG86	-445.0	-1575.0
291	SEG87	-445.0	-1625.0
292	SEG88	-445.0	-1675.0
293	SEG89	-445.0	-1725.0
294	SEG90	-445.0	-1775.0
295	SEG91	-445.0	-1825.0
296	SEG92	-445.0	-1875.0
297	SEG93	-445.0	-1925.0
298	SEG94	-445.0	-1975.0
299	SEG95	-445.0	-2025.0
300	SEG96	-445.0	-2075.0
301	SEG97	-445.0	-2125.0
302	SEG98	-445.0	-2175.0
303	SEG99	-445.0	-2225.0
304	SEG100	-445.0	-2275.0
305	SEG101	-445.0	-2325.0
306	SEG102	-445.0	-2375.0
307	SEG103	-445.0	-2425.0
308	SEG104	-445.0	-2475.0
309	SEG105	-445.0	-2525.0
310	SEG106	-445.0	-2575.0
311	SEG107	-445.0	-2625.0
312	SEG108	-445.0	-2675.0
313	SEG109	-445.0	-2725.0
314	SEG110	-445.0	-2775.0
315	SEG111	-445.0	-2825.0
316	SEG112	-445.0	-2875.0
317	SEG113	-445.0	-2925.0
318	SEG114	-445.0	-2975.0
319	SEG115	-445.0	-3025.0
320	SEG116	-445.0	-3075.0

Table 4.2 Bump Center Coordinates (continued)

BUMP No.	Pin Name	X (μm)	Y (μm)
321	SEG117	-445.0	-3125.0
322	SEG118	-445.0	-3175.0
323	SEG119	-445.0	-3225.0
324	NC	-445.0	-3275.0
325	NC	-445.0	-3325.0
326	NC	-445.0	-3375.0
327	NC	-445.0	-3425.0
328	NC	-445.0	-3475.0
329	NC	-445.0	-3525.0
330	NC	-445.0	-3575.0
331	NC	-445.0	-3625.0
332	NC	-445.0	-3675.0
333	NC	-445.0	-3725.0
334	NC	-445.0	-3775.0
335	NC	-445.0	-3825.0
336	NC	-445.0	-3875.0
337	NC	-445.0	-3925.0
338	NC	-445.0	-3975.0
339	NC	-445.0	-4025.0
340	NC	-445.0	-4075.0
341	NC	-445.0	-4125.0
342	NC	-445.0	-4175.0
343	NC	-445.0	-4225.0
344	NC	-445.0	-4275.0
345	NC	-445.0	-4325.0
346	NC	-445.0	-4375.0
347	NC	-445.0	-4425.0
348	NC	-445.0	-4475.0
349	NC	-445.0	-4525.0
350	NC	-445.0	-4575.0
351	NC	-445.0	-4625.0
352	NC	-445.0	-4675.0
353	NC	-445.0	-4725.0
354	NC	-445.0	-4775.0
355	NC	-445.0	-4825.0
356	NC	-445.0	-4875.0
357	NC	-445.0	-4925.0
358	NC	-445.0	-4975.0
359	NC	-445.0	-5025.0
360	NC	-445.0	-5075.0
361	NC	-445.0	-5125.0

5. Pin Description

5.1 Power Pins

Pin Name	I/O	Description	Pin Count
VDD	Power I	System power supply pins. Must be supplied common voltage with MPU power supply VCC.	8
VDD2	Power I	Power supply pins for VLCD voltage generating circuit. Must be connected to VDD when supplying same voltage level as VDD or not using VLCD voltage generating circuit.	6
VSS	Power I	0V pins connected to System GND.	13

5.2 Power Pins for LCD Drive

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Pin Count</th></tr>
<tr><td>VDC</td><td>O</td><td>Regulator output pin for booster circuit. Must be left open.</td><td>1</td></tr>
<tr><td>VLCD</td><td>Power
I/O</td><td>Power pins for LCD drive.
● When using VLCD voltage generating circuit, VLCD voltage is output. Must be connected stabilizing capacitors between VSS and VLCD pins.
● When not using VLCD voltage generating circuit, must be supplied VLCD voltage from external power source.</td><td>10</td></tr>
<tr><td>V1
V2
V3
V4</td><td>Power
I/O</td><td>Bias power pins for LCD drive.
● When using bias voltage generating circuit, the following voltages for each of bias pins are output. The bias selection is defined by the command setting. Because the V2 and V3 with 1/2 bias setting and the V1 to V4 with 1/1 bias setting are not used, those outputs are high-impedance (“HZ”) state.
<table>
<tr><th></th><th>1/3 Bias</th><th>1/2 Bias</th><th>1/1 Bias</th></tr>
<tr><td>V1</td><td>2/3 VLCD</td><td>1/2 VLCD</td><td>(“HZ”)</td></tr>
<tr><td>V2</td><td>1/3 VLCD</td><td>(“HZ”)</td><td>(“HZ”)</td></tr>
<tr><td>V3</td><td>2/3 VLCD</td><td>(“HZ”)</td><td>(“HZ”)</td></tr>
<tr><td>V4</td><td>1/3 VLCD</td><td>1/2 VLCD</td><td>(“HZ”)</td></tr>
</table>
● When not using bias voltage generating circuit, the following V1, V2, V3 and V4 voltages must be supplied from external power source. (The V2 and V3 voltages when 1/2 bias setting and the V1 to V4 voltages when 1/1 bias setting must also be supplied.)
<table>
<tr><th></th><th>1/3 Bias</th><th>1/2 Bias</th><th>1/1 Bias</th></tr>
<tr><td>V1</td><td>2/3 VLCD</td><td>1/2 VLCD</td><td>VLCD</td></tr>
<tr><td>V2</td><td>1/3 VLCD</td><td>VSS</td><td>VSS</td></tr>
<tr><td>V3</td><td>2/3 VLCD</td><td>VLCD</td><td>VLCD</td></tr>
<tr><td>V4</td><td>1/3 VLCD</td><td>1/2 VLCD</td><td>VSS</td></tr>
</table>
</td><td>8
(2 for each)</td></tr>
</table>

5.3 MPU Interface Pins

Pin Name	I/O	Description	Pin Count
IFS	I	Interface select pin. IFS="L": 4-wire serial interface (SPI) IFS="H": 2-wire serial interface (I2C-Bus compliant)	1
SDI / SDAIN	I	Serial data input pins. Use for control command and display data input. The input data is read by the rising edge of the input signal SCL. ● 4-wire serial interface (IFS="L"): SDI input pins. ● 2-wire serial interface (IFS="H"): SDAIN input pins.	2
SDO / SDAACK	O	● 4-wire serial interface (IFS="L"): SDO serial data output pins. The output data is only applicable when reading by commands RDICREV or RDICLOT and the data is output at the falling edge of the input signal SCL. In the other conditions, this pin outputs High-impedance ("HiZ") state. ● 2-wire serial interface (IFS="H"): SDAACK acknowledge output pins. This pin outputs "L" level from the falling edge of the 8th bit to the falling edge of the 9th bit of the input signal SCL. In the other conditions, this pin outputs High-impedance ("HiZ") state.	2
SCL	I	Serial clock input pins.	2
A0	I	SI input discrimination pin. ● 4-wire serial interface (IFS="L"): SDI input discrimination pin. A0="H": SDI input is command parameter. A0="L": SDI input is command. ● 2-wire serial interface (IFS="H"): Invalid. It is recommended to be tied to "L" level.	1
XCS	I	Chip select pin. ● 4-wire serial interface (IFS="L"): Chip select pin. XCS="L": Active. Data/Command input and output can be enabled. XCS="H": Inactive. Data/Command input and output can be disabled. ● 2-wire serial interface (IFS="H"): Invalid. It is recommended to be tied to "L" level.	1
XRES	I	Reset pin. When XRES="L", this IC is initialized. This IC contains power-on reset function. When using only power-on reset function without this reset pin, this pin must be tied to "H" level.	1
DCGSEL	I	Discharge ON/OFF select pin during execution of resetting (XRES="L"). This pin is enabled in case of master mode (M/S="H"). DCGSEL="H": Discharge ON during execution of resetting (XRES="L"). DCGSEL="L": Discharge OFF during execution of resetting (XRES="L"). In case of slave mode (M/S="L"), this pin is disabled and discharge OFF during execution of resetting (XRES="L"). It is recommended to be tied to "L" level.	1
SA1, SA0	I	● 2-wire serial interface (IFS="H"): Slave address (*1) setting pin of this IC. The upper 5 bits from MSB of 7 bits address are fixed to (0,1,1,1,0). The slave address is set by connecting lower 2 bits, SA1 and SA0 (LSB), to either "H" or "L" level. *1: The "Slave" described here is different from a "Slave" used for cascading of these ICs as a master/slave connection, is a general term of the I2C-Bus interface. ● 4-wire serial interface (IFS="L"): Invalid. It is recommended to be tied to "L" level.	2 (1 for each)
ERR	O	Monitoring pin for operating status of this IC. ERR="L": Normal operation. No error detected. ERR="H": Initial state or error detected. When ERR="H", a part of the internal registers may occur a bit error caused by an excessive external noise. All commands and all display data must be rewrite to the internal registers and to the display data RAM. In addition, ERR="H" during initial state after resetting.	1

5.4 Display Timing Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Pin Count</th></tr>
<tr><td>M/S</td><td>I</td><td>Master or slave operation select pin.
M/S=”H”: Master operation
M/S=”L”: Slave operation
In a master operation, the necessary timing signals using for LCD display is output. Then in a slave operation, the necessary timing signals using for LCD display is input. The built-in oscillation circuit and the built-in power supply circuit for LCD drive can be enabled for only master operation.
The following table indicates the setting configuration by pin M/S and CLS
<table>
<tr><th>M/S</th><th>CLS</th><th>Display Clock Source</th><th>Power Supply Circuit</th><th>CL</th><th>SYNC</th><th>FR</th><th>XDOF</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Built-in Oscillation Circuit</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>External</td><td>Enable</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>“H” or “L"</td><td>External</td><td>Disable</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table>
When using this IC as a single chip, this pin must be tied to “H”.</td><td>1</td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillation circuit select pin.
When this IC is used as master operation (M/S=”H”), this pin selects display clock as either generated by built-in oscillation circuit or supplied from external clock input.
M/S=”H”, CLS=”H”: Generated by built-in oscillation circuit.
M/S=”H”, CLS=”L”: Supplied from external clock input.
When this IC is used as slave operation (M/S=”L”), display clock is supplied from external clock input in both CLS settings as “H” and “L” level.
In case of external clock input, display clock is supplied from the CL pin.</td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input and output pin.
M/S=”H” and CLS=”H”: CL is output.
M/S=”L” or CLS=”L”: CL is input.
In case of using this IC as a master/slave connection, each of the CL pins in master and slave chip must be connected together.</td><td>1</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>Display frame start signal input and output pin.
M/S=”H”: SYNC is output.
M/S=”L”: SYNC is input.
In case of using this IC as a master/slave connection, each of the SYNC pins in master and slave chip must be connected together.</td><td></td></tr>
<tr><td>FR</td><td>I/O</td><td>AC signal input and output pin.
M/S=”H”: FR is output.
M/S=”L”: FR is input.
In case of using this IC as a master/slave connection, each of the FR pins in master and slave chip must be connected together.</td><td>1</td></tr>
<tr><td>XDOF</td><td>I/O</td><td>Display blanking control pin.
M/S=”H”: XDOF is output.
M/S=”L”: XDOF is input.
In case of using this IC as a master/slave connection, each of the XDOF pins in master and slave chip must be connected together.</td><td>1</td></tr>
</table>

5.5 LCD Output Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Pin Count</th></tr>
<tr><td>SEG0
to
SEG119</td><td>O</td><td>LCD segment drive output pins.
Either VLCD, V2, V3 or VSS level is selected by the following conditions of the display data stored in display data RAM and the FR signal.
The VSS level is output when Display OFF mode1 (DISOFF1) or power saving mode.
The off-state level (“0” level of RAM data in case of normal display mode or “1” level of RAM data in case of inverted display mode) is output when Display OFF mode2 (DISOFF2).

<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverted Display</th></tr>
<tr><td rowspan="2">“1”</td><td>“H”</td><td>VLCD</td><td>V2</td></tr>
<tr><td>“L”</td><td>VSS</td><td>V3</td></tr>
<tr><td rowspan="2">“0”</td><td>“H”</td><td>V2</td><td>VLCD</td></tr>
<tr><td>“L”</td><td>V3</td><td>VSS</td></tr>
<tr><td>Display OFF1
Power Save</td><td>-</td><td>VSS</td><td>VSS</td></tr>
<tr><td rowspan="2">Display OFF2</td><td>“H”</td><td>V2</td><td>V2</td></tr>
<tr><td>“L”</td><td>V3</td><td>V3</td></tr>
</table>

Unused pins must be left open.</td><td>120
(1 for each)</td></tr>
<tr><td>COM0
to
COM3</td><td>O</td><td>LCD common drive output pins.
Either VLCD, V1 or V4 level is selected by the following conditions of the scan signal and the FR signal.
The VSS level is output when Display OFF mode1 (DISOFF1) or power saving mode.
The non-selected level is output when Display OFF mode2 (DISOFF2).

Either V0, V1, V4 or VSS level is selected by the following condition of the scanning signal and the FR signal.

<table>
<tr><th>Scan Signal</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td rowspan="2">Selected</td><td>“H”</td><td>VSS</td></tr>
<tr><td>“L”</td><td>VLCD</td></tr>
<tr><td rowspan="2">Non-selected</td><td>“H”</td><td>V1</td></tr>
<tr><td>“L”</td><td>V4</td></tr>
<tr><td>Display OFF1
Power Save</td><td>-</td><td>VSS</td></tr>
<tr><td rowspan="2">Display OFF2</td><td>“H”</td><td>V1</td></tr>
<tr><td>“L”</td><td>V4</td></tr>
</table>

Unused pins must be left open.</td><td>12
(3 for each)</td></tr>
</table>

5.6 Test Pins

Pin Name	I/O	Description	Pin Count
TEST1 to TEST10	I	Test pins of this IC. Must be tied to “L” level.	10 (1 for each)
TEST11	I/O	Test pins of this IC. Must be left open. This pin is “HZ” (High Impedance) state except for testing.	1
TEST12, TEST13	I/O	Test pins of this IC. Must be left open. These pins output “L” level except for testing.	2 (1 for each)

6. Functional Description

6.1 MPU Interface

6.1.1 Serial Interface Selection

The command and the display data transmitting between MPU and this IC is executed via the 4-wire (SPI) or the 2-wire (I2C-Bus compliant) serial interface. The following table indicates the interface type selection either the 4-wire (SPI) or the 2-wire (I2C-Bus compliant) serial interface by the IFS pin setting. Switching the serial interface type during an operation is prohibited.
In addition, this IC cannot provide a read function except by commands RDICREV and RDICLOT with 4-wire serial interface (SPI).

Table 6.1 Serial Interface Type

IFS	XCS	A0	SDI/SDAIN	SDO/SDAACK	SCL
L: 4-wire Serial Interface	XCS	A0	SDI	SDO	SCL
H: 2-wire Serial Interface	-	-	SDAIN	SDAACK	SCL

-: Must be tied to "H" or "L" level

6.1.2 4-wire Serial Interface (SPI)

The serial interface circuit is comprised of the 8-bit shift register and the 3-bit counter.
When the 4-wire serial interface type is selected (IFS="L"), the 8-bit serial data can be transmitted by the 4-wire containing of Chip Select (XCS), Serial Clock (SCL), Serial Data (SD *1) and Command/Parameter discrimination signal (A0).

**1: The SD pin is separated into the input pin SDI and the output pin SDO in this IC. The SDO pin is only used for reading IC revision and lot number by commands RDICREV and RDICLOT. When not using these reading functions described above, the SDO pin must be left open and the only use for the SDI pin. When using these reading functions described above, it can be used whether to be tied the SDI pin and the SDO pin together or to use as separated signals each other.*

The A0, SI, SCL signals can be accepted while this IC is in active state (XCS="L"). As for the data transmitting except the display data RAM write (WRRAM), IC revision read (RDICREV) and IC lot number read (RDICLOT) commands, the SD input data (SDI) is captured in order of D7, D6 to D0 at the rising edges of the SCL signal, and the A0 input is captured at the 8th rising edge of the SCL signal. The signal type of the serial data is discriminated as shown in Table 6.2 below.

Table 6.2 Signal Discrimination of Serial Data

A0	Serial Data
"L"	Command
"H"	Command Parameter

Figure 6.1 provides a timing diagram for the 4-wire serial interface.

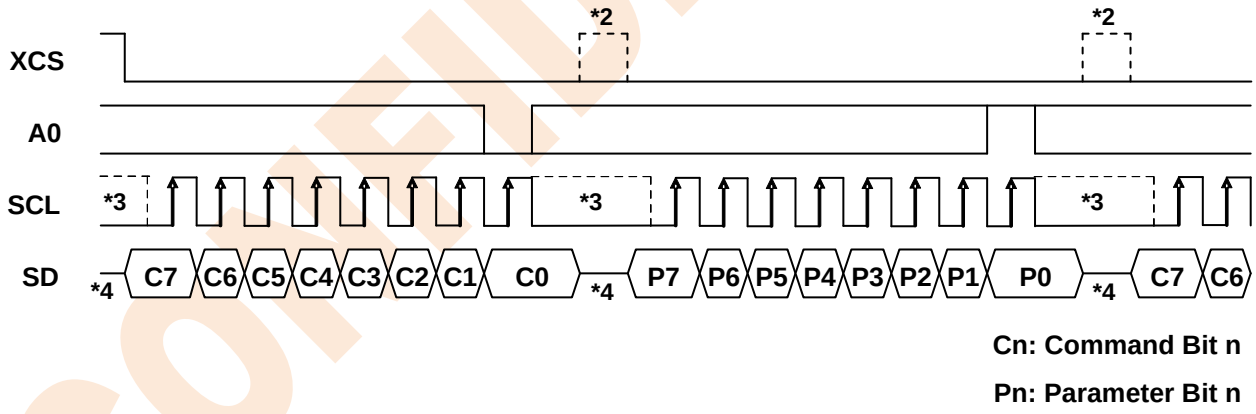


Figure 6.1 Write Operation for 4-wire Serial Interface

**2: In order to prevent malfunctions caused by the external noise, it is recommended to reset the serial counter by setting the XCS signal to "H" level in every 8 bits in case of inputting command except the WRRAM, RDICREV and RDICLOT commands.*
**3: The SCL signal can be set to either "H" or "L" level while the period of XCS="H".*
**4: The intermediate voltage level of the SD signal can be set to either "H" level, "L" level or open while the period of XCS="H".*

The data transmitting of the WRRAM command is also executed by 8 bits unit. However, the XCS signal input procedure is different from the other commands. After invoking the WRRAM command, the display data is written to the display data RAM at the rising edge of the SCL signal in order from D7, D6 to D0 by continuing to input the SCL and SDI signals while holding XCS= "L" level.
Figure 6.2 provides a timing diagram of the write operation to the display data RAM. After completion of the data transmitting, the XCS pin must be set to "H" level in order to release the write operation to the display data RAM.

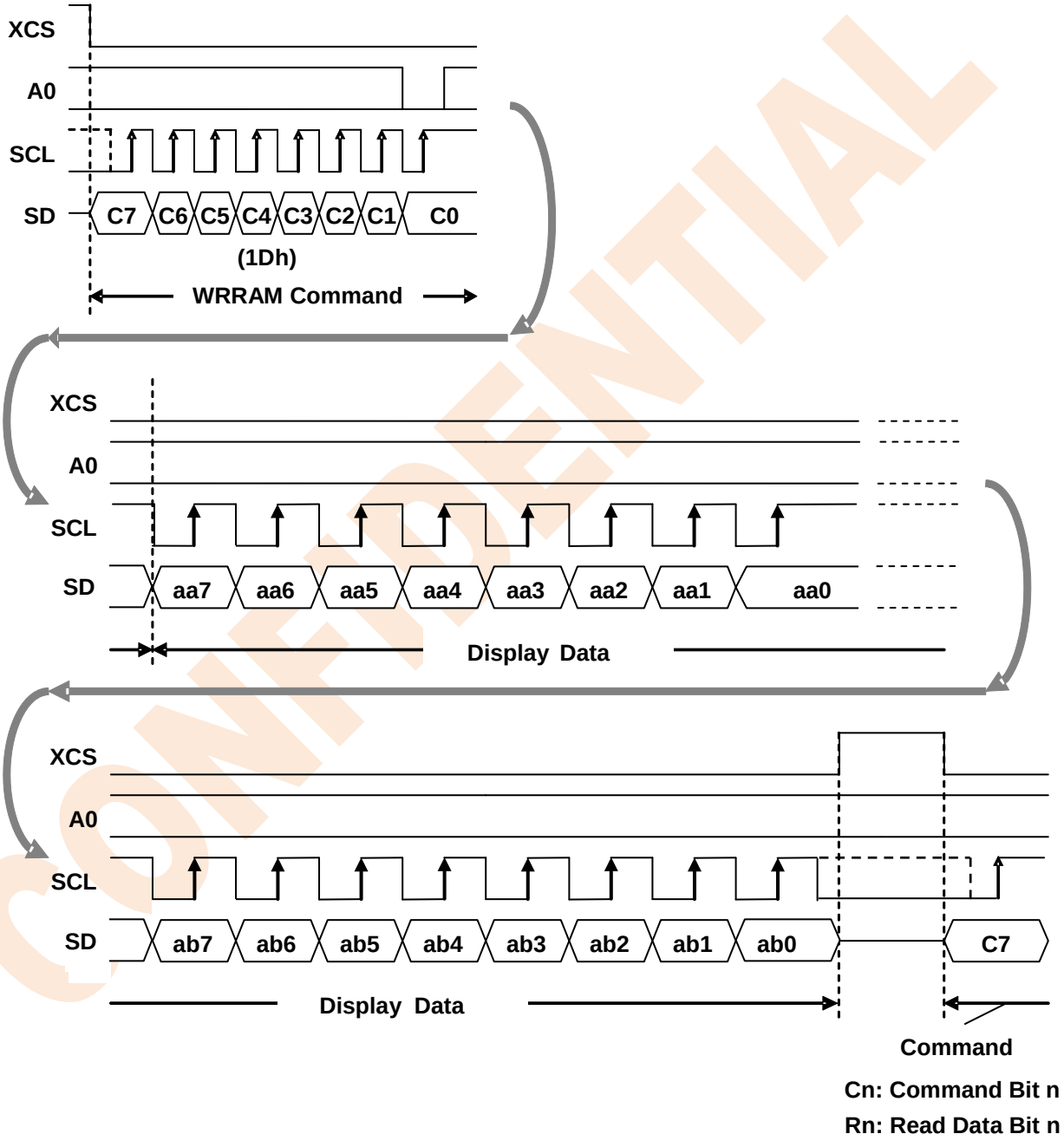


Figure 6.2 Display Data RAM Write Operation for Serial Interface (WRRAM Command)

The data transmitting of the RDICREV and RDICLOT commands are also executed by 8 bits unit. The XCS signal input procedure is different from the other commands as well as the WRRAM command. After invoking the RDICREV or RDICLOT commands, the data is output to the SD (SDO) pin at the falling edge of the SCL signal in order from D7, D6 to D0 by continuing to input the SCL signal while holding XCS= "L" level.
When using with the SDI pin and the SDO pin tied together, the data input from MPU side is prohibited because the SD pin is output state until completing the transmitting of the read data. When using the SDI pin and the SDO pin as separated signals each other, the data input from MPU side can be set either "H" level, "L" level or open state because the SDI pin is "HZ" (High-Impedance) state until completing the transmitting of the read data.
Figure 6.3 provides a timing diagram for read operation. After completing the data transmitting, the XCS pin must be set to "H" level in order to cancel the read operation. In addition, the SD pin releases the output state at the rising edge of the SCL signal on last bit as shown R40 bit in Figure 6.2.
The intermediate voltage level in this figure can be set either "H" level, "L" level or open state.

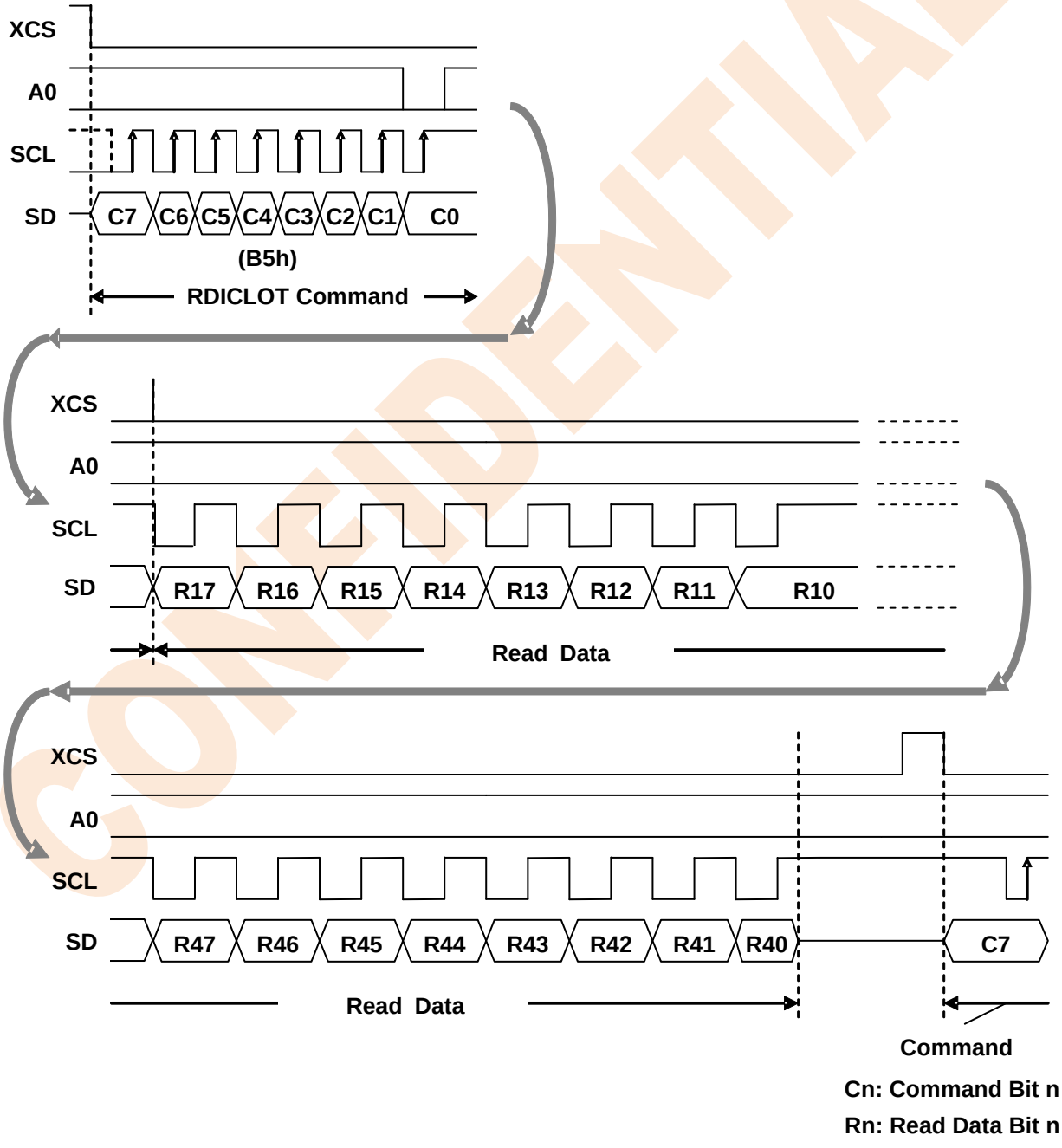


Figure 6.3 Read Operation Example for Serial Interface (RDICLOT Command)

6.1.3 2-wire Serial Interface (I2C-Bus Compliant)

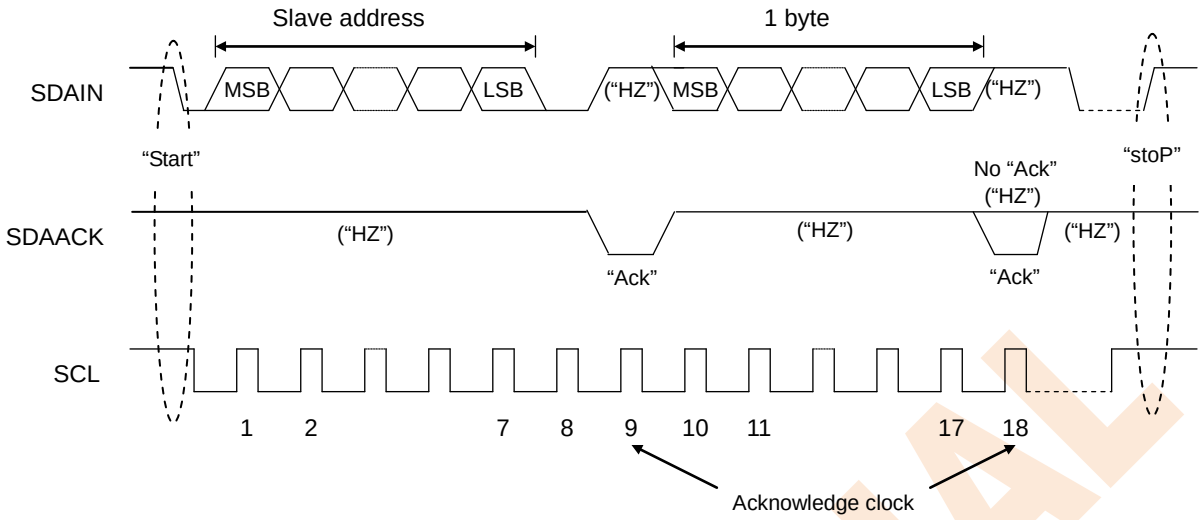
When the 2-wire serial interface is selected (IFS=”H”), the interface of this IC is complied with the I2C-Bus specification.
The I2C-Bus is comprised of two bus lines assigned to the serial data line (SDA) and the serial clock line (SCL), and these lines are connected to VDD with parallel resistance. Each device connected to the buses has a unique address, and can be specified with using this address. The data communication can be executed based on the relation between master and slave (*1), however this IC cannot be operated as a master chip and can only be operated as a slave chip.

**1: The “Master” and “Slave” described in this section is different from a “Master” and a “Slave” used for cascading of these ICs as a master/slave connection, is a general term of the I2C-Bus interface.*

The slave address is set by tying the salve address pins (SA1 and SA0) to either "H" or "L" level. This IC supports 7-bit address and the upper 5 bits from the MSB of the address are fixed to (0, 1, 1, 1, 0). The slave address is set by tying lower 2 bits, SA1 and SA0 (LSB), to either “H” or “L” level.
The communication with the master device starts when the SDA line changes from "H" to "L" levels during the period of SCL="H" (“Start”) and stops when the SDA line changes from "L" to "H" levels during the period of SCL="H" (“stoP”). These conditions are generated by the master device. In addition, the SCL signal is also generated by the master device.
Each byte to be output to the SDA line by the master device is in 8 bits unit and transmitted sequentially from the MSB to the LSB. After 8-bit data is transmitted, the master device generates an acknowledge clock and releases the SDA line. This IC performs to change the SDA line to "L" level at the falling edge of the 8th bit clock for one clock period and returns an acknowledge signal ("Ack") (*2). The master device detects the SDA line’s status at the rising edge of the 9th bit clock, and receives the “Ack”. The communication is performed by a 9 bits unit consisted of 8bits data and “Ack”.

**2: The SDA line of this IC separates into the input pin SDAIN and the acknowledge output pin SDAACK. In case of the master device detects the voltage level of the SDA line in acknowledge cycle, both of the SDAIN pin and the SDAACK pin must be connected to the SDA line. Otherwise, the output pin SDAACK must be left open.*

The first byte to be transmitted from the master device is comprised of the 7 bits slave address and the 8th bit that is tied to "L" level. When this address number is identical with this IC’s address, the "Ack" signal is generated and the communication can be enabled. The second and the following bytes can be transmitted the control byte followed by commands, parameters and display data. The transmitted data is discriminated either data, command, command parameter or display data by the control byte. However, writing to the display data RAM must be executed after completion of all condition settings. All following data subsequent to the control byte indicating display data writes to the display data RAM as the display data. In order to receive another command again, current communication must be completed once and restarted it from the beginning.



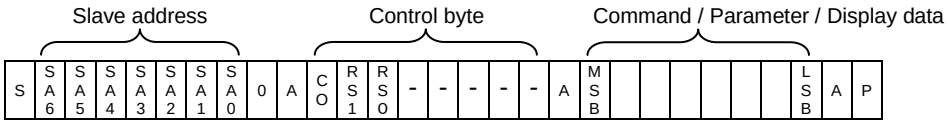
- *("HZ") indicates the releasing the SDA line by the master device or this IC.*
- *The SDA line must be connected to VDD with parallel resistance.*

Figure 6.4 2-wire Serial Interface

Table 6.3 Data Discrimination by Control Byte

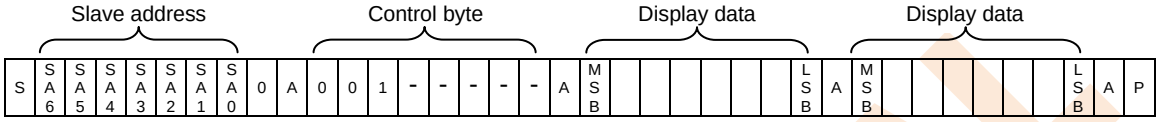
CO	RS1	RS0	Description
0			Last Control Byte
1			Control Bytes Continue
	0	0	Command
	1	0	Parameter of Command
(*3)	0	1	Display Data

**3: Since writing to the display data RAM must be executed after completion of all condition settings, the CO bit of the control byte for the display data becomes "0".*

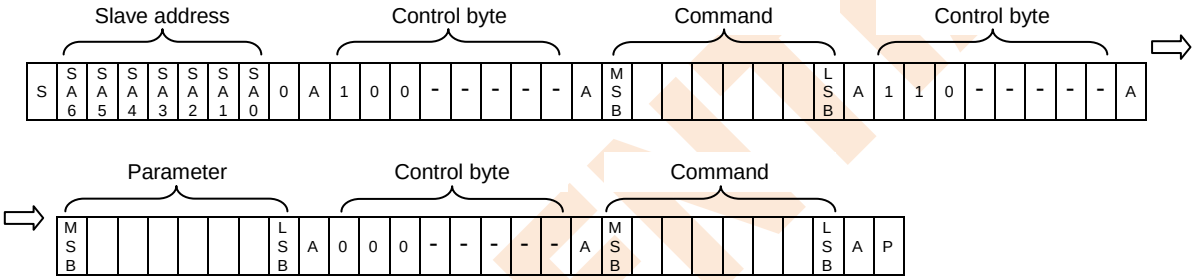


*: "-" in control panel must be tied to "H" or "L" level.

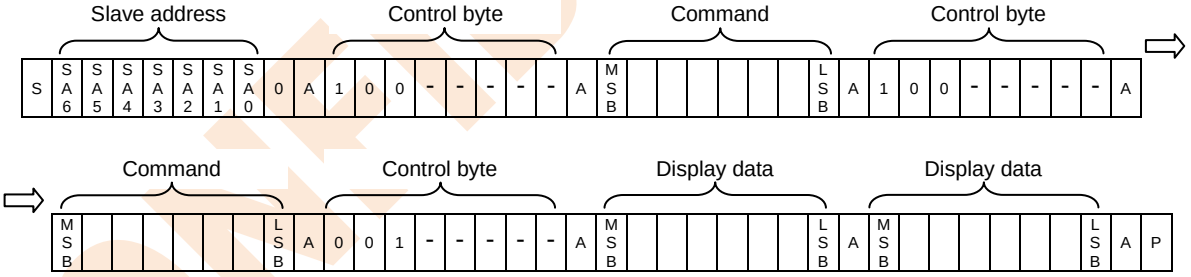
(1) Format



(2) Example of 2 bytes display data transmitting



(3) Example of 2 commands (command with parameter and without parameter) transmitting



(4) Example of 2 commands (command without parameter) and 2 bytes display data transmitting

Figure 6.5 Example of 2-wire Serial Interface Protocol

6.1.4 Chip Select

For the 4-wire serial interface (IFS="L"), an active/inactive state of this IC is controlled by the XCS pin.

Table 6.3 Control of Pin XCS

XCS	Description of Control
"L"	This IC becomes active state, and accepts access from the MPU.
"H"	This IC becomes inactive state, and unable to accept access from the MPU. In this case, this IC becomes the following states. ● Pins SDI and SDO become High-impedance state. ● Inputs from pins A0 and SCL are disabled. ● Counter of the serial interface is reset.

For the 2-wire serial interface (IFS="H"), a chip select is complied with I2C-Bus. The XCS pin is disabled.

6.2 Command Decoder

When an input serial data is a command, the command decoder decodes the input data and this IC is controlled by this command.

6.3 Display Data RAM

6.3.1 Display Data and LCD

The display data RAM, which stores the on-state data/off-state data of the display segment, is comprised of 8 x 120 bits. It can be stored the display data to the desired bit by specifying the page address and the column address.
There is a one-to-one correspondence between the bit in the display data RAM and the pixel in the LCD segment. The bit data “1” in the display data RAM indicates the on-state and the bit data “0” indicates the off-state.

Bit Data
“1”: On-state Black (Normally white in Normal display mode)
“0”: Off-state White (Normally white in Normal display mode)

Figure 6.6 indicates an example of correspondence between the display data RAM and LCD.
The writing display data to the display data RAM from MPU is controlled independently of the display data output to the LCD drive circuit. Therefore, this allows the MPU can access to the display data RAM asynchronous with the display timing signals.

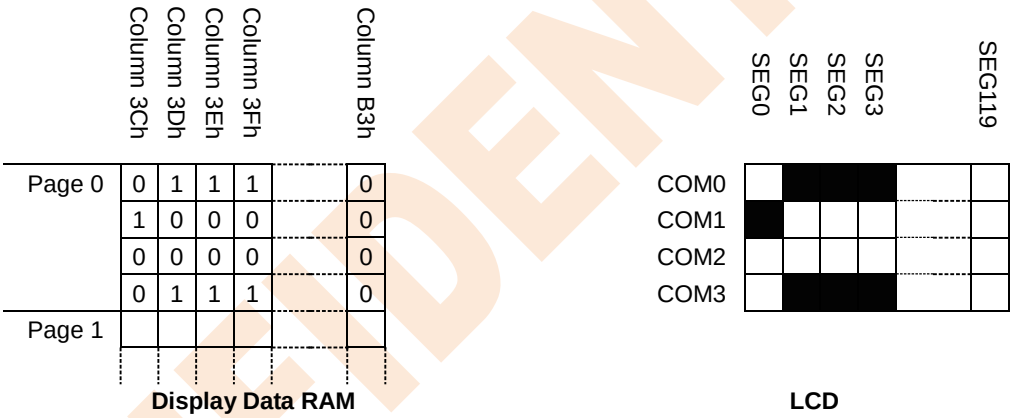


Figure 6.6 Example of 1/4 Duty

6.3.2 Memory Map of Display Data RAM

The display data is stored in order of D7 (MSB) to D0 (LSB) by 1 byte (=8 bits) unit as shown in the following table.

Table 6.5 Display Data Input

Bit / Byte	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
1	aa7	aa6	aa5	aa4	aa3	aa2	aa1	aa0
2	ab7	ab6	ab5	ab4	ab3	ab2	ab1	ab0
3	ac7	ac6	ac5	ac4	ac3	ac2	ac1	ac0
:	:	:	:	:	:	:	:	:

The examples of memory mapping between input data and the display data RAM are as shown in Figure 6.7 to Figure 6.14.

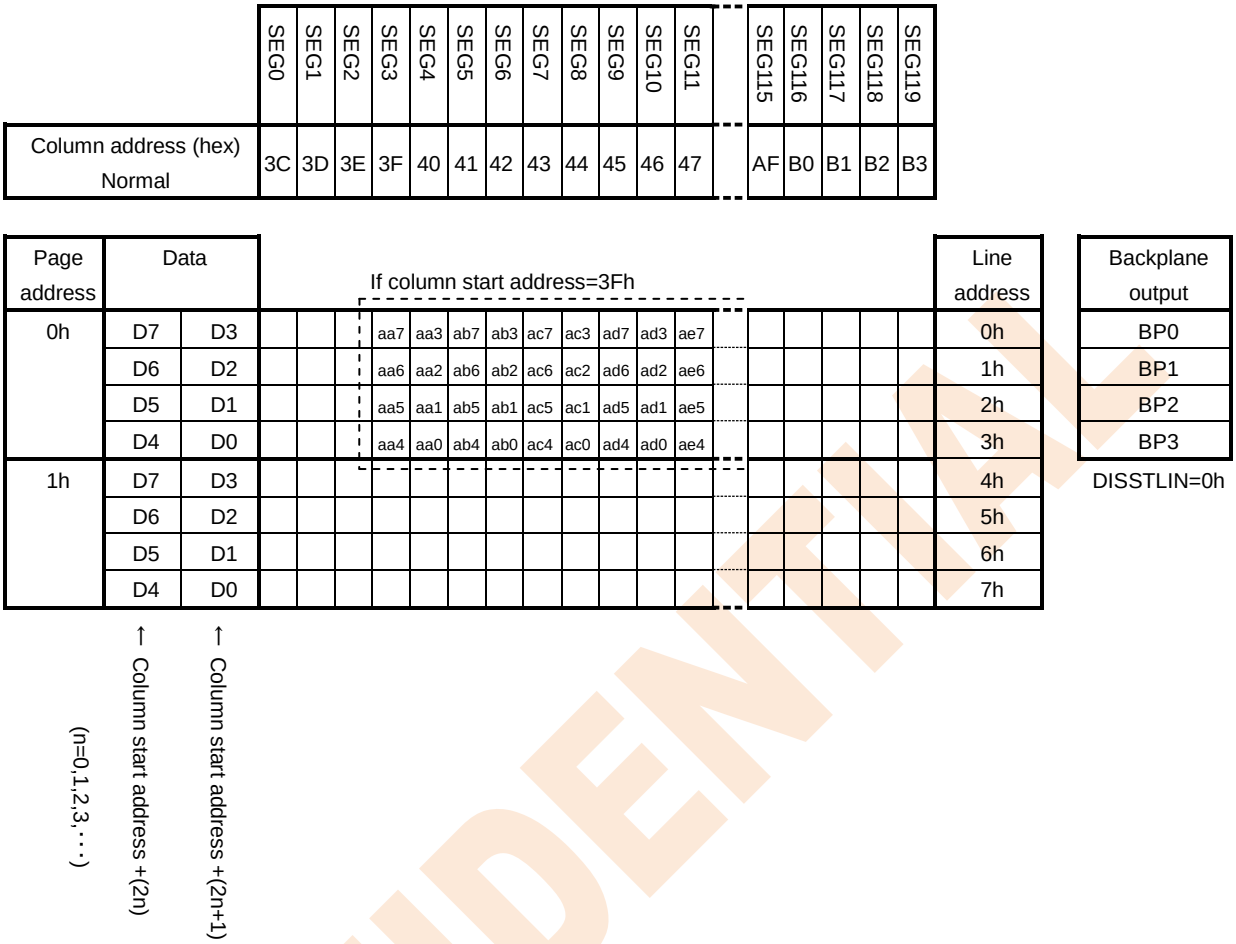


Figure 6.7 Example of 4-line Display with Normal Column Address Direction

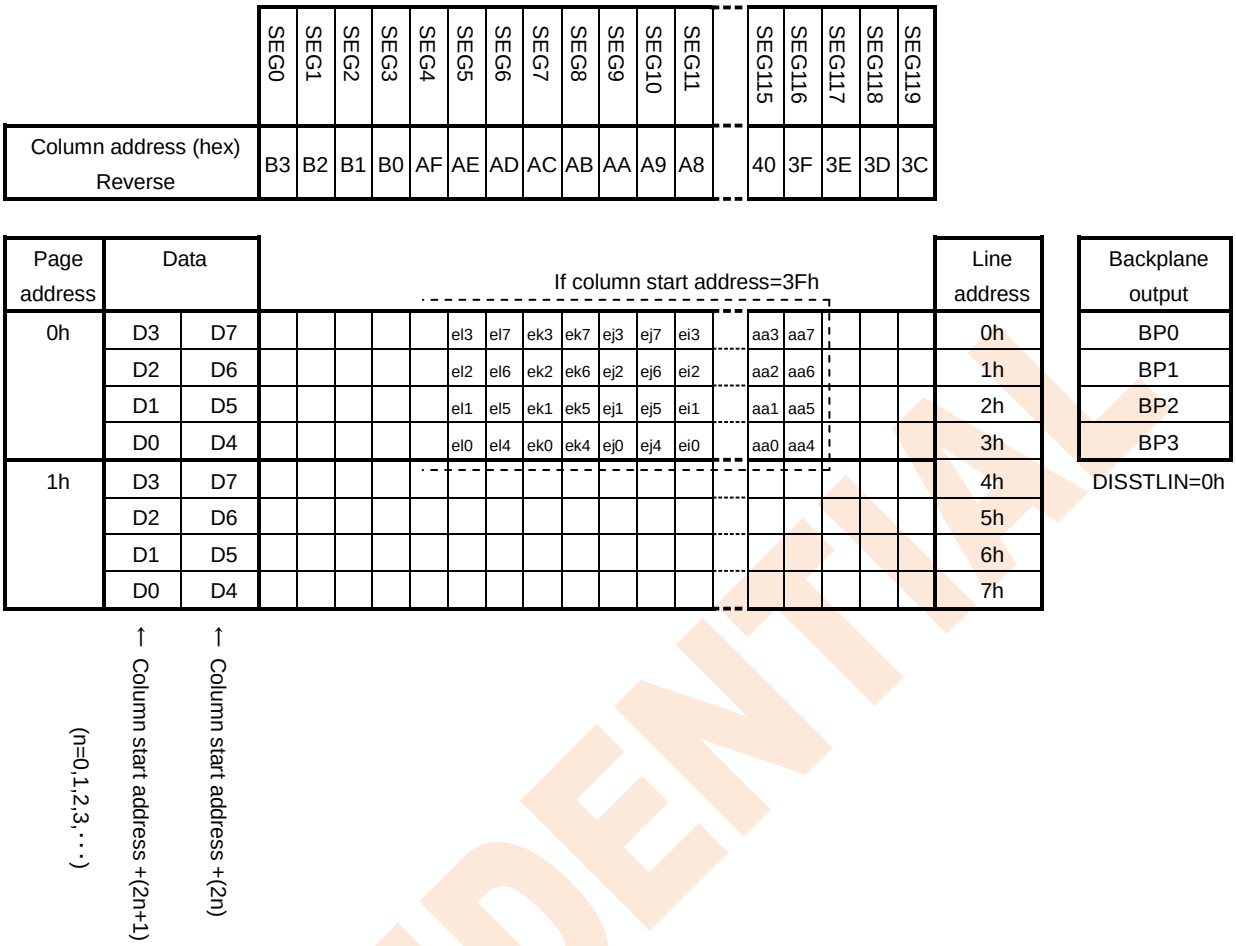


Figure 6.8 Example of 4-line Display with Reverse Column Address Direction

	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11		SEG115	SEG116	SEG117	SEG118	SEG119
Column address (hex) Normal	3C	3D	3E	3F	40	41	42	43	44	45	46	47		AF	B0	B1	B2	B3

Page address	Data		If column start address=3Fh																Line address	Backplane output
0h	D7	D4				aa7	aa4	ab7	ab4	ac7	ac4	ad7	ad4	ae7						0h	BP0
	D6	D3				aa6	aa3	ab6	ab3	ac6	ac3	ad6	ad3	ae6						1h	BP1
	D5	D2				aa5	aa2	ab5	ab2	ac5	ac2	ad5	ad2	ae5						2h	BP2
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3h	DISSTLIN=0h
1h	D7	D4																		4h	
	D6	D3																		5h	
	D5	D2																		6h	
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	7h	

↑ Column start address +(2n)

↑ Column start address +(2n+1)

(n=0,1,2,3,・・・)

Figure 6.9 Example of 3-line Display with Normal Column Address Direction

	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11		SEG115	SEG116	SEG117	SEG118	SEG119
Column address (hex) Reverse	B3	B2	B1	B0	AF	AE	AD	AC	AB	AA	A9	A8		40	3F	3E	3D	3C

Page address	Data		If column start address=3Fh																Line address	Backplane output
0h	D4	D7					el4	el7	ek4	ek7	ej4	ej7	ei4		aa4	aa7				0h	BP0
	D3	D6					el3	el6	ek3	ek6	ej3	ej6	ei3		aa3	aa6				1h	BP1
	D2	D5					el2	el5	ek2	ek5	ej2	ej5	ei2		aa2	aa5				2h	BP2
	-	-	-	-	-	-	-	-	-	-	-	-	-		-	-	-	-	-	3h	DISSTLIN=0h
1h	D4	D7																		4h	
	D3	D6																		5h	
	D2	D5																		6h	
	-	-	-	-	-	-	-	-	-	-	-	-	-		-	-	-	-	-	7h	

↑ Column start address +(2n+1)

↑ Column start address +(2n)

(n=0,1,2,3,・・・)

Figure 6.10 Example of 3-line Display with Reverse Column Address Direction

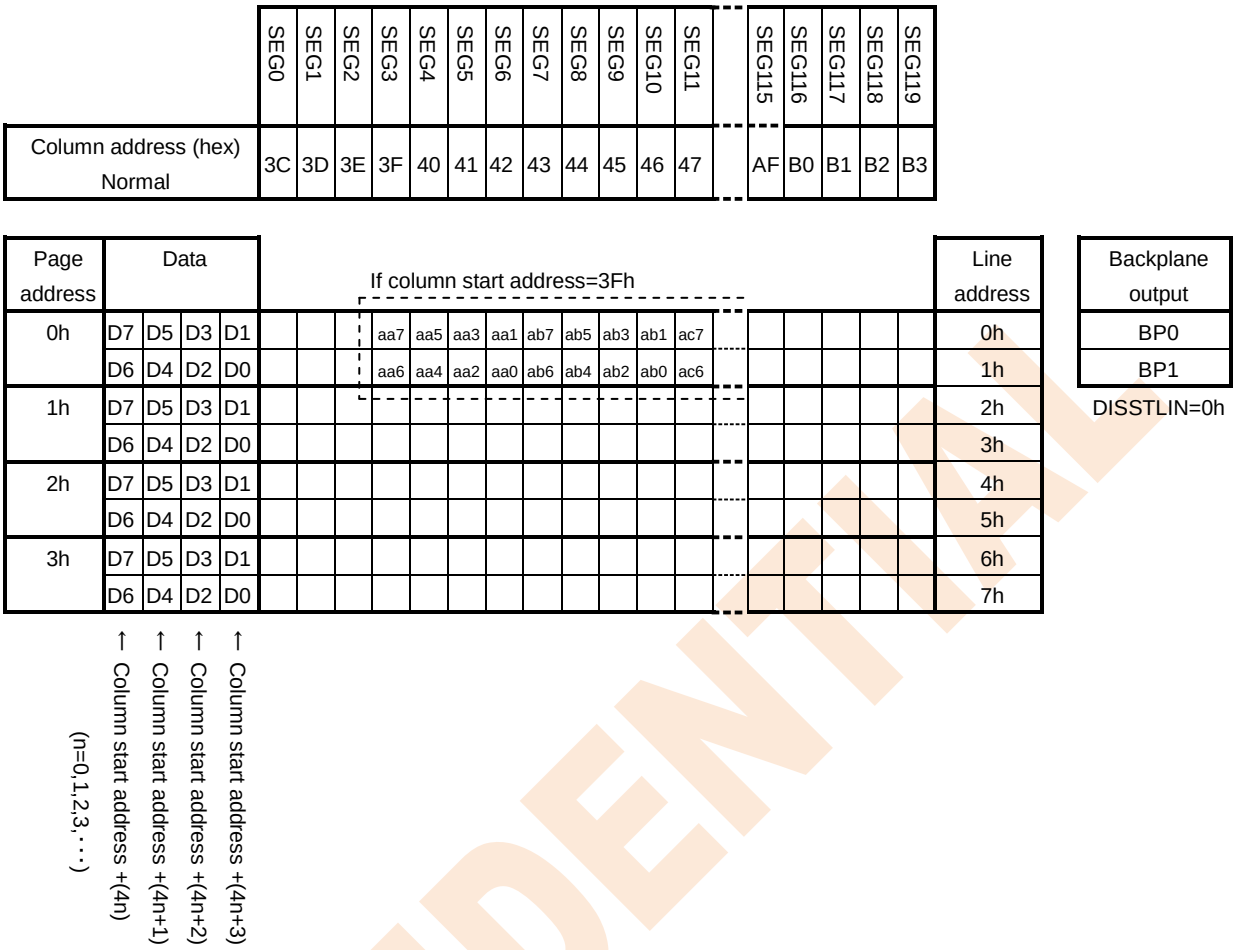


Figure 6.11 Example of 2-line Display with Normal Column Address Direction

	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11		SEG115	SEG116	SEG117	SEG118	SEG119
Column address (hex) Reverse	B3	B2	B1	B0	AF	AE	AD	AC	AB	AA	A9	A8		40	3F	3E	3D	3C

Page address	Data																		Line address
														If column start address=3Fh					
0h	D1	D3	D5	D7						cf1	cf3	cf5	cf7	ce1	ce3	ce5		aa5	aa7				0h
	D0	D2	D4	D6						cf0	cf2	cf4	cf6	ce0	ce2	ce4		aa4	aa6				1h
1h	D1	D3	D5	D7																			2h
	D0	D2	D4	D6																			3h
2h	D1	D3	D5	D7																			4h
	D0	D2	D4	D6																			5h
3h	D1	D3	D5	D7																			6h
	D0	D2	D4	D6																			7h

Backplane output
BP0
BP1

DISSTLIN=0h

↑ Column start address +(4n+3)
↑ Column start address +(4n+2)
↑ Column start address +(4n+1)
↑ Column start address +(4n)
(n=0,1,2,3,・・・)

Figure 6.12 Example of 2-line Display with Reverse Column Address Direction

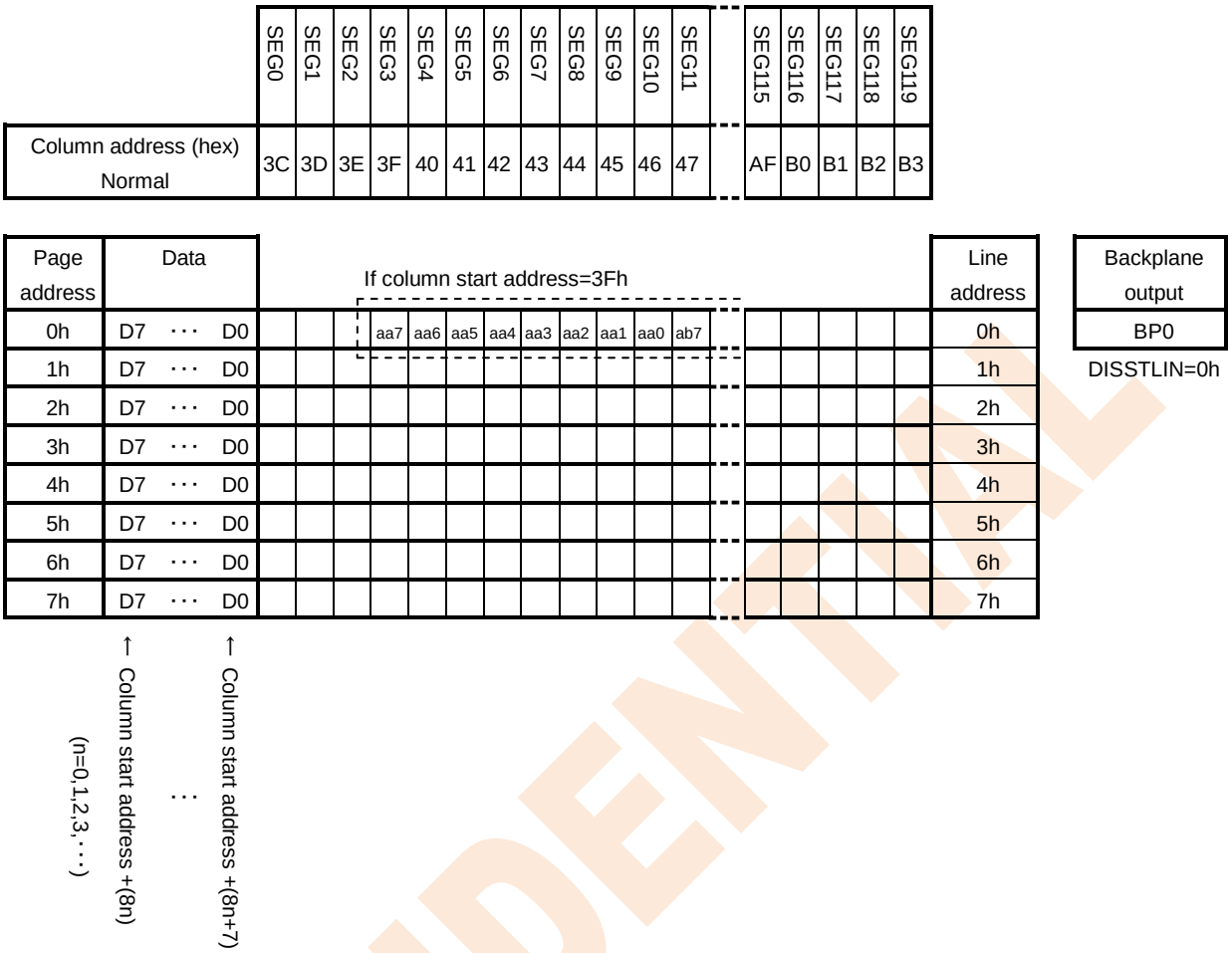


Figure 6.13 Example of 1-line Display (Static Drive) with Normal Column Address Direction

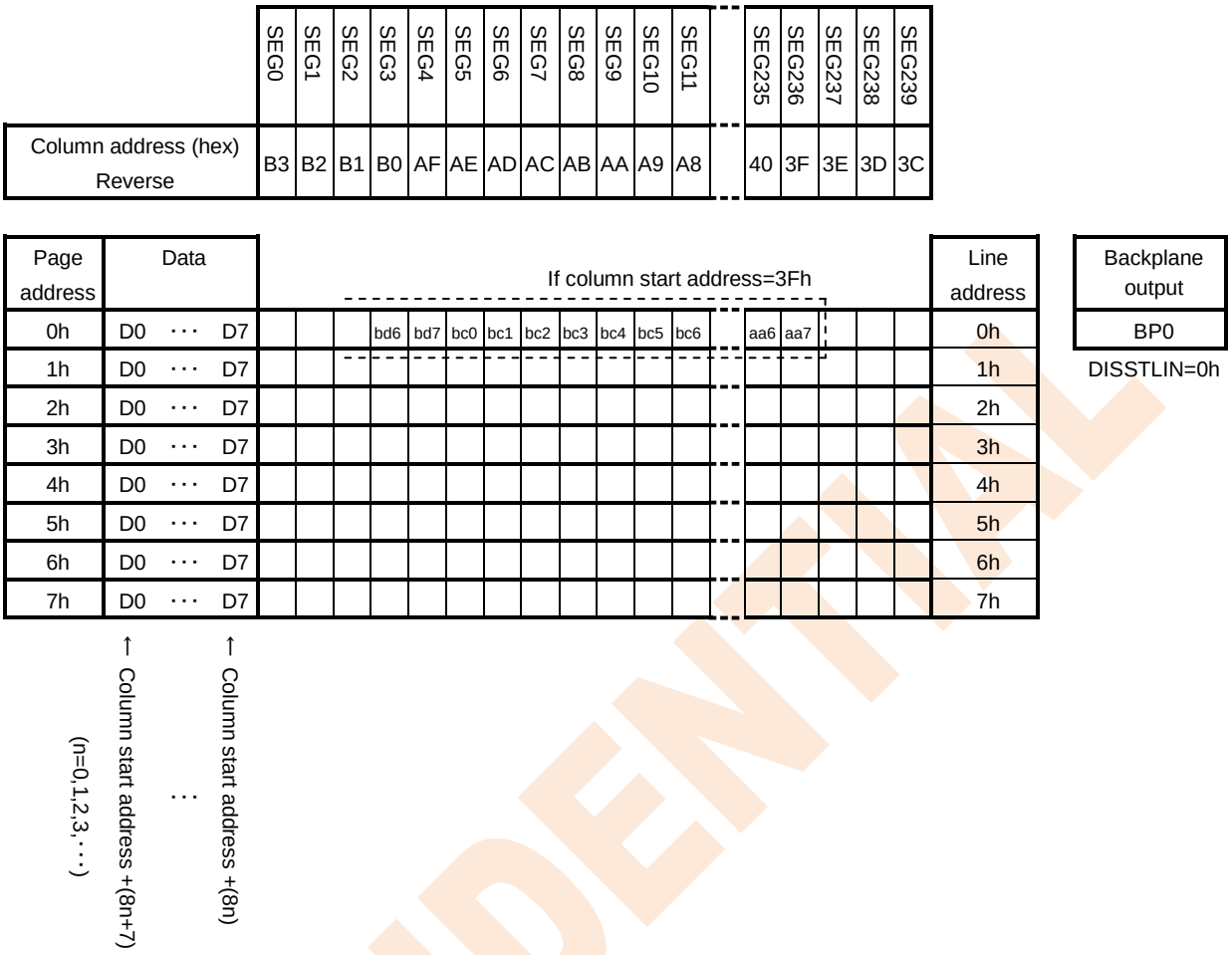


Figure 6.14 Example of 1-line Display (Static Drive) with Reverse Column Address Direction

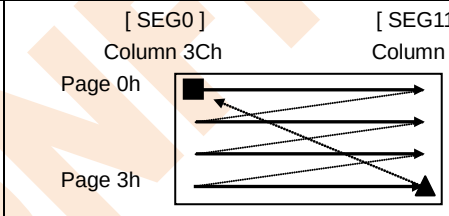
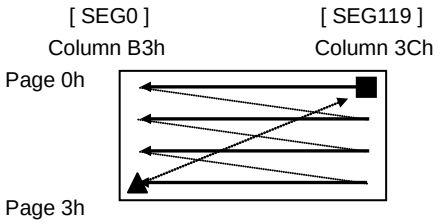
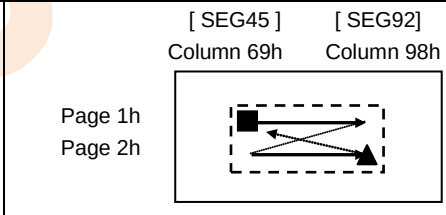
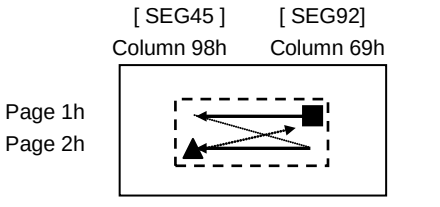
6.3.3 Page Address Circuit / Column Address Circuit

The commands PASET and CASET specify the writing area of the display data RAM defined by the page addresses and the column addresses as shown in the table below.
The writing data to the display data RAM starts from both column and page start addresses. After completion of the writing data to one column, the column address is automatically incremented by +1. Then, after reached the writing data to the column end address, the column address returns to the start address and the page address is automatically incremented by +1. Subsequently, after reached the writing data to both column and page end addresses, both column and page addresses return to the start addresses. In addition, if the writing data completed prior to reaching both column and page end addresses, next writing operation starts from both column and page start addresses.
In addition, the column start address and the column end address must be kept the following restrictions by the number of display line because the display data is input by 1 byte (8 bits) unit.

4-line Display: 60(3Ch) ≦ column start address ≦ 178(B2h),
column end address = column start address+1+2n ≦ 179(B3h)
3-line Display: 60(3Ch) ≦ column start address ≦ 178(B2h),
column end address = column start address+1+2n ≦ 179(B3h)
2-line Display: 60(3Ch) ≦ column start address ≦ 176(B0h),
column end address = column start address+3+4n ≦ 179(B3h)
1-line Display: 60(3Ch) ≦ column start address ≦ 172(ACh),
column end address = column start address+7+8n ≦ 179(B3h)
(n=0,1,2,3,・・・)

The CANOR/CARVS commands can select normal/reverse setting of the column address.
Table 6.5 indicates the writing area and the address direction according to the above command settings in where ■ indicates the start address, and ▲ indicates the end address.

Table 6.5 Writing Area and Address Direction (In case of 1/2 Duty)

Writing Area \ Column Address	Normal	Reverse
Whole Area		
Specified Area		

6.3.4 Line Address Circuit

The line address circuit coordinates between a line address and a back plane output when the contents of the display data RAM displays to the LCD.
The DISSTLIN command defines the display start line address corresponding to the BP0. The display area is defined as the number of lines specified by the DISLINSET command from the display start line address toward the incremental address direction.
By changing the display start line address using the DISSTLIN command, the page displayed to the LCD can be switched.

6.3.5 Display Data Latch Circuit

The display data latch circuit is a latch for temporarily storing the display data that is output to the LCD drive circuit from the display data RAM.
The display mode setting of normal display/inverted display/all ON display/all OFF display using the DISSET command controls this latch data. Therefore, this makes data inside the display data RAM remain unchanged.

6.4 Oscillation Circuit

The oscillation circuit is a CR-type oscillator with featured Typ. 4MHz (TBD) oscillation frequency (fOSC) and generates the signals for the display clock, the boosting clock and the built-in timer for enabling/disabling of the power supply for LCD drive. It can be enabled when generating the display clock from the built-in oscillation circuit (CLS="H") while the master operation (M/S="H") or enabling the power supply for LCD drive (Parameter P13=1 or P10=1 of the PWRCTL command) while the master operation (M/S="H").
This oscillation circuit disables operation under initial state (OSCOFF state) and enables operation by executing the OSCON command.

Table 6.6 Enable/Disable Built-in Oscillation Circuit

M/S	CLS (Display Clock Source)	Power Supply Circuit for LCD Drive (Parameter setting of PWRCTL command)	Built-in Oscillation Circuit (OSCON, OSCOFF command)
"H"	"H" (Built-in Oscillation Circuit)	Used (P13=1 or P10=1)	Enable
		Not used (P13=P10=0)	
	"L" (External Input)	Used (P13=1 or P10=1)	
		Not used (P13=P10=0)	Disable (Fixed to OSCOFFstate)
"L"	"H" or "L" (External Input)	Not used (Invalid PWRCTL command when M/S="L")	

When the master operation mode (M/S="H") and CLS="H", the display clock is output to the CL pin. The display clock frequency (fCL) is selected from 30 types by the FCLSEL command as shown in Table 6.8. When the slave operation mode (M/S="L") or CLS="L", the display clock is input externally from the CL pin.
The boosting clock frequency (fBST) is selected from 8 types by the FBSTSEL command as shown in Table 6.7. The higher frequency makes higher drivability of power supply for LCD drive, accordingly the current consumption also increases. The boosting clock frequency must be determined by evaluating various display patterns.

Table 6.7 Boosting Clock Frequency

FBSTSEL Parameter			Boosting Clock Frequency (kHz)
P12	P11	P10	
0	0	0	15.625
0	0	1	31.25
0	1	0	62.5
0	1	1	125
1	0	0	250
1	0	1	500
1	1	0	1000
1	1	1	2000

6.5 Display Timing Generating Circuit

The display timing generating circuit generates necessary timing signals required for the display based on the display clock (fCL) when the master operation mode (M/S="H"). The generating timing signals are as follows,

- Start signal of display frame: SYNC
- AC signal: FR
- Blanking control signal of LCD display: XDOF

When using the built-in oscillation circuit, the display clock frequency (fCL) and the frame frequency (fSYNC) are defined by the FCLSEL, DISLINSET and NLSET (+1H Dummy ON/OFF) commands as shown in Table 6.8.

Table 6.8 Display Clock Frequency (fCL) and Frame Frequency (fSYNC) in case of using Built-in Oscillation Circuit

FCLSEL Parameter	fCL (kHz)	fSYNC (Hz)				
		4-line +1H (1/5 Duty)	4-line (1/4 Duty)	3-line (1/3 Duty)	2-line (1/2 Duty)	1-line (Static Drive =1/1 Duty)
00000	6.410	49.3	50.1	50.9	50.1	50.1
00001	7.042	54.2	55.0	55.9	55.0	55.0
00010	7.692	59.2	60.1	61.0	60.1	60.1
00011	8.333	64.1	65.1	66.1	65.1	65.1
00100	8.929	68.7	69.8	70.9	69.8	69.8
00101	9.615	74.0	75.1	76.3	75.1	75.1
00110	10.204	78.5	79.7	81.0	79.7	79.7
00111	10.870	83.6	84.9	86.3	84.9	84.9
01000	11.628	89.4	90.8	92.3	90.8	90.8
01001	12.195	93.8	95.3	96.8	95.3	95.3
01010	12.821	98.6	100	102	100	100
01011	14.085	108	110	112	110	110
01100	15.385	118	120	122	120	120
01101	16.667	128	130	132	130	130
01110	17.857	137	140	142	140	140
01111	19.231	148	150	153	150	150
10000	20.408	157	159	162	159	159
10001	21.739	167	170	173	170	170
10010	23.256	179	182	185	182	182
10011	24.390	188	191	194	191	191
10100	25.641	197	200	203.5	200	200
10101	28.169	217	220	224	220	220
10110	30.769	237	240	244	240	240
10111	33.333	256	260	265	260	260
11000	35.714	275	279	283	279	279
11001	38.462	296	300	305	300	300
11010	40.816	314	319	324	319	319
11011	43.478	334	340	345	340	340
11100	46.512	358	363	369	363	363
11101	48.780	375	381	387	381	381

In addition, when supplying the display clock externally, the display clock frequency (fCL) and the frame frequency (fSYNC) are defined by the DISLINSET and NLSET (+1H Dummy ON/OFF) commands as shown in Table 6.9.

Table 6.9 Display Clock Frequency (fCL) and Frame Frequency (fSYNC) in case of supplying Display Clock Externally

DISLINSET, NLSET (+1H Dummy ON/OFF)		fSYNC
4-line +1H	(1/5 Duty)	fCL/130
4-line	(1/4 Duty)	fCL/128
3-line	(1/3 Duty)	fCL/126
2-line	(1/2 Duty)	fCL/128
1-line (Static Drive)	(1/1 Duty)	fCL/128

The AC signal FR is controlled by the NLSET command. The display quality caused by crosstalk issues for example may be able to improve by changing this NLSET command setting. The drive waveform A or B can be selected by this NLSET command. In addition, the settings of the n-line inversion ON/OFF, the number of inversion line n and the +1H dummy ON/OFF can be set when using the drive waveform B. These settings must be determined by evaluating actual LCD display.
In addition, the 1-line display (Static drive=1/1 Duty) is only applicable for the drive waveform B and the n-line inversion function is disabled (OFF).
Waveform examples of the SYNC, FR, SEG and COM signals are as shown in Figure 6.15 to Figure 6.18.

The LCD blanking signal XDOF becomes “L” level during the period of (TBD) frames after invoking the PWRON command when using the power supply for LCD drive while Display OFF mode 1 and the power save ON mode. In this case, the outputs of SEG and COM are VSS level.

When cascading multiple of these ICs as a master/slave connection, the SYNC, FR and XDOF signals generated by the master chip must be supplied to the slave chip..

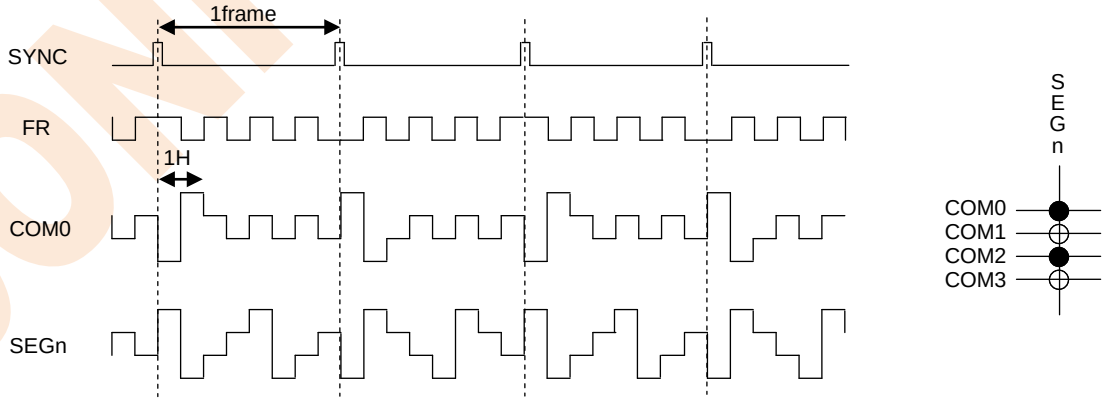


Figure 6.15 Example Waveform of 4-line Display (1/4 Duty) with Drive Waveform A

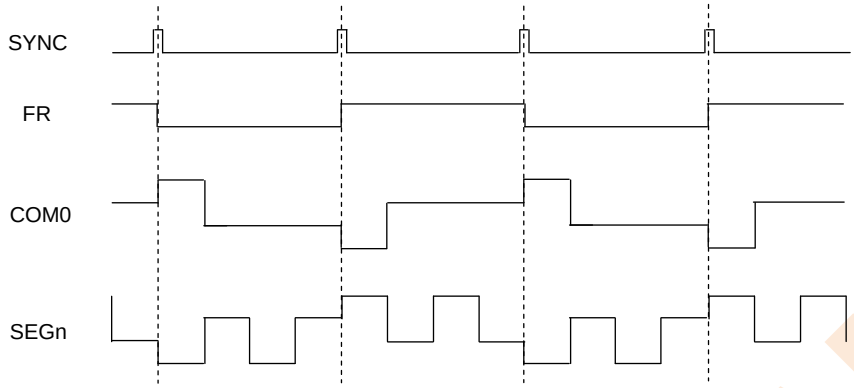


Figure 6.16 Example Waveform of 4-line Display (1/4 Duty) with Drive Waveform B

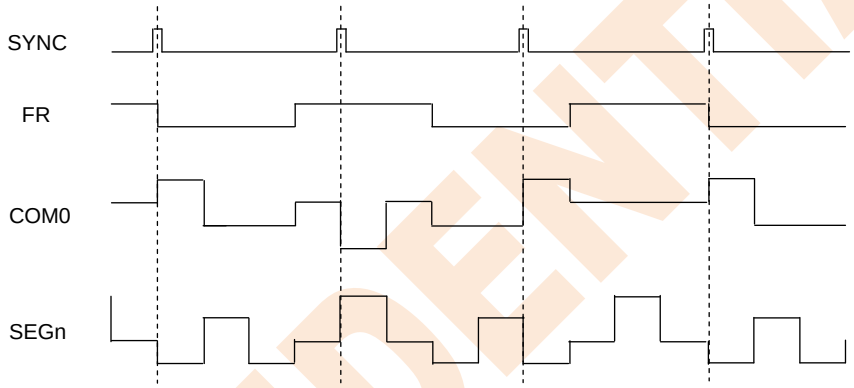


Figure 6.17 Example Waveform of 4-line Display (1/4 Duty), 3-line inversion with Drive Waveform B

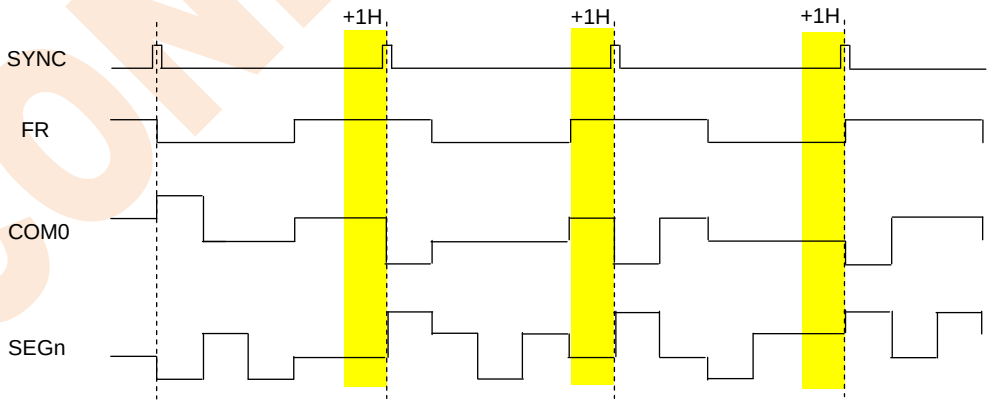


Figure 6.18 Example Waveform of 4-line Display (1/5 Duty by adding +1H), 3-line inversion with Drive Waveform B

6.6 LCD Drive Circuit

6.6.1 Segment Driver

The segment driver is an output circuit for the segment drive. The driver selects one of output voltage level from VLCD, V2, V3 and VSS by the condition of the contents of display data RAM and the FR signal.
The driver outputs VSS level when Display OFF mode1 (DISOFF1, Initial state) or power saving mode (PSON).
The driver outputs off-state level ("0" level of RAM data in case of normal display mode or "1" level of RAM data in case of inverted display mode) when Display OFF mode2 (DISOFF2).

Table 6.10 Output Voltage of SEG

RAM Data	FR	Output Voltage	
		Normal Display	Inverted Display
"1"	"H"	VLCD	V2
	"L"	VSS	V3
"0"	"H"	V2	VLCD
	"L"	V3	VSS
Display OFF1/Power Save	–	VSS	VSS
Display OFF2	"H"	V2	V2
	"L"	V3	V3

6.6.2 Common Driver

The common driver is an output circuit for the common drive. The driver selects one of output voltage level from VLCD, V1, V4 and VSS by the condition of the scan signal and the FR signal.
The driver outputs VSS level when Display OFF mode1 (DISOFF1, Initial state) or power saving mode (PSON).
The driver outputs non-selected level when Display OFF mode2 (DISOFF2).

Table 6.11 Output Voltage of COM

Scan Signal	FR	Output Voltage
Selected	"H"	VSS
	"L"	VLCD
Non-selected	"H"	V1
	"L"	V4
Display OFF1/Power Save	–	VSS
Display OFF2	"H"	V1
	"L"	V4

6.6.3 Setting of Common Output State

The correspondence between the backplane output and the COM output of the display data RAM are defined by the COMNOR/COMRVS command as shown in Table 6.12. This makes to minimize the placement restrictions of this IC when assembling the LCD module.

Table 6.12 Relation between Backplane Output and COM Output of Display Data RAM

COM Output	4-line Display		3-line Display		2-line Display		1-line Display
	COMNOR	COMREV	COMNOR	COMREV	COMNOR	COMREV	—
COM0	BP0	BP3	BP0	BP2	BP0	BP1	BP0
COM1	BP1	BP2	BP1	BP1	BP1	BP0	BP0
COM2	BP2	BP1	BP2	BP0	BP0	BP1	BP0
COM3	BP3	BP0	—	—	BP1	BP0	BP0

6.6.4 Examples of Drive Waveform

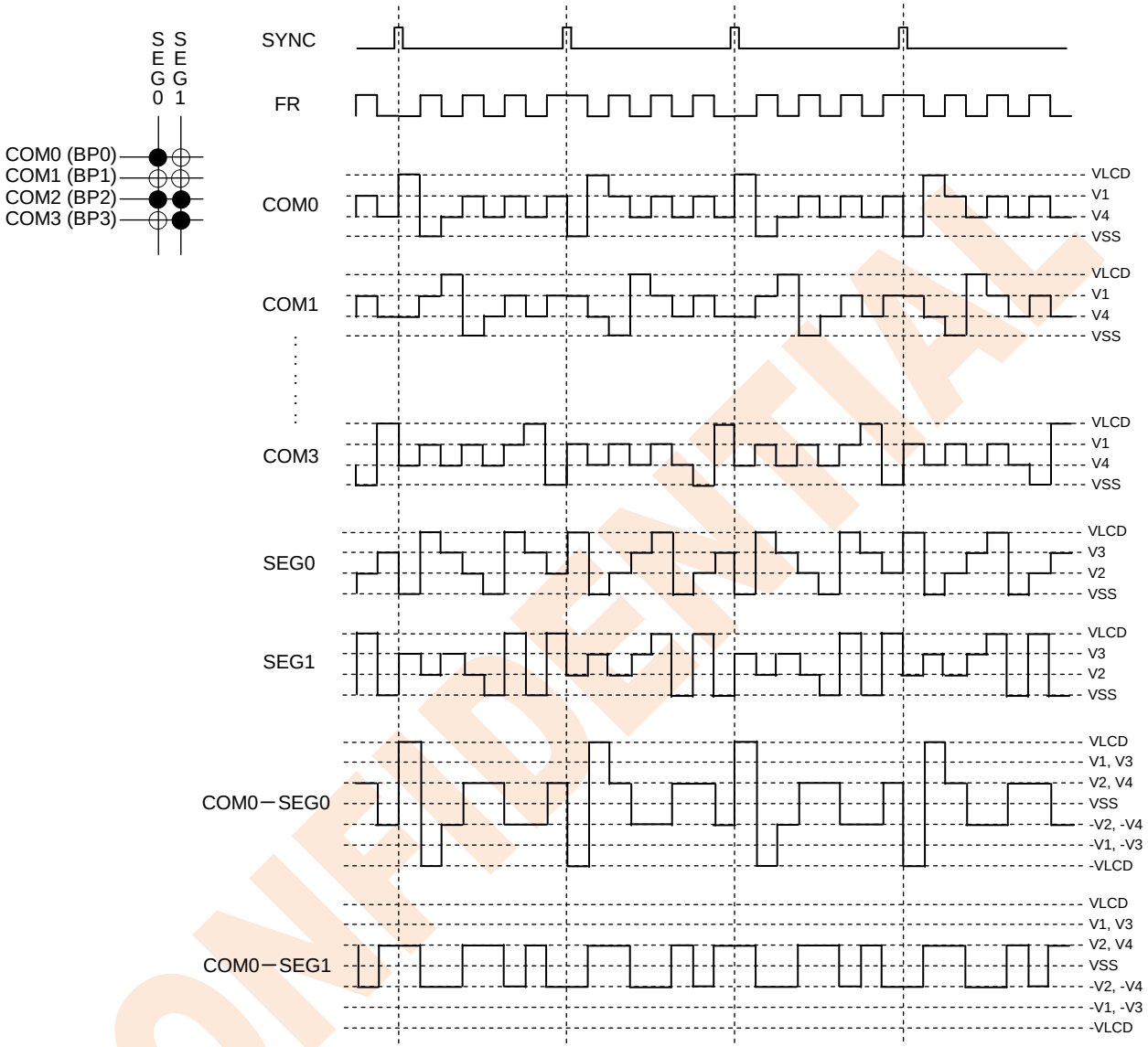


Figure 6.19 Drive Waveform A, 4-line Display (1/4 Duty) and 1/3 Bias

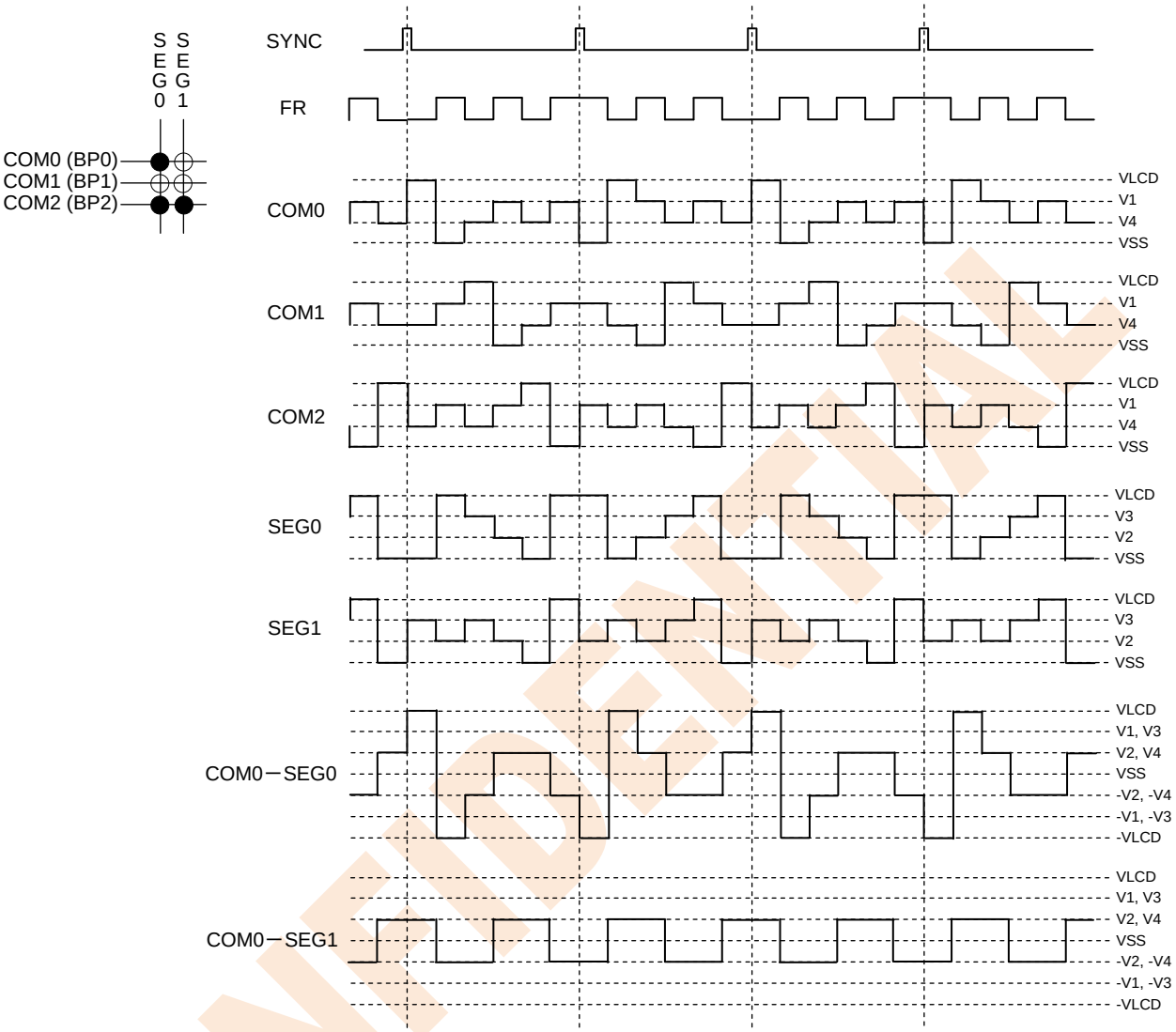


Figure 6.20 Drive Waveform A, 3-line Display (1/3 Duty) and 1/3 Bias

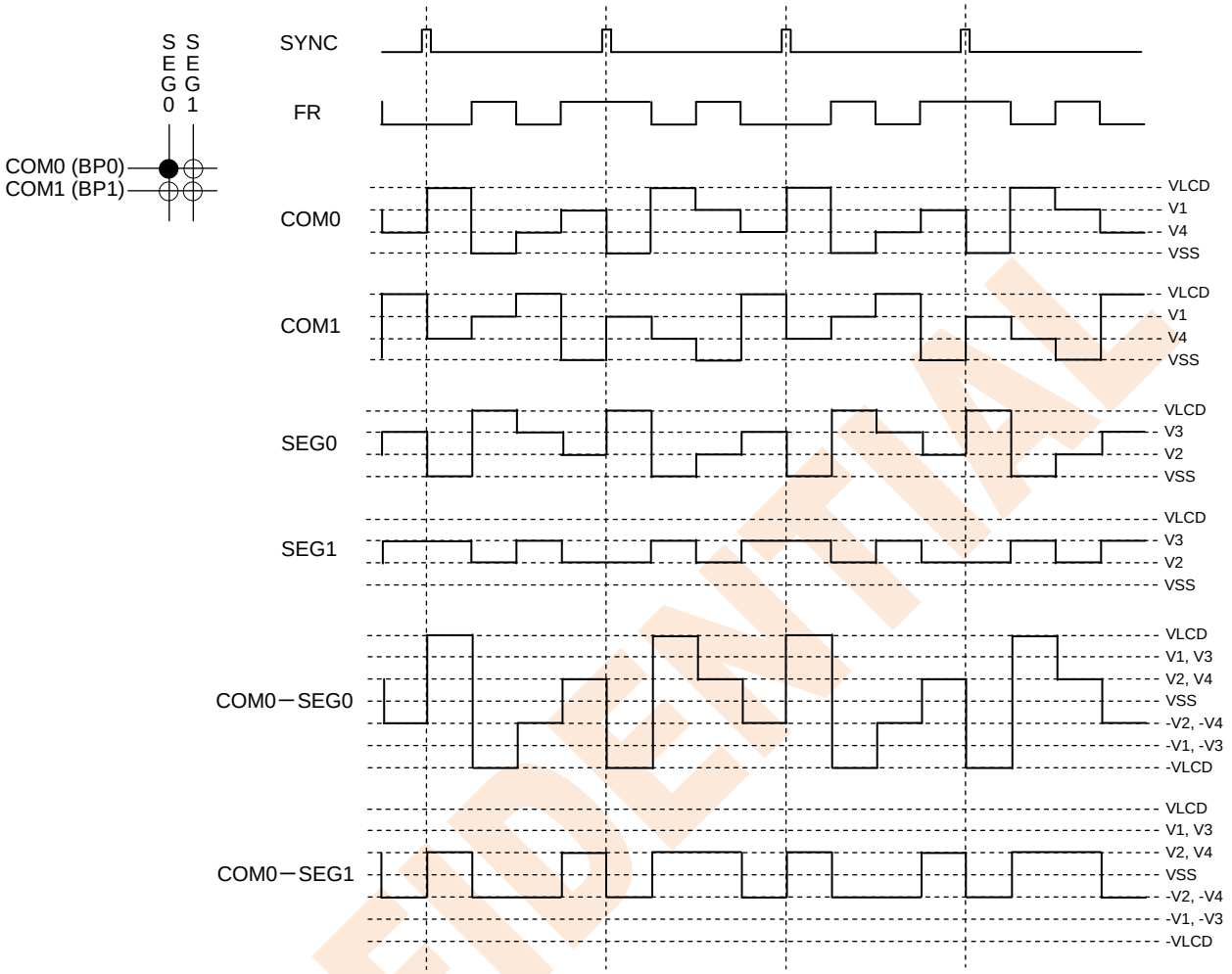


Figure 6.21 Drive Waveform A, 2-line Display (1/2 Duty) and 1/3 Bias

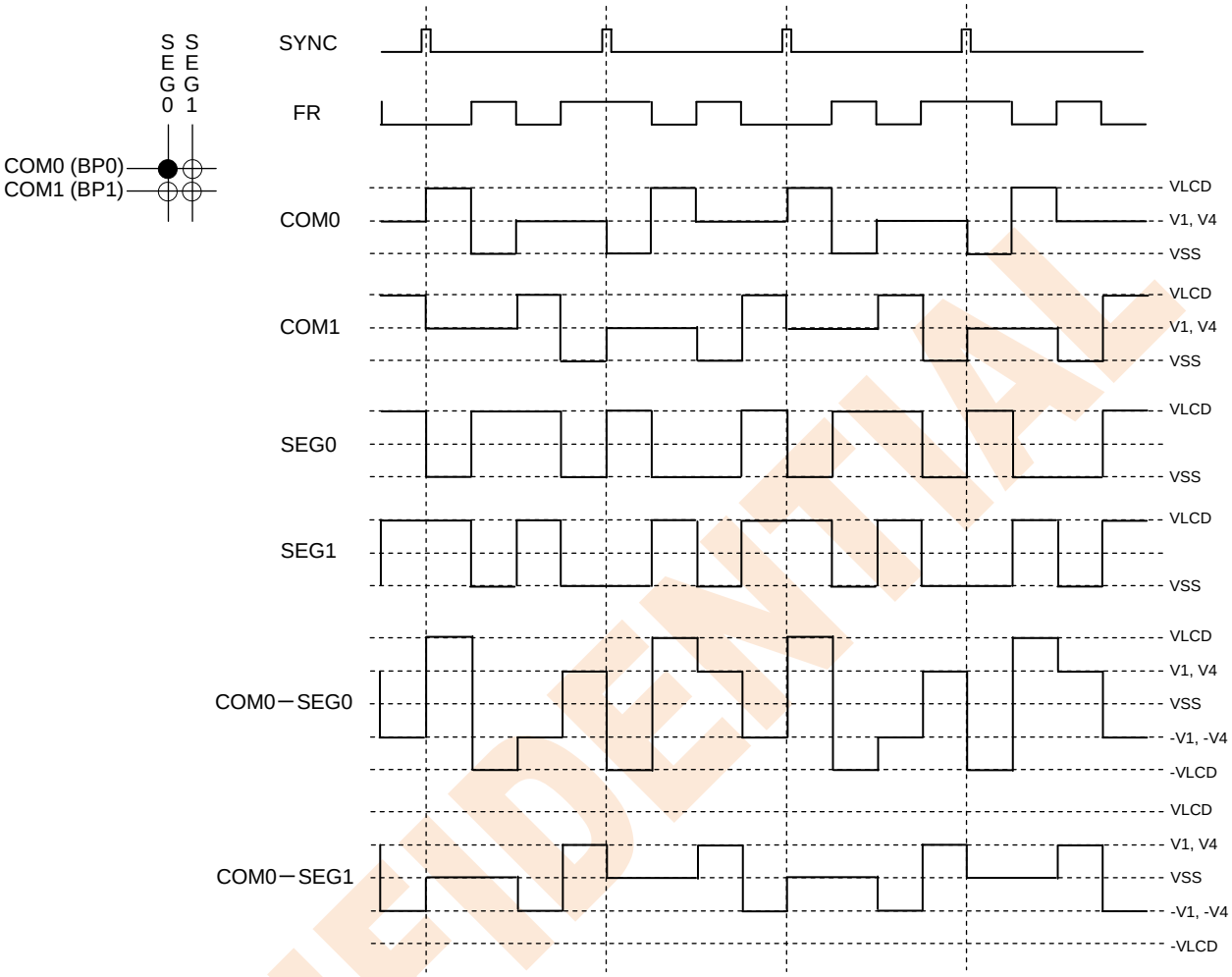


Figure 6.22 Drive Waveform A, 2-line Display (1/2 Duty) and 1/2 Bias

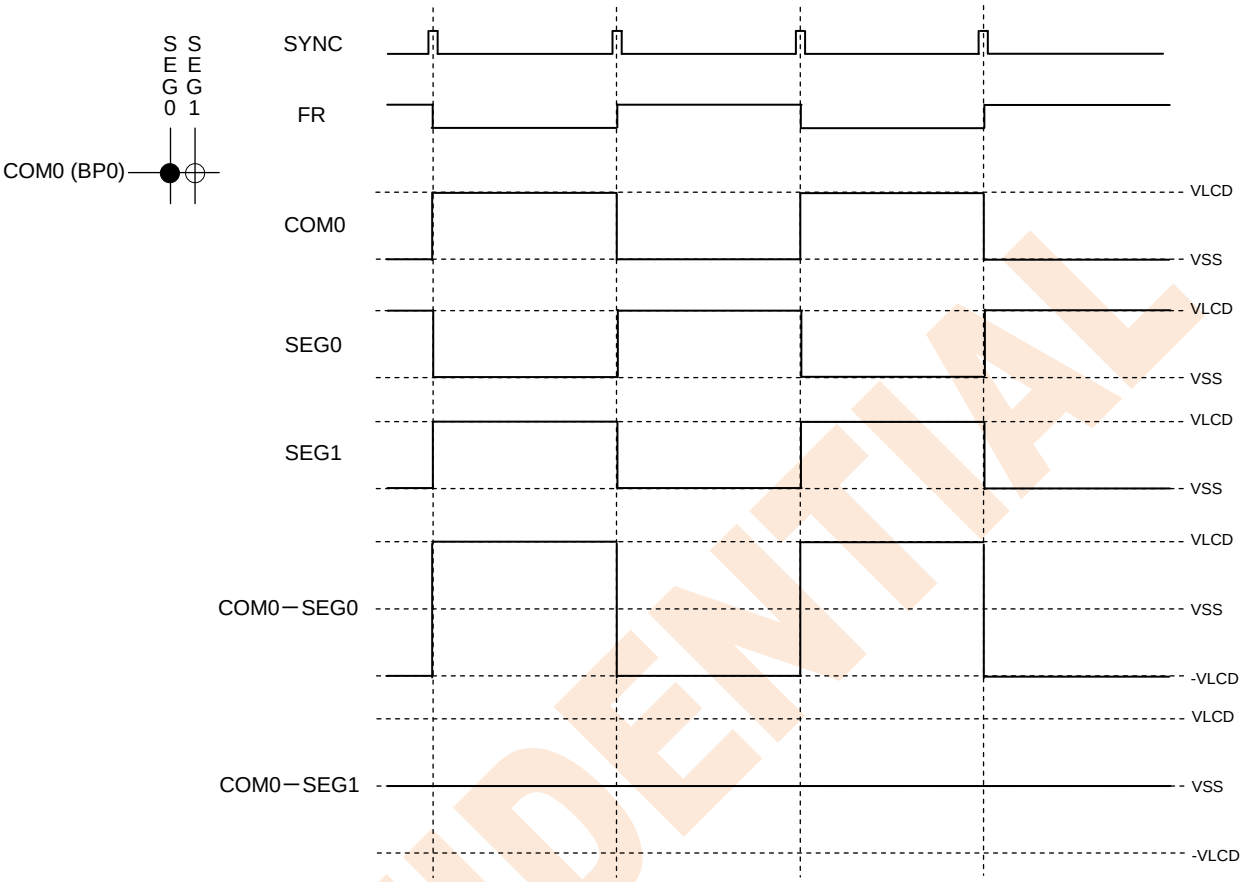


Figure 6.23 Drive Waveform B, 1-line Display (Static Drive=1/1 Duty) and 1/1 Bias

6.7 Power Supply Circuit for LCD Drive

6.7.1 Circuit Configuration

The power supply circuit for LCD drive is comprised of the VLCD voltage generating circuit and the bias voltage generating circuit as shown in Figure 6.24. In addition, the VLCD voltage generating circuit is comprised of the electronic volume, the VDC regulator and the booster circuit. The functional descriptions of those circuits described above are as shown in Table 6.13.
Those power supply circuits for LCD drive are enabled only in master operation mode (M/S="H").
Enabling/disabling the VLCD voltage generating circuit and the bias voltage generating circuit are selected by the PWRCTL command as shown in Table 6.14. The reference voltage VDC and the boosting ratio of the booster circuit can also be selected.
In addition, the external power supply can also be applicable.

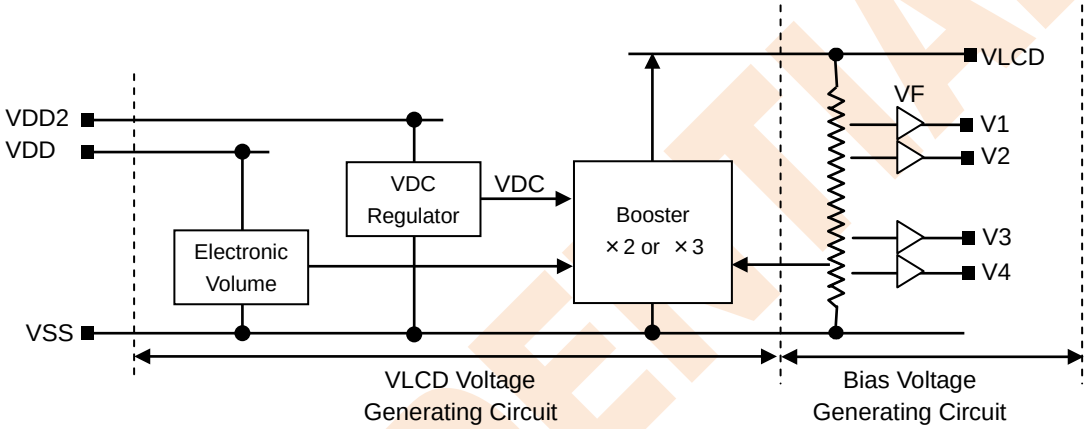


Figure 6.24 Configuration of Power Supply Circuit for LCD Drive

Table 6.13 Functional Description of Power Supply Circuit for LCD Drive

Circuit		Description	Power Supply	Generated Voltage
VLCD Voltage Generating Circuit	Electronic Volume	VLCD voltage is set by the EVSET command.	VDD	–
	VDC Regulator	VDC is generated from VDD2 by VDC regulator. VDC voltage is set to 4.0V (TBD) or 2.7V (TBD) by the PWRCTL command.	VDD2	VDC
	Booster	VLCD is generated by boosting the VDC using booster with charge pump method. VLCD is adjusted to setting voltage by controlling boosting operation using electronic volume and VLCD feedback signal.	VDC	VLCD
Bias Voltage Generation Circuit		Resistance between VLCD and VSS is divided by the specified bias ratio, and V1, V2, V3 and V4 are generated by the impedance-conversion.	VLCD	V1,V2, V3,V4

Table 6.14 PWRCTL Command Setting

P13	P12	P11	P10	Description
1				VLCD Voltage Generating Circuit: Used
0				VLCD Voltage Generating Circuit: Not used
	1			VDC Voltage: 4.0V (TBD)
	0			VDC Voltage: 2.7V (TBD)
		1		Boosting Ratio: x2
		0		Boosting Ratio: x3
			1	Bias Voltage Generating Circuit: Used
			0	Bias Voltage Generating Circuit: Not used

The power supply circuit for LCD drive can be used in any one of the following settings 1 to 3. The other settings are prohibited to use. The following settings 1 to 3 can be set by the PWRCTL command.

Table 6.15 Combination of Settings for LCD Drive Power Supply

Setting	Used Built-in Power Supply Circuit	P13	P12	P11	P10	External Power Supply
1	VLCD Voltage Generating Circuit Bias Voltage Generating Circuit	1	1/0 *1	1/0 *1	1	VDD, VDD2
2	Bias Voltage Generating Circuit	0	0	0	1	VDD, VDD2, VLCD
3	All External Power Supply	0	0	0	0	VDD, VDD2, VLCD, V1 to V4 *2

**1: 1 or 0 setting must be selected by the usage.*
**2: V1 to V4 must be set by the bias setting. Refer to Table 6.18.*

Each of the power supply circuits starts the operation with the PWRON command and stops with the PWROFF command.

6.7.2 VLCD Voltage Generating Circuit

6.7.2.1 Electronic Volume

The electronic volume circuit divides the VLCD output voltage range between 2.7V and 7.0V by 173, and selects one of the 173 states using the EVSET command. The relation between the electronic volume value α set by the EVSET command and the VLCD voltage is as shown in Table 6.16. The accuracy of VLCD output voltage is ±3% (TBD) at 25℃.

Table 6.16 Relation between Electronic Volume Value α and VLCD Voltage

D7	D6	D5	D4	D3	D2	D1	D0	α	VLCD Voltage
0	0	0	0	0	0	0	0	0	Minimum: 2.7V
0	0	0	0	0	0	0	1	1	
0	0	0	0	0	0	1	0	2	
:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	
1	0	1	0	1	0	1	0	170	
1	0	1	0	1	0	1	1	171	
1	0	1	0	1	1	0	0	172	Maximum: 7.0V

The VLCD voltage defined by the EVSET command can be determined by the following formula. The α in the formula indicates the electronic volume value (α= 0 to 172) in Table 6.16.

$$VLCD = 2.7 + 0.025 \times \alpha \ (V)$$

In addition, it is prohibited to set the VLCD voltage to be equal or lower than the VDC voltage. Therefore, when the electronic volume value α is set to the range of 0 to 60 (TBD) (α=60 corresponds to VDC_typ=4.0V+Margin=4.2V), the VDC voltage must be set to 2.7V (TBD) by the PWRCTL command.

6.7.2.2 VDC Regulator

The VDC regulator generates the input voltage VDC for the booster circuit from the power supply for the booster VDD2. The VDC voltage is set to 4.0V (TBD) or 2.7V (TBD) by the PWRCTL command.

6.7.2.3 Booster Circuit

The booster circuit generates the VLCD voltage by boosting the VCD voltage to the boosting ratio x2 or x3. The setting of boosting ratio can be selected by the PWRCTL command as shown in Table 6.14.

(1) In case of using VLCD generating circuit (Setting 1 in Table 6.15)
The external capacitor between VLCD and VSS must be connected. Refer to Figure 6.25 (1).

(2) In case of supplying VLCD from external without using VLCD generating circuit (Setting 2, 3 in Table 6.15)
The external power supply must be input to VLCD and the external capacitor between VLCD and VSS must be connected. Refer to Figure 6.25 (2).

(1) Use for VLCD Generating Circuit (2) No Use for VLCD Generating Circuit

Figure 6.25 Boosting Pin Connection of Booster

Table 6.17 indicates the recommended capacitance values connected between VLCD and VSS. The optimum capacitance values of the capacitors vary depending on the LCD panel and the display pattern. The display quality must be evaluated sufficiently using actual devices in order to determine the optimum capacitance value.

Table 6.17 Recommended Capacitance Values

Capacitor Connection Pin		Recommended Capacitance	Boosting Ratio Setting	Voltage Formula Biased at Both Ends of Capacitor	Maximum Voltage Biased at Both Ends of Capacitor
VLCD	VSS	1uF (TBD)	x2	(VDC-VSS) × 2	8.00V (TBD)
			x3	(VDC-VSS) × 3	8.00V (TBD)

The capacitor connected between VLCD and VSS that features the R-characteristics or the X7R-characteristics must be used. When this IC is operating at 85℃ or below, the capacitor that features the B-characteristics must be used. The capacitor that has 1.5 times or more of the rated voltage than the maximum applied voltage biased at the both ends of the capacitor is recommended to use as a guideline. Both of the polarized and nonpolarized capacitors can be connected.
If the load of the LCD panel is too large to obtain sufficient display quality, the VLCD voltage must be supplied externally without using the VLCD voltage generating circuit.

Load-current characteristic of the booster circuit is as shown in Figure 6.26 for reference data.

Figure 6.26 Load-Current Characteristic of Booster Circuit when using Built-in Capacitor

[Measurement Conditions]

- Wiring resistances of ITO (30ohm (TBD)) are connected to each of the power supplies VDD, VDD2, VSS and VLCD.

- VDD = VDD2 = 5.0V, x2/x3 booster, fBST = 2MHz/500kHz/125kHz (TBD), Ta = 25℃

6.7.3 Bias Voltage Generating Circuit

The bias voltage generating circuit generates the V1, V2, V3 and V4 voltages from the VLCD voltage corresponding to the bias ratio. Each of the generated voltages output from pins V1, V2, V3 and V4 by the impedance-conversion.
The bias ratio can be selected by the BIASSET command as shown in Table 6.18.
Because the V2 and V3 with 1/2 bias setting and the V1 to V4 with 1/1 bias setting are not used, those outputs are high-impedance (“HZ”) state.

Table 6.18 Bias Ratio

Voltage	BIASSET Command Parameter (P11, P10)		
	(0, 1)	(1, 0)	(1, 1)
	1/3 bias	1/2 bias	1/1 bias
V1	2/3 VLCD	1/2 VLCD	(“HZ”)
V2	1/3 VLCD	(“HZ”)	(“HZ”)
V3	2/3 VLCD	(“HZ”)	(“HZ”)
V4	1/3 VLCD	1/2 VLCD	(“HZ”)

This IC can provide sufficient display quality without connecting the stabilizing capacitors to pins V1 to V4 if the load of the LCD panel is small.
However, if the sufficient display quality cannot be obtained because of the load of the LCD panel is too large and then the V1 to V4 voltages become unstable, the external capacitors between each of the V1 to V4 pins and VSS must be connected. (The external capacitors are not required because the V2 and V3 voltages when 1/2 Bias setting, and the V1 to V4 voltages when 1/1 Bias setting are not used.)
The recommended capacitance value of the external capacitor is 1uF (TBD). The optimum capacitance values of the capacitors vary depending on the LCD panel and the display pattern. The display quality must be evaluated sufficiently using actual devices in order to determine the optimum capacitance value.
The capacitor that features the R-characteristics or the X7R-characteristics must be used. When this IC is operating at 85℃ or below, the capacitor that features the B-characteristics must be used.
The capacitor that has 1.5 times or more of the rated voltage than the maximum applied voltage biased at the both ends of the capacitor for each of the V1 to V4 is recommended to use as a guideline. Both of the polarized and nonpolarized capacitors can be connected.
Furthermore, if the load of the LCD panel is too large to obtain sufficient display quality even after connecting the capacitors, the VLCD from external and V1 to V4 voltages as shown in Table 6.19 must be supplied without using the built-in power supply circuit for LCD drive.

Table 6.19 Bias Voltage Supplied from External

Voltage	1/3 Bias *1	1/2 Bias *1	1/1 Bias *1
V1	2/3 VLCD	1/2 VLCD	VLCD *2
V2	1/3 VLCD	VSS *2	VSS *2
V3	2/3 VLCD	VLCD *2	VLCD *2
V4	1/3 VLCD	1/2 VLCD	VSS *2

**1: The BIASSET command input is not necessary when supplying bias voltages from external.*
**2: The V2 and V3 voltages when 1/2 Bias setting, and the V1 to V4 voltages when 1/1 Bias setting must also be supplied.*

6.7.4 Discharge Circuit

The discharge circuit discharges the charge of capacitors connected to the power supply circuit for LCD drive. This circuit is enabled in the master operation mode (M/S="H").
When invoking any one of the PWROFF, PSON and DSCHG commands, the discharge circuit is enabled.
In addition, the discharge circuit is also enabled during the period of XRES="L" while DCGSEL="H".

Table 6.20 Condition of Discharge ON

M/S	DCGSEL	During Operation of Power Supply Circuit for LCD Drive		DSCHG Command Input during PSON	XRES="L"
		PWROFF Command Input	PSON Command Input		
"H"	"H"	Enable	Enable	Enable	Enable
	"L"				Disable
"L"	"L" *1	Disable	Disable	Disable	Disable

**1: When the slave operation mode (M/S="L"), the DCGSEL pin is disabled. This pin must be tied to "L".*

- PWROFF Command or PSON Command Input;
  The output of the power supply circuits set to enable by the parameters P3 and P0 of the PWRCTL command is discharged for (TBD) ms when invoking the PWROFF command or the PSON command during the operation of the built-in power supply circuit for LCD drive while M/S="H". The VLCD is discharged when P3=1 and the V1 to V4 are discharged when P0=1. (The discharge circuit can be enabled even though the V2 and V3 voltages when 1/2 Bias setting, and the V1 to V4 voltages when 1/1 Bias setting are not used.)

- DSCHG Command Input;
  The power supply circuits set to ON by the DSCHG command parameter is discharged when invoking the DSCHG command while M/S="H" and PSON state. The VLCD is discharged when P1=1 and the V1 to V4 are discharged when P0=1.
  When using the external power supply by the PWRCTL command (Setting 2 and 3), the capacitors connected to the external power supplies can also be discharged according to the parameter setting of the DSCHG command. When enabling the discharge operation, the DSCHG command is invoked after turning-off the external power supplies.
  In addition, the parameter of the DSCHG command is initial state (OFF setting) when M/S="L" or PSOFF state.

- Period of XRES="L";
  When M/S="H" and DCHSEL="H", all of the VLCD and the V1 to V4 are discharged during the period of XRES="L".

In addition, because the V2 and V3 with 1/2 bias setting and the V1 to V4 with 1/1 bias setting are not used, those outputs are high-impedance ("HZ") state. However, those discharge circuits are enabled.

Figure 6.27 shows the discharge circuit of the power supply circuit. All switches in the following figure indicate discharging routes.

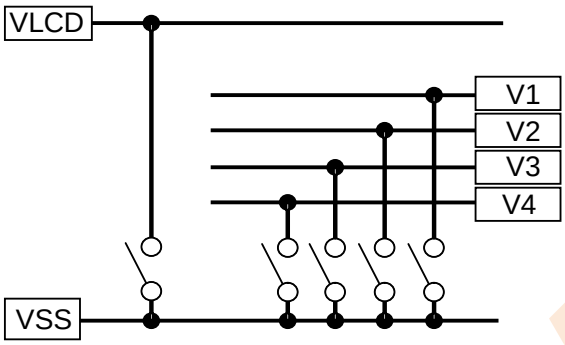


Figure 6.27 Discharging Routes of Power Supply Circuit

6.7.5 Precautions of Designing LCD Module

When assembling to COG, the resistance components are generated due to ITO wiring connected between this IC and the external components (capacitors) and between this IC and the power supply. These resistance components may cause of decreasing the display quality or malfunctions of this IC. When designing the LCD module, the assembling resistance value as shown in Table 6.21 must be followed as a guideline. In addition, the display quality and operations of this IC must be evaluated sufficiently using actual devices.

Table 6.21 Guideline of Assembling Resistance

Pin Type	Pin Name	Resistance Value
Power Supply Pin	VDD, VDD2, VSS	50Ω or less (TBD)
Power Supply Pin for LCD Drive	VLCD, V1 to V4	100Ω or less (TBD)
MPU Interface Pin	SDI/SDAIN, SDO/SDAACK, SCL, A0, XCS, XRES, ERR	500Ω or less (TBD)
Display Timing Pin	CL, SYNC, FR, XDOF	100Ω or less (TBD)

**1: The other pins have no guideline because these pins must be tied to "H" level, "L" level or left open according to the operating conditions.*

6.7.6 Examples of External Connection

① VDD=VDD2, Generate VLCD and V1 to V4 by using VLCD voltage generating circuit and Bias voltage generating circuit.
(PWRCTL command : P13=P10=1)

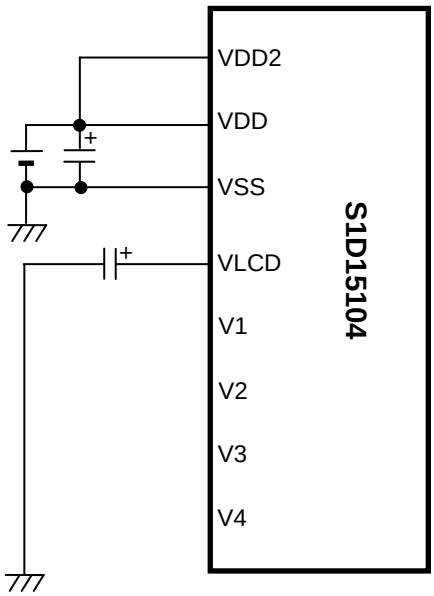


Figure 6.28 Connection Example ①

② VDD=VDD2, Supply VLCD externally, Generate V1 to V4 by using Bias voltage generating circuit.
(PWRCTL command: P13=0, P10=1)

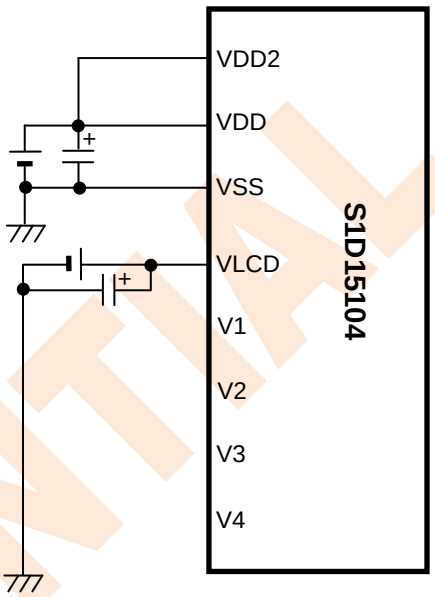


Figure 6.29 Connection Example ②

③ VDD=VDD, Supply VLCD and V1 to V4 externally.
(PWRCTL command: P13=P10=0)

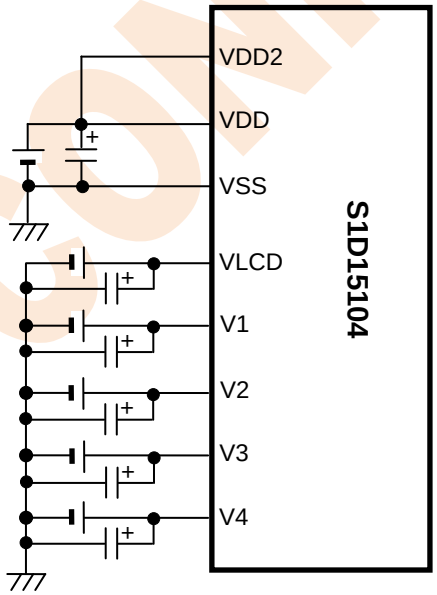


Figure 6.30 Connection Example ③

④ Another example of example ① (VDD=VDD2, Generate VLCD and V1 to V4 by using VLCD voltage generating circuit and Bias voltage generating circuit. (PWRCTL command : P13=P10=1)) in case of higher LCD panel losding.

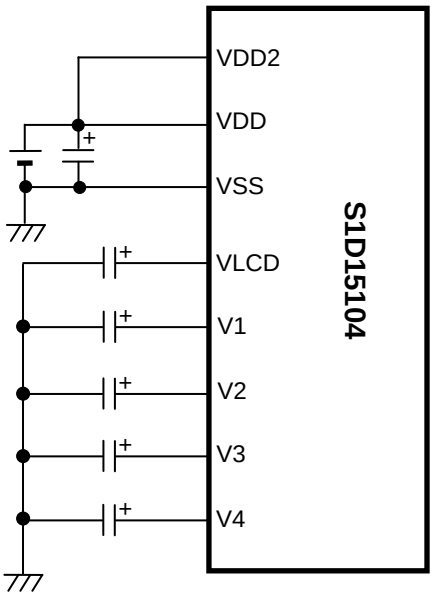


Figure 6.31 Connection Example ④

6.8 Error Detection Circuit

Error detection circuit detects the following operating status,

- Bit error detection of command registers
- Operating status detection of IC test circuit

Above detecting functions detect limited error modes. It is not guaranteed to detect all errors. Therefore, it is recommended that not only using above functions, but also executing periodical refreshing of the command settings and the contents of the display data RAM by referring to Section “8.2 Refresh”.

6.8.1 Bit Error Detection of Command Registers

This function can detect a bit error stored in the command registers caused by external noise and voltage fluctuation of the power supply for example.
Applied command registers for detecting a bit error of the command registers are as follows,

- DISON/DISOFF command
- DISSET command
- COMNOR/COMRVS command
- CANOR/CARVS command
- OSCON/OSCOFF command
- PWRCTL command
- PWRON/PWROFF command
- PSON/PSOFF command

When either command register described above 3 (TBD) commands generates a bit error, the ERR pin outputs “H” level. All command registers must be reset when detecting a bit error.
In addition, a bit error is also detected when this IC becomes initial state. So that, it becomes an error state after resetting by the XRES pin or after executing the power-on reset function. Then, the error state can be released after invoking above 3 (TBD) commands from the MPU while initial state.

6.8.2 Operating State Detection of IC Test Circuit

This function is to detect whether this IC is in a test mode for testing. The ERR pin outputs “H” level when this IC becomes in a test mode caused by some errors such as open state of the TEST pin for example. This IC holds an error state (ERR=”H” level output) until releasing above error.
When an error state (ERR=”H” level output) is not released even if all display data RAM and all commands are refreshed, there is a possibility of this error.

6.9 Reset

By setting XRES=”L”, this IC becomes initial state. In addition, because this IC contains the built-in power-on reset function, this IC also becomes initial state when turning on the power supply by enabling the built-in power-on reset circuit. When using the built-in power-on reset function without using the XRES pin for resetting, the XRES pin must be tied to “H” level. For details regarding the reset timing, refer to the description in Section “8.1 Initial Setting” and “11.4 Reset Timing”.
When M/S=”H” and DCHSEL=”H”, all of the VLCD and the V1 to V4 are discharged during the period of XRES=”L”. For details, refer to the description in Section “6.6.4 Discharge Circuit”.
For the initial setting values of commands and parameters after resetting, refer to the description in Section “7.2 Initial States”.

6.10 Master/Slave Mode

The display area can be extended by connecting multiple of this ICs as the master and slave sides.
The built-in circuit functions and input/output of the display timing signals are as shown in Table 6.22 by setting of the M/S and the CLS pins.

Table 6.22 Built-in Circuit Functions and Input/Output of Display Timing Signals

M/S	CLS	Display Clock Source	Power Supply Circuit	CL	SYNC	FR	XDOF
"H" (Master)	"H"	Built-in Oscillation Circuit	Enable	Output	Output	Output	Output
	"L"	External Input	Enable	Input	Output	Output	Output
"L" (Slave)	"H" or "L"	External Input	Disable	Input	Input	Input	Input

Figure 6.32 indicates an example of master/slave connection.

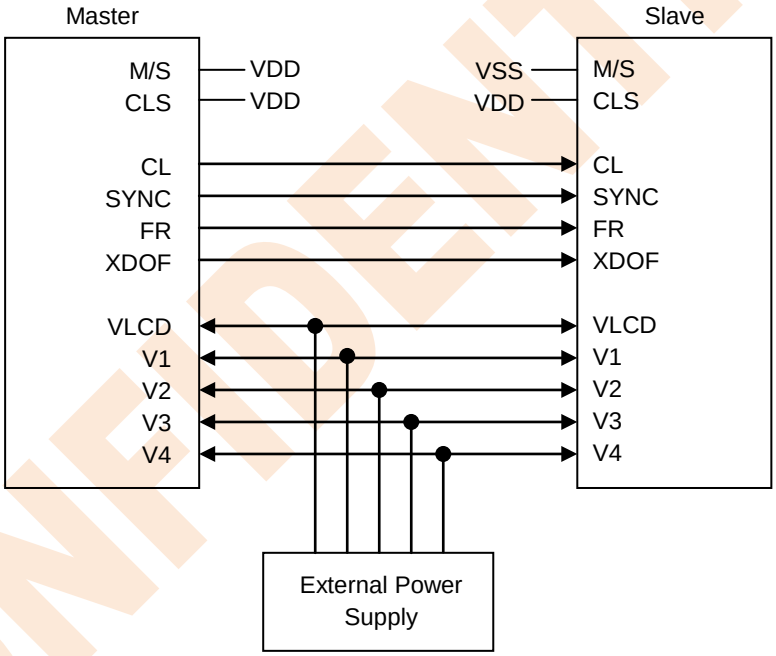


Figure 6.32 Example of Master/Slave Connection

The external voltages are recommended to use for the power supply for LCD drive (VLCD and V1 to V4).
The VLCD and the V1 to V4 voltages can also be generated by the power supply circuit for LCD drive in the master side and supplied them to the slave side. However, the LCD drive capability in the slave side may not be sufficient according to the load of the display panel. In addition, the power supply in the slave side may drop due to a wiring resistance from the master side to the slave side. Therefore, differences then may occur in the display contrast between the master and the slave sides. In order to prevent such a problem, the display quality must be evaluated sufficiently and must be determined whether to use or not the built-in power supply for LCD drive in the master side.

7. Commands

For the 4-wire serial interface (SPI), the data input signal (SDI) is identified by a combination of XCS, A0 and SCL. For the 2-wire serial interface (I2C-Bus compliant), the data input signal (SDAIN) is identified by a combination with SCL. For the timing diagram regarding command input, refer to Section "6.1.2 4-wire Serial Interface (SPI)" and Section "6.1.3 2-wire Serial Interface (I2C-Bus Compliant)".
The following notice must be taken into consideration when invoking a command.

- A command code that is not described in the commands list is prohibited to input.
- In order to prevent malfunctions caused by the excessive external noise, refreshing of the command settings must be executed periodically.

The data signals (D7 to D0) marked by asterisk "*" on the command tables in this Chapter must be set either "1 (H)" or "0 (L)". (The Hex codes on the command tables in this Chapter are described as "0 (L)".)

7.1 Commands List

No	Command Name	Command Code (Hex)	Instruction Length (Byte)	Description
(1)	DISON	AF	1	Display ON
(2)	DISOFF1	AE	1	Display OFF Mode 1
(3)	DISOFF2	AD	1	Display OFF Mode 2
(4)	DISSET	66	2	Display Mode Set
(5)	COMNOR	C4	1	Common Output Status: Normal
(6)	COMRVS	C5	1	Common Output Status: Reverse
(7)	DISSTLIN	8A	2	Display Start Line Set
(8)	PASET	B1	2	Page Address Set
(9)	CASET	13	3	Column Address Set
(10)	CANOR	84	1	Column Address Direction: Normal
(11)	CARVS	85	1	Column Address Direction: Reverse
(12)	WRRAM	1D	1+Display Data	Display Data RAM Write
(13)	NLSET	36	2	N-line Inversion Set
(14)	DISLINSET	6D	2	Number of Display Line Set
(15)	OSCON	AB	1	Built-in Oscillation Circuit: ON
(16)	OSCOFF	AA	1	Built-in Oscillation Circuit: OFF
(17)	FCLSEL	5F	2	Display Clock Frequency Select
(18)	FBSTSEL	55	2	Booster Clock Frequency Select
(19)	PWRCTL	27	2	Power Supply Control for LCD Drive
(20)	PWRON	25	1	Power Supply Circuit for LCD Drive: ON
(21)	PWROFF	24	1	Power Supply Circuit for LCD Drive: OFF
(22)	EVSET	81	2	Electronic Volume Set
(23)	BIASSET	A2	2	LCD Bias Set
(24)	DSCHG	EA	2	Discharge
(25)	PSON	A9	1	Power Save: ON
(26)	PSOFF	A8	1	Power Save: OFF
(27)	SWRST	5A	2	Software Reset
(28)	RDICREV	B5	2	IC Revision Number Read
(29)	RDICLOT	B6	3	IC Lot Number Read
(30)	NOP	E3	1	Non Operation

7.2 Initial Setting Value of Command Parameters

Initial state of the 1-byte command after resetting is as follows.

- DISON / DISOFF1 / DISOFF2 : DISOFF1
- COMNOR / COMRVS : COMNOR
- CANOR / CARVS : CANOR
- OSCON / OSCOFF : OSCOFF
- PWRON / PWROFF : PWROFF
- PSON / PSOFF : PSOFF

Initial state of the parameter of the multi-byte command except SWRST, RDICREV and RDICLOT after resetting is as follows.

Command Name		Parameter	Initial Setting Value									Initial State
			D7	D6	D5	D4	D3	D2	D1	D0	HEX	
(4)	DISSET	P11 to P10	*	*	*	*	*	*	0	0	00	Normal Display
(7)	DISSTLIN	P12 to P10	*	*	*	*	*	0	0	0	00	Display Start Line Address: 0h
(8)	PASET	P12 to P10 P16 to P14	*	0	0	0	*	0	0	0	00	Page Start Address: 0h Page End Address: 0h
(9)	CASET	P17 to P10 P27 to P20	0 1	0 1	0 1	0 0	0 1	0 1	0 1	0 1	00 EF	Column Start Address: 00h Column End Address: EFh
(13)	NLSET	P15 to P10	*	0	0	0	0	0	0	0	00	Waveform A (In this initial state, P15 to P10 are invalid.)
(14)	DISLINSET	P12 to P10	*	*	*	*	*	1	1	1	07	Prohibit (must be changed)
(17)	FCLSEL	P14 to P10	*	*	*	0	0	1	1	0	06	fCL=10.204kHz
(18)	FBSTSEL	P12 to P10	*	*	*	*	*	1	1	1	07	fBST=2000kHz
(19)	PWRCTL	P17 to P10	*	*	*	*	0	0	0	0	00	Not used Built-in Power Supply for LCD Drive (Use external Power Supply)
(22)	EVSET	P17 to P10	0	0	0	0	0	0	0	0	00	α=0
(23)	BIASSET	P12 to P10	*	*	*	*	*	*	0	1	00	1/3 Bias
(24)	DSCHG	P13 to P10	*	*	*	*	*	*	0	0	00	Discharge OFF

7.3 Command Descriptions

(1) DISON (DISplay ON): Display ON

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	0	1	1	1	1	AF	Command

This command turns on the display.
This command must be input after stabilizing the power supply for LCD drive. When using the power supply circuit for LCD drive (Parameter P13=1 or P10=1 of the PWRCTL command), this command enables after the period of the timer ON (about (TBD) ms) when turning on the power supply. When invoking this command during the period of the timer ON, this IC turns to the DISON state after the period of the timer ON.

(2) DISOFF1 (DISplay OFF mode 1): Display OFF mode 1

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	0	1	1	1	0	AE	Command

This command turns off the display (Display OFF mode 1). All SEG and COM pins are tied to VSS level.

(3) DISOFF2 (DISplay OFF mode 2): Display OFF mode 2

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	0	1	1	0	1	AD	Command

This command turns off the display (Display OFF mode 2). All SEG pins are output the off-state level ("0" level of RAM data in case of normal display mode or "1" level of RAM data in case of inverted display mode). In addition, all COM pins are output the non-selected level.
This command must be input after the power supply for LCD drive is stabilized. When using the power supply circuit for LCD drive (Parameter P13=1 or P10=1 of the PWRCTL command), this command enables after the period of the timer ON (about (TBD) ms) when turning on the power supply. When invoking this command during the period of the timer ON, this IC turns to the DISOFF2 state after the period of the timer ON.
The display quality must be evaluated and determined whether to switch or not to the DISOFF2 state prior to the DISON state from the DISOFF1 state.
When using 1-line display mode, this command is invalid.

Figure 7.1 indicates the timing diagram of the DISON/DISOFF when using the DISOFF2 command. When switching to the DISON state from the DISOFF1 state, the PWRON command must be input during the DISOFF1 state and input the DISOFF2 command during the period of the timer ON (about (TBD) ms) when turning on the power supply. After the period of the timer ON, this IC turns to the DISOFF2 state. The DISON command must be input after Min (TBD) ms later than the PWRON command input.
When switching to the DISOFF1 state from the DISON state, the DISOFF1 command must be input during the DISON state. The LCD display switches to the DISOFF1 state synchronizing with the SYNC signal. In case of switching to the DISOFF2 state from the DISON state, the procedure is same as above. The switching of the display mode for DISON/DISOFF1/DISOFF2 synchronizes to the SYNC signal.

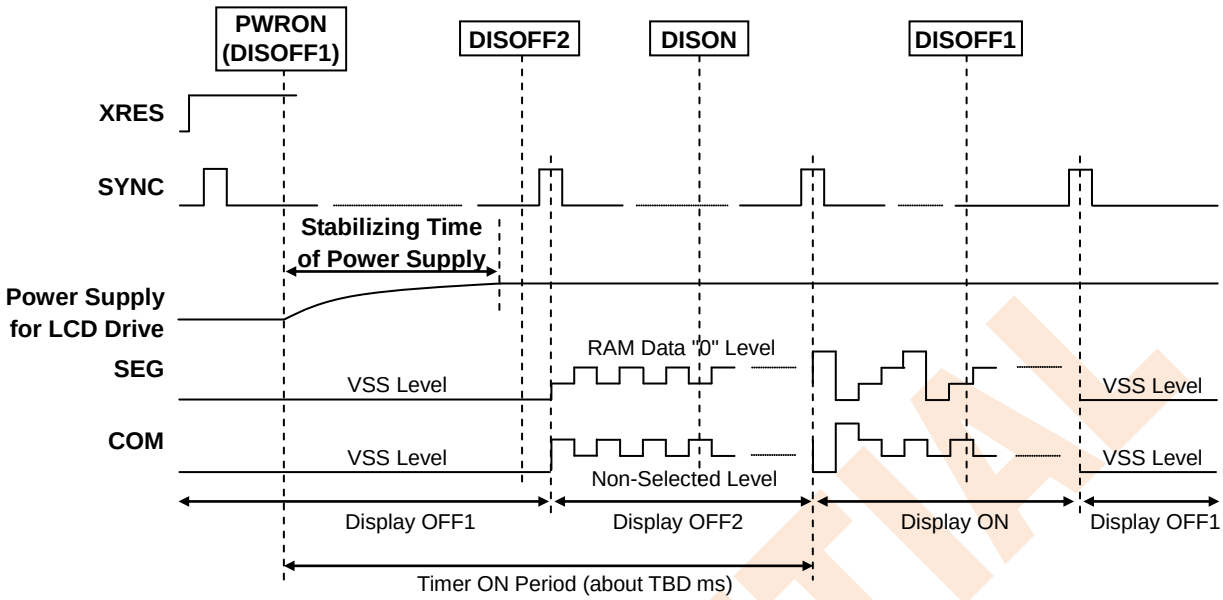


Figure 7.1 Timing Diagram of DISON / DISOFF

(4) DISSET (DISplay mode SET): Display mode set

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	1	1	0	0	1	1	0	66	Command
1	*	*	*	*	*	*	P11	P10	–	Parameter

This command defines the display mode.

P11, P10: Display mode

These parameters can switch the display mode without re-writing data to the display data RAM.

P11	P10	Display Mode
0	0	Normal
0	1	Inverted
1	0	All ON
1	1	All OFF

(5) COMNOR (COMmon output status NORmal): Common output status Normal

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	1	0	0	0	1	0	0	C4	Command

This command sets the common output state to normal. The connection method and the scanning direction can be selectable by the LCD module configuration. For details, refer to the description in Section “6.6.3 Setting of Common Output State”.

(6) COMRVS (COMmon output status ReVerSe): Common output status Reverse

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	1	0	0	0	1	0	1	C5	Command

This command sets the common output state to reverse. The connection method and the scanning direction can be selectable by the LCD module configuration. For details, refer to the description in Section “6.6.3 Setting of Common Output State”.

(7) DISSTLIN (DISplay STart LINe set): Display start line set

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	0	0	1	0	1	0	8A	Command
1	*	*	*	*	*	P12	P11	P10	—	Parameter

This command defines the display start line address of the display data RAM (Line address corresponding to BP0).
For details, refer to the description in Section “6.3.4 Line Address Circuit”.

P12 to P10: Display start line address

P12	P11	P10	Display Start Line Address			
			4-line Display	3-line Display	2-line Display	1-line Display
0	0	0	0h	0h	0h	0h
0	0	1	Prohibited	Prohibited	Prohibited	1h
0	1	0			2h	2h
0	1	1			Prohibited	3h
1	0	0	4h	4h	4h	4h
1	0	1	Prohibited	Prohibited	Prohibited	5h
1	1	0			6h	6h
1	1	1			Prohibited	7h

(8) PASET (Page Address SET): Page address set

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	1	0	0	0	1	B1	Command
1	*	P16	P15	P14	*	P12	P11	P10	—	Parameter

This command specifies the page start and end addresses of the display data RAM.
For details, refer to the description in Section “6.3.3 Page Address Circuit / Column Address Circuit”.

P12 to P10: Page start address
P16 to P14: Page end address

These parameters specify the page start address and the page end address.
The following condition must be kept.

Start Address ≦ End Address

P12	P11	P10	Page Start Address			
P16	P15	P14	Page End Address			
			4-line Display	3-line Display	2-line Display	1-line Display
0	0	0	0h	0h	0h	0h
0	0	1	1h	1h	1h	1h
0	1	0	Prohibited	Prohibited	2h	2h
0	1	1			3h	3h
1	0	0			Prohibited	4h
1	0	1				5h
1	1	0				6h
1	1	1				7h

(9) CASET (Column Address SET): Column address set

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	0	0	1	0	0	1	1	13	Command
1	P17	P16	P15	P14	P13	P12	P11	P10	–	Parameter
1	P27	P26	P25	P24	P23	P22	P21	P20	–	Parameter

This command specifies the column start and end addresses of the display data RAM.
For details, refer to the description in Section "6.3.3 Page Address Circuit / Column Address Circuit".

P17 to P10: Column start address
P27 to P20: Column end address

These parameters specify the column start address and the column end address.
The following condition must be kept.

Start Address ≦ End Address

In addition, the column start address and the column end address must be kept the following restrictions by the number of display line because the display data is input by 1 byte (8 bits) unit.

4-line Display: 60(3Ch) ≦ column start address ≦ 178(B2h),
column end address = column start address+1+2n ≦ 179(B3h)
3-line Display: 60(3Ch) ≦ column start address ≦ 178(B2h),
column end address = column start address+1+2n ≦ 179(B3h)
2-line Display: 60(3Ch) ≦ column start address ≦ 176(B0h),
column end address = column start address+3+4n ≦ 179(B3h)
1-line Display: 60(3Ch) ≦ column start address ≦ 172(ACh),
column end address = column start address+7+8n ≦ 179(B3h)
(n=0,1,2,3,・・・)

P17	P16	P15	P14	P13	P12	P11	P10	Start Address
P27	P26	P25	P24	P23	P22	P21	P20	End Address
0	0	0	0	0	0	0	0	Column 60 (3Ch)
0	0	0	0	0	0	0	1	Column 61 (3Dh)
0	0	0	0	0	0	1	0	Column 62 (3Eh)
:	:	:	:	:	:	:	:	:
1	1	1	0	1	1	1	0	Column 178 (B2h)
1	1	1	0	1	1	1	1	Column 179 (B3h)

(10) CANOR (Column Address direction NORmal): Column address direction Normal

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	0	0	0	1	0	0	84	Command

This command sets the relation between the column address and the SEG output to normal. The increment direction of the column address can be selectable by the LCD module configuration. For details regarding the setting, refer to the description in Sections “6.3.2 Memory Map of Display Data RAM” and “6.3.3 Page Address Circuit / Column Address Circuit”.

(11) CARVS (Column Address direction ReVerSe): Column address direction Reverse

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	0	0	0	1	0	1	85	Command

This command sets the relation between the column address and the SEG output to reverse. The increment direction of the column address can be selectable by the LCD module configuration. For details regarding the setting, refer to the description in Sections “6.3.2 Memory Map of Display Data RAM” and “6.3.3 Page Address Circuit / Column Address Circuit”.

(12) WRRAM (WRite RAM): Display data RAM write

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	0	0	1	1	1	0	1	1D	Command
1	*	*	*	*	*	*	*	*	—	Display Data

This command writes the display data to the specified address of the display data RAM.
For the 4-wire serial interface (SPI), the display data is written after invoking the command code (1Dh). There is no restriction for the number of parameter bytes of the display data. Writing operation to the display data RAM is automatically completed by invoking a next command.
For the 2-wire serial interface (I2C-Bus compliant), the display data is written after invoking the control byte identified the display data instead of invoking the command code (1Dh). There is no restriction for the number of parameter bytes of the display data. Writing operation to the display data RAM is completed by proceeding the communication completion procedure.
For more details regarding the operation of the column and page address, refer to the description in Section “6.3.3 Page Address Circuit / Column Address Circuit”.

(13) NLSET (N Line inversion SET): N-line set

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	0	1	1	0	1	1	0	36	Command
1	*	P16	P15	P14	P13	P12	P11	P10	–	Parameter

This command sets the inversion method and the number of inverted lines of the LCD AC drive.
For details, refer to the description in Section "6.5 Display Timing Generating Circuit".
The display quality caused by crosstalk issue for example may be able to improve by changing this command setting. These settings must be determined by evaluating the actual LCD display.

P16: Drive waveform A / B

0: Drive Waveform A
1: Drive Waveform B

P15: N-line inversion drive ON / OFF

This parameter is applicable only for P16=1 (Drive waveform B).

0: N-line inversion drive OFF (Frame inversion)
1: N-line inversion drive ON

P14: +1H dummy ON / OFF

This parameter is applicable only for P16=P15=1 (Drive waveform B and N-line inversion drive ON).
The contrast unevenness stripe may occur on the LCD display by generating the polarity deviation for each of the COMs according to the combination of the number of display lines and the number of N-line inversion. In this case, this parameter can change the above setting of the combination by adding +1H to frame cycle in order to remove this contrast unevenness stripe. The setting of the number of N-line inversion must be determined by evaluating the actual LCD display.
This parameter is invalid when using 1-line display mode (P12=P11=P10=0 of the DISLINSET command).

0: +1H dummy OFF
1: +1H dummy ON (Adding +1H to frame cycle)

P13: ON-state / OFF-state during +1H dummy period

This parameter is applicable only for P16=P15=P14=1 (Drive waveform B, N-line inversion drive ON and +1H dummy ON).
This parameter defines the SEG output state during the +1H dummy period. This setting must be determined by evaluating the actual LCD display.

0: Off-state during +1H dummy period (Output voltage correspond to RAM data "0" level)
1: On-state during +1H dummy period (Output voltage correspond to RAM data "1" level)

P12 to P10: Number of N-line inversion

These parameters are applicable only for P16=P15=1 (Drive waveform B and N-line inversion drive ON).
These parameters defines the number of N-line inversion of the LCD AC drive
Normally, the following condition must be kept.

$$\text{Number of N-line inversion} \leqq \text{Number of display lines} - 1$$

If the above condition is not met, this IC operates with the number of N-line inversion set by these parameters. In this case, the LCD AC drive may operate slower frequency than the frame inversion drive with the N-line inversion dive OFF.

P12	P11	P10	Number of N-line inversion
0	0	0	1-line (1H)
0	0	1	2-line (2H)
0	1	0	3-line (3H)
0	1	1	4-line (4H)
1	0	0	Prohibited
1	0	1	Prohibited
1	1	0	Prohibited
1	1	1	Prohibited

(14) DISLINSET (number of DISplay LINes SET): Number of display lines set

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	1	1	0	1	1	0	1	6D	Command
1	*	*	*	*	*	P12	P11	P10	–	Parameter

This Command defines the number of display lines.

P12 to P10: Number of display lines

P12	P11	P10	Number of Display Line
0	0	0	1-line
0	0	1	2-line
0	1	0	3-line
0	1	1	4-line
1	0	0	Prohibited
1	0	1	Prohibited
1	1	0	Prohibited
1	1	1	Prohibited

The relation between the number of display lines and the display duty (the ratio of 1 selection period (1H) of the line-sequential drive LCD to the frame cycle) is as follows.

In case of +1H dummy OFF,
Duty = 1 / Number of display lines
In case of +1H dummy ON,
Duty = 1 / (Number of display lines + 1)

(15) OSCON (OSCillator ON): Built-in oscillation circuit ON

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	0	1	0	1	1	AB	Command

When using the built-in oscillation circuit (CLS="H") as the display clock source in the master operation mode (M/S="H") or using the power supply circuit for LCD drive (Parameter P13=1 or P10=1 of the PWRCTL command) in the master operation mode (M/S="H"), the built-in oscillation circuit is enabled and can start the operation with this command.

(16) OSCOFF (OSCillator OFF): Built-in oscillation circuit OFF

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	0	1	0	1	0	AA	Command

When using the built-in oscillation circuit (CLS="H") as the display clock source in the master operation mode (M/S="H") or using the power supply circuit for LCD drive (Parameter P13=1 or P10=1 of the PWRCTL command) in the master operation mode (M/S="H"), the built-in oscillation circuit is enabled and can stop the operation with this command.

(17) FCLSEL (Frequency of display CLock SELect): Display clock frequency select

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	1	0	1	1	1	1	1	5F	Command
1	*	*	*	P14	P13	P12	P11	P10	–	Parameter

This command defines the display clock frequency fCL in case of using the built-in oscillation circuit (CLS="H") as the display clock source in the master operation mode (M/S="H"). The fCL is generated by dividing the built-in oscillation frequency fOSC (Typ. 4MHz).
This command is not applicable when the slave operation mode (M/S="L") or the external display clock input is selected (CLS="L").

P15 to P10: Display clock frequency selection

FCLSEL Parameter P14 to P10	fCL [kHz]	fSYNC [Hz]				
		4-line +1H (1/5 Duty)	4-line (1/4 Duty)	3-line (1/3 Duty)	2-line (1/2 Duty)	1-line (Static Drive =1/1 Duty)
00000	6.410	49.3	50.1	50.9	50.1	50.1
00001	7.042	54.2	55.0	55.9	55.0	55.0
00010	7.692	59.2	60.1	61.0	60.1	60.1
00011	8.333	64.1	65.1	66.1	65.1	65.1
00100	8.929	68.7	69.8	70.9	69.8	69.8
00101	9.615	74.0	75.1	76.3	75.1	75.1
00110	10.204	78.5	79.7	81.0	79.7	79.7
00111	10.870	83.6	84.9	86.3	84.9	84.9
01000	11.628	89.4	90.8	92.3	90.8	90.8
01001	12.195	93.8	95.3	96.8	95.3	95.3
01010	12.821	98.6	100	102	100	100
01011	14.085	108	110	112	110	110
01100	15.385	118	120	122	120	120
01101	16.667	128	130	132	130	130
01110	17.857	137	140	142	140	140
01111	19.231	148	150	153	150	150
10000	20.408	157	159	162	159	159
10001	21.739	167	170	173	170	170
10010	23.256	179	182	185	182	182
10011	24.390	188	191	194	191	191
10100	25.641	197	200	203.5	200	200
10101	28.169	217	220	224	220	220
10110	30.769	237	240	244	240	240
10111	33.333	256	260	265	260	260
11000	35.714	275	279	283	279	279
11001	38.462	296	300	305	300	300
11010	40.816	314	319	324	319	319
11011	43.478	334	340	345	340	340
11100	46.512	358	363	369	363	363
11101	48.780	375	381	387	381	381

[Definition of symbols]

fOSC : An oscillation frequency of a built-in oscillation circuit. 4MHz at typ. condition.

fCL : A display clock frequency. A basic clock that is required for the display operation and output to the CL pin when the master operation mode (M/S="H") and CLS="H". It is a frequency of an external clock that is input from the CL pin when the slave operation mode (M/S="L") or CLS="L".

fSYNC : The frame frequency fSYNC is defined by the display clock frequency fCL and the duty.

DISLINSET, NLSET (+1H dummy ON/OFF)		fSYNC
4-line +1H	(1/5 Duty)	fCL / 130
4-line	(1/4 Duty)	fCL / 128
3-line	(1/3 Duty)	fCL / 126
2-line	(1/2 Duty)	fCL / 128
1-line (Static Drive)	(1/1 Duty)	fCL / 128

(18) FBSTSEL (Frequency of BooST clock SELect): Booster clock frequency select

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	1	0	1	0	1	0	1	55	Command
1	*	*	*	*	*	P12	P11	P10	–	Parameter

This command defines the booster clock frequency fBST in case of using the VLCD voltage generating circuit (Parameter P13=1 of the PWRCTL command) in the master operation mode (M/S="H"). The fBST is generated by dividing the built-in oscillation frequency fOSC (Typ. 4MHz).
This command is not applicable when the slave operation mode (M/S="L") or the VLCD voltage generating circuit is not selected (Parameter P13=0 of the PWRCTL command).

P12 to P10: Booster clock frequency selection

P12	P11	P10	Booster Clock Frequency [kHz]
0	0	0	15.625
0	0	1	31.25
0	1	0	62.5
0	1	1	125
1	0	0	250
1	0	1	500
1	1	0	1000
1	1	1	2000

(19) PWRCTL (PoWeR supply ConTroL): Power supply control for LCD drive

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	0	1	0	0	1	1	1	27	Command
1	*	*	*	*	*	P12	P11	P10	—	Parameter

This command defines whether to use or not the VLCD voltage generating circuit and the bias voltage generating circuit. In addition, this command selects the reference voltage VDC and the boosting ratio of the booster circuit.
Each of the power supply circuits can start the operation by the PWRON command and can stop the operation by the PWROFF command.
For the parameter settings of P13 to P10, refer to the description in Section "6.7.1 Circuit Configuration".
This command is only applicable for the master operation mode (M/S="H")

P12 to P10: Setting of power supply circuit configuration for LCD drive

P13	P12 *1	P11 *1	P10	Description
1				VLCD Voltage Generating Circuit: Used
0				VLCD Voltage Generating Circuit: Not used
	1			VDC Voltage: 4.0V (TBD)
	0			VDC Voltage: 2.7V (TBD)
		1		Boosting Ratio: x2
		0		Boosting Ratio: x3
			1	Bias Voltage Generating Circuit: Used
			0	Bias Voltage Generating Circuit: Not used

**1: P12 and P11 is only applicable for P13=1. Setting of (P12,P11)=(1,0) is prohibited.*

(20) PWRON (PoWeR supply ON): Power supply ON for LCD drive

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	0	1	0	0	1	0	1	25	Command

This command turns on the power supply circuits set to use by the PWRCTL command.
Refer to the timing diagram in "Figure 7.1 Timing Diagram of DISON / DISOFF".
This IC turns to the DISOFF1 (Display OFF mode 1) state for about (TBD) ms until stabilizing the power supply by the built-in timer circuit. It can be invoked the DISOFF2 (Display OFF mode 2) command prior to the DISON command if necessary (During the period of the timer ON can also be applicable). In addition, the display quality must be evaluated and determined whether to input or not the DISOFF2 command prior to the DISON command.
The built-in timer can enable when the PWRON command is invoked while the PWROFF state. Therefore, the built-in timer cannot enable when the PWRON command is invoked while the PWRON state such as periodical refreshing for example.
This command input is not necessary when all power supplies are supplied from the external input (Parameter P13=P10=0 of the PWRCTL command).

(21) PWROFF (PoWeR supply OFF): Power supply OFF for LCD drive

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	0	1	0	0	1	0	0	24	Command

This command turns off the power supply circuits set to use by the PWRCTL command.

(22) EVSET (Electronic Volume SET): Electronic volume set

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	0	0	0	0	0	1	81	Command
1	P17	P16	P15	P14	P13	P12	P11	P10	–	Parameter

This command defines the electronic volume value α to adjust the VLCD voltage.
For details, refer to the description in Section "6.7.2.1 Electronic Volume".
When not using the VLCD voltage generating circuit (P13=0 of the PWRCTL command), this command is not necessary to set.

P17 to P10: VLCD voltage adjustment

P17	P16	P15	P14	P13	P12	P11	P10	α	VLCD Voltage
0	0	0	0	0	0	0	0	0	Minimum: 2.7V (TBD)
0	0	0	0	0	0	0	1	1	
0	0	1	0	0	0	1	0	2	
:	:	:	:	:	:	:	:	:	
1	0	1	0	1	0	1	0	170	
1	0	1	0	1	0	1	1	171	
1	0	1	0	1	1	0	0	172	Maximum: 7.0V

In addition, it is prohibited to set the VLCD voltage to under VDC voltage. Therefore, the VDC voltage must be set to use as 2.7V (TBD) by the PWRCTL command in case of setting the electronic voltage varue α = 0 to 60 (TBD) (α =60 corresponds to VDC_typ=4.0V+Mrgin=4.2V).

(23) BIASSET (lcd BIAS SET): LCD bias set

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	0	0	0	1	0	A2	Command
1	*	*	*	*	*	*	P11	P10	–	Parameter

This command defines the bias ration of the LCD drive voltage V1, V2, V3 and V4.
For details, refer to the description in Section "6.7.3 Bias Voltage Generating Circuit".
When not using the bias voltage generating circuit (P10=0 of the PWRCTL command), this command is not necessary to set.

P12 to P10: Setting of LCD bias ratio

P11	P10	Bias Ratio
0	0	Prohibited
0	1	1/3
1	0	1/2
1	1	1/1 (Static Drive)

(24) DSCHG (DiSCHarGe): Discharge

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	1	1	0	1	0	1	0	EA	Command
1	*	*	*	*	*	*	P11	P10	—	Parameter

This command discharges the capacitor connected to the power supply for LCD drive.
This command is enabled when the master operation mode (M/S="H").
For details, refer to the description in Section "6.7.4 Discharge Circuit".
This command is applicable only for the power saving mode by the PSON command.
The circuits set by the parameters P11 and P10 of this command can be discharged independent from the setting of the PWRCTL command. Therefore, this command must be executed after turning off the external power supply when supplying the power supply for LCD drive from the external.
In addition, the parameters P11 and P10 of the DSCHG command are set to initial state (0: OFF state) when M/S="L" or the PSOFF state..

P11: Discharge control of VLCD voltage

This parameter controls discharging of the VLCD voltage.
0: Discharge OFF
1: Discharge ON

P10: Discharge control of bias voltage

This parameter controls discharging of the bias voltage (V1,V2,V3,V4)..
0: Discharge OFF
1: Discharge ON

(25) PSON (Power Save ON): Power save ON

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	0	1	0	0	1	A9	Command

This command sets this IC to the power saving mode.
The internal states of this IC are as follows.

- The display mode is turned to the display OFF mode 1. All SEG and COM outputs are set to VSS level.
- The built-in power supply for LCD dive is disabled (PWROFF state).
- The outputs of the power supply for LCD drive set to use by the PWRCTL command are discharged.
- The built-in oscillation circuit is disabled.
- The contents of the command registers and the display data RAM are not rewritten by this command. In addition, the accessing from MPU such as rewriting of the display data for example is enabled.

(26) PSOFF (Power Save OFF): Power save OFF

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	0	1	0	0	0	A8	Command

This command releases the power saving state of this IC. The state of this IC returns to the state just before executing the PSON command. (However, the contents of the command registers and the display data RAM that are rewritten after executing the PSON command are not able to return.)
This IC turns to the DISOFF1 (Display OFF mode 1) state for about (TBD) ms by the built-in timer circuit when the power supply for LCD drive set to use by the PWRCTL command turns on again by the PSOFF command. After the period of the timer ON, this IC turns to the DISON state automatically.
The DISOFF2 (Display OFF mode 2) command can be invoked during the period of the timer ON, if necessary. In this case, this IC turns to the DISOFF2 state and does not turn to the display ON state after the period of the timer ON. In order to turn to the display ON state, the DISON command must be invoked. Refer to the timing diagram in “Figure 7.1 Timing Diagram of DISON / DISOFF”. The display quality must be evaluated and determined whether to invoke or not the DISOFF2 command.
In addition, the built-in timer circuit can be enabled when the PSOFF command is invoked while the PSON state. Therefore, the built-in timer cannot be enabled when the PSOFF command is invoked while the PSOFF state for periodical refreshing.

(27) SWRST (SoftWare ReSeT): Software reset

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	1	0	1	1	0	1	0	5A	Command
1	1	0	1	0	0	1	0	1	A5	Fixed Parameter

This command sets this IC to the initial state.

(28) RDICREV (ReaD IC REVision): IC revision read

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	1	0	1	0	1	B5	Command
–	R17	R16	R15	R14	R13	R12	R11	R10	–	Read Data

This command reads the revision data of this IC.
This command is only applicable for the 4-wire serial interface mode (IFS=”L”).

R17 to R10: Revision data of this IC

Register	Read Result	Description
R17 to R10	–	Revision data of this IC ・TS：01h

(29) RDICLOT (ReaD IC LOT number): IC lot number read

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	0	1	1	0	1	1	0	B6	Command
–	0	0	R15	R14	R13	R12	R11	R10	–	Read Data
–	R27	R26	R25	R24	R23	R22	R21	R20	–	Read Data

This command reads the lot number of this IC.
This command is only applicable for the 4-wire serial interface mode (IFS="L").

R15 to R10: Upper bit of the lot number
R27 to R20: Lower bit of the lot number

Correspondence between the read value and the lot number is as shown in Table 7.2. The lot number, 0000 to 9999 represented in binary data is read by this command.

Table 7.2 Read Value and Lot Number

Read Value														Lot No.
R15	R14	R13	R12	R11	R10	R27	R26	R25	R24	R23	R22	R21	R20	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002
:	:	:	:	:	:	:	:	:	:	:	:	:	:	
1	0	0	1	1	1	0	0	0	0	1	0	0	1	9997
1	0	0	1	1	1	0	0	0	0	1	0	1	0	9998
1	0	0	1	1	1	0	0	0	0	1	0	1	1	9999

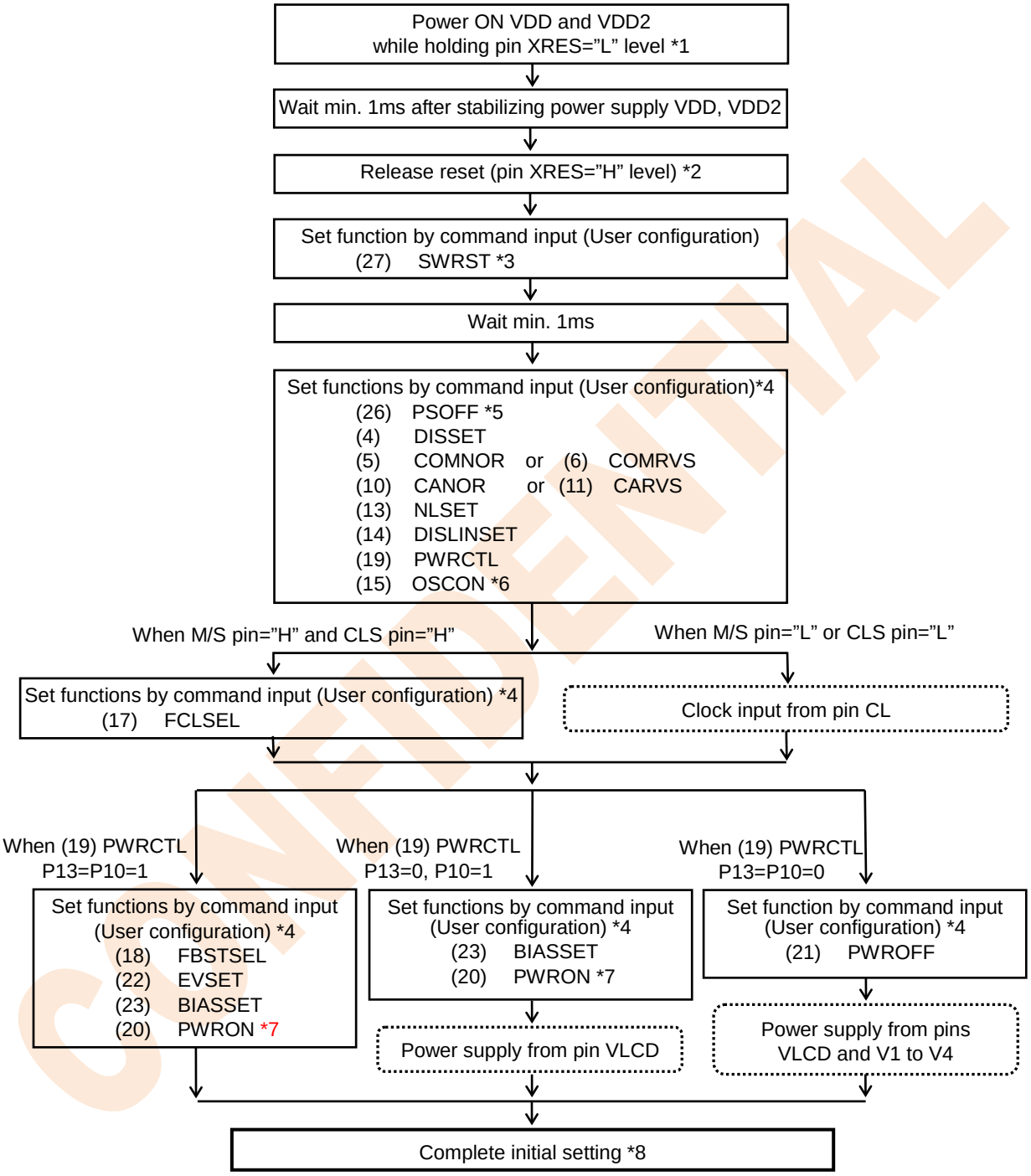
(30) NOP (Non Operation)

A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	1	1	1	0	0	0	1	1	E3	Command

This command is for the non-operation.

8. Instruction Settings

8.1 Initial Setting

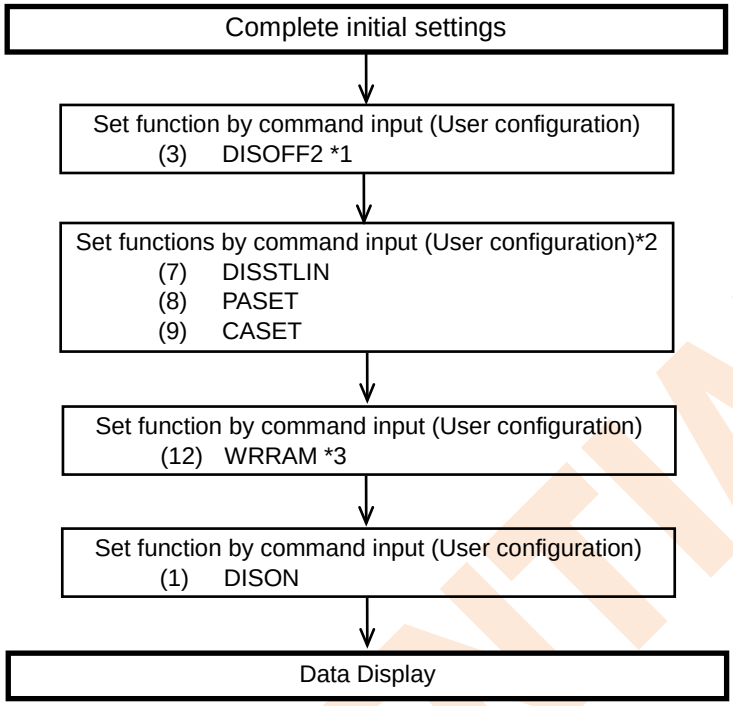


**: Numbers in parentheses correspond to the number in the item of command description.*

Figure 8.1 Example of Initial Setting

**1: When using the built-in power-on reset function and not using the XRES pin, the VDD must be turned on while the XRES pin is tied to VDD.*
The rise time of the VDD must be set min. (TBD) ms.
The VDD2 must be turned on at the same time or later than turning on the VDD.
**2: When using the built-in power-on reset function and not using the XRES pin (tied to XRES="H" level), this procedure is not necessary.*
The contents of the display data RAM are undefined in the initial state after reset.
**3: When using the XRES pin to reset, this procedure is not necessary.*
The contents of the display data RAM are undefined in the initial state after reset.
**4: Each of the OFF commands must be input and the default values must be set in order to recover from a sudden change of internal state caused by the excessive external noise for example, even if each of the functions are not used or the default values are used.*
**5: The PSOFF command is input for setting output of the ERR pin to "L" level when completing the initialization.*
**6: When using the built-in oscillation circuit (CLS="H") as a display clock source while the master operation (M/S="H") or using the power supply circuit for LCD drive (Parameter P13=1 or P10=1 of the PWRCTL command) while the master operation mode (M/S="H"), the OSCON command must be input.*
In other cases, that is, when the slave operation mode (M/S="L"), or using the external clock (CLS="L") as a display clock source and not using the power supply circuit for LCD drive (Parameter P13=P10=0 of the PWRCTL command) while the master operation mode (M/S="H"), the OSCON command input is not be required. In addition, the OSCON command canbe input because the built-in oscillation circuit turns to disable state according to the setting of the M/S pin, the CLS pin and the PWRCTL command.
**7: This IC becomes DISOFF1 (Display OFF mode 1) state during about (TBD) ms by the built-in timer circuit when the power supply for LCD drive set to use by the PWRCTL command starts up by the PWRON command.*
**8: It is recommended that this IC must not be accessed until the built-in LCD drive voltage becomes stable. The rise time of this voltage depends on the operating condition of this IC. In case of fBST=(TBD), VLCD stabilizing capacitor=(TBD)uF, VLCD=(TBD)V at the state 1 of the power supply for LCD drive, the rise time is max. (TBD)ms. Care must be taken to set with sufficient margin after evaluating the display quality and the operation using the actual device..*

8.2 Data Display



**: Numbers in parentheses correspond to the number in the item of command description.*

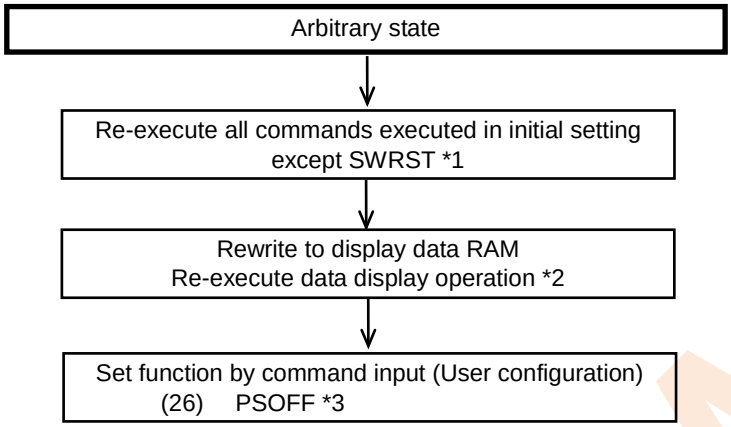
Figure 8.2 Setting Example of Data Display

**1:The display quality must be evaluated and determined whether to input or not the DISOFF2 (Display OFF mode 2) command. When not using the DISOFF2 command, this procedure is not necessary.*
The DISOFF2 command must be input after stabilizing the power supply for LCD drive. Tthis command can also be input during the period of the timer ON (about (TBD) ms) when turning on the power supply in the initial setting. Refer to the timing diagram in "Figure 7.1 Timing Diagram of DISON / DISOFF".

**2: Each of the commands must be input and must be set in order to recover from a sudden change of internal state caused by the excessive external noise for example, even if the default values of each of the functions are used.*

**3: For the 4-wire serial interface (SPI), the display data is input after invoking the command code (1Dh). Writing operation to the display data RAM (WRRAM status) is automatically completed by the next command input.*
For the 2-wire serial interface (I2C-Bus compliant), the display data is input after inputting the control byte identified the display data instead of invoking the command code (1Dh). Writing operation to the display data RAM (WRRAM status) is completed by proceeding the communication completion.

8.3 Refreshing



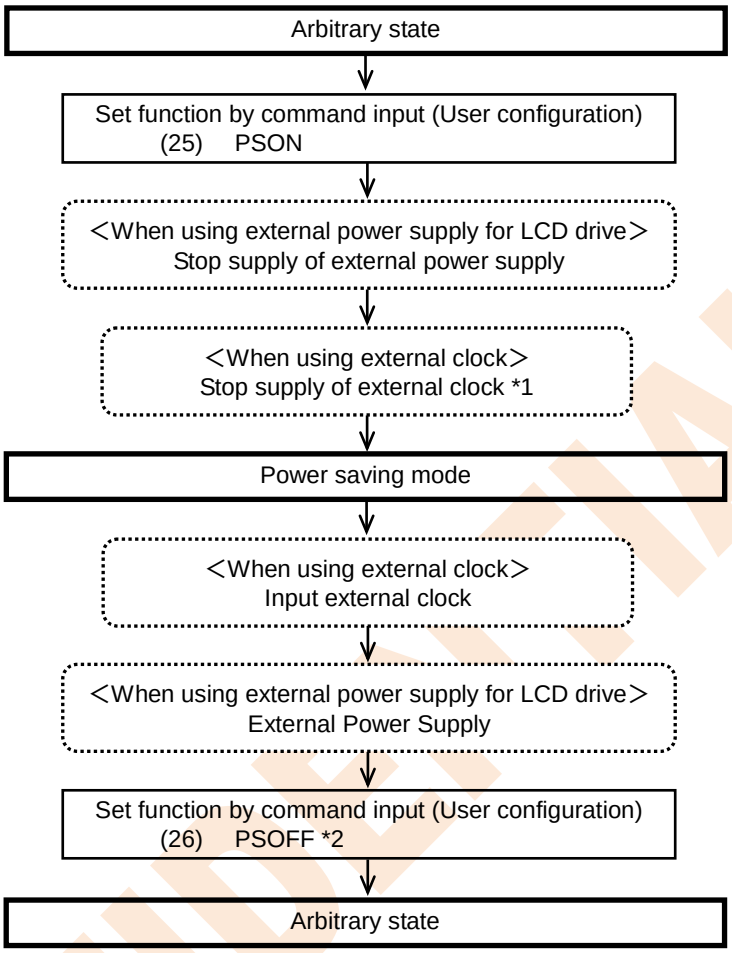
**: Numbers in parentheses correspond to the number in the item of command description.*

Figure 8.3 Setting Example of Refreshing

This IC holds the operating state by each of the commands. However, the internal state may change by the excessive external noise for example. The measures must be taken to prevent the noise generation or influence in terms of assembling and the system itself. In order to prevent malfunctions caused by the sudden external noise, it is recommended to refresh the operating state and the contents of the display periodically.

**1: Refer to the description in Section "8.1 Initial Setting". In addition, the SWRST command must not be used.*
**2: Refer to the description in Section "8.2 Data Display".*
**3: When this IC becomes the power-saving mode incorrectly, the PSOFF command must be used to exit. In addition, when this IC becomes the discharge mode (DSCHRG) incorrectly, the PSOFF command must also be used to exit by setting to the discharge OFF.*

8.4 Power Save ON / OFF



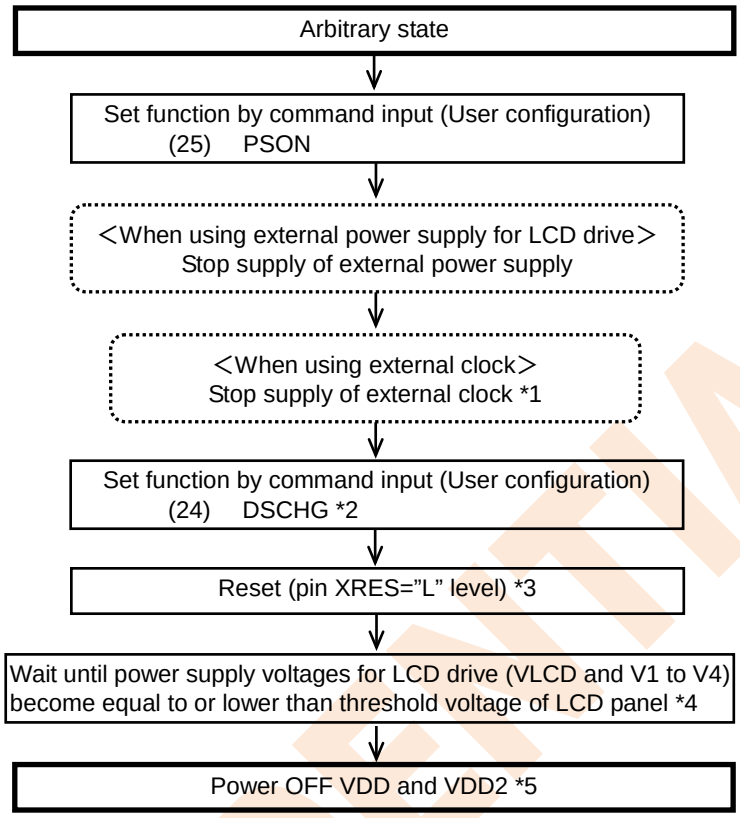
**: Numbers in parentheses correspond to the number in the item of command description.*

Figure 8.4 Setting Example of Power Saving

**1: It is necessary to wait 70ms + 2200 or more clocks (TBD) until the external clock supply stops after invoking the PSON command.*

**2: When using the built-in power supply circuit for LCD drive, the power supply circuit for LCD drive starts up by the PSOFF command input. It is recommended that this IC must not be accessed until the built-in LCD drive voltage becomes stable. The rise time of this voltage depends on the operating condition of this IC. In case of fBST=(TBD), VLCD stabilizing capacitor=(TBD)uF, VLCD=(TBD)V at the state 1 of the power supply for LCD drive, the rise time is max. (TBD)ms. Care must be taken to set with sufficient margin after evaluating the display quality and the operation using the actual device.*
This IC becomes DISOFF1 (Display OFF mode 1) state during the period of (TBD) frames from the PSOFF command input by the built-in timer circuit. After the period of the timer ON, this IC turns to the DISON state automatically.
The DISOFF2 (Display OFF mode 2) command can be input during the period of the timer ON, if necessary. In this case, it cannot be turned to the display ON state automatically after the period of the timer ON. In order to turn to the display ON state, the DISON command must be invoked. Refer to the timing diagram in "Figure 7.1 Timing Diagram of DISON / DISOFF". The display quality must be evaluated and determined whether to input or not the DISOFF2 command.

8.5 Power OFF



**: Numbers in parentheses correspond to the number in the item of command description.*

Figure 8.5 Setting Example of Power OFF

**1: It is necessary to wait 70ms + 2200 or more clocks (TBD) until the external clock supply stops after invoking the PSON command.*

**2: When using the external power supply (Power supply for LCD drive State-2 or State-3), this command can discharge the capacitor connected to the external power supply to VSS.*
If the external power supply circuit has a discharge function, this procedure can be eliminated.
In addition, when executing reset (XRES="L" level) while DCGSEL="H", this procedure can be eliminated.

**3: When using the built-in power-on reset function and not using the XRES pin (tied to XRES="H" level), this procedure is not necessary.*

**4: The threshold voltage of the LCD panel is approximately 1[V] as reference. The wait time must be determined by evaluating the actual device.*

**5: The fall time of the VDD must be set min. (TBD)ms.*
The VDD2 must be turned off at the same time or earlier than turning off the VDD.

9. Absolute Maximum Ratings

Table 9.1 Absolute Maximum Ratings

Paremeter	Symbol	Specification	Unit
Supply Voltage (1)	VDD	-0.3 to 6.2 (TBD)	V
Supply Voltage (2)	VDD2	-0.3 to 6.2 (TBD)	
Supply Voltage (3)	VDC	-0.3 to 3.6 (TBD)	
Supply Voltage (4)	VLCD	-0.3 to 9.0 (TBD)	
Supply Voltage (5)	V1, V2, V3, V4	-0.3 to 9.0 (TBD)	
Input Voltage	V_{IN}	-0.3 to VDD+0.3	
Output Voltage	V_O	-0.3 to VDD+0.3	
Operating Temperature	T_{OPR}	-40 to 105	℃
Storage Temperature	T_{STR}	-55 to 125	

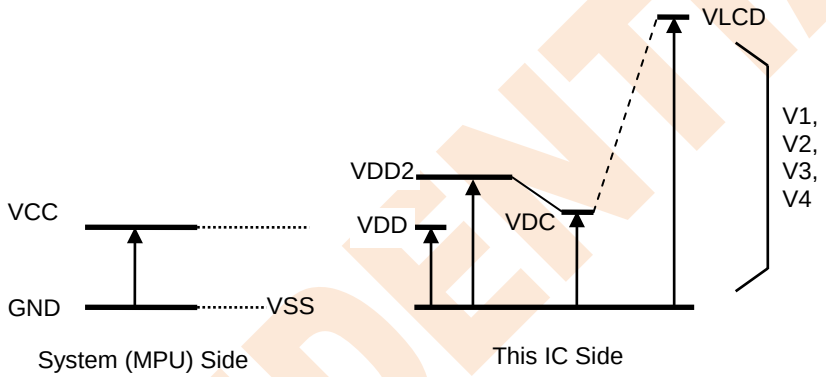


Figure 9.1 Voltage Relation Diagram

**1: Unless otherwise noted, all voltages are specified based on VSS=0V.*
**2: If this IC is operated by exceeding above absolute maximum ratings, this IC may damage permanently. In the normal operation, this IC must be operated within the following range as shown in Chapter "10. DC Characteristics". If this IC is operated over the following DC characteristics, it may cause this IC to malfunction. In addition, the reliability of this IC may decrease.*
**3:The following voltage conditions must be always kept.*

- *VDD2≧VDD*
- *VDD2≧VDC*
- *VLCD≧V1≧VSS, VLCD≧V2≧VSS, VLCD≧V3≧VSS, VLCD≧V4≧VSS*

10. DC Characteristics

10.1 Power Supply Voltage

Table 10.1 Power Supply Voltage

VSS=0V, Ta=-40 to 105℃

Parameter	Symbol	Conditions		Specification			Unit	Applied Pins
				Min.	Typ.	Max.		
Operating Voltage (1)	VDD	External Supply		2.7	–	5.5	V	VDD
Operating Voltage (2)	VDD2	External Supply		VDD	–	5.5		VDD2
Operating Voltage (3)	VDC	Internal Generation (Output)	x2 Booster	(TBD)	(TBD)	(TBD)		VDC
			x3 Booster	(TBD)	(TBD)	(TBD)		
Operating Voltage (4)	VLCD	Internal Generation (Output) 25℃	1/3 Bias, 1/2 Bias *2	4.5 (TBD)	–	7		VLCD
			1/1 Bias *2	2.7	–	7		
			Deviation *3	-3	–	3	%	
		External Supply	1/3 Bias, 1/2 Bias	4.5 (TBD)	–	8	V	
			1/1 Bias	2.7	–	8		
Operating Voltage (5)	V1 to V4	Internal Generation (Output)	Deviation *4	-0.1	–	0.1		V1 to V4
		External Supply	Deviation *4	-0.1	–	0.1		

**1: The operations of this IC cannot be guaranteed when rapid voltage fluctuations are observed.*
**2: Configurable voltage range set by VLCD = 2.7 + 0.025 x α [V] (α : Electronic volume value).*
**3: Deviation range from VLCD = 2.7 + 0.025 x α [V] (α : Electronic volume value)*
**4: Deviation range from the following bias voltage calculation value.*

Voltage	1/3 Bias	1/2 Bias	1/1 Bias
V1	2/3 VLCD	1/2 VLCD	VLCD
V2	1/3 VLCD	VSS	VSS
V3	2/3 VLCD	VLCD	VLCD
V4	1/3 VLCD	1/2 VLCD	VSS

10.2 Pin Characteristics

Table 10.2 Pin Characteristics

VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105℃

Parameter	Symbol	Conditions		Specification			Unit	Applied Pins
				Min.	Typ.	Max.		
HIGH-Level Input Voltage	VIHC	—		0.8×VDD	—	VDD	V	*1
LOW-Level Input Voltage	VILC	—		VSS	—	0.2×VDD		
Hysteresis Voltage	VH	VDD = 5.0V		0.5	0.7	—		
HIGH-Level Output Voltage	VOHC	IO = -0.1mA		0.8×VDD	—	VDD		*2
LOW-Level Output Voltage	VOLC	IOL = +0.1mA		VSS	—	0.2×VDD		
Input Leakage Current	ILI	VIN=VDD or VSS		−3.0	—	3.0	μA	*3
I/O Leakage Current	ILIO			−3.0	—	3.0		*4
LCD Driver ON-Resistance	RON	Ta=25℃ *5	VLCD = 3.3V	—	(TBD)	(TBD)	kΩ	SEGn, COMn
			VLCD = 5.0V	—	(TBD)	(TBD)		
Input Pin Capacitance	CIN	Ta = 25℃, f = 1Mz		—	(TBD)	10	pF	*1

1: IFS, SDI/SDAIN, SCL, A0, XCS, XRES, DCGSEL, SA1, SA0, CLS, M/S, CL, SYNC, FR, XDOF, TEST
**2: SDO/SDAACK (no specification of VOHC for SDAACK), ERR, CL, SYNC, FR, XDOF*
3: IFS, SDI/SDAIN, SCL, A0, XCS, XRES, DCGSEL, SA1, SA0, CLS, M/S, TEST
**4: Applied for when the SDO/SDAACK, CL, SYNC, FR and XDOF pins are in "High-impedance" state or input mode.*
**5: Measured by applying the 0.1V potential difference to the output voltage of SEGn or COMn.*

10.3 Oscillation Characteristics

Table 10.3 Oscillation Characteristics

VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105℃

Parameter		Symbol	Conditions	Specification			Unit	Applied Pins
				Min.	Typ.	Max.		
Oscillation Frequency	Built-in Oscillator *1	fOSC	—	3600	4000	4400	kHz	—
	External Input *2	fCL	—	—	—	300		CL

**1: This specification indicates the oscillation frequency and its production fluctuation of the built-in oscillator. Regarding the display clock frequency fCL and the frame frequency fSYNC divided by this oscillation frequency, refer to the description in Section "7.3 Command Description (17) FCLSEL command". The fCL, fSYNC and fBST also fluctuates ±10%.*
**2: This specification indicates the operable maximum frequency of the external input clock fCL in case of supplying the display clock from external (CLS="L"). The relation between the external input clock frequency fCL and the frame frequency fSYNC is as shown in the following table.*

DISLINSET, NLSET (+1H Dummy ON/OFF)		fSYNC
4 lines +1H	(1/5 Duty)	fCL / 130
4 lines	(1/4 Duty)	fCL / 128
3 lines	(1/3 Duty)	fCL / 126
2 lines	(1/2 Duty)	fCL / 128
1 line (Static Drive)	(1/1 Duty)	fCL / 128

10.4 Current Consumption

10.4.1 Static Current Consumption

The following table indicates the static current consumption in case of the initial state after reset or in the power-saving mode.

Table 10.4 Static Current Consumption

VSS=0V, Ta=25℃

Parameter	Symbol	Conditions	Specification			Unit	Applied Pins
			Min.	Typ.	Max.		
Static Current Consumption	IDDQ	VDD=5.5V	–	(TBD)	(TBD)	μA	VDD
	IDD2Q	VDD2=5.5V	–	(TBD)	(TBD)	μA	VDD2
	ILCDQ	VLCD=8.0V	–	(TBD)	(TBD)	μA	VLCD

10.4.2 Dynamic Current Consumption

The following current consumption is the current that consumed by this IC alone, and is not included the current that consumed by the LCD panel capacitance and the wiring capacitance.

10.4.2.1 Current Consumption when Display ON

Table 10.5 Current Consumption in case of Drive Waveform A and All Checker Display

VSS=0V, Ta=25℃

Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
1/4 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 5.0V VLCD= 6.0V VLCD Voltage Generating Circuit ON x2 Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	μA
1/4 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 5.0V VLCD= 5.0V VLCD Voltage Generating Circuit OFF Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	μA
1/4 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 3.0V VLCD= 6.0V VLCD Voltage Generating Circuit ON x3 Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	μA
1/3 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 5.0V VLCD= 5.0V VLCD Voltage Generating Circuit OFF Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	μA
1/3 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 3.0V VLCD= 5.0V VLCD Voltage Generating Circuit ON x2 Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	μA
1/2 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 5.0V VLCD= 5.0V VLCD Voltage Generating Circuit OFF Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	μA
1/2 Duty, 1/2 Bias fSYNC=**Hz	IOP	VDD=VDD2= 3.0V VLCD= 3.0V VLCD Voltage Generating Circuit OFF Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	μA

Table 10.6 Current Consumption in case of Drive Waveform B and All Checker Display

VSS=0V, Ta=25°C

Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
1/4 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 5.0V VLCD= 6.0V VLCD Voltage Generating Circuit ON x2 Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	µA
1/4 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 5.0V VLCD= 5.0V VLCD Voltage Generating Circuit OFF Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	µA
1/4 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 3.0V VLCD= 6.0V VLCD Voltage Generating Circuit ON x3 Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	µA
1/3 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 5.0V VLCD= 5.0V VLCD Voltage Generating Circuit OFF Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	µA
1/3 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 3.0V VLCD= 5.0V VLCD Voltage Generating Circuit ON x2 Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	µA
1/2 Duty, 1/3 Bias fSYNC=**Hz	IOP	VDD=VDD2= 5.0V VLCD= 5.0V VLCD Voltage Generating Circuit OFF Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	µA
1/2 Duty, 1/2 Bias fSYNC=**Hz	IOP	VDD=VDD2= 3.0V VLCD= 3.0V VLCD Voltage Generating Circuit OFF Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	µA
1/1 Duty, 1/1 Bias fSYNC=**Hz	IOP	VDD=VDD2= 3.0V VLCD= 3.0V VLCD Voltage Generating Circuit OFF Bias Voltage Generating Circuit ON Built-in Oscillation Circuit ON	–	(TBD)	(TBD)	µA

10.4.2.2 Current Consumption when Accessing to MPU

The current consumption flowed through the VDD pin when the display data is transmitted all the time from MPU by the frequency of fCYC is as shown in Figure 10.1 as reference. In this case, the power supply circuit for LCD drive and the built-in oscillation circuit are disabled. The current consumption that consumed by this IC alone when accessing to MPU while display ON is the sum of this current and the current indicated in Section “10.4.2.1 Current Consumption when Display ON”.

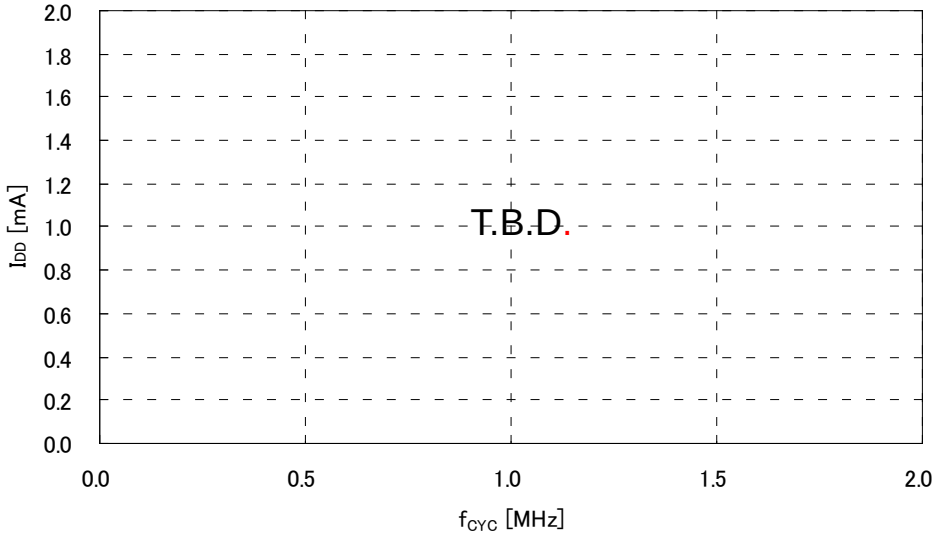


Figure 10.1 VDD Current Consumption when accessing to MPU

11. AC Characteristics

11.1 4-wire Serial Interface (SPI)

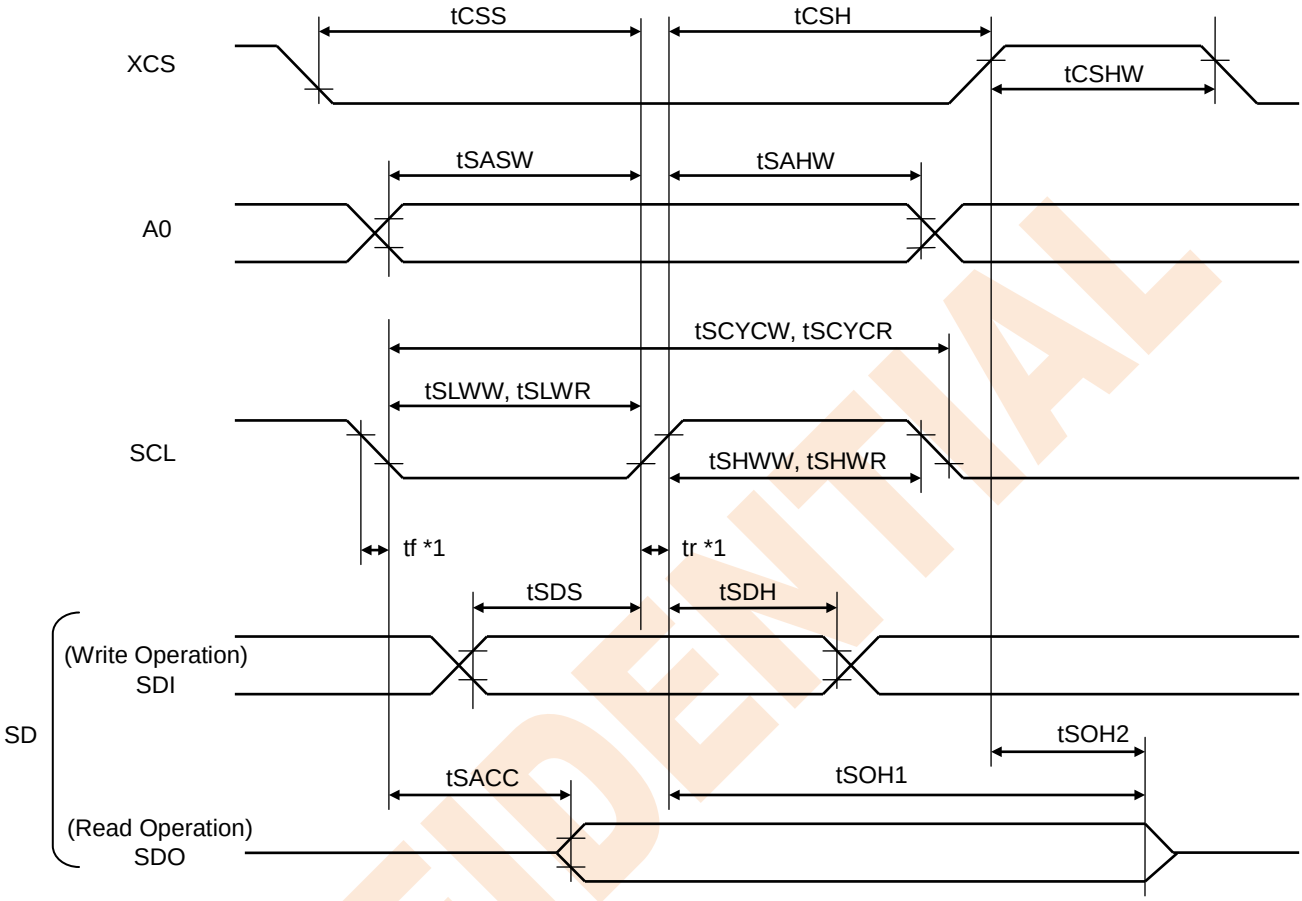


Figure 11.1 4-wire Serial Interface (SPI)

Table 11.1 4-wire Serial Interface (SPI)

VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C

Parameter		Signal	Symbol	Conditions	Specification		Unit
					Min.	Max.	
Address Setup Time	Write	A0	tSASW	–	(200) (TBD)	–	ns
Address Hold Time	Write	A0	tSAHW	–	(200) (TBD)	–	
Serial Clock Cycle	Write	SCL	tSCYCW	–	(550) (TBD)	–	
	Read	SCL	tSCYCR	–	(1500) (TBD)	–	
SCL_L Pulse Width	Write	SCL	tSLWW	–	(250) (TBD)	–	
	Read	SCL	tSLWR	–	(900) (TBD)	–	
SCL_H Pulse Width	Write	SCL	tSHWW	–	(250) (TBD)	–	
	Read	SCL	tSHWR	–	(450) (TBD)	–	
Data Setup Time		SD	tSDS	–	(200) (TBD)	–	
Data Hold Time		SD	tSDH	–	(200) (TBD)	–	
XCS-SCL Time		XCS	tCSS	–	(300) (TBD)	–	
		XCS	tCSH	–	(200) (TBD)	–	
XCS_H Pulse Width		XCS	tCSHW	–	(450) (TBD)	–	
Read Access Time		SD	tSACC	Cload=100pF	–	(900) (TBD)	
Output Disable Time *2		SD	tSOH1	Cload=100pF	(30) (TBD)	(400) (TBD)	
		SD	tSOH2	Cload=100pF	(30) (TBD)	(400) (TBD)	

**1: tr + tf = tSCYC - (tSLW + tSHW)*
**2: The output disable time is the time that the SD signal turns to "High-impedance" state after read output.*
**3: All timing specifications except the output disable time are specified based on the voltage level at 20% and 80% of the VDD.*

11.2 2-wire Serial Interface (I2C-Bus Compliant)

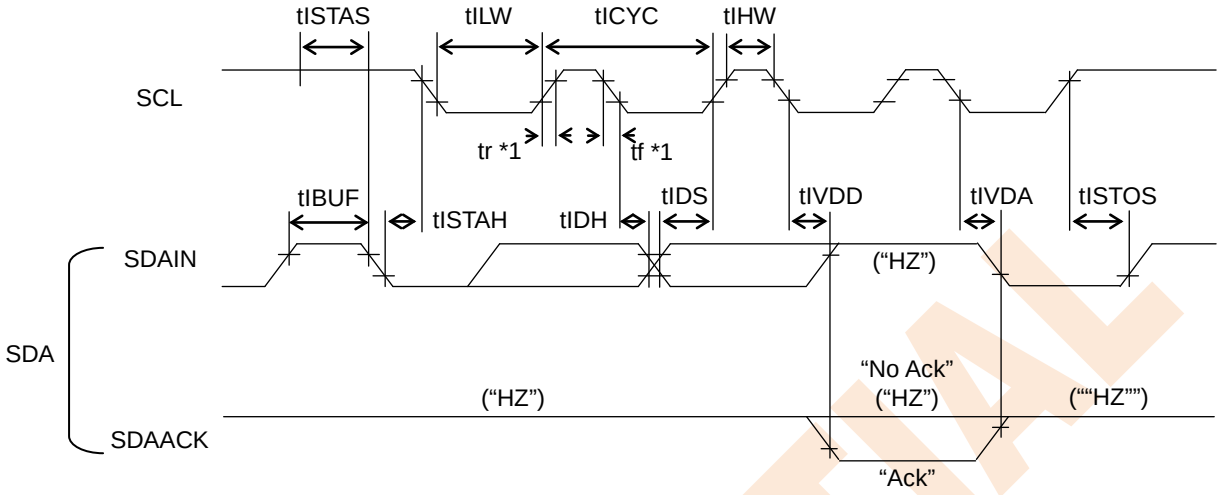


Figure 11.2 2-wire Serial Interface (I2C-Bus Compliant)

Table 11.2 2-wire Serial Interface (I2C-Bus Compliant)

VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105℃

Parameter	Signal	Symbol	Conditions	Specification		Unit
				Min.	Max.	
Serial Clock Cycle	SCL	tICYC	–	(2500) (TBD)	–	ns
SCL_L Pulse Width	SCL	tILW	–	(1300) (TBD)	–	
SCL_H Pulse Width	SCL	tIHW	–	(600) (TBD)	–	
Bus Free Time	SDA	tIBUF	–	(1300) (TBD)	–	
Setup Time for START Condition	SDA	tISTAS	–	(600) (TBD)	–	
Hold Time for START Condition	SDA	tISTAH	–	(600) (TBD)	–	
Setup Time for STOP Condition	SDA	tISTOS	–	(600) (TBD)	–	
Data Setup Time	SDA	tIDS	–	(100) (TBD)	–	
Data Hold Time	SDA	tIDH	–	(0) (TBD)	–	
Data Valid Time *2	SDA	tIVDD	–	–	(900) (TBD)	
Data Valid Acknowledge Time *3	SDA	tIVDA	–	–	(900) (TBD)	

**1: tr + tf = tICYC – (tILW + tIHW)*
**2: The data valid time is the time until releasing SDA line by the master device (MPU).*
**3: The data valid acknowledge time is the time until releasing SDA line by the SDAACK signal of this IC.*
**4: All timing specifications are specified based on the voltage level at 20% and 80% of the VDD.*

11.3 I/O Timing of Display Timing Signal

11.3.1 Output Timing

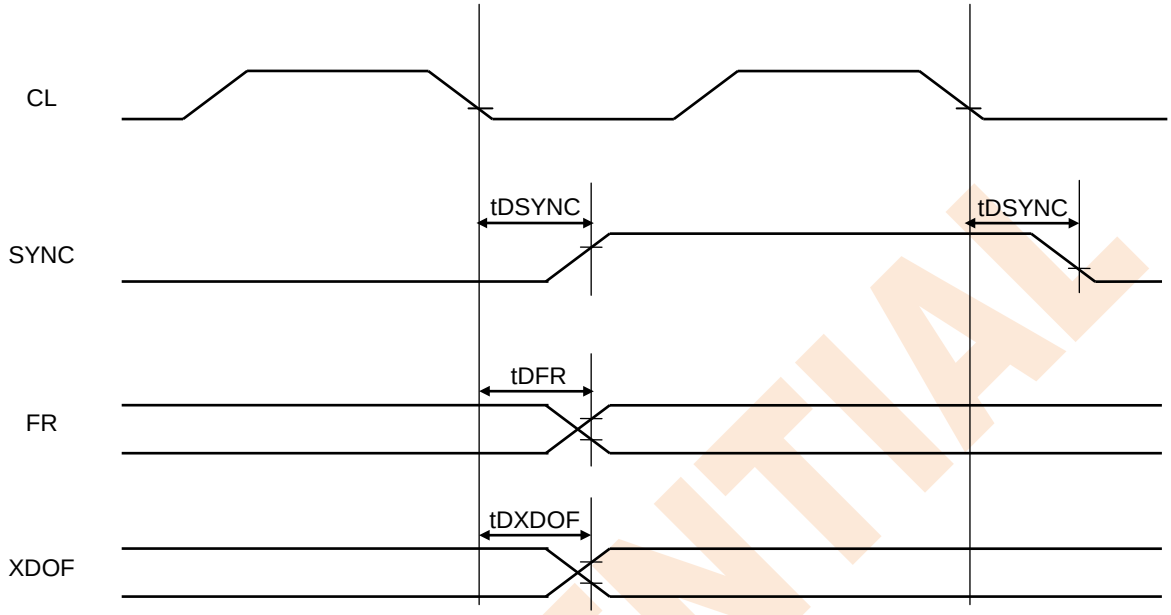


Figure 11.3 Output Timing of Display Control

**1: All timing specifications when switching the outputs are specified based on the voltage level at 10% and 90% of the VDD.*

Table 11.3 Output Timing (CLS=H: In case of using Built-in Oscillator Output for Display Clock)

VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105℃

Parameter	Signal	Symbol	Conditions	Specification		Unit
				Min.	Max.	
SYNC Delay Time	SYNC	tDSYNC	Cload=50pF	(TBD)	(TBD)	ns
FR Delay Time	FR	tDFR		(TBD)	(TBD)	
XDOF Delay Time	XDOF	tDXDOF		(TBD)	(TBD)	

Table 11.4 Output Timing (CLS=L: In case of using External Clock Input for Display Clock)

VSS＝0V, VDD＝2.7 to 5.5V, Ta＝－40 to 105℃

Parameter	Signal	Symbol	Conditions	Specification		Unit
				Min.	Max.	
SYNC Delay Time	SYNC	tDSYNC	Cload=50pF	(TBD)	(TBD)	ns
FR Delay Time	FR	tDFR		(TBD)	(TBD)	
XDOF Delay Time	XDOF	tDXDOF		(TBD)	(TBD)	

11.3.2 Input Timing

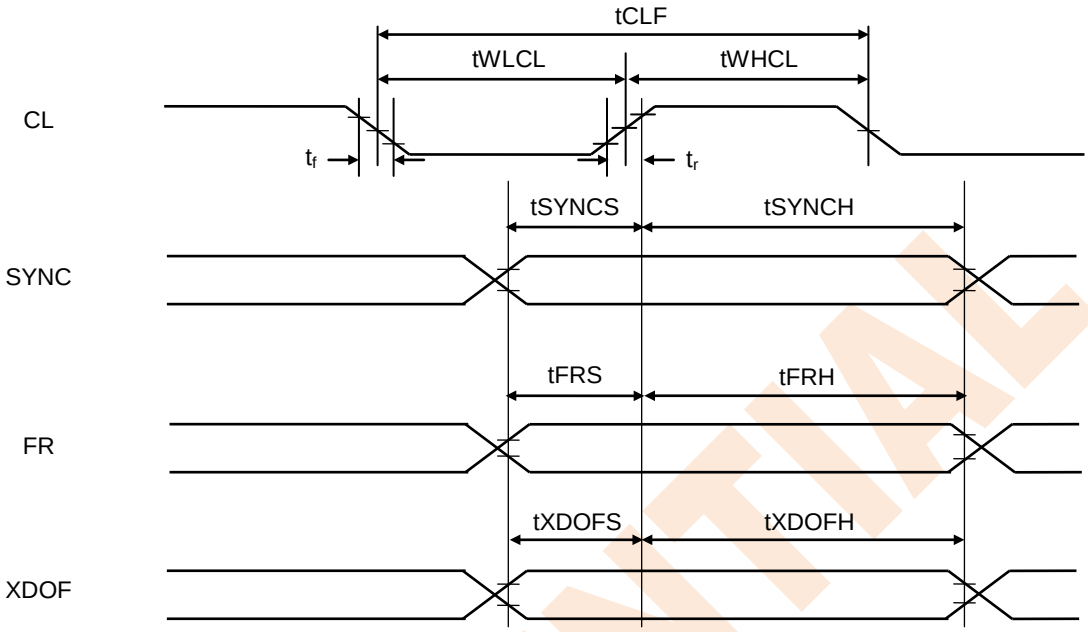


Figure 11.4 Input Timing

Table 11.5 Input Timing

VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105℃

Parameter	Signal	Symbol	Conditions	Specification		Unit
				Min.	Max.	
Input Clock Duty Ratio *2	CL	tCLD	–	(TBD)	(TBD)	%
Input Clock Cycle 1 *1	CL	tCLF	Single chip Operation	(TBD)	–	ns
Input Clock LOW Pulse Width 1 *1	CL	tWLCL		(TBD)	–	
Input Clock HIGH Pulse Width 1 *1	CL	tWHCL		(TBD)	–	
Input Clock Cycle 2 *1	CL	tCLF	Master/Slave Operation	(TBD)	–	
Input Clock LOW Pulse Width 2 *1	CL	tWLCL		(TBD)	–	
Input Clock HIGH Pulse Width 2 *1	CL	tWHCL		(TBD)	–	
SYNC Setup Time	SYNC	tSYNCS	–	(TBD)	–	
SYNC Hold Time	SYNC	tSYNCH	–	(TBD)	–	
FR Setup Time	FR	tFRS	–	(TBD)	–	
FR Hold Time	FR	tFRH	–	(TBD)	–	
XDOF Setup Time	XDOF	tXDOFS	–	(TBD)	–	
XDOF Hold Time	XDOF	tXDOFH	–	(TBD)	–	

*1: The timing specifications of tCLF, tWLC and tWHCL are specified based on the voltage level at 50% of the VDD.
The other timing specifications except tCLF, tWLC and tWHCL are specified based on the voltage level at 20% and 80% of the VDD.
*2: The duty ratio of CL is specified by tCLD = tWHCL / tCLF ×100％ or tCLD = tWLCL / tCLF ×100％.

11.4 Reset Timing

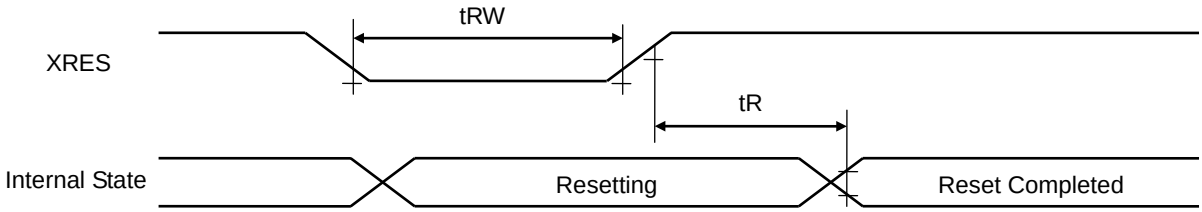


Figure 11.5 Reset Timing

Table 11.6 Reset Timing

VSS=VST=MV3=0V, VDD=2.7 to 5.5V, Ta=-40 to 105℃

Parameter	Signal	Symbol	Conditions	Specification		Unit
				Min.	Max.	
Reset Time	XRES	tR	–	–	10	µs
Reset LOW Pulse Width	XRES	tRW	–	10	–	

**1: All timing specifications are specified based on the voltage level at 20% and 80% of the VDD.*

11.5 ERR Output Timing

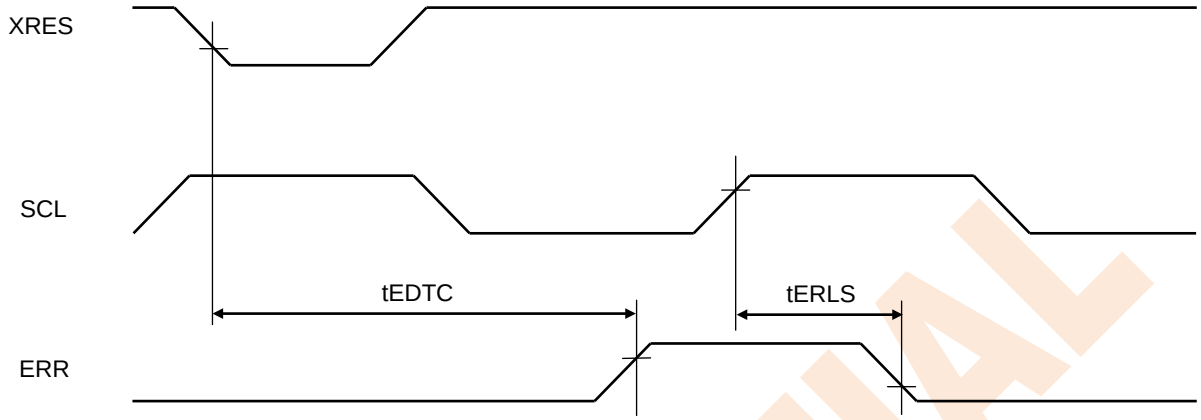


Figure 11.6 ERR Output Timing

Table 11.7 ERR Output Timing

VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105℃

Parameter	Signal	Symbol	Conditions	Specification		Unit
				Min.	Max.	
ERR Detect Time *2	ERR	tEDTC	Cload=50pF	–	(1) (TBD)	µs
ERR Release Time *3	ERR	tERLS		–	(1) (TBD)	

**1: All timing specifications are specified based on the voltage level at 20% and 80% of the VDD.*
**2: The ERR detect time is the time until the ERR pin turns to "H" level after XRES="L" as an example.*
**3: The ERR release time is the time until the ERR pin output returns to "L" level after 3 commands (DISOFF, PWROFF and PSOFF) input..*

12. LCD Panel Connection Examples

12.1 Single Chip Configuration

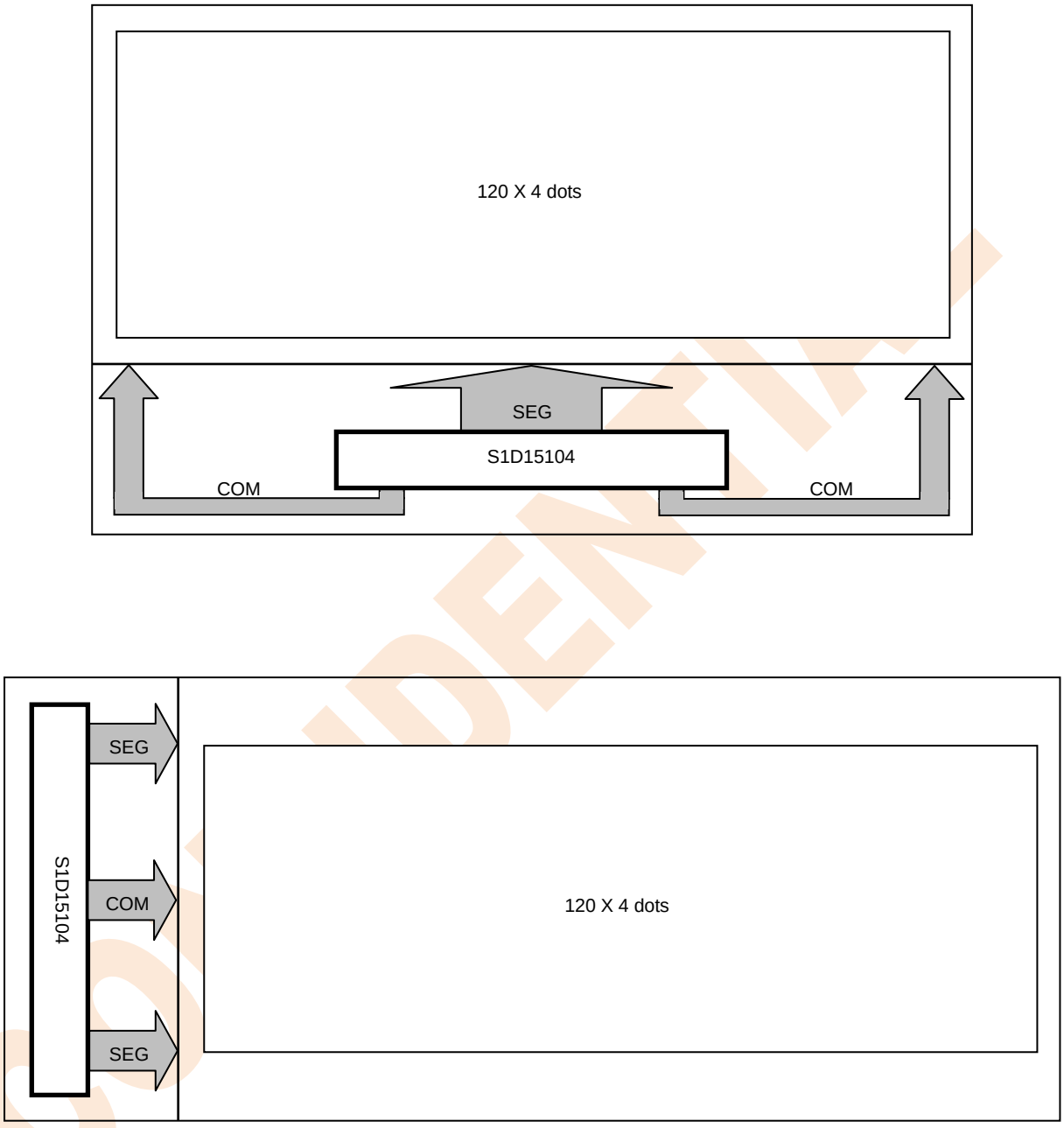


Figure 12.1 Connection Example in case of Single Chip Configuration

12.2 2-Chip Configuration

The resolution can be extended by connecting 2 chips of this IC.

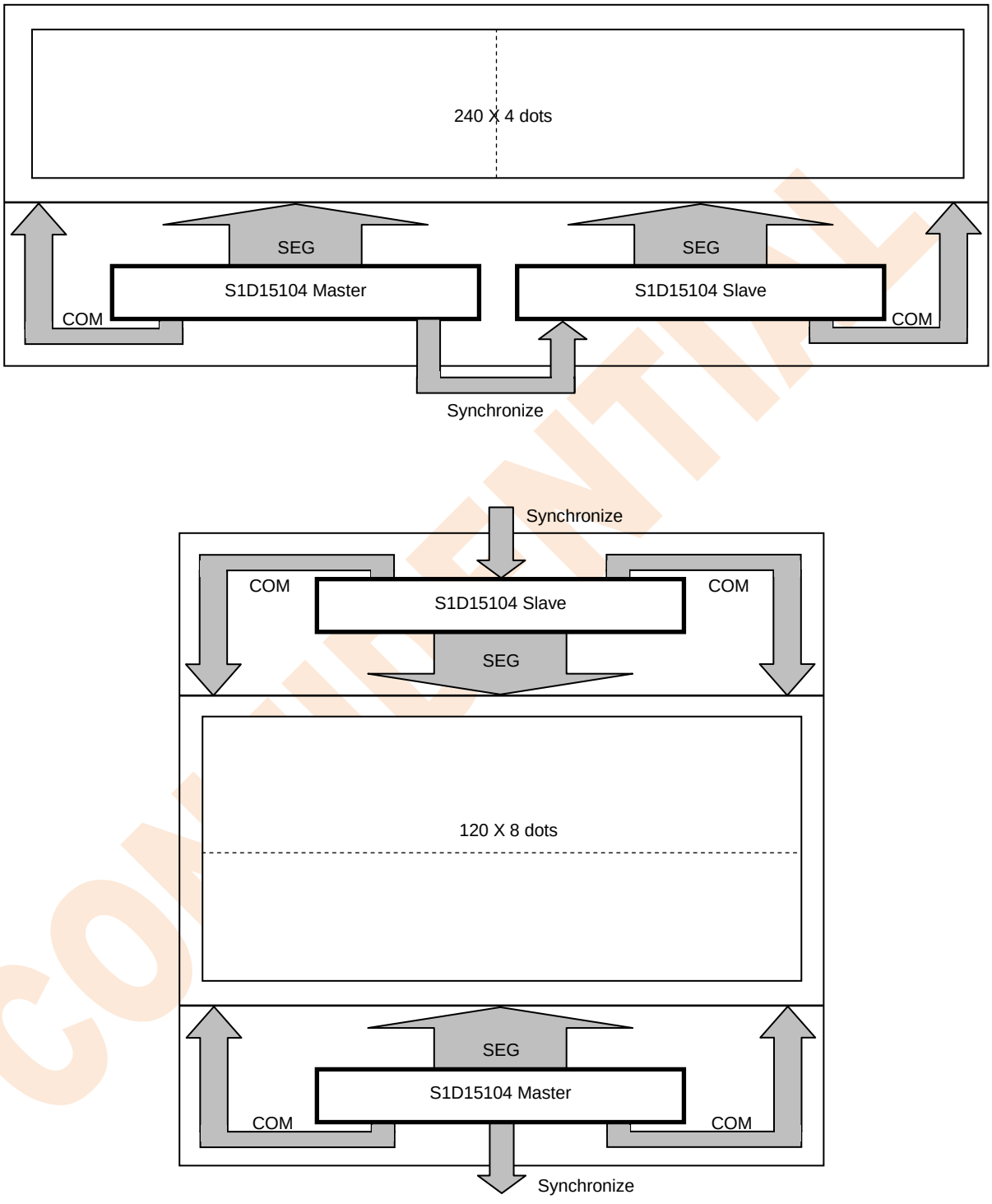


Figure 12.2 Connection Example in case of 2-Chip Configuration

13. Precautions

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(1) Do not expose the ICs to the light before they are mounted in the board design and IC mounting phases.
(2) Also, do not expose the ICs to the light in the inspection phase.
(3) Take all surfaces, top, bottom and sides, of the IC chip into consideration when blocking out light.

Revision History

Attachment-1

Rev. No.	Date	Page	Category	Contents
Rev 0.1	2016/11/18	All	New	Newly established.

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