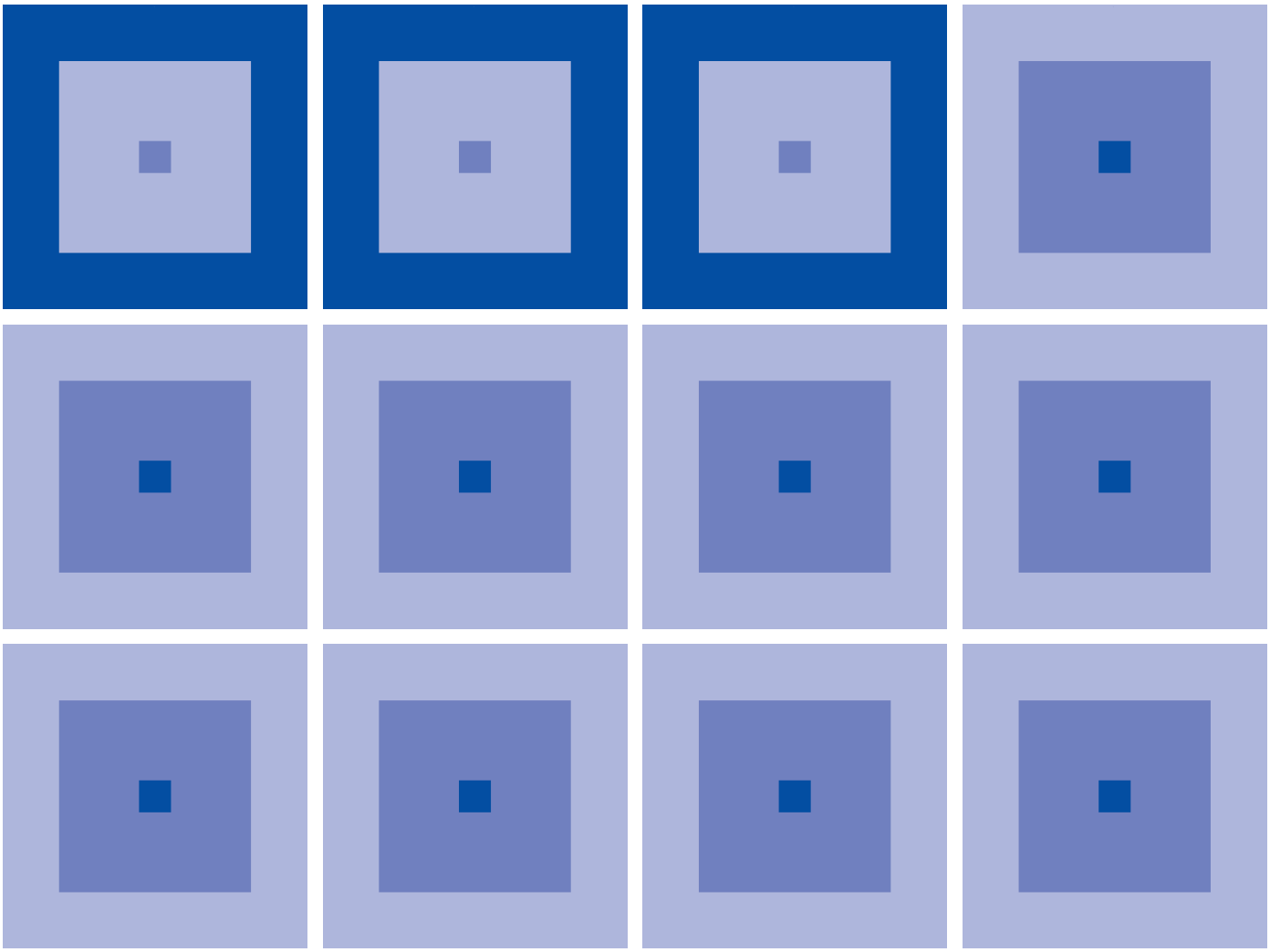
EPSON

S1D15715 Series
Technical Manual



SEIKO EPSON CORPORATION

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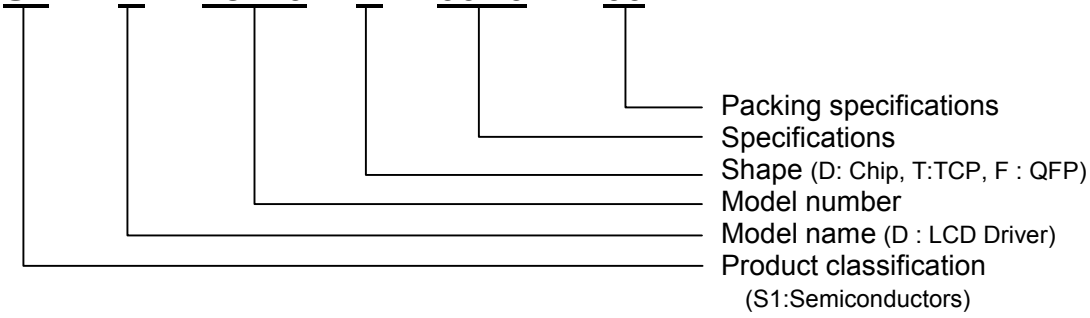
Configuration of product number

●DEVICES

S1 D 15710 D 00B0 00



General Rule

When using these development specifications, note the following points:

1. The contents of the Development Specifications are subject to change without notice for improvement.
2. The Development Specifications do not guarantee or grant license of any industrial property or other rights to any person.
   Examples of application shown in the Development Specifications are intended for your better understanding of the product. We are not responsible for any problems about circuit arising out of their use.
   "Large" or "Small" in the characteristics refers to the relationship on a numbered line.
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When using the semiconductor chip, note the following points:

IC handling notes on light:

As a semiconductor chip is principally identical to a solar cell, its performance may change if exposed to bright light.

Therefore, the IC may malfunction if exposed to light.

Since the measures against light is incomplete, perform the following to boards and products that the IC is implemented.

(1) Design and mount the IC so that it is not exposed to light during actual operation.
(2) During the inspection process, the environment design must made be made so that the IC is not exposed to light.
(3) Make sure that the front, back and the sides of the IC chip are not exposed to light.

CONTENTS

1. DESCRIPTION

S1D15715 Series is a single-chip liquid crystal display (=LCD) driver for dot matrix LCDs that can be connected directly to a microprocessor (=MPU) bus.
It accepts 8-bit parallel or serial display data from a MPU, stores it in an on-chip display data RAM (=DDRAM), and generates a LCD drive signal independent of the MPU clock.
The use of the on-chip DDRAM of 33×102 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip DDRAM bits offer high flexibility in graphic display.
The S1D15715 is equipped with 17 circuits of common output and 102 circuits of segment output, and displays in 17×102 dots. The S1D15716 is equipped with 9 circuits of common output and 102 circuits of segment output, and displays in 9×102 dots. The S1D15717 is equipped with 33 circuits of common output and 102 circuits of segment output, and displays in33×102 dots.
S1D15715 series can perform reading and writing of the display data RAM with minimum power consumption since it does not require external operation clock. Moreover, since the series is equipped with low-power-consumption and highly efficient LCD driver power supply and display clock CR oscillation circuit, it is suited for display system of the high-performance handy device and in-vehicle device.

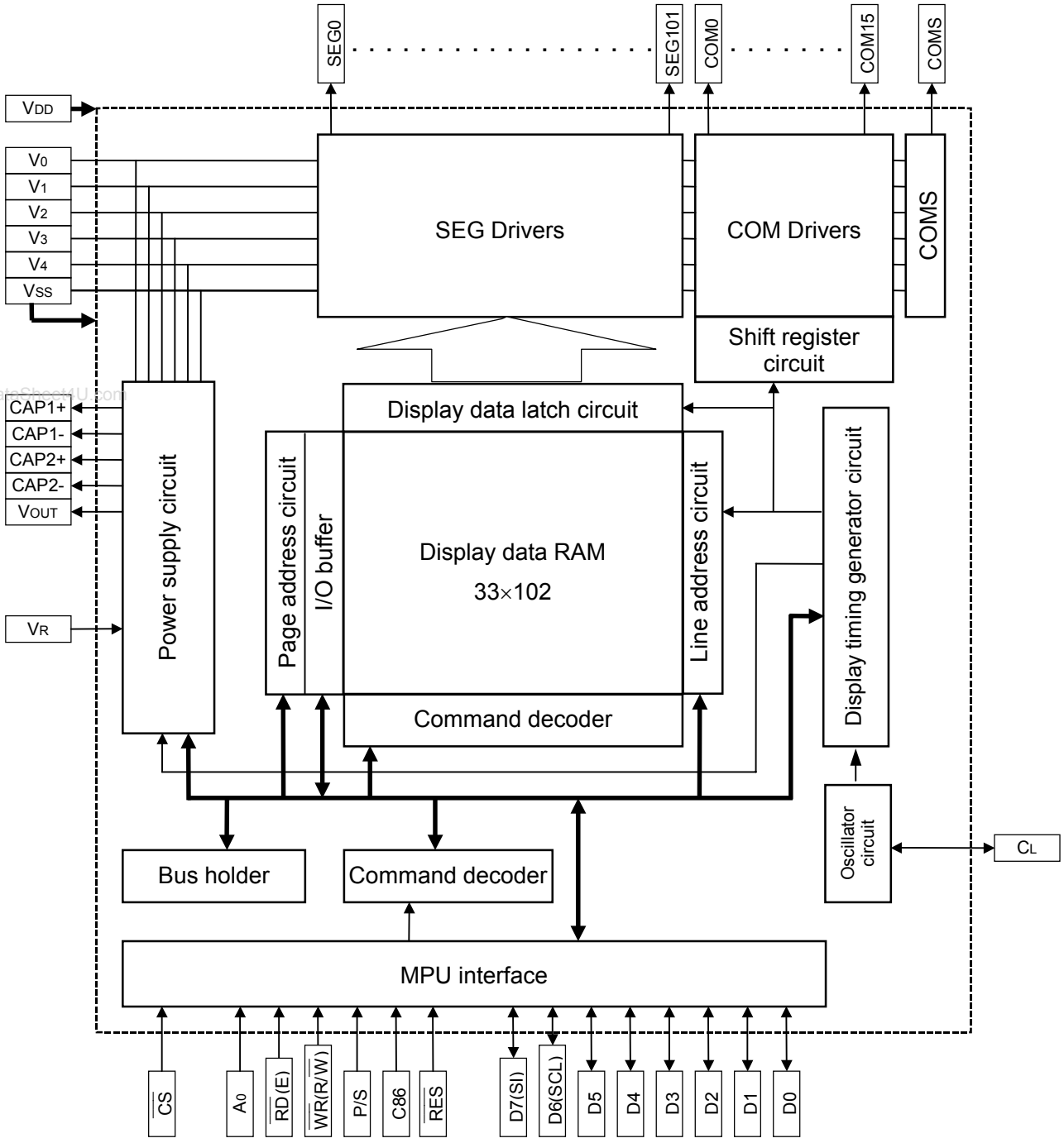
2. FEATURES

- Direct display of RAM data through the display data RAM.
  RAM bit data: "1" Non-illuminated
  "0" Illuminated
  (during normal display)
- RAM capacity 33×102=3366 bits
- Display driver circuits
  Common output of 17, segment output of 102: S1D15715
  Common output of 9, segment output of 102: S1D15716
  Common output of 33, segment output of 102: S1D15717
- High-speed 8-bit MPU interface (The chip can be connected directly to the 80-series MPUs and the 68-series MPUs)
- High-speed serial interface are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, display all points ON/OFF, electronic volume, Read modify write, segment driver direction select, power saver, common output direction select, V_0 voltage regulator internal resistor ratio set, n-line inversion drive
- Liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of Double/Triple, where the step-up voltage reference power supply can be input externally)
  High-accuracy voltage regulator circuit (Thermal gradient -0.05%/ºC)
  V_0 voltage regulator resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Low power consumption
- Power supply
  Logic power supply voltage : V_{DD}-V_{SS}=1.8V to 5.5V
  Liquid crystal drive power supply : V_0-V_{SS}=4.5V to 9.0V
- Wide range of operating temperatures : -40 to +85°C
- CMOS process
- Shipping forms : bare chip
- The chip is not designed for resistance to light or resistance to radiation.

Series Specifications

Product Name	Duty	COM Dr	SEG Dr	Bias	V_{REG} Temperature	Shipping Forms
S1D15715D00B000	1/17	17	102	1/6, 1/5	-0.05%/°C	Bare Chip
S1D15716D00B000	1/9	9				
S1D15717D00B000	1/33	33				

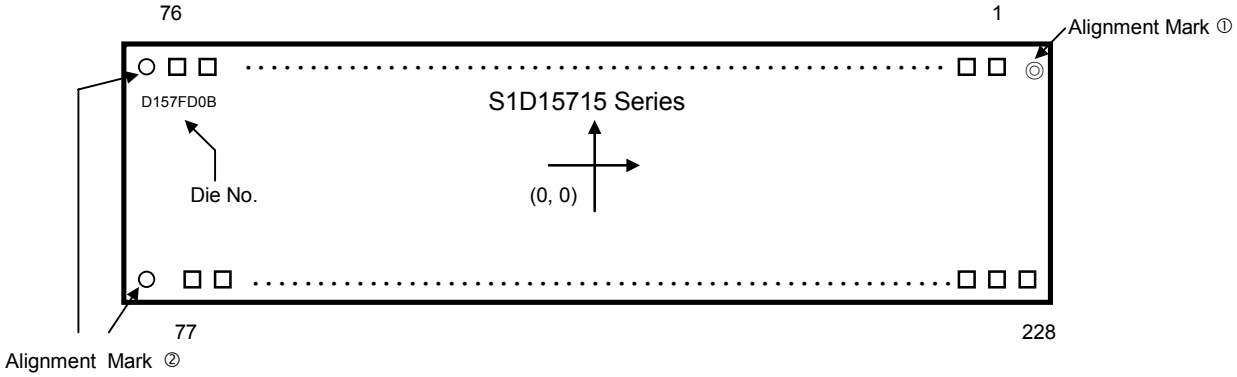
3. BLOCK DIAGRAM (S1D15715 1/17 Duty)



* The COM pins for S1D15716 and S1D15717 differ.
  S1D15715 COM0 to COM15, COMS
  S1D15716 COM0 to COM7, COMS
  S1D15717 COM0 to COM32, COMS

4. PIN ASSIGNMENT

4.1 Chip Specification



		Size			Unit
		X		Y	
Chip Size		8.13	×	1.99	mm
Chip Thickness		0.625			mm
Bump Pitch		50 (Min.)			μm
Bump Size	PAD No.1 to 76	71	×	86	μm
	PAD No.77 to 78	86	×	117	μm
	PAD No.79 to 226	33	×	117	μm
	PAD No.227 to 228	86	×	117	μm
Bump Height		17 (Typ.)			μm

4.2 Alignment marks

Alignment coordinates:

① (3924.1, 842.7) μm

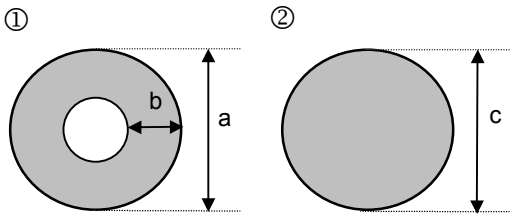
② (-3918.6, -842.7) μm

Mark size:

a =69.5μm

b =29.6μm

c =80.8μm



・ S1D15715 Series Pad Center Coordinates

Unit: μm

PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y
1	(NC)	3809	843	51	VOUT	-1401	843	101	(NC)	-2600	-828
2	$\overline{RES}$	3713		52	VOUT	-1497		102	SEG0	-2550	
3	$\overline{CS}$	3618		53	VSS	-1593		103	SEG1	-2499	
4	VSS	3522		54	VR	-1689		104	SEG2	-2449	
5	VSS	3426		55	V0	-1785		105	SEG3	-2398	
6	VSS	3330		56	V0	-1881		106	SEG4	-2348	
7	$\overline{WR}$(R/$\overline{W}$)	3234		57	V1	-1977		107	SEG5	-2297	
8	$\overline{RD}$(E)	3138		58	V1	-2072		108	SEG6	-2247	
9	TEST0	3042		59	V2	-2168		109	SEG7	-2196	
10	TEST1	2946		60	V2	-2264		110	SEG8	-2146	
11	VSS	2850		61	V3	-2360		111	SEG9	-2095	
12	TEST2	2755		62	V3	-2456		112	SEG10	-2045	
13	TEST3	2659		63	V4	-2552		113	SEG11	-1994	
14	$\overline{RES}$	2563		64	V4	-2648		114	SEG12	-1944	
15	$\overline{CS}$	2467		65	VOUT	-2744		115	SEG13	-1893	
16	VSS	2371		66	CAP2+	-2839		116	SEG14	-1843	
17	VSS	2275		67	CAP2+	-2935		117	SEG15	-1792	
18	VSS	2179		68	CAP2+	-3031		118	SEG16	-1742	
19	VDD	2083		69	CAP2-	-3127		119	SEG17	-1691	
20	CL	1988		70	CAP2-	-3223		120	SEG18	-1641	
21	A0	1892		71	CAP2-	-3319		121	SEG19	-1590	
22	D7(SI)	1796		72	CAP1+	-3415		122	SEG20	-1540	
23	D7(SI)	1700		73	CAP1+	-3511		123	SEG21	-1489	
24	D6(SCL)	1604		74	CAP1-	-3606		124	SEG22	-1439	
25	D6(SCL)	1508		75	CAP1-	-3702		125	SEG23	-1388	
26	D5	1412		76	(NC)	-3798	▼	126	SEG24	-1338	
27	D4	1316		77	(NC)	-3909	-828	127	SEG25	-1287	
28	D3	1221		78	(NC)	-3797		128	SEG26	-1237	
29	D2	1125		79	COMS	-3711		129	SEG27	-1187	
30	D1	1029		80	COM0	-3661		130	SEG28	-1136	
31	D0	933		81	COM1	-3610		131	SEG29	-1086	
32	VDD	837		82	COM2	-3560		132	SEG30	-1035	
33	VDD	741		83	COM3	-3509		133	SEG31	-985	
34	VDD	645		84	COM4	-3459		134	SEG32	-934	
35	P/S	549		85	COM5	-3408		135	SEG33	-884	
36	C86	453		86	COM6	-3358		136	SEG34	-833	
37	VSS	358		87	COM7	-3307		137	SEG35	-783	
38	TEST4	262		88	COM8	-3257		138	SEG36	-732	
39	TEST5	106		89	COM9	-3206		139	SEG37	-682	
40	TEST6	-49		90	COM10	-3156		140	SEG38	-631	
41	TEST7	-204		91	COM11	-3105		141	SEG39	-581	
42	TEST8	-360		92	COM12	-3055		142	SEG40	-530	
43	TEST9	-515		93	COM13	-3004		143	SEG41	-480	
44	TEST10	-671		94	COM14	-2954		144	SEG42	-429	
45	VSS	-826		95	COM15	-2903		145	SEG43	-379	
46	VSS	-922		96	COMS	-2853		146	SEG44	-328	
47	VSS	-1018		97	(NC)	-2802		147	SEG45	-278	
48	VSS	-1114		98	(NC)	-2752		148	SEG46	-227	
49	VSS	-1209		99	(NC)	-2701		149	SEG47	-177	
50	VSS	-1305	▼	100	(NC)	-2651	▼	150	SEG48	-126	▼

Unit: μm

PAD No.	Pin Name	X	Y
151	SEG49	-76	-828
152	SEG50	-25	
153	SEG51	25	
154	SEG52	76	
155	SEG53	126	
156	SEG54	177	
157	SEG55	227	
158	SEG56	278	
159	SEG57	328	
160	SEG58	379	
161	SEG59	429	
162	SEG60	480	
163	SEG61	530	
164	SEG62	581	
165	SEG63	631	
166	SEG64	682	
167	SEG65	732	
168	SEG66	783	
169	SEG67	833	
170	SEG68	884	
171	SEG69	934	
172	SEG70	985	
173	SEG71	1035	
174	SEG72	1086	
175	SEG73	1136	
176	SEG74	1187	
177	SEG75	1237	
178	SEG76	1287	
179	SEG77	1338	
180	SEG78	1388	
181	SEG79	1439	
182	SEG80	1489	
183	SEG81	1540	
184	SEG82	1590	
185	SEG83	1641	
186	SEG84	1691	
187	SEG85	1742	
188	SEG86	1792	
189	SEG87	1843	
190	SEG88	1893	
191	SEG89	1944	
192	SEG90	1994	
193	SEG91	2045	
194	SEG92	2095	
195	SEG93	2146	
196	SEG94	2196	
197	SEG95	2247	
198	SEG96	2297	
199	SEG97	2348	
200	SEG98	2398	▼

Pad No.	Pin Name	X	Y
201	SEG99	2449	-828
202	SEG100	2499	
203	SEG101	2550	
204	(NC)	2600	
205	(NC)	2651	
206	(NC)	2701	
207	(NC)	2752	
208	(NC)	2802	
209	COMS	2853	
210	COM15	2903	
211	COM14	2954	
212	COM13	3004	
213	COM12	3055	
214	COM11	3105	
215	COM10	3156	
216	COM9	3206	
217	COM8	3257	
218	COM7	3307	
219	COM6	3358	
220	COM5	3408	
221	COM4	3459	
222	COM3	3509	
223	COM2	3560	
224	COM1	3610	
225	COM0	3661	
226	COMS	3711	
227	(NC)	3797	
228	(NC)	3909	▼

・ S1D15716 Series Pad Center Coordinates

Unit: μm

PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y
1	(NC)	3809	843	51	VOUT	-1401	843	101	(NC)	-2600	-828
2	$\overline{RES}$	3713		52	VOUT	-1497		102	SEG0	-2550	
3	$\overline{CS}$	3618		53	VSS	-1593		103	SEG1	-2499	
4	VSS	3522		54	VR	-1689		104	SEG2	-2449	
5	VSS	3426		55	V0	-1785		105	SEG3	-2398	
6	VSS	3330		56	V0	-1881		106	SEG4	-2348	
7	$\overline{WR}$(R/$\overline{W}$)	3234		57	V1	-1977		107	SEG5	-2297	
8	$\overline{RD}$(E)	3138		58	V1	-2072		108	SEG6	-2247	
9	TEST0	3042		59	V2	-2168		109	SEG7	-2196	
10	TEST1	2946		60	V2	-2264		110	SEG8	-2146	
11	VSS	2850		61	V3	-2360		111	SEG9	-2095	
12	TEST2	2755		62	V3	-2456		112	SEG10	-2045	
13	TEST3	2659		63	V4	-2552		113	SEG11	-1994	
14	$\overline{RES}$	2563		64	V4	-2648		114	SEG12	-1944	
15	$\overline{CS}$	2467		65	VOUT	-2744		115	SEG13	-1893	
16	VSS	2371		66	CAP2+	-2839		116	SEG14	-1843	
17	VSS	2275		67	CAP2+	-2935		117	SEG15	-1792	
18	VSS	2179		68	CAP2+	-3031		118	SEG16	-1742	
19	VDD	2083		69	CAP2-	-3127		119	SEG17	-1691	
20	CL	1988		70	CAP2-	-3223		120	SEG18	-1641	
21	A0	1892		71	CAP2-	-3319		121	SEG19	-1590	
22	D7(SI)	1796		72	CAP1+	-3415		122	SEG20	-1540	
23	D7(SI)	1700		73	CAP1+	-3511		123	SEG21	-1489	
24	D6(SCL)	1604		74	CAP1-	-3606		124	SEG22	-1439	
25	D6(SCL)	1508		75	CAP1-	-3702		125	SEG23	-1388	
26	D5	1412		76	(NC)	-3798	▼	126	SEG24	-1338	
27	D4	1316		77	(NC)	-3909	-828	127	SEG25	-1287	
28	D3	1221		78	(NC)	-3797		128	SEG26	-1237	
29	D2	1125		79	COMS	-3711		129	SEG27	-1187	
30	D1	1029		80	COM0	-3661		130	SEG28	-1136	
31	D0	933		81	COM0	-3610		131	SEG29	-1086	
32	VDD	837		82	COM1	-3560		132	SEG30	-1035	
33	VDD	741		83	COM1	-3509		133	SEG31	-985	
34	VDD	645		84	COM2	-3459		134	SEG32	-934	
35	P/S	549		85	COM2	-3408		135	SEG33	-884	
36	C86	453		86	COM3	-3358		136	SEG34	-833	
37	VSS	358		87	COM3	-3307		137	SEG35	-783	
38	TEST4	262		88	COM4	-3257		138	SEG36	-732	
39	TEST5	106		89	COM4	-3206		139	SEG37	-682	
40	TEST6	-49		90	COM5	-3156		140	SEG38	-631	
41	TEST7	-204		91	COM5	-3105		141	SEG39	-581	
42	TEST8	-360		92	COM6	-3055		142	SEG40	-530	
43	TEST9	-515		93	COM6	-3004		143	SEG41	-480	
44	TEST10	-671		94	COM7	-2954		144	SEG42	-429	
45	VSS	-826		95	COM7	-2903		145	SEG43	-379	
46	VSS	-922		96	COMS	-2853		146	SEG44	-328	
47	VSS	-1018		97	(NC)	-2802		147	SEG45	-278	
48	VSS	-1114		98	(NC)	-2752		148	SEG46	-227	
49	VSS	-1209		99	(NC)	-2701		149	SEG47	-177	
50	VSS	-1305	▼	100	(NC)	-2651	▼	150	SEG48	-126	▼

Unit: μm

PAD No.	Pin Name	X	Y
151	SEG49	-76	-828
152	SEG50	-25	
153	SEG51	25	
154	SEG52	76	
155	SEG53	126	
156	SEG54	177	
157	SEG55	227	
158	SEG56	278	
159	SEG57	328	
160	SEG58	379	
161	SEG59	429	
162	SEG60	480	
163	SEG61	530	
164	SEG62	581	
165	SEG63	631	
166	SEG64	682	
167	SEG65	732	
168	SEG66	783	
169	SEG67	833	
170	SEG68	884	
171	SEG69	934	
172	SEG70	985	
173	SEG71	1035	
174	SEG72	1086	
175	SEG73	1136	
176	SEG74	1187	
177	SEG75	1237	
178	SEG76	1287	
179	SEG77	1338	
180	SEG78	1388	
181	SEG79	1439	
182	SEG80	1489	
183	SEG81	1540	
184	SEG82	1590	
185	SEG83	1641	
186	SEG84	1691	
187	SEG85	1742	
188	SEG86	1792	
189	SEG87	1843	
190	SEG88	1893	
191	SEG89	1944	
192	SEG90	1994	
193	SEG91	2045	
194	SEG92	2095	
195	SEG93	2146	
196	SEG94	2196	
197	SEG95	2247	
198	SEG96	2297	
199	SEG97	2348	
200	SEG98	2398	▼

PAD No.	Pin Name	X	Y
201	SEG99	2449	-828
202	SEG100	2499	
203	SEG101	2550	
204	(NC)	2600	
205	(NC)	2651	
206	(NC)	2701	
207	(NC)	2752	
208	(NC)	2802	
209	COMS	2853	
210	COM7	2903	
211	COM7	2954	
212	COM6	3004	
213	COM6	3055	
214	COM5	3105	
215	COM5	3156	
216	COM4	3206	
217	COM4	3257	
218	COM3	3307	
219	COM3	3358	
220	COM2	3408	
221	COM2	3459	
222	COM1	3509	
223	COM1	3560	
224	COM0	3610	
225	COM0	3661	
226	COMS	3711	
227	(NC)	3797	
228	(NC)	3909	▼

・ S1D15717 Series Pad Center Coordinates

Unit: μm

PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y
1	(NC)	3809	843	51	VOUT	-1401	843	101	(NC)	-2600	-828
2	$\overline{RES}$	3713		52	VOUT	-1497		102	SEG0	-2550	
3	$\overline{CS}$	3618		53	VSS	-1593		103	SEG1	-2499	
4	VSS	3522		54	VR	-1689		104	SEG2	-2449	
5	VSS	3426		55	V0	-1785		105	SEG3	-2398	
6	VSS	3330		56	V0	-1881		106	SEG4	-2348	
7	$\overline{WR}$(R/$\overline{W}$)	3234		57	V1	-1977		107	SEG5	-2297	
8	$\overline{RD}$(E)	3138		58	V1	-2072		108	SEG6	-2247	
9	TEST0	3042		59	V2	-2168		109	SEG7	-2196	
10	TEST1	2946		60	V2	-2264		110	SEG8	-2146	
11	VSS	2850		61	V3	-2360		111	SEG9	-2095	
12	TEST2	2755		62	V3	-2456		112	SEG10	-2045	
13	TEST3	2659		63	V4	-2552		113	SEG11	-1994	
14	$\overline{RES}$	2563		64	V4	-2648		114	SEG12	-1944	
15	$\overline{CS}$	2467		65	VOUT	-2744		115	SEG13	-1893	
16	VSS	2371		66	CAP2+	-2839		116	SEG14	-1843	
17	VSS	2275		67	CAP2+	-2935		117	SEG15	-1792	
18	VSS	2179		68	CAP2+	-3031		118	SEG16	-1742	
19	VDD	2083		69	CAP2-	-3127		119	SEG17	-1691	
20	CL	1988		70	CAP2-	-3223		120	SEG18	-1641	
21	A0	1892		71	CAP2-	-3319		121	SEG19	-1590	
22	D7(SI)	1796		72	CAP1+	-3415		122	SEG20	-1540	
23	D7(SI)	1700		73	CAP1+	-3511		123	SEG21	-1489	
24	D6(SCL)	1604		74	CAP1-	-3606		124	SEG22	-1439	
25	D6(SCL)	1508		75	CAP1-	-3702		125	SEG23	-1388	
26	D5	1412		76	(NC)	-3798	▼	126	SEG24	-1338	
27	D4	1316		77	(NC)	-3909	-828	127	SEG25	-1287	
28	D3	1221		78	(NC)	-3797		128	SEG26	-1237	
29	D2	1125		79	COMS	-3711		129	SEG27	-1187	
30	D1	1029		80	COM0	-3661		130	SEG28	-1136	
31	D0	933		81	COM1	-3610		131	SEG29	-1086	
32	VDD	837		82	COM2	-3560		132	SEG30	-1035	
33	VDD	741		83	COM3	-3509		133	SEG31	-985	
34	VDD	645		84	COM4	-3459		134	SEG32	-934	
35	P/S	549		85	COM5	-3408		135	SEG33	-884	
36	C86	453		86	COM6	-3358		136	SEG34	-833	
37	VSS	358		87	COM7	-3307		137	SEG35	-783	
38	TEST4	262		88	COM8	-3257		138	SEG36	-732	
39	TEST5	106		89	COM9	-3206		139	SEG37	-682	
40	TEST6	-49		90	COM10	-3156		140	SEG38	-631	
41	TEST7	-204		91	COM11	-3105		141	SEG39	-581	
42	TEST8	-360		92	COM12	-3055		142	SEG40	-530	
43	TEST9	-515		93	COM13	-3004		143	SEG41	-480	
44	TEST10	-671		94	COM14	-2954		144	SEG42	-429	
45	VSS	-826		95	COM15	-2903		145	SEG43	-379	
46	VSS	-922		96	COMS	-2853		146	SEG44	-328	
47	VSS	-1018		97	(NC)	-2802		147	SEG45	-278	
48	VSS	-1114		98	(NC)	-2752		148	SEG46	-227	
49	VSS	-1209		99	(NC)	-2701		149	SEG47	-177	
50	VSS	-1305	▼	100	(NC)	-2651	▼	150	SEG48	-126	▼

Unit: μm

PAD No.	Pin Name	X	Y
151	SEG49	-76	-828
152	SEG50	-25	
153	SEG51	25	
154	SEG52	76	
155	SEG53	126	
156	SEG54	177	
157	SEG55	227	
158	SEG56	278	
159	SEG57	328	
160	SEG58	379	
161	SEG59	429	
162	SEG60	480	
163	SEG61	530	
164	SEG62	581	
165	SEG63	631	
166	SEG64	682	
167	SEG65	732	
168	SEG66	783	
169	SEG67	833	
170	SEG68	884	
171	SEG69	934	
172	SEG70	985	
173	SEG71	1035	
174	SEG72	1086	
175	SEG73	1136	
176	SEG74	1187	
177	SEG75	1237	
178	SEG76	1287	
179	SEG77	1338	
180	SEG78	1388	
181	SEG79	1439	
182	SEG80	1489	
183	SEG81	1540	
184	SEG82	1590	
185	SEG83	1641	
186	SEG84	1691	
187	SEG85	1742	
188	SEG86	1792	
189	SEG87	1843	
190	SEG88	1893	
191	SEG89	1944	
192	SEG90	1994	
193	SEG91	2045	
194	SEG92	2095	
195	SEG93	2146	
196	SEG94	2196	
197	SEG95	2247	
198	SEG96	2297	
199	SEG97	2348	
200	SEG98	2398	▼

PAD No.	Pin Name	X	Y
201	SEG99	2449	-828
202	SEG100	2499	
203	SEG101	2550	
204	(NC)	2600	
205	(NC)	2651	
206	(NC)	2701	
207	(NC)	2752	
208	(NC)	2802	
209	COMS	2853	
210	COM31	2903	
211	COM30	2954	
212	COM29	3004	
213	COM28	3055	
214	COM27	3105	
215	COM26	3156	
216	COM25	3206	
217	COM24	3257	
218	COM23	3307	
219	COM22	3358	
220	COM21	3408	
221	COM20	3459	
222	COM19	3509	
223	COM18	3560	
224	COM17	3610	
225	COM16	3661	
226	COMS	3711	
227	(NC)	3797	
228	(NC)	3909	▼

5. PIN DESCRIPTION

5.1 Power supply pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>V_{DD}</td><td>Supply</td><td>Internal logic power supply and internal power circuit power supply.
Connect to MPU power pin V_{CC}.</td><td>4</td></tr>
<tr><td>V_{SS}</td><td>Supply</td><td>0V pin connected to the system ground.</td><td>15</td></tr>
<tr><td>V_0,V_1,V_2,
V_3,V_4</td><td>Supply</td><td>Multi-level, LCD drive power supply pins.
The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operational amplifier and applied.
The voltages need to be specified based on the V_{SS} to establish the following relationship:
$V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$
When power circuit turns on, the following voltages are applied to V_1 to V_4 from the internal power circuit.
<table>
<tr><td></td><td colspan="2">S1D15715/16/17</td></tr>
<tr><td></td><td>1/5 bias</td><td>1/6 bias</td></tr>
<tr><td>V_1</td><td>4/5 • V_0</td><td>5/6 • V_0</td></tr>
<tr><td>V_2</td><td>3/5 • V_0</td><td>4/6 • V_0</td></tr>
<tr><td>V_3</td><td>2/5 • V_0</td><td>2/6 • V_0</td></tr>
<tr><td>V_4</td><td>1/5 • V_0</td><td>1/6 • V_0</td></tr>
</table>
</td><td>10
(2 each)</td></tr>
</table>

5.2 LCD power supply circuit pins

Pin name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP1-pins.	2
CAP1-	O	Boosting capacitor negative connection pin. Capacitor is connected across CAP1+pins.	2
CAP2+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP2-pins.	3
CAP2-	O	Boosting capacitor negative connection pin. Capacitor is connected across CAP2+pins.	3
V_{OUT}	O	Booster output. Capacitor is connected across V_{SS} or V_{DD}.	3
V_R	I	Voltage regulator pin. Provides V_0 to V_{SS} voltage using split resistors. Operable only when the built-in resistor for V_0 adjustment is not used. [V_0 resistance ratio is (D_2, D_1, D_0)=(1.1.1)] This pin is disabled when the built-in resistor for V_0 adjustment is used. The pin must be open in this case.	1

5.3 System bus connection pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0
(SI)
(SCL)</td><td>I/O</td><td>8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit MPU data bus.
When the serial interface is selected (P/S=LOW);
D7: Serial data input (SI)
D6: Serial clock input (SCL)
D0 to D5 switches to high impedance status.
When chip select is in non-active status, D0 to D7 switches to high impedance status.</td><td>10</td></tr>
<tr><td>A0</td><td>I</td><td>Normally the lowest order bit of the MPU address bus is connected to discriminate data/commands.
A0=HIGH: The data on D7 to D0 is display data.
A0=LOW: The data on D7 to D0 is control data.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal. When $\overline{CS}$=LOW, the MPU interface of the IC becomes active and the input/output of data/command is enabled.</td><td>2</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Initialized by setting $\overline{RES}$ to LOW.
Reset operation is performed at the signal level.</td><td>2</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>○When connected to an 80-series MPU; This is active LOW.
This pin connects the $\overline{RD}$ signal of the 80-series MPU. While the signal is LOW, S1D15715 series data bus is in an output status.
○When connected to an 68-series MPU; This is active HIGH.
This is used as an enable clock input pin of the 68-series MPU.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>○ When connected to an 80-series MPU; This is active LOW.
This pin connects the $\overline{WR}$ signal of 80-series MPU.
The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
○ When connected to an 68-series MPU;
This is used as the input pin of the read/write control signal.
R/$\overline{W}$=HIGH: Read
R/$\overline{W}$=LOW: Write</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU interface selection pin.
C86=HIGH: 68-series MPU interface
C86=LOW: 80-series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Serial data input/parallel data input selection pin.
P/S=HIGH: Parallel data input
P/S=LOW: Serial data input
The following applies depending on the P/S status:
<table><tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr><tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$,$\overline{WR}$</td><td>—</td></tr><tr><td>LOW</td><td>A0</td><td>SI(D7)</td><td>Write only</td><td>SCL(D6)</td></tr></table>When P/S=LOW, D5 to D0 switches to high impedance status. D5 to D0 can also be HIGH, LOW or OPEN.
$\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) must always be HIGH or LOW.
In serial mode, no data can be read from DDRAM.</td><td>1</td></tr>
</table>

5.4 LCD driver pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CL</td><td>I</td><td>This pin is used for enabling or disabling the built-in oscillation circuit for the display clock.
CL=HIGH : Built-in oscillation circuit is enabled.
CL=LOW : Built-in oscillation circuit (external input) is disabled.
When inputting external clock, input clock to the CL pin.
When using the built-in oscillation circuit, select CL=HIGH (V_{DD}).</td><td>1</td></tr>
<tr><td>SEG0
to SED101</td><td>O</td><td>These pins output the signal for the segment drive of LCD.
One of V_0, V_2, V_3 and V_{SS} levels is selected depending on a given combination of display RAM data and internal FR signal.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">Internal FR signal</th><th colspan="2">Output voltage</th></tr>
<tr><th>Normal display</th><th>Reversing display</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_0</td><td>V_2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_2</td><td>V_0</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{SS}</td></tr>
</table>
</td><td>102</td></tr>
<tr><td>COM0
to COM15
(COM0
to COM7)
(COM0
to COM31)</td><td>O</td><td>These pins output the signal for the common drive of LCD.
They are branched by the SEL pins as follows.
<table>
<tr><th>Model</th><th>COM</th></tr>
<tr><td>S1D15715</td><td>COM0 to COM15</td></tr>
<tr><td>S1D15716</td><td>COM0 to COM7</td></tr>
<tr><td>S1D15717</td><td>COM0 to COM31</td></tr>
</table>
One of V_0, V_1, V_4 and V_{SS} levels is selected depending on a given combination of scan data and FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_{SS}</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_0</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{SS}</td></tr>
</table>
In case multiple number of the COM pins for the same signal names exist, the same signal will be output from all the pins.</td><td>32
(16)</td></tr>
<tr><td>COMS</td><td>O</td><td>They are COM pins exclusively used for the indicator.
The same signal will be output from all the 4 pins.
They must be made open when not used.</td><td>4</td></tr>
</table>

5.5 Test pins

Pin name	I/O	Description	Number of pins
TEST0 to TEST10	I	These are terminals for IC chip testing. They are set to OPEN.	11

Total: 212 pins

Note and caution

- In case the control signal being transmit from the MPU is at a high impedance, excess current may occur in the inside of the IC.
  Take measures to prevent the input pin from switching to the high impedance status.

6. FUNCTIONAL DESCRIPTION

6.1 MPU interface

6.1.1 Interface type selection

S1D15715 Series can transfer data via 8-bit bi-directional buses (D7 to D0) or via serial data input (SI). Through selecting the P/S pin polarity to HIGH or LOW, it is possible to select either 8-bit parallel data input or serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH: Parallel input	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW: Serial input	$\overline{CS}$	A0	—	—	—	SI	SCL	HZ

—: Must always be HIGH or LOW.
HZ is a high impedance state

6.1.2 Parallel interface

When the parallel interface has been selected (P/S=HIGH), then it is possible to connect directly to either an 80-series MPU or 68-series MPU (as shown in Table 2) by selecting C86 pin to either HIGH or LOW.

Table 2

C86	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH: 68-series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7 to D0
LOW: 80-series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

Moreover, the S1D15715 Series identifies the data bus signal according to A0, $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$) signals, as shown in Table 3.

Table 3

Common	68-series	80-series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	0	1	0	Writes control data (command)

6.1.3 Serial interface

When the serial interface has been selected (P/S=LOW), then when the chip is in active state ($\overline{CS}$=LOW) the serial data input (SI) and the serial clock input (SCL) can be received.
The serial interface consists of an 8-bit shift register and a 3-bit counter.
The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.
The A0 input is used to determine whether the serial data input is display data or command data; when A0=HIGH, the data is display data, and when A0=LOW, then the data is command data.
The A0 input is read and used for detection every 8×n-th rising edge of the serial clock after the chip becomes active.
Fig.1 is a serial interface signal chart.

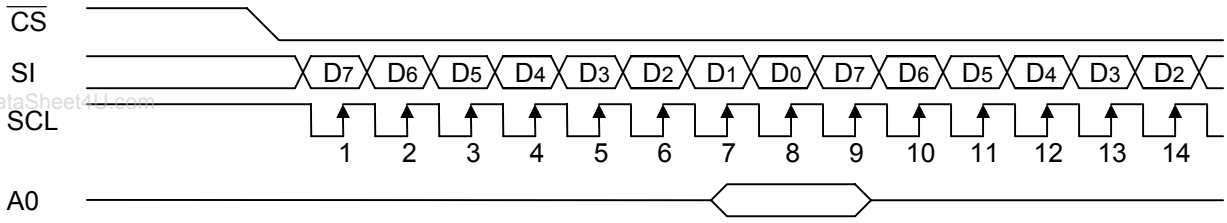


Fig.1

- ※ When the chip is inactive, the shift register and the counter is reset to the initial state.
- ※ Data read is not available as long as the serial interface is selected.
- ※ Reasonable care must be exercised so that SCL signal may not be exposed undesirable effects resulting from, for instance, terminal reflection of wiring or external noises. Before using the signal, it is recommended to test the signal in actual system.

6.1.4 Chip select

The MPU interface (either parallel or serial) is enabled only when $\overline{CS}$=LOW.
When the chip select is inactive, D0 to D7 enter a high impedance state, and A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled. When the serial interface is selected, the shift register and the counter are reset.

6.1.5 Access to DDRAM and internal registers

In accessing the DDRAM and the internal registers of the S1D15715 Series, the MPU is required to satisfy the only cycle time (t_{CYC}), and is not needed to consider the wait time. Accordingly, it is possible to transfer data at higher speed.

In order to realize the higher speed accessing, the S1D15715 Series can perform a type of pipeline processing between LSIs using bus holder of internal data bus when data is sent from/to the MPU.

For example, when the MPU writes data to the DDRAM, once the data is stored in the bus holder, then it is written to the DDRAM before the next data write cycle.

And when the MPU reads the contents of the DDRAM, the first data cycle (dummy read cycle) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle. Thus, there is a certain restriction in the DDRAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read.

A single dummy read must be inserted after address setup and after write cycle.

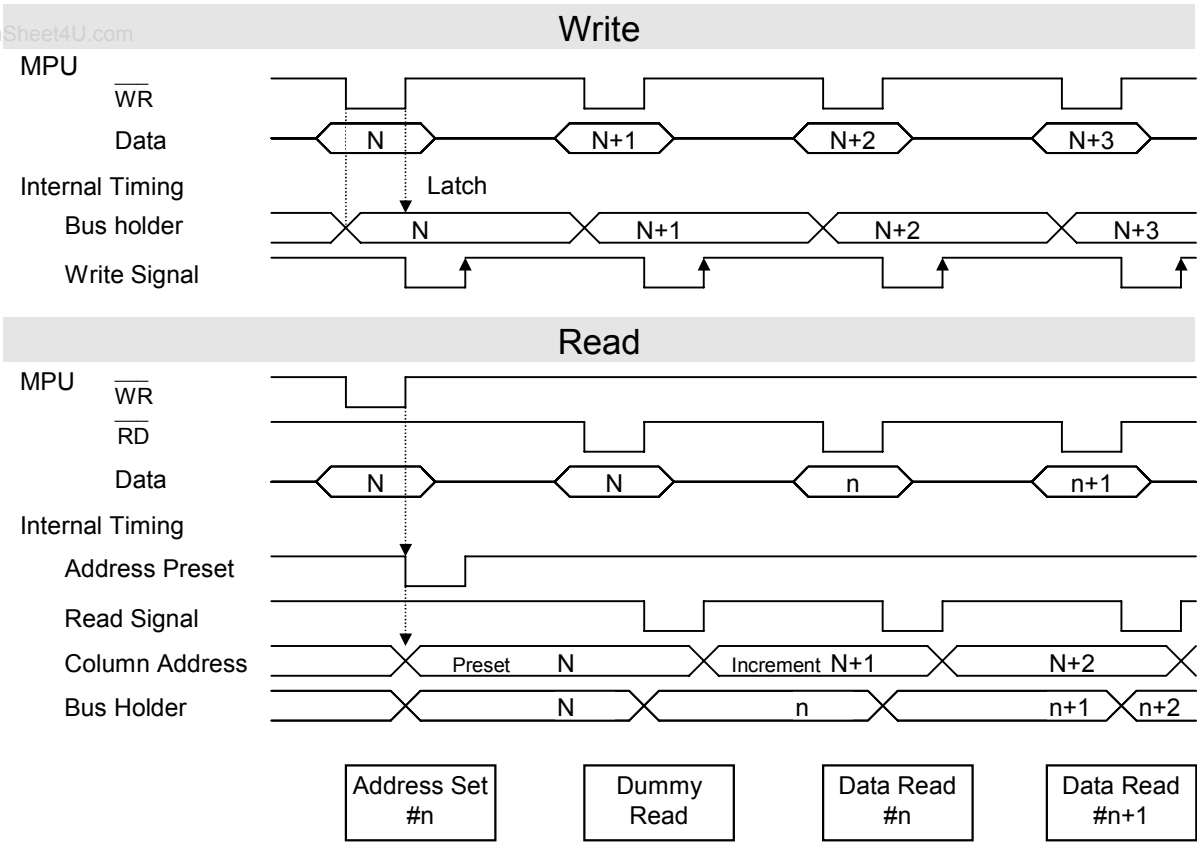


Fig.2

6.2 DDRAM

6.2.1 DDRAM

The DDRAM stores pixel data for LCD. It is in a 33 (4 page×8 bit+1) × 102bit array.
Desired bits can be accessed by specifying page and column addresses.
As is shown in Fig.3, the D7 to D0 display data from the MPU corresponds to the LCD common direction.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver
Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

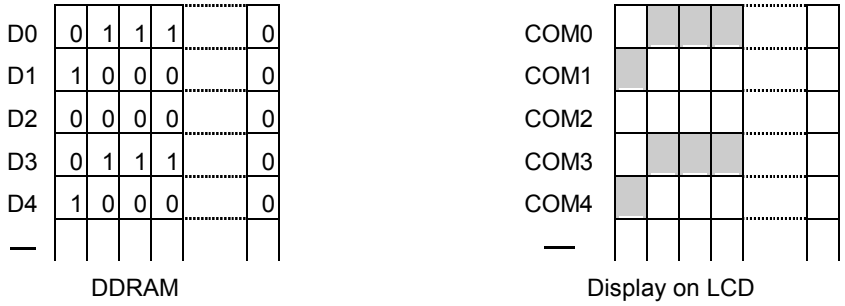


Fig.3

6.2.2 Page address circuit

As shown in Fig.4, the page address of the DDRAM is specified using the page address set command. To access the data using a new page, the page address is respecified.
Page address 4H (D3, D2, D1, D0=0, 1, 1, 0) is DDRAM area dedicate to the indicator, and display data D0 is only valid.

6.2.3 Column address circuit

Designate the column side address of the indication data RAM as shown in Fig.4, using the column address setting command. Since the designated column address increments (+1) each time an indication data read/write command is input, the MPU can make access to the indication data in succession.
Also, as shown in Fig.5, after an access has been made to the final column address (65H), the column address will return to (00H) and the page address will be automatically incremented (by +1).
Thanks to this feature, it is possible to write continuous data being divided between adjoining pages. Furthermore, after accesses have been made to the final addresses of both of the page and column (column=65H and page=3H), both of the column address and the page address returns to (00H).
(The page will not increment to 4H. Therefore, be careful when executing “read modify write” processes).
Also, as shown in Table 4, the correlation between the column address of the indication data RAM and the segment output can be reversed by use of the ADC select command (segment driver direction select command).
Thanks to this feature, IC layout limitations when constituting a LCD module can be lessened.

Table 4

Column Address	00H	01H	02H		63H	64H	65H
Normal Direction	SEG0	SEG1	SEG2		SEG99	SEG100	SEG101
Reverse Direction	SEG101	SEG100	SEG99		SEG2	SEG1	SEG0

Example of S1D15715 (1/17Duty)

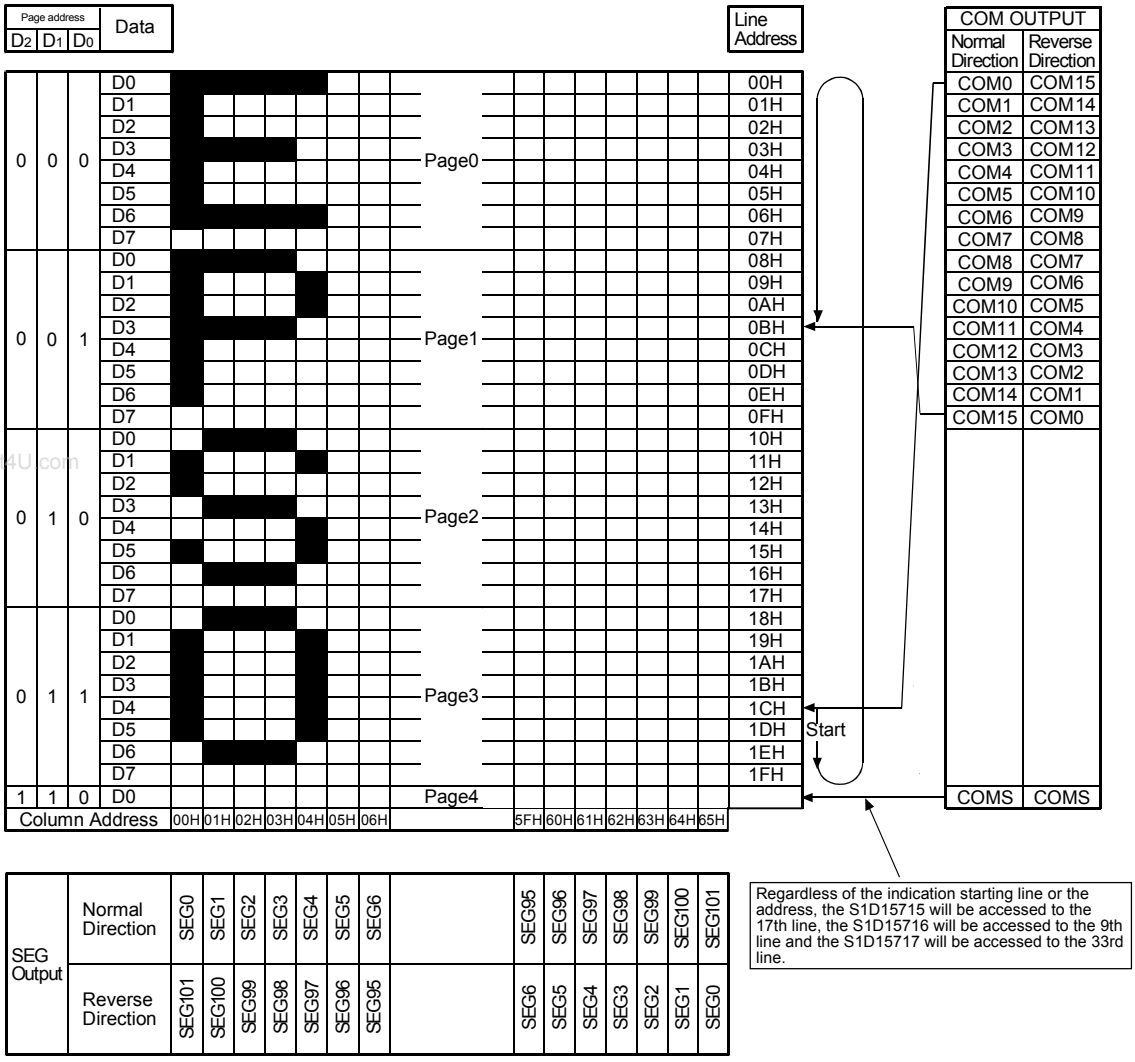


Fig.4

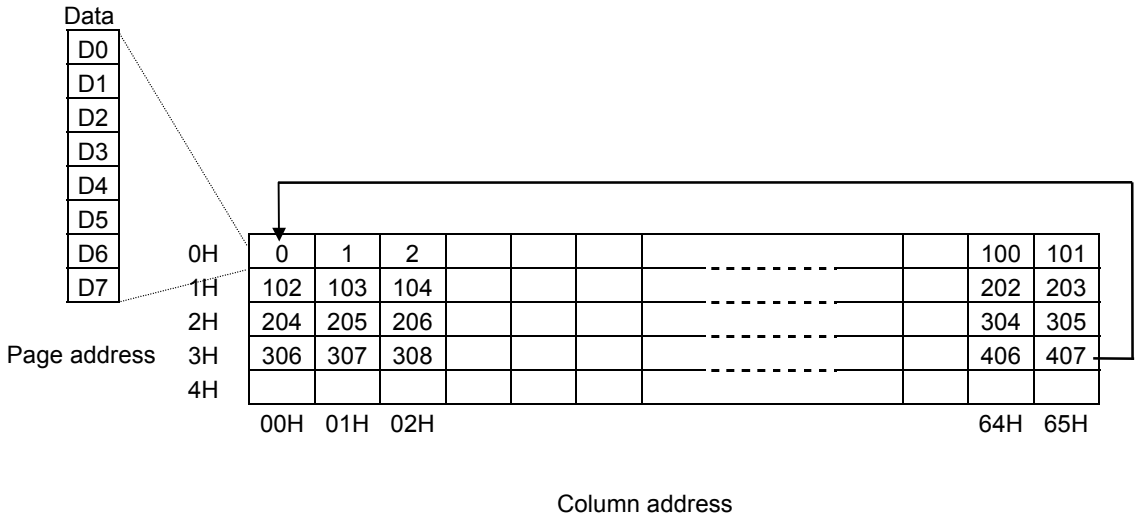


Fig.5

6.2.4 Line address circuit

The line address specifies the line address (as shown in Fig.4) relating to the COM output when the contents of the DDRAM are displayed.
Using the Display start line address set command, the top line is normally selected (In case of the forward common output state, the S1D15715 will designate the COM0 output, in case of the reverse common output state, the S1D15715 will designate the COM15 output, the S1D15716 will designate the COM7 output and the S1D15717 will designate the COM31 output.)
The display area of each driver is secured starting from the specified display start line address in the address incrementing direction as follows: For S1D15715 (1/17Duty), 16 lines and a line of page 4 (total of 17 lines); for S1D15716 (1/9Duty), 8 lines and a line of page 4 (total of 9 lines); for S1D15717 (1/33Duty), 32 lines and a line of page 4 (total of 33 lines).
And Common driver direction select command can be used to reverse the relationship between the DDRAM line address and common output.
For example, as is shown in Table 5, the display start line address corresponds to the COM0 output when the common driver direction is normal, or the COM15 output when common driver direction is reversed (S1D15715).
This allows flexible IC layout during LCD module assembly.
If the display start line address is changed dynamically using the display start line address set command, then screen scrolling and page swapping can be performed.

Table 5 S1D15715 at display start line address=1CH (corresponds to Fig.4)

Line Address	1CH	1DH		1FH	00H		0AH	0BH
Normal Direction	COM0	COM1		COM3	COM4		COM14	COM15
Reverse Direction	COM15	COM14		COM12	COM11		COM1	COM0

6.2.5 Display data latch circuit

The display data latch circuit is a latch which temporarily stores the display data that is output to the LCD driver circuit from the DDRAM.
Display ON/OFF command, Display normal/reverse command, and Display all points ON/OFF command control only the data within the latch, and do not change the data within the DDRAM.

6.3 Oscillation circuit

S1D15715 Series generates display clocks using its built-in CR oscillation circuit.
The built-in oscillation circuit is enabled when CL=HIGH is selected and the power save mode is turned off.
You can stop operation of the CR oscillation circuit by selecting CL=LOW. Display clock can be externally entered via CL pin (when external clock is turned off, CL pin must be placed in LOW).

Table 6

CL	Operation
HIGH	Built-in CR oscillation circuit is enabled.
LOW	Built-in CR oscillation circuit is turned off [display clock is turned off].
Clock input	External clock input mode

Table 7 shows relationship between frequency of external clock (f_{CL}), frequency of built-in oscillation circuit (f_{OSC}) and f_{FR}.
Since CL pin is used for resetting the built-in CR oscillation circuit, it must satisfy the f_{CL} requirements given in the “DC Characteristics”.

Table 7

Item		f_{FR} computation formula
S1D15715 1/17 Duty	When built-in oscillation circuit is used	$f_{FR}=f_{OSC} / (17 \times 16)$
	When external clock input is used	$f_{FR}=f_{CL} / (17 \times 16)$
S1D15716 1/9 Duty	When built-in oscillation circuit is used	$f_{FR}=f_{OSC} / (9 \times 32)$
	When external clock input is used	$f_{FR}=f_{CL} / (9 \times 16)$
S1D15717 1/33 Duty	When built-in oscillation circuit is used	$f_{FR}=f_{OSC} / (33 \times 8)$
	When external clock input is used	$f_{FR}=f_{CL} / (33 \times 16)$

6.4 Display Timing Generator Circuit

The display timing generator circuit generates the timing signal from the display clocks to the line address circuit and the display data latch circuit. Since the read out of the displayed data to the LCD driver circuit is independent from access to the display data RAM from MPU, accessing the display data RAM asynchronously during liquid crystal display will not negatively affect the display such as flickering.
The display timing generator circuit also generates common timing signal and liquid crystal alternating signal from the display clocks. Normally, LCD waveform generates dual-frame driver waveform. However, by setting the data (n-1) to the n-line inversion drive register, n-line inversion driver waveform can be generated. When problem in display quality such as crosstalk exists, it can be solved by using the n-line inversion driver waveform. The number of the lines n to be alternated shall be determined by actually displaying on the LCD.

Dual-frame driver waveform (example of S1D15715 1/17Duty)

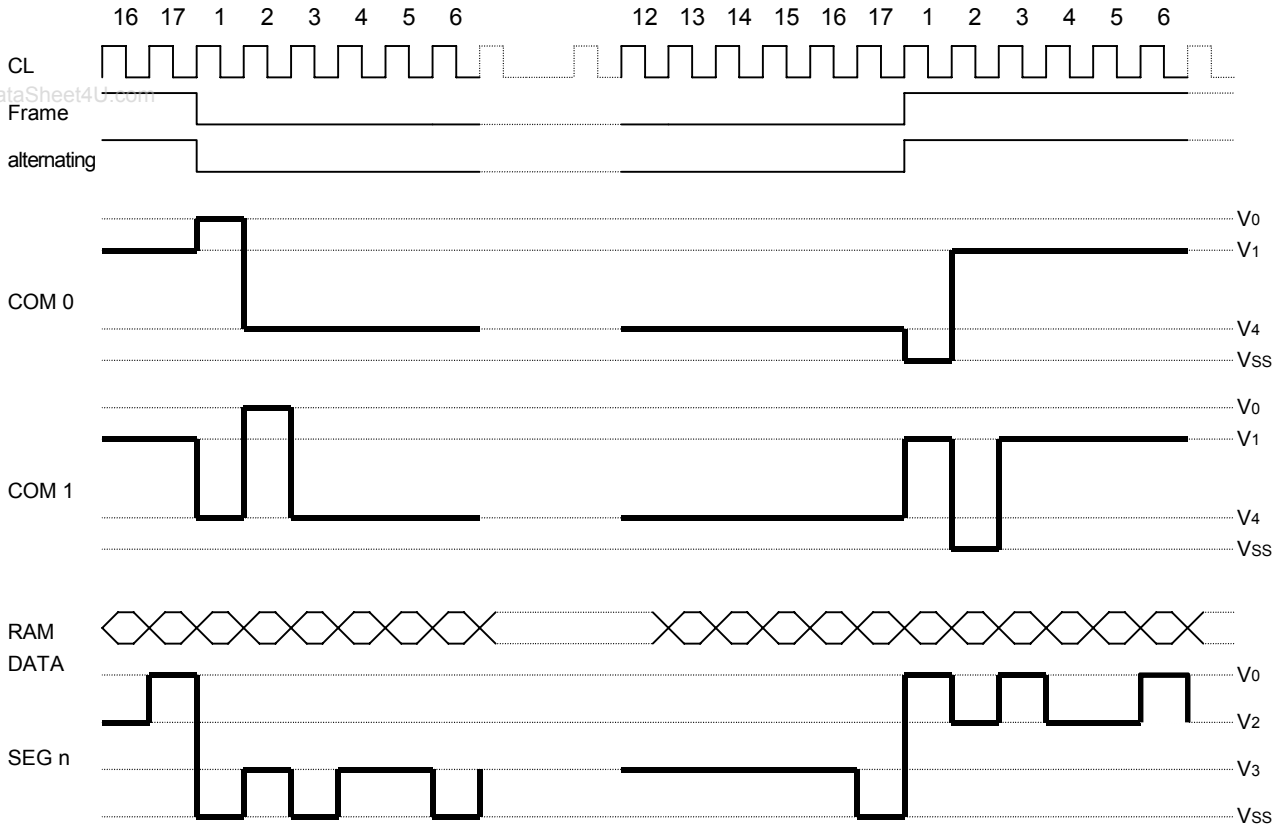


Fig.6

n-line inversion driver waveform (example when S1D15715 1/17Duty n=5 line reverse register is set to 4)

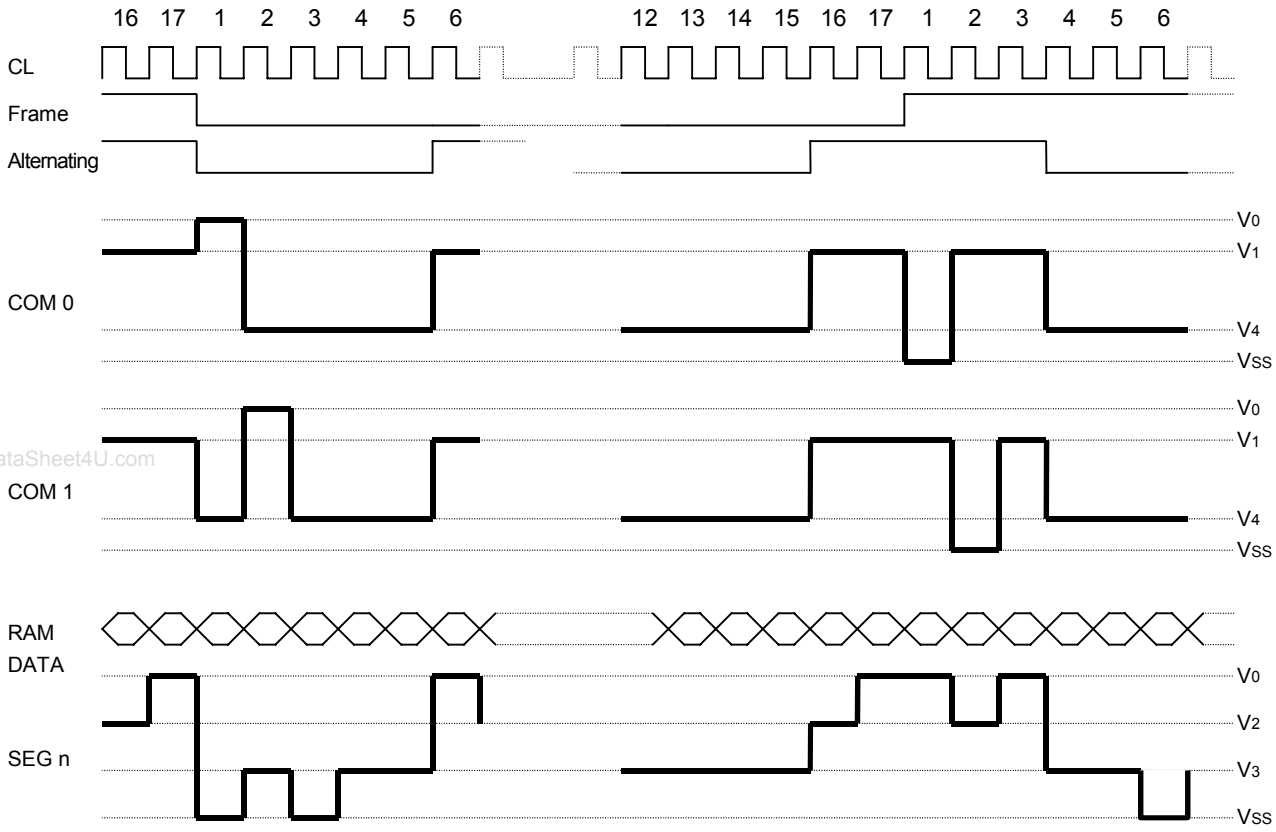


Fig.7

6.5 LCD Driver Circuits

These are multiplexers outputting the LCD panel driving 4-level signal. It outputs LCD driver voltage that corresponds to the combinations of the display data, COM scan signal and LCD AC signal. Fig.8 shows an example of SEG and COM output waveforms.

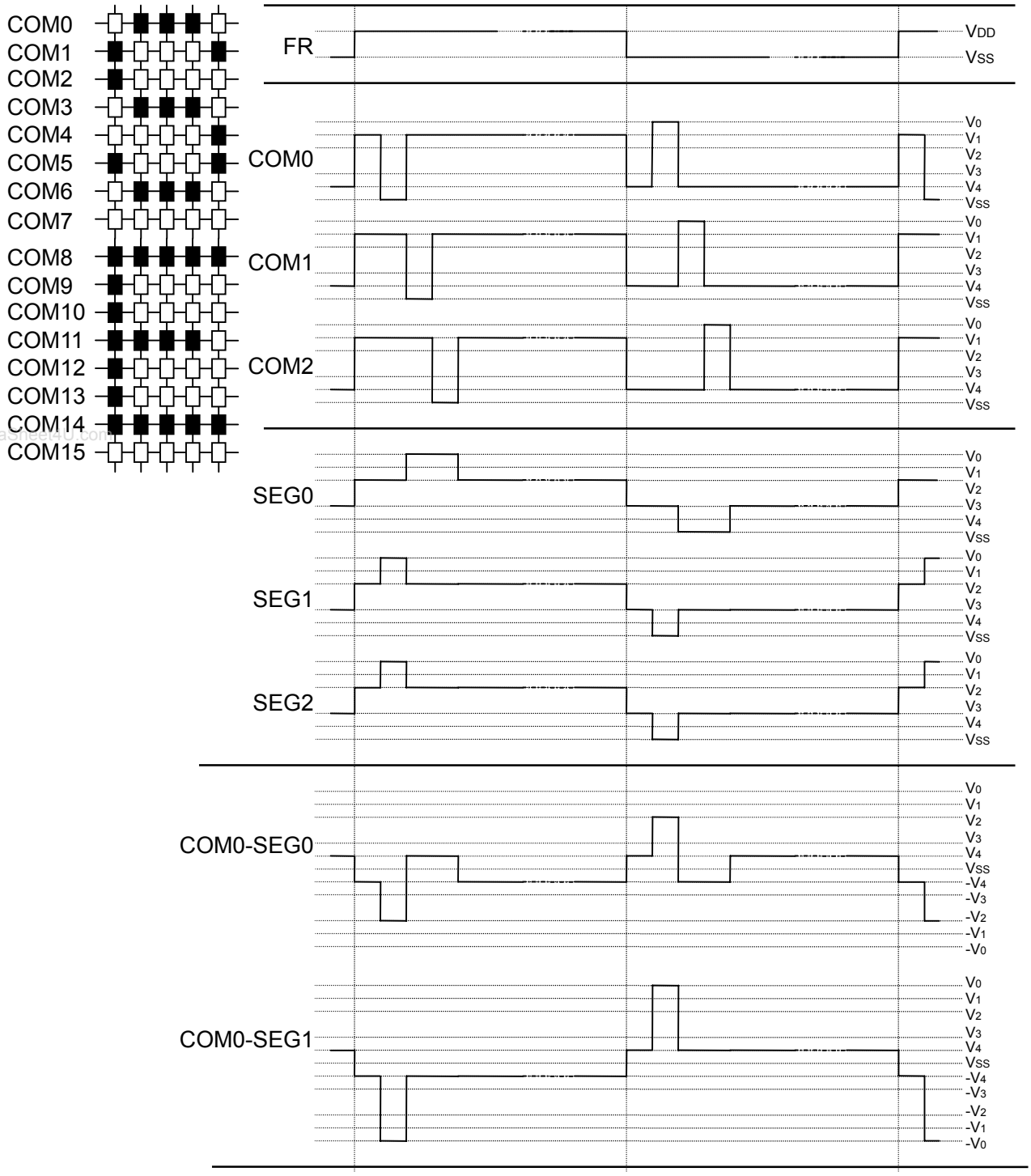


Fig.8

6.6 Power supply circuit

This power supply circuit is a low power supply consumption circuit that generates voltage required for driving liquid crystals, which consists of booster, voltage regulator and voltage follower circuits.
The power supply circuit is controlled by power control set command. Using this command, the booster circuit, the voltage regulator circuit, and the voltage follower circuit can be independently turned ON or OFF. Consequently, the external power supply and part of internal power supply circuit functions can be used simultaneously.
Table 8 lists the functions controllable from 3 bits data of the power control set command. And, Table 9 shows sample combinations of the bits.

Table 8

Item	State	
	"1"	"0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 9

Usage	D2	D1	D0	Booster circuit	V regulator circuit	V/F circuit	External voltage input	Pins on booster circuit
Built-in power supply alone is used	1	1	1	ON	ON	ON	V_{DD}	Used
V regulator circuit and V/F circuits are used	0	1	1	OFF	ON	ON	V_{OUT} ※1	OPEN
V/F circuits alone are used	0	0	1	OFF	OFF	ON	V_0 ※1	OPEN
External power supply alone is used	0	0	0	OFF	OFF	OFF	V_0 to V_4 ※1	OPEN

※ Pins on the booster circuits denote CAP1+, CAP1-, CAP2+, CAP2- pins.
※ Combinations other than the above cannot be used.

6.6.1 Booster circuit

Using the booster circuit, it is possible to Triple/Double boosting of the V_{DD}-V_{SS} voltage level.

Triple boosting:
If capacitor C_1 is inserted between CAP1+ and CAP1-, between CAP2+ and CAP2- and between V_{OUT} and V_{DD}, the potential between V_{DD} and V_{SS} is boosted to triple toward the positive side and it is output at V_{OUT} pin.
Double boosting:
If capacitor C_1 is inserted between CAP1+ and CAP1-, between V_{OUT} and V_{DD}, open CAP2-, and jumper between CAP2+ and V_{OUT}, the potential between V_{DD} and V_{SS} is boosted to double toward the positive side and it is output at V_{OUT} pin.

If the potential between V_{DD} -V_{SS} is 5V±10% and is double boosting, the clamp circuit (approximately 5V) built in the V_{DD} will prevent the V_{OUT} potential from exceeding the absolute maximum rating (10V)

Fig.9 shows the connections and voltage relationships :

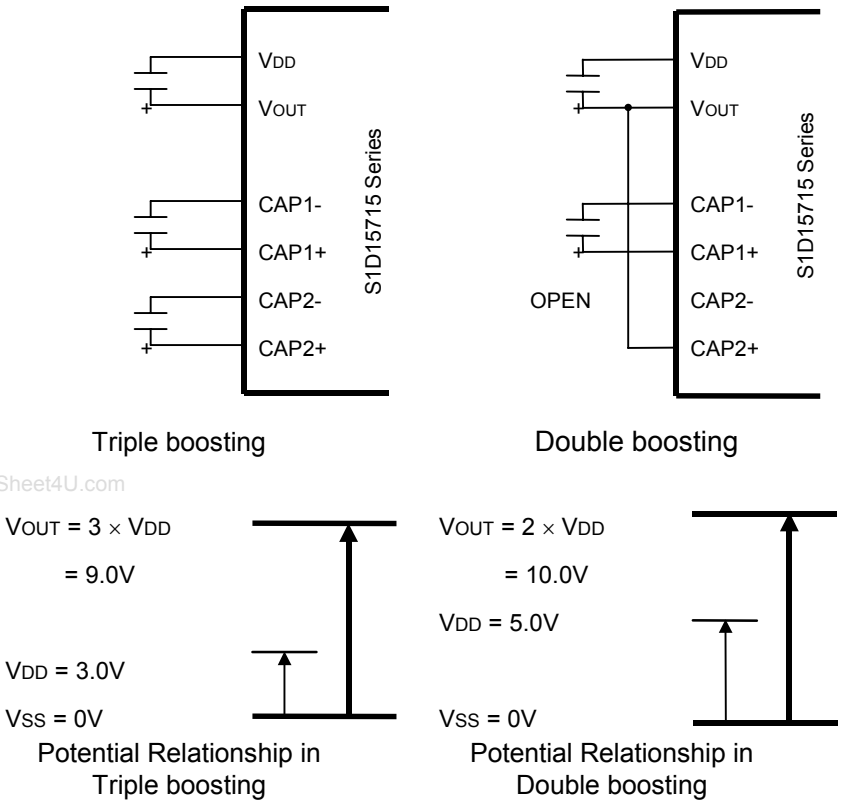


Fig.9

* The Capacitance depends on the load of the LCD panel to be driven. Set a value that LCD driver voltage may be stable (reference value = 1.0 to 4.7μF).

6.6.2 Voltage regulator circuit

The boosting voltage generated at the V_{OUT} pin outputs liquid crystal drive voltage V_0 through the voltage regulator circuit.
Because the S1D15715 Series has the high-accuracy constant voltage source, the 32-level electronic volume function and the internal resistor for the V_0 voltage regulator (= V_0-resistor), it is possible to construct a high-accuracy voltage regulator circuit without external component.

(A) When using the V_0 voltage regulator internal resistor
The internal resistor for the V_0 voltage regulator resistor and the electronic volume function allows for the control of the liquid crystal voltage V_0 through commands only, without the need of adding an external resistor, and allows for the adjustment of the liquid crystal display contrast.
The V_0 voltage can be calculated using the following expression within the range of $|V_0|<|V_{OUT}|$.

$$V_0=(1+Rb/Ra)\cdot V_{EV}$$
$$=(1+ Rb/Ra)\cdot(1-\alpha/200)\cdot V_{REG} \quad \text{(Expression A-1)}$$
$$[V_{EV}=(1-\alpha/200)\cdot V_{REG}]$$

V_{REG} represents the constant voltage source within an IC. Its value at T_a=25°C is constant as shown in Table 10.

Table 10

Model	V_{REG}	Thermal Gradient
S1D15715, S1D15716, S1D15717	1.2V	-0.05%/°C

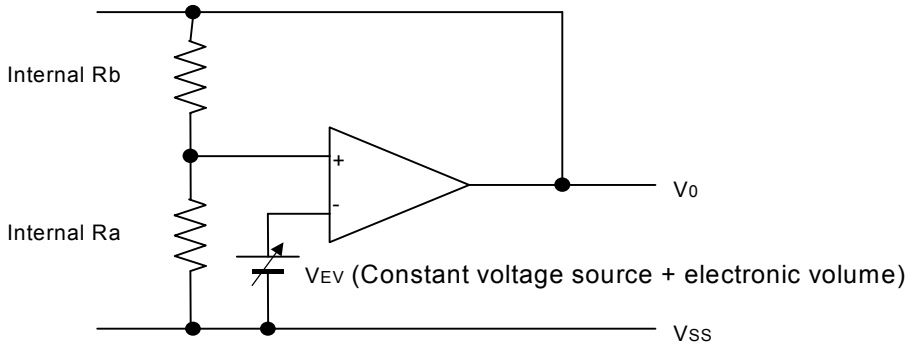


Fig.10

α is a value of the electronic volume, and can be set to one of 32-states by setting the 5-bit data in the electronic volume register. Table 11 shows the value of α.

Table 11

D4	D3	D2	D1	D0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
		:			:
		:			:
1	1	1	0	0	3
1	1	1	0	1	2
1	1	1	1	0	1
1	1	1	1	1	0

Table 12 (Reference values)

D3	D2	D1	1+Rb/Ra
0	0	0	5.45
0	0	1	5.71
0	1	0	6.00
0	1	1	6.32
1	0	0	6.67
1	0	1	7.06
1	1	0	7.50
1	1	1	External resistor can be used.

Rb/Ra is the V0 voltage regulator internal resistance ratio, and can be set to one of the 7 steps using the V0 voltage regulator internal resistance ratio set command.
By setting the 3-bit data in the V0 voltage regulator internal resistance ratio register, the reference value of (1+Rb/Ra) ratio will be as the values shown in Table 12.
Fig.11 shows the V0 voltage based on the values of the V0 voltage regulator internal resistance ratio register and the electronic volume register at Ta=25°C.

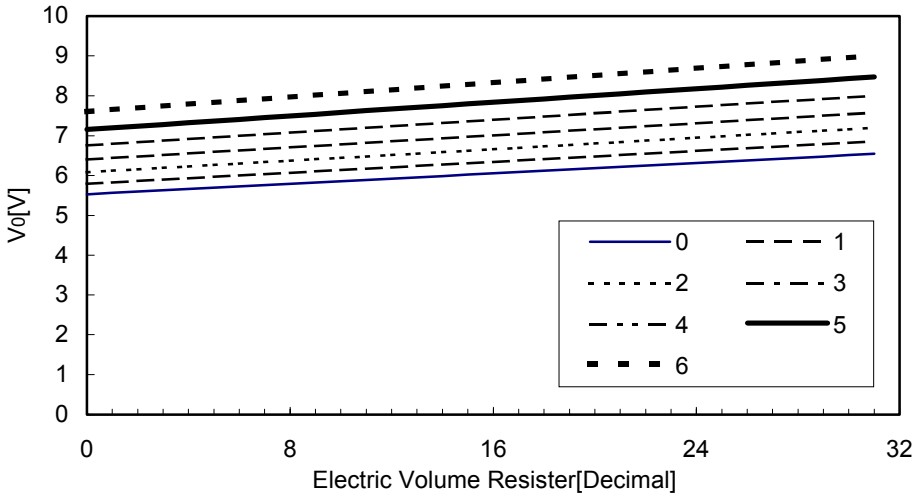


Fig.11 V0 voltage based on the values of V0 voltage regulator internal resistance ratio register and the electronic volume register [Ta=25°C]

<Setup example: When setting T_a=25°C and V_0=7V>
From Fig.11 and expression A-1, the following setting will be employed.

Table 13

Content	Register							
	D7	D6	D5	D4	D3	D2	D1	D0
V_0 voltage regulator internal resistance ratio	0	0	1	0	0	0	1	1
Electronic volume	1	0	0	1	0	0	0	0

Table 14 shows V_0 voltage variable range and its pitch width available from electronic volume function when the above setting is employed.

Table 14

V_0	Min.		Typ.		Max.	Unit
Variable range	6.41[80H]	to	7.0[90H]	to	7.58[9FH]	[V]
Pitch width			38			[mV]

[ ]: Commands selected from the electronic volume.

(B) When using the external resistor (when V_0 voltage regulator internal resistor is not used)
It is also possible to select a supply voltage V_0 for LCD without using the V_0 voltage regulator internal resistor (resistance ratio select command [27H] for the internal V_0 voltage regulator resistors) by adding a resistor across V_{SS} and V_R as well as V_R and V_0.
In this case too, using the electronic volume allows you to control LCD V_0 through the command and, thus, adjust the contrast of LCD display.
Voltage V_0 is given by the following expression when external resistance values Ra' and Rb' are specified in the range of $|V_0|<|V_{OUT}|$.

$$V_0 = (1+Rb'/Ra') \cdot V_{EV}$$
$$= (1+ Rb'/Ra') \cdot (1-\alpha/200) \cdot V_{REG} \quad \text{(Expression B-1)}$$
$$[V_{EV}=(1-\alpha/200) \cdot V_{REG}]$$

V_{REG} represents the constant voltage source on the IC. Its value at T_a=25°C is constant as shown in Table 10.

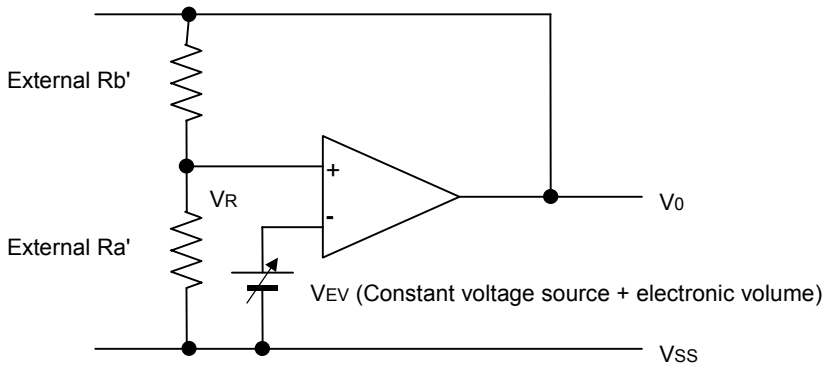


Fig.12

<Setting example: When setting T_a=25°C and V_0=7V>
When the intermediate resistor values (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0) are selected from the electronic volume, the following is given by expression B-1 since α = 15 and V_{REG} = 1.2V (Expression B-2).

$$V_0=(1+ Rb'/Ra')\cdot(1-\alpha/200)\cdot V_{REG}$$
$$7V=(1+ Rb'/Ra')\cdot(1-15/200)\cdot 1.2 \quad \text{(Expression B-2)}$$

If you select 5μA for the current conducted to Ra' and Rb', the following expression is derived:

$$Ra'+Rb'=1.4M\Omega \quad \text{(Expression B-3)}$$

Thus, the following is derived from expressions B-2 and B-3:

$$Rb'/Ra'=5.31$$
$$\therefore Ra'=220k\Omega,\ Rb'=1180k\Omega$$

Table 15 shows the command selected from the electronic volume. Table 16 lists V_0 voltage variable range and pitch width available from the electronic volume function.

Table 15

Content	Register							
	D7	D6	D5	D4	D3	D2	D1	D0
V_0 voltage regulator internal resistance ratio	0	0	1	0	0	1	1	1
Electronic volume	1	0	0	1	0	0	0	0

Table 16

V_0	Min.		Typ.		Max.	Unit
Variable range	6.45[80H]	to	7.0[90H]	to	7.64[9FH]	[V]
Pitch width			38.4			[mV]

[ ]: Commands selected from the electronic volume.

(C) When using external resistors (When using variable resistors instead of the V_0 voltage regulator internal resistors)

When using the above external resistor, LCD voltage V_0 can also be set by adding a variable resistor to finely tune Ra' and Rb'.

In this case too, using the electronic volume function permits you to control an LCD voltage V_0 through the command and, thus, adjust the contrast of LCD display.

The V_0 voltage can be obtained from the following expression by setting external resistors R1, R2 (variable resistors) and R3 within the range of $|V_0|<|V_{OUT}|$ and finely tuning R2 (ΔR2):

$$V_0=\{1+ (R3+R2-\Delta R2) / (R1+\Delta R2)\}\cdot V_{EV}$$
$$=\{1+ (R3+R2-\Delta R2) / (R1+\Delta R2)\}\cdot(1-\alpha/200)\cdot V_{REG} \quad \text{(Expression C-1)}$$
$$[V_{EV}=(1-\alpha/200)\cdot V_{REG}]$$

V_{REG} is the constant voltage source in the IC and its value remains at a constant level as shown in Table 10 (T_a=25°C).

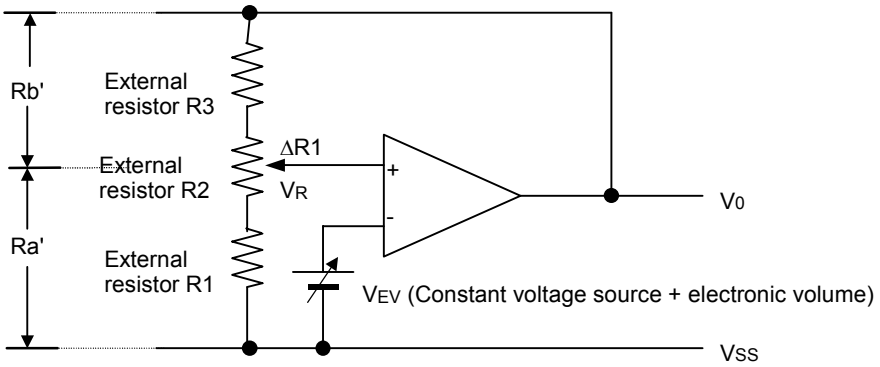


Fig.13

<Setting example: When setting Ta=25°C and V_0=5 to 9V>

α=15 and V_{REG} = 1.2V when intermediate resistor values (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0) are selected from the electronic volume.

Thus, using expression C-1, you can select V_0=9V when ΔR2=0Ω in the following manner:

9V={1+(R3+R2)/R1}・(1-15/200)・1.2

R3+R2=7.11 ・ R1 (Expression C-2)

If you select 5μA for the current to be conducted across V_0 and V_{SS} when V_0=7V (center value), sum of resistance of R1, R2 and R3 can be derived as shown below:

R1+R2+R3＝1.4MΩ (Expression C-3)

From expressions C-2 and C-3, R1＝1.4MΩ/8.11＝173kΩ

And, you can select V=5V when ΔR2=R2 through the following computation:

5V={1+R3/(R1+R2)}・(1-15/200)・1.2

R3/(R1+R2)=3.5 (Expression C-4)

R2＝137kΩ, R3＝1.09MΩ are derived from expressions C-2, C-3 and C-4.

Table 15 lists the command used, and Table 17 lists V_0 voltage variable range and pitch width available from the electronic volume.

Table 17

V_0	Min.		Typ.		Max.	Unit
Variable range	6.39[80H]	to	7.0[90H]	to	7.57[9FH]	[V]
Pitch width			38.1			[mV]

[ ]: Commands selected from the electronic volume.

※ When using the V_0 voltage regulator internal resistor or the electronic volume function, both of the voltage regulator circuit and the voltage follower circuit must be activated, as a minimum requirement, by the power control set command. When the booster circuit is turned off, necessary voltage must be supplied from V_{OUT}.

※ V_R pin is enabled only when the V_0 voltage regulator internal resistors are not used. V_R pin must be made open when these resistors are used.

※ Since VR pin has a higher input impedance, appropriate noise protection measures must be provided including cutting the wiring distance shorter or using shielded wire.

6.6.3 Liquid crystal voltage generator circuit

The V_0 voltage is divided by resistor-split within an IC and generates V_1, V_2, V_3 and V_4 potentials required for driving liquid crystals.

Then, V_1, V_2, V_3 and V_4 potentials are impedance-converted by the voltage follower circuit and supplied to the liquid crystal drive circuit.

Using the command, either 1/5 bias or 1/6 bias can be selected as bias ratio.

6.6.4 On-chip power supply turn OFF command sequence

To turn the built-in power supply off, it is recommended that the following command sequence be observed to set the system in the power save state beforehand so that the residual power is discharged from the LCD panel, power supply pins and others.

You can also turn the built-in power supply off by initializing it using $\overline{RES}$ pin or the reset command. When LOW Level is input to the $\overline{RES}$ Pin, short-circuit occurs between V_{OUT} and V_{DD2} and between V_0 and V_{SS} due to discharge. Keep this in mind when using an external power supply.

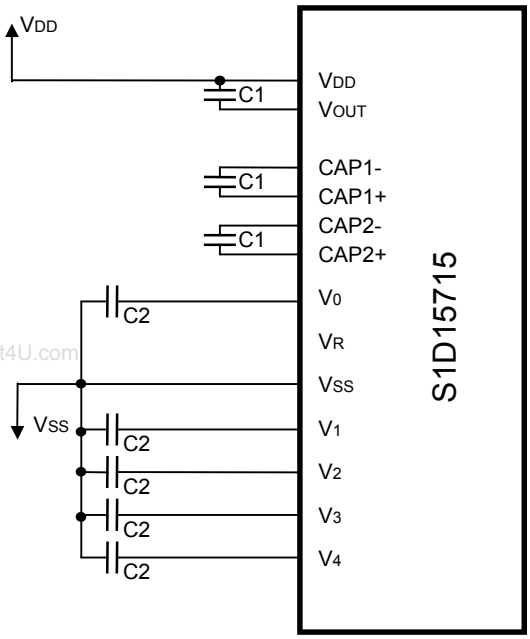
Table 18

Sequence	Contents (command and state)	Command address								
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power save command (composite command)
	↓									
Step2	Display all points on	1	0	1	0	0	1	0	1	
	↓									
End	Built-in power OFF	0	0	1	0	1	0	0	0	

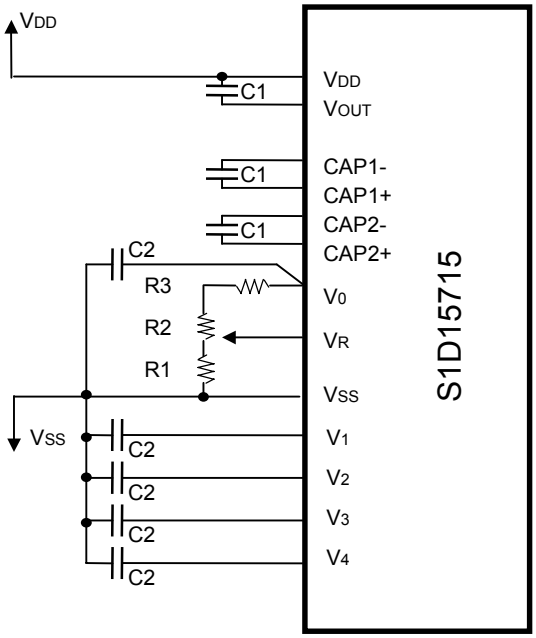
6.6.5 Sample circuits

① When booster, voltage regulator and V/F circuits are all used

(1) When V_0 voltage regulator internal resistors are used (when triple boosting)

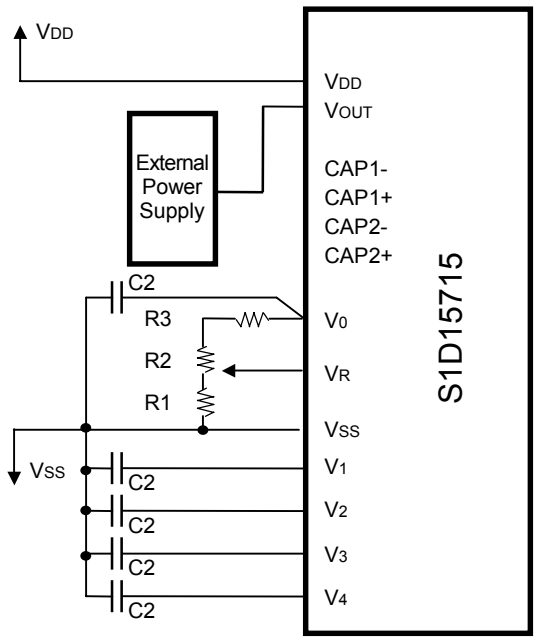


(2) When V_0 voltage regulator internal resistors are not used (when triple boosting)

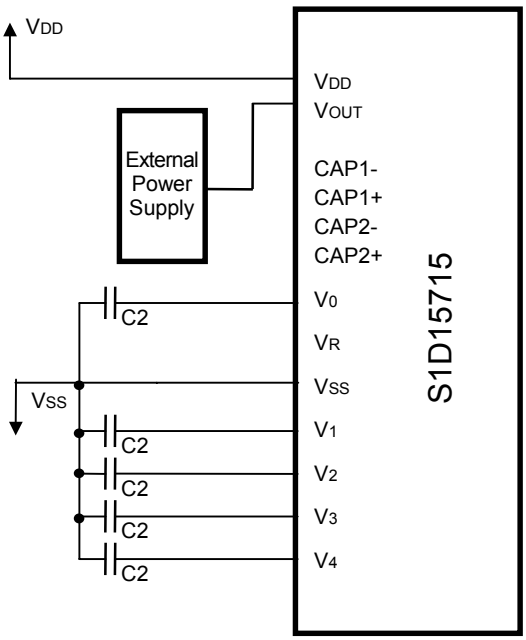


② When voltage regulator and V/F circuits alone are used

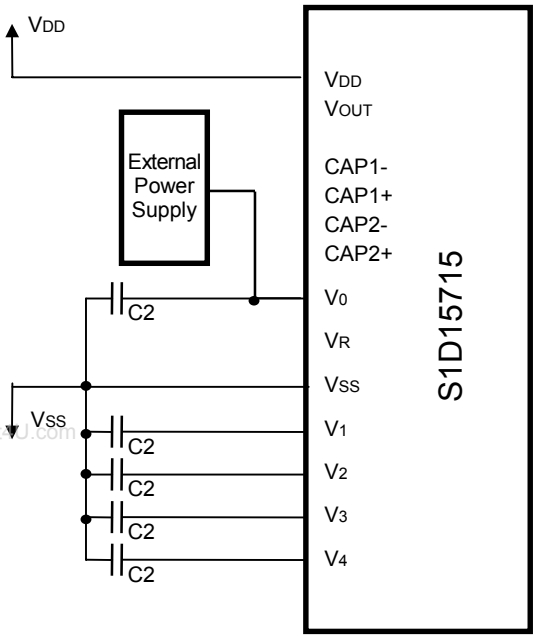
(1) When V_0 voltage regulator internal resistors are not used



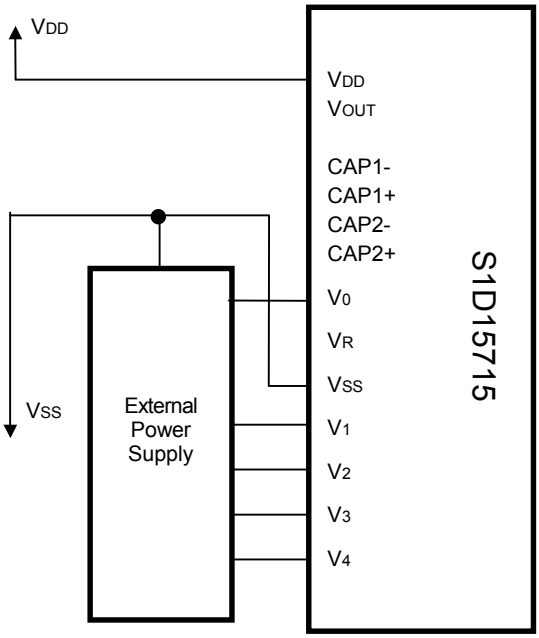
(2) When V_0 voltage regulator internal resistors are used



(3) When V/F circuit alone is used



(4) When built-in power supply is not used



※ Since VR pin has a higher impedance, wiring distance must be minimized or shielded wire must be used.

Sample setting
When V0 is varied between 8 and 9V

Item	Setting	Unit
C1	1.0 to 4.7	μF
C2	0.01 to 1.0	μF

Fig.14

6.7 Reset circuit

When the $\overline{RES}$ pin is made to the LOW level or when the reset command is used, this LSI will become the initial setting state. Indicated below is the initial setting state.

- Serial interface internal shift register and counter clear
- Power saver mode is entered.
  - Oscillation circuit is stopped.
  - LCD power supply circuit is stopped.
  - Display OFF
  - Display all points ON : (Display all points ON ON/OFF command D0="1")
  - Segment/common driver outputs go to the V_{SS} level.
- Display normal
- Page address : 0H
- Column address : 0H
- Display start line address : set at the first line
- Segment driver direction : normal
- Common driver direction : normal
- n-line inversion drive : Cancel
- Read modify write : OFF
- Power control register : (D2, D1, D0) = (0, 0, 0)
- V_0-resistor ratio register : (D2, D1, D0) = (0, 0, 0)
- Electronic volume register : (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0)
- Test mode is released.

* Voltage short circuit across V_{OUT} and V_{DD} as well as V_0 and V_{SS} [allowed only when $\overline{RES}$ pin = LOW level].

When reset is detected, this LSI is set to above initialized states. However it has no effect on contents of DDRAM.
Because the internal state of the IC becomes inconstant during power on, initialization by $\overline{RES}$ pin is always required.
Check that each input pin is controlled after initialization through $\overline{RES}$ pin.
If the control signal from MPU has high impedance, an overcurrent may flow through the IC.
A protection is required to prevent high impedance at the input pin during power-on.

7. COMMAND DESCRIPTION

S1D15715 Series identifies the data bus signal by a combination of A0, $\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$) signals.
Interpretation and execution of commands are performed only by the internal timing independent of external clocks.
In the 80-series MPU interface, the command is activated when a LOW pulse is input to $\overline{RD}$ pin for reading and when a LOW pulse in input to $\overline{WR}$ pin for writing.
In the 68-series MPU interface, the S1D15715 series enters a read mode when a HIGH level is input to R/W pin and a write mode when a LOW level is input to R/$\overline{W}$ pin, and the command is activated when a HIGH pulse is input to E pin.
Therefore, in the command description and command table, the 68-series MPU interface is different from the 80-series MPU interface in that $\overline{RD}$(E) becomes "1(H)" in status read and display data read command.
Taking the 80-series MPU interface as an example, commands will be explained below.
When the serial interface is selected, the data is input in sequence starting with D7.

7.1 Display ON/OFF

This command turns the display ON and OFF.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	0	Display OFF
										1	Display ON

When the display OFF command is executed when in the Display all points ON mode, Power saver mode is entered. See the section on the Power saver for details.

7.2 Display normal/reverse

This command can reverse the lit and unlit display without overwriting the contents of the DDRAM.
The contents of the DDRAM will be maintained.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	Normal: DDRAM Data HIGH = LCD ON potential
										1	Normal: DDRAM Data LOW = LCD ON potential

7.3 Display all points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the DDRAM.
Even when this is done, the DDRAM contents are maintained.
This command takes priority over the display normal/reverse command.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display all points ON command is executed when in the Display OFF mode, Power saver mode is entered.
See the section on the Power saver for details.

7.4 Page address set

This command specifies the page address that corresponds to the low address when accessing the DDRAM from the MPU side (refer to Fig.4).
Specifying the page address and column address enables the access to a desired bit of the DDRAM.
Even when the page address is changed, the display state will not be changed. For details, see the Page address circuit of the "Functional Description".
After the last column address (65H), page address is incremented by +1 (refer to Fig.5).
After the very last address (column=65H, page=3H), page address returns to 0H.
Page address 7H is the DDRAM area dedicate to the indicator, and only D0 is valid for data change.
See the function explanation in "DDRAM and page/column address circuit", for details.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0H
								0	0	1	1H
								0	1	0	2H
								0	1	1	3H
								1	0	0	4H

7.5 Column address set

This command specifies the column address of the DDRAM (refer to Fig.4).
The column address is split into two sections (the upper 3-bits and lower 4-bits) when it is set (fundamentally, set continuously).
Each time the DDRAM is accessed, the column address automatically increments, making it possible for the MPU to continuously read and write the display data
After the last column address (65H), column address returns to 00H (refer to Fig.5).
See the function explanation in "DDRAM and page/column address circuit", for details.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	0	0	1	0	A6	A5	A4	Upper bit address
						0	A3	A2	A1	A0	Lower bit address

*Disabled bit

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	00H
0	0	0	0	0	0	1	01H
0	0	0	0	0	1	0	02H
			:				:
1	1	0	0	1	0	0	64H
1	1	0	0	1	0	1	65H

7.6 Display start line address set

This command is used to specify the display start line address of the DDRAM (refer to Fig.4).
See the function explanation in "Line address circuit" for details.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	00H
						0	0	0	0	1	01H
						0	0	0	1	0	02H
							:				:
						1	1	1	1	0	1EH
						1	1	1	1	1	1FH

7.7 ADC select (Segment driver direction select)

This command can reverse the correspondence between the DDRAM column address and the segment driver output (refer to Fig.4).

See the function explanation in "DDRAM and page/column address circuit", for details.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

7.8 Common output status select

This command can select the scanning direction of the COM output pin. It can reverse the correspondence between the DDRAM line address and the common driver output.
See the function explanation in "Line address circuit" for details.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	0	0	0	*	*	*	Normal
							1				Reverse

*Disabled bit

7.9 Display data read

This commands reads 8-bit data from the specified DDRAM address.
Since the column address is automatically incremented after each read, the MPU can continuously read multiple-word data.
One dummy read is required immediately after the column address has been set.
See the function explanation in "Access to DDRAM and internal registers" and "DDRAM and page/column address circuit", for details.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

7.10 Display data write

This command writes 8-bit data to the specified DDRAM address.
Since the column address is automatically incremented after each write, the MPU can continuously write multiple-word data.
See the function explanation in "DDRAM and page/column address circuit", for details.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

7.11 Read modify write

This command is used paired with end command.
Once this command is issued, the column address is not incremented by display data read command but is incremented by display data write command. This mode is maintained until end command is issued.
When end command is issued, the column address returns to the address it was at when read modify write command was issued.

This function makes it possible to reduce the MPU load when there are data to change repeatedly in a specified display region, such as blinking cursor.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* When end command is issued, only column address returns to the address.
Consequently, Read modify write mode cannot be used over pages.
Since the page address is automatically incremented for this IC, when end command is executed after the data is written to the last column address (65H), it does not return to the original location in the display.
When you want to maintain the current page address after a read modify write operation done on a column address between the start and the final column address (65H), you must specify the page address again.

* Even if in Read modify write mode, other commands besides display data read/write can also be used.
However, column address set command cannot be used.

- The sequence for cursor display

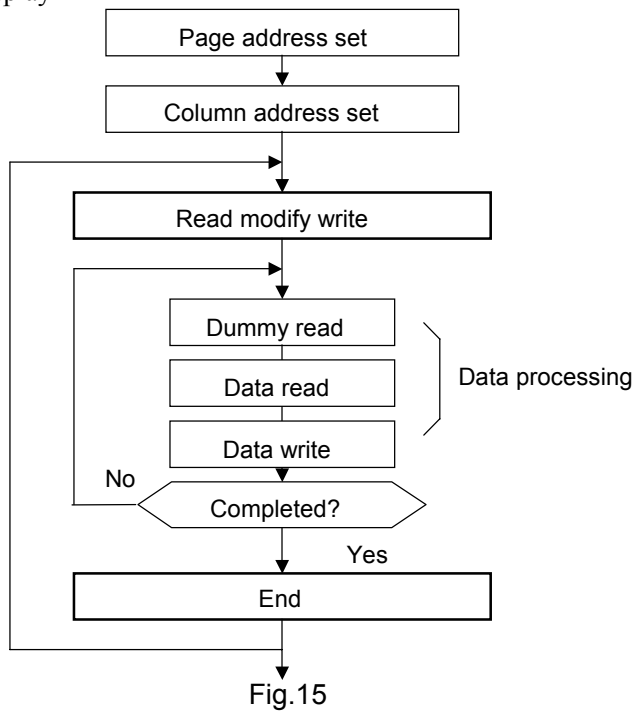


Fig.15

7.12 End

This command releases the Read modify write mode, and returns the column address to the address it was when read modify write command was issued.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

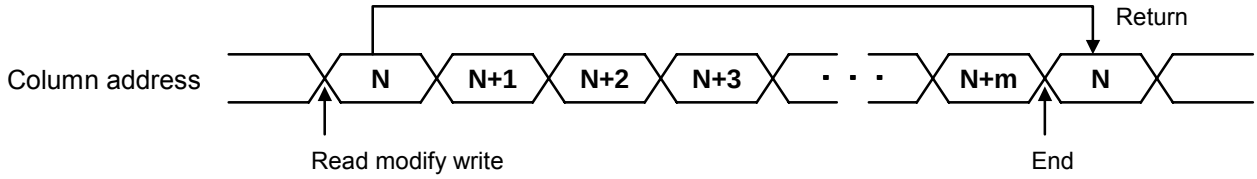


Fig.16

7.13 Power control set

This command sets the power supply circuit function ON/OFF.
See the function explanation in "Power supply circuit" for details.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Mode
0	1	0	0	0	1	0	1	0			Booster: OFF
								1			Booster: ON
									0		Voltage regulator: OFF
									1		Voltage regulator: ON
										0	Voltage follower: OFF
										1	Voltage follower: ON

7.14 V_0 voltage regulator internal resistance ratio set

This command sets the V_0 voltage regulator circuit internal resistance ratio.
See the function explanation in "Power supply circuit" for details.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra ratio	V_0 voltage
0	1	0	0	0	1	0	0	0	0	0	small	LOW
								0	0	1		
								0	1	0		
								0	1	1	↓	↓
								1	0	0		
								1	0	1		
								1	1	0	large	HIGH
								1	1	1	External resistor mode	

7.15 Electronic volume set

This command controls the liquid crystal drive voltage V0 output from the voltage regulator circuit of the built-in liquid crystal power supply and can adjust the contrast of LCD panel display.
See the function explanation in "Power supply circuit" for details.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	α	V0 voltage
0	1	0	1	0	0	0	0	0	0	0	31	LOW
						0	0	0	0	1	30	
						0	0	0	1	0	29	
								↓			↓	↓
						1	1	1	1	0	1	
						1	1	1	1	1	0	HIGH

7.16 LCD bias set

This command selects the voltage bias ratio required for the LCD.
This command is enabled when the voltage follower circuit operates.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Bias S1D15A08
0	1	0	1	0	1	0	0	0	1	0	1/5 bias
										1	1/6 bias

7.17 n-line inversion drive register set

This command sets the number of the inversion lines of the LCD alternating driver to the register. The number of lines that can be set is between 2 to 16. For details, refer to the functional description of "Display Timing Generation Circuit".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Number of reverse line
0	1	0	0	0	1	1	0	0	0	0	—
							0	0	0	1	2
							0	0	1	0	3
								↓			↓
							1	1	1	0	15
							1	1	1	1	16

7.18 Canceling n-line inversion drive

This command cancels n-line inversion drive and restores the normal dual-frame inversion driving. The value of n-line inversion drive register will not change.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	0	0

7.19 Power save (composite command)

When the display all points ON command is executed when in the display OFF mode, power save mode is entered, and the power consumption can be greatly reduced.

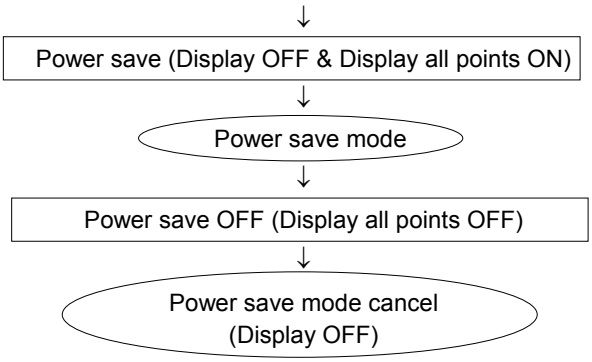


Fig.17

This mode stops every operation of the circuits for the driver, and can reduce current consumption nearly to a static current value if no access is made from the MPU.
The internal states in the power saver mode is as follows:

- The oscillation circuit is stopped.
- The LCD power supply circuit is stopped.
- All LCD driver circuits are stopped and segment/common driver outputs output the VSS level.
- The display data and operation mode before execution of the power saver command are held, and the MPU can access to the DDRAM and internal registers.

7.20 Reset

When this command is issued, S1D15715 Series is initialized (same operation as $\overline{RES}$ pin=LOW input this command, however, is not used for introducing short circuit across VOUT and VDD or V0 and VSS.)
Also note that initialization of the DDRAM does not take place in parallel with initialization of the LSI.
See the function explanation in "Reset circuit" for details.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

When initializing the S1D15715 Series while power is turned on, reset signal to the $\overline{RES}$ pin is used. This signal cannot be replaced by the reset command.

7.21 NOP

Non-operation command

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

7.22 Test

This is a command for LSI chip testing. Please do not use.
If the test command is issued by accident, it can be cleared by applying an LOW signal to the $\overline{RES}$ pin, or by issuing the reset command or the display ON/OFF command.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	*	1	*	*	*	*

*Disabled bit

*: S1D15715 Series chip maintain their operating modes, but excessive external noise, etc., may happen to change them.
Measures are required to prevent noise generation or influence on installation and systems.
Moreover, it is recommended that the operating modes are refreshed periodically to prevent the effects of unanticipated noise.

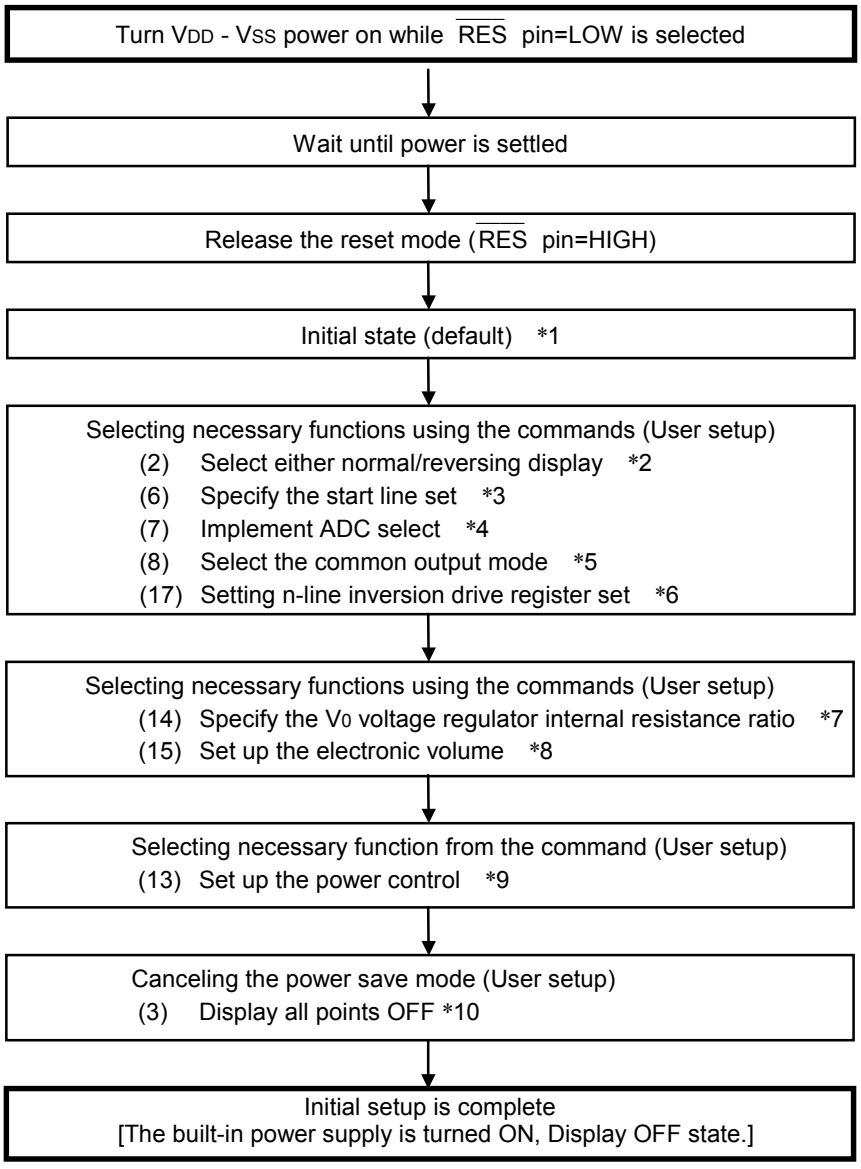
Table 19 S1D15715 Series Command Table

Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0 1	LCD display normal/reverse 0: normal, 1: reverse
(3) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display, 1: all points ON
(4) Page address set	0	1	0	1	0	1	1	0	Page address			Page address Sets the DDRAM page address
(5) Column address set Upper 3-bit address	0	1	0	0	0	0	1	0	Upper column address			Upper column address Sets the upper 3-bit for DDRAM column address
Column address set Lower 4-bit address	0	1	0	0	0	0	0	Lower column address				Lower column address Sets the lower 4-bit for DDRAM column address
(6) Display start line address set	0	1	0	0	1	0	Display start address					Display start address Sets the DDRAM display start line address
(7) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Supports the SEG output of the DDRAM 0: normal, 1: reverse
(8) Common output status select	0	1	0	1	1	0	0	0 1	*	*	*	Selects the scanning direction of COM output 0: normal, 1: reverse
(9) Display data read	1	0	1	Read data								Reads from the DDRAM
(10) Display data write	1	1	0	Write data								Writes to the DDRAM
(11) Read modify write	0	1	0	1	1	1	0	0	0	0	0	Column address increment at write: +1, at read: 0
(12) End	0	1	0	1	1	1	0	1	1	1	0	Releases Read modify write mode
(13) Power control set	0	1	0	0	0	1	0	1	Operating mode			Sets the on-chip power supply circuit operating mode
(14) V_0 voltage regulator internal resistance ratio set	0	1	0	0	0	1	0	0	Resistance ratio setting			Selects the state of internal resistance ratio (Rb/Ra)
(15) Electronic volume register	0	1	0	1	0	0	Electronic volume value					Sets the V_0 output voltage to the electronic volume register
(16) LCD bias set	—	—	—	1	0	1	0	0	0	1	0 1	Setting the LCD driver voltage bias ratio 0: : 1/5 bias, 1 : 1/6 bias
(17) n-line inversion drive register set	0	1	0	0	0	1	1	Number of inversion line				Line inversion drive Setting the line number
(18) n-line inversion drive cancel	0	1	0	1	1	1	0	0	1	0	0	Canceling the line inversion drive
(19) Power saver	—	—	—	—	—	—	—	—	—	—	—	Compound command of Display OFF and Display all points ON
(20) Reset	0	1	0	1	1	1	0	0	0	1	0	software reset
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-operation
(22) Test	0	1	0	1	1	*	1	*	*	*	*	IC test command. Do not use.
												(Note)*: disabled data

Instruction Setup Example (For your reference)

Note: If charge remains on the smoothing capacitor connected across the LCD drive voltage output pin troubles (such as momentary blackening) can occur on the display screen during its powering on process.
In order to avoid such troubles, it is recommended to implement the following flow.

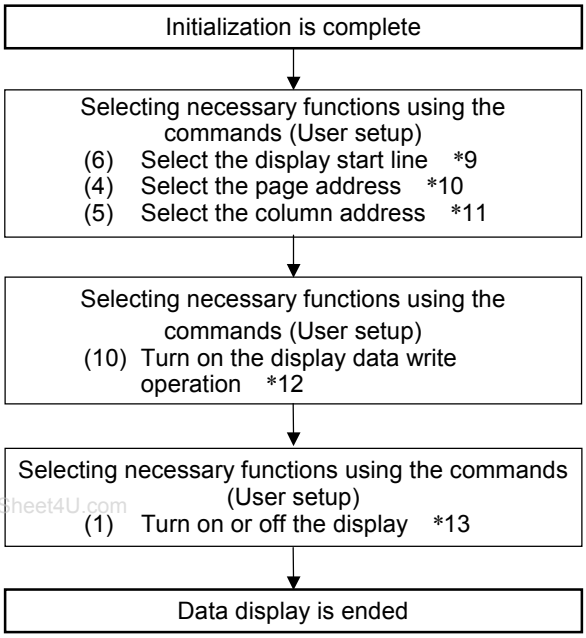
① When switching to the built-in power supply takes place immediately after powering on:



Note : Reference Items

*1: Refer to 6. Functional Description “6.7 Reset circuit”
In the initial setup mode (default), too, contents of the display data RAM is still uncertain.
*2: Refer to the 7. Command Description “(2) Normal/reversing display”
*3: Refer to the 7. Command Description “(6) Display start line set”
*4: Refer to the 7. Command Description “(7) ADC select”
*5: Refer to the 7. Command Description “(8) Common output status select”
*6: Refer to the 7. Command Description “(17) Setting n-line inversion drive register set”
*7: Refer to thee 6. Functional Description “6.6 Power supply circuit” and 7. Command Description “(14) V_0 voltage regulator internal resistance ratio set”.
*8: Refer to the 6. Functional Description “6.6 Power supply circuit” and 7. Command Description “(15) Electronic volume”.
*9: Refer to the 6. Functional Description “6.6 Power supply circuit” and 7. Command Description “(13) Power control set”.
*10: Refer to the 7. Command Description : “(19) Power save”

② Data display



Note: Reference Items

*9: Refer to the 7. Command Description "(6) Display start line set"

*10: Refer to the 7. Command Description "(4) Page address set"

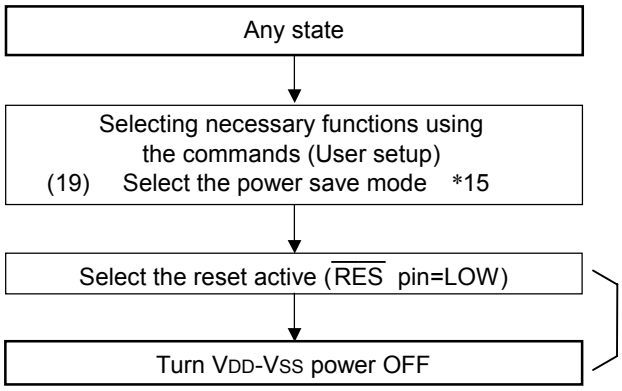
*11: Refer to the 7. Command Description "(5) Column address set"

*12: Refer to the 7. Command Description "(10) Display data write"

*13: Refer to the 7. Command Description "(1) Display ON/OFF"

The all-white display of data should be avoided as much as practicable right after the display mode is turned on (during display ON).

③Powering OFF *14



The time (t_L) provided between turning on of the reset active and turning off of V_{DD}-V_{SS} power (V_{DD}-V_{SS}=1.8V) must be longer than the time required for V_0-V_4 potential to go lower (t_H) than the threshold voltage set on the LCD panel (usually 1V).

For "t_H", see the "Reference data" in the following section.

If "t_H" is excessively long, it must be cut short by installing a resistor across V_0 and V_{SS}.

Note: Reference Items

*14: This IC is provided on the power supply V_{DD}-V_{SS} logic to offer control over the V_0-V_{SS} drivers on the LCD power supply.

Thus, if the power supply V_{DD}-V_{SS} is turned OFF while voltage is still remaining on the LCD power supply V_0-V_{SS}, the drivers (both COM and SEG) can generate uncontrolled output. Make sure to observe the following powering off procedure:

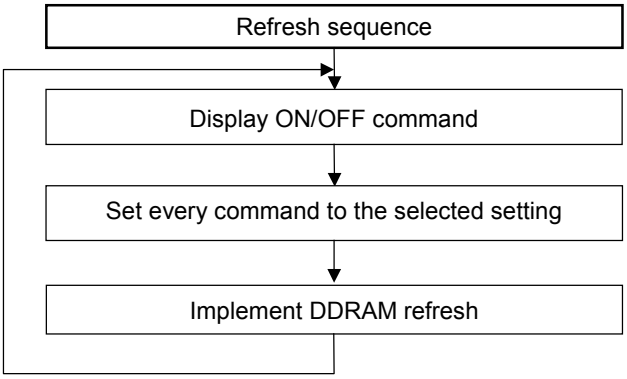
- Turn OFF the built-in power supply first, then, after making sure that potential on V_0 to V_4 is lower than the LCD panel threshold voltage, turn the IC power (V_{DD}-V_{SS}) OFF.
  Also refer to the 6. Functional Description "Power supply circuit".

*15: Refer to the 7. Command Description "(19) Power save"

After entering the power save command, you must implement reset procedure from $\overline{RES}$ pin before turning off V_{DD}-V_{SS} power.

④ Refresh

It is recommended that the operating modes and display contents be refreshed periodically.



⑤ Precautions on powering OFF

<Power (V_{DD}-V_{SS}) OFF >

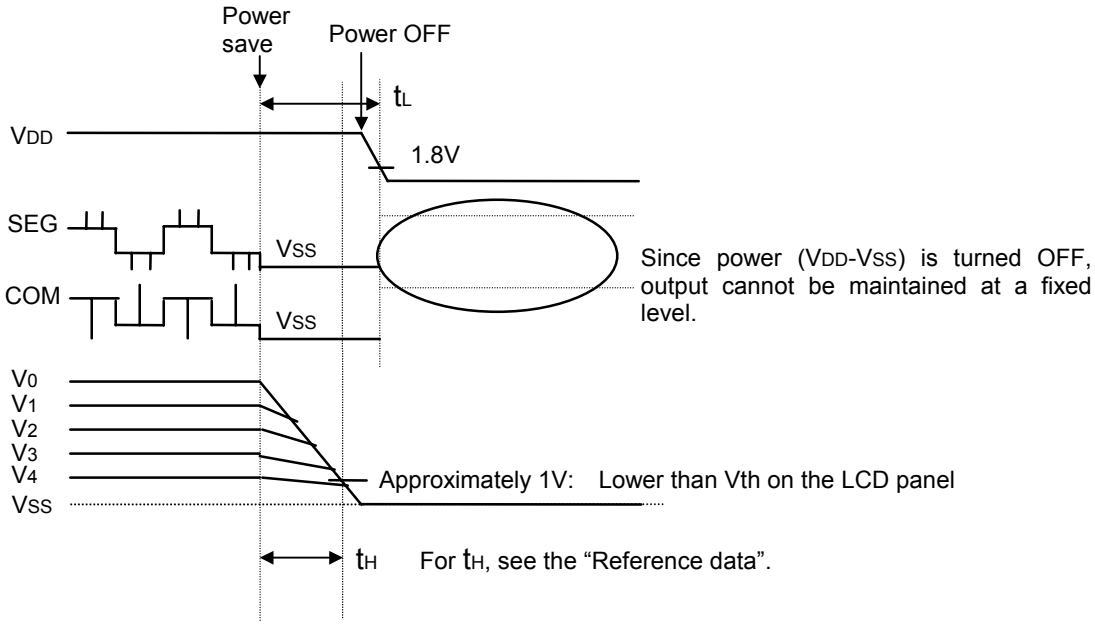
Turn the power (LCD power (V_0-V_{SS}) system OFF) save mode off -> Then, turn the power (V_{DD}-V_{SS}) off.

- The requirement $t_L > t_H$ must be strictly observed.
- If $t_L < t_H$, display failures can result.

t_L must be specified on software from MPU.

t_H depends on discharging capability of the drivers. See "Reference data" in the following section.

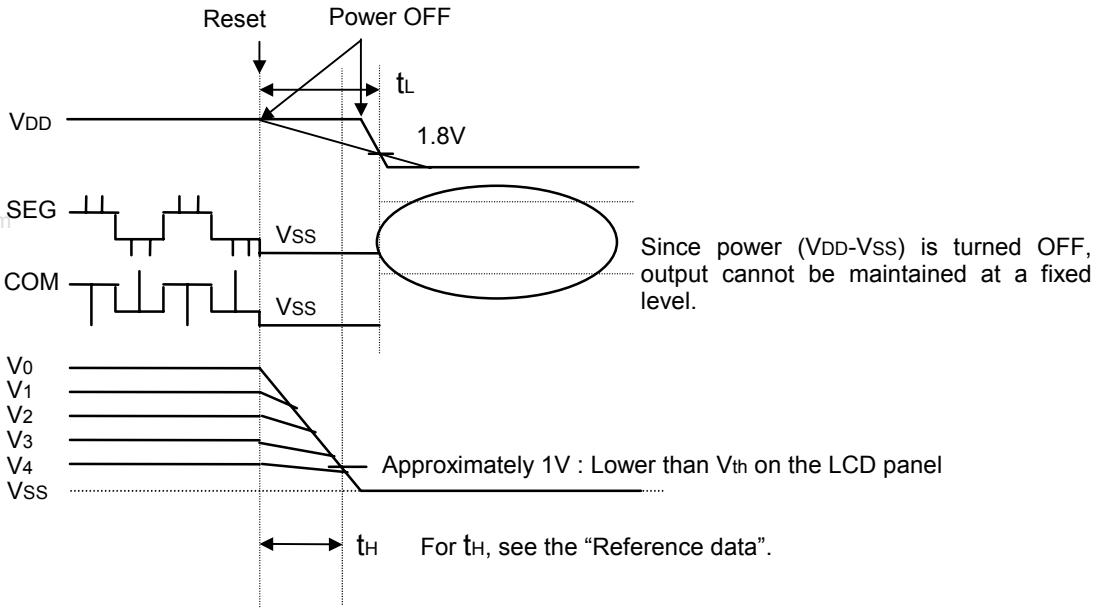
It also depends on a given LCD panel, thus actual timing must be determined after experimenting on your LCD panel.



<When powering OFF (V_{DD}-V_{SS}) is not available with the command>
Turn off the reset mode(LCD power (V_0-V_{SS}) system). -> Then turn the power (V_{DD}-V_{SS}) OFF.

- The requirement $t_L > t_H$ must be strictly observed.
- If $t_L < t_H$, display failures can result.

When specifying t_L, measures such as extending fall time of power supply (V_{DD}-V_{SS}) should be considered.
t_H depends on discharging capability of the drivers. See "Reference data" in the following section.
It also depends on model of a given LCD panel, thus actual timing must be determined after experimenting on your LCD panel.



⑥ Reference data
The following data is for your reference alone.
t_H is significantly affected by capacity of V_0 pin, thus you must verify appropriateness of a selected t_H on the panel being equipped with the pin.

[Conditions: V_{DD}=1.8V, voltage is tripled and capacity of the boosting capacitor=1.0µF]
When V_0 is under no-load, t_H per voltage is 22µs. It becomes 200µs when V_0=9V.
Capacity dependency is 1pF. Δt_H per voltage is 50ns.

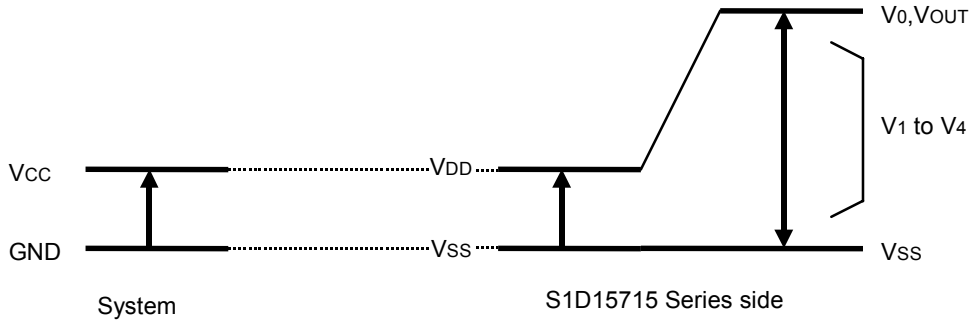
An example: When V_{DD}=1.8V, V_0=8.0V and V_0 pin capacity [board capacity] (C_L)=100pF.

t_H =22µs×8V+50ns×100pF×8V=216µs

8. ABSOLUTE MAXIMUM RATING

Table 20

Item		Symbol	Standard value	Unit
Supply voltage (1)		V_{DD}	-0.3 to +6.0	V
	Double boosting		-0.3 to +5.0	
	Triple boosting		-0.3 to +3.3	
Supply voltage (2)		V_0, V_{OUT}	-0.3 to +10.0	V
Supply voltage (3)		V_1, V_2, V_3, V_4	-0.3 to V_0	V
Input voltage		V_{IN}	-0.3 to V_{DD}+0.3	V
Output voltage		V_O	-0.3 to V_{DD}+0.3	V
Operating temperature		T_{OPR}	-40 to +85	°C
Storage temperature	TCP	T_{STR}	-55 to +100	°C
	Bare chip		-55 to +125	



Note 1: All voltages are based on the condition that the V_{SS} is equal to 0V.

Note 2: Voltages V_0, V_1, V_2, V_3 and V_4 must always keep up the condition of $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ and $V_{OUT} \geq V_0 \geq V_{SS}$, $V_{OUT} \geq V_{DD}$.

Note 3: If the LSI chip is used in an environment exceeding the absolute maximum ratings, it may be destroyed permanently.
During normal operation, electrical characteristics conditions should be observed. Otherwise, the LSI chip may malfunction or the LSI reliability may drop.

9. DC CHARACTERISTICS

Table 21

V_{SS} = 0V, V_{DD} = 3V±10%, T_a = -40 to +85°C unless otherwise noted

Item		Symbol	Condition		Standard value			Unit	Pin used
					Min.	Typ.	Max.		
Supply voltage (1)		V_{DD}	—		1.8	—	5.5	V	V_{DD} *1
Supply voltage (2)		V_0	—		4.5	—	9.0	—	V_0 *2
		V_1, V_2	—		0.6×V_0	—	V_0	V	V_1, V_2
		V_3, V_4	—		V_{SS}	—	0.4×V_0	—	V_3, V_4
High-level input voltage		V_{IH}	—		0.8×V_{DD}	—	V_{DD}	V	*3
Low-level input voltage		V_{IL}	—		V_{SS}	—	0.2×V_{DD}	V	
High-level output voltage		V_{OH}	I_{OH}=-0.5mA		0.8×V_{DD}	—	V_{DD}	V	*4
Low-level output voltage		V_{OL}	I_{OL}= 0.5mA		V_{SS}	—	0.2×V_{DD}	V	
Input leak current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		-1.0	—	1.0	μA	*5
Output leak current		I_{LO}			-3.0	—	3.0	μA	*6
LCD driver ON resistance		R_{ON}	V_0=7.0V T_a=25°C		—	4.0	10.0	kΩ	SEGn, COMn *7
Static current consumption		I_{DDQ}	T_a=25°C		—	0.01	5.0	μA	V_{DD}, V_{DD2}
Output leak current		I_{0Q}	V_0=7.0V T_a=25°C		—	0.01	15.0	μA	V_0
Input pin capacitance		C_{IN}	T_a=25°C, f=1MHz		—	20.0	30.0	pF	
Oscillation frequency	Built-in oscillation	f_{OSC}	T_a=25°C	S1D15715	20.67	21.76	22.85	kHz	*8
				S1D15716	21.88	23.04	24.2		
				S1D15717	20.06	21.12	22.18		
	External input	f_{CL}	T_a=25°C	S1D15715	10.88	21.76	43.52	kHz	CL *8
				S1D15716	5.76	11.52	23.04		
				S1D15717	21.12	42.24	84.48		

Table 22

Item		Symbol	Condition	Standard value			Unit	Pin used
				Min.	Typ.	Max.		
Built-in power supply circuit	Input voltage	V_{DD}	Double boosting	1.8	—	5.5	V	V_{DD} *1
			Triple boosting	1.8	—	3.3		
	Boosted output voltage	V_{OUT}	—	—	—	10.0		V_{OUT}
	Operating voltage of voltage regulator circuit	V_{OUT}	—	5.0	—	10.0		V_{OUT}
	Operating voltage of V/F circuit	V_0	—	4.5	—	9.0		V_0 *9
	Reference voltage	V_{REG}	-0.05%/°C T_a=25°C	1.16	1.20	1.24		

Note 1: All voltages are based on the condition that the V_{SS} is equal to 0V.

Note 2: Voltages V_0, V_1, V_2, V_3 and V_4 must always keep the condition of $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ and $V_{OUT} \geq V_0 \geq V_{SS}$, $V_{OUT} \geq V_{DD}$.

Note 3: If the LSI chip is used in an environment exceeding the absolute maximum ratings, it may be destroyed permanently.
During normal operation, electrical characteristics conditions should be observed. Otherwise, the LSI chip may malfunction or the LSI reliability may drop.

◇Dynamic operating current (1) - When display is turned on with the built-in power supply being disconnected [T_a=25°C and output under no-load].

Following shows current consumed by entire IC when external power supply is used.

Table 23.1 Display: All-white

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
S1D15715	I_{SS}(1)	V_{DD}=3.0V,V_0=7.0V	—	24	41	μA	*10
	I_{SS}(1)	V_{DD}=5.0V,V_0=7.0V	—	26	44		
S1D15716	I_{SS}(1)	V_{DD}=3.0V,V_0=7.0V	—	24	41	μA	*10
	I_{SS}(1)	V_{DD}=5.0V,V_0=7.0V	—	25	43		
S1D15717	I_{SS}(1)	V_{DD}=3.0V,V_0=7.0V	—	25	43	μA	*10
	I_{SS}(1)	V_{DD}=5.0V,V_0=7.0V	—	27	46		

Table 23.2 Display: Checker pattern

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
S1D15715	I_{SS}(1)	V_{DD}=3.0V,V_0=7.0V	—	25	43	μA	*10
	I_{SS}(1)	V_{DD}=5.0V,V_0=7.0V	—	27	46		
S1D15716	I_{SS}(1)	V_{DD}=3.0V,V_0=7.0V	—	24	41	μA	*10
	I_{SS}(1)	V_{DD}=5.0V,V_0=7.0V	—	26	44		
S1D15717	I_{SS}(1)	V_{DD}=3.0V,V_0=7.0V	—	26	44	μA	*10
	I_{SS}(1)	V_{DD}=5.0V,V_0=7.0V	—	29	49		

◇Dynamic operating current (2) - When display is turned on with the built-in power supply being connected [T_a=25°C and output under no-load].

Table 24.1 Display: All-white

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
S1D15715	I_{SS}(2)	V_{DD}=5.0V,V_0=7.0V, double boosting	—	35	60	μA	*10
	I_{SS}(2)	V_{DD}=3.0V,V_0=7.0V, triple boosting	—	42	72		
S1D15716	I_{SS}(2)	V_{DD}=5.0V,V_0=7.0V, double boosting	—	32	55	μA	*10
	I_{SS}(2)	V_{DD}=3.0V,V_0=7.0V, triple boosting	—	38	65		
S1D15717	I_{SS}(2)	V_{DD}=5.0V,V_0=7.0V, double boosting	—	36	62	μA	*10
	I_{SS}(2)	V_{DD}=3.0V,V_0=7.0V, triple boosting	—	43	73		

Table 24.2 Display: Checker pattern

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
S1D15715	I_{SS}(2)	V_{DD}=5.0V,V_0=7.0V, double boosting	—	37	63	μA	*10
	I_{SS}(2)	V_{DD}=3.0V,V_0=7.0V, triple boosting	—	43	73		
S1D15716	I_{SS}(2)	V_{DD}=5.0V,V_0=7.0V, double boosting	—	33	56	μA	*10
	I_{SS}(2)	V_{DD}=3.0V,V_0=7.0V, triple boosting	—	39	67		
S1D15717	I_{SS}(2)	V_{DD}=5.0V,V_0=7.0V, double boosting	—	39	67	μA	*10
	I_{SS}(2)	V_{DD}=3.0V,V_0=7.0V, triple boosting	—	46	78		

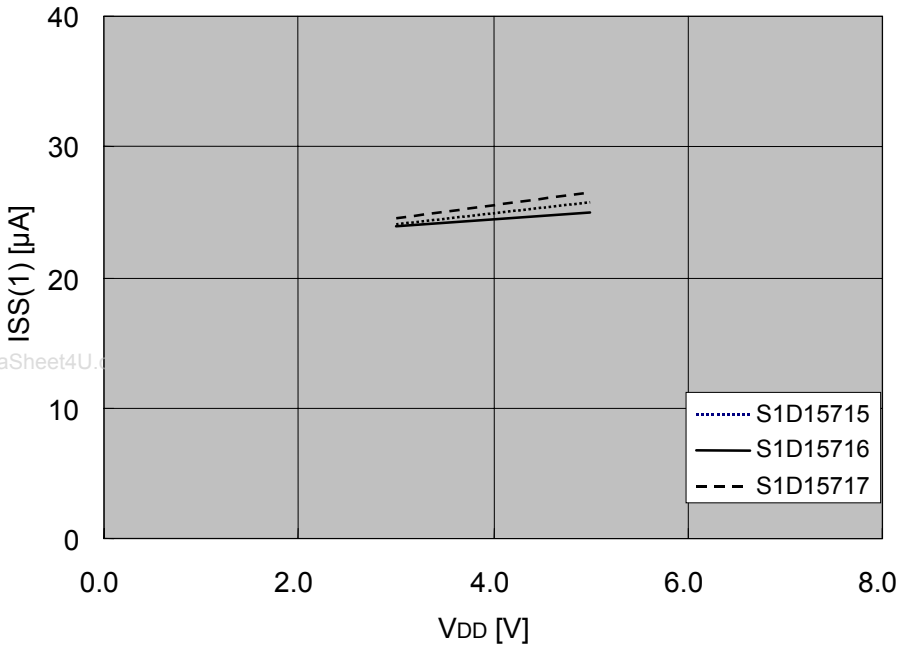
◇Current consumption in the power save mode [T_a=25°C and output under no-load]

Table 25

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
S1D15715	I_{SS}(3)	V_{DD}=1.8V to 5.0V	—	0.01	5	μA	—
S1D15716	I_{SS}(3)	V_{DD}=1.8V to 5.0V	—	0.01	5		—
S1D15717	I_{SS}(3)	V_{DD}=1.8V to 5.0V	—	0.01	5		—

[Reference data 1]

◇Dynamic operating current (1) - When LCD display is turned on with external power supply being connected (All-white display)



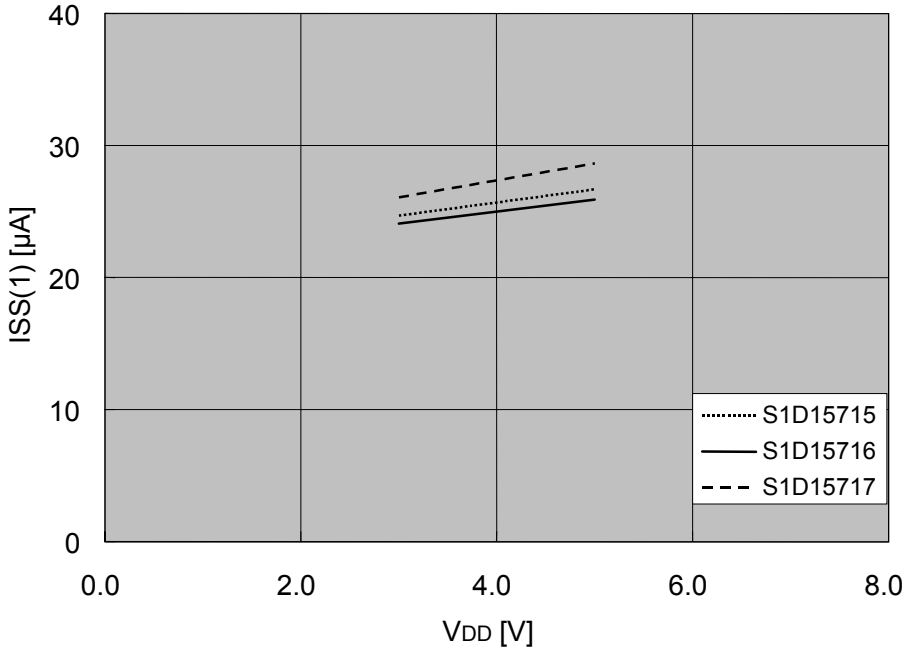
Conditions:
Built-in power supply OFF
External power supply ON
V_0-V_{SS}=7.0V
T_a=25°C

Display pattern : All-white

Remarks: See *10

Fig.16

◇Dynamic operating current (1) - When LCD display is turned on with external power supply being connected (Checker pattern display)



Conditions:
Built-in power supply OFF
External power supply ON
V_0-V_{SS}＝7.0V
T_a=25°C

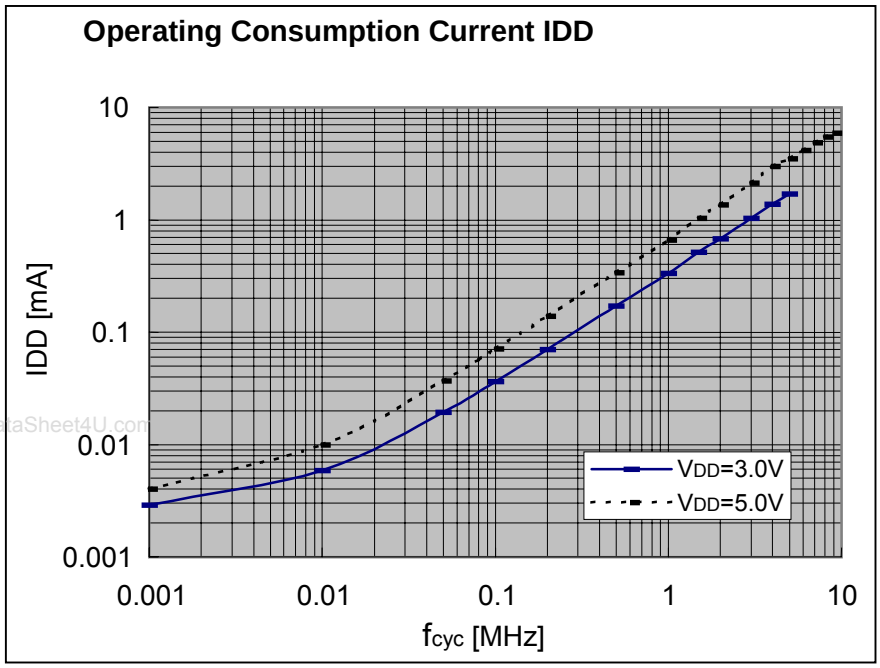
Display pattern : Checker

Remarks: See *10

Fig.17

[Reference data 2]

◇Dynamic operating current (3) - During an access is being made



This chart shows current consumption when the checker pattern write is constantly implemented in fCYC.
ISS (1) alone is consumed when an access is not taking place.

Conditions:
S1D15717
Built-in power supply OFF,
External power supply ON
V0-VSS＝7.0V
Ta=25°C

Fig.18

[Reference data 3]

◇Operating voltage range of VDD and V0 systems. *2

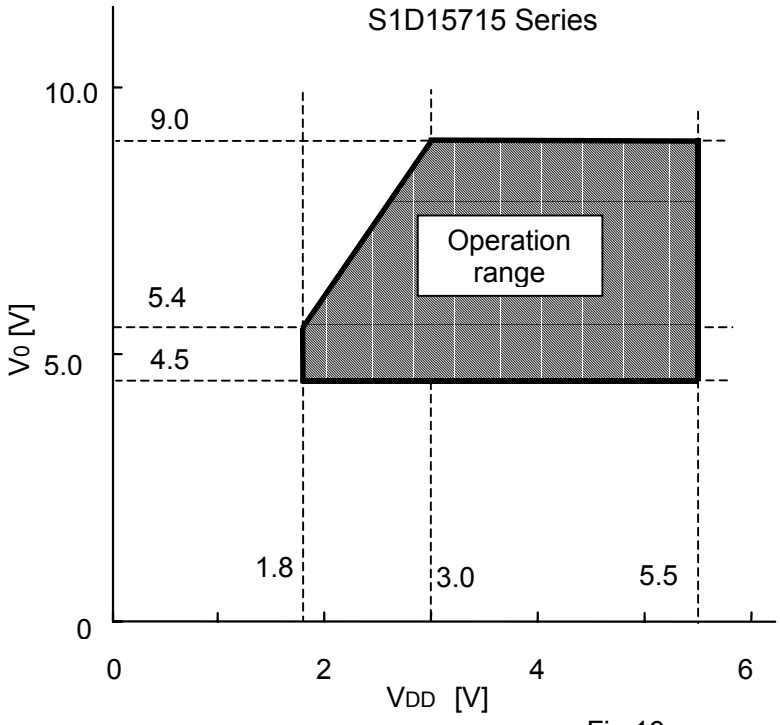


Fig.19

[Reference items]

*1 Although wide operating voltage range is warranted, and exemption to it is when an access made by MPU is accompanied with radical voltage fluctuations.
an access made by MPU is accompanied with radical voltage fluctuations.

*2 See Fig.21 for the operating voltage range of V_{DD} and V_0 systems. It is applicable when an external power supply is used.

*3 A0, D0 to D5, D6(SCL), D7(SI), $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$), $\overline{CS}$, CL, C86, P/S, $\overline{RES}$ and SEL pins.
V_{IH}=0.8×V_{DD} to V_{DD}, V_{IL}=V_{SS} to 0.2×V_{DD} when V_{DD}=1.8V to 2.7V.

*4 D0 to D7 pins.
I_{OH}=-0.25mA, I_{OL}=0.25mA when V_{DD}=1.8V to 2.7V.

*5 A0, $\overline{RD}$ (E), $\overline{WR}$(R/$\overline{W}$), $\overline{CS}$, C86, P/S, CL, $\overline{RES}$ and SEL pins.

*6 It is applicable when D0 to D5, D6(SCL) and D7(SI) pins are placed in high impedance.

*7 It represents the resistance value to be employed when 0.1V is applied across the output pin SEGn or COMn and respective power terminals (V_1, V_2, V_3 and V_4).
It must be selected within the operating voltage range (3).
R_{ON}=0.1V/ΔI (ΔI represents the current conducted when 0.1V is applied when the power supply is turned on).

*8 For the relationship between the oscillating frequency and frame frequency, refer to Table 6. External inputs listed in the standard value space are recommended values.

*9 Adjustment of the V_0 voltage regulator circuit must be done within the operating voltage range of the voltage follower circuit.

*10 The built-in oscillation circuit is used. It indicates current consumed by the independent IC when the display is turned on.
It does not include current consumed due to the LCD panel capacity or wiring capacity (driver output is under no-load).
These values are applicable when the access is not made by MPU.

10. AC CHARACTERISTICS

◇System bus read/write characteristics 1 (80-series MPU)

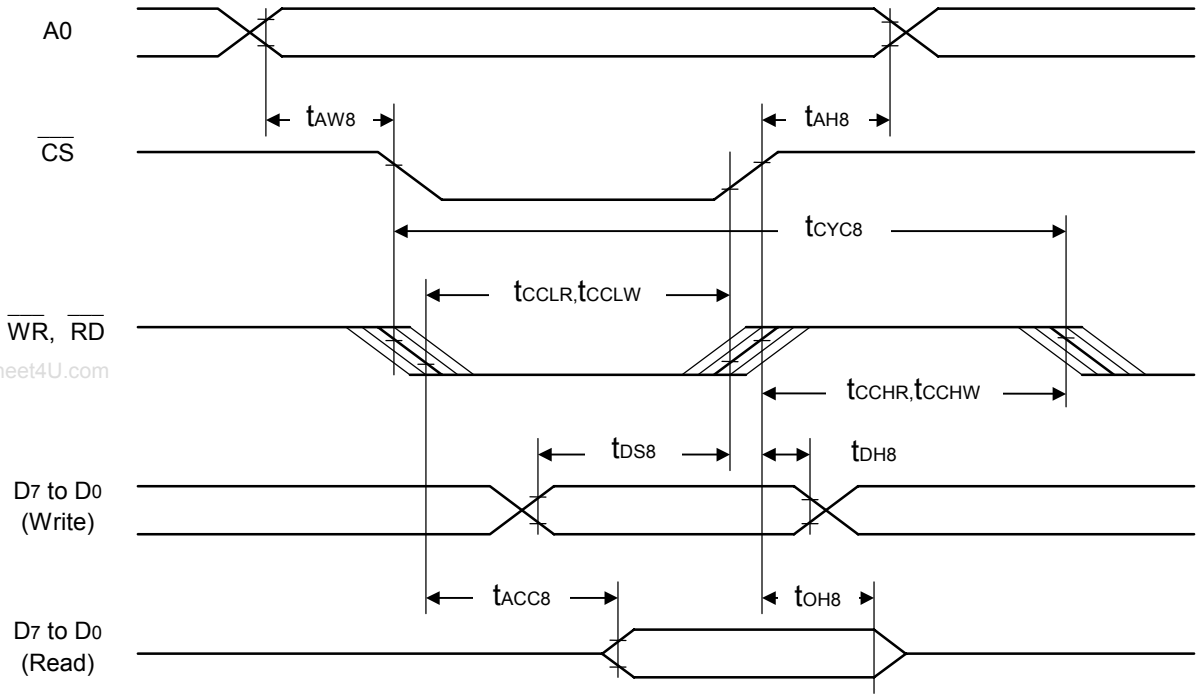


Fig.20

Table 26

V_{DD} = 4.5V to 5.5V, T_a = -40 to +85°C

Item	Signal	Symbol	Condition	Standard value		Unit
				Min.	Max.	
Address setup time	A0	t_{AW8}	—	0	—	ns
Address hold time		t_{AH8}	—	15	—	
System cycle time	—	t_{CYC8}	—	400	—	
Control LOW pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}	—	80	—	
Control LOW pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}	—	200	—	
Control HIGH pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}	—	100	—	
Control HIGH pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}	—	100	—	
Data setup time	D7 to D0	t_{DS8}	—	60	—	
Data hold time		t_{DH8}	—	25	—	
RD access time		t_{ACC8}	C_L=100pF	—	210	
Output disable time		t_{OH8}	—	5	100	

Table 27

V_{DD} = 2.7V to 4.5V, T_a = -40 to +85°C

Item	Signal	Symbol	Condition	Standard value		Unit
				Min.	Max.	
Address setup time	A0	t_{AW8}	—	0	—	ns
Address hold time		t_{AH8}	—	15	—	
System cycle time	—	t_{CYC8}	—	500	—	
Control LOW pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}	—	100	—	
Control LOW pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}	—	250	—	
Control HIGH pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}	—	100	—	
Control HIGH pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}	—	100	—	
Data setup time	D7 to D0	t_{DS8}	—	120	—	
Data hold time		t_{DH8}	—	20	—	
RD access time		t_{ACC8}	C_L=100pF	—	230	
Output disable time		t_{OH8}	—	5	100	

Table 28

V_{DD} = 1.8V to 2.7V, T_a = -40 to +85°C

Item	Signal	Symbol	Condition	Standard value		Unit
				Min.	Max.	
Address setup time	A0	t_{AW8}	—	0	—	ns
Address hold time		t_{AH8}	—	10	—	
System cycle time	—	t_{CYC8}	—	1000	—	
Control LOW pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}	—	150	—	
Control LOW pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}	—	350	—	
Control HIGH pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}	—	150	—	
Control HIGH pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}	—	150	—	
Data setup time	D7 to D0	t_{DS8}	—	120	—	
Data hold time		t_{DH8}	—	20	—	
RD access time		t_{ACC8}	C_L=100pF	—	310	
Output disable time		t_{OH8}	—	10	200	

- The rise and fall times (tr and tf) of the input signal are specified for less than 15ns.
- When using the system cycle time at high speed, they are specified for $(t_r+t_f) \le (t_{CYC8}-t_{CCLW}-t_{CCHW})$ or $(t_r+t_f) \le (t_{CYC8}-t_{CCLR}-t_{CCHR})$.
- All timings are specified based on the 20 and 80% of V_{DD}.
- t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS}$ is at LOW level and $\overline{WR}$, $\overline{RD}$ are at the LOW level.
- The timing for A_0 is specified for the overlap period when $\overline{CS}$ is at LOW level and $\overline{WR}$, $\overline{RD}$ are at the LOW level.

◇System bus read/write characteristics 2 (68-series MPU)

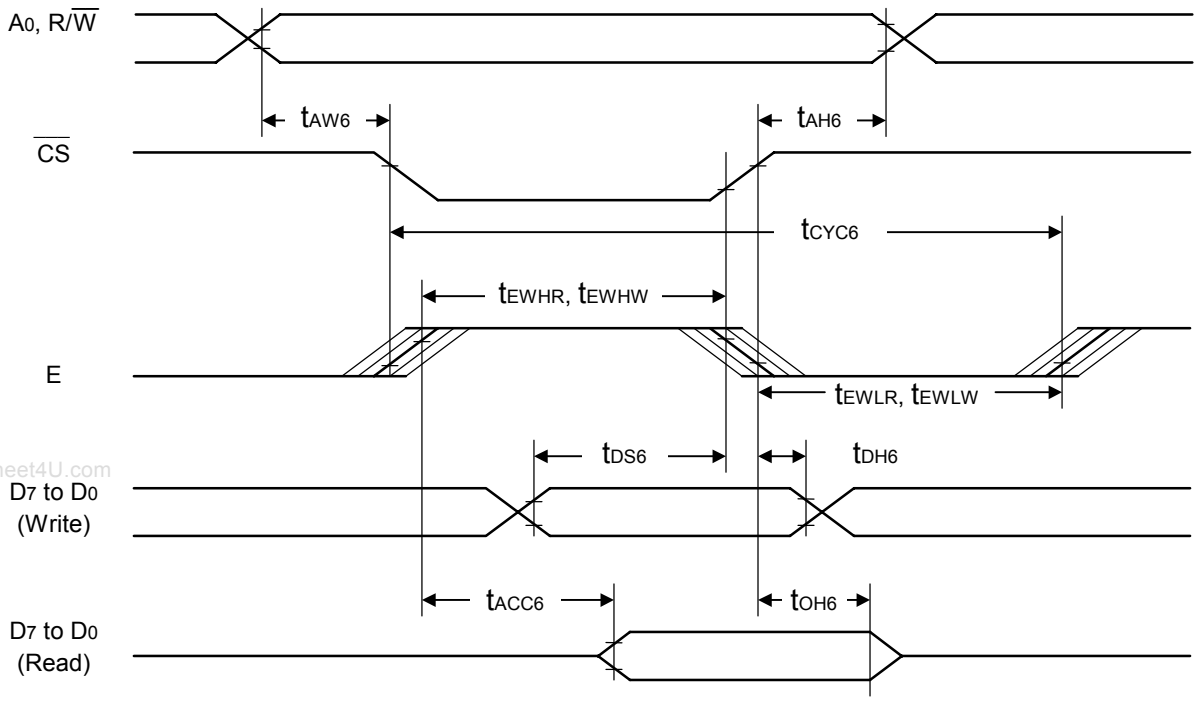


Fig.21

Table 29

V_{DD} = 4.5V to 5.5V, T_a = -40 to +85°C

Item		Signal	Symbol	Condition	Standard value		Unit
					Min.	Max.	
Address setup time		A0,	t_{AW6}	—	0	—	ns
Address hold time		$\overline{WR}$	t_{AH6}	—	5	—	
System cycle time		—	t_{CYC6}	—	400	—	
Enable HIGH pulse width	Read	E	t_{EWHR}	—	200	—	
	Write		t_{EWHW}	—	80	—	
Enable LOW pulse width	Read	—	t_{EWLR}	—	100	—	
	Write		t_{EWLW}	—	100	—	
Data setup time		D7 to D0	t_{DS6}	—	60	—	
Data hold time			t_{DH6}	—	25	—	
RD access time			t_{ACC6}	C_L=100pF	—	210	
Output disable time			t_{OH6}	—	5	100	

Table 30

V_{DD} = 2.7V to 4.5V, T_a = -40 to +85°C

Item		Signal	Symbol	Condition	Standard value		Unit
					Min.	Max.	
Address setup time		A0,	t_{AW6}	—	0	—	ns
Address hold time		$\overline{WR}$	t_{AH6}	—	5	—	
System cycle time		—	t_{CYC6}	—	500	—	
Enable HIGH pulse width	Read	E	t_{EWHR}	—	250	—	
	Write		t_{EWHW}	—	100	—	
Enable LOW pulse width	Read	—	t_{EWLR}	—	100	—	
	Write		t_{EWLW}	—	100	—	
Data setup time		D7 to D0	t_{DS6}	—	70	—	
Data hold time			t_{DH6}	—	20	—	
RD access time			t_{ACC6}	C_L=100pF	—	230	
Output disable time			t_{OH6}	—	5	100	

Table 31

V_{DD} = 1.8V to 2.7V, T_a = -40 to +85°C

Item		Signal	Symbol	Condition	Standard value		Unit
					Min.	Max.	
Address setup time		A0,	t_{AW6}	—	0	—	ns
Address hold time		$\overline{WR}$	t_{AH6}	—	5	—	
System cycle time		—	t_{CYC6}	—	1000	—	
Enable HIGH pulse width	Read	E	t_{EWHR}	—	350	—	
	Write		t_{EWHW}	—	150	—	
Enable LOW pulse width	Read	—	t_{EWLR}	—	150	—	
	Write		t_{EWLW}	—	150	—	
Data setup time		D7 to D0	t_{DS6}	—	120	—	
Data hold time			t_{DH6}	—	20	—	
RD access time			t_{ACC6}	C_L=100pF	—	310	
Output disable time			t_{OH6}	—	10	200	

- The rise and fall times (t_r and t_f) of the input signal are specified for less than 15ns.
  When using the system cycle time at high speed, they are specified for (t_r+t_f) ≤ (t_{CYC6}-t_{EWLW}-t_{EWHW}) or (t_r+t_f) ≤ (t_{CYC6}-t_{EWLR}-t_{EWHR}).
- All timings are specified based on the 20 and 80% of V_{DD}.
- t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS}$ is at LOW level and E is at the HIGH level.
- The timing of A0 is specified for the overlap period when $\overline{CS}$ is at LOW level and E is at the HIGH level.

◇Serial interface characteristics

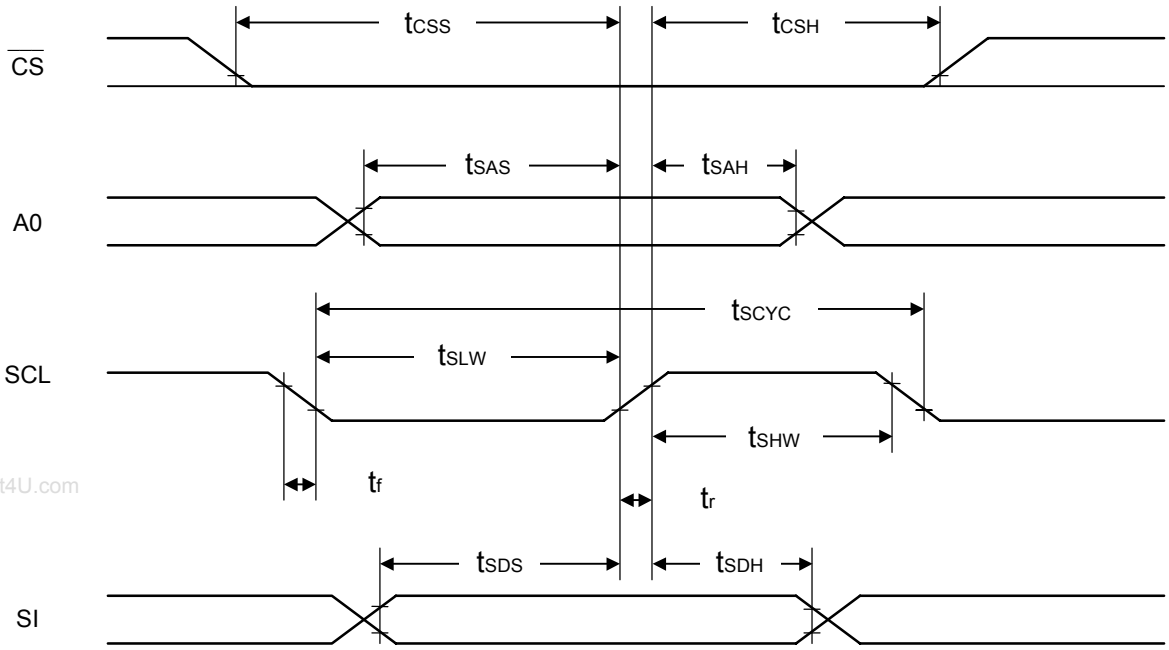


Fig.22

Table 32

V_{DD} = 4.5V to 5.5V, T_a = -40 to +85°C

Item	Signal	Symbol	Condition	Standard value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}	—	125	—	ns
SCL HIGH pulse width		t_{SHW}	—	50	—	
SCL LOW pulse width		t_{SLW}	—	50	—	
Address setup time	A0	t_{SAS}	—	75	—	
Address hold time		t_{SAH}	—	75	—	
Data setup time	SI	t_{SDS}	—	50	—	
Data hold time		t_{SDH}	—	50	—	
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}	—	75	—	
		t_{CSH}	—	75	—	

Table 33

V_{DD} = 2.7V to 4.5V, T_a = -40 to +85°C

Item	Signal	Symbol	Condition	Standard value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}	—	125	—	ns
SCL HIGH pulse width		t_{SHW}	—	50	—	
SCL LOW pulse width		t_{SLW}	—	50	—	
Address setup time	A0	t_{SAS}	—	75	—	
Address hold time		t_{SAH}	—	75	—	
Data setup time	SI	t_{SDS}	—	50	—	
Data hold time		t_{SDH}	—	50	—	
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}	—	75	—	
		t_{CSH}	—	75	—	

Table 34

V_{DD} = 1.8V to 2.7V, T_a = -40 to +85°C

Item	Signal	Symbol	Condition	Standard value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}	—	200	—	ns
SCL HIGH pulse width		t_{SHW}	—	75	—	
SCL LOW pulse width		t_{SLW}	—	75	—	
Address setup time	A0	t_{SAS}	—	75	—	
Address hold time		t_{SAH}	—	75	—	
Data setup time	SI	t_{SDS}	—	50	—	
Data hold time		t_{SDH}	—	50	—	
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}	—	100	—	
		t_{CSH}	—	100	—	

- The rise and fall times (t_r and t_f) of the input signal are specified for less than 15ns.
- Every timing is specified on the basis of 20% and 80% of V_{DD}.

◇Reset input timing

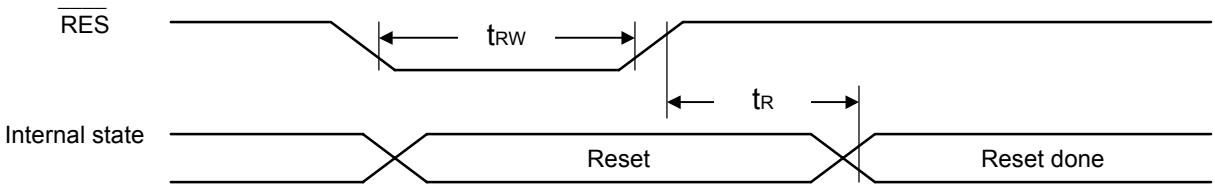


Fig.23

Table 35

V_{DD} = 4.5V to 5.5V, Ta = -40 to +85°C

Item	Signal	Symbol	Condition	Standard value		Unit
				Min.	Max.	
Reset time	—	t_R	—	—	1000	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}	—	1000	—	

Table 36

V_{DD} = 2.7V to 4.5V, Ta = -40 to +85°C

Item	Signal	Symbol	Condition	Standard value		Unit
				Min.	Max.	
Reset time	—	t_R	—	—	1000	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}	—	1000	—	

Table 37

V_{DD} = 1.8V to 2.7V, Ta = -40 to +85°C

Item	Signal	Symbol	Condition	Standard value		Unit
				Min.	Max.	
Reset time	—	t_R	—	—	1500	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}	—	1500	—	

- The rise and fall times (t_r and t_f) of the input signal are specified for less than 15ns.
- Every timing is specified on the basis of 20% and 80% of V_{DD}.

11. MPU INTERFACE (REFERENCE EXAMPLES)

The S1D15715 Series can be directly connected to the 80-Series MPU or to the 68-Series MPU. Furthermore, by employment of the serial interface, they can be operated by smaller number of signal lines.
After initialization has been made by the $\overline{RES}$ pin, each input pin of the S1D15715 Series needs to be controlled properly.

(1) 80-Series MPU

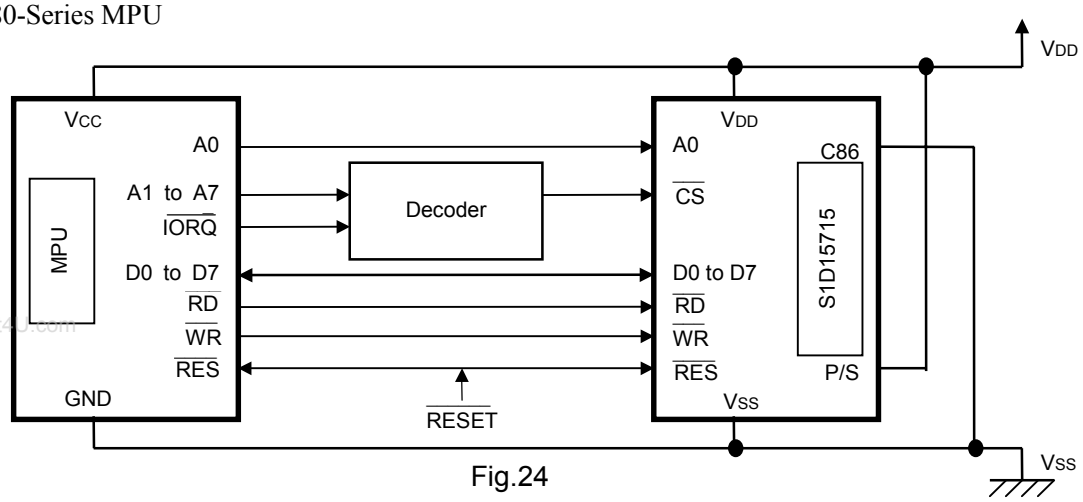


Fig.24

(2) 68-Series MPU

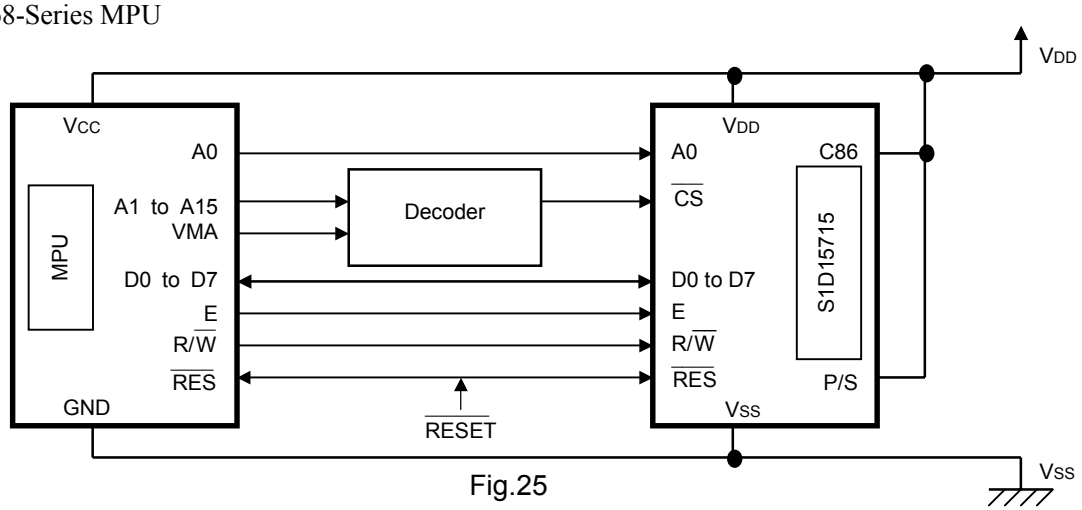


Fig.25

(3) Serial interface

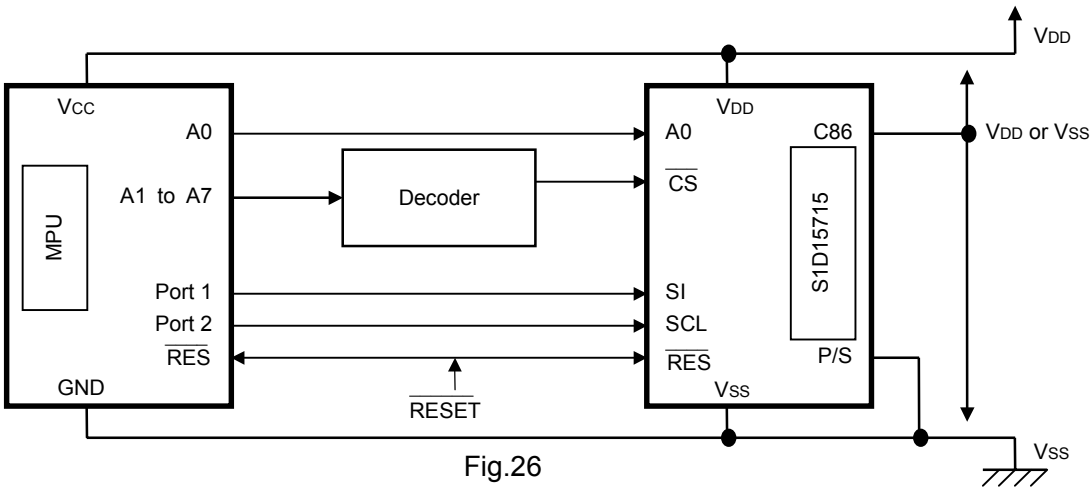


Fig.26

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
HEADQUARTERS
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 FAX: +1-408-922-0238

SALES OFFICES
West
1960 E.Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 FAX: +1-310-955-5400

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 FAX: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 FAX: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020 FAX: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH
HEADQUARTERS
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-(0)89-14005-0 FAX: +49-(0)89-14005-110

DÜSSELDORF BRANCH OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)2171-5045-0 FAX: +49-(0)2171-5045-10

UK & IRELAND BRANCH OFFICE
Unit 2.4, Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 FAX: +44-(0)1344-381701

FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 FAX: +33-(0)1-64862355

BARCELONA BRANCH OFFICE
Barcelona Design Center
Edificio Testa, Avda. Alcalde Barrils num. 64-68
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490 FAX: +34-93-544-2491

Scotland Design Center
Integration House, The Alba Campus
Livingston West Lothian, EH54 7EG, SCOTLAND
Phone: +44-1506-605040 FAX: +44-1506-605041

ASIA

EPSON (CHINA) CO., LTD.
23F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: 64106655 FAX: 64107319

SHANGHAI BRANCH
7F, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: 86-21-5423-5577 FAX: 86-21-5423-4677

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110
Phone: 02-8786-6688 FAX: 02-8786-6660

HSINCHU OFFICE
No. 99, Jiangong Road,
Hsinchu City 300
Phone: +886-3-573-9900 FAX: +886-3-573-9169

EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-6337-7911 FAX: +65-6334-2716

SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: 02-784-6027 FAX: 02-767-3677

GUMI OFFICE
6F, Good Morning Securities Bldg., 56 Songjeong-Dong,
Gumi-City, Seoul, 730-090, KOREA
Phone: 054-454-6027 FAX: 054-454-6093

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

ED International Marketing Department
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 FAX: +81-(0)42-587-5117

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