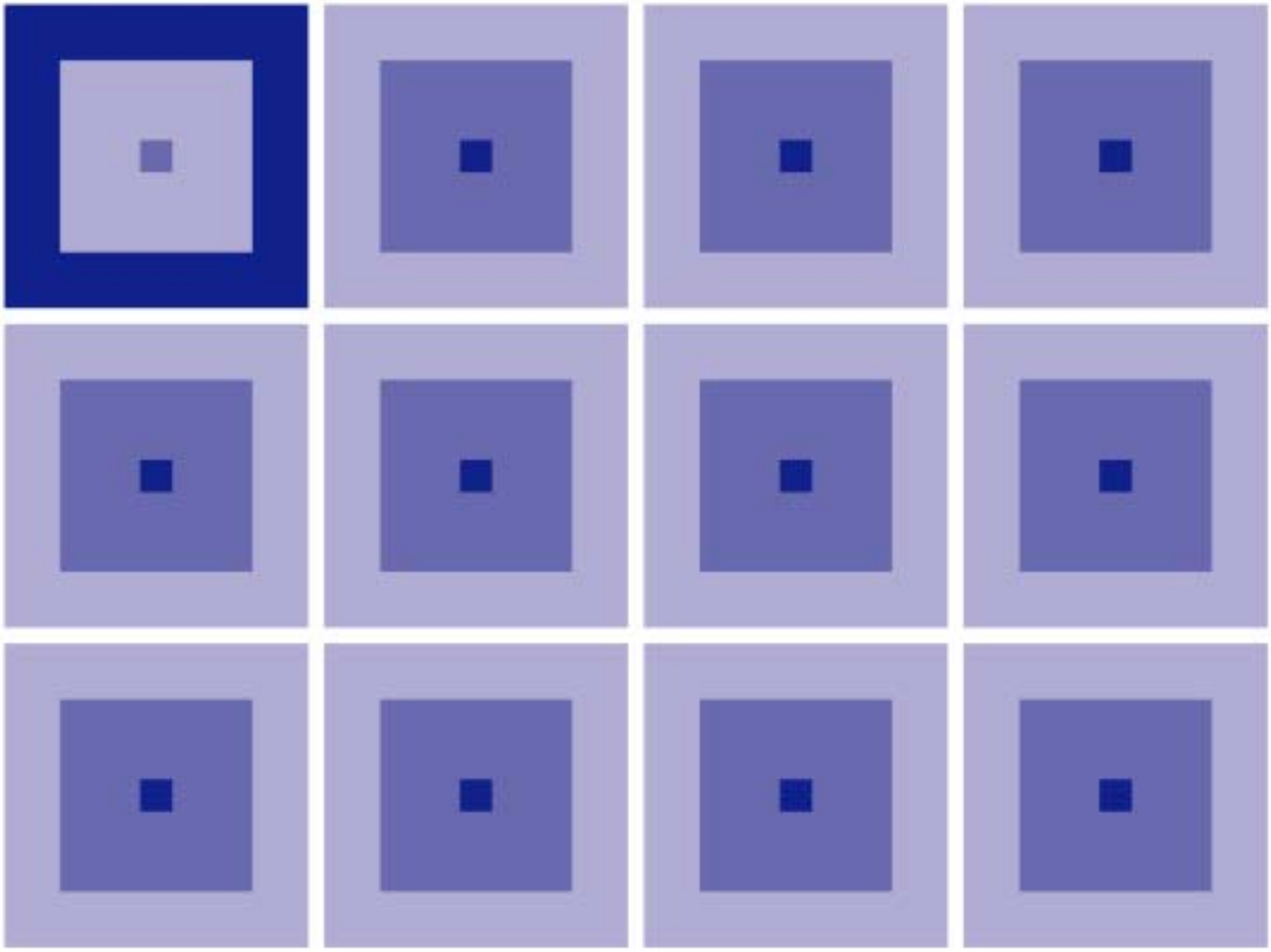
EPSON
EXCEED YOUR VISION

LCD Driver ICs

S1D19122 Series

Technical Manual



SEIKO EPSON CORPORATION

NOTICE

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

General Rules

Scope of Application

The Technical Manual presented herein apply to the S1D19122 Series of ICs made by Seiko Epson Corporation.

Specification Changes and Consultation

If the need arises to revise the specifications presented herein, consultations shall be held promptly with the other party, and an agreement between the two parties shall be reached before the specifications can be revised. Furthermore, if a problem arises with respect to matters not stipulated in the specifications, it shall be resolved in good faith through consultation between the two parties.

− Contents −

1. Overview

The S1D19122 Series (hereinafter referred to simply as the “S1D19122”) is a single-chip amorphous Si-TFT color LCD driver incorporating a 256-gray-scale-level VRAM, designed to achieve the high picture quality with low power consumption that is required for portable equipment. As it incorporates a 240-output gate driver, a 320 (pixel)-output source driver, and all of the power-supply circuits required for display, the user can configure an amorphous Si-TFT color LCD panel module having a display size of up to 320 (pixels) × 240 dots, with the minimum possible components.

The driver can be connected directly to the MPU bus. It stores the gray scale display data sent from the MPU in its internal display VRAM, and generates LCD drive signals independently of the MPU. Furthermore, it can be connected directly to an LCDC, permitting the data to be written into the internal VRAM without MPU intervention. It provides 960 LCD drive outputs, and its internal display VRAM provides display capability of 320 (pixels) × 240 (lines) × 24 (bits: 16.8 M colors). The display area in the source direction can be set in the range from 119 to 320 using a command. The RGB bits of the internal VRAM, 8 R bits, 8 G bits, and 8 B bits, correspond on a one-for-one basis to each pixel on the LCDpanel, enabling display of 320 (pixels) × 240 (lines).

Writing from the MPU to the internal VRAM can be performed with minimal power consumption, as no external operating clocks are needed. In addition, the driver features a slim profile, making it suitable for narrow-framed LCD panels.

2. Features

- Number of LCD drive outputs Source driver: 960 outs; gated driver: 240 outs
- Number of drive display lines Maximum of 240
- Color display in 256 gray scale levels for RGB and 16,777,216 shades of color
- Video memory for direct data display (normally white LCD)

  VRAM-bit data “00000000-00000000-00000000”･･･ON (maximum voltage) Black
  VRAM-bit data “11111111-00000000-00000000”･･･OFF (minimum voltage) Red
  VRAM-bit data “00000000-11111111-00000000”･･･OFF (minimum voltage) Green
  VRAM-bit data “00000000-00000000-11111111”･･･OFF (minimum voltage) Blue
  VRAM-bit data “11111111-11111111-11111111”･･･OFF (minimum voltage) White
  * During display in normal mode

- Partial-display function Display can be partly turned off for power-saving operation.
- Internal VRAM capacity 320×240×24 = 1,843,200 bits
- MPU interface

  Directly connectable to MPUs that have an 80-series MPU parallel interface
  Directly connectable to MPUs that have a 68-series MPU parallel interface
  Directly connectable to MPUs that have a 4-wire, 8-bit data serial interface
  Directly connectable to MPUs that have a 3-wire, 9-bit data serial interface

- LCDC interface

  Directly connectable to an LCDC interface for writing gray scale display data into the internal VRAM

- Wide range of command functions (area scroll function, page & column automatic increment function, and power control function)
- Drive-method setup function (V_{COM} inverted drive, frame/line inverted drive)
- Self-initialization function
- LCD module system self-diagnostic function
- Power-supply blocks

Logic input/output signal & control block	V_{DDI} = 1.65 to 3.3V
Logic power supply	V_{CORE} = 1.65 to 1.95V
Booster power-supply block	V_{DD} = 2.3 to 3.3V
Internal power-supply circuit	V_{DD}
LCD block (source)	V_{DDHS} = 2.4 to 5.5V
LCD block (gate)	V_{EE} to V_{DDHG}= -16 to 16V

- Built-in oscillator circuit Oscillator circuit with built-in RC network
- Slim chip profile
- Shipping form Chip form
- This product is not designed to resist radiation or intense light. Please refer to Chapter 14, “Precautions.”

3. List of Product Types

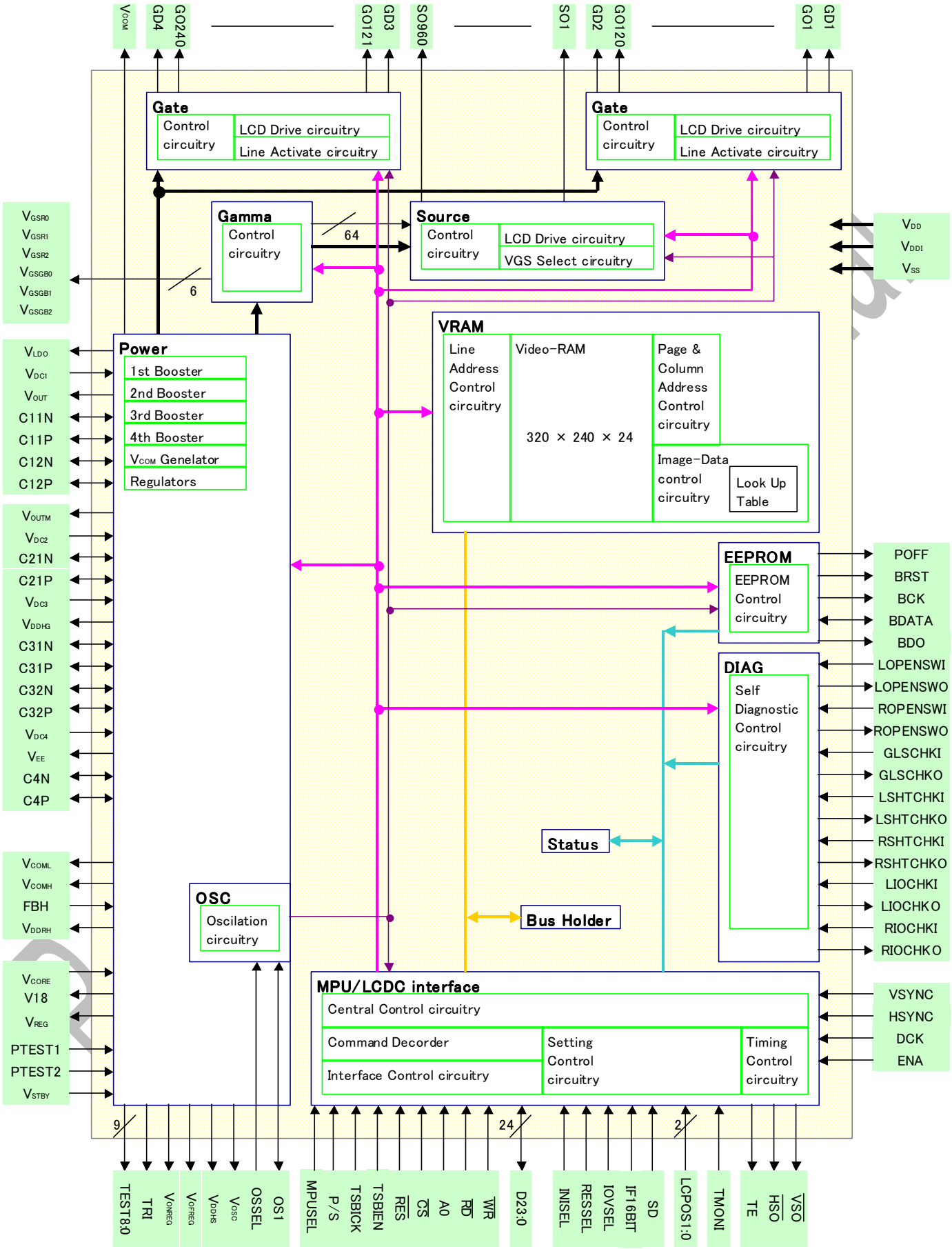
The table below lists the types of products conforming to the specifications presented herein.

◇ S1D19122 Series

Product type name	Die.No	Simplified name	Differences and limitations
S1D19122D00B000	D191MD0B	D00B	

In the pages to follow, the product type name used is “S1D19122” for the contents common to this series; a simplified name is used when type-dependent contents are described.

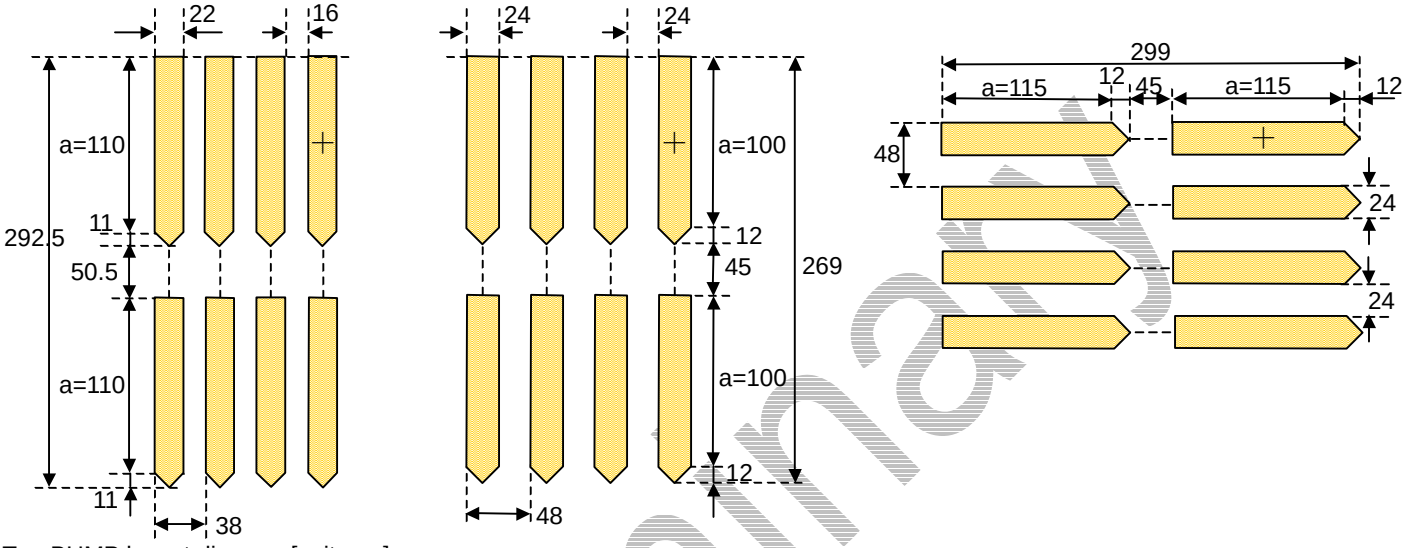
4. Block Diagram



5. Pin Layout and Coordinates

5-1. Pin Layout Diagram

Chip size: 26.82 × 2.25 mm Chip thickness: 400 µm ± 25 µm Die No.: D191MD0B

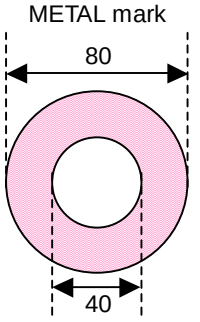


Top BUMP layout diagram [unit: µm]

The 1/2 point of 'a' is the center coordinate position of BUMP.

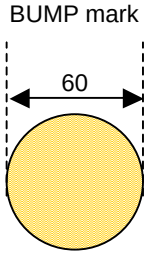
BUMP size	Tolerance	± 4 µm	
	Center at top	22 × 110 µm	<BUMP No.423 to 1461>
	Both sides at top	24 × 100 µm	<BUMP No.327 to 422, 1462 to 1557>
	Short side	24 × 115 µm	<BUMP No.273 to 326, 1558 to 1611>
	Bottom side	60 × 80 µm	<BUMP No.1 to 272> I/O
Space between bumps	Tolerance	± 4 µm	
(Long side)	X direction	16 µm	<BUMP No.423 to 1461>
(Long side)		24 µm	<BUMP No.327 to 423,1461 to 1557>
(Short side)		45 µm	<BUMP No.273 to 326,1558 to 1611>
(Long side)	Y direction	45 µm	<BUMP No.327 tp 422,1462 to 1557>
(Long side)		50.5 µm	<BUMP No.423 to 896,988 to 1461>
(Short side)		24 µm	<BUMP No.273 to 326,1558 to 1611>
BUMP pitch	Gate	48 µm	<BUMP No.281 to 324, 332 to 410, 1474 to 1553, 1560 to 1603>
	Source	38 µm	<BUMP No.429 to 908, 976 to 1455>
BUMP height		15 ± 3 µm	<for reference>

Alignment-mark shape and center coordinates [unit: µm]



(13262.69 , -759.79)

(-13262.69 , -759.79)



(13162.69 , -759.79)

(-13162.69 , -759.79)

5-2. Pin Coordinates

5-2-1. Pins on Input Side

BUMP No.	Signal Name	X Coordinate [µm]	Y Coordinate [µm]	X BUMP [µm]	Y BUMP [µm]	BUMP No.	Signal Name	X Coordinate [µm]	Y Coordinate [µm]	X BUMP [µm]	Y BUMP [µm]
1	DUMMY	-13122	-1005	60	80	76	$\overline{WR}$	-6352	-1005	60	80
2	TESTDUM	-13014	-1005	60	80	77	V_{SS}	-6244	-1005	60	80
3	TESTDUM	-12906	-1005	60	80	78	IOVSEL	-6136	-1005	60	80
4	V_{OSC}	-12798	-1005	60	80	79	V_{DDI}	-6028	-1005	60	80
5	V_{REG}	-12690	-1005	60	80	80	V_{DDI}	-5958	-1005	60	80
6	TRI	-12582	-1005	60	80	81	LSD	-5850	-1005	60	80
7	V_{LDO}	-12474	-1005	60	80	82	SD	-5742	-1005	60	80
8	V_{LDO}	-12404	-1005	60	80	83	LD0	-5634	-1005	60	80
9	V_{LDO}	-12334	-1005	60	80	84	D0	-5526	-1005	60	80
10	V_{LDO}	-12264	-1005	60	80	85	LD1	-5418	-1005	60	80
11	V_{LDO}	-12194	-1005	60	80	86	D1	-5310	-1005	60	80
12	V_{DC1}	-12086	-1005	60	80	87	LD2	-5202	-1005	60	80
13	V_{DC1}	-12016	-1005	60	80	88	D2	-5094	-1005	60	80
14	V_{DC1}	-11946	-1005	60	80	89	LD3	-4986	-1005	60	80
15	V_{DC1}	-11876	-1005	60	80	90	D3	-4878	-1005	60	80
16	V_{DD}	-11768	-1005	60	80	91	LD4	-4770	-1005	60	80
17	V_{DD}	-11698	-1005	60	80	92	D4	-4662	-1005	60	80
18	V_{DD}	-11628	-1005	60	80	93	LD5	-4554	-1005	60	80
19	V_{SS}	-11520	-1005	60	80	94	D5	-4446	-1005	60	80
20	V_{SS}	-11450	-1005	60	80	95	LD6	-4338	-1005	60	80
21	V_{SS}	-11380	-1005	60	80	96	D6	-4230	-1005	60	80
22	C11N	-11272	-1005	60	80	97	LD7	-4122	-1005	60	80
23	C11N	-11202	-1005	60	80	98	D7	-4014	-1005	60	80
24	C11N	-11132	-1005	60	80	99	V_{SS}	-3906	-1005	60	80
25	C11N	-11062	-1005	60	80	100	V_{SS}	-3836	-1005	60	80
26	C11P	-10954	-1005	60	80	101	V_{DDI}	-3728	-1005	60	80
27	C11P	-10884	-1005	60	80	102	V_{DDI}	-3658	-1005	60	80
28	C11P	-10814	-1005	60	80	103	D8	-3550	-1005	60	80
29	C11P	-10744	-1005	60	80	104	D9	-3442	-1005	60	80
30	C12N	-10636	-1005	60	80	105	D10	-3334	-1005	60	80
31	C12N	-10566	-1005	60	80	106	D11	-3226	-1005	60	80
32	C12N	-10496	-1005	60	80	107	D12	-3118	-1005	60	80
33	C12N	-10426	-1005	60	80	108	D13	-3010	-1005	60	80
34	C12P	-10318	-1005	60	80	109	D14	-2902	-1005	60	80
35	C12P	-10248	-1005	60	80	110	D15	-2794	-1005	60	80
36	C12P	-10178	-1005	60	80	111	D16	-2686	-1005	60	80
37	C12P	-10108	-1005	60	80	112	D17	-2578	-1005	60	80
38	V_{OUT}	-10000	-1005	60	80	113	D18	-2470	-1005	60	80
39	V_{OUT}	-9930	-1005	60	80	114	D19	-2362	-1005	60	80
40	V_{OUT}	-9860	-1005	60	80	115	D20	-2254	-1005	60	80
41	V_{OUT}	-9790	-1005	60	80	116	D21	-2146	-1005	60	80
42	V_{OUT}	-9720	-1005	60	80	117	D22	-2038	-1005	60	80
43	V_{DDHS}	-9612	-1005	60	80	118	D23	-1930	-1005	60	80
44	V_{DDRH}	-9504	-1005	60	80	119	DUMMY	-1822	-1005	60	80
45	V_{18}	-9396	-1005	60	80	120	DUMMY	-1599	-1005	60	80
46	V_{18}	-9326	-1005	60	80	121	DUMMY	-1529	-1005	60	80
47	V_{18}	-9256	-1005	60	80	122	DUMMY	-1415	-1005	60	80
48	V_{18}	-9186	-1005	60	80	123	DUMMY	-1345	-1005	60	80
49	V_{CORE}	-9078	-1005	60	80	124	DUMMY	-1231	-1005	60	80
50	V_{CORE}	-9008	-1005	60	80	125	DUMMY	-1161	-1005	60	80
51	V_{CORE}	-8938	-1005	60	80	126	DUMMY	-1047	-1005	60	80
52	V_{CORE}	-8868	-1005	60	80	127	DUMMY	-977	-1005	60	80
53	V_{DDI}	-8760	-1005	60	80	128	DUMMY	-863	-1005	60	80
54	V_{DDI}	-8690	-1005	60	80	129	DUMMY	-793	-1005	60	80
55	V_{DDI}	-8620	-1005	60	80	130	DUMMY	-679	-1005	60	80
56	V_{DD}	-8512	-1005	60	80	131	DUMMY	-609	-1005	60	80
57	V_{STBY}	-8404	-1005	60	80	132	DUMMY	-495	-1005	60	80
58	PTEST1	-8296	-1005	60	80	133	DUMMY	-425	-1005	60	80
59	PTEST2	-8188	-1005	60	80	134	DUMMY	-311	-1005	60	80
60	V_{SS}	-8080	-1005	60	80	135	DUMMY	-241	-1005	60	80
61	POFF	-7972	-1005	60	80	136	DUMMY	-127	-1005	60	80
62	BCK	-7864	-1005	60	80	137	DUMMY	-57	-1005	60	80
63	BDATA	-7756	-1005	60	80	138	DUMMY	57	-1005	60	80
64	BRST	-7648	-1005	60	80	139	DUMMY	127	-1005	60	80
65	BDO	-7540	-1005	60	80	140	DUMMY	241	-1005	60	80
66	TE	-7432	-1005	60	80	141	DUMMY	311	-1005	60	80
67	VSYNC	-7324	-1005	60	80	142	DUMMY	425	-1005	60	80
68	HSYNC	-7216	-1005	60	80	143	DUMMY	495	-1005	60	80
69	DCK	-7108	-1005	60	80	144	DUMMY	609	-1005	60	80
70	ENA	-7000	-1005	60	80	145	DUMMY	679	-1005	60	80
71	$\overline{CS}$	-6892	-1005	60	80	146	DUMMY	793	-1005	60	80
72	A0	-6784	-1005	60	80	147	DUMMY	863	-1005	60	80
73	V_{SS}	-6676	-1005	60	80	148	DUMMY	977	-1005	60	80
74	$\overline{RD}$	-6568	-1005	60	80	149	DUMMY	1047	-1005	60	80
75	V_{SS}	-6460	-1005	60	80	150	DUMMY	1161	-1005	60	80

BUMP No.	Signal Name	X Coordinate [µm]	Y Coordinate [µm]	X BUMP [µm]	Y BUMP [µm]	BUMP No.	Signal Name	X Coordinate [µm]	Y Coordinate [µm]	X BUMP [µm]	Y BUMP [µm]
151	DUMMY	1231	-1005	60	80	213	V_{COMH}	7722	-1005	60	80
152	DUMMY	1345	-1005	60	80	214	V_{COML}	7830	-1005	60	80
153	DUMMY	1415	-1005	60	80	215	V_{OUTM}	7960	-1005	60	80
154	DUMMY	1529	-1005	60	80	216	V_{OUTM}	8030	-1005	60	80
155	DUMMY	1599	-1005	60	80	217	V_{OUTM}	8100	-1005	60	80
156	V_{GSR0}	1800	-1005	60	80	218	C21N	8208	-1005	60	80
157	V_{GSR1}	1908	-1005	60	80	219	C21N	8278	-1005	60	80
158	V_{GSR2}	2016	-1005	60	80	220	C21N	8348	-1005	60	80
159	V_{GSGB0}	2124	-1005	60	80	221	C21P	8478	-1005	60	80
160	V_{GSGB1}	2232	-1005	60	80	222	C21P	8548	-1005	60	80
161	V_{GSGB2}	2340	-1005	60	80	223	C21P	8618	-1005	60	80
162	TSBIEN	2448	-1005	60	80	224	V_{ONREG}	8726	-1005	60	80
163	TSBICK	2556	-1005	60	80	225	V_{ONREG}	8796	-1005	60	80
164	DUMMY	2664	-1005	60	80	226	V_{DC3}	8904	-1005	60	80
165	DUMMY	2772	-1005	60	80	227	V_{DC3}	8974	-1005	60	80
166	DUMMY	2880	-1005	60	80	228	V_{OUT}	9082	-1005	60	80
167	DUMMY	2988	-1005	60	80	229	V_{OUT}	9152	-1005	60	80
168	DUMMY	3096	-1005	60	80	230	V_{DD}	9260	-1005	60	80
169	V_{DDI}	3204	-1005	60	80	231	V_{DD}	9330	-1005	60	80
170	V_{DDI}	3274	-1005	60	80	232	V_{DC4}	9438	-1005	60	80
171	V_{SS}	3382	-1005	60	80	233	V_{DC4}	9508	-1005	60	80
172	V_{SS}	3452	-1005	60	80	234	V_{OFREG}	9616	-1005	60	80
173	$\overline{RES}$	3560	-1005	60	80	235	V_{OFREG}	9686	-1005	60	80
174	MPUSEL	3668	-1005	60	80	236	V_{SS}	9794	-1005	60	80
175	P/S	3776	-1005	60	80	237	V_{SS}	9864	-1005	60	80
176	LCPOS0	3884	-1005	60	80	238	C32N	9972	-1005	60	80
177	LCPOS1	3992	-1005	60	80	239	C32N	10042	-1005	60	80
178	INISEL	4100	-1005	60	80	240	C31N	10150	-1005	60	80
179	RESSEL	4208	-1005	60	80	241	C31N	10220	-1005	60	80
180	TMONI	4316	-1005	60	80	242	C31P	10328	-975	60	80
181	OSSEL	4424	-1005	60	80	243	C31P	10398	-975	60	80
182	OS1	4532	-1005	60	80	244	C32P	10506	-975	60	80
183	DUMMY	4640	-1005	60	80	245	C32P	10576	-975	60	80
184	V_{SS}	4748	-1005	60	80	246	V_{DDHG}	10746	-975	60	80
185	V_{DDI}	4856	-1005	60	80	247	V_{DDHG}	10816	-975	60	80
186	$\overline{VSO}$	4964	-1005	60	80	248	V_{DDHG}	10886	-975	60	80
187	$\overline{HSO}$	5072	-1005	60	80	249	DUMMY	11001	-975	60	80
188	TEST0	5180	-1005	60	80	250	C4P	11116	-975	60	80
189	TEST1	5288	-1005	60	80	251	C4P	11186	-975	60	80
190	TEST2	5396	-1005	60	80	252	C4P	11256	-975	60	80
191	TEST3	5504	-1005	60	80	253	DUMMY	11371	-975	60	80
192	TEST4	5612	-1005	60	80	254	C4N	11486	-975	60	80
193	TEST5	5720	-1005	60	80	255	C4N	11556	-975	60	80
194	TEST6	5828	-1005	60	80	256	C4N	11626	-975	60	80
195	TEST7	5936	-1005	60	80	257	DUMMY	11741	-975	60	80
196	TEST8	6044	-1005	60	80	258	V_{EE}	11856	-975	60	80
197	V_{SS}	6152	-1005	60	80	259	V_{EE}	11926	-975	60	80
198	V_{DDI}	6260	-1005	60	80	260	V_{EE}	11996	-975	60	80
199	IF16BIT	6368	-1005	60	80	261	DUMMY	12111	-1005	60	80
200	V_{CORE}	6476	-1005	60	80	262	V_{DD}	12226	-1005	60	80
201	V_{CORE}	6546	-1005	60	80	263	V_{DD}	12296	-1005	60	80
202	DUMMY	6654	-1005	60	80	264	V_{DD}	12366	-1005	60	80
203	DUMMY	6762	-1005	60	80	265	V_{SS}	12474	-1005	60	80
204	V_{LDO}	6902	-1005	60	80	266	V_{SS}	12544	-1005	60	80
205	V_{LDO}	6972	-1005	60	80	267	V_{SS}	12614	-1005	60	80
206	V_{DC2}	7080	-1005	60	80	268	DUMMY	12722	-1005	60	80
207	V_{DC2}	7150	-1005	60	80	269	DUMMY	12830	-1005	60	80
208	V_{DD}	7258	-1005	60	80	270	TESTDUM	12938	-1005	60	80
209	V_{DD}	7328	-1005	60	80	271	TESTDUM	13046	-1005	60	80
210	V_{SS}	7436	-1005	60	80	272	DUMMY	13154	-1005	60	80
211	V_{SS}	7506	-1005	60	80						
212	FBH	7614	-1005	60	80						

5-2-2. Pins on Output Side

BUMP No.	Signal Name	X Coordinate [µm]	Y Coordinate [µm]	X BUMP [µm]	Y BUMP [µm]	BUMP No.	Signal Name	X Coordinate [µm]	Y Coordinate [µm]	X BUMP [µm]	Y BUMP [µm]
273	TESTDM	13268.5	-651	115	24	901	SO473	1565	985.5	22	110
274	TESTDM	13096.5	-651	115	24	902	SO474	1527	985.5	22	110
275	TESTDM	13268.5	-603	115	24	903	SO475	1489	985.5	22	110
276	TESTDM	13096.5	-603	115	24	904	SO476	1451	985.5	22	110
277	V_{COM}	13268.5	-555	115	24	905	SO477	1413	985.5	22	110
278	V_{COM}	13096.5	-555	115	24	906	SO478	1375	985.5	22	110
279	V_{COM}	13268.5	-507	115	24	907	SO479	1337	985.5	22	110
280	V_{COM}	13096.5	-507	115	24	908	SO480	1299	985.5	22	110
281	GO1	13268.5	-459	115	24	909	DUMMY	1254	985.5	22	110
282	GD1	13096.5	-459	115	24	910	DUMMY	1216	985.5	22	110
283	GO3	13268.5	-411	115	24	911	DUMMY	1178	985.5	22	110
284	GO2	13096.5	-411	115	24	912	DUMMY	1140	985.5	22	110
↓	↓	↓	↓	↓	↓	913	DUMMY	1102	985.5	22	110
319	GO39	13268.5	453	115	24	↓	↓	↓	↓	↓	↓
320	GO38	13096.5	453	115	24	971	DUMMY	-1102	985.5	22	110
321	GO41	13268.5	501	115	24	972	DUMMY	-1140	985.5	22	110
322	GO40	13096.5	501	115	24	973	DUMMY	-1178	985.5	22	110
323	DUMMY	13268.5	549	115	24	974	DUMMY	-1216	985.5	22	110
324	GO42	13096.5	549	115	24	975	DUMMY	-1254	985.5	22	110
325	DUMMY	13268.5	597	115	24	976	SO481	-1299	985.5	22	110
326	DUMMY	13096.5	597	115	24	977	SO482	-1337	985.5	22	110
327	TESTDM	13027	991	24	100	978	SO483	-1375	985.5	22	110
328	DUMMY	13027	834	24	100	979	SO484	-1413	985.5	22	110
329	TESTDM	12979	991	24	100	980	SO485	-1451	985.5	22	110
330	DUMMY	12979	834	24	100	981	SO486	-1489	985.5	22	110
331	DUMMY	12931	991	24	100	982	SO487	-1527	985.5	22	110
332	GO43	12931	834	24	100	983	SO488	-1565	985.5	22	110
333	GO44	12883	991	24	100	984	SO489	-1603	985.5	22	110
334	GO45	12883	834	24	100	985	SO490	-1641	985.5	22	110
335	GO46	12835	991	24	100	986	SO491	-1679	985.5	22	110
↓	↓	↓	↓	↓	↓	987	SO492	-1717	985.5	22	110
406	GO117	11155	834	24	100	988	SO493	-1755	985.5	22	110
407	GO118	11107	991	24	100	989	SO494	-1755	814	22	110
408	GO119	11107	834	24	100	990	SO495	-1793	985.5	22	110
409	GO120	11059	991	24	100	991	SO496	-1793	814	22	110
410	GD2	11059	834	24	100	↓	↓	↓	↓	↓	↓
411	DUMMY	11011	991	24	100	1452	SO957	-10571	985.5	22	110
412	DUMMY	11011	834	24	100	1453	SO958	-10571	814	22	110
413	DUMMY	10963	991	24	100	1454	SO959	-10609	985.5	22	110
414	DUMMY	10963	834	24	100	1455	SO960	-10609	814	22	110
415	DUMMY	10915	991	24	100	1456	DUMMY	-10647	985.5	22	110
416	DUMMY	10915	834	24	100	1457	DUMMY	-10647	814	22	110
417	DUMMY	10867	991	24	100	1458	TESTDM	-10685	985.5	22	110
418	DUMMY	10867	834	24	100	1459	TESTDM	-10685	814	22	110
419	DUMMY	10819	991	24	100	1460	TESTDM	-10723	985.5	22	110
420	DUMMY	10819	834	24	100	1461	TESTDM	-10723	814	22	110
421	DUMMY	10771	991	24	100	1462	DUMMY	-10771	991	24	100
422	DUMMY	10771	834	24	100	1463	DUMMY	-10771	834	24	100
423	TESTDM	10723	985.5	22	110	1464	DUMMY	-10819	991	24	100
424	TESTDM	10723	814	22	110	1465	DUMMY	-10819	834	24	100
425	TESTDM	10685	985.5	22	110	1466	DUMMY	-10867	991	24	100
426	TESTDM	10685	814	22	110	1467	DUMMY	-10867	834	24	100
427	DUMMY	10647	985.5	22	110	1468	DUMMY	-10915	991	24	100
428	DUMMY	10647	814	22	110	1469	DUMMY	-10915	834	24	100
429	SO1	10609	985.5	22	110	1470	DUMMY	-10963	991	24	100
430	SO2	10609	814	22	110	1471	DUMMY	-10963	834	24	100
431	SO3	10571	985.5	22	110	1472	DUMMY	-11011	991	24	100
432	SO4	10571	814	22	110	1473	DUMMY	-11011	834	24	100
↓	↓	↓	↓	↓	↓	1474	GO121	-11059	991	24	100
893	SO465	1793	985.5	22	110	1475	GD3	-11059	834	24	100
894	SO466	1793	814	22	110	1476	GO123	-11107	991	24	100
895	SO467	1755	985.5	22	110	1477	GO122	-11107	834	24	100
896	SO468	1755	814	22	110	1478	GO125	-11155	991	24	100
897	SO469	1717	985.5	22	110	↓	↓	↓	↓	↓	↓
898	SO470	1679	985.5	22	110	1549	GO194	-12835	834	24	100
899	SO471	1641	985.5	22	110	1550	GO197	-12883	991	24	100
900	SO472	1603	985.5	22	110	1551	GO196	-12883	834	24	100

BUMP No.	Signal Name	X Coordinate [µm]	Y Coordinate [µm]	X BUMP [µm]	Y BUMP [µm]	BUMP No.	Signal Name	X Coordinate [µm]	Y Coordinate [µm]	X BUMP [µm]	Y BUMP [µm]
1552	DUMMY	-12931	991	24	100	1598	GO237	-13096.5	-363	115	24
1553	GO198	-12931	834	24	100	1599	GO236	-13268.5	-363	115	24
1554	TESTDM	-12979	991	24	100	1600	GO239	-13096.5	-411	115	24
1555	DUMMY	-12979	834	24	100	1601	GO238	-13268.5	-411	115	24
1556	TESTDM	-13027	991	24	100	1602	GD4	-13096.5	-459	115	24
1557	DUMMY	-13027	834	24	100	1603	GO240	-13268.5	-459	115	24
1558	DUMMY	-13096.5	597	115	24	1604	V_{COM}	-13096.5	-507	115	24
1559	DUMMY	-13268.5	597	115	24	1605	V_{COM}	-13268.5	-507	115	24
1560	GO199	-13096.5	549	115	24	1606	V_{COM}	-13096.5	-555	115	24
1561	DUMMY	-13268.5	549	115	24	1607	V_{COM}	-13268.5	-555	115	24
1562	GO201	-13096.5	501	115	24	1608	TESTDM	-13096.5	-603	115	24
1563	GO200	-13268.5	501	115	24	1609	TESTDM	-13268.5	-603	115	24
1564	GO203	-13096.5	453	115	24	1610	TESTDM	-13096.5	-651	115	24
↓	↓	↓	↓	↓	↓	1611	TESTDM	-13268.5	-651	115	24

6. Pin Description

6-1. Power-Supply-Related Pins

6-1-1. External Power-Supply Pins

Pin Name	I/O	Description	No. of Pins
V_{DD}	Power supply	Power-supply pin for the internal power-supply circuit This is the power used for the internal power supply of the chip. It serves as the reference power supply for the primary booster circuit. Connect an external power supply to this pin. Refer to Section 8-18, “Power-Supply Circuit.”	11
V_{SS}	Power supply	Ground pin This is the 0-V pin connected to the system GND. It serves as the substrate potential of the IC.	20
V_{DDI}	Power supply	Interface-only power-supply pin This power supply is used exclusively for interface pins. Connect an external power supply to this pin.	11
V_{CORE}	Power supply	Voltage input pin for the internal logic This supplies power to the internal logic. When V_{CORE} power supply is internal power supply (V_{18}), it is connected to V_{18}. When V_{CORE} power supply is external input, it is inputted 1.65 to 1.95V.	6

6-1-2. Internal Power-Supply Pins

Pin Name	I/O	Description	No. of Pins
V_{REG}	O	Reference-voltage output pin for the internal power-supply circuit Connect this pin to the capacitance. Refer to Section 8-18, “Power-Supply Circuit.”	1
V_{DDHS}	O	Voltage output pin used to generate the source-driver drive voltage Connect this pin to the capacitance. Refer to Section 8-18, “Power-Supply Circuit.”	1
V_{ONREG}	O	Voltage output pin used to adjust VDDHG Connect this pin to the capacitance. Refer to Section 8-18, “Power-Supply Circuit.”	2
V_{OFREG}	O	Voltage output pin used to adjust VEE Connect this pin to the capacitance. Refer to Section 8-18, “Power-Supply Circuit.”	2
V_{OSC}	O	Voltage output pin for the RC oscillator circuit Connect this pin to the capacitance.	1
V_{18}	O	Voltage output pin for the internal logic When an internal power supply is used, it outputs 1.8 V (Typ.).	4
V_{LDO}	O	1st and 2nd booster reference-voltage output pin Connect this pin to the capacitance. Refer to Section 8-18, “Power-Supply Circuit.”	7

6-1-3. Internal Power-Supply Setup Pins

(V_{DD} block I/O)

Pin Name	I/O	Description	No. of Pins
V_{STBY}	I	Input pin used to set up operation of the V_{18} power supply HIGH: V_{CORE} external input (stop V_{18}) LOW: V_{CORE} intrernal generate (operate V_{18})	1

6-1-4. 1st Booster Pins

Pin Name	I/O	Description	No. of Pins
V_{OUT}	O	1st booster-voltage output pin This pin outputs a voltage derived from V_{DC1} by multiplying it by 2 or 3. Connect this pin to the capacitance. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-4, “1st Booster Circuit.”	7
V_{DC1}	I	1st booster reference-voltage input pin Connect this pin to V_{DD} or V_{LDO}. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-4, “1st Booster Circuit.”	4
C11N	I/O	Flying-capacitor negative-electrode connecting pin used to generate V_{OUT} output 1 Connect this pin to the negative-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-4, “1st Booster Circuit.”	4
C11P	I/O	Flying-capacitor positive-electrode connecting pin used to generate V_{OUT} output 1 Connect this pin to the positive-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-4, “1st Booster Circuit.”	4
C12N	I/O	Flying-capacitor negative-electrode connecting pin used to generate V_{OUT} output 2 Connect this pin to the negative-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-4, “1st Booster Circuit.”	4
C12P	I/O	Flying-capacitor positive-electrode connecting pin used to generate V_{OUT} output 2 Connect this pin to the positive-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-4, “1st Booster Circuit.”	4

6-1-5. 2nd Booster Pins

Pin Name	I/O	Description	No. of Pins
V_{DC2}	I	2nd booster reference-voltage input pin Connect this pin to V_{DD} or V_{LDO}. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-5, “2nd Booster Circuit.”	2
C21P	I/O	Flying-capacitor positive-electrode connecting pin used to generate V_{OUTM} output Connect this pin to the positive-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-5, “2nd Booster Circuit.”	3
C21N	I/O	Flying-capacitor negative-electrode connecting pin used to generate V_{OUTM} output Connect this pin to the negative-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-5, “2nd Booster Circuit.”	3
V_{OUTM}	O	Voltage output pin used to generate V_{COML} This pin outputs a voltage derived from $V_{DC2} \times (-1)$. Connect this pin to the capacitance. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-5, “2nd Booster Circuit.”	3

6-1-6. 3rd Booster Pins

Pin Name	I/O	Description	No. of Pins
V_{DC3}	I	3rd booster reference-voltage input pin Connect this pin to V_{ONREG}. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-6, “3rd Booster Circuit.”	2
C31P	I/O	Flying-capacitor positive-electrode connecting pin used to generate V_{DDHG} output 1 Connect this pin to the positive-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-6, “3rd Booster Circuit.”	2
C31N	I/O	Flying-capacitor negative-electrode connecting pin used to generate V_{DDHG} output 1 Connect this pin to the negative-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-6, “3rd Booster Circuit.”	2
C32P	I/O	Flying-capacitor positive-electrode connecting pin used to generate V_{DDHG} output 2 Connect this pin to the positive-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-6, “3rd Booster Circuit.”	2
C32N	I/O	Flying-capacitor negative-electrode connecting pin used to generate V_{DDHG} output 2 Connect this pin to the negative-electrode side. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-6, “3rd Booster Circuit.”	2
V_{DDHG}	O	V_{DDHG} output pin This is a gate-on voltage. It outputs a voltage derived from the V_{ONREG} voltage by double or triple boosting relative to V_{SS}. Connect this pin to the capacitance. Refer to Section 8-18, “Power-Supply Circuit,” and Section 8-18-6, “3rd Booster Circuit.”	3

6-1-7. 4th Booster Pins

Pin Name	I/O	Description	No. of Pins
V_{DC4}	I	4th booster reference-voltage input pin Connect this pin to V_{SS} or V_{OFREG}. Refer to Section 8-18, "Power-Supply Circuit," and Section 8-18-7, "4th Booster Circuit."	2
C4P	I/O	Flying-capacitor positive-electrode connecting pin used to generate V_{EE} output Connect this pin to the positive-electrode side. Refer to Section 8-18, "Power-Supply Circuit," and Section 8-18-7, "4th Booster Circuit."	3
C4N	I/O	Flying-capacitor negative-electrode connecting pin used to generate V_{EE} output Connect this pin to the negative-electrode side. Refer to Section 8-18, "Power-Supply Circuit," and Section 8-18-7, "4th Booster Circuit."	3
V_{EE}	O	V_{EE} output pin This is a gate-off voltage. It outputs a voltage derived from $(V_{DDHG} – V_{DC4}) \times (–1)$ relative to V_{DC4}. Connect this pin to the capacitance. Refer to Section 8-18, "Power-Supply Circuit," and Section 8-18-7, "4th Booster Circuit."	3

6-1-8. V_{COM} Generation Pins

Pin Name	I/O	Description	No. of Pins
V_{COMH}	O	High-potential-side V_{COM}-signal voltage output pin. Connect this pin to the capacitance. Refer to Section 8-18, "Power-Supply Circuit," and Section 8-18-8, "V_{COM} Generator Circuit."	1
FBH	I	This pin is provided for adjustment of the V_{COMH} voltage through internal electronic volume control. Refer to Section 8-18, "Power-Supply Circuit," and Section 8-18-8, "V_{COM} Generator Circuit."	1
V_{COML}	O	Low-potential-side V_{COM}-signal voltage output pin This output voltage is equal to the V_{COMH} voltage minus the V_{COM}-signal amplitude voltage (= V_{COMW}, adjustable through internal electronic volume control) multiplied by 2, as expressed by the following equation: $V_{COML} = V_{COMH} – V_{COMW} \times 2$ Connect this pin to the capacitance. Refer to Section 8-18, "Power-Supply Circuit," and Section 8-18-8, "V_{COM} Generator Circuit."	1

When mounting the IC on a board, ensure that its power supply and potential input signal pins having different names but the same potential will not have a common impedance when they are wired.

6-2. Gamma (γ) Reference Output Pins

Pin Name	I/O	Description	No. of Pins
V_{DDRH}	O	Reference-voltage output pin used to generate the gamma-correction-resistance gray scale voltage Refer to Section 8-19, “Gray-Scale-Voltage Generator Circuit.”	1
V_{GSR0}	O	Intermediate gray-scale-voltage output pin Refer to Section 8-19, “Gray-Scale-Voltage Generator Circuit.”	1
V_{GSR1}	O	Intermediate gray-scale-voltage output pin Refer to Section 8-19, “Gray-Scale-Voltage Generator Circuit.”	1
V_{GSR2}	O	Intermediate gray-scale-voltage output pin Refer to Section 8-19, “Gray-Scale-Voltage Generator Circuit.”	1
V_{GSGB0}	O	Intermediate gray-scale-voltage output pin Refer to Section 8-19, “Gray-Scale-Voltage Generator Circuit.”	1
V_{GSGB1}	O	Intermediate gray-scale-voltage output pin Refer to Section 8-19, “Gray-Scale-Voltage Generator Circuit.”	1
V_{GSGB2}	O	Intermediate gray-scale-voltage output pin Refer to Section 8-19, “Gray-Scale-Voltage Generator Circuit.”	1

6-3. LCD Drive Signals

(V_{DDRH} / V_{DDRL} block I/O)

Pin Name	I/O	Description	No. of Pins
SOn	O	This output is used for the TFT LCD source drive.	960

(V_{DDHG} / V_{EE} block I/O)

Pin Name	I/O	Description	No. of Pins
GOn	O	This output is used for the TFT LCD gate drive.	240
GDn	O	This output is used for the TFT LCD dummy gate drive. It always outputs the V_{EE}-level voltage.	4

(V_{COM} block I/O)

Pin Name	I/O	Description	No. of Pins
V_{COM}	O	This output is used for the common electrode of TFT LCD.	8

6-4. Operation Setup Pins

(V_{DDI} block I/O)

Pin Name	I/O	Description	No. of Pins
P/S	I	MPU interface select pin Refer to Section 8-1, “MPU Interface.”	1
MPUSEL	I	MPU interface select pin Refer to Section 8-1, “MPU Interface.”	1
OSSEL	I	Oscillator-circuit-type select input pin This pin selects whether the internal oscillator circuit that incorporates a complete RC network or an external clock will be used to generate the oscillation of approximately 1.00 MHz required for display in 256 gray scale levels. When LOW, it selects the internal RC oscillator; when HIGH, it selects an external input.	1
INISEL	I	This input pin selects whether EEPROM-based initialize operation is performed, and whether automatic light-contrast operation is performed. When HIGH, it specifies that initialize operation is to be performed, and that automatic light-contrast operation is to be performed. When LOW, it specifies that no initialize operation is to be performed, and that no automatic light-contrast operation is to be performed. Refer to Section 8-12, “Initialize Function.”	1
RESSEL	I	This input pin selects whether an automatic display sequence is performed after a reset. When HIGH, it specifies that an automatic display sequence is to be performed. When LOW, it specifies that no automatic display sequence is to be performed. For the setting of the RESSEL pin to take effect, the INISEL pin must be set HIGH. If the INISEL pin is LOW, the automatic display-off sequence is not performed regardless of how the RESSEL pin is set. Refer to Section 8-13, “Auto Display-Off Function.”	1

<table>
<tr><td>IF16BIT</td><td>I</td><td>This input pin sets the data bus-width when the MPU parallel interface is selected.
When HIGH, the data bus used is 16 bits in width.
When LOW, the data bus used depends on the IFMOD command.
Note: When a serial interface is selected, this input should be set LOW.</td><td>1</td></tr>
<tr><td>IOVSEL</td><td>I</td><td>This input pin sets the data pins used.
When HIGH, the data bus used consists of D7-D0 and SD.
When LOW, the data bus used consists of LD7-D0 and LSD.</td><td>1</td></tr>
<tr><td>LCPOS1
LCPOS0</td><td>I</td><td>These input pins select gate-driver implementation.
One of four gate-drive methods can be selected by setting LCPOS1 and LCPOS0 as shown below.
<table>
<tr><th>LCPOS1</th><th>LCPOS0</th><th>Gate-drive method</th></tr>
<tr><td>LOW</td><td>LOW</td><td>Interlace drive 1</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>Interlace drive 2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>Interlace drive 1</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>Interlace drive 2</td></tr>
</table>
Refer to Chapter 7, “Mounting and Wiring the IC on the Panel.”</td><td>2</td></tr>
</table>

The set level of the operation setup pins determines the internal operation of the driver. To prevent the erratic operation of the driver that may occur if the set level of any pin is changed during operation, connect the stable potential of V_{DDI} or V_{SS} to these pins. When the IC is mounted on the board, it is recommended that these pins be connected to a fixed potential.

6-5. MPU-Block-Related Pins

(V_{DDI} block I/O)

Pin Name	I/O	Description	No. of Pins
$\overline{RES}$	I	Pulling $\overline{RES}$ LOW initializes the MPU. The MPU is reset according to the $\overline{RES}$ signal level.	1
$\overline{CS}$	I	MPU-interface control pin Refer to Section 8-1-1, “MPU Interface and Pin Assignment.”	1
A0	I	MPU-interface control pin Refer to Section 8-1-1, “MPU Interface and Pin Assignment.”	1
$\overline{RD}$	I	MPU-interface control pin Refer to Section 8-1-1, “MPU Interface and Pin Assignment.”	1
$\overline{WR}$	I	MPU-interface control pin Refer to Section 8-1-1, “MPU Interface and Pin Assignment.”	1
D23–D8	I/O	MPU-interface control pins Refer to Section 8-1-1, “MPU Interface and Pin Assignment.”	16
D7–D0	I/O	MPU-interface control pins These pins are used when IOVSEL = HIGH. Connecting these pins when IOVSEL = LOW is prohibited. Refer to Section 8-1-1, “MPU Interface and Pin Assignment.”	8
SD	I/O	MPU-interface control pin This pin is used when IOVSEL = HIGH. Connecting this pin when IOVSEL = LOW is prohibited. Refer to Section 8-1-1, “MPU Interface and Pin Assignment.”	1
TE	O	This pin outputs an LCD timing synchronizing signal. This signal is output after the TEON command and parameter have been input. It outputs a LOW after the TEOFF command is issued.	1
VSYNC	I	MPU/LCDC-interface control pin	1
HSYNC	I	LCDC-interface control pin	1
ENA	I	LCDC-interface control pin	1
DCK	I	LCDC-interface control pin	1
$\overline{VSO}$	O	This pin outputs an LCD timing vertical sync signal.	1
$\overline{HSO}$	O	This pin outputs an LCD timing horizontal sync signal.	1

6-6. Low-Voltage MPU-Block-Related Pins

(V_{CORE} block I/O)

Pin Name	I/O	Description	No. of Pins
LD7-LD 0	I/O	MPU-interface control pins These pins are used when IOVSEL = LOW. Connecting these pins when IOVSEL = HIGH is prohibited. Refer to Section 8-1-1, “MPU Interface and Pin Assignment.”	8
LSD	I/O	MPU-interface control pin This pin is used when IOVSEL = LOW. Connecting this pin when IOVSEL = HIGH is prohibited. Refer to Section 8-1-1, “MPU Interface and Pin Assignment.”	1

6-7. Oscillator-Circuit Signals

(V_{DDI} block I/O)

Pin Name	I/O	Description	No. of Pins
OS1	I/O	External clock input/output pin When using an external clock, feed it to this pin. When not using this pin, connect it to the V_{SS} potential. In test mode, the internally generated clock can be output from this pin.	1

6-8. EEPROM Control Pins

(V_{DD} block I/O)

Pin Name	I/O	Description	No. of Pins
POFF	O	Power-supply control output pin It outputs a LOW when the LCD is powered off and is in the SLPIN state; it outputs a HIGH in SLPOUT state. Refer to Section 8-14, “EEPROM Control Function.”	1
BCK	O	EEPROM control clock output pin This pin is used to control the EEPROM clock. Data transfer from the S1D19122 to EEPROM is performed synchronously with this clock. Output of this signal is controlled by a command. Refer to Section 8-14, “EEPROM Control Function.”	1
BDATA	I/O	EEPROM control-data input/output pin This pin is used to control the EEPROM by supplying control data to it. Output/input of this signal is controlled by a command. This signal is latched onto the rising edge of BCK. Refer to Section 8-14, “EEPROM Control Function.”	1
BRST	O	EEPROM chip select output pin It outputs a HIGH when controlling the EEPROM, or a LOW when not controlling the EEPROM. Refer to Section 8-14, “EEPROM Control Function.”	1
BDO	O	EEPROM data output pin Refer to Section 8-14, “EEPROM Control Function.”	1

6-9. TEST Control Pins

(V_{DD} block I/O)

Pin Name	I/O	Description	No. of Pins
TRI	O	Test-signal output pin This pin is used to adjust the internal constant current. Leave it open.	1
PTEST1	I	Test-signal input pin This test pin is used for the internal power supply. Apply V_{SS} potential to it.	1
PTEST2	I	Test-signal input pin This test pin is used for the internal power supply. Apply V_{SS} potential to it.	1

6-10. TEST Control Pins

(V_{DDI} block I/O)

Pin Name	I/O	Description	No. of Pins
TMONI	I	Test-signal input pin. Apply V_{SS} potential to this pin.	1
TEST8 to TEST0	O	Test-signal output pins. Leave these pins open.	9
TSBIEN	I	Test-signal input pin. Apply V_{SS} potential to this pin.	1
TSBICK	I	Test-signal input pin. Apply V_{SS} potential to this pin.	1

6-11. Other Pins

(V_{DDI} block I/O)

Pin Name	I/O	Description	No. of Pins
TESTDUM	I/O	Test pin. Leave it open.	24

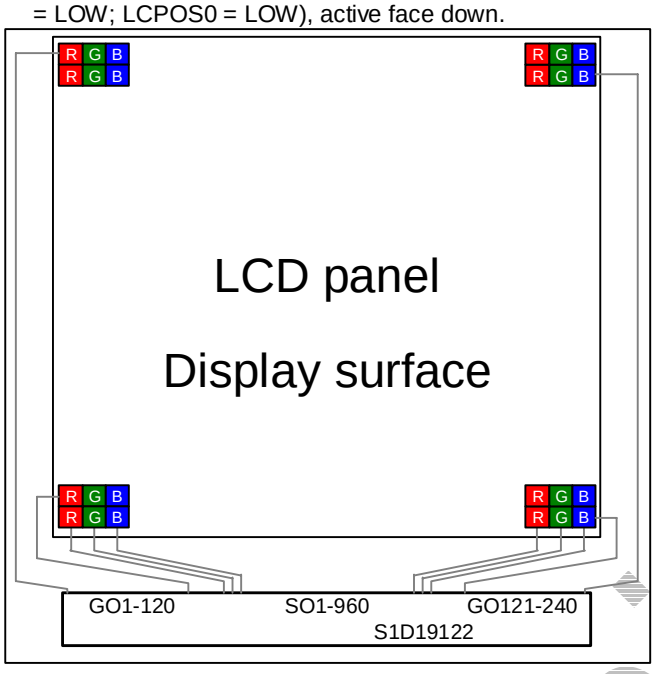
7. Mounting and Wiring the IC on the Panel

7-1. Gate-Driver Wiring

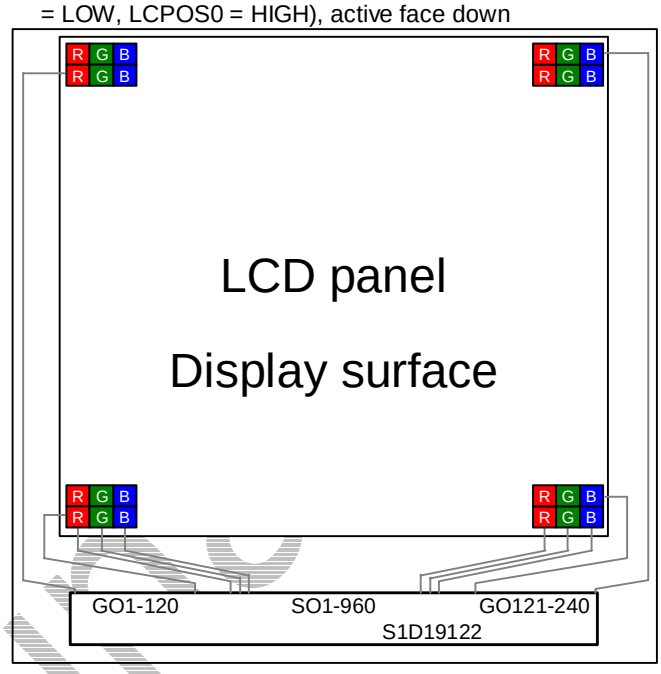
7-1-1. Gate-Driver Interlace Wiring

The S1D19122 supports two types of interlace wiring.

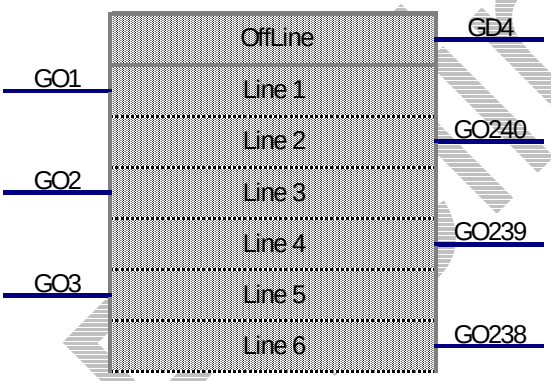
◇ When mounted on the upper-right of the panel (LCPOS1 = LOW; LCPOS0 = LOW), active face down.



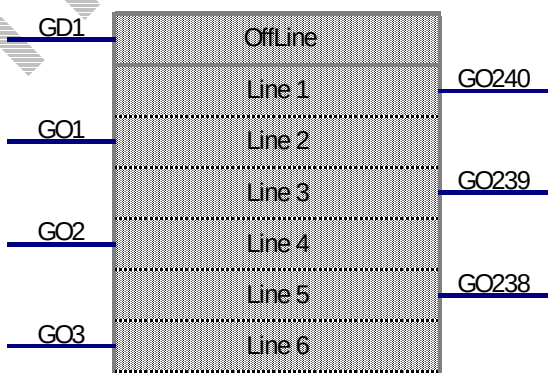
◇ When mounted on the upper-left of the panel (LCPOS1 = LOW, LCPOS0 = HIGH), active face down



◇ Top offline = 1; LCPOS1 = LOW; LCPOS0 = LOW



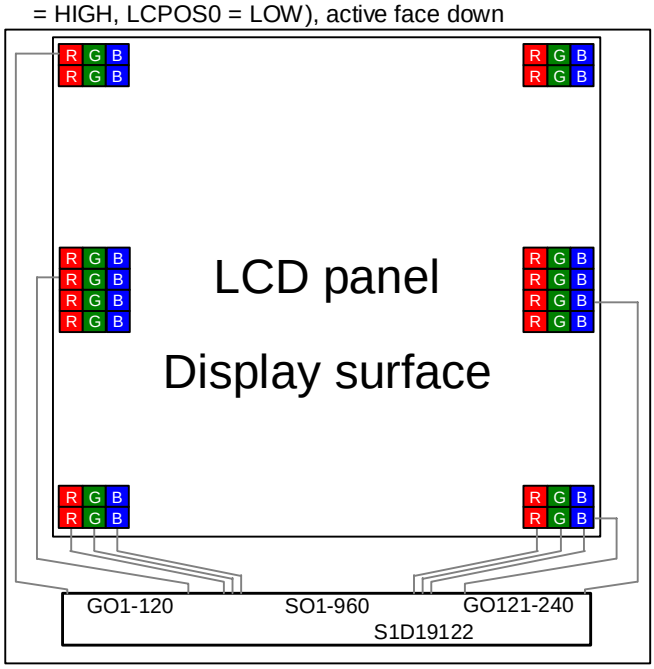
◇ Top offline = 1; LCPOS1 = LOW; LCPOS0 = HIGH



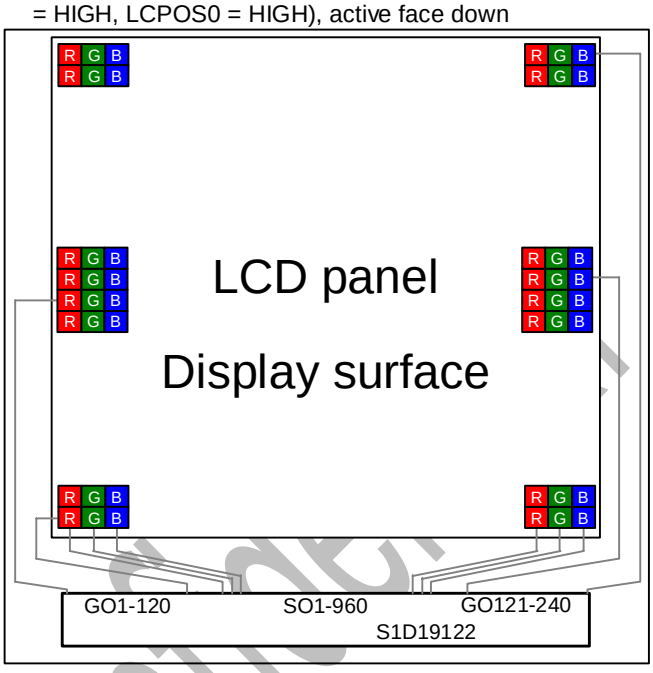
7-1-2. Gate-Driver Interlace Wiring

The S1D19122 supports two types of continuous wiring.

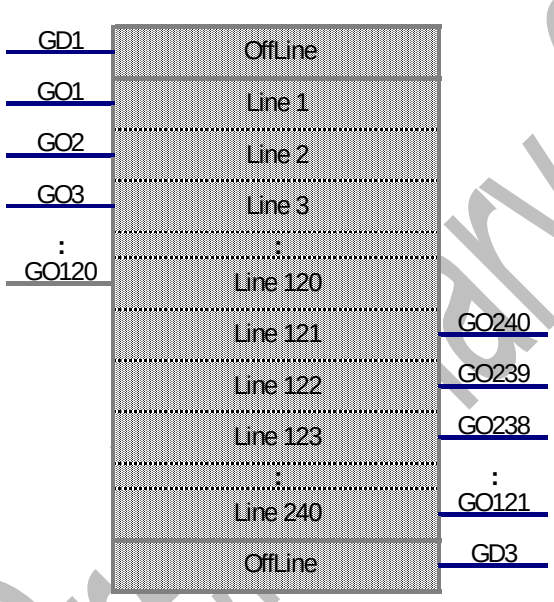
◇ When mounted on the upper-right of the panel (LCPOS1 = HIGH, LCPOS0 = LOW), active face down



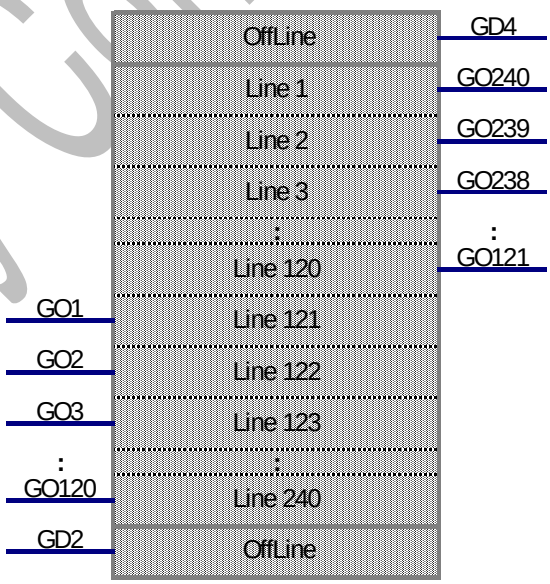
◇ When mounted on the upper-left of the panel (LCPOS1 = HIGH, LCPOS0 = HIGH), active face down



◇ Top offline = 1; LCPOS1 = HIGH; LCPOS0 = LOW



◇ Top offline = 1; LCPOS1 = HIGH; LCPOS0 = HIGH



8. Functional Description

8-1. MPU Interface

When the S1D19122 is used with a parallel interface, it transfers command/parameters and display data to and from the MPU using a bidirectional data bus up to 24 bits in width (D23-D0).

The interface with which it communicates with the MPU is selected using a combination of the P/S and MPUSEL pins, which are set HIGH or LOW. Make sure that when the IC is mounted, fixed levels are applied to the P/S and MPUSEL pins. Changing the MPU interface during operation is prohibited.

Interface	Pin input level	
	P/S	MPUSEL
80-series MPU parallel interface	HIGH	LOW
68-series MPU parallel interface	HIGH	HIGH
4-wire, 8-bit data serial interface	LOW	HIGH
3-wire, 9-bit data serial interface	LOW	LOW

Note that the MPU interface referred to in this development specification means the 80-series MPU parallel interface unless otherwise noted.

8-1-1. MPU Interface and Pin Assignments

The pin assignments of the S1D19122 are changed according to the MPU interface used. The pin assignments are listed in the table below. Process the unused pins by applying the V_{DDI} or V_{SS} potential or leaving them open.

◇ Common

Pin name	Pin definition	Description	Remark
VSYNC	VSYNC	This is the vertical sync-signal input pin used for externally synchronized display by VSYNCIN. During externally synchronized display, display for one frame begins with the falling edge. When not using externally synchronized display, input V_{DDI} potential to this pin.	-

◇ 80-series MPU parallel interface

When $\overline{CS}$ is inactive ($\overline{CS}$ = HIGH), D23-D0 are placed in the high-impedance state internally.

Pin name	Pin definition	Description	Remark
$\overline{CS}$	$\overline{CS}$	Chip select signal	-
A0	A0	Least significant bit of the address bus When LOW, this signal indicates that the data bus is a command. When HIGH, it indicates that the data bus is a parameter or display data.	-
$\overline{RD}$	$\overline{RD}$	Read signal: While it is held LOW, the data bus is in an output state.	-
$\overline{WR}$	$\overline{WR}$	Write signal: Data is latched on rising edge of this signal.	-
D23–D18	D23–D18	Data bus (These pins are used when the bus is 24 bits in width.)	The unused pins may be left open.
D17–D16	D17–D16	Data bus (These pins are used when the bus is 18 bits or more in width.)	The unused pins may be left open.
D15–D12	D15–D12	Data bus (These pins are used when the bus is 16 bits or more in width.)	The unused pins may be left open.
D11–D9	D11–D9	Data bus (These pins are used when the bus is 12 bits or more in width.)	The unused pins may be left open.
D8	D8	Data bus (These pins are used when the bus is 9 bits or more in width.)	The unused pins may be left open.
D7–D0	D7–D0	Data bus	-
SD	-	Unused	This pin may be left open.

◇ 68-series MPU parallel interface

When $\overline{CS}$ is inactive ($\overline{CS}$ = HIGH), D23-D0 are placed in the high-impedance state internally.

Pin name	Pin definition	Description	Remark
$\overline{CS}$	$\overline{CS}$	Chip select signal	-
A0	A0	Least significant bit of the address bus When LOW, this signal appears as a command to the data bus. When HIGH, it appears as a parameter or display data to the data bus.	-
$\overline{RD}$	E	During write, data is latched on the rising edge of this signal. During read, the data bus is in an output state while this signal is held HIGH.	-
$\overline{WR}$	R/$\overline{W}$	LOW: write; HIGH: read	-
D23–D18	D23–D18	Data bus (These pins are used when the bus is 23 bits in width.)	The unused pins may be left open.
D17–D16	D17–D16	Data bus (These pins are used when the bus is 18 bits or more in width.)	The unused pins may be left open.
D15–D12	D15–D12	Data bus (These pins are used when the bus is 16 bits or more in width.)	The unused pins may be left open.
D11–D9	D11–D9	Data bus (These pins are used when the bus is 12 bits or more in width.)	The unused pins may be left open.
D8	D8	Data bus (These pins are used when the bus is 9 bits or more in width.)	The unused pins may be left open.
D7–D0	D7–D0	Data bus	-
SD	-	Unused	This pin may be left open.

The signals D7-D0 and SD are the pin definitions that apply when LOVSEL = HIGH. When LOVSEL = LOW, these signals should be read as LD7-LD0.

The pin that becomes unused by setting IOVSEL becomes a prohibition of connecting.

◇ 4-wire, 8-bit data serial interface

When $\overline{CS}$ is inactive ($\overline{CS}$ = HIGH), SD is placed in the high-impedance state internally.

Pin name	Pin definition	Description	Remark
$\overline{CS}$	$\overline{CS}$	Chip select signal	-
A0	A0	When LOW, this signal appears as a command to the data bus. When HIGH, it appears as a parameter or display data to the data bus.	-
$\overline{RD}$	-	Unused	The pin may be left open.
$\overline{WR}$	SCL	Clock signal During write, data is latched on the rising edge of this signal. During read, the data bus is in an output state while this signal is held LOW.	-
D23–D0	D23–D0	Data bus used for the LCDC interface	See 8-2-1.
SD	SD	Data signal	-

◇ 3-wire, 9-bit data serial interface

When $\overline{CS}$ is inactive ($\overline{CS}$ = HIGH), SD is placed in the high-impedance state internally.

Pin name	Pin definition	Description	Remark
$\overline{CS}$	$\overline{CS}$	Chip select signal	-
A0	SCL	Clock signal During write, data is latched on the rising edge of this signal. During read, the data bus is in an output state while this signal is held LOW.	-
$\overline{RD}$	-	Unused	The pin may be left open.
$\overline{WR}$	-	Unused	The pin may be left open.
D23–D0	D23–D0	Data bus used for the LCDC interface	See 8-2-1.
SD	SD	Data signal	-

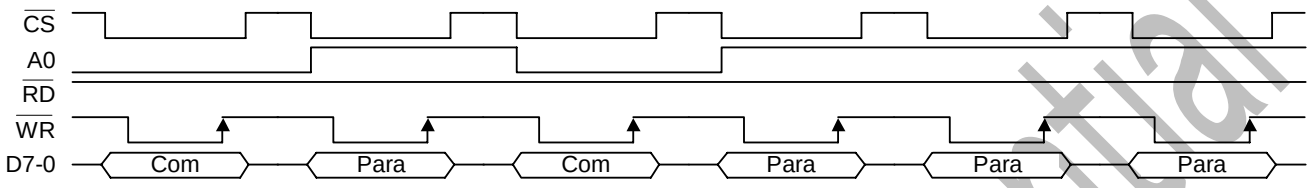
8-1-2. 80-Series MPU Parallel Interface

This is the parallel interface through which the S1D19122 communicates with the MPU using $\overline{CS}$, A0, $\overline{RD}$, $\overline{WR}$, and D23-D0. This interface is enabled when P/S = HIGH and MPUSEL = LOW. Depending on the bus width specified by IFMOD, the data-bus bit width required for communication changes to 8 bits (D7-D0), 9 bits (D8-D0), 12 bits (D11-D0), 16 bits (D15-D0), 18 bits (D17-D0), or 24 bits (D23-D0). When the MPU is communicated with in 9/12/16/18/24 bits, all data bits other than D7-D0 have no effect during command/parameter input (i.e., when display data is not being transferred). These invalid bits should be driven either HIGH or LOW when input.

Internally in the IC, the overlapping portion of $\overline{CS}$ = LOW and $\overline{WR}$ = LOW comprises a write signal, and of $\overline{CS}$ = LOW and $\overline{RD}$ = LOW comprises a read signal. Executing read and write operations simultaneously is prohibited.

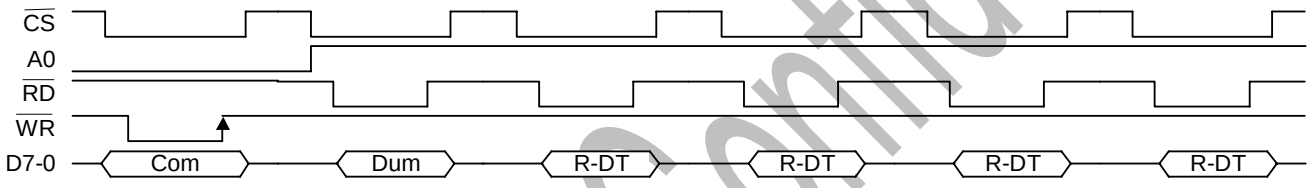
Example interface operations are shown below.

◇ During write



Com: Command
Para: Parameter

◇ During read



Com: Read Command
Dum: Dummy Read
R-DT: Read Data

◇ Precautions

As the overlapping portion of $\overline{CS}$ = LOW and $\overline{RD}$ = LOW comprises a read signal, even in cases in which a read command has no effect, the overlapping LOW levels of these signals may be recognized as a read signal. In such a case, a read state will be assumed and dummy data will be output. Conversely, in a read state in which a read operation is performed by a read command, A0 must always be held HIGH while the read signal is active. If the read signal recognizes A0 = LOW, the read data thereafter is handled as dummy data, requiring that the operation be reexecuted beginning with command issuance. Changes to the A0 level while the read signal is inactive are ignored. The time during which the A0 level is allowed to change depends on the AC characteristics of the IC (tAW8, tAH8).

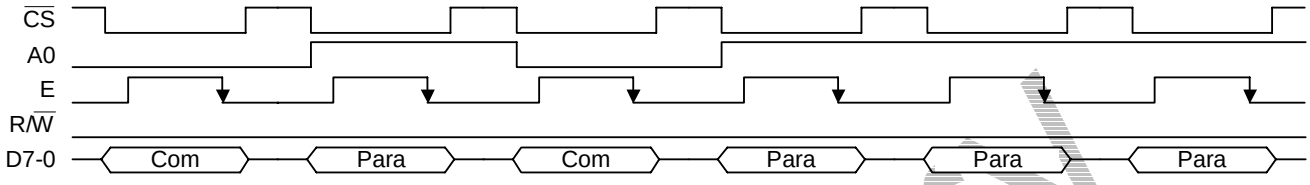
8-1-3. 68-Series MPU Parallel Interface

This is the parallel interface through which the S1D19122 communicates with the MPU using $\overline{CS}$, A0, E ($\overline{RD}$), R/$\overline{W}$ ($\overline{WR}$), and D23-D0. This interface is enabled when P/S = HIGH and MPUSEL = HIGH. Depending on the bus width specified by IFMOD, the data-bus bit width required for communication changes to 8 bits (D7-D0), 9 bits (D8-D0), 12 bits (D11-D0), 16 bits (D15-D0), 18 bits (D17-D0), or 24 bits (D23-D0). When the MPU is communicated with in 9/12/16/18/24 bits, all data bits other than D7-D0 have no effect during command/parameter input (i.e., when display data is not being transferred). These invalid bits should be driven either HIGH or LOW when input.

Internally in the IC, the overlapping portion of $\overline{CS}$ = LOW, E = HIGH, and R/$\overline{W}$ = LOW comprises a write signal, and of $\overline{CS}$ = LOW, E = HIGH, and R/$\overline{W}$ = HIGH comprises a read signal.

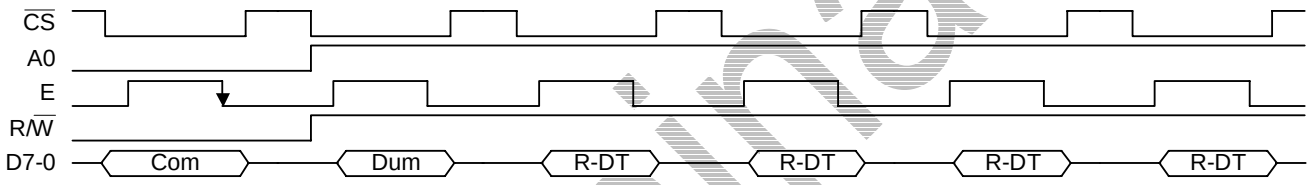
Example interface operations are shown below.

◇ During write



Com: Command
Para: Parameter

◇ During read



Com: Read Command
Dum: Dummy Read
R-DT: Read Data

◇ Precautions

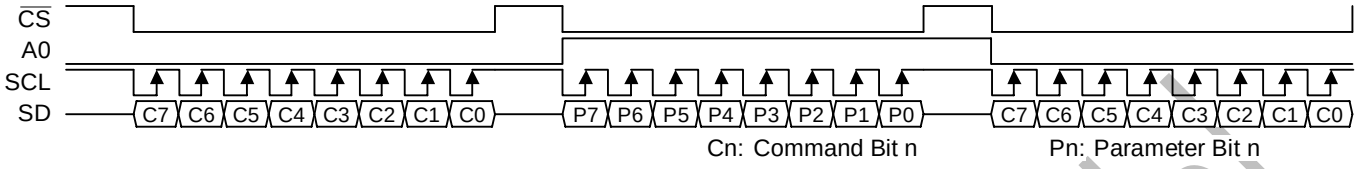
As the overlapping portion of $\overline{CS}$ = LOW, E = HIGH, and R/$\overline{W}$ = HIGH comprises a read signal, even in cases in which a read command has no effect, the overlapping HIGH and LOW levels of these signals may be recognized as a read signal. In such a case, a read state will be assumed and dummy data will be output. Conversely, in a read state in which a read operation is performed by a read command, A0 must always be held HIGH while the read signal is active. If the read signal recognizes A0 = LOW, the read data thereafter is handled as dummy data, requiring the operation to be reexecuted beginning with command issuance. Changes in the A0 level while the read signal is inactive are ignored. The time during which the A0 level is allowed to change depends on the AC characteristics of the IC (tAW6, tAH6).

8-1-4. 4-Wire, 8-Bit Data Serial Interface

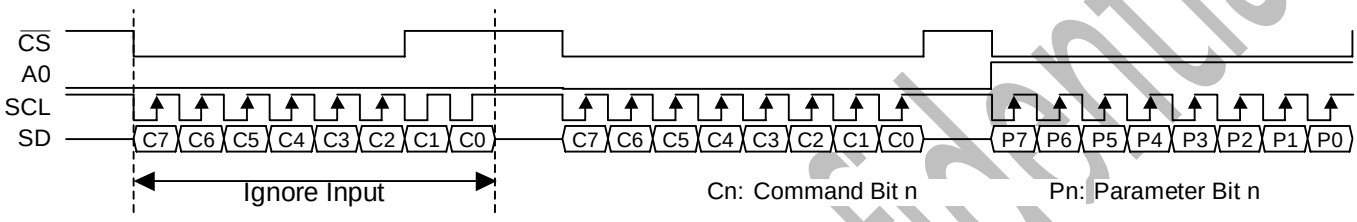
This is the serial interface through which the S1D19122 communicates with the MPU using the four wires of $\overline{CS}$, A0, SCL ($\overline{WR}$), and SD. This interface is enabled when P/S = LOW and MPUSEL = HIGH. The data bus internally is always 8 bits in width regardless of what bus width is specified by IFMOD.

Example interface operations are shown below. (The intermediate level of SD in the diagrams below denotes the high-impedance state.)

◇ During write

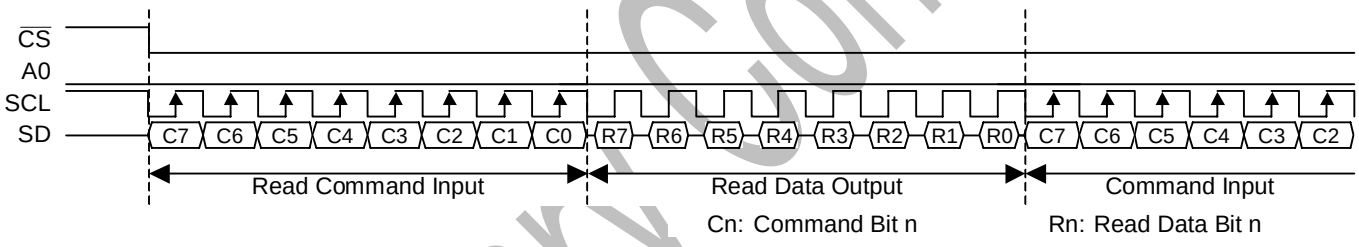


$\overline{CS}$ must be held LOW while 8-bit serial data (single packet) is being transferred. If $\overline{CS}$ is changed to HIGH during the transfer of a packet, the packet being transferred is cancelled. When $\overline{CS}$ is pulled LOW again, the driver is ready to accept a retransfer of the packet.

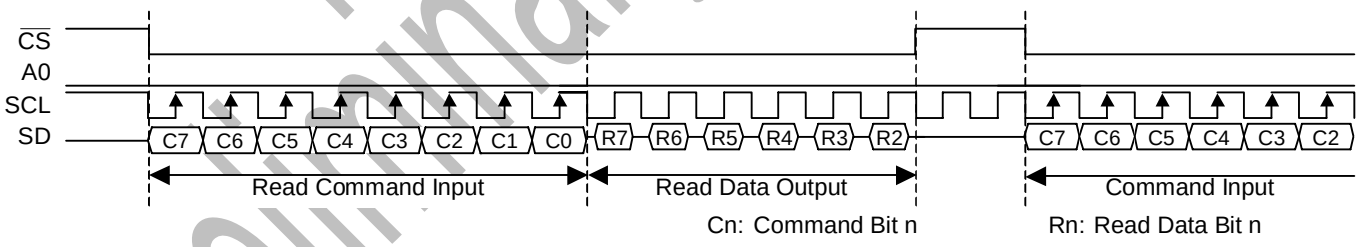


◇ During 1-byte read

To read 1-byte data using the commands RDDPM, RDDMADCTL, RDDCOLMOD, RDDIM, RDDSM, RDDSDR, RDID1, RDID2, RDID3, and STREAD2, an interface operation like the one shown below is performed. When the driver has finished transferring the last bit of the read data, it internally exits a read state and is readied to accept commands.



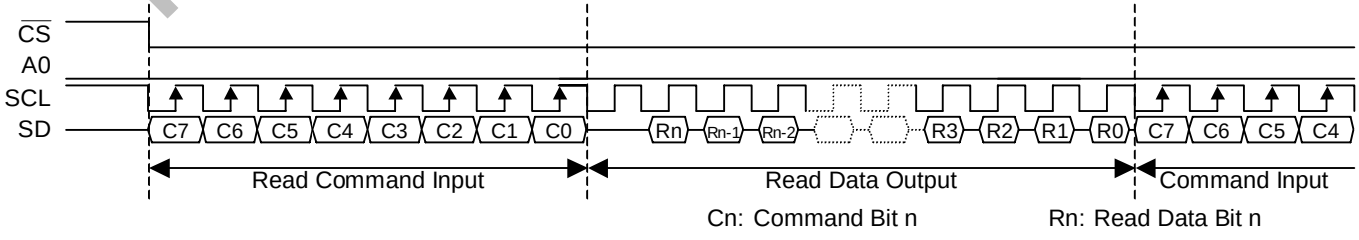
If $\overline{CS}$ is changed to HIGH while the read data is being transferred, the read state is cancelled. When $\overline{CS}$ is pulled LOW again, the driver is ready to accept commands.



◇ During multi-byte read

To read multi-byte data using the commands RDDIDIF, RDDST, RAMRD, RDDATM and TESTREG, an interface operation like the one shown below is performed. When the driver has finished transferring the last bit of the read data, it internally exits a read state and is readied to accept commands. However, the read state entered into by RAMRD or TESTREG must be cancelled by $\overline{CS}$.

The first cycle (clock) immediately after a read state is entered from a command input state constitutes a dummy cycle.



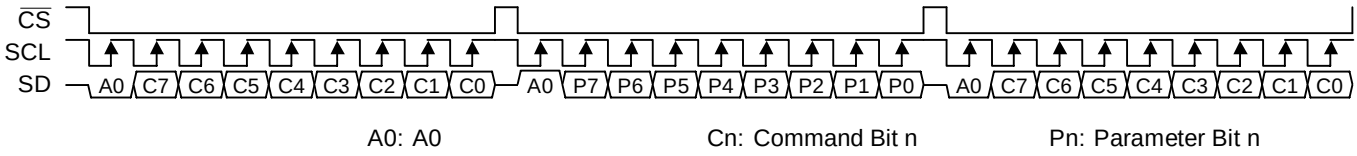
If $\overline{CS}$ is changed to HIGH while the read data is being transferred, the operation is processed in the same way as in 1-byte read.

8-1-5. 3-Wire, 9-Bit Data Serial Interface

This is the serial interface through which the S1D19122 communicates with the MPU using the three wires $\overline{CS}$, SCL (A0), and SD. This interface is enabled when P/S = LOW and MPUSEL = LOW. The data bus internally is always 8 bits in width regardless of what bus width is specified by IFMOD.

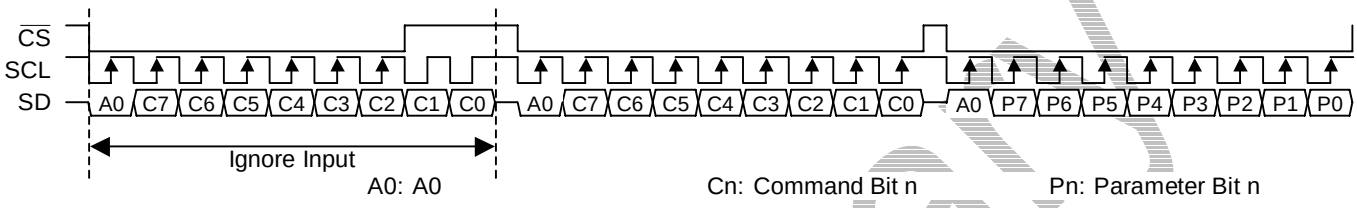
Example interface operations are shown below. (The intermediate level of SD in the diagrams below denotes the high-impedance state.)

◇ During write



A0: A0 Cn: Command Bit n Pn: Parameter Bit n

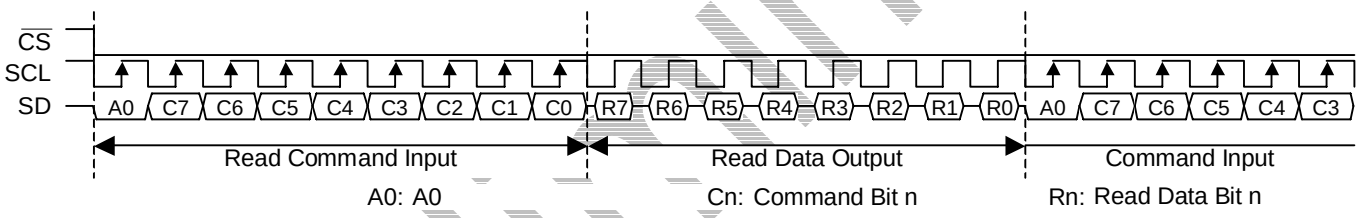
$\overline{CS}$ must be held LOW while 9-bit serial data (single packet) is being transferred. If $\overline{CS}$ is changed to HIGH during the transfer of a packet, the packet being transferred is cancelled. When $\overline{CS}$ is pulled LOW again, the driver is ready to accept a retransfer of the packet.



A0: A0 Cn: Command Bit n Pn: Parameter Bit n

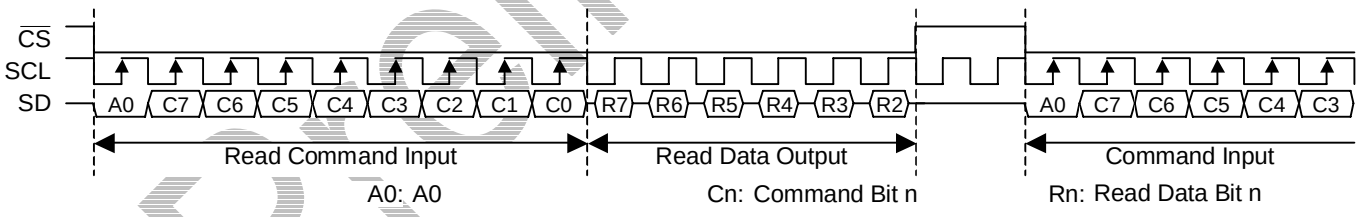
◇ During 1-byte read

To read 1-byte data using the commands RDDPM, RDDMADCTL, RDDCOLMOD, RDDIM, RDDSM, RDDSDR, RDID1, RDID2, RDID3, and STREAD2, an interface operation like the one shown below is performed. When the driver has finished transferring the last bit of the read data, it internally exits a read state and is readied to accept commands.



A0: A0 Cn: Command Bit n Rn: Read Data Bit n

If $\overline{CS}$ is changed to HIGH while the read data is being transferred, the read state is cancelled. When $\overline{CS}$ is pulled LOW again, the driver is ready to accept commands.

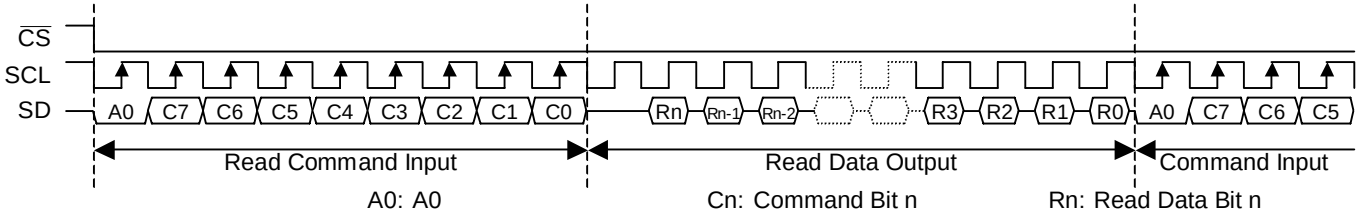


A0: A0 Cn: Command Bit n Rn: Read Data Bit n

◇ During multi-byte read

To read multi-byte data using the commands RDDIDIF, RDDST, RAMRD, RDDATM and TESTREG, an interface operation like the one shown below is performed. When the driver has finished transferring the last bit of read data, it internally exits a read state and is readied to accept commands. However, the read state entered into by RAMRD and TESTREG must be cancelled by $\overline{CS}$.

The first cycle (clock) immediately after a read state is entered from a command input state constitutes a dummy cycle.



A0: A0 Cn: Command Bit n Rn: Read Data Bit n

If $\overline{CS}$ is changed to HIGH while the read data is being transferred, the operation is processed in the same way as in 1-byte read.

8-1-6. Bidirectional Data Bus

As the MPU interface of the S1D19122 is designed to communicate with the MPU in a direct connection, if access to the S1D19122 is not chip-selected ($\overline{CS}$ = HIGH) or reset in the hardware ($\overline{RES}$ = LOW), the data bus (data line) is placed in the high-impedance state to prevent the other ICs from being adversely affected. The high-impedance state is a condition in which the output pins of the bus are of a high-impedance to the ground and V_{DD}, and are in effect isolated from the other connected devices.

When access to the S1D19122 is not chip-selected, inputs through the MPU interface (A0, $\overline{RD}$, and $\overline{WR}$ signals) have no effect.

An example of the 80-series MPU parallel interface is shown below.

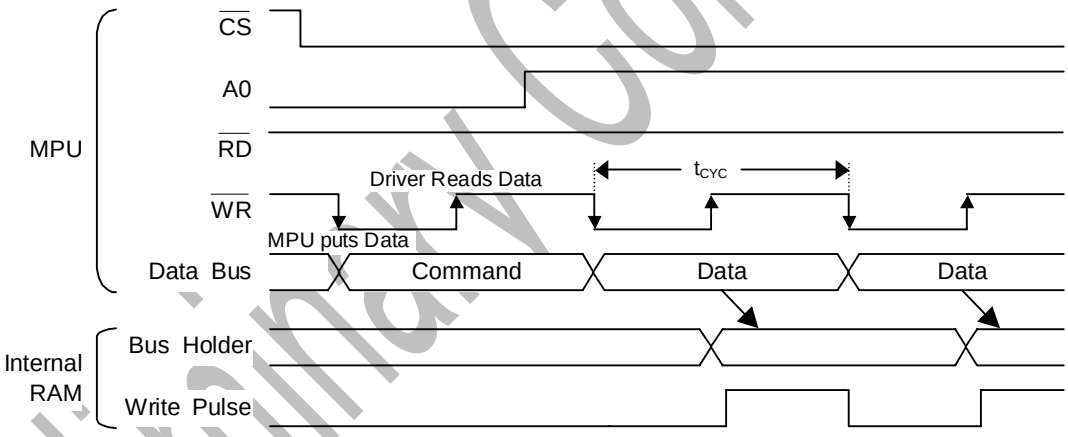
A0	$\overline{RD}$	$\overline{WR}$	Detail
LOW	↑	HIGH	Command write: Commands are input to D7-D0.
HIGH	↑	HIGH	Parameter and display data write: Parameters and display data are input to D7-D0 and D23-D0, respectively.
HIGH	HIGH	↓ LOW	Parameter and display data read: Parameters and display data are output to D7-D0 and D23-D0, respectively.
LOW	HIGH	↓ LOW	Dummy data output (It is recommended that not be used.)

During a parallel interface, the bus width used changes depending on the display-data format. When a display-data format that uses D23-D8 is selected, although D23-D8 are ignored when command/parameters are input, it is necessary that D23-D8 be driven either HIGH or LOW when input on the MPU side.

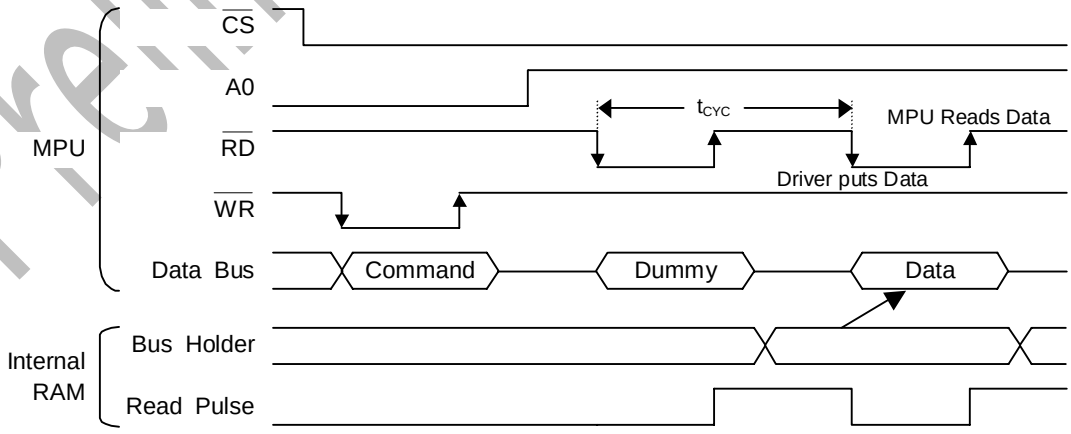
8-1-7. Access to Video Memory and Internal Registers

To ensure that the operations of the built-in video memory or the internal registers of the S1D19122 will be matched in timing with the MPU, the S1D19122 performs what can be referred to as “pipelined processing” via the bus holder attached to its internal data bus. The limitations on access to the S1D19122 as viewed from the MPU side are predominantly imposed by cycle time rather than video-memory access time (t_{ACC}). If the cycle time cannot be satisfied, the MPU issues the NOP2 command. This appears as an equivalent to inserting a wait state.

◇ Write



◇ Read



8-1-8. Command Recognition and Parameter/Display Data Latch

The S1D19122 checks the data mode indicated by A0 to determine whether the data sent from the MPU is a command, parameter, or display data.

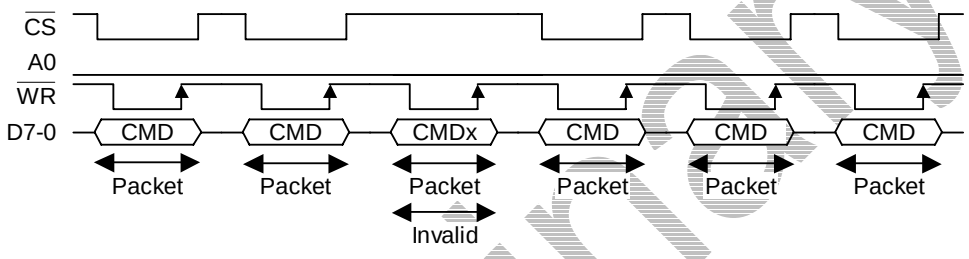
Data has a finite packet length specific to each data mode, and data transfers are performed in packet units. It is recommended that the $\overline{CS}$ signal be pulled LOW during a packet transfer.

The five command formats are as follows.

Type	Command format	Command recognition/parameter latch	Example command
Type1	Command only	A command is recognized at the time it is input.	SLPOUT, IDMON
Type2	Parameter included	A parameter is latched at the time it is input.	RGBSET, GCPSET0
Type3	Parameter included	A parameter value is latched when a range of parameters have been input.	PTLAR, RAMWR
Type4	Parameter included	A command is recognized and a parameter value is latched when a parameter is input.	VSCRSADD, EPCTIN
Type5	Parameter included	Combination of types 2 and 3	DISCTL

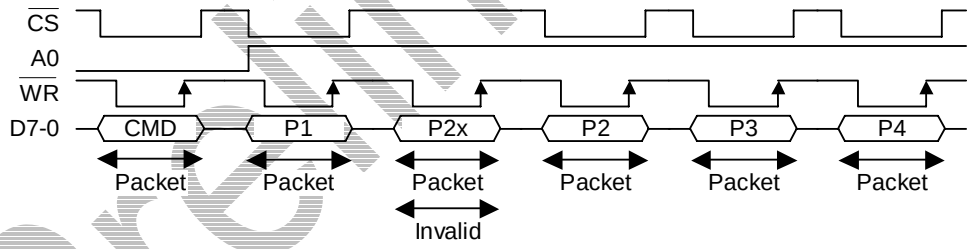
◇ Type1

The command CMDx where $\overline{CS}$ = HIGH has no effect. The packet length includes only a command.



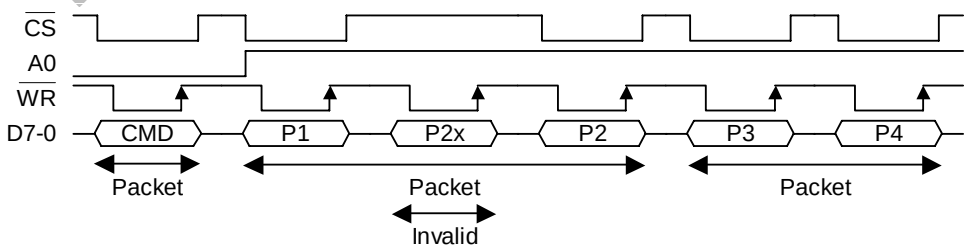
◇ Type 2

The parameter P2x where $\overline{CS}$ = HIGH has no effect. However, if this is followed by the successive input of the subsequent parameters, the command CMD is not cancelled and the driver continues to latch parameter values beginning with the ignored parameter P2. The packet length includes a command and a single parameter.



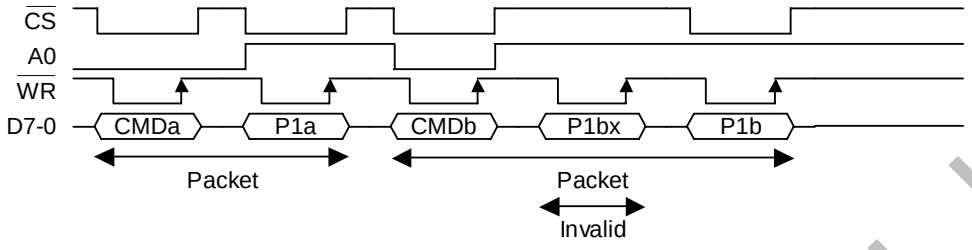
◇ Type3

The parameter P2x input when $\overline{CS}$ = HIGH has no effect. If parameter input ends with P2x, the packet length is insufficient and the parameter P1 therefore has no effect. However, if this is followed by the successive input of parameter P2, the packet length is satisfied and the driver latches parameters P1 and P2. The packet length varies depending on the parameters latched.



◇ Type4

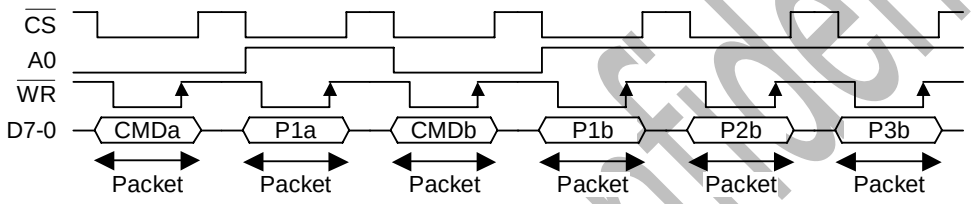
The parameter P1bx input when $\overline{CS}$ = HIGH has no effect. If parameter input ends with P1bx, the packet length is insufficient and the command CMDb therefore has no effect. However, if this is followed by the successive input of parameter P1b, the packet length requirement is satisfied and the driver recognizes the command CMDb and latches the parameter P1b. The packet length includes a command and the parameters input.



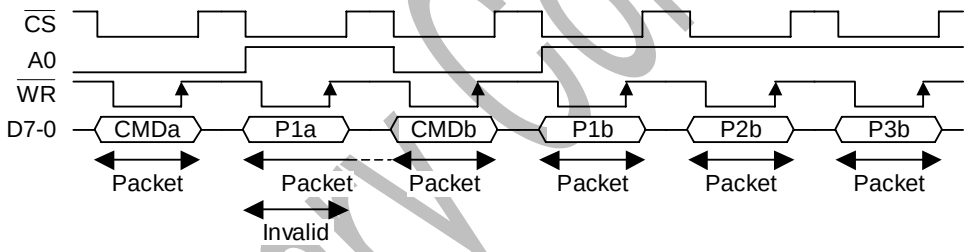
◇ When a command is issued during parameter input

If the command CMDb is issued while a parameter is being input (assuming that CMDa is accompanied by parameters up to P2a), the command CMDa that has hitherto been input is cancelled and the newly issued command CMDb is effective.

In this case, if the command CMDa is Type 2, the parameter P1a is effective. As the parameter P2a is not input, the parameter value is not rewritten.

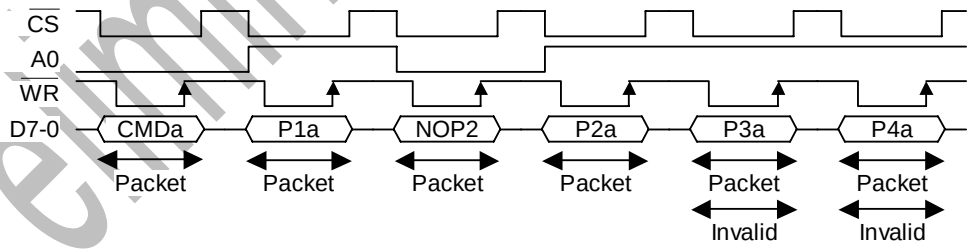


If the command CMDa is Type 3, as the command was cancelled before the packet length was reached, the parameter P1a is not effective. Therefore, neither parameter P1a nor parameter P2a are rewritten.



If the parameter P2a needs to be input, parameter input must be reexecuted beginning with command input (CMDa). It is recommended that during command or parameter input, no other commands be input.

If the command CMDb is the NOP2 command, the command CMDa is not cancelled and the successively input parameter P2a is latched as a valid parameter.



If more than the designated number of parameters are input, parameters P3a and P4a are ignored.

Refer to Section 8-12-3, “SENOP.”

Refer to Section 9-1, “Command Table.”

8-2. LCDC Interface

The LCDC interface is used exclusively for the transfer of display data. The LCDC interface uses a dedicated data bus of up to 24 bits in width (D23–D0) to transfer the display data.

8-2-1. LCDC Interface and Pin Assignments

During the LCDC interface, the pin assignments change in accordance with the bus width. The pin assignments are listed in the table below. Process unused pins by applying the V_{DDI} or GNDL potential or leaving them open.

◇ LCDC interface

The data-bus width is set by IFMOD.

When the LCDC interface is enabled, all pins of the interface except for unused pins are in the input state.

Pin name	Pin definition	Description	Remark
VSYNC	VSYNC	Vertical sync signal	-
HSYNC	HSYNC	Horizontal sync signal	-
ENA	ENA	Display-data valid signal	-
DCK	DCK	Write signal (Data is latched on the rising edge of this signal.)	-
D23–D18	D23–D18	Data bus (These pins are used when the bus is 24 bits in width.)	The unused pins may be left open.
D17–D16	D17–D16	Data bus (These pins are used when the bus is 18 bits or more in width.)	The unused pins may be left open.
D15–D12	D15–D12	Data bus (These pins are used when the bus is 16 bits or more in width.)	The unused pins may be left open.
D11–D9	D11–D9	Data bus (These pins are used when the bus is 12 bits or more in width.)	The unused pins may be left open.
D8	D8	Data bus (These pins are used when the bus is 9 bits or more in width.)	The unused pins may be left open.
D7–D0	D7–D0	Data bus	-

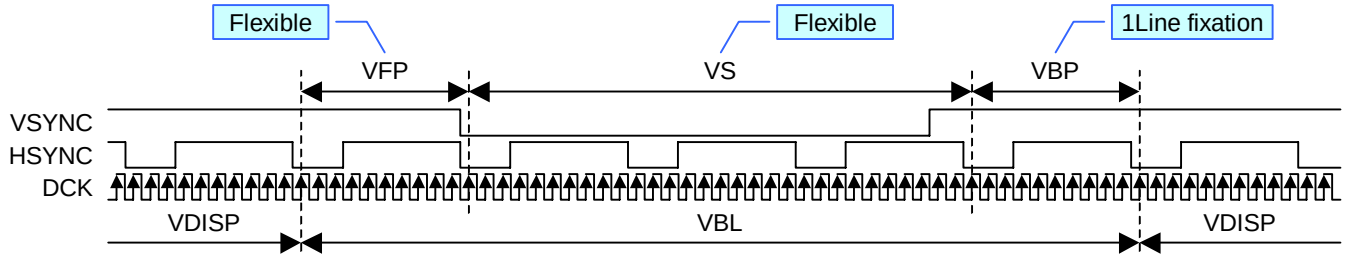
8-2-2. LCDC Interface

This is the interface through which the driver communicates with the LCDC using VSYNC, HSYNC, ENA, DCK, and D23-D0. When the driver is using the MPU parallel interface, this interface is made usable by enabling the LCDC interface using the LCDCIF command. When the driver is using the MPU serial interface, this interface is always effective regardless of how it is set by the LCDCIF command. Depending on the bus width specified by IFMOD command, the data-bus bit width required for communication changes to 8 bits (D7-D0), 9 bits (D8-D0), 12 bits (D11-D0), 16 bits (D15-D0), 18 bits (D17-D0), or 24 bits (D23-D0).

The following defines the terms associated with the LCDC interface that are stipulated in this development specification.

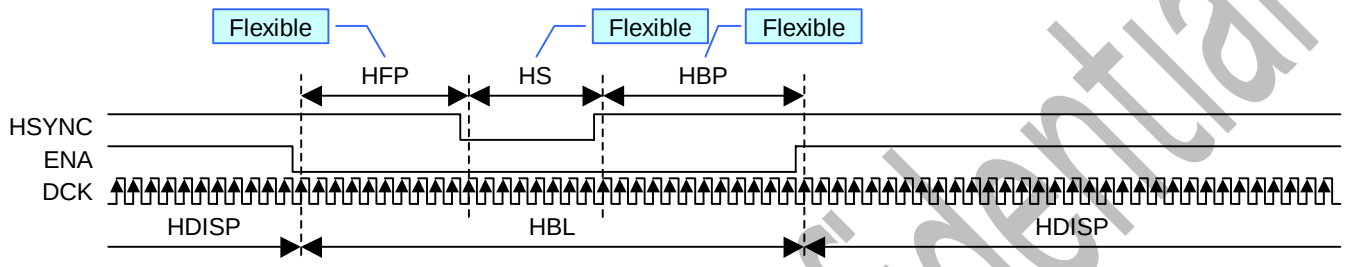
Definition name	Definition detail	Description
Vertical sync	—	VSYNC = LOW shall be recognized by the rising edge of DCK.
Horizontal sync	—	VSYNC = HIGH and HSYNC = LOW shall be recognized by the rising edge of DCK.
LAR	LCDC Access Range	VRAM access range of the LCDC interface (Set by LCDCDADEF)
VR	Vertical Resolution	Number of display lines in the vertical direction (Number of pages set by LCDCDADEF)
VS	Vertical Sync time	Vertical-direction synchronizing interval (Interval from vertical sync to the next horizontal sync)
VFP	Vertical Front Porch	Vertical-direction front porch
VBP	Vertical Back Porch	Vertical-direction back porch
VBL	Vertical BLanking time	Vertical-direction blanking interval (VS + VFP + VBP)
VDISP	Vertical Display Active time	Vertical-direction display-active interval (Display-data valid line interval)
HR	Horizontal Resolution	Number of display pixels in the horizontal direction (Number of columns set by LCDCDADEF)
HS	Horizontal Sync time	Horizontal-direction synchronizing interval (Interval from vertical sync to the next horizontal sync)
HFP	Horizontal Front Porch	Horizontal-direction front porch
HBP	Horizontal Back Porch	Horizontal-direction back porch
HBL	Horizontal BLanking time	Horizontal-direction blanking interval (HS + HFP + HBP)
HDISP	Horizontal Display Active time	Horizontal-direction display-active interval (Display-data valid interval)
VPCC	Vertical Pixel Clock Count	Number of DCK clocks required for writing an amount of display data for VR × HR
HPCC	Horizontal Pixel Clock Count	Number of DCK clocks required for writing an amount of display data for HR

◇ Definitions of vertical direction



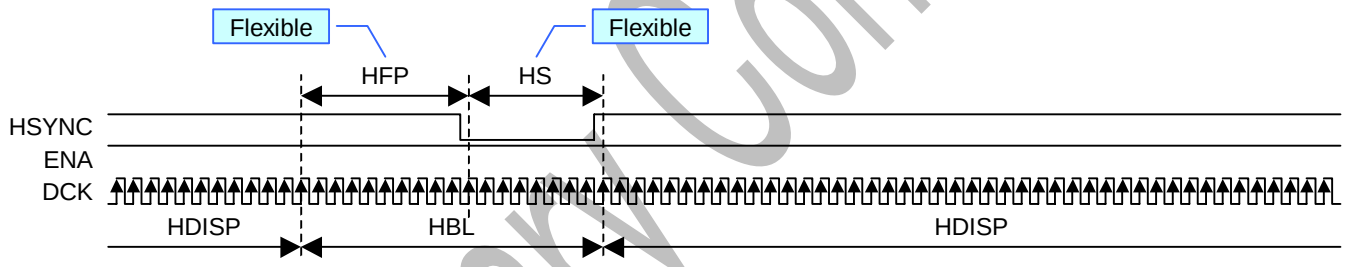
The VBP interval is fixed to a 1-line interval time. The VFP interval varies with the transfer direction of display data. The minimum VFP interval is 0. The length of time for which VSYNC is recognized as being held LOW is the VS interval.

◇ Definitions of horizontal direction (when using ENA)



The HFP and HBP intervals vary depending on the ENA signal. Furthermore, even when ENA = HIGH in the HDISP interval, the HFP interval is entered once DCK has satisfied the HPCC. The length of time for which HSYNC is recognized as being held LOW is the HS interval.

◇ Definitions of horizontal direction (when not using ENA)



The HBP interval is nonexistent. When DCK has satisfied the HPCC in the HDISP interval, the HFP interval is entered. The length of time for which HSYNC is recognized as being held LOW is the HS interval.

When vertically synchronized, the start address set by LAR is reloaded. The interval from vertical sync to the next horizontal sync is the VS interval. The VS interval continues for as long as vertical sync is recognized as being active. A VBP interval equal to one line in duration is entered after the VS interval, which constitutes the VDISP interval in that frame (display-data valid line interval). The VS and VBP intervals are counted by horizontal sync, and the page address is incremented by horizontal sync within the VDISP interval. The interval following VS + VBP + VDISP in one frame automatically comprises the VFP interval, and the VFP interval continues until the next vertical sync occurs. The VS, VFP, and VBP intervals comprise the VBL interval (display-data invalid interval).

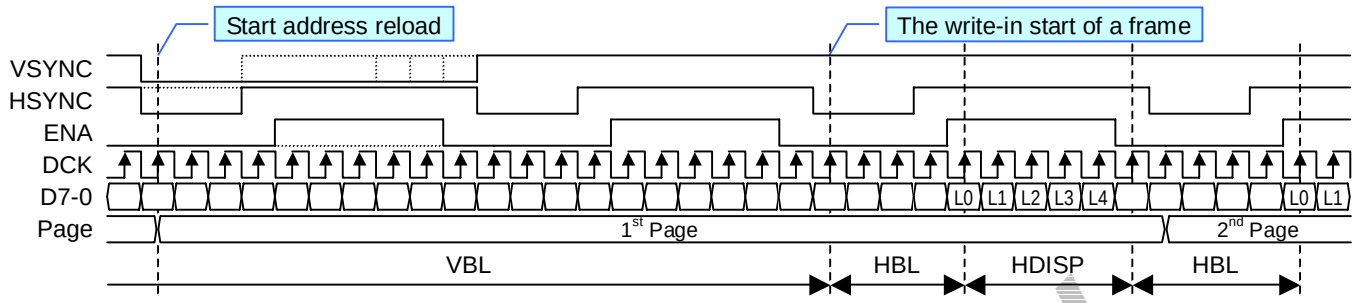
The length of time for which HSYNC = LOW is recognized on the rising edges of DCK in one line within the VDISP interval comprises the HS interval. The length of time for which both HSYNC = HIGH and ENA = LOW are recognized on the rising edges of DCK after the HS interval comprises the HBP interval. When ENA (ENA fixed HIGH) is not being used, the HBP interval is nonexistent. The length of time for which both HSYNC = HIGH and ENA = HIGH are recognized on the rising edges of DCK comprises the HDISP interval in that one line (display-data valid interval). Display data is assumed to be present within the HDISP interval, and the data is latched onto the internal bus holder. After the data for the HPCC has been transferred within the HDISP interval, the HFP interval is entered automatically. The HFP interval continues until the next horizontal sync occurs. The HPCC is determined by the number of accessed columns and the display-data format used, and the column address is automatically incremented according to the valid data and the display-data format.

If DCK oscillation was turned off in the VFP/HFP or other interval in order to recognize VSYNC or HSYNC on the rising edges of DCK, vertical sync or horizontal sync must always be achieved before write can be started again. While DCK is off, the start address is not reloaded and the page address is not incremented by a change in the VSYNC or HSYNC level.

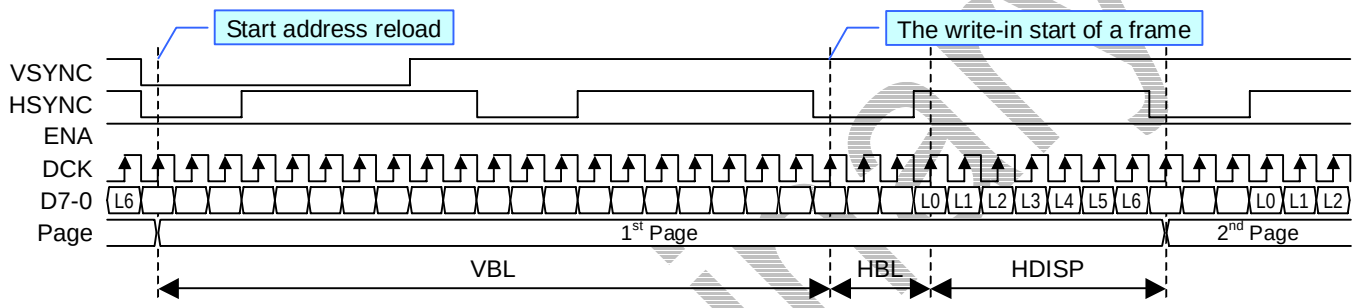
Example interface operations are shown below. The “Ln” in the diagrams below denotes valid data with respect to the horizontal direction, with the number indicating the order of the valid data. The data not marked with an “Ln” is invalid data that is not written into the VRAM.

“Page” in the diagrams below indicates the state of the internal VRAM page address.

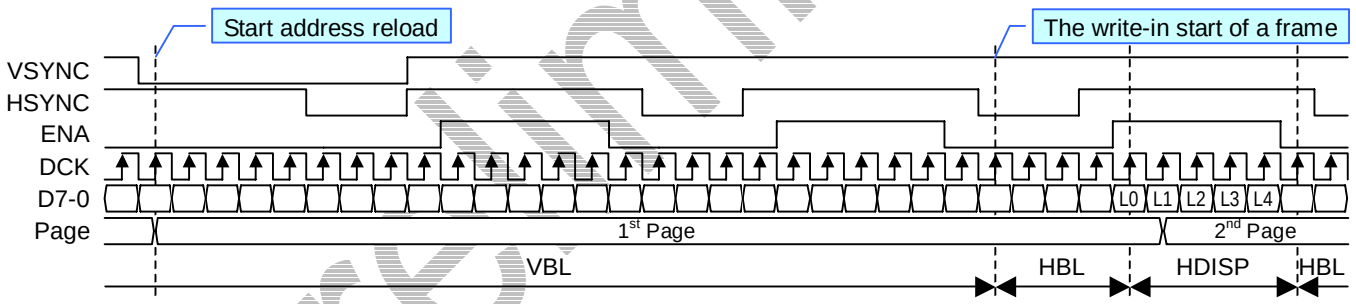
◇ Pattern 1



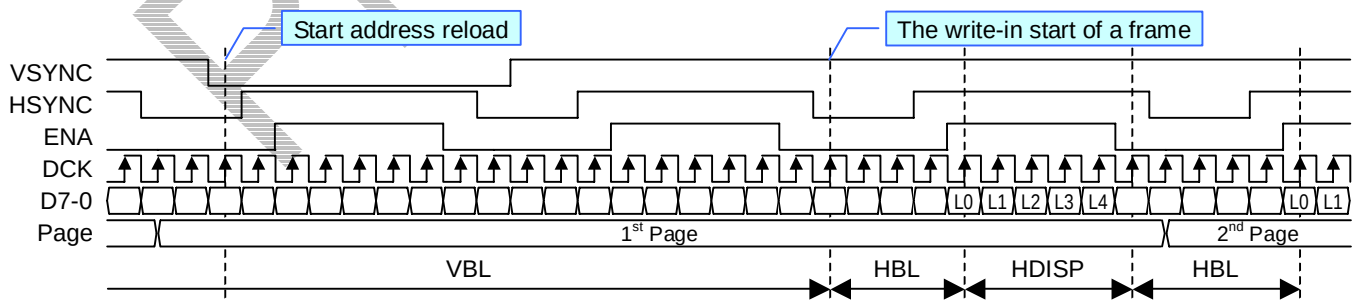
◇ Pattern 2



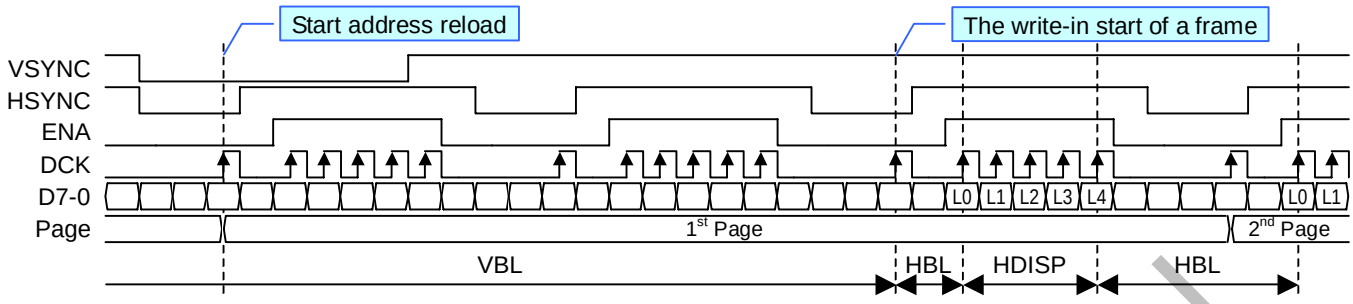
◇ Pattern 3



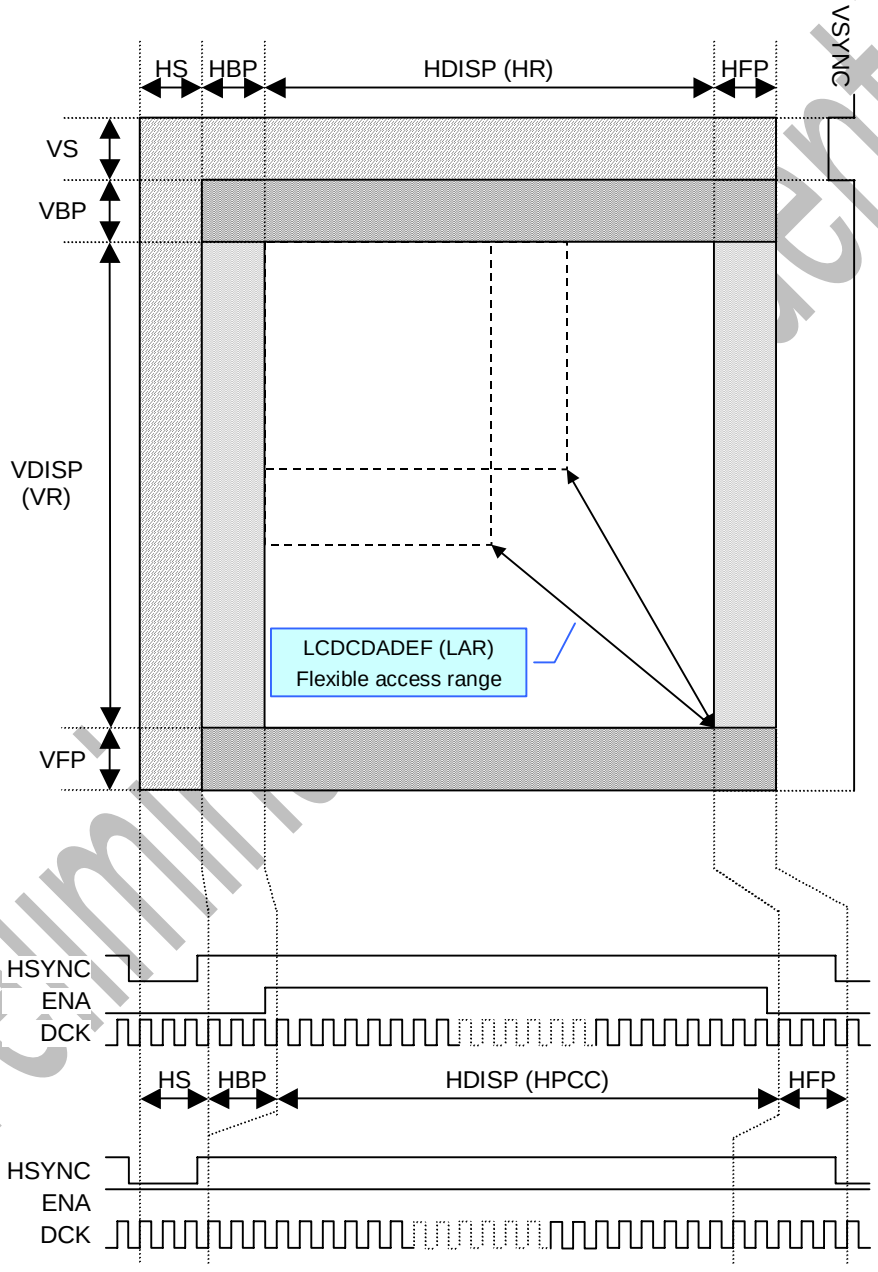
◇ Pattern 4



◇ Pattern 5



◇ Image depicting LCDC interface access

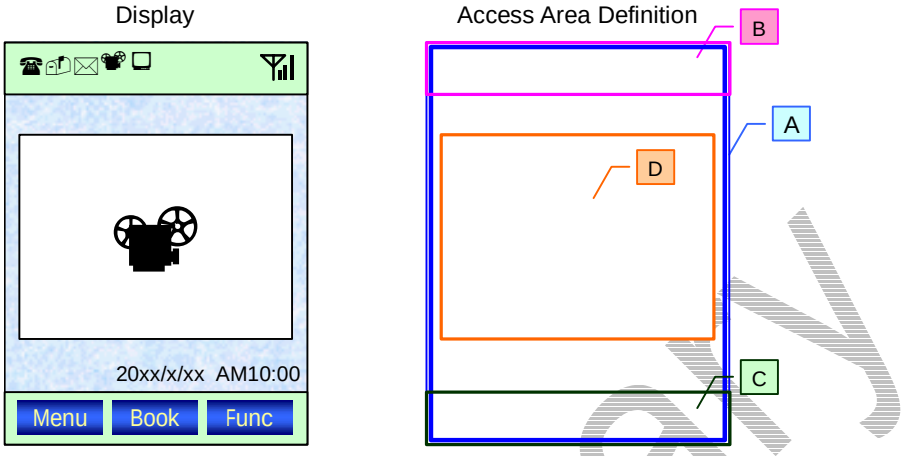


8-2-3. Example Uses of the LCDC Interface

Shown below is an example of the writing of a still picture to the internal VRAM via the MPU interface, and a moving picture via the LCDC interface.

◇ Display screen

The image shown below to the left depicts the display screen. For the example of moving picture, it is assumed that a 15-fps pictorial image is written into the VRAM at a data-transfer rate equivalent to 60 fps. The VRAM access area is defined at below-right.



◇ Writing display data (when using a parallel interface)

(1) Use the LCDCIF command to disable the LCDC interface.

(2) Use the DADEF command to set a full-screen region (A) and the LCDCDADEF command to set a moving-picture region (D).

(3) Write a one-screen image into the full-screen region (A) from the MPU.

(4) Use the LCDCIF command to enable the LCDC interface.

(5) Write moving picture 1 into the moving-picture region (D) from the LCDC.

(6) Use the LCDCIF command to disable the LCDC interface.

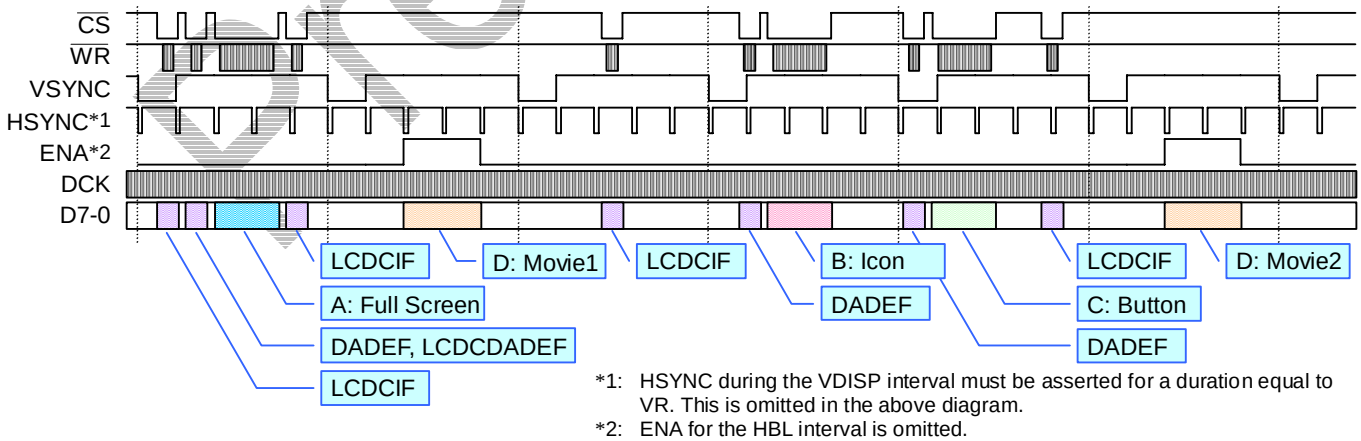
(7) Use the DADEF command to set an icon region (B) and write an image into it as necessary.

(8) Use the DADEF command to set a button region (C) and write an image into it as necessary.

(9) Use the LCDCIF command to enable the LCDC interface.

(10) Write moving picture 2 into the moving-picture region (D) from the LCDC.

* Thereafter, repeat steps (6) to (10). However, the moving-picture image in (10) must be a new moving-picture image.



*1: HSYNC during the VDISP interval must be asserted for a duration equal to VR. This is omitted in the above diagram.
*2: ENA for the HBL interval is omitted.

For the display data to be written, it is necessary that in addition to the above VRAM access areas, the display-data format, LUT, etc., must be set. In the example here, these settings are assumed to have been finished.

8-2-4. Limitations on LCDC Interface

The S1D19122 permits the MPU interface and LCDC interface to be used in combination to write the display data into the VRAM. However, data can only be written to the physical RAM through either of the two interfaces. Therefore, simultaneous accesses to the VRAM from the MPU interface and LCDC interface are prohibited.

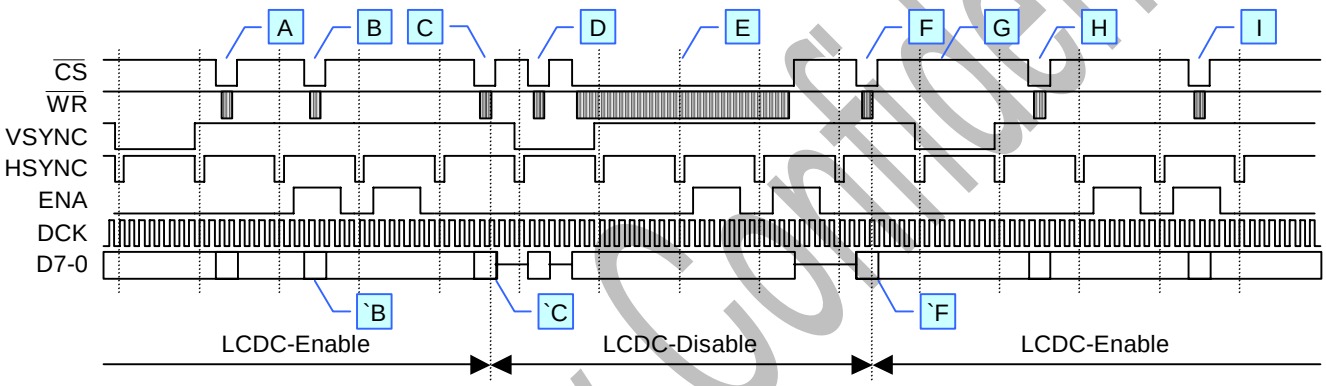
To avoid simultaneous accesses, each interface is subject to the following limitations.

◇ When using the MPU parallel interface

When the LCDC interface is enabled by the LCDCIF command, the MPU interface and LCDC interface use the same data bus, so that when it is necessary to issue command/parameters, they must all be issued within the blank interval of the LCDC interface (VBL or HBL interval). If during the HDISP interval (when the display data is valid) all of the MPU interface access conditions hold true, the driver will assume that command/parameters have been issued despite the fact that the data bus indicates the presence of display data. At the same time, a write from the LCDC interface side will be recognized.

The RAMWR, RAMRD, RDDIDIF, RDID1, RDID2, RDID3, RDDST, STREAD2, EPSRRD, and TESTREG commands that have been issued while the LCDC interface is effective will be interpreted as NOP commands.

For command/parameter issuance, VRAM access, or status readout to be performed from the MPU as necessary, the LCDC interface must first be disabled by the LCDCIF command. If display data again needs to be written from the LCDC interface thereafter, reenable the LCDC interface using the LCDCIF command and then start writing the display data in synchronism with the vertical sync. To issue the LCDCIF command in such cases, always make sure the command is issued within the blank interval.



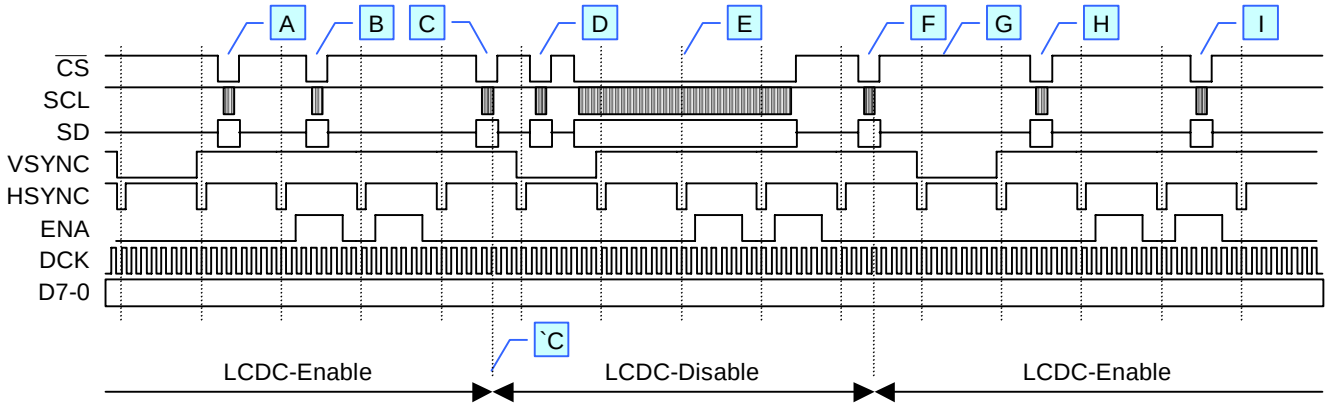
Symbol in diagram	Description	
A	Permitted:	Because this is the blank interval, command/parameters can be issued.
B	Prohibited:	Because this is the HDISP interval, command/parameters cannot be issued.
`B	Caution:	The data bus is assumed to contain display data, commands, or parameters.
C	Limited:	The LCDCIF command and parameters can only be issued in the blank interval.
`C	Limited:	For 100 ns or more after parameters are issued, the data bus must be held at the V_{DDI} or GND potential.
D	Permitted:	Because this is the LCDC interface disabled interval, command/parameters can be issued.
E	Permitted:	Display data can be written from the MPU interface using the RAMWR command.
F	Limited:	LCDCIF command/parameters must be issued in the blank interval.
`F	Limited:	After parameters are issued, the data bus must be held at the V_{DDI} or GND potential.
G	Limited:	After the vertical sync, the MPU must start writing display data from the LCDC interface.
H	Function:	The RAMWR and other commands are interpreted as NOP commands during the LCDC-interface enabled interval.
I	Prohibited:	Because this is the HDISP interval, command/parameters cannot be issued.

◇ When using the MPU serial interface

In this case, as the MPU interface and LCDC interface each operate as a separate interface, there is no need to enable or disable the LCDC interface using the LCDCIF command. Therefore, when a serial interface is selected (P/S = LOW), the LCDC interface is always enabled.

At power-on, the data bus (D7–D0 pins) is directed for input, and must therefore have the V_{DDI} or GNDL potential applied. The data-bus pins cannot be left open.

To access the VRAM from the MPU interface using the RAMWR or RAMRD command, it is necessary that the command be issued within the blank interval of the LCDC interface (VBL or HBL interval). Once the RAMWR or RAMRD command issued is recognized, a state is entered in which only read/write from the MPU interface can be performed. If display data needs to be written from the LCDC interface thereafter, the VRAM access state of the MPU interface must be cancelled by issuing the NOP or other command. The LCDC interface is enabled when said state has been cancelled, so start writing display data in synchronism with the vertical sync. To issue any command equivalent to this cancel command, make sure the command is issued in the blank interval. No other particular limitations are imposed on the issuance of command/parameters in the operation-stabilized interval after power-on.



Symbol in diagram	Description	
A	Permitted:	Because this is the blank interval, command/parameters can be issued.
B	Limited:	Because this is the HDISP interval, command/parameters other than RAMWR and RAMRD can be issued.
C	Limited:	The RAMWR and RAMRD commands must be issued in the blank interval.
`C	Limited:	For at least 100 ns after the blank interval is entered, command issuance must be restrained.
D	Permitted:	Display data can be written (or read out).
E	Permitted:	Display data can be written (or read out).
F	Limited:	A cancel command (other than RAMWR and RAMRD) must be issued in the blank interval.
G	Limited:	After the vertical sync, the MPU must start writing display data from the LCDC interface.
H	Permitted:	Because this is the blank interval, command/parameters can be issued.
I	Limited:	Because this is the HDISP interval, commands other than RAMWR and RAMRD and parameters can be issued.

8-3. Versatile Display-Data Formats

Various data formats are available in which display data can be written to the VRAM. Choose a format suitable for the purpose of use. The data format is determined by a combination of COLMOD and IFMOD commands.

In the table of data formats shown in the following sections, “CD” denotes the RAMWR command (2Ch), and an asterisk (*) denotes invalid bits. The input levels of these bits can be either HIGH or LOW.

◇ Table of display-data formats (IF16BIT=LOW)

			IFMOD B2-B0						IFMOD B4	RGBSET (LUT)
			101b	100b	011b	010b	001b	000b		
			24Bit	18Bit	16Bit	12Bit	9Bit	8Bit		
COLMOD B2-B0	111b	16.8M	24Bit 888 1/1	-	16Bit 888 2/3	-	-	8Bit 888 1/3	0	Un-necessary
					16Bit 888 1/2				1	
	110b	262K	-	18Bit 666 1/1	16Bit 666 2/3	12Bit 666 2/3	9Bit 666 1/2	8Bit 666 1/3	0	Necessary
					16Bit 666 1/2	12Bit 666 1/2			1	
	101b	65K	-	-	16Bit 565 1/1	-	-	8Bit 565 1/2	-	Necessary
	011b	4096	-	-	-	12Bit 444 1/1	-	8Bit 444 2/3	0	Necessary
								8Bit 444 1/2	1	

◇ Table of display-data formats (IF16BIT=HIGH)

			Display Data Format	IFMOD B4	RGBSET (262KC LUT)
COLMOD B2-B0	111b	16.8M	16Bit 888 2/3	-	Un-necessary
	110b	262K	16Bit 666 2/3	-	Necessary
	101b	65K	16Bit 565 1/1	-	Necessary
	011b	4096	12Bit 444 1/1	-	Necessary

◇ About the serial interface

When a serial interface is used, only the display-data formats whose display data is 8 bits in width can be selected. Therefore, the display-data width is fixed internally to 8 bits regardless of what value is set by IFMOD.

8-3-1. 16.8M Color Mode

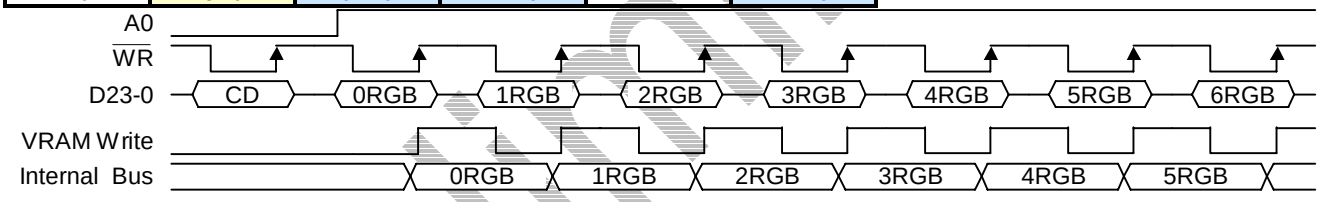
For display data to be accessed in 16.8M color mode, it is necessary that 16.8M color mode be selected (B2-B0: 111) using the COLMOD command before writing or reading to or from the VRAM.

In this mode, per-pixel display data comprised of 8 bits for R, 8 bits for G, and 8 bits for B is written to the VRAM. When all of the data for one pixel (RGB) been prepared in the internal register, the MPU writes the data to the VRAM.

When data is read from the VRAM one dummy read cycle after the RAMRD command is issued, the data is read out to the MPU bus according to the selected format.

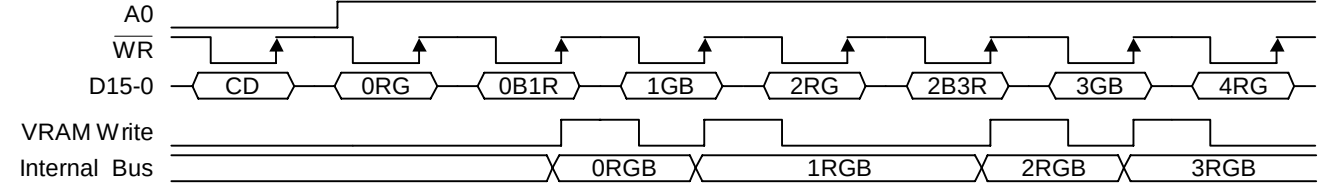
◇ 24-bit 888 1/1 format

Cycle count	0	1	2	…	n+1
A0	L	H	H	…	H
D23	*	0DR7	1DR7	…	nDR7
D22	*	0DR6	1DR6	…	nDR6
D21	*	0DR5	1DR5	…	nDR5
D20	*	0DR4	1DR4	…	nDR4
D19	*	0DR3	1DR3	…	nDR3
D18	*	0DR2	1DR2	…	nDR2
D17	*	0DR1	1DR1	…	nDR1
D16	*	0DR0	1DR0	…	nDR0
D15	*	0DG7	1DG7	…	nDG7
D14	*	0DG6	1DG6	…	nDG6
D13	*	0DG5	1DG5	…	nDG5
D12	*	0DG4	1DG4	…	nDG4
D11	*	0DG3	1DG3	…	nDG3
D10	*	0DG2	1DG2	…	nDG2
D9	*	0DG1	1DG1	…	nDG1
D8	*	0DG0	1DG0	…	nDG0
D7	CD7	0DB7	1DB7	…	nDB7
D6	CD6	0DB6	1DB6	…	nDB6
D5	CD5	0DB5	1DB5	…	nDB5
D4	CD4	0DB4	1DB4	…	nDB4
D3	CD3	0DB3	1DB3	…	nDB3
D2	CD2	0DB2	1DB2	…	nDB2
D1	CD1	0DB1	1DB1	…	nDB1
D0	CD0	0DB0	1DB0	…	nDB0



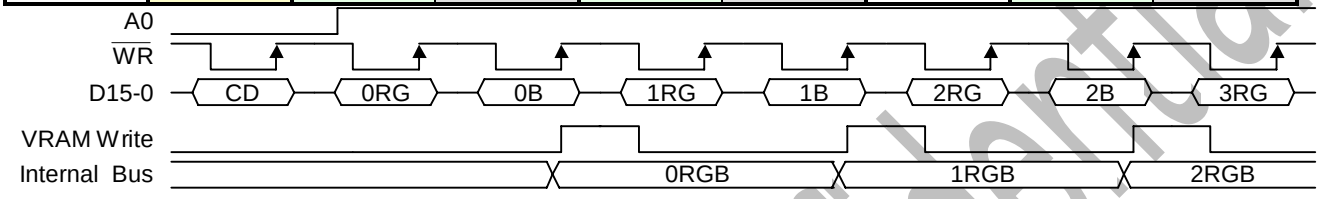
◇ 16-bit 888 2/3 format

Cycle count	0	1	2	3	…	3n+1	3n+2	3n+3
A0	L	H	H	H	…	H	H	H
D15	*	0DR7	0DB7	1DG7	…	2nDR7	2nDB7	(2n+1)DG7
D14	*	0DR6	0DB6	1DG6		2nDR6	2nDB6	(2n+1)DG6
D13	*	0DR5	0DB5	1DG5		2nDR5	2nDB5	(2n+1)DG5
D12	*	0DR4	0DB4	1DG4		2nDR4	2nDB4	(2n+1)DG4
D11	*	0DR3	0DB3	1DG3		2nDR3	2nDB3	(2n+1)DG3
D10	*	0DR2	0DB2	1DG2		2nDR2	2nDB2	(2n+1)DG2
D9	*	0DR1	0DB1	1DG1	…	2nDR1	2nDB1	(2n+1)DG1
D8	*	0DR0	0DB0	1DG0	…	2nDR0	2nDB0	(2n+1)DG0
D7	CD7	0DG7	1DR7	1DB7	…	2nDG7	(2n+1)DR7	(2n+1)DB7
D6	CD6	0DG6	1DR6	1DB6	…	2nDG6	(2n+1)DR6	(2n+1)DB6
D5	CD5	0DG5	1DR5	1DB5	…	2nDG5	(2n+1)DR5	(2n+1)DB5
D4	CD4	0DG4	1DR4	1DB4	…	2nDG4	(2n+1)DR4	(2n+1)DB4
D3	CD3	0DG3	1DR3	1DB3	…	2nDG3	(2n+1)DR3	(2n+1)DB3
D2	CD2	0DG2	1DR2	1DB2	…	2nDG2	(2n+1)DR2	(2n+1)DB2
D1	CD1	0DG1	1DR1	1DB1	…	2nDG1	(2n+1)DR1	(2n+1)DB1
D0	CD0	0DG0	1DR0	1DB0	…	2nDG0	(2n+1)DR0	(2n+1)DB0



◇ 16-bit 888 1/2 format

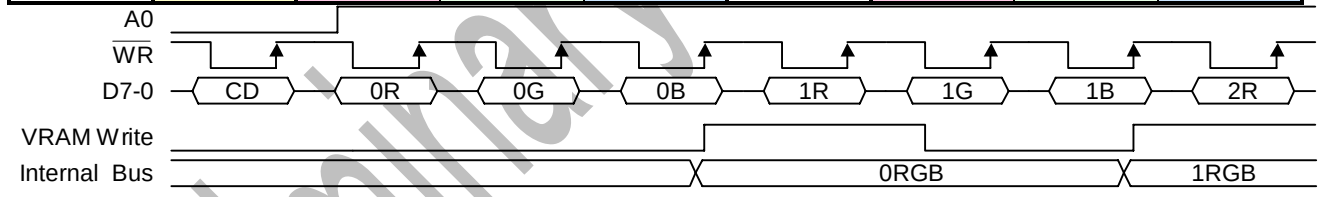
Cycle count	0	1	2	3	4	…	2n+1	2n+2
A0	L	H	H	H	H	…	H	H
D15	*	0DR7	0DB7	1DR7	1DB7	…	nDR7	nDB7
D14	*	0DR6	0DB6	1DR6	1DB6	…	nDR6	nDB6
D13	*	0DR5	0DB5	1DR5	1DB5	…	nDR5	nDB5
D12	*	0DR4	0DB4	1DR4	1DB4	…	nDR4	nDB4
D11	*	0DR3	0DB3	1DR3	1DB3	…	nDR3	nDB3
D10	*	0DR2	0DB2	1DR2	1DB2	…	nDR2	nDB2
D9	*	0DR1	0DB1	1DR1	1DB1	…	nDR2	nDB1
D8	*	0DR0	0DB0	1DR0	1DB0	…	nDR0	nDB0
D7	CD7	0DG7	*	1DG7	*	…	nDG7	*
D6	CD6	0DG6	*	1DG6	*	…	nDG6	*
D5	CD5	0DG5	*	1DG5	*	…	nDG5	*
D4	CD4	0DG4	*	1DG4	*	…	nDG4	*
D3	CD3	0DG3	*	1DG3	*	…	nDG3	*
D2	CD2	0DG2	*	1DG2	*	…	nDG2	*
D1	CD1	0DG1	*	1DG1	*	…	nDG1	*
D0	CD0	0DG0	*	1DG0	*	…	nDG0	*



◇ 8-bit 888 1/3 format

For the 1/3 format (written to the VRAM once every 3 transfers) only, the HIGH pulse width for write to the internal VRAM is 1.5 times the clock pulse. If any command (including RAMWR) needs to be issued after the last pixel data is written to the VRAM, an idle time sufficient for 2 bytes of data to be transferred must be provided. During the LCDC interface, HFP must be asserted for a period of two DCK cycles or more.

Cycle count	0	1	2	3	…	3n+1	3n+2	3n+3
A0	L	H	H	H	…	H	H	H
D7	CD7	0DR7	0DG7	0DB7	…	nDR7	nDG7	nDB7
D6	CD6	0DR6	0DG6	0DB6	…	nDR6	nDG6	nDB6
D5	CD5	0DR5	0DG5	0DB5	…	nDR5	nDG5	nDB5
D4	CD4	0DR4	0DG4	0DB4	…	nDR4	nDG4	nDB4
D3	CD3	0DR3	0DG3	0DB3	…	nDR3	nDG3	nDB3
D2	CD2	0DR2	0DG2	0DB2	…	nDR2	nDG2	nDB2
D1	CD1	0DR1	0DG1	0DB1	…	nDR1	nDG1	nDB1
D0	CD0	0DR0	0DG0	0DB0	…	nDR0	nDG0	nDB0



8-3-2. 262K Color Mode

For display data to be accessed in 262K color mode, it is necessary that 262K color mode be selected (B2-B0: 110) using the COLMOD command before writing or reading to or from the VRAM.

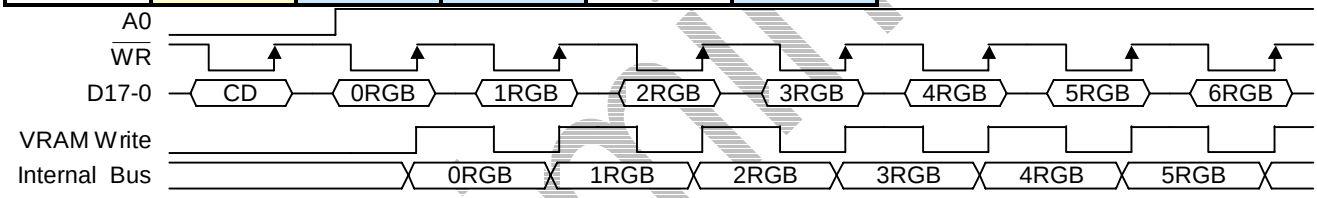
In this mode, per-pixel display data comprised of 6 bits for R, 6 bits for G, and 6 bits for B is written to the VRAM. When all of the data for one pixel (RGB) has been prepared in the internal register, the MPU writes the data to the VRAM.

When data is written to the VRAM, the data is converted by the LUT (lookup table) set via RGBSET before being written to the VRAM. Before writing data to the VRAM in this mode, always be sure to set the RGBSET command.

When data is read from the VRAM one dummy read cycle after the RAMRD command is issued, the data is read out to the MPU bus according to a selected format.

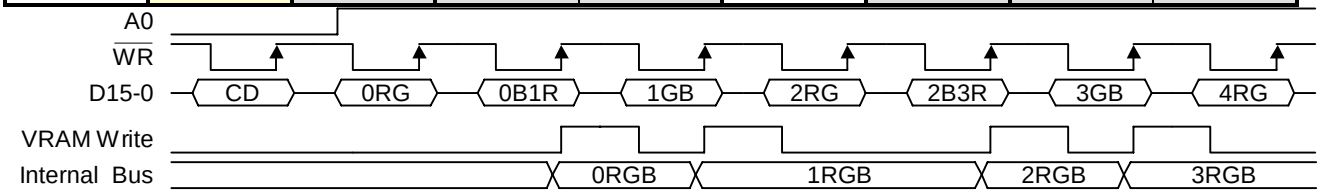
◇ 18-bit 666 1/1 format

Cycle count	0	1	2	…	n+1
A0	L	H	H	…	H
D17	*	0DR7	1DR7	…	nDR7
D16	*	0DR6	1DR6	…	nDR6
D15	*	0DR5	1DR5	…	nDR5
D14	*	0DR4	1DR4	…	nDR4
D13	*	0DR3	1DR3	…	nDR3
D12	*	0DR2	1DR2	…	nDR2
D11	*	0DG7	1DG7	…	nDG7
D10	*	0DG6	1DG6	…	nDG6
D9	*	0DG5	1DG5	…	nDG5
D8	*	0DG4	1DG4	…	nDG4
D7	CD7	0DG3	1DG3	…	nDG3
D6	CD6	0DG2	1DG2	…	nDG2
D5	CD5	0DB7	1DB7	…	nDB7
D4	CD4	0DB6	1DB6	…	nDB6
D3	CD3	0DB5	1DB5	…	nDB5
D2	CD2	0DB4	1DB4	…	nDB4
D1	CD1	0DB3	1DB3	…	nDB3
D0	CD0	0DB2	1DB2	…	nDB2



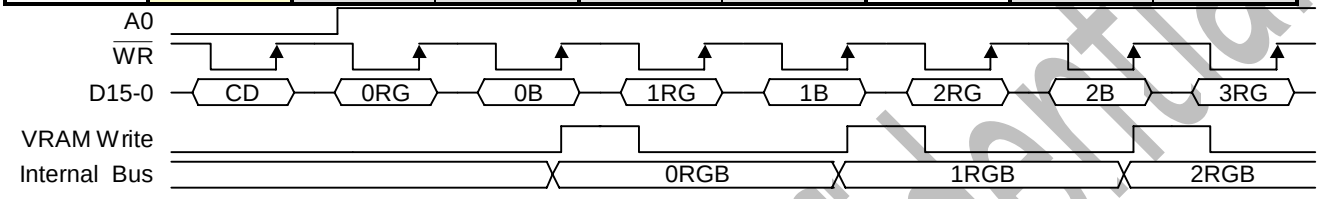
◇ 16-bit 666 2/3 format

Cycle count	0	1	2	3	…	3n+1	3n+2	3n+3
A0	L	H	H	H	…	H	H	H
D15	*	0DR7	0DB7	1DG7	…	2nDR7	2nDB7	(2n+1)DG7
D14	*	0DR6	0DB6	1DG6	…	2nDR6	2nDB6	(2n+1)DG6
D13	*	0DR5	0DB5	1DG5	…	2nDR5	2nDB5	(2n+1)DG5
D12	*	0DR4	0DB4	1DG4		2nDR4	2nDB4	(2n+1)DG4
D11	*	0DR3	0DB3	1DG3		2nDR3	2nDB3	(2n+1)DG3
D10	*	0DR2	0DB2	1DG2	…	2nDR2	2nDB2	(2n+1)DG2
D9	*	*	*	*	…	*	*	*
D8	*	*	*	*	…	*	*	*
D7	CD7	0DG7	1DR7	1DB7	…	2nDG7	(2n+1)DR7	(2n+1)DB7
D6	CD6	0DG6	1DR6	1DB6		2nDG6	(2n+1)DR6	(2n+1)DB6
D5	CD5	0DG5	1DR5	1DB5		2nDG5	(2n+1)DR5	(2n+1)DB5
D4	CD4	0DG4	1DR4	1DB4	…	2nDG4	(2n+1)DR4	(2n+1)DB4
D3	CD3	0DG3	1DR3	1DB3	…	2nDG3	(2n+1)DR3	(2n+1)DB3
D2	CD2	0DG2	1DR2	1DB2	…	2nDG2	(2n+1)DR2	(2n+1)DB2
D1	CD1	*	*	*	…	*	*	*
D0	CD0	*	*	*	…	*	*	*



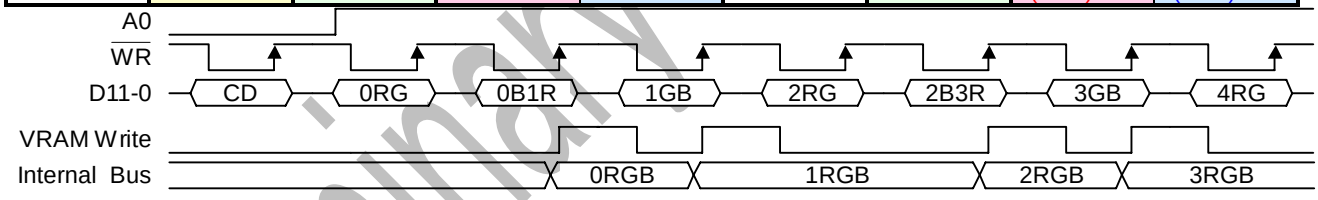
◇ 16-bit 666 1/2 format

Cycle count	0	1	2	3	4	…	2n+1	2n+2
A0	L	H	H	H	H	…	H	H
D15	*	0DR7	0DB7	1DR7	1DB7	…	nDR7	nDB7
D14	*	0DR6	0DB6	1DR6	1DB6	…	nDR6	nDB6
D13	*	0DR5	0DB5	1DR5	1DB5	…	nDR5	nDB5
D12	*	0DR4	0DB4	1DR4	1DB4		nDR4	nDB4
D11	*	0DR3	0DB3	1DR3	1DB3		nDR3	nDB3
D10	*	0DR2	0DB2	1DR2	1DB2	…	nDR2	nDB2
D9	*	*	*	*	*	…	*	*
D8	*	*	*	*	*	…	*	*
D7	CD7	0DG7	*	1DG7	*	…	nDG7	*
D6	CD6	0DG6	*	1DG6	*		nDG6	*
D5	CD5	0DG5	*	1DG5	*		nDG5	*
D4	CD4	0DG4	*	1DG4	*	…	nDG4	*
D3	CD3	0DG3	*	1DG3	*	…	nDG3	*
D2	CD2	0DG2	*	1DG2	*	…	nDG2	*
D1	CD1	*	*	*	*	…	*	*
D0	CD0	*	*	*	*	…	*	*



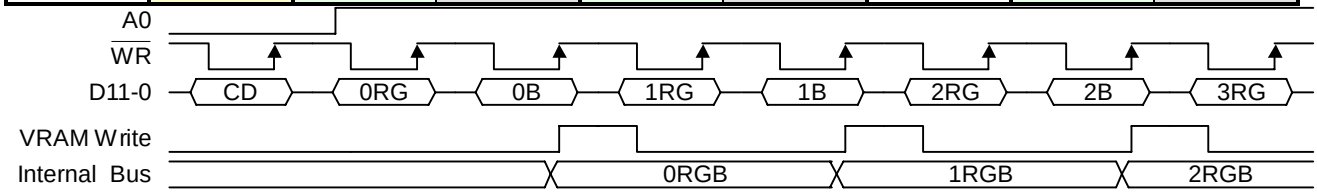
◇ 12-bit 666 2/3 format

Cycle count	0	1	2	3	…	3n+1	3n+2	3n+3
A0	L	H	H	H	…	H	H	H
D11	*	0DR7	0DB7	1DG7	…	2nDR7	2nDB7	(2n+1)DG7
D10	*	0DR6	0DB6	1DG6	…	2nDR6	2nDB6	(2n+1)DG6
D9	*	0DR5	0DB5	1DG5	…	2nDR5	2nDB5	(2n+1)DG5
D8	*	0DR4	0DB4	1DG4	…	2nDR4	2nDB4	(2n+1)DG4
D7	CD7	0DR3	0DB3	1DG3	…	2nDR3	2nDB3	(2n+1)DG3
D6	CD6	0DR2	0DB2	1DG2	…	2nDR2	2nDB2	(2n+1)DG2
D5	CD5	0DG7	1DR7	1DB7	…	2nDG7	(2n+1)DR7	(2n+1)DB7
D4	CD4	0DG6	1DR6	1DB6	…	2nDG6	(2n+1)DR6	(2n+1)DB6
D3	CD3	0DG5	1DR5	1DB5	…	2nDG5	(2n+1)DR5	(2n+1)DB5
D2	CD2	0DG4	1DR4	1DB4	…	2nDG4	(2n+1)DR4	(2n+1)DB4
D1	CD1	0DG3	1DR3	1DB3	…	2nDG3	(2n+1)DR3	(2n+1)DB3
D0	CD0	0DG2	1DR2	1DB2	…	2nDG2	(2n+1)DR2	(2n+1)DB2



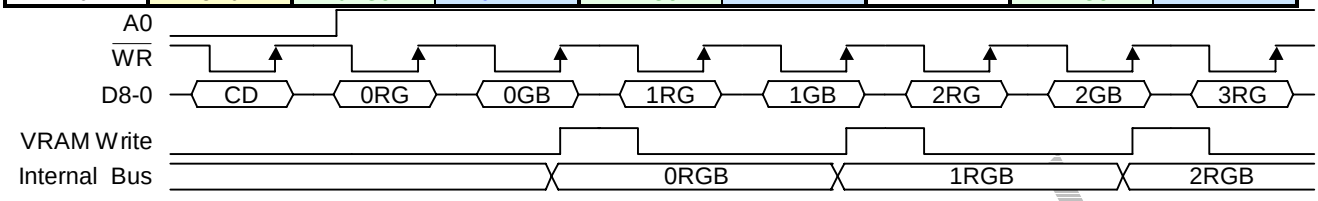
◇ 12-bit 666 1/2 format

Cycle count	0	1	2	3	4	…	2n+1	2n+2
A0	L	H	H	H	H	…	H	H
D11	*	0DR7	0DB7	1DR7	1DB7	…	nDR7	nDB7
D10	*	0DR6	0DB6	1DR6	1DB6	…	nDR6	nDB6
D9	*	0DR5	0DB5	1DR5	1DB5	…	nDR5	nDB5
D8	*	0DR4	0DB4	1DR4	1DB4	…	nDR4	nDB4
D7	CD7	0DR3	0DB3	1DR3	1DB3	…	nDR3	nDB3
D6	CD6	0DR2	0DB2	1DR2	1DB2	…	nDR2	nDB2
D5	CD5	0DG7	*	1DG7	*	…	nDG7	*
D4	CD4	0DG6	*	1DG6	*	…	nDG6	*
D3	CD3	0DG5	*	1DG5	*	…	nDG5	*
D2	CD2	0DG4	*	1DG4	*	…	nDG4	*
D1	CD1	0DG3	*	1DG3	*	…	nDG3	*
D0	CD0	0DG2	*	1DG2	*	…	nDG2	*



◇ 9-bit 666 1/2 format

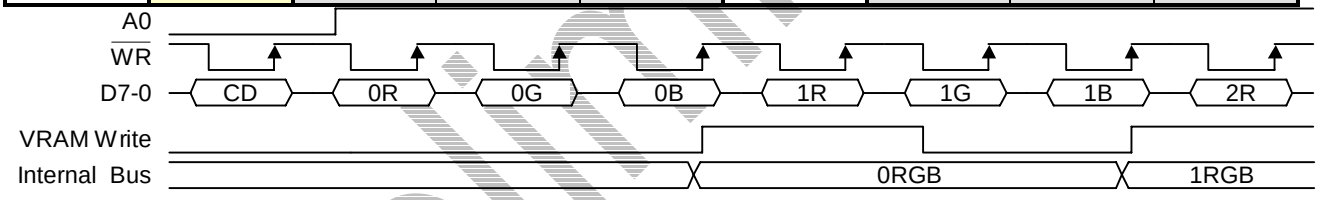
Cycle count	0	1	2	3	4	…	2n+1	2n+2
A0	L	H	H	H	H	…	H	H
D8	*	0DR7	0DG4	1DR7	1DG4	…	nDR7	nDG4
D7	CD7	0DR6	0DG3	1DR6	1DG3	…	nDR6	nDG3
D6	CD6	0DR5	0DG2	1DR5	1DG2	…	nDR5	nDG2
D5	CD5	0DR4	0DB7	1DR4	1DB7	…	nDR4	nDB7
D4	CD4	0DR3	0DB6	1DR3	1DB6	…	nDR3	nDB6
D3	CD3	0DR2	0DB5	1DR2	1DB5	…	nDR2	nDB5
D2	CD2	0DG7	0DB4	1DG7	1DB4	…	nDG7	nDB4
D1	CD1	0DG6	0DB3	1DG6	1DB3	…	nDG6	nDB3
D0	CD0	0DG5	0DB2	1DG5	1DB2	…	nDG5	nDB2



◇ 8-bit 666 1/3 format

For the 1/3 format (written to the VRAM once every 3 transfers) only, the HIGH pulse width for write to the internal VRAM is 1.5 times the clock pulse. If any command (including RAMWR) needs to be issued after the last pixel data is written to the VRAM, an idle time sufficient for 2 bytes of data to be transferred must be provided. During the LCDC interface, HFP must be asserted for a period of two DCK cycles or more.

Cycle count	0	1	2	3	…	3n+1	3n+2	3n+3
A0	L	H	H	H	…	H	H	H
D7	CD7	0DR7	0DG7	0DB7	…	nDR7	nDG7	nDB7
D6	CD6	0DR6	0DG6	0DB6	…	nDR6	nDG6	nDB6
D5	CD5	0DR5	0DG5	0DB5	…	nDR5	nDG5	nDB5
D4	CD4	0DR4	0DG4	0DB4	…	nDR4	nDG4	nDB4
D3	CD3	0DR3	0DG3	0DB3	…	nDR3	nDG3	nDB3
D2	CD2	0DR2	0DG2	0DB2	…	nDR2	nDG2	nDB2
D1	CD1	*	*	*	…	*	*	*
D0	CD0	*	*	*	…	*	*	*



8-3-3. 65K Color Mode

For display data to be accessed in 65K color mode, it is necessary that 65K color mode be selected (B2-B0: 101) using the COLMOD command before writing or reading to or from the VRAM.

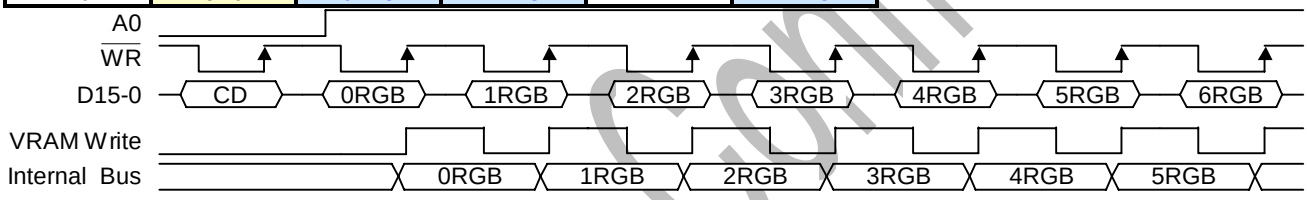
In this mode, per-pixel display data comprised of 5 bits for R, 6 bits for G, and 5 bits for B is written to the VRAM. When all of the data for one pixel (RGB) has been prepared in the internal register, the MPU writes the data to the VRAM.

When data is written to the VRAM, the data is converted by the LUT (lookup table) set via RGBSET before being written to the VRAM. Before writing data to the VRAM in this mode, always be sure to set the RGBSET command.

When data is read from the VRAM one dummy read cycle after the RAMRD command is issued, the data is read out to the MPU bus according to a selected format.

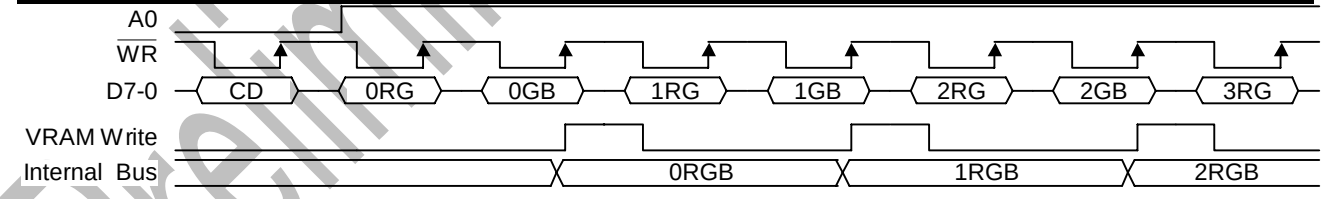
◇ 16-bit 565 1/1 format

Cycle count	0	1	2	…	n+1
A0	L	H	H	…	H
D15	*	0DR7	1DR7	…	nDR7
D14	*	0DR6	1DR6	…	nDR6
D13	*	0DR5	1DR5	…	nDR5
D12	*	0DR4	1DR4	…	nDR4
D11	*	0DR3	1DR3	…	nDR3
D10	*	0DG7	1DG7	…	nDG7
D9	*	0DG6	1DG6	…	nDG6
D8	*	0DG5	1DG5	…	nDG5
D7	CD7	0DG4	1DG4	…	nDG4
D6	CD6	0DG3	1DG3	…	nDG3
D5	CD5	0DG2	1DG2	…	nDG2
D4	CD4	0DB7	1DB7	…	nDB7
D3	CD3	0DB6	1DB6	…	nDB6
D2	CD2	0DB5	1DB5	…	nDB5
D1	CD1	0DB4	1DB4	…	nDB4
D0	CD0	0DB3	1DB3	…	nDB3



◇ 8-bit 565 1/2 format

Cycle count	0	1	2	3	4	…	2n+1	2n+2
A0	L	H	H	H	H	…	H	H
D7	CD7	0DR7	0DG4	1DR7	1DG4	…	nDR7	nDG4
D6	CD6	0DR6	0DG3	1DR6	1DG3	…	nDR6	nDG3
D5	CD5	0DR5	0DG2	1DR5	1DG2	…	nDR5	nDG2
D4	CD4	0DR4	0DB7	1DR4	1DB7	…	nDR4	nDB7
D3	CD3	0DR3	0DB6	1DR3	1DB6	…	nDR3	nDB6
D2	CD2	0DG7	0DB5	1DG7	1DB5	…	nDG7	nDB5
D1	CD1	0DG6	0DB4	1DG6	1DB4	…	nDG6	nDB4
D0	CD0	0DG5	0DB3	1DG5	1DB3	…	nDG5	nDB3



8-3-4. 4096-Color Mode

For display data to be accessed in 4096-color mode, it is necessary that the mode be selected (B2-B0: 011) using the COLMOD command before writing or reading to or from the VRAM.

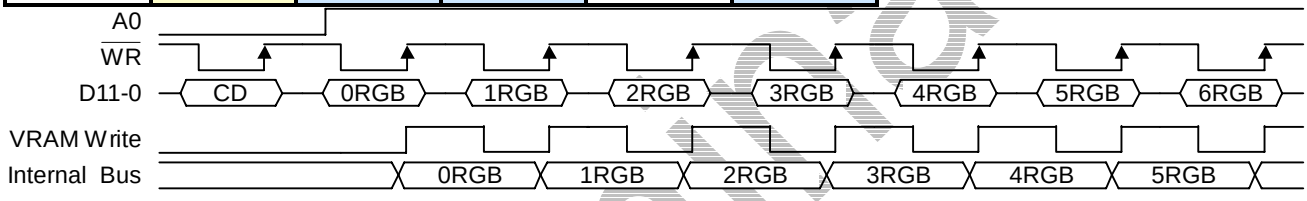
In this mode, per-pixel display data comprised of 4 bits for R, 4 bits for G, and 4 bits for B is written to the VRAM. When all of the data for one pixel (RGB) has been prepared in the internal register, the MPU writes the data to the VRAM.

When data is written to the VRAM, the data is converted by the LUT (lookup table) set via RGBSET before being written to the VRAM. Before writing data to the VRAM in this mode, always be sure to set the RGBSET command.

When data is read from the VRAM one dummy read cycle after the RAMRD command is issued, the data is read out to the MPU bus according to a selected format. The read-out data consists of 4 LUT-converted high-order bits for each of R, G, and B.

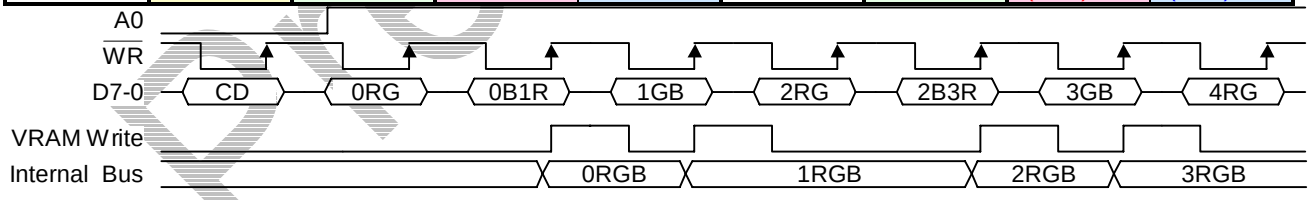
◇ 12-bit 444 1/1 format

Cycle count	0	1	2	…	n+1
A0	L	H	H	…	H
D11	*	0DR7	1DR7	…	nDR7
D10	*	0DR6	1DR6	…	nDR6
D9	*	0DR5	1DR5	…	nDR5
D8	*	0DR4	1DR4	…	nDR4
D7	CD7	0DG7	1DG7	…	nDG7
D6	CD6	0DG6	1DG6	…	nDG6
D5	CD5	0DG5	1DG5	…	nDG5
D4	CD4	0DG4	1DG4	…	nDG4
D3	CD3	0DB7	1DB7	…	nDB7
D2	CD2	0DB6	1DB6	…	nDB6
D1	CD1	0DB5	1DB5	…	nDB5
D0	CD0	0DB4	1DB4	…	nDB4



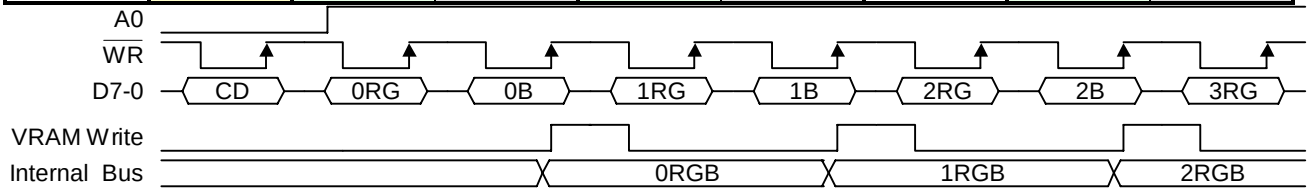
◇ 8-bit 444 2/3 format

Cycle count	0	1	2	3	…	3n+1	3n+2	3n+3
A0	L	H	H	H	…	H	H	H
D7	CD7	0DR7	0DB7	1DG7	…	2nDR7	2nDB7	(2n+1)DG7
D6	CD6	0DR6	0DB6	1DG6	…	2nDR6	2nDB6	(2n+1)DG6
D5	CD5	0DR5	0DB5	1DG5	…	2nDR5	2nDB5	(2n+1)DG5
D4	CD4	0DR4	0DB4	1DG4	…	2nDR4	2nDB4	(2n+1)DG4
D3	CD3	0DG7	1DR7	1DB7	…	2nDG7	(2n+1)DR7	(2n+1)DB7
D2	CD2	0DG6	1DR6	1DB6	…	2nDG6	(2n+1)DR6	(2n+1)DB6
D1	CD1	0DG5	1DR5	1DB5	…	2nDG5	(2n+1)DR5	(2n+1)DB5
D0	CD0	0DG4	1DR4	1DB4	…	2nDG4	(2n+1)DR4	(2n+1)DB4



◇ 8-bit 444 1/2 format

Cycle count	0	1	2	3	4	…	2n+1	2n+2
A0	L	H	H	H	H	…	H	H
D7	CD7	0DR7	0DB7	1DR7	1DB7	…	nDR7	nDB7
D6	CD6	0DR6	0DB6	1DR6	1DB6	…	nDR6	nDB6
D5	CD5	0DR5	0DB5	1DR5	1DB5	…	nDR5	nDB5
D4	CD4	0DR4	0DB4	1DR4	1DB4	…	nDR4	nDB4
D3	CD3	0DG7	*	1DG7	*	…	nDG7	*
D2	CD2	0DG6	*	1DG6	*	…	nDG6	*
D1	CD1	0DG5	*	1DG5	*	…	nDG5	*
D0	CD0	0DG4	*	1DG4	*	…	nDG4	*



8-4. Reset

The S1D19122 may be reset in either the hardware or software. However, when the IC needs to be reset after power-on, it must always be reset in the hardware.

8-4-1. Hardware Reset

This refers to resetting the IC using the $\overline{RES}$ pin level.

When the $\overline{RES}$ pin is pulled LOW, all operations of the IC stop and the IC is placed in a reset state. The timing with which the $\overline{RES}$ pin is recognized as being pulled LOW depends on the AC characteristics of the IC.

Refer to Section 11-2-5, “Reset Timing Characteristics.”

8-4-2. Software Reset

This refers to resetting the IC by issuing the SWRESET command.

The IC is placed in a reset state after the SWRESET command is recognized. However, depending on how the IC pins are set, the IC may be stopped from operating in a sleep state after executing an initialize or an auto display-off sequence.

Refer to Section 8-12-2, “Initialize.”

Refer to Section 8-13-1, “Auto Display-Off Sequence.”

8-4-3. Comparison between Hardware and Software Resets

In addition to the difference in reset methods, the IC behaves differently for hardware and software resets. The tables below compare hardware and software resets.

◇ Reset method

Reset	Description	Remark
Hardware	Reset using the $\overline{RES}$ pin level	-
Software	Reset using the SWRESET command	-

◇ Reset state 1

Reset	Description	Remark
Hardware	All operations stop	-
Software	All operations stop	INISEL=LOW, RESSEL=LOW
	Initialized before all operations stop	INISEL=HIGH, RESSEL=LOW
	The auto-display off sequence is executed before all operations stop.	INISEL=HIGH, RESSEL=HIGH

◇ Reset state 2

Reset	Description	Remark
Hardware	The commands that have initial values are reset to those values.	-
Software	All commands except special commands are reset to their initial values.	INISEL=LOW
	The commands subject to initialization are reset to their initialized values.	INISEL=HIGH

Regardless of whether the IC is reset in hardware or software, the video memory data is not reset.

Refer to Section 8-4-4, “Reset State.”

Refer to Section 9-1, “Command Table.”

◇ Auto-display off sequence

Reset	Description	Remark
Hardware	Reset immediately. When reset, POFF = LOW.	-
Software	Reset after recognition of the SWRESET command. When reset, POFF = LOW.	When the display is off
	Reset after internal horizontal sync. When reset, POFF = HIGH.	When the display is on

8-4-4. Reset State

The table below lists the default settings that are assumed when the IC is reset.

◇ State

Function	Related command	Default value	
Sleep state	SLPIN / SLPOUT	Sleep	SLPIN
Display state	DISOFF / DISON	Displayed turned off	DISOFF
Gradation normal/reverse	DISINOFF / DISINV	Gradation normal mode	DISINOFF
Display mode	NORON / PTLON VSCRSADD	Normal display mode	NORON
Binary mode	IDMON / IDMOFF	Normal mode (256 gray scale levels)	IDMOFF
Read ID	RDDIDIF RDID1 / RDID2 / RDID3	RDID1 (manufacturer ID)	P1 (29h)
		RDID2 (module version)	P1 (00h)
		RDID3 (module ID)	P1 (00h)
Partial area	PTLAR	Beginning line: 0	P1, P2 (0000h)
		Ending line: 239	P3, P4 (00EFh)
Scroll area	VSCRDEF	Top fix line: 0	P1, P2 (0000h)
		Scroll area: 240	P3, P4 (00F0h)
		Bottom fix line: 0	P5, P6 (0000h)
MPU column address area	CASET (DADEF)	Column start: 0	P1, P2 (0000h)
		Column end: 319	P3, P4 (013Fh)
MPU page address area	PASET (DADEF)	Page start: 0	P1, P2 (0000h)
		Page end: 239	P3, P4 (00EFh)
LCDC address area	LCDCDADEF	Page start: 0	P1, P2 (0000h)
		Column start: 0	P3, P4 (0000h)
		Page end: 239	P5, P6 (00EFh)
		Column end: 319	P7, P8 (013Fh)
Memory address control	MADCTL MADDEF	LCD readout: Top to bottom Common scan direction: Top to bottom RGB layout: RGB VRAM scan direction: Horizontal Horizontal address-0 position: Left edge Vertical address-0 position: Top edge	MADCTL P1 (00h) MADDEF P1 (00h)
Color mode	COLMOD	16.8M colors	P1 (07h)
Interface mode	IFMOD	8-bit interface	P1 (00h)
LCDC	LCDCIF	Disabled * During parallel interface	P1 (00h)
External VSYNC synchronization	VSYNCIN / VSYNCOUT	Internally synchronized	VSYNCOUT
	EXVSYNCDEF	Correction for display scan start: 0H	P1 (00h)
TE signal output	TEON / TEOFF	Turned off	TEOFF
Gamma set	GAMSET	Gamma curve: GC0	P1 (01h)

Function	Related command	Default value	
Power control	PWRDEF	Source-driver bias: Power save Soft start: Available 1st-to-4th booster circuits: Normal operation	P1 (2Fh)
		3rd-to-4th booster CLK: 1H × 1 1st-to-2nd booster CLK: 1H × 1	P2 (1Bh)
		Regulator operation: Normal operation Reference power-supply bias current: 10B Reference power-supply setting: Work-function difference + Vth	P3 (F9h)
		Regulator on: All turned on	P4 (FFh)
		V_{COMH} adjustment: Internal circuit V_{COML} drive capacity: Normal V_{COML} low power: Normal V_{COML} phase compensation: Connected V_{COMH} drive capacity: Normal V_{COMH} low power: Normal V_{COMH} phase compensation: Connected	P5 (00h)
		Regulator on: Normal operation	P6 (00h)
		V_{OFREG} capacity-up interval: 0	P7 (00h)
		V_{COMH} capacity-up interval: 0	P8 (00h)
		V_{COML} capacity-up interval: 0	P9 (00h)
		1st-to-2nd booster wait time: 0	P10 (00h)
		Regulator-on wait time: 0	P11 (00h)
		3rd-to-4th booster stabilization time: 0	P12 (00h)
Settings of the internal power supply	EVRSET	V_{LDO} = 2.0 V 1st booster: × 2 V_{LDO}: Operating	P1 (01h)
		V_{DDHS} output voltage	P2 (1Ah)
		V_{COMH} output voltage	P3 (28h)
		V_{COMW} output voltage	P4 (0Fh)
		V_{DDRH} output voltage	P5 (15h)
		V_{ONREG} output voltage	P6 (15h)
		V_{OFREG} output voltage	P7 (06h)

Function	Related command	Default value	
Display control	DISCTL	Vertical back porch: 5 lines	P1 (05h)
		Number of display lines: 240 lines	P2,P3 (F0h)
		Vertical front porch: 4 lines	P4 (04h)
		1H period: 65 clocks	P5 (41h)
		Drive mode: 0	P6 (00h)
		Source prebuffer on: 15	P7 (0Fh)
		Source prebuffer off: 35	P8 (23h)
		Source correction on: 36	P9 (24h)
		Source correction off: 46	P10 (2Eh)
		DAC drive on: 47	P11 (2Fh)
		DAC drive off: 55	P12 (37h)
		Gate on: 3	P13 (03h)
		Gate off: 54	P14 (36h)
		Gamma off: 56	P15 (38h)
		Alternating drive: Line inversion FRC adder stop Number of line inversions: 0 Normally white LCD	P16 (0Ah)
		Damping resistance: 30 kΩ Source driver: Normal drive	P17 (80h)
		Partial non-display area: Normal drive Partial non-display-area V_{COM}: Normal drive Partial non-display-area refresh rate: 0	P18 (00h)
		Clock division raite during idle display: 1/1	P19 (01h)
		VFP addition during idele display: 8 lines	P20 (08h)

◇ Output/input pins

Signal	State
D7-D0	High impedance (P/S="HIGH") Input (P/S="LOW")
D23-D8	High impedance
BRST, BCK, BDATA, POFF	"LOW" Output
TE	"LOW" Output
$\overline{VSO}$, $\overline{HSO}$	"HIGH" Output
SOn	"V_{DDRL}" Output
GOn	"V_{EE}" Output
TS8-TS0	High impedance

8-5. LCD Drive Control Circuit

Gradation is expressed by controlling the gray scale voltages that are generated based on the gray scale data written into the video memory. However, the gray scale voltages are generated for only 64 gray scale levels out of the 256 shades of gray. Accordingly, the 6 high-order bits of data comprising each element of the display data are used to generate the gray scale voltages. The gray scale expression for the 2 low-order bits of the display data is achieved by FRC control. Therefore, the 256 shades of gray are expressed through the combined use of gray-scale-voltage control and FRC control.

The frame-inversion and line-inversion methods have been adopted for LCD drives.

8-5-1. 64-Gray-scale-level 2-Bit FRC Drive

This drive method uses the 6 high-order bits of data comprising each element of the display data to generate the 64-gray-scale-level voltages and the 2 low-order bits of display data in order to drive the FRC, thereby expressing the 256 shades of gray.

As the 2 low-order bits for driving the FRC are expressed in 4-frame units, for a given gray scale level of a given pixel to be expressed it is necessary that the pixel be displayed with the same gray scale level for a 4-frame period.

The FRC patterns are available in 4 display pixel $\times$ 4 display line = 16 patterns, which are switched over every frame. These FRC patterns are provided for each element of R, G, and B individually.

The 64-gray-scale-level 2-bit FRC drive is used only for the lines being displayed in 256 shades of gray. Therefore, this drive is not used for non-display lines in offline or partial mode, or during 2-gray-scale-level display.

◇

8-6. Address Control Circuit and Video Memory

The S1D19122 contains video memory (VRAM) in which the display data is stored, so that the data displayed on the LCD is always the data stored in the VRAM. Therefore, the data to be displayed on the LCD must be stored in (written to) the VRAM before being displayed.

When the VRAM is accessed from the MPU, and when the content of the VRAM is read out for display on the LCD, the driver exercises address control.

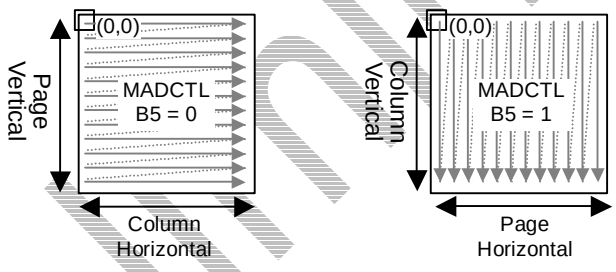
The driver has dedicated address pointers for the MPU and the Display, which move according to the operation of the MPU and the Display, respectively.

8-6-1. VRAM Access Scan Direction and VRAM Address Mapping

The VRAM address map is provided for 320 pixels × 240 lines. VRAM read/write is performed in pixel (RGB) units, with one pixel mapped to one address. Therefore, the internal VRAM consists of 240 addresses in the vertical direction and 320 addresses in the horizontal direction.

Specification of the VRAM access scan direction (MADCTL: B5) refers to specifying an access scan direction with respect to the physical position of the VRAM. The page and column definitions for the vertical and horizontal addresses of the physical VRAM location vary depending on the VRAM access scan direction. Caution is also required because the maximum value of the area in which pages and columns can be set changes depending on the VRAM access scan direction. The commands to which this applies include CASET, PASET, and LCDCDADEF. Be aware also that the Display address does not depend on the VRAM access scan direction, and is always mapped in the same direction as the vertical addresses.

Internal address	VRAM access scan direction		Address area	
	Horizontal direction	Vertical direction	Min.	Max.
Vertical address	page	column	0	239
Horizontal address	column	page	0	319



* This is for the cases in which address 0 is located at the upper left corner.

If the VRAM access scan direction is set to vertical, tearing effects cannot be avoided.
Refer to Section 8-17-4, “Conditions under Which the Tearing Effect Cannot be Avoided.”

8-6-2. Address Pointers

◇ MPU address pointer

When the MPU accesses the VRAM, the address pointer is controlled for the performance of matrix mapping. Therefore, the MPU address pointer is expressed in two dimensions (page address ‘n’ and column address ‘m’).
The MPU address pointer moves within the VRAM access area. The VRAM access area of the MPU is set using the CASET or PASET command.
The MPU address pointer is moved to the start address (start page, start column) of the VRAM access area using the RAMWR, RAMRD, or NOP command. While the VRAM is accessed for read or write, the MPU address pointer is incremented by one address in the column direction according to the display-data format used. When the MPU address pointer has reached the end column address, it is returned to the start address in the column direction and incremented by one address in the page direction. When the MPU address pointer has reached the last address (end page, end column), it is returns to the start address.

◇ LCDC address pointer

When the LCDC writes display data to the VRAM, the address pointer is controlled for the performance of matrix mapping. Therefore, the LCDC address pointer is expressed in two dimensions (page address ‘n’ and column address ‘m’).
The LCDC address pointer moves within the VRAM access area. The VRAM access area of the LCDC is set using the LCDCDADEF command.
The LCDC address pointer is moved to the start address (start page, start column) of the VRAM access area by VS, and, during HDISP, the LCDC address pointer is incremented by one address in the column direction according to the display-data format used. The LCDC address pointer is returned to the start address in the column direction and incremented by one address in the page direction by HS during VDISP. Even when the LCDC interface is disabled (LCDC in the background), the LCDC address pointer in the page direction is incremented according to the above conditions.

Refer to Section 8-2-2, “LCDC Interface.”

◇ Display address pointer

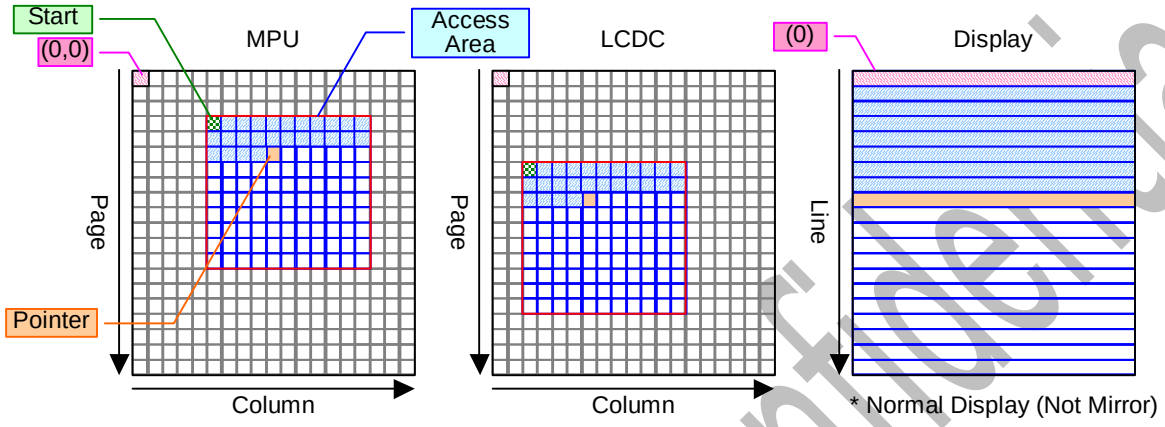
When the content of the video memory is read out for display on the LCD, the address pointer is controlled for the performance of line mapping. Therefore, the display address pointer is expressed by line address ‘n.’ The VRAM readout for display consists of mono-dimensional address mapping, as the display data is read out every line.

The display address pointer is moved as the display scan progresses. Except in the case of partial or scroll display, the pointer is incremented by one address each time the display line moves, from address 0 to the address determined by the number of display lines –1.

Refer to Section 8-9-3, “Address-0 Position and VRAM Access Scan Direction.”

Refer to Section 8-9-4, “LCD Readout Scan Direction and Gate Scan Direction.”

Refer to Section 8-9-5, “Partial/Scroll Areas and Scan Direction.”



Always make sure the VRAM access area start column (page) and end column (page) are set in pairs. The MPU and LCDC address pointers are incremented in two dimensions. Therefore, do not reverse the relative magnitudes of the start column (page) and end column (page) that have been set. Otherwise, an area may be accessed unintentionally.

The driver has a dedicated address pointer for the MPU, LCDC, and Display, respectively. The address pointers are moved independently of each other.

8-6-3. Video Memory

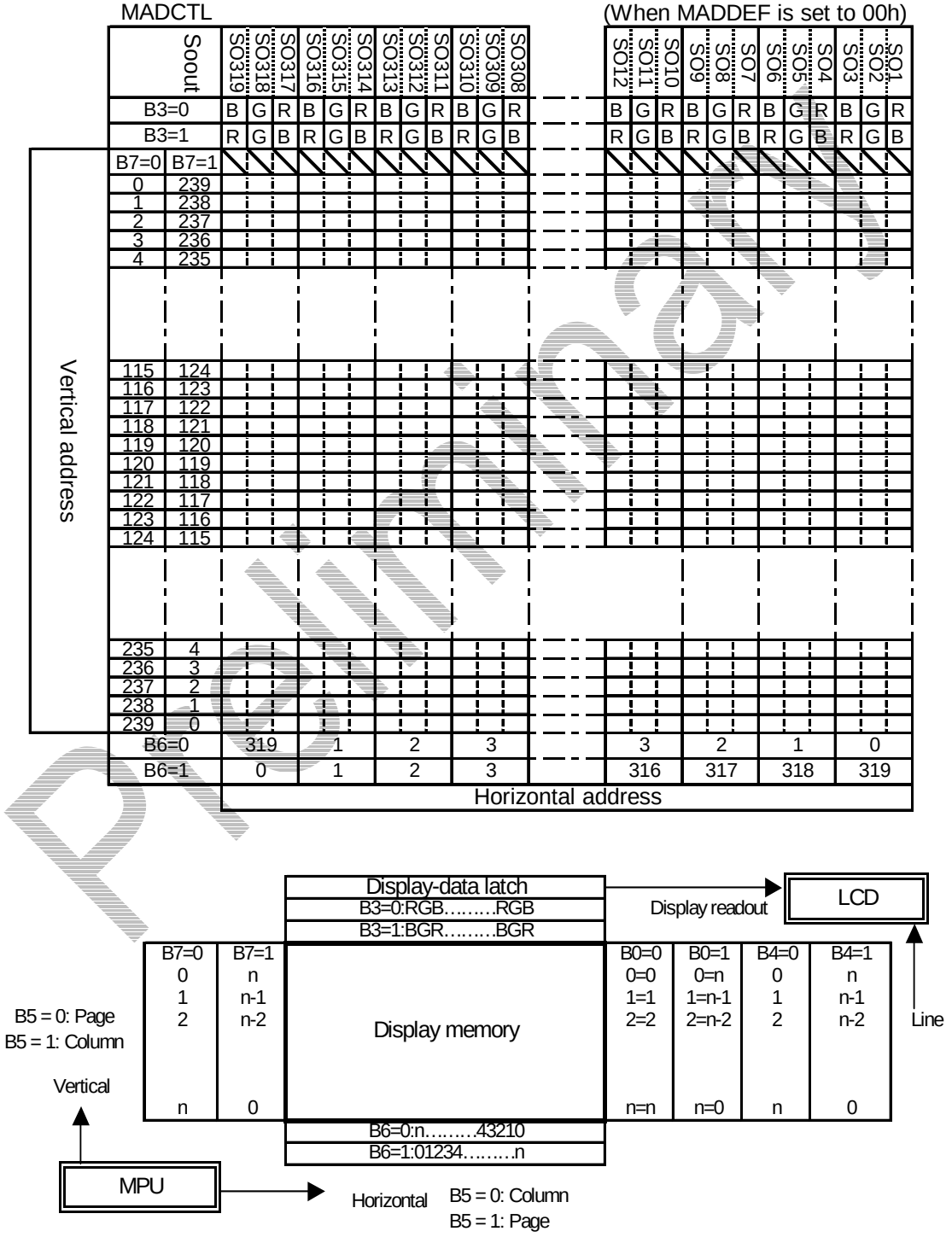
The video memory (Video-RAM or VRAM) is RAM in which the driver stores the pixel data used for display. It is configured in 320 × 240 × 24 bits. Any location in it can be selected by specifying a page address and column address.

Read/write to the video memory from the MPU side is performed via the I/O buffer circuit, and readout from the video memory for the LCD drive is controlled by a circuit in a separate block.

For moving-picture display, caution is required to ensure that the display image write frame and the display scan cycle will not become out of sync. For this reason, a display-data rewrite method synchronized with display timing (TE or DY output) is recommended.

Refer to Section 8-17, “Solutions for Moving-Picture Display.”

◇ Memory mapping



8-7. Display On/Off Function

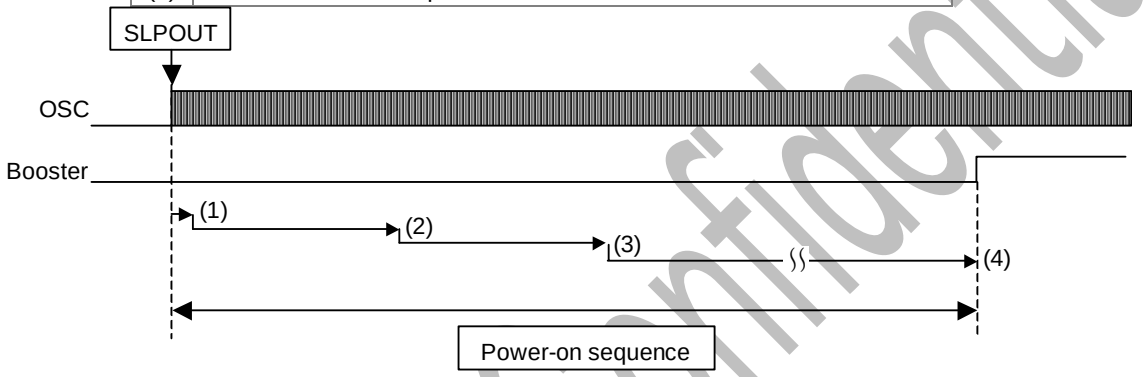
To turn on the LCD display, it is necessary to input the SLPOUT and DISON commands. (In this case, duty settings, internal power-supply on/off sequence settings, and the like are not included.)

The display can be turned on or off in various sequences depending on the timing with which SLPOUT and DISON are input.

8-7-1. Power-On Sequence

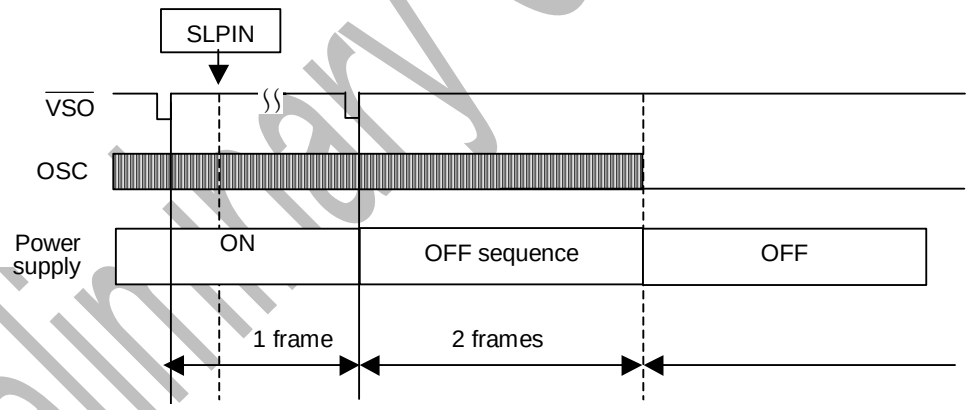
When the SLPOUT command is issued, a power-on sequence is automatically executed according to the PWRDEF settings. After the power-on sequence is executed, the booster flag is set HIGH internally in the IC. The state of the booster flag (power-supply stabilization time) can be monitored by checking B31 of RDDST or B4 of STREAD2.

	Power-on sequence
-	1st-booster reference voltage on (SLPOUT)
(1)	1st/2nd-booster start timing
(2)	Regulator startup timing
(3)	3rd/4th-booster start timing
(4)	Booster stabilization period



8-7-2. Power-Off Sequence

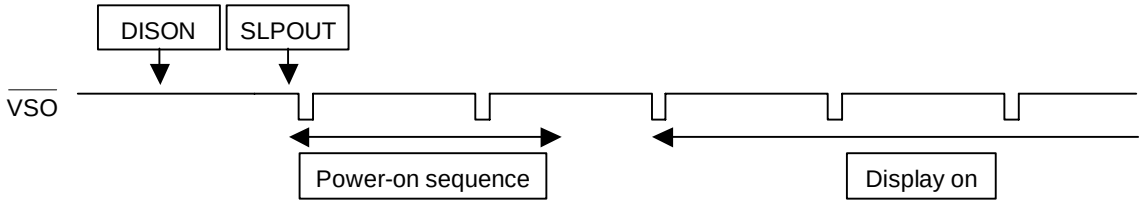
When the SLPIN command is issued, a power-off sequence is automatically executed synchronously with the next frame.



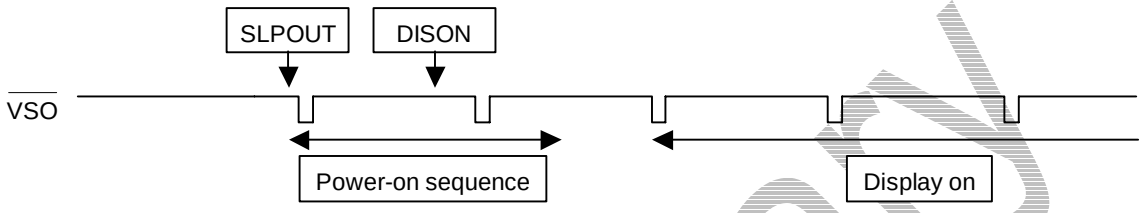
8-7-3. Display-On Sequence

The display-on sequence behaves differently depending on the order in which the DISON and SLPOUT commands are input.

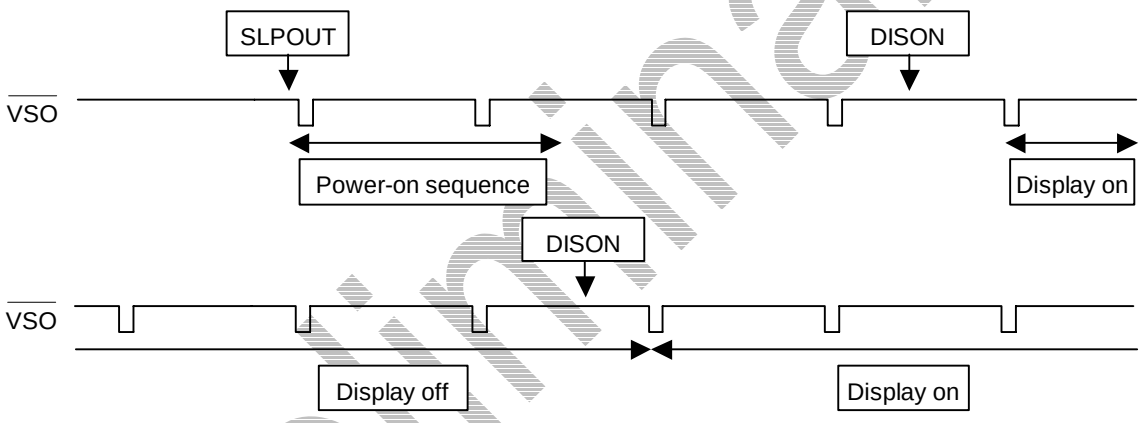
When the commands are input in order of DISON and SLPOUT, display is automatically turned on synchronously with the next frame after the power-on sequence.



When the commands are input in order of SLPOUT and DISON, the driver is placed in a sleep-out state after SLPOUT is input. If DISON is input during the power-on sequence after SLPOUT was input, a length of time is waited until the power supply outputs a stable voltage (power supply stabilization period after SLPOUT), and the display is then turned on synchronously with the next frame.

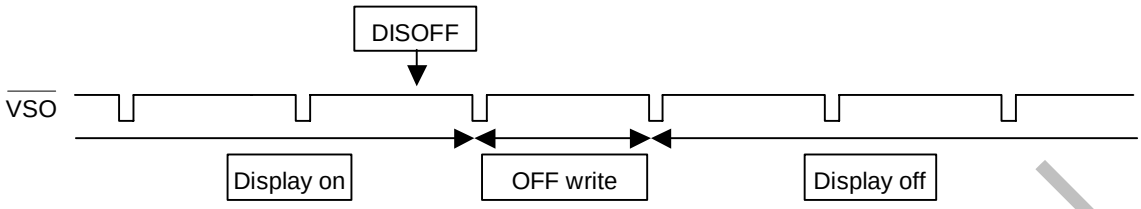


If DISON is input while the power supply is stabilizing, the display is turned on synchronously with the next frame.

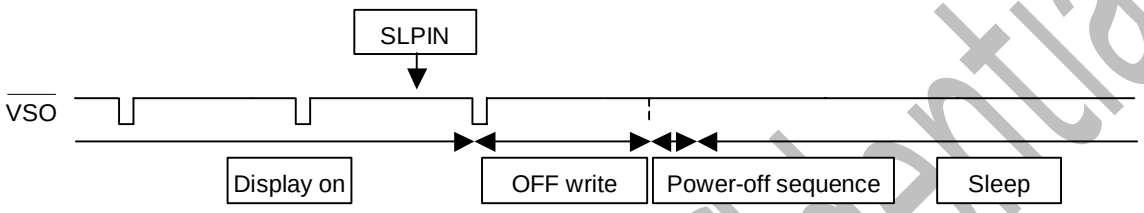


8-7-4. Display-Off Sequence

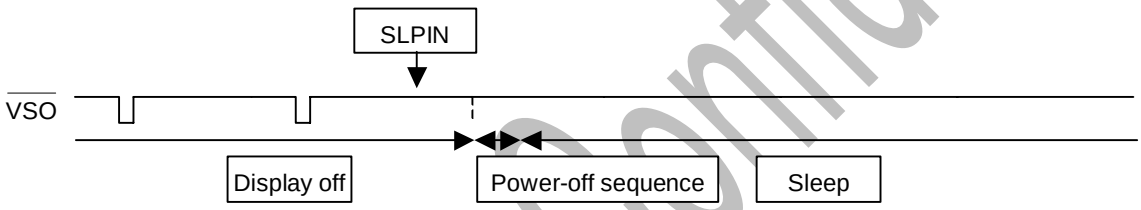
If the DISOFF command is input while the display is on, OFF data is written into the LCD for a 1-frame period synchronously with the next frame, thereby turning the display off. The driver operation at this time is such that it places all source outputs in the high-impedance state after outputting OFF data for a duration of one frame. In addition, the gate and V_{COM} outputs are turned off after operating normally for a duration of one frame. The driver state in this case is the same as in a sleep-out state.



If the SLPIN command is input while the display is on, a display-off sequence (OFF write) is performed and then a power-off sequence is executed, causing the oscillator circuit to stop oscillating. After oscillation has stopped, the LCD module enters a sleep-in state.



If the SLPIN command is input while the display is off (in sleep-out state), a power-off sequence is executed synchronously with the next frame and then the oscillator circuit stops oscillating, with the LCD module in a sleep-in state.



8-8. Display-Mode Switching Function

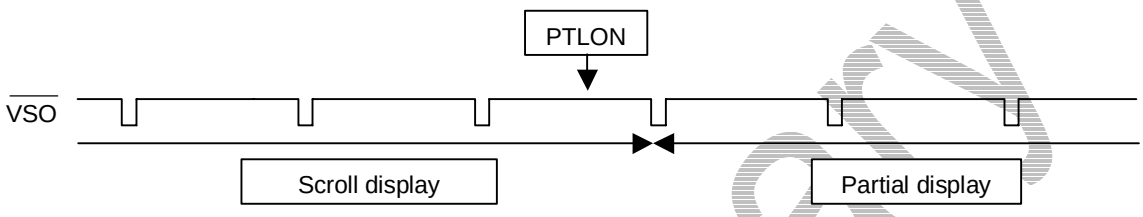
There are various display modes available for setting, as shown below. These display modes can be switched over by entering a command.

	256-gray-scale-level display (IDMOFF)		2-gray-scale-level display (IDMON)	
A	Normal display	NORON	Normal display	NORON
B	Partial display	PTLON	Partial display	PTLON
C	Scroll display	VSCRSADD	Scroll display	VSCRSADD
D	Partial + scroll display	PTLON + VSCRSADD	Partial + scroll display	PTLON + VSCRSADD

8-8-1. Display-Mode Switchover Timing

When display modes are changed by entering a command, the new display mode specified by a command is entered beginning with the next frame. However, when changing between a 256-gray-scale-level display mode and a 2-gray-scale-level display mode, a length of time equal to the oscillator circuit stabilization period (2 frames) is waited before the new display mode is applied.

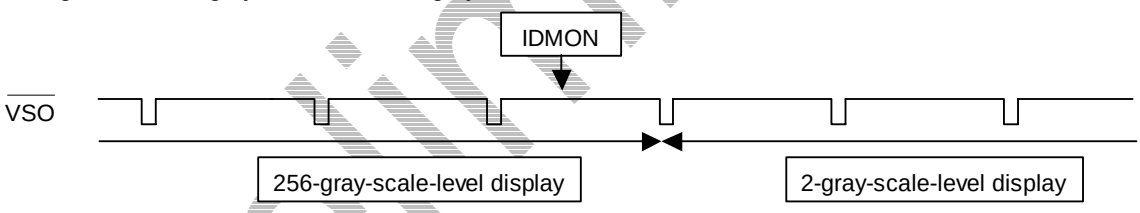
Shown below is a case in which display modes are changed from “scroll display (C)” to “partial display (B).”



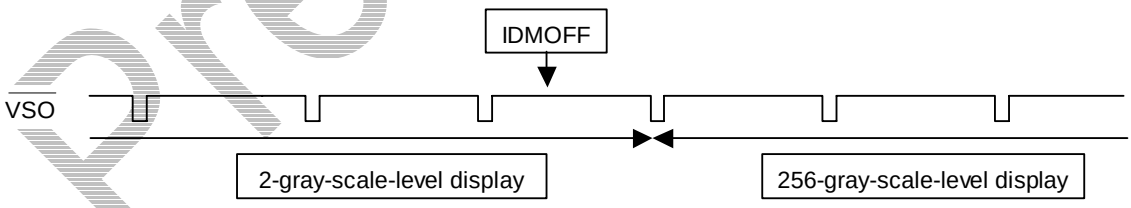
8-8-2. Display Gray-Scale-Level Switchover Timing

When display modes are changed between 256-gray-scale-level display and 2-gray-scale-level display, the new display mode (either 2- or 256-gray-scale-level) is entered beginning with the next frame after the IDMON (IDMOFF) command is input.

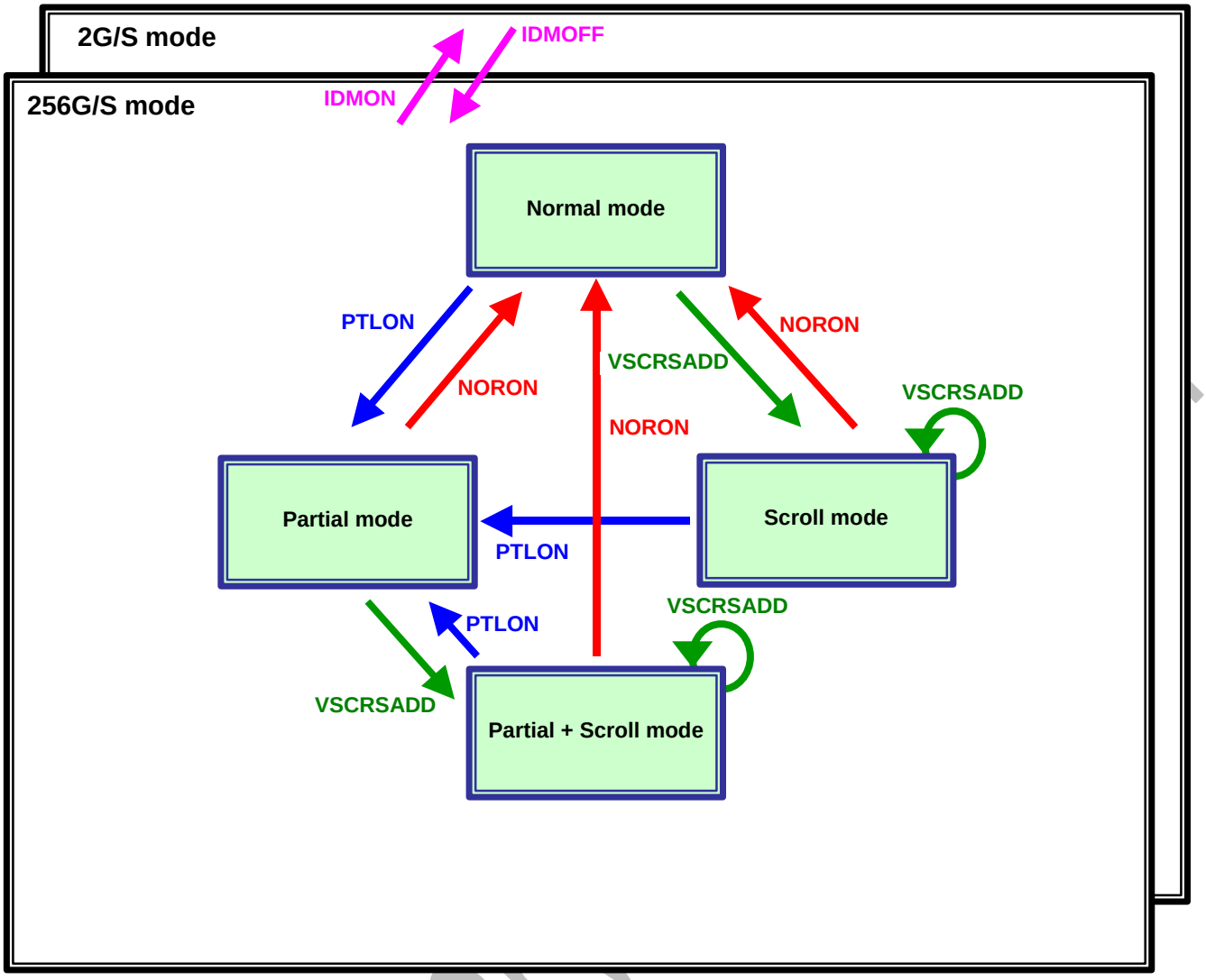
◇ When changed from 256-gray-scale-level to 2-gray-scale-level



◇ When changed from 2-gray-scale-level to 256-gray-scale-level



8-8-3. Display-Mode Transition Diagram



The commands in the above diagram and the commands SLPIN, SLPOUT, DISOFF, and DISON require caution. Issuing these commands together within the command operation period shown in 9-1 is prohibited.

8-9. Command Definition Independent of the IC Mount Position

Depending on how the MADDEF command is set, the top-bottom/left-right definitions in the MADCTL command are changed internally in the IC to suit the mounted form of the IC. This enables memory access control independent of the mounted IC position.

8-9-1. A Model LCD Module for the S1D19122

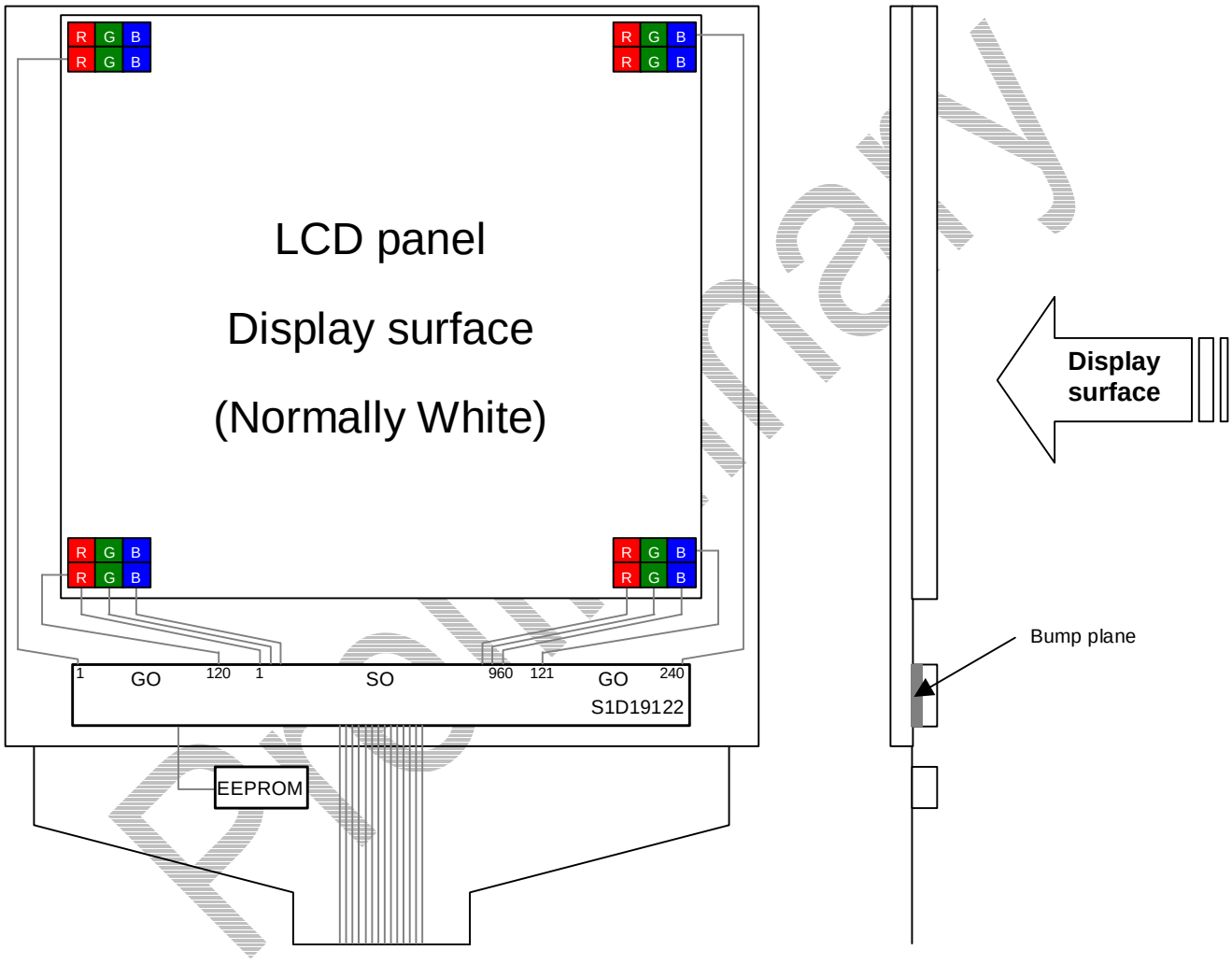
Shown below is a model LCD module for the S1D19122. The top-bottom/left-right positions defined in this development specification, as well as the RGB filter arrangement, white or black background, and the like described in it, are in accordance with the diagram shown below.

Top view

Viewed from the display surface (below the bump plane)

Side view

Viewed from the left side
(left of the bump plane)



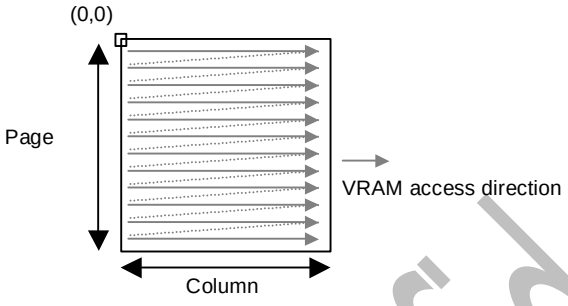
8-9-2. Position Definitions by IC Mount Position

The set value of MADCTL actually used internally in the IC changes depending on how MADDEF is set.

The arithmetic operation shown below is performed on each bit. (The letter 'n' in the table denotes the nth bit.)

MADCTL (Bn)	MADDEF (Bn)	IC internal set value
0	0	0
0	1	1
1	0	1
1	1	0

The following shows the set values of MADDEF for the case in which MADCTL is set to "00h" that will result in a memory access direction on the LCD panel like those shown below, separately for each IC mount position.

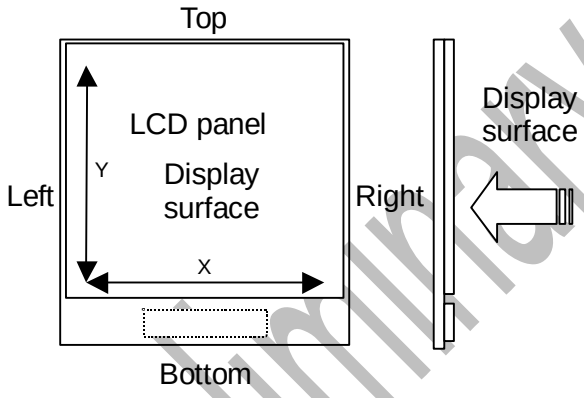


The explanation given here is based on Section 8-9-1, "A Model LCD Module for the S1D19122." Therefore, if the color-filter arrangement differs from that of the model, B3 of MADDEF must be set to 1.

The top-bottom/left-right relationship shown below applies. (The non-bump plane is the surface.)

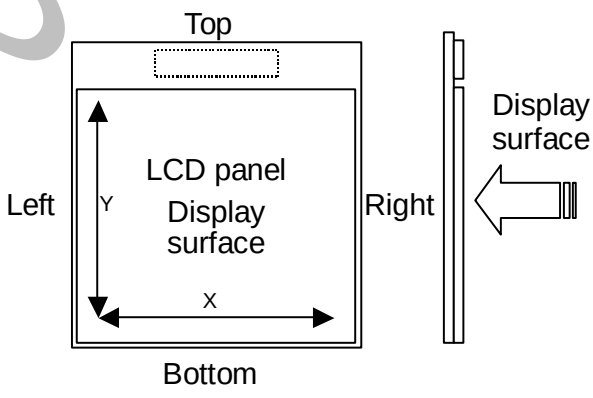
If left-mounted or right-mounted, be aware that, due to the device structure, the VRAM-to-LCD readout direction and gate scan direction should be set left-right rather than top-bottom.

◇ When bottom-mounted



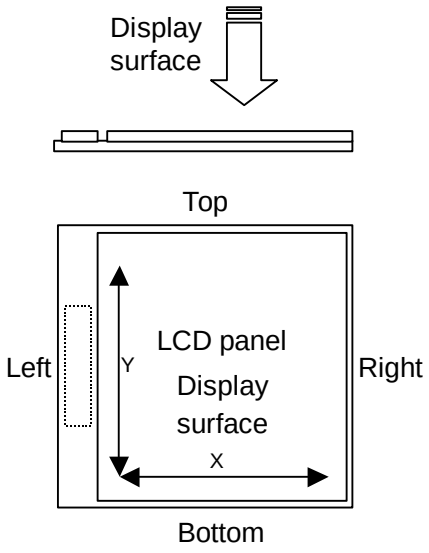
MADDEF (00h)	
VRAM address (0,0) position	Upper left
VRAM access direction	Column direction
Column	X direction
Page	Y direction
VRAM-to-LCD readout direction	Top to bottom
Gate scan direction	Top to bottom

◇ When top-mounted



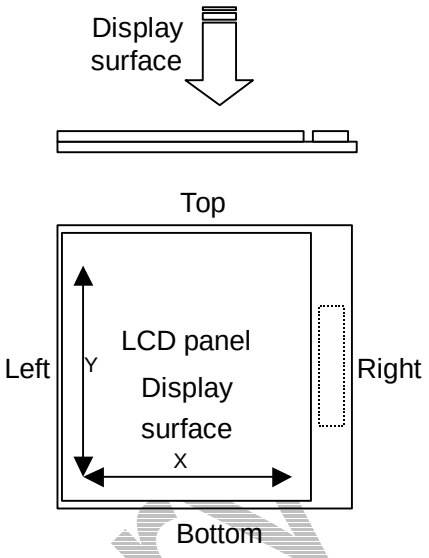
MADDEF (D0h)	
VRAM address (0,0) position	Upper left
VRAM access direction	Column direction
Column	X direction
Page	Y direction
VRAM-to-LCD readout direction	Top to bottom
Gate scan direction	Top to bottom

◇ When left-mounted



MADDEF (A0h)	
VRAM address (0,0) position	Upper left
VRAM access direction	Column direction
Column	X direction
Page	Y direction
VRAM-to-LCD readout direction	Right to left
Gate scan direction	Right to left

◇ When right-mounted



MADDEF (60h)	
VRAM address (0,0) position	Upper left
VRAM access direction	Column direction
Column	X direction
Page	Y direction
VRAM-to-LCD readout direction	Left to right
Gate scan direction	Left to right

8-9-3. Address-0 Position and VRAM Access Scan Direction

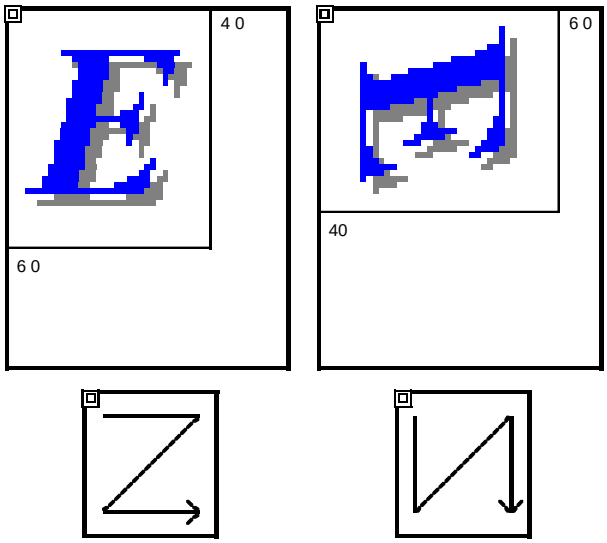
Refer to MADCTL (MADDEF = 00h).

VRAM image = Display image (When B0 = 0)

Memory Address (0, 0)

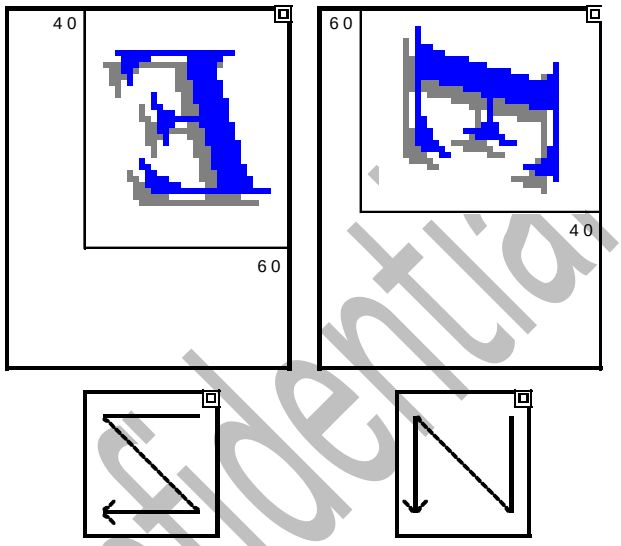
(B7, B6)=(0, 0)

B5=0 B5=1

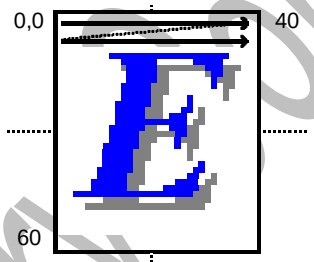


(B7, B6)=(0, 1)

B5=0 B5=1



HOST



B5 : RAM scan direction(Host to RAM)

B5 = 0

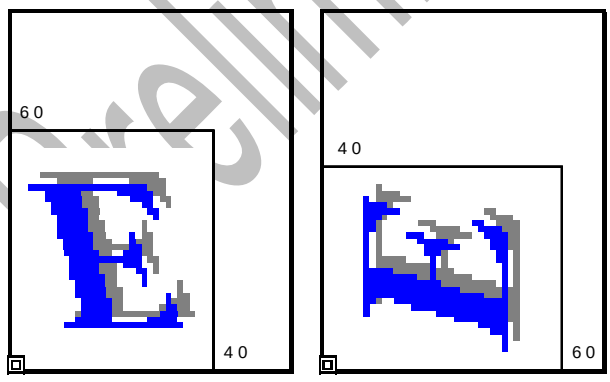
	HOST	DrIC
Increment direction	Page	Vertical
	Column	Horizontal

B5 = 1

	HOST	DrIC
Increment direction	Page	Horizontal
	Column	Vertical

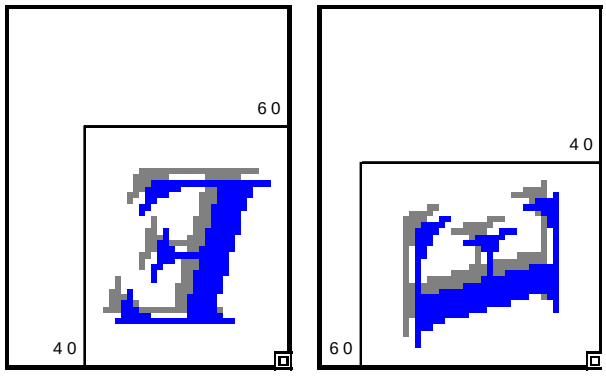
(B7, B6)=(1, 0)

B5=0 B5=1



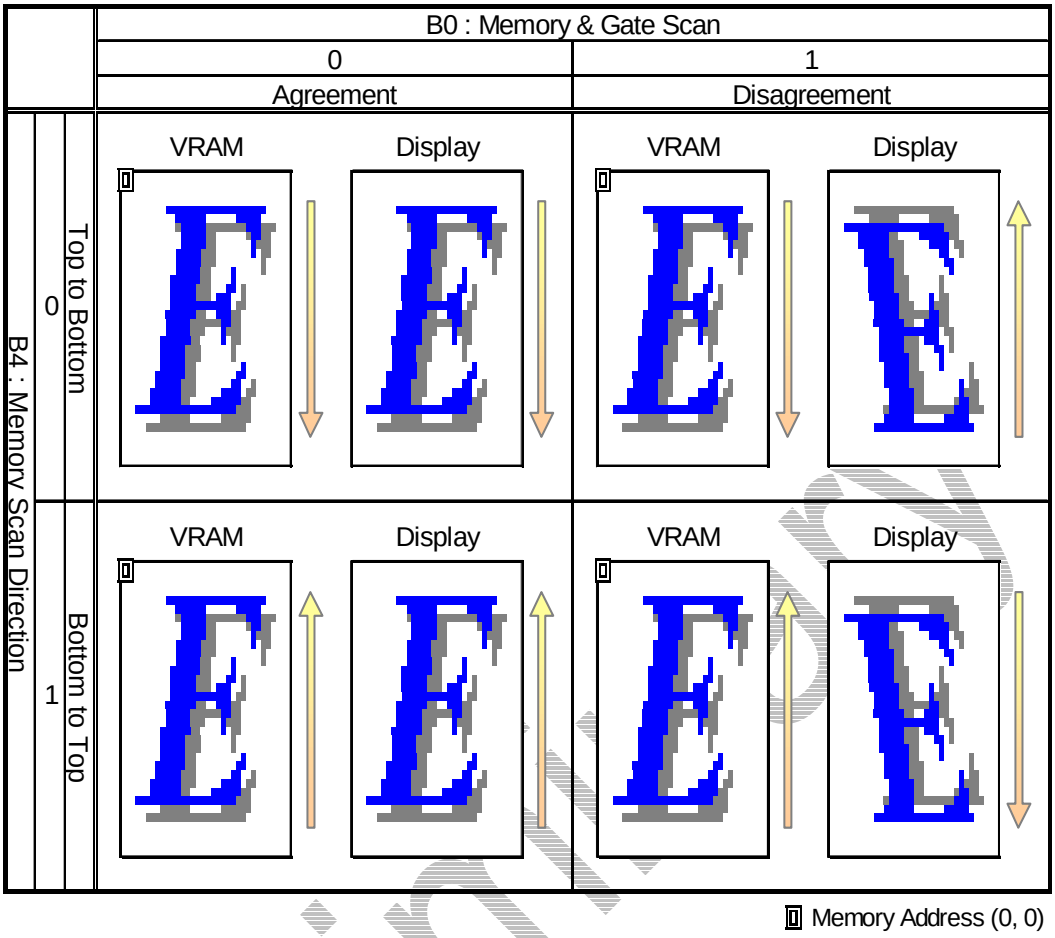
(B7, B6)=(1, 1)

B5=0 B5=1



8-9-4. LCD Readout Scan Direction and Gate Scan Direction

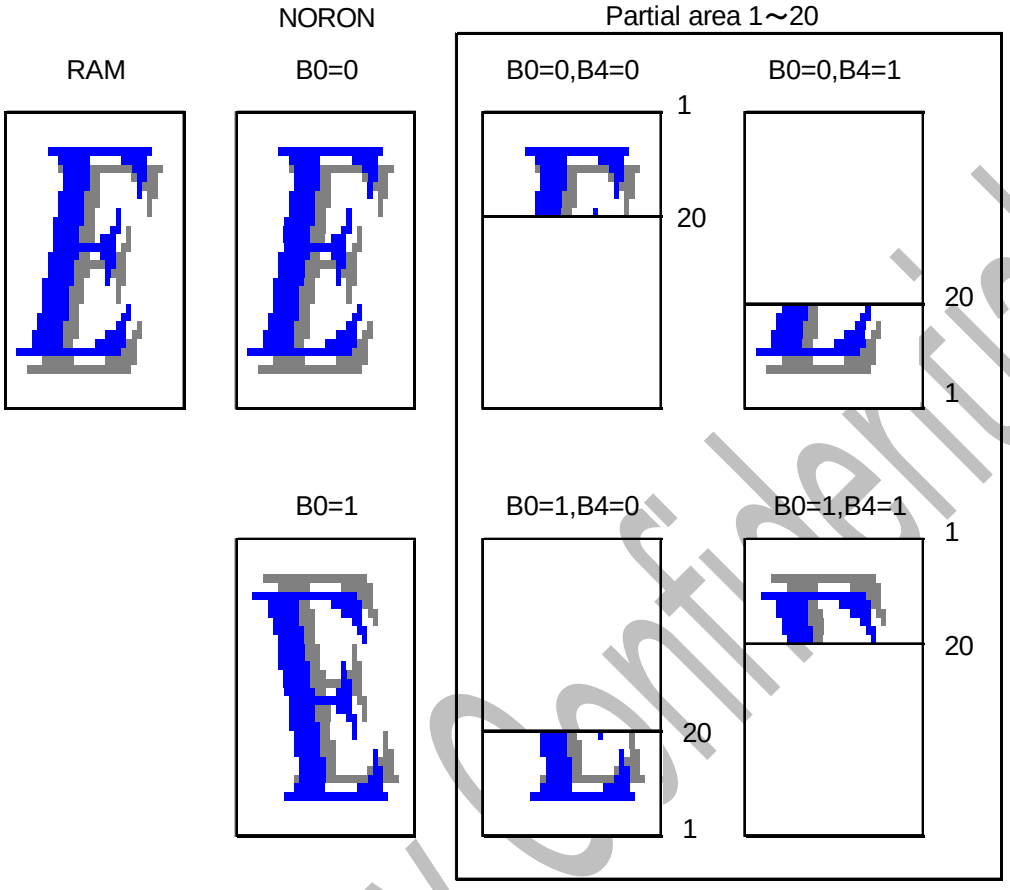
Refer to MADCTL (MADDEF = 00h).



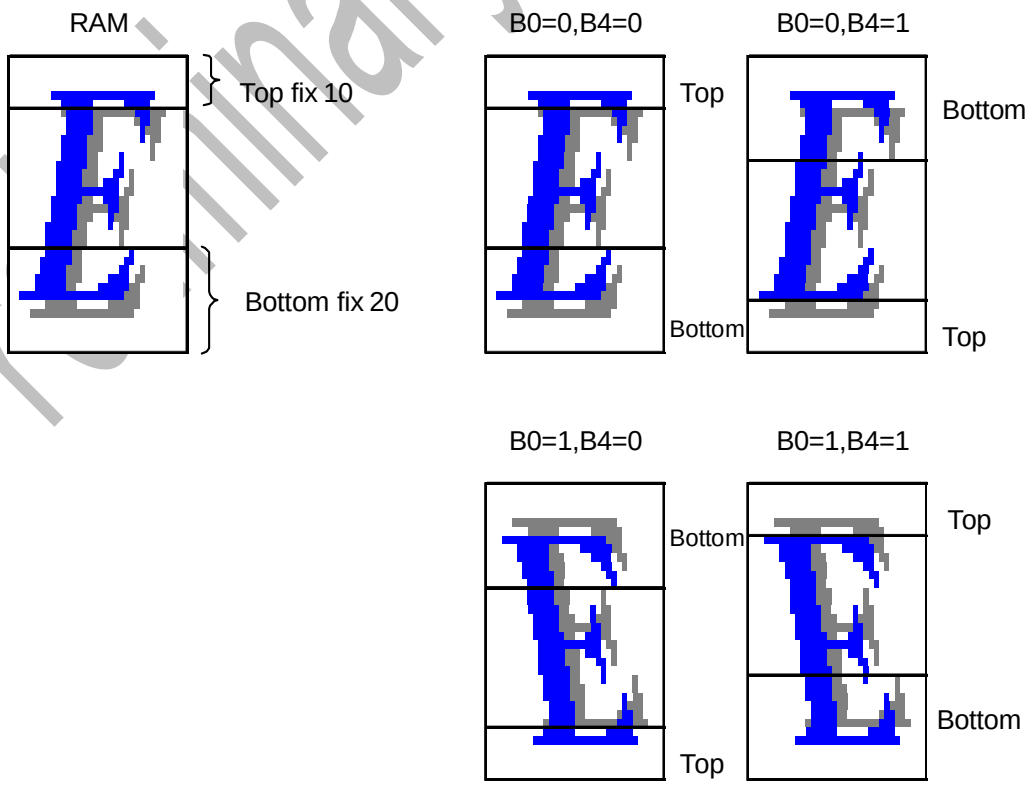
8-9-5. Partial/Scroll Areas and Scan Direction

Refer to MADCTL, PTLAR, and VSCRDEF (MADDEF = 00h).

◇Partial mode



◇Scroll mode



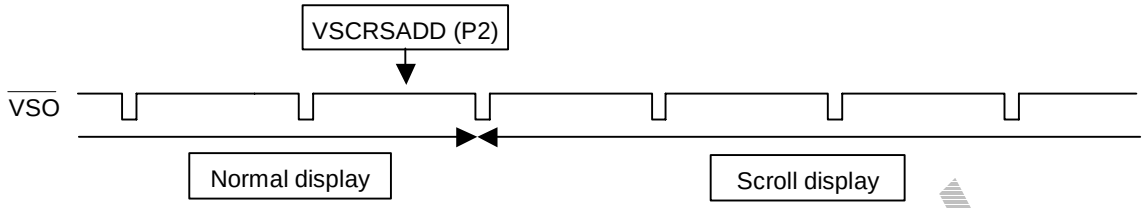
8-10. Area Scroll Display Function

The VSCRDEF command permits an area scroll region (top fixed lines, scroll memory, and bottom fixed lines) to be set, allowing the display screen to be partially scrolled.

8-10-1. Scroll Display Sequence

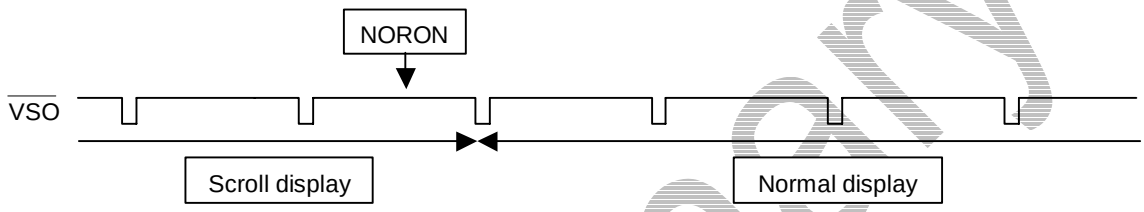
Scroll display mode is entered in the manner shown below.

After the scroll start address is specified using the VSCRSADD command, the scroll display mode is entered beginning with the next frame.



Normal display is entered into from scroll display in the manner shown below.

After the NORON command is input, the display mode returns to normal display synchronously with the next frame.

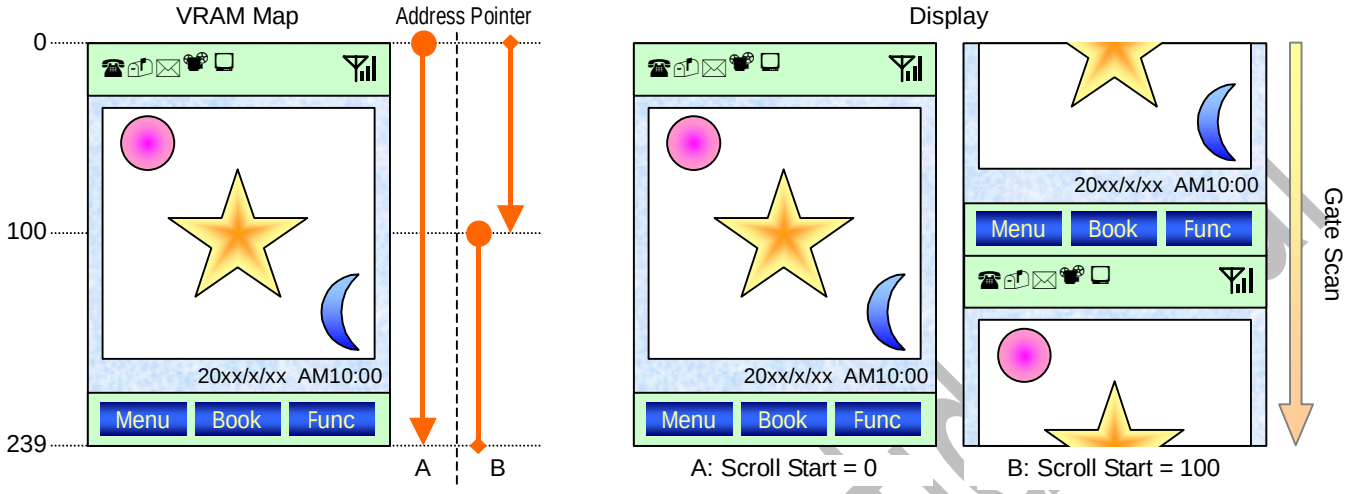


8-10-2. Full Scroll Display

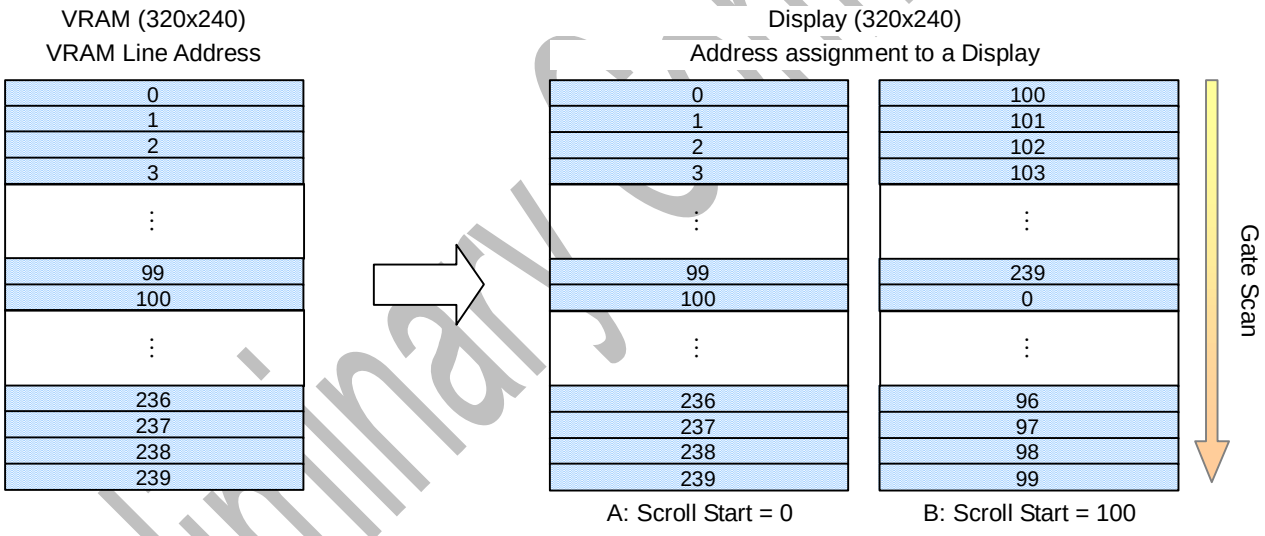
Shown below is an example in which the number of top fixed lines, the VRAM scroll area, and the number of bottom fixed lines are set to 0, 240, and 0, respectively, by the VSCRDEF command. In this example, furthermore, both VRAM readout and gate scan are performed from top to bottom (MADCTL: B4 = 0; B0 = 0).

The scroll start address must always be an address within the scroll area. Setting scroll start address outside the scroll area is prohibited.

◇ Display image



◇ Address image



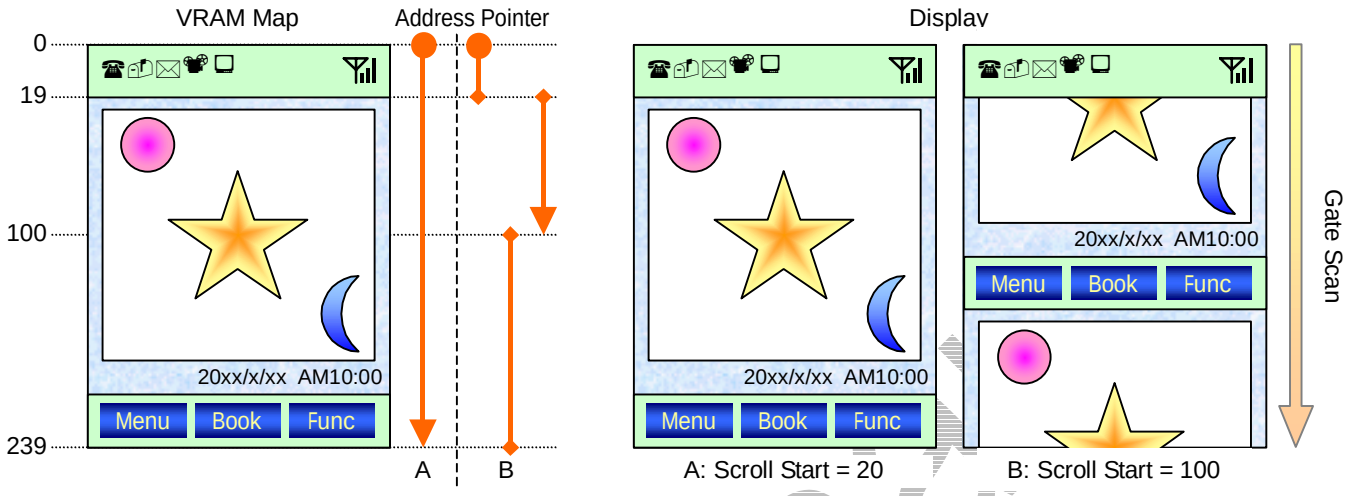
If the number of LCD display lines is smaller than the number of line addresses of the VRAM, the display is “thinned out” from the scroll area for an interval equal to the deficiency in the number of display lines.

8-10-3. Bottom Scroll Display

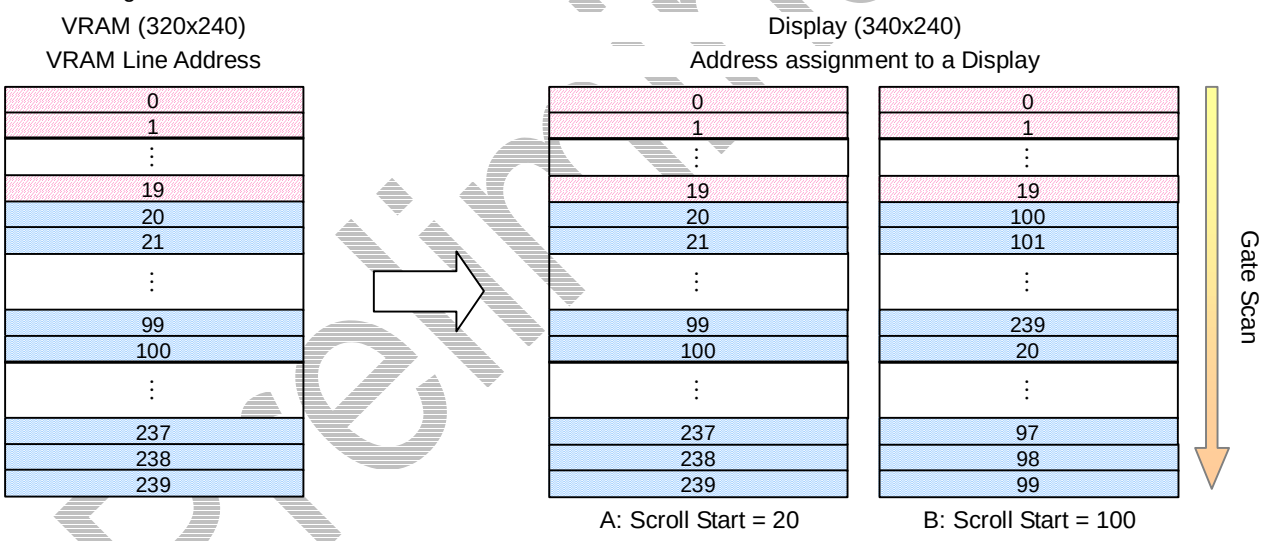
Shown below is an example in which the number of top fixed lines, the VRAM scroll area, and the number of bottom fixed lines are set to 20, 220, and 0, respectively, by the VSCRDEF command. In this example, furthermore, both VRAM readout and gate scan are performed from top to bottom (MADCTL: B4 = 0; B0 = 0).

The scroll start address must always be an address within the scroll area. Setting scroll start address outside the scroll area is prohibited.

◇ Display image



◇ Address image



The top fixed area is always calculated from the number of top fixed lines relative to address 0.

Top fixed start address = 0

Top fixed end address = 0 + (number of top fixed lines – 1)

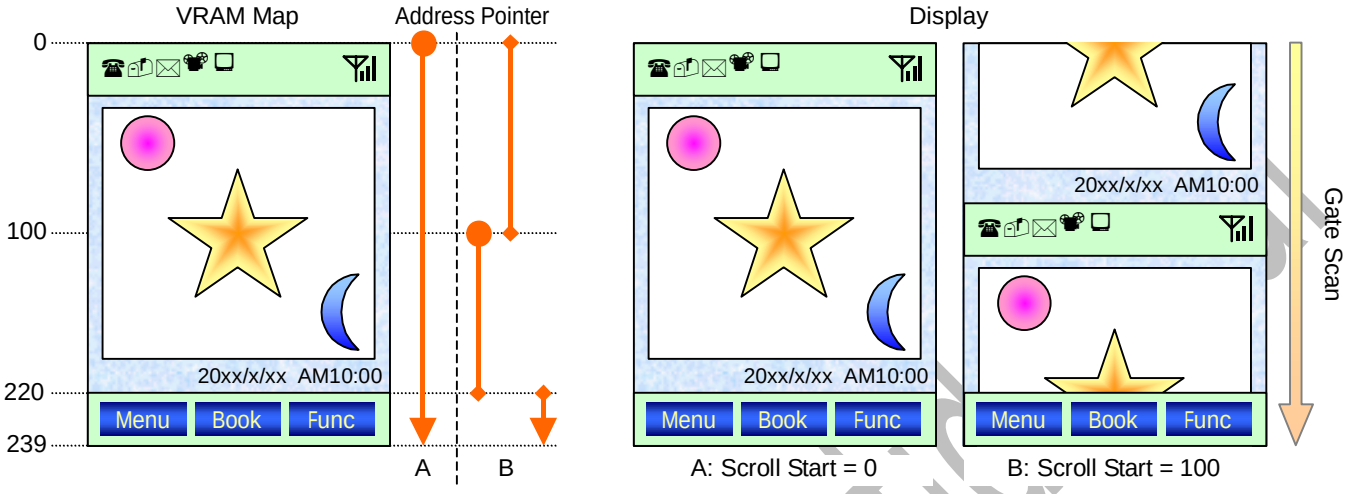
The top fixed area is always an area to be displayed. If the number of LCD display lines is smaller than the number of line addresses of the VRAM, the display is “thinned out” from the scroll area for an interval equal to the deficiency in the number of display lines.

8-10-4. Top Scroll Display

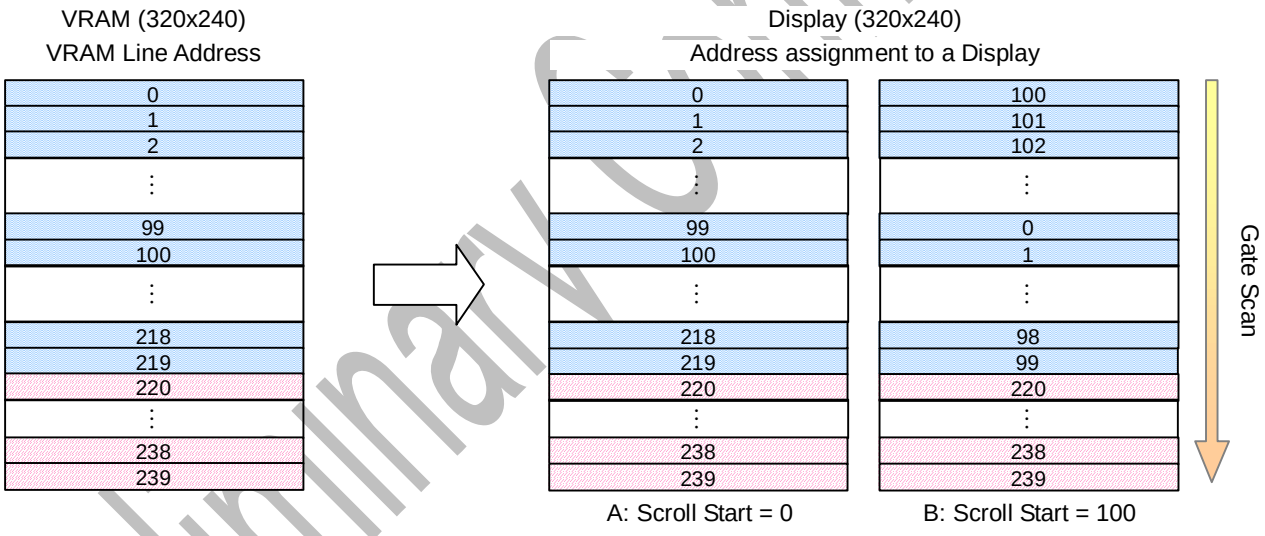
Shown below is an example in which the number of top fixed lines, the VRAM scroll area, and the number of bottom fixed lines are set to 0, 220, and 20, respectively, by the VSCRDEF command. In this example, furthermore, both VRAM readout and gate scan are performed from top to bottom (MADCTL: B4 = 0; B0 = 0).

The scroll start address must always be an address within the scroll area. Setting scroll start address outside the scroll area is prohibited.

◇ Display image



◇ Address image



The bottom fixed area is always calculated from the number of bottom fixed lines relative to address 239 (number of vertical addresses determined by RAMDIV).

Bottom fixed start address = 239 – (number of bottom fixed lines – 1)

Bottom fixed end address = 239

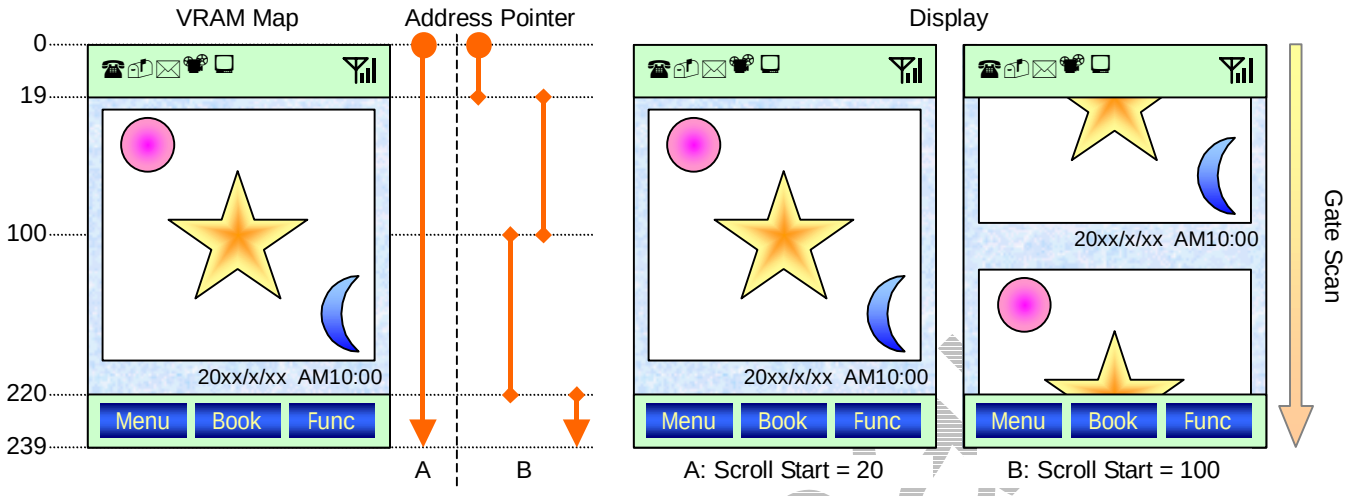
The bottom fixed area is always an area to be displayed. If the number of LCD display lines is smaller than the number of line addresses of the VRAM, the display is “thinned out” from the scroll area for an interval equal to the deficiency in the number of display lines.

8-10-5. Middle Scroll Display

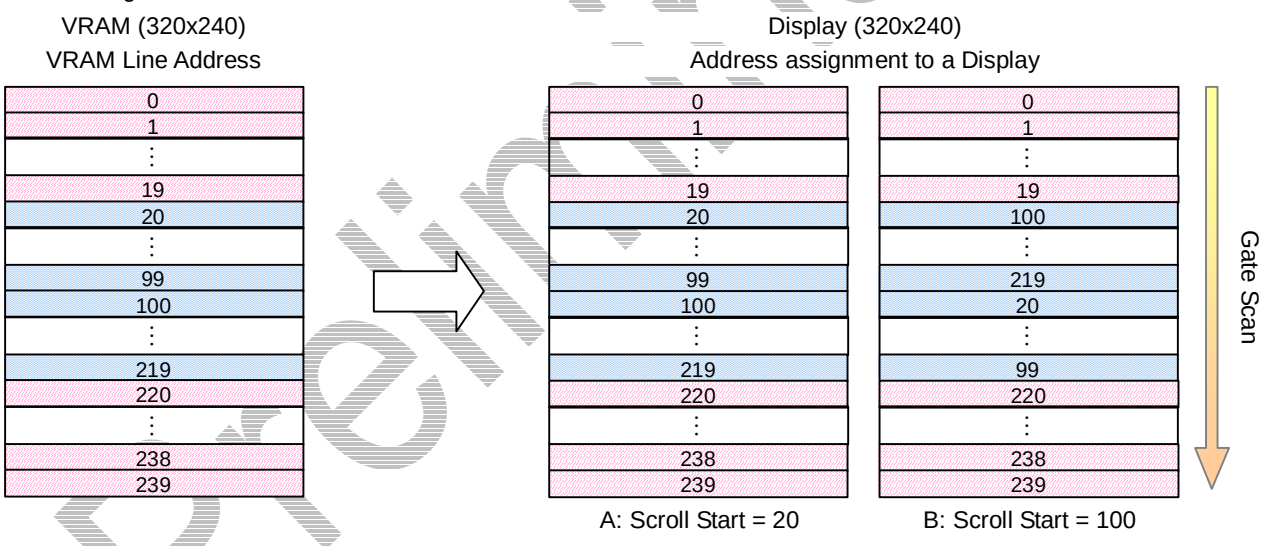
Shown below is an example in which the number of top fixed lines, the VRAM scroll area, and the number of bottom fixed lines are set to 20, 200, and 20, respectively, by the VSCRDEF command. In this example, furthermore, both VRAM readout and gate scan are performed from top to bottom (MADCTL: B4 = 0; B0 = 0).

The scroll start address must always be an address within the scroll area. Setting scroll start address outside the scroll area is prohibited.

◇ Display image



◇ Address image



The top fixed area is always calculated from the number of top fixed lines relative to address 0.

Top fixed start address = 0

Top fixed end address = 0 + (number of top fixed lines – 1)

The bottom fixed area is always calculated from the number of bottom fixed lines relative to address 239 (number of vertical addresses determined by RAMDIV).

Bottom fixed start address = 239 – (number of bottom fixed lines – 1)

Bottom fixed end address = 239

The top and bottom fixed areas are always areas to be displayed. If the number of LCD display lines is smaller than the number of line addresses of the VRAM, the display is “thinned out” from the scroll area for an interval equal to the deficiency in the number of display lines.

8-11. Partial-Display Function

Partial display of the screen is enabled by setting a partial area (start line, end line) via the PTLAR command. Because video memory readout and gate line select pulse are turned off during non-display intervals, the IC consumes less current than in full-screen display, making it ideal for use in portable equipment and the like.

8-11-1. Partial-Display Sequence

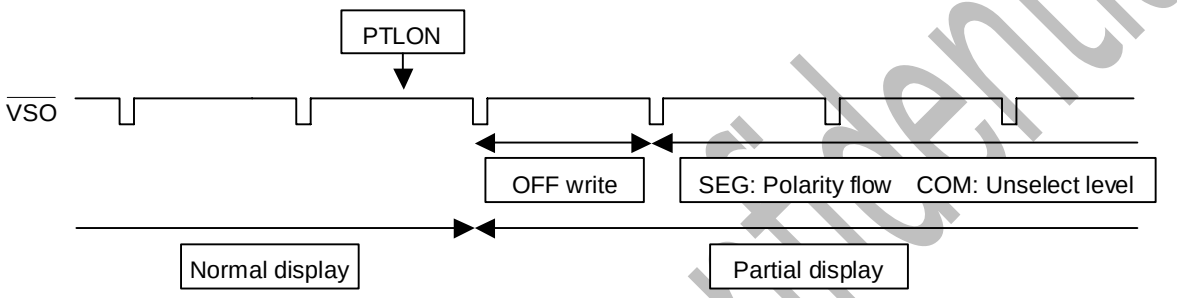
Partial display is entered as specified below.

After the PTLON command is input, the display mode enters partial display beginning with the next frame. The first frame of partial display and those that follow operate differently in a non-display area. Frame operation in a display area is the same as for normal display. The description below refers to frame operation within a non-display area.

◇ Frames following the first frame

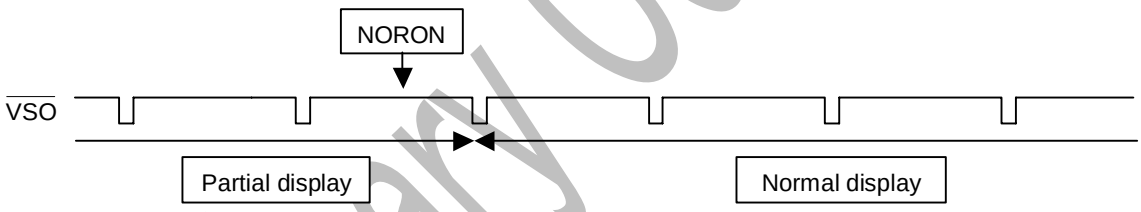
The SO output is polarity-inverted from the first frame as many times as set by DISCTL. The GO output is polarity-inverted in the same way as during normal display.

The SO output outputs a display-off gray scale voltage. VRAM readout is not performed. The GO output outputs an unselect level (VD or VS).



Normal display is entered into from partial display as specified below.

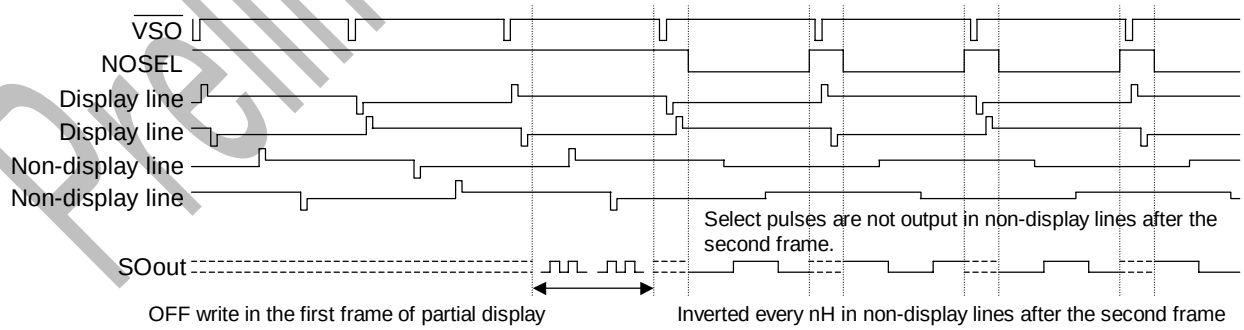
After the NORON command is input, the display mode returns to normal display synchronously with the next frame. No particular operation is involved.



8-11-2. Partial-Display State

The following shows the operation of non-display lines after the first frame of partial display:

- The gate select pulse is not output.
- The source output outputs a line-inverted waveform set by DISCTL.



8-12. Initialize Function

If the initialize function is to be used, it is necessary to set the INISEL pin HIGH and connect an EEPROM. Furthermore, the parameter values best suited for LCD display must be written into the EEPROM before the function can be used.

Two methods of refresh are available: “auto refresh” and “command refresh.” The combined use of these refresh methods is prohibited.

8-12-1. Initialize Sequences

The operation performed after a chip reset is defined as “initialize.”

The range of data in the EEPROM from address 0 to the address of RDDATM is read out. Data readout from the EEPROM is timed by a divide-by-1 OSC clock.

For details on the time required for initialize and refresh sequences, as well as on EEPROM address mapping, refer to Section 8-12-7, “EEPROM Address Mapping.”

8-12-2. Initialize

After the IC is reset from the $\overline{RES}$ pin or using the SWRESET command, an EEPROM-based initialize sequence is started. The oscillator circuit is active during the initialize sequence, and stops oscillating upon completion of the initialize sequence.

8-12-3. SENOP

SENOP is a state in which, if any bit string is outside the range of values 00h to FFh, defined in command level 1 as those that can be input in 8 bit quantities, is input as if it were a command by the MPU, it is assumed to be NOP (00h) and an NOP operation is performed for it. (This also includes those outside the range of command levels 2 and 3.) For details on command levels, refer to Section 9-1, “Command Table.”

The following conditions apply for SENOP mode:

SENOP mode is entered when INISEL = HIGH and an initialize/refresh is performed and 5Ah is recognized from the SENOP address in the EEPROM. To exit SENOP mode, the IC must be reset.

If the IC is mounted in place and EEPROM data is set under the above conditions by the LCD-module manufacturer, the expected command operation of command levels 2/3 may not be confirmed in normal use. In such a case, issue the INIESC command before SENOP is recognized after a reset (i.e., before the SENOP address is read from the EEPROM) in order to stop the initialize operation.

Because the amount of data read from the EEPROM at this time differs depending on the timing with which INIESC is issued, if the commands are to be set by EEPROM readout as well, the user should set them by issuing commands.

The INIESC issuance timing requires that it be issued 10 us or more after reset, but within the initialization time.

8-12-4. EEPROM Address Mapping

EEPROM address mapping refers to what contents are set at each EEPROM address.

EEPROM address mapping is fixed, and cannot be altered. The table below shows the address mapping of an EEPROM. Note that the set values in this table are shown for reference purposes only.

EEPROM Address	D15	D14	D13	D12	D11	D10	D9	D8	HEX	DEC	Set value	
1	0	0	1	0	1	0	0	1	29	41	RDID1	
3	0	0	0	0	0	0	0	0	0	0	RDID3	
5	0	0	0	0	0	0	0	0	00	0	E2RCTL	P2
7	0	0	0	0	0	0	0	0	00	0	DISCTL	P2
25	0	0	0	0	0	0	0	0	00	0		P20
27	0	0	0	0	0	0	0	0	00	0	EVRSET	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
37	0	0	0	0	0	0	0	0	00	0	MDLDEF	P1
39	0	0	0	0	0	0	0	0	00	0		P3
41	0	0	0	0	0	0	0	0	00	0	PWRDEF	P2
59	0	0	0	0	0	0	0	0	00	0		P20
61	0	0	0	0	0	0	0	0	00	0	Reserve	
63	0	0	0	0	0	0	0	0	00	0	GCPSET0P R	P2
93	0	0	0	0	0	0	0	0	00	0		P32
95	0	0	0	0	0	0	0	0	00	0	GCPSET0N R	P2
125	0	0	0	0	0	0	0	0	00	0		P32
127	0	0	0	0	0	0	0	0	00	0	GCPSET0P GB	P2
157	0	0	0	0	0	0	0	0	00	0		P32
159	0	0	0	0	0	0	0	0	00	0	GCPSET0N GB	P2
189	0	0	0	0	0	0	0	0	00	0		P32
191	0	0	0	0	0	0	0	0	00	0	GCPSET1P R	P2
221	0	0	0	0	0	0	0	0	00	0		P32
223	0	0	0	0	0	0	0	0	00	0	GCPSET1N R	P2
253	0	0	0	0	0	0	0	0	00	0		P32
255	0	0	0	0	0	0	0	0	00	0	GCPSET1P GB	P2
285	0	0	0	0	0	0	0	0	00	0		P32
287	0	0	0	0	0	0	0	0	00	0	GCPSET1N GB	P2
317	0	0	0	0	0	0	0	0	00	0		P32
319	0	0	0	0	0	0	0	0	00	0	GCPSET2P R	P2
349	0	0	0	0	0	0	0	0	00	0		P32
351	0	0	0	0	0	0	0	0	00	0	GCPSET2N R	P2
381	0	0	0	0	0	0	0	0	00	0		P32
383	0	0	0	0	0	0	0	0	00	0	GCPSET2P GB	P2
413	0	0	0	0	0	0	0	0	00	0		P32
415	0	0	0	0	0	0	0	0	00	0	GCPSET2N GB	P2
445	0	0	0	0	0	0	0	0	00	0		P32
447	0	0	0	0	0	0	0	0	00	0	GCPSET3PR	P2
477	0	0	0	0	0	0	0	0	00	0		P32
479	0	0	0	0	0	0	0	0	00	0	GCPSET3NR	P2
509	0	0	0	0	0	0	0	0	00	0		P32
511	0	0	0	0	0	0	0	0	00	0	Reserve	
513	0	0	0	0	1	0	0	0	08	8	END	

EEPROM Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX	DEC	Set value	
2	0	0	0	0	0	0	0	0	00	0	EDID2	
4	0	0	0	0	0	0	0	0	00	0	E2RCTL	P1
6	0	0	0	0	0	0	0	0	00	0	DISCTL	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
26	0	0	0	0	0	0	0	0	00	0	MADDEF	P1
28	0	0	0	0	0	0	0	0	00	0	EVRSET	P2
36	0	0	0	0	0	0	0	0	00	0		P10
38	0	0	0	0	0	0	0	0	00	0	MDLDEF	P2
40	0	0	0	0	0	0	0	0	00	0	PWRDEF	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
60	0	0	0	0	0	0	0	0	00	0	EXVSYNCDEF	P1
62	0	0	0	0	0	0	0	0	00	0	GCPSET0P R	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
94	0	0	0	0	0	0	0	0	00	0	GCPSET0N R	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
126	0	0	0	0	0	0	0	0	00	0	GCPSET0P GB	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
158	0	0	0	0	0	0	0	0	00	0	GCPSET0N GB	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
190	0	0	0	0	0	0	0	0	00	0	GCPSET1P R	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
222	0	0	0	0	0	0	0	0	00	0	GCPSET1N R	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
254	0	0	0	0	0	0	0	0	00	0	GCPSET1P GB	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
286	0	0	0	0	0	0	0	0	00	0	GCPSET1N GB	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
318	0	0	0	0	0	0	0	0	00	0	GCPSET2P R	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
350	0	0	0	0	0	0	0	0	00	0	GCPSET2N R	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
382	0	0	0	0	0	0	0	0	00	0	GCPSET2P GB	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
414	0	0	0	0	0	0	0	0	00	0	GCPSET2N GB	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
446	0	0	0	0	0	0	0	0	00	0	GCPSET3PR	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
478	0	0	0	0	0	0	0	0	00	0	GCPSET3NR	P1
⋮	0	0	0	0	0	0	0	0	00	0		⋮
510	0	0	0	0	0	0	0	0	00	0	Reserve	
512	0	1	0	1	1	0	1	0	5A	90	SENOP	

Oscillation frequency: Approx. 1 MHz
Oscillation period: Approx. 1000 ns
Total number of bytes read: 512Byte
Approx.4.11ms = (512Byte x 8 times + ID 12 times + DUMMY 1 time) x 1000

8-13. Auto Display-Off Function

If the auto display-off function is to be used, it is necessary to set both the INISEL pin and the RESSEL pin HIGH.

This function is used to turn the display off without leaving after-images by writing OFF data to the LCD when the IC is reset during display on the LCD.

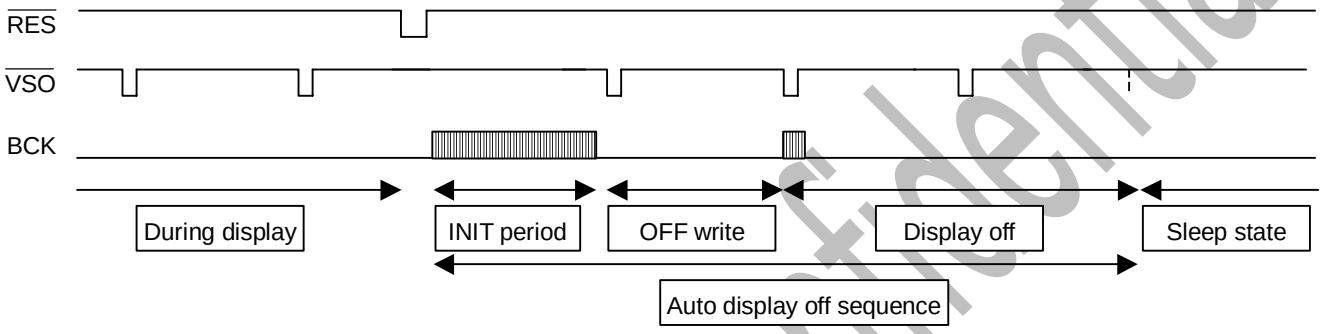
Normally, when the IC is reset during display on the LCD, the LCD drive and power-supply boost become inactive, causing after-images to remain until the charge collected in the LCD is completely dissipated.

8-13-1. Auto Display-Off Sequence

The auto display-off sequence starts initializing the VRAM after reset, and writes OFF data to the LCD after initialization. The auto-off sequence requires a time equal to the initialize period (1 frame) + 4 frames.

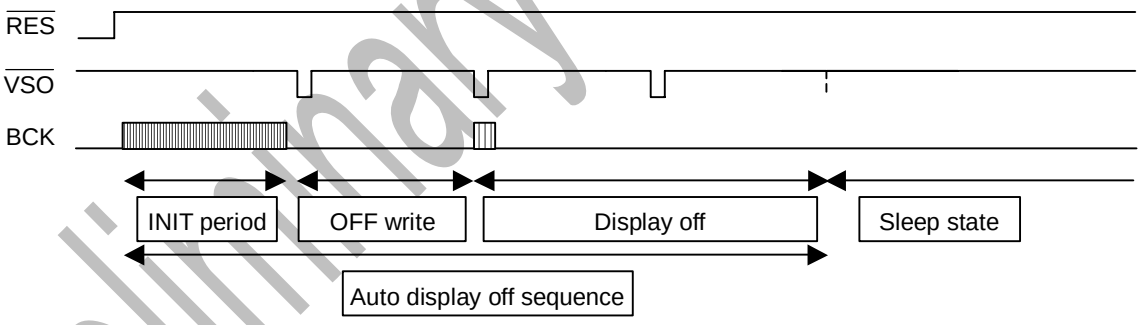
Refer to Section 8-4, “Reset.”

◇ When reset in the hardware



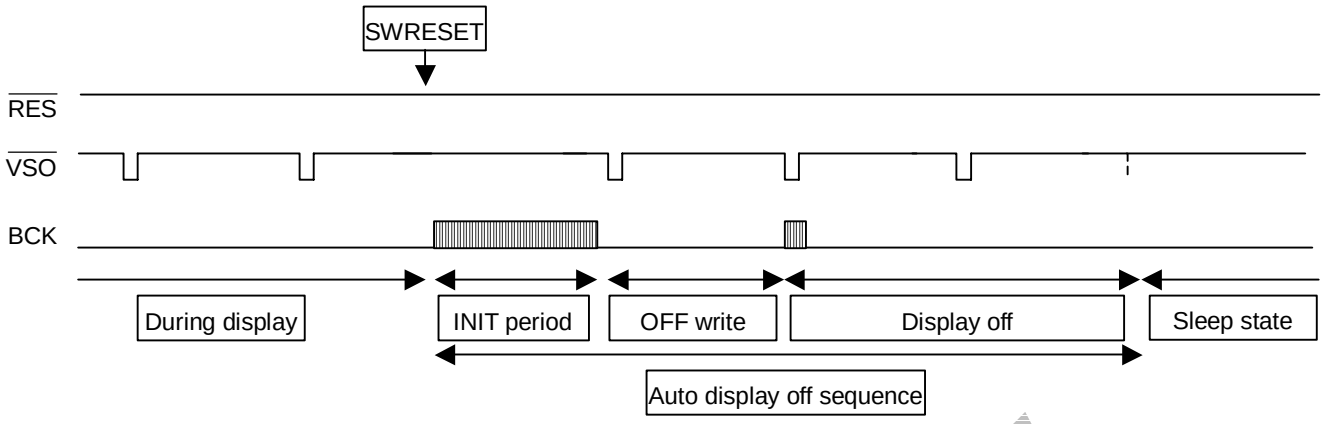
Because the auto display-off sequence is executed after reset, if the reset period is excessively long the effects of this operation may be less than expected, as all operations are stopped during the reset period and after-images remain in the LCD.

If the IC is powered down while in a reset state (reset in the hardware by $\overline{RES}$ = LOW), after-images will remain until the charge in the LCD is completely dissipated because no auto-off sequences are performed in such case.



In cases in which both the INISEL and RESSEL pins are set HIGH, an auto display-off sequence is executed after reset. Therefore, when the IC is reset at power-on, an auto display-off sequence is performed after the reset.

◇ When reset in software



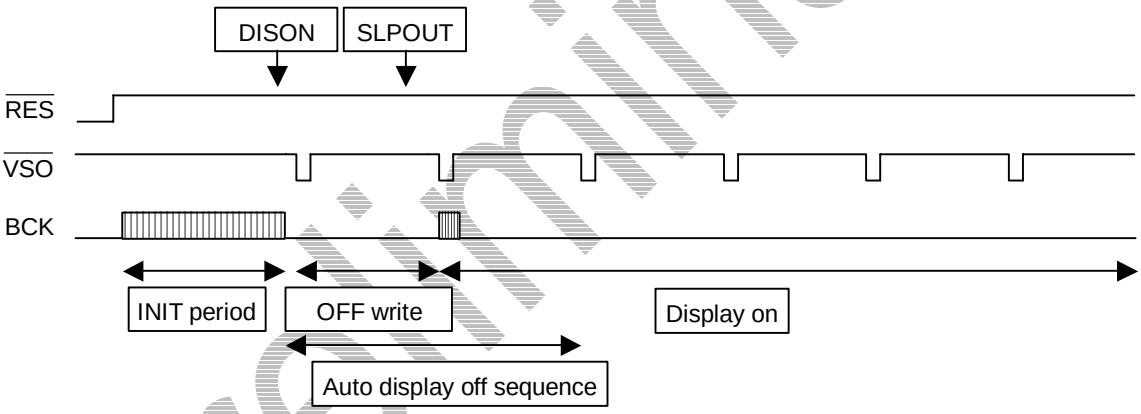
If a software reset is performed during display or during OFF write in a display-off sequence, the IC is reset synchronously with the internal horizontal sync signal.

If a software reset is performed during sleep mode, the IC is reset immediately upon recognition of the command, with no need for internal synchronization.

If the IC needs to be powered down after a software reset, wait a length of time equal to or greater than the "auto-off-sequence period + 1H," after issuing the command and before turning the power off.

◇ Command issuance during auto display-off sequence

If the SLPOUT and DISON commands are input during an auto display-off sequence, the driver enters a sleep-out or a display-on state directly.



8-14. EEPROM Control Function

The S1D19122 permits bidirectional communication of EEPROM data.

Control classification	Control method	Access destination	Command	Setting	Other conditions
User	Command refresh	EEPROM	SLPOUT	-	INISEL=HIGH

Refer to Section 8-12, “Initialize Function.”

Separate from the above classifications, there is another type of control, known as EEPROM pin control.

8-14-1. Access Limitations on EEPROM Control

Because EEPROM control is exercised using the BRST, BCK, and BDATA pins, no two methods of control can be used simultaneously.

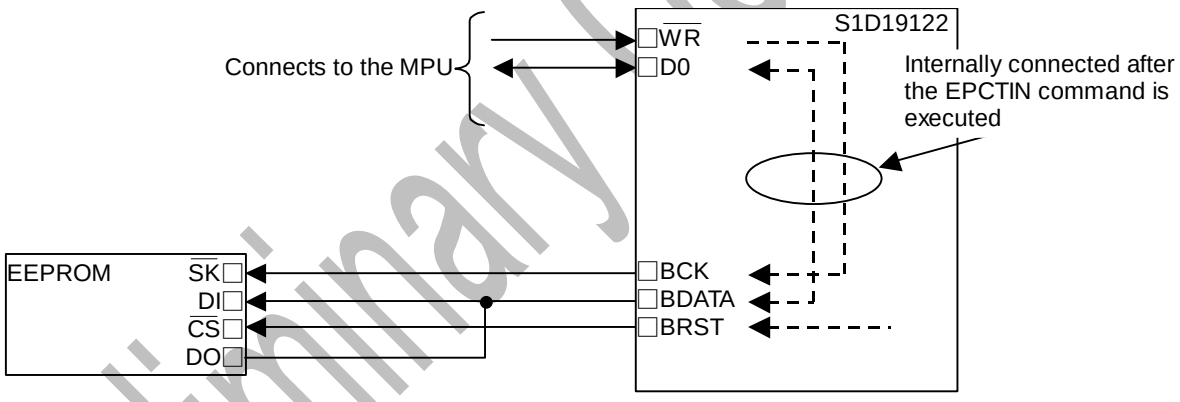
8-14-2. EEPROM Pin Control Function

EEPROM pin control is a function that, when pin control is selected using the EPCTIN command, directly accesses the EEPROM without the intervention of the S1D19122 function by connecting its MPU interface pins of $\overline{WR}$ ($\overline{RD}$, A0) and D0 internally to BCK and BDATA, and automatically generating the BRST pin by internal logic.

This function is intended to permit the LCD-module manufacturer to write the initial value to EEPROM before shipping the LCD module, or to read out the written EEPROM data for confirmation. Please do not use this function for any other purpose. In addition, make sure commands are issued only when the driver is in a sleep state and not performing an initialize or any other operation.

When pin control is selected using the EPCTIN command, the pins are connected as shown below. BRST is an EEPROM enable signal, and BRST = HIGH initiates access to the EEPROM. For pin control to be exercised, the $\overline{CS}$ pin must be held LOW beginning with EPCTIN command issuance. When the $\overline{CS}$ pin is released HIGH after pin control is entered, the driver exits pin control and becomes ready to accept other normal commands.

◇ Image depicting wire connections during pin control (when using 80-series MPU parallel interface)



◇ MPU interface and pin assignments during pin control

Interface	Pin assignment		
	BCK	BRST	BDATA
80-series MPU parallel interface	$\overline{WR}$	Auto-generation	D0
68-series MPU parallel interface	$\overline{RD}$	Auto-generation	D0
4-wire, 8-bit data serial interface	$\overline{WR}$	Auto-generation	D0
3-wire, 9-bit data serial interface	A0	Auto-generation	D0

◇ Precautions to be observed during pin control

For pin control to be exercised with the use of a parallel interface, it is necessary that the $\overline{RD}$ pin be set HIGH when 80 MPU is being used, or that the $\overline{RD}$ (R/$\overline{W}$) pin be set LOW when 68 MPU is being used.

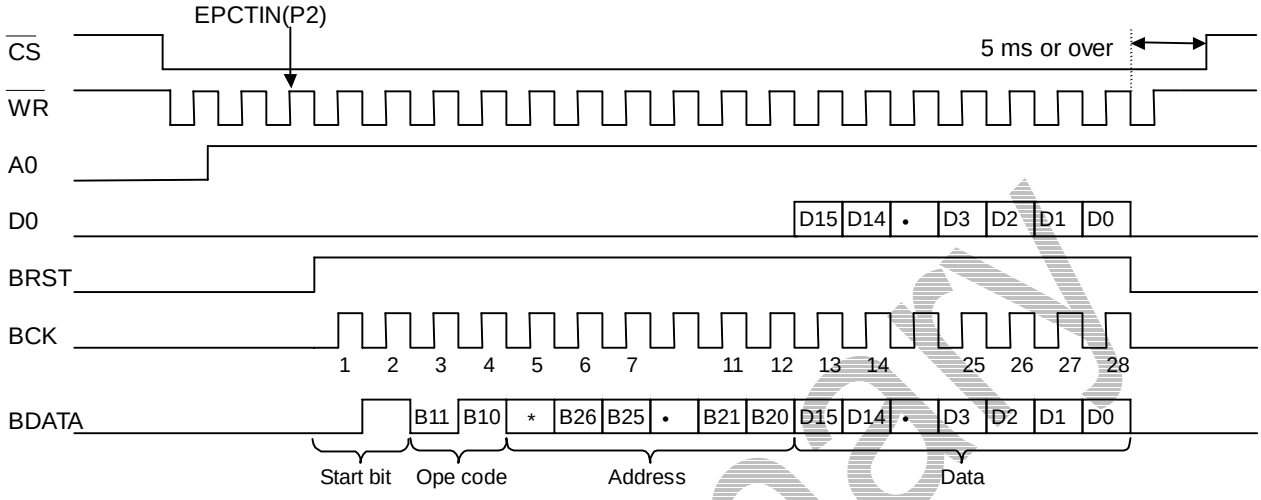
If the power supply needs to be accessed during pin control while a serial interface is being used, it is necessary that the D1 and D0 pins can be controlled on the LCD module.

It is also necessary that A0 be held HIGH while the EEPROM data is being accessed.

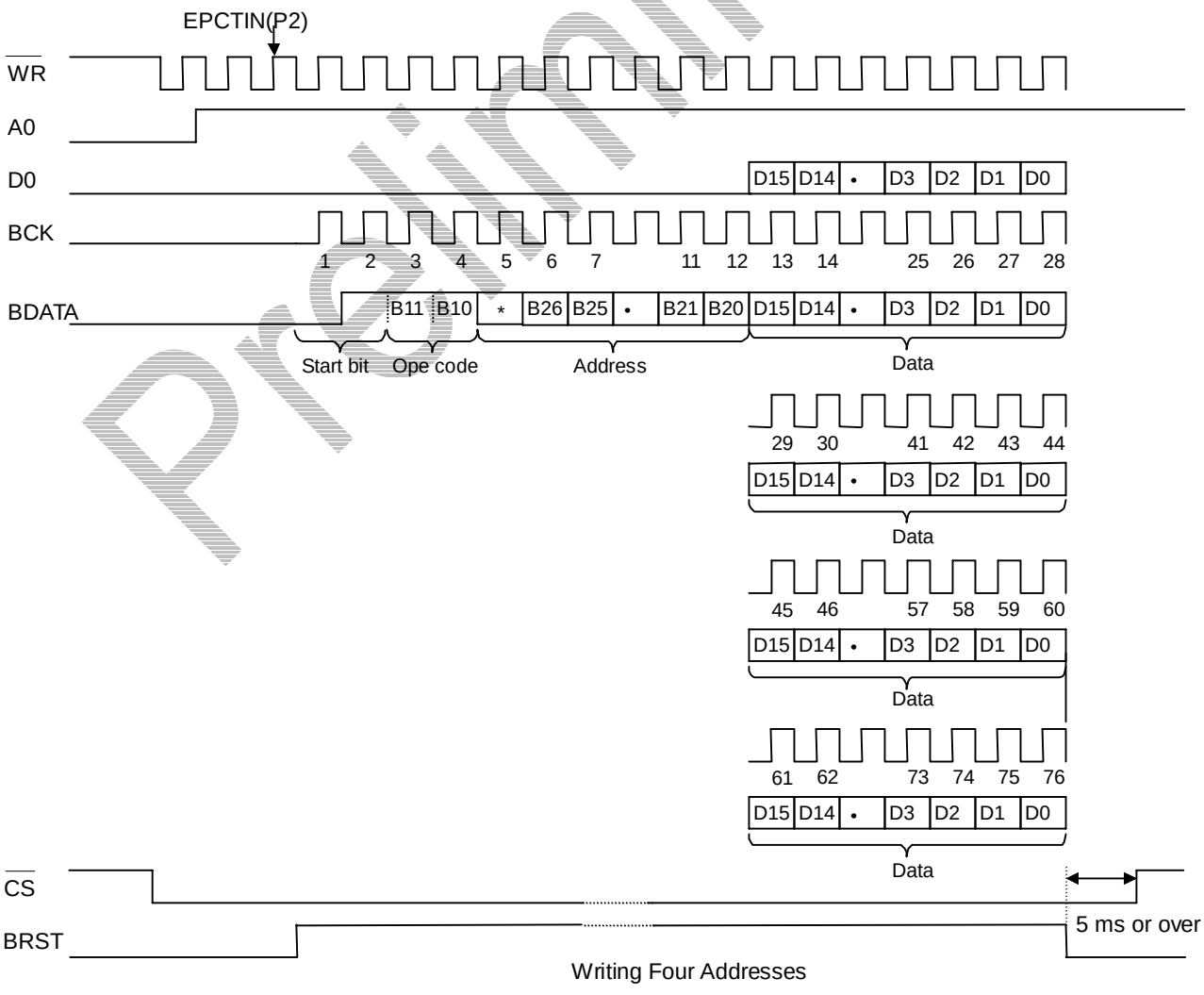
8-14-3. Pin Control – For Write to EEPROM

The $\overline{WR}$ ($\overline{RD}$, A0) and D0 pins are assigned to the BCK and BDATA pins.

If the EEPROM needs to be accessed for read, an operation code for read must be issued in the first 5 bits of the command. The S1D19122 generates an operation code according to the access code that is set in the command parameter, in order to supplement the issuance of an operation code. This task is processed via a serial transfer: an operation code is serially transferred from the BDATA pin synchronously with the $\overline{WR}$ ($\overline{RD}$, A0) signal. After an operation code has been transferred, input data from outside to the D0 pin. This signal will be input to the EEPROM through BCK and BDATA.



Writing One Address

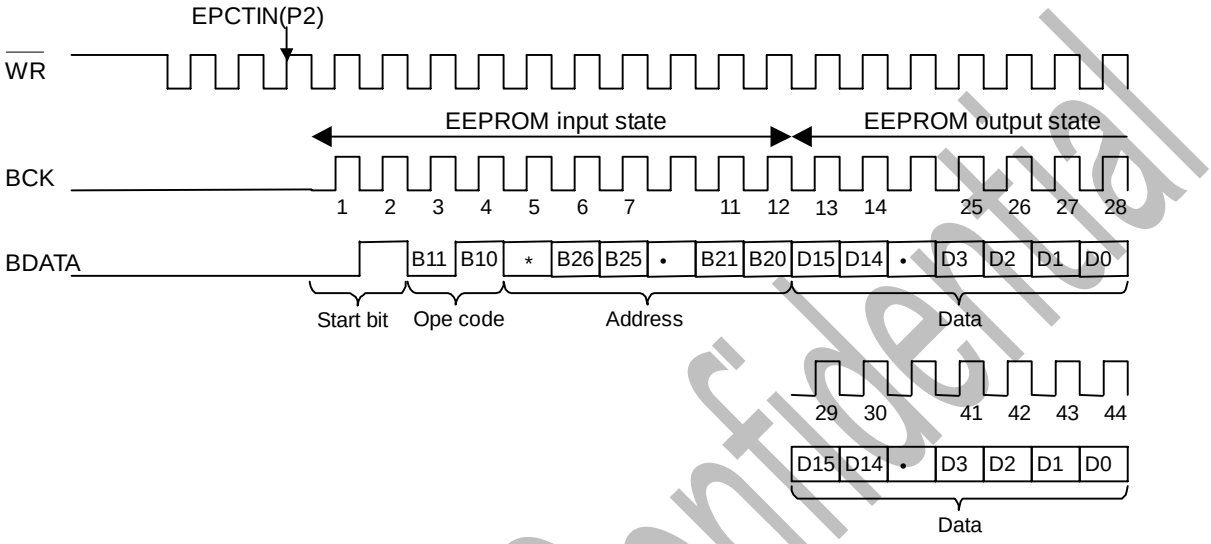


Writing Four Addresses

8-14-4. Pin Control – For Read from EEPROM

The $\overline{WR}$ ($\overline{RD}$, A0) and D0 pins are assigned to the BCK and BDATA pins.

If the EEPROM needs to be accessed for read, an operation code for read must be issued in the first 5 bits of the command. The S1D19122 generates an operation code according to the access code set in the command parameter, in order to supplement the issuance of an operation code. This task is processed via a serial transfer: an operation code is serially transferred from the BDATA pin synchronously with the $\overline{WR}$ ($\overline{RD}$, A0) signal. After the operation code has been transferred, switch the BDATA and D0 pins for input and output, respectively, synchronously with the falling edge of BCK, and read data from the EEPROM. Then, set the $\overline{CS}$ pin HIGH to switch the BDATA and D0 pins back for output and input, in order to terminate the read operation.



8-15. Versatile LCD Support

Although the S1D19122 is basically designed for use in the model LCD module described in Section 8-9-1, it can be set so as to be suitable for several other LCDs.

8-15-1. Support for Normally White and Normally Black LCDs

The S1D19122 can be set so as to be suitable for Normally White and Normally Black LCDs. However, care should be taken, as off-display colors differ between Normally White and Normally Black LCDs.

By default, the S1D19122 is set for Normally White LCDs.

	Normally White LCD	Normally Black LCD
Display-off line	White	Black
Partial non-display line	White	Black
Display off (DISOFF)	White	Black
DISINOFF	Normal color	Normal color
DISINV	Inverted color	Inverted color

8-16. Oscillator Circuit

This circuit generates a synchronizing signal for the LCD drive. The S1D19122 contains one 256-gray-scale-level oscillator circuit that is a complete circuit comprised of an RC network. To use this built-in 256-gray-scale-level oscillator circuit, set OSSEL LOW. Setting OSSEL HIGH enables an external clock to be input to OS1.

OSSEL	Oscillator circuit	Input
0	Complete built-in RC oscillator circuit	—
1	External clock input	OS1

To use an external clock, input that external clock to OS1. External-clock input is disabled when the complete built-in RC oscillator circuit is selected.

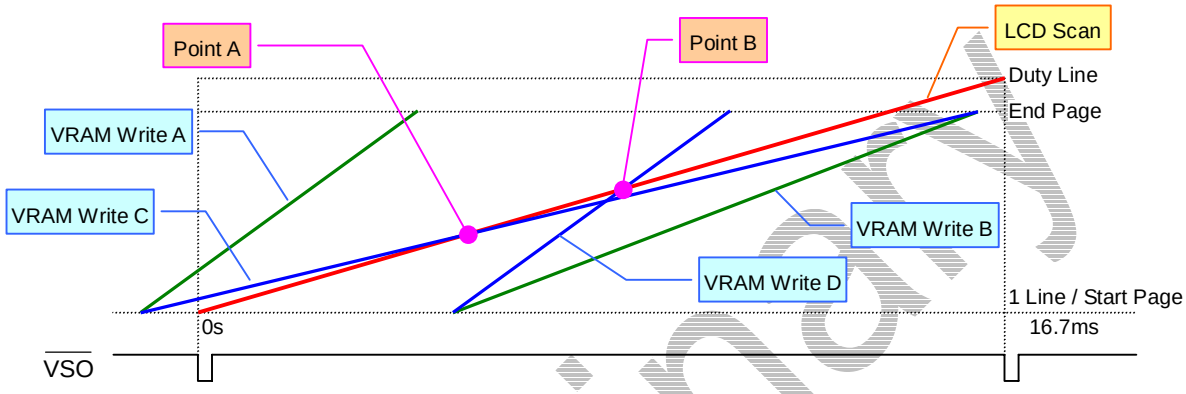
8-17. Solutions for Moving-Picture Display

If, when the display screen changes frequently as in moving-picture display, display scan and display data write are performed asynchronously, the display screen may sometimes appear as if it were torn (known as the “tearing effect”). The following describes the mechanism by which the tearing effect occurs and a method for correcting it.

8-17-1. Tearing Effect

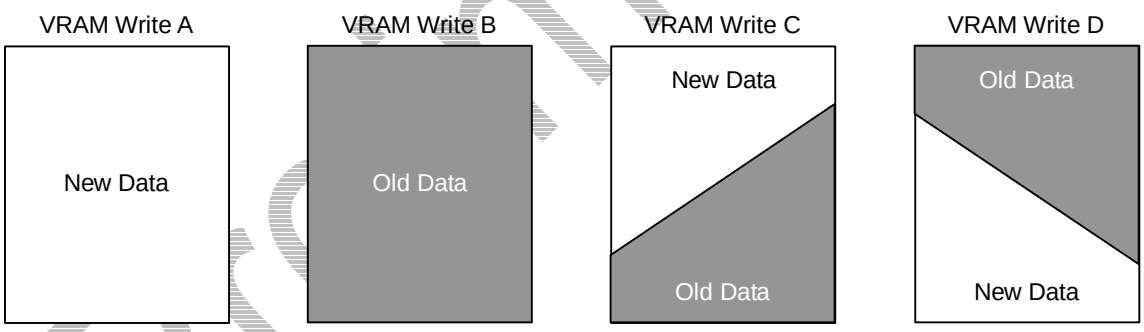
If the displayed data changes frequently as in moving-picture display, what is known as the “tearing effect” occurs, presenting a problem in terms of display quality. In the explanation of the tearing effect given below, the data already being displayed is referred to as “old data,” the data to be newly displayed is referred to as “new data,” and the explanation is premised on the assumption that display-data write is performed within the display scan time.

The tearing effect is a condition in which old data and new data are displayed at the same time in a frame in which the driver is transferring data to the VRAM in order to display new data. Within a single frame, the screen is split vertically between the old and new data. This is a symptom that occurs when display scan and display-data write are reversed in a given timing.



In the above diagram, “LCD Scan” denotes display scan in one frame, and “VRAM Write*” denotes display-data write for one screen of data in the VRAM access area.

The display upon completion of display scan is similar to that shown below. Display-data rewriting of the entire screen is assumed here.



No tearing effects occur in the cases of “VRAM Write A” and “VRAM Write B.” In the case of “VRAM Write C” or “VRAM Write D,” a tearing effect occurs at “Point A,” where display scan gets ahead of display-data write, or at “Point B,” where display-data write gets ahead of display scan. The old-data/new-data split start position depends on the position at which a display-data write starts, and the angle of the old/new boundary depends on the write speed. The closer the relative speeds of display scan and write, the sharper the angle.

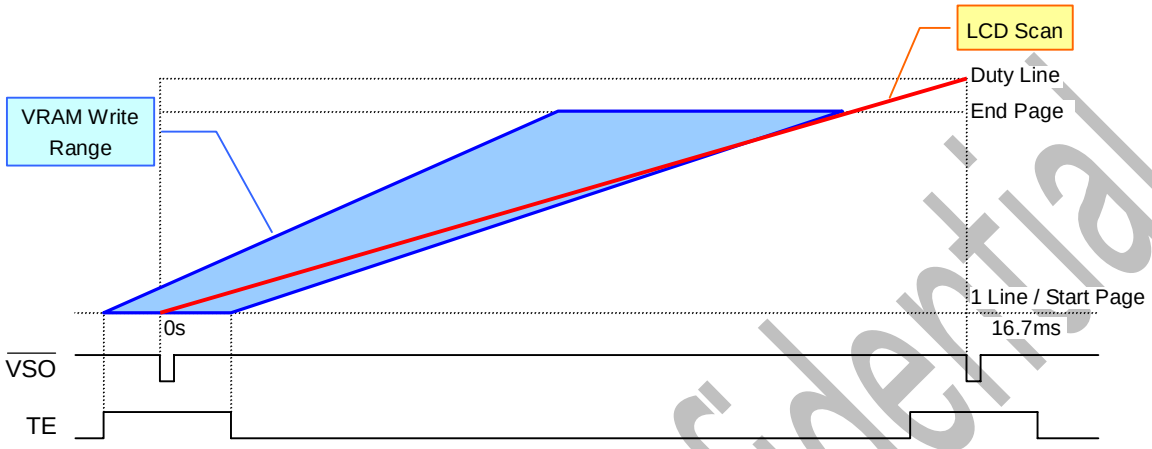
A symptom similar to the above also occurs in still-picture display, but because the tearing effect occurs only in the frame in which display data is being rewritten, and the next display scan after a display data write has finished produces the intended display, this does not normally present a problem.

8-17-2. Display Synchronous Data Transfer by TE Signal

The problem of the tearing effect can be solved by synchronizing display-data rewrite and display scan.

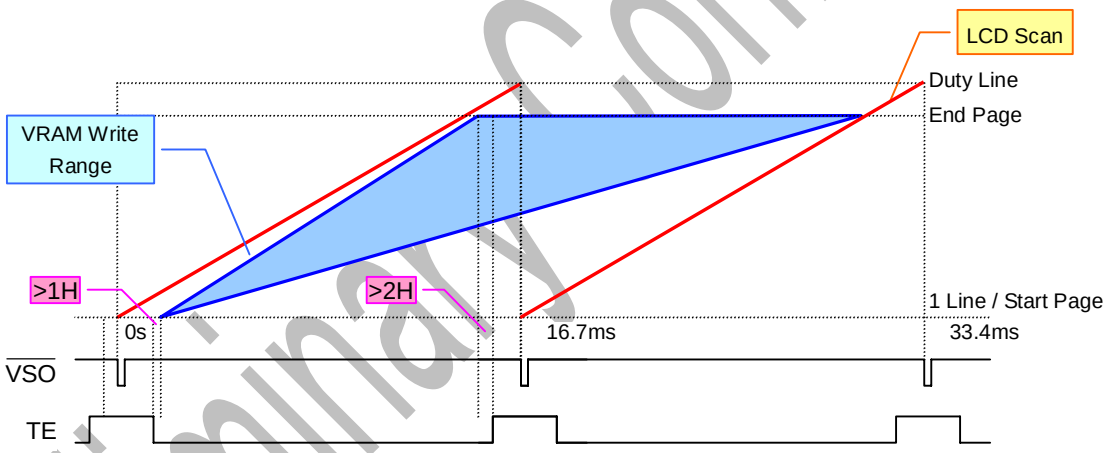
To this end, it is necessary that display-data write be started from a point at which no tearing effect will occur as a result of monitoring of the display-scan state using the TE signal, and that the display data be transferred so as to complete a write of one screen of display data before display scan finishes. In the diagram below, “VRAM Write Range” denotes the display-data transfer interval in which no tearing effects occur, and the TE signal is used in Mode1.

◇ Pattern 1



The written display data is displayed within the same frame. If the host’s display-data transfer capability is high (i.e., the transfer speed is high), use of this pattern is recommended.

◇ Pattern 2



The written display data is displayed in the next frame. If the host’s display-data transfer capability is low (i.e., the transfer speed is low), use of this pattern is recommended.

The fastest cycle in which display-data write can be performed depends on the AC characteristics of the IC. Furthermore, the number of cycles required for the display data to be written is determined by the display-data format and the VRAM access area.

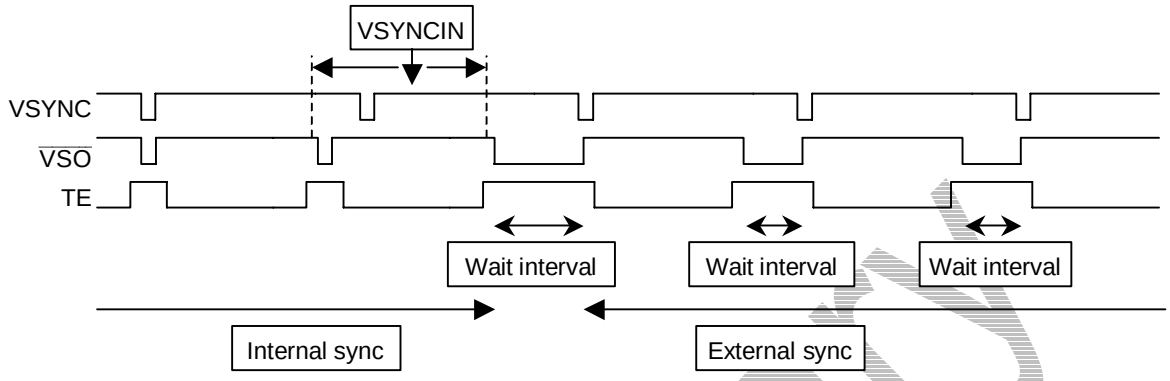
- Effective display-area scan time = frame period × (display lines / drive duty)
- Display-data write time = write cycle time × number of write cycles

Therefore, the problem of the tearing effect can be avoided by writing the display data shown in pattern 1 if the display-data write time is shorter than the effective display-area scan time, or by writing the display data shown in pattern 2 if the display-data write time is longer.

8-17-3. Display Synchronous Data Transfer by External VSYNC

The problem of the tearing effect can be avoided by entering external VSYNC synchronization mode using the VSYNCIN command to achieve synchronization of display-data rewrite and display scan.

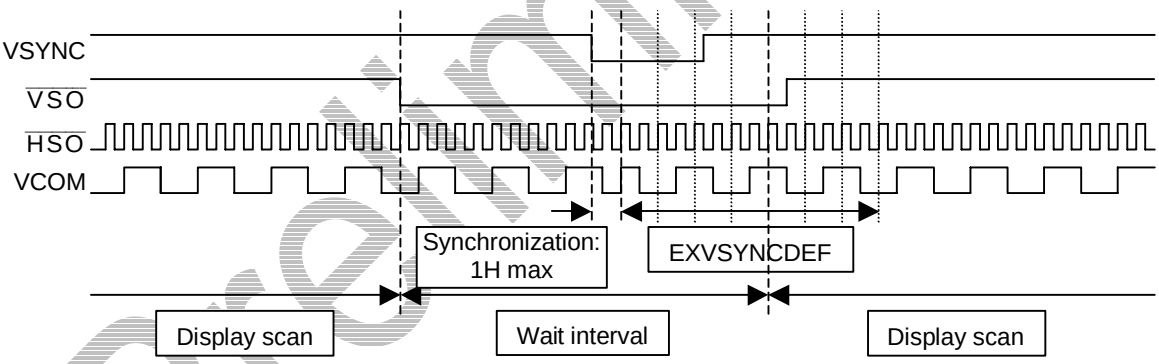
In the frame in which the VSYNCIN command was input, display scan is executed using the internal vertical sync signal. Then, a synchronization wait interval is entered, in which the external vertical sync signal (VSYNC) is awaited. Next, external VSYNC synchronization mode is entered. During external VSYNC synchronization, the VSYNC signal is synchronized with the internal operation by detecting its LOW level, and then one frame of display scan is performed. Upon completion of display scan, a synchronization wait interval is entered again. The VSYNCIN command issued within the range shown in the diagram below undergoes the same transition of operations (recognized 1H + 1OSC before the fall of $\overline{VSO}$).



To ensure that the LCD will not be overcharged during the synchronization wait interval, SO outputs OFF data according to VCOM. $\overline{VSO}$ is stopped at the LOW level, thereby turning the common driver control signal off. VRAM readout is not performed.

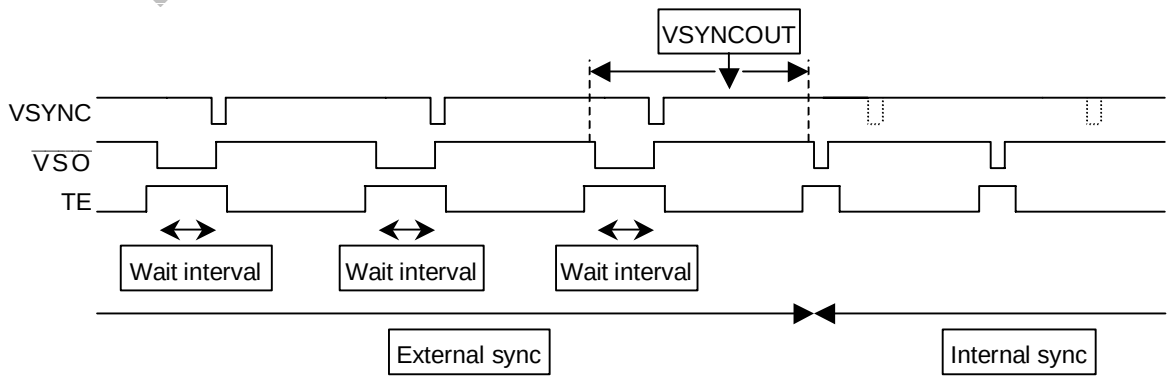
The interval from when the VSYNC signal is synchronized with the internal operation to when display scan is started by the EXVSYNCDEF command can be corrected. The VSYNC signal requires at least 1H for its LOW level to be synchronized with the internal operation. Therefore, the external VSYNC period requires a larger number of cycles than specified below.

External VSYNC period = internal vertical sync period (display scan interval) + synchronization interval (1H) + correction interval (EXVSYNCDEF)



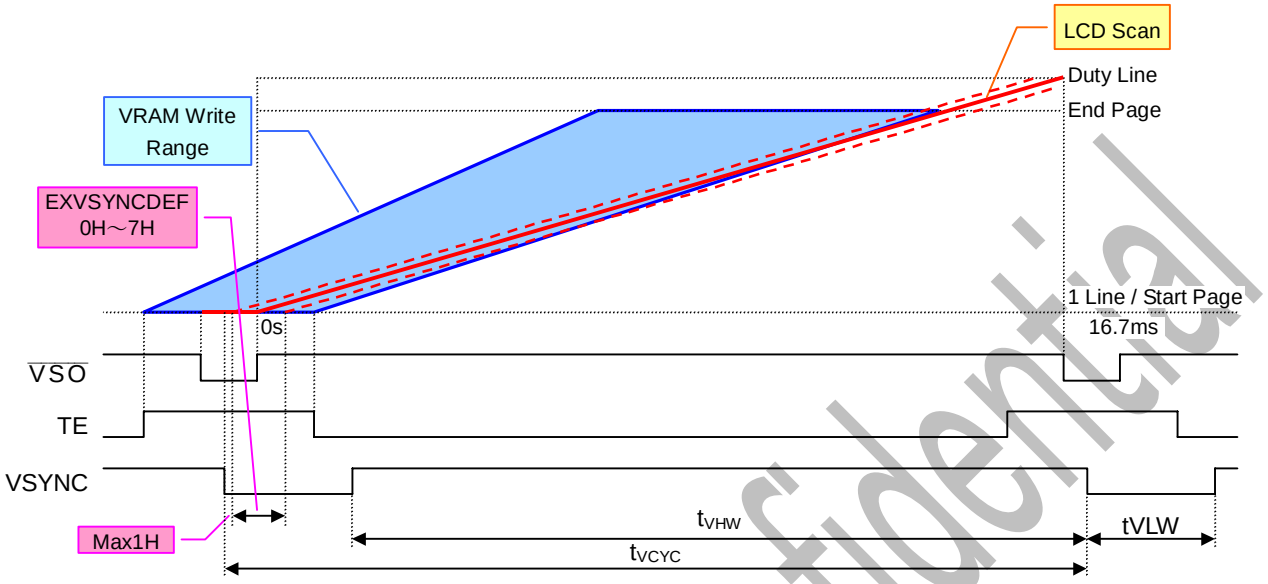
Shown above is a case in which the correction interval is set to 4H using the EXVSYNC command.

During external VSYNC synchronization, internal synchronization mode is entered using the VSYNCOUT command, which is recognized in frame sync. The VSYNCOUT command issued within the range shown in the diagram below undergoes the same transition of operations (recognized 1H + 1OSC before the fall of $\overline{VSO}$).



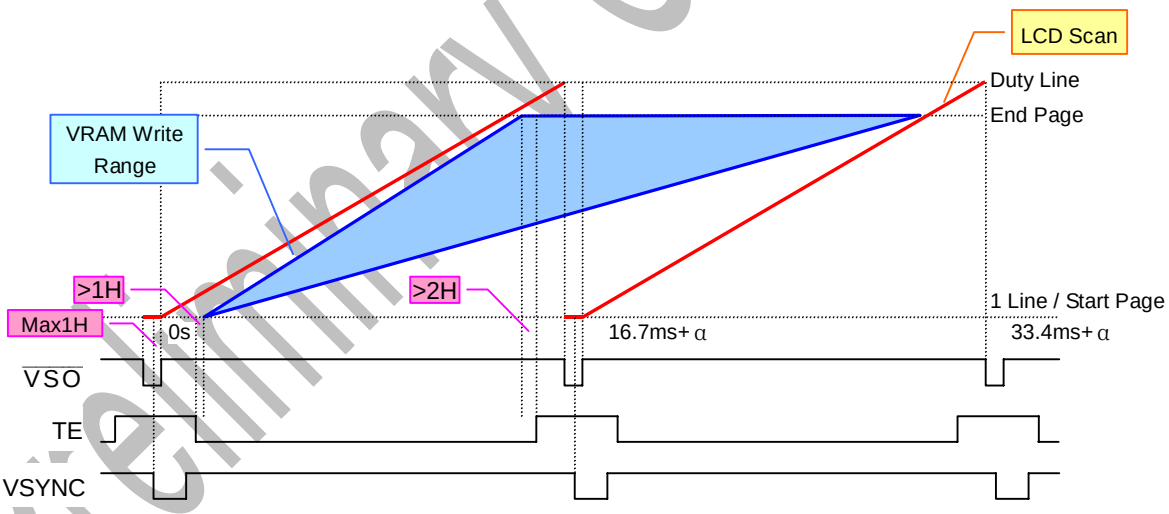
◇ Solution for the MPU interface

Shown below is a case in which, in external VSYNC synchronization mode with the correction interval set to 4H by the EXVSYNC command, the display data is written synchronously with the rising edge of the TE signal (Mode1). The problem of the tearing effect can be avoided provided that display-data write is started and ended within the “VRAM Write Range” shown in the diagram.



The written display data is displayed within the same frame. If the host’s display-data transfer capability is high (i.e., the transfer speed is high), use of this pattern is recommended.

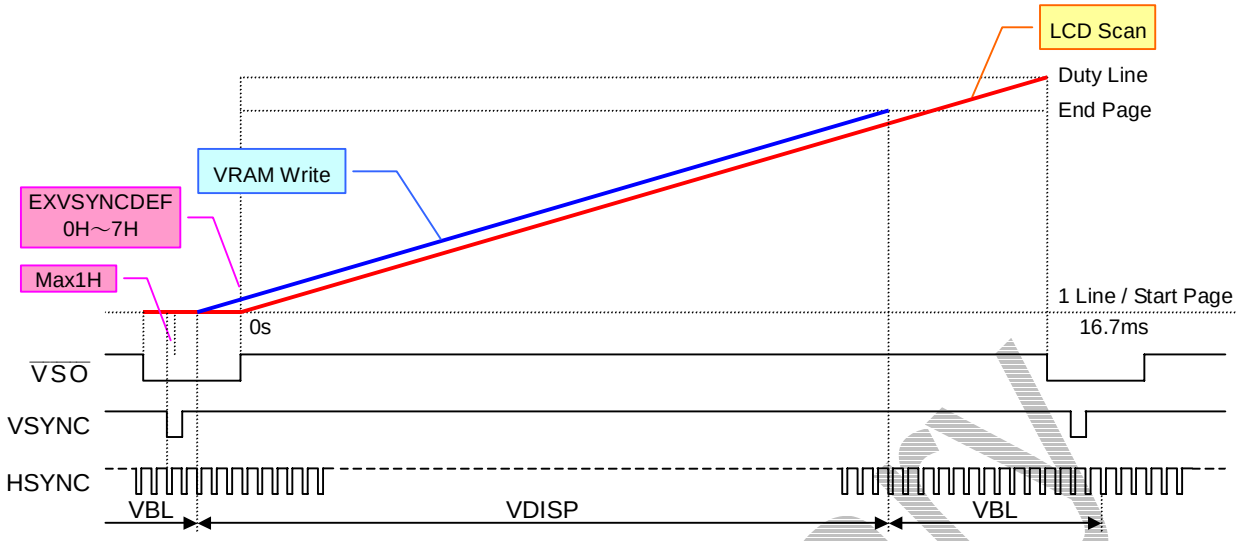
Shown below is a case in which, in external VSYNC synchronization mode with the correction interval set to 0H by the EXVSYNC command, the display data is written synchronously with the falling edge of the TE signal (Mode1). The problem of the tearing effect can be avoided provided that display-data write is started and ended within the “VRAM Write Range” shown in the diagram.



The written display data is displayed in the next frame. If the host’s display-data transfer capability is low (i.e., the transfer speed is slow), use of this pattern is recommended.

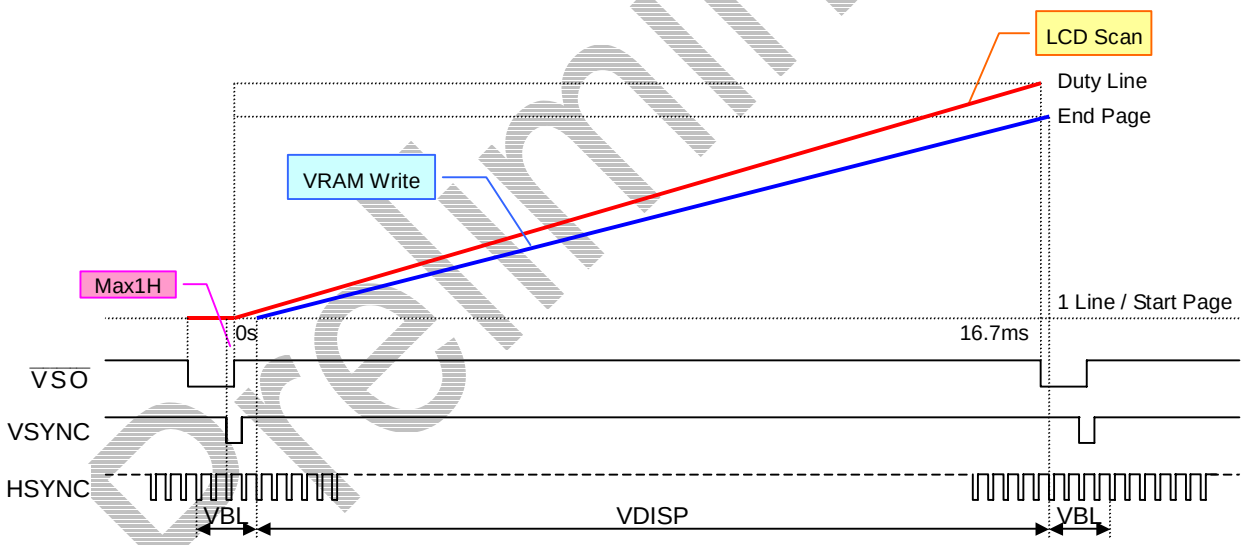
◇ Solution for the LCDC interface

Shown below is a case in which the correction interval is set to 0H or greater by the EXVSYNC command, and the display data is written via the LCDC interface.



If the LCDC's display-data transfer capability is high (i.e., the transfer speed is fast), or display-data write and display scan are not reversed due to a narrow VR interval, use of this pattern is recommended.

Shown below is a case in which the correction interval is set to 0H by the EXVSYNC command, and the display data is written via the LCDC interface.



If the LCDC's display-data transfer capability is low (i.e., the transfer speed is slow), use of this pattern is recommended.

8-17-4. Conditions under Which the Tearing Effect Cannot be Avoided

Methods for avoiding the problem of the tearing effect are as specified above; the following requirements must be met in utilizing these methods.

In order to increase the ease of VRAM access, the MADCTL and MADDEF commands are provided to enable the VRAM address-0 position and the VRAM access scan direction to be set in a wide variety of ways. To enable mirror display, furthermore, the MADCTL and MADDEF commands now permit the LCD readout scan direction and common scan direction to be set in combination. However, avoiding the tearing effect requires that the direction of display scan and that of display-data write always match.

Refer to Section 8-9-3, "Address-0 Position and VRAM Access Scan Direction."

Refer to Section 8-9-4, "LCD Readout Scan Direction and Gate Scan Direction."

In addition, it is necessary that the display data be transferred every screen, and that a transfer of one screen of data be started and ended within an interval that does not overlap the display scan.

Unless the above settings and conditions are complied with, a tearing effect may occur.

8-18. Power-Supply Circuit

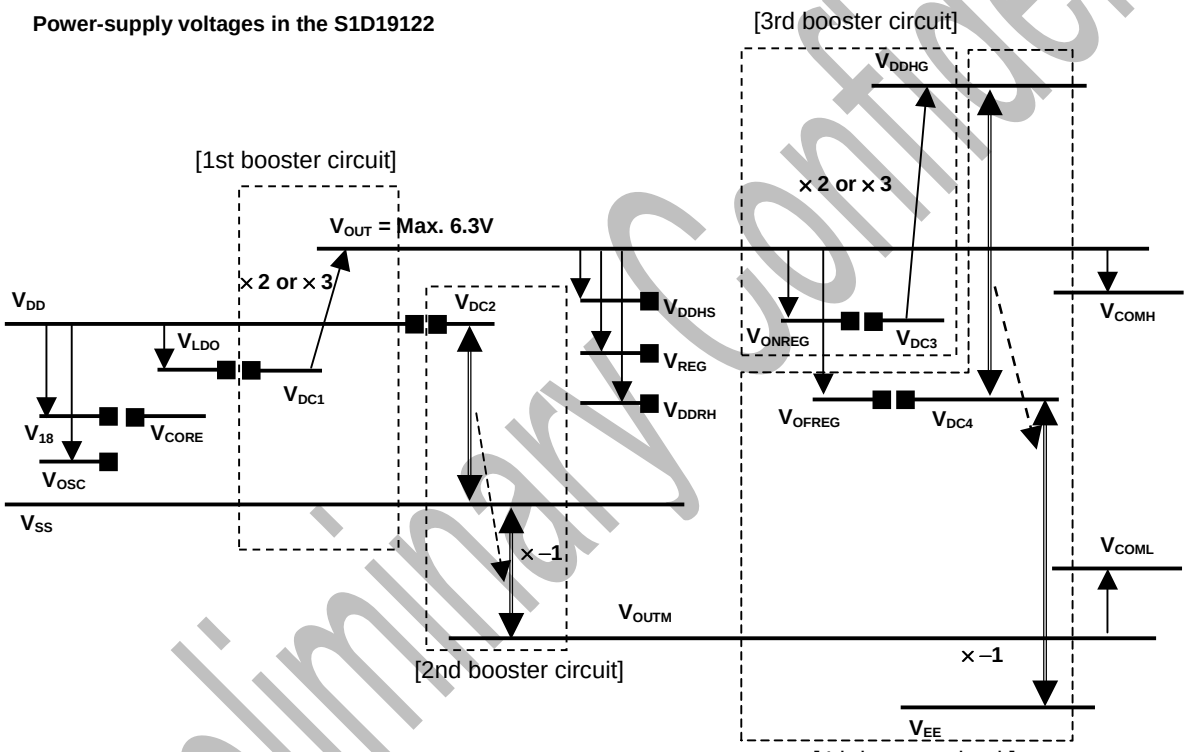
8-18-1. Operation of the Power-Supply Unit

The input of a single power supply (V_{DD}) can generate all of the bias voltages required for the LCD drive. The generated voltage levels are listed below.

Oscillator-circuit power-supply voltage:	V_{OSC}
Internal-logic power-supply voltage:	V_{18}
1st and 2nd booster reference power-supply voltage:	V_{LDO}
Reference power-supply voltage:	V_{REG}
Power-supply voltages:	V_{OUT}, V_{OUTM}
Source-driver power-supply voltages:	V_{DDHS}, V_{DDRH}
Gate-driver power-supply voltages	V_{DDHG}, V_{EE}, V_{ONREG}, V_{OFREG}
Opposite-electrode power-supply voltages:	V_{COMH}, V_{COML}

Because electronic volume control is incorporated, each output voltage can be adjusted. The electronic volume control can be controlled using the EVRSET command. Furthermore, because a reference-voltage circuit is incorporated, a LCD drive power supply that is consistently stable can be supplied with no need to rely on the system power supply. The 1st, 2nd, 3nd and 4th booster circuits incorporated into the IC make it possible to supply highly accurate, constant voltages.

Power-supply voltages in the S1D19122



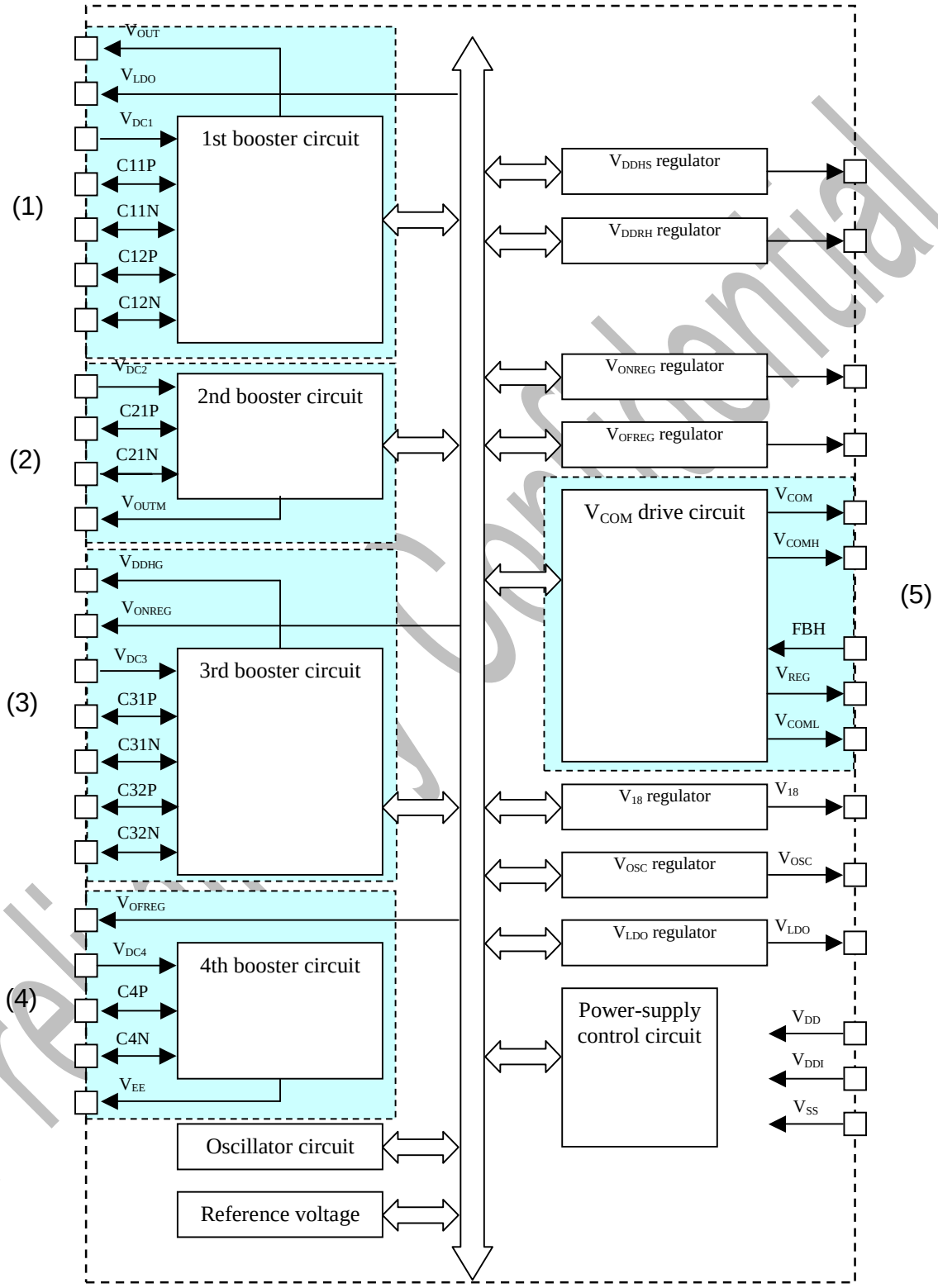
V_{DC1} connects to V_{DD} or V_{LDO}
V_{DC2} connects to V_{DD} or V_{LDO}
V_{DC3} connects to V_{OUT} or V_{ONREG}
V_{DC4} connects to V_{SS}, V_{DD}, V_{OUT}, or V_{OFREG}

8-18-2. LCD Drive Power Supplies and Power-Supply Specification

Item			S1D19122
LCD drive output	SO1 – SO960		VGS0-VGS63 (analog 64 gray scales)
	GO1 – GO240		Gate-on voltage: V_{DDHG} Gate-off voltage: V_{EE}
	GD1 - GD4		Gate-off voltage: V_{EE}
	V_{COM}		Common HIGH voltage: V_{COMH} Adjusted by electronic volume control or external resistor Common LOW voltage: V_{COML} Automatically set by $V_{COMH} - V_{COMW} \times 2$ Common amplitude: V_{COMW} Adjusted by electronic volume control
Input power supply	V_{DDI}		I/O power supply
	V_{DD}		Booster-circuit reference power supply
Built-in power supply	V_{LDO}		1st and 2nd booster reference power supply
	V_{OSC}		Oscillator power supply
	V_{18}		Internal-logic power supply
	V_{OUT} (1st-booster output)		Source, V_{COM}, etc. generation power supply (V_{DD} or $V_{OUT} \times 2$ or 3
		V_{REG}	Reference power supply
		V_{DDHS}	Source-driver power supply
		V_{DDRH}	Maximum gray-scale-level voltage
		V_{COMH}	V_{COM}-signal-HIGH power supply
		V_{COML}	V_{COM}-signal-low power supply
		V_{OFREG}	V_{EE}-generation reference voltage
		V_{ONREG}	V_{DDHG}-generation reference voltage
	V_{OUTM} (2nd-booster output)		V_{COML}-generation power supply $V_{OUT} \times -1$ boosted
	V_{DDHG} (3rd-booster output)		Gate-on voltage Boosted by 2 or 3 times
	V_{EE} (4th-booster output)		Gate-off voltage $V_{DDHG} \times -1$ boosted

8-18-3. Basic Configuration Diagram of the Built-In Power Supply

The S1D19122 comes with a built-in power supply for a LCD drive. To ensure that the built-in power supply circuit will operate stably, a recommended basic circuit is shown below for your reference. Select an external circuit configuration that suits the specifications of your system.



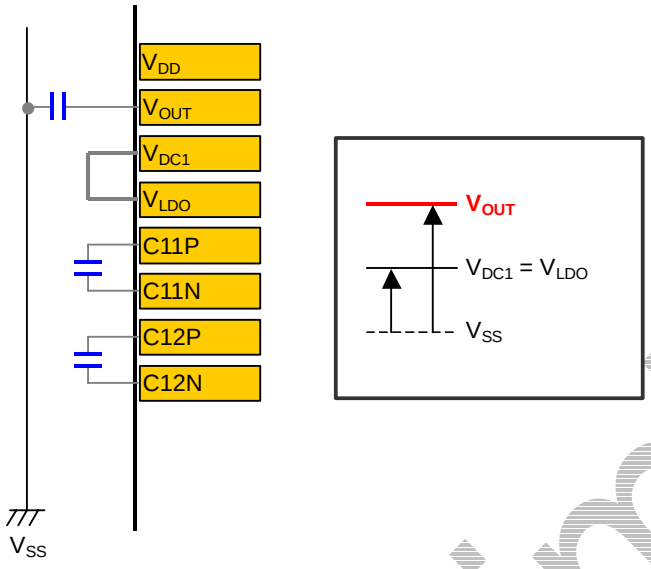
8-18-4. 1st Booster Circuit

The 1st booster circuit is comprised of a charge-pump-type DC/DC converter; its boost reference power supply can be selected by switching external connections. The selected input power-supply voltage (V_{DC1}) is converted into the power-supply voltage (V_{OUT}) for the LCD power-supply circuit by multiplying the input voltage by 'n.' The multiplying factor for this voltage conversion can be selected from between 2-fold and 3-fold using a command.

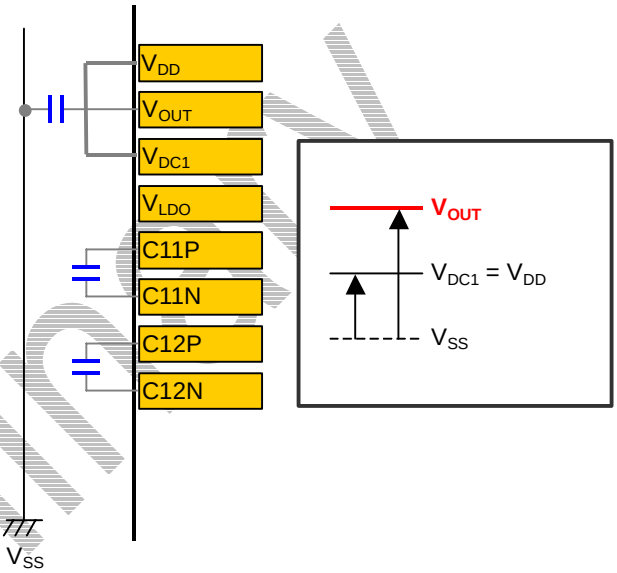
$$V_{OUT} = n \times V_{DC1} \text{ [V] (where n = 2 or 3)}$$

The pin connections corresponding to (1) in the basic configuration diagram of the built-in power supply circuit can be altered as shown below to realize a desired booster circuit.

◇ × 2 or × 3 boost ($V_{DC1} = V_{LDO}$)



◇ × 2 or × 3 boost ($V_{DC1} = (V_{DD})$



*VLDO can be set outputs 3.0V by B1=0 of the EVRSET command. However, because VLDO is generated with VDD, the voltage of VDD -0.15V or more is not output.

* When x2 boosting is used with VDD≦3.1V, VDC1 is recommended to be connected with VDD.

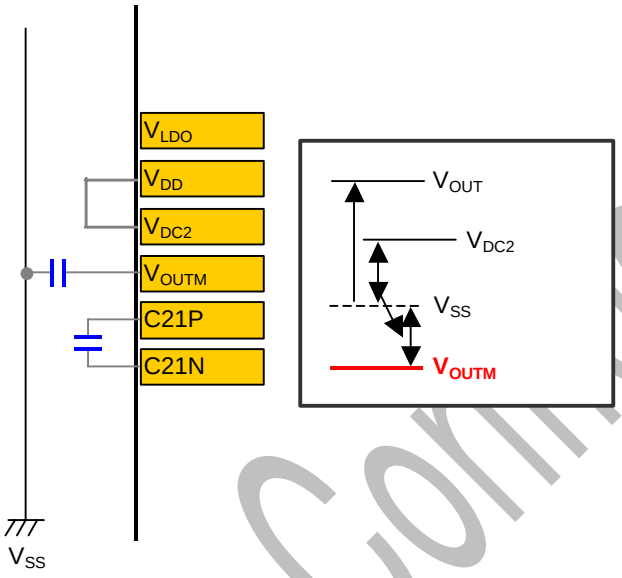
8-18-5. 2nd Booster Circuit

The 2nd booster circuit is an inverting booster circuit comprised of a charge-pump-type DC/DC converter. It converts the V_{DC2} voltage into the power-supply voltage (V_{OUTM}) for the V_{COM} circuit by multiplying it by –1 relative to V_{SS}.

$$V_{OUTM} = -1 \times V_{DC2} \text{ [V]}$$

The pin connections corresponding to (2) in the basic configuration diagram of the built-in power supply circuit can be altered as shown below to realize a desired booster circuit.

◇ Invert (× –1) boost ($V_{DC2} = (V_{DD})$



Care should be taken to ensure that $V_{DD} - V_{OUTM}$ is not greater than 6.3 V.

If $V_{DD} \leq 3.15$ V, connect V_{DC2} to V_{DD}.

If $V_{DD} > 3.15$ V, connect V_{DC2} to V_{LDO}.

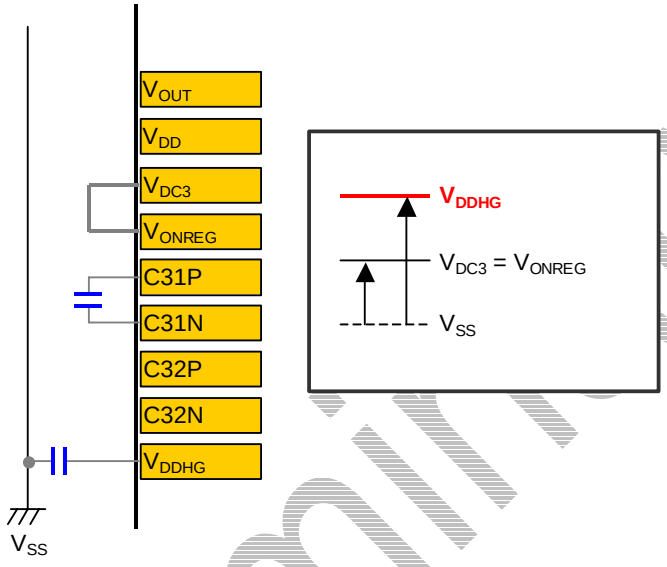
8-18-6. 3rd Booster Circuit

The 3rd booster circuit is comprised of a charge-pump-type DC/DC converter; its boost reference power supply can be selected by switching external connections. The voltage across the selected input power-supply voltage and the V_{SS} (V_{DC3} – V_{SS}) is converted to the gate-driver positive power-supply voltage (V_{DDHG}) by multiplying the input voltage by 'n.' The multiplying factor can be selected from between 2-fold and 3-fold.

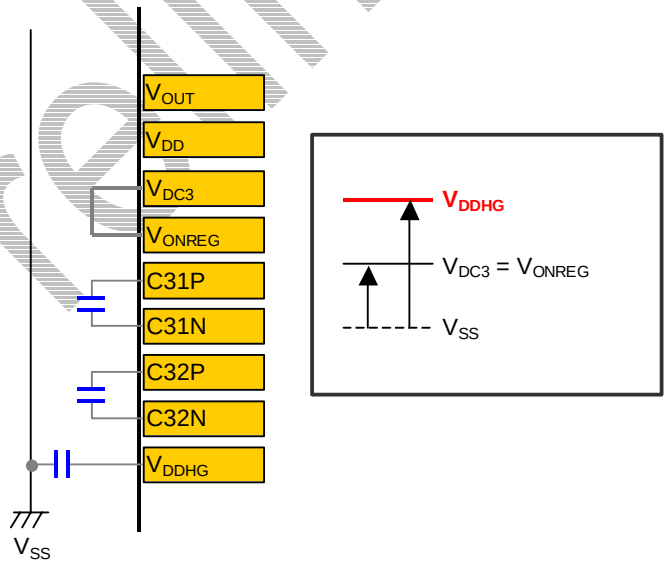
$$V_{DDHG} = n \times V_{DC3}\ [V] \text{ (where n = 2 or 3)}$$

The pin connections corresponding to (3) in the basic configuration diagram of the built-in power supply circuit can be altered as shown below to realize a desired booster circuit.

◇ $V_{DDHG} \times 2$ boost ($V_{DC3} = V_{ONREG}$)



◇ $V_{DDHG} \times 3$ boost ($V_{DC3} = V_{ONREG}$)



◇ Selected V_{DC3} voltage

The V_{ONREG} selected for V_{DC3} should satisfy the relationship $V_{DDHG} - V_{EE} \leq 30.0$ V at any multiplying factor. Selecting $V_{ONREG} = V_{DC3}$ permits the V_{DDHG} output voltage to be fine-tuned using the internal regulator. The voltage variable range is shown below.

Pin	Voltage range [V]	Variable step [V]	Output
V_{ONREG} output pin	2.4 to 5.5	0.1	Internal-regulator output

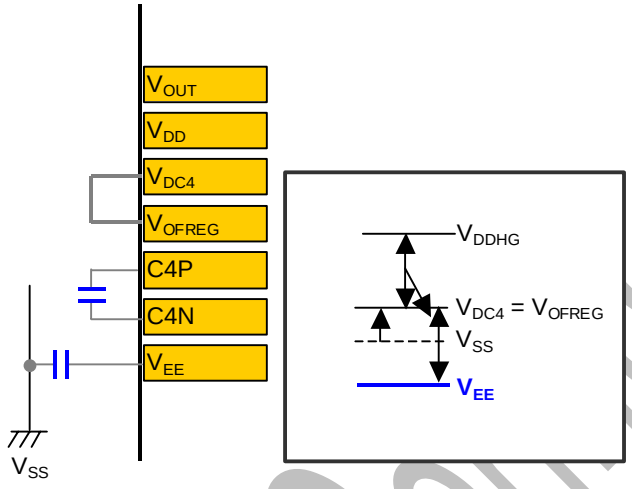
8-18-7. 4th Booster Circuit

The 4th booster circuit is comprised of a charge-pump-type DC/DC converter; its boost reference power supply can be selected by switching external connections. The selected input power-supply voltage V_{DDHG} is converted into the gate-driver negative power-supply voltage (V_{EE}) by multiplying the input voltage by '–n' relative to V_{DC4}. The multiplying factor is –1.

$$V_{EE} = n \times (V_{DDHG} - V_{DC4}) + V_{DC4} \text{ [V] (where n = –1)}$$

The pin connections corresponding to (4) in the basic configuration diagram of the built-in power supply circuit can be altered as shown below to realize a desired booster circuit.

◇ $V_{EE} \times -1$ boost



◇ Selected V_{DC4} voltage

The V_{OFREG} selected for V_{DC4} should satisfy the relationship $V_{DDHG} - V_{EE} \leq 30.0$ V at any multiplying factor. Selecting $V_{OFREG} = V_{DC4}$ permits the V_{EE} output voltage to be fine-tuned using the internal regulator. The voltage variable range is shown below.

Pin	Voltage range [V]	Variable step [V]	Output
V_{OFREG} output pin	1.0 to 4.1	0.1	Internal-regulator output

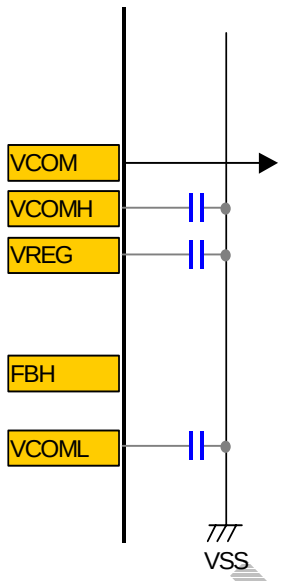
8-18-8. V_{COM} Generator Circuit

The V_{COM} generator circuit generates the V_{COMH} and V_{COML} voltages required to generate the V_{COM} output voltage. The respective voltages can be set in combination by setting the V_{COMH} electronic volume control register and the V_{COMW} electronic volume control register (V_{COMW}: V_{COM}-signal voltage amplitude). V_{COML} is determined by ($V_{COMH} - V_{COMW} \times 2$).

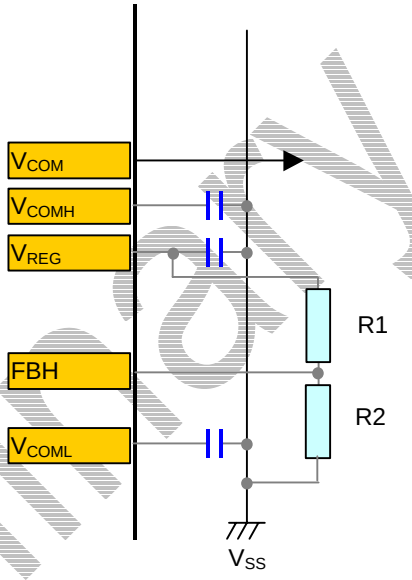
◇ V_{COMH}-adjusting internal resistors used

- V_{COMH} (V_{COM}-signal maximum voltage): Set by the electronic volume control register using the internal resistors
- V_{COMW} (V_{COM}-signal amplitude voltage): Set by the electronic volume control register using the internal resistors
- V_{COML} (V_{COM}-signal minimum voltage): $V_{COML} = V_{COMH} - V_{COMW} \times 2$ [V]

The pin connections corresponding to (5) in the basic configuration diagram of the built-in power supply circuit can be altered as shown below to realize a desired booster circuit.



Internal resister for V_{COMH} adjustment



External resistance for V_{COMW} adjustment

Pin	Voltage range [V]	Variable step [V]	Output
V_{COMH} output pin	2.00 to 5.00	0.02	Internal-regulator output
V_{COMW} voltage	1.50 to 3.05	0.05	Internal-regulator output

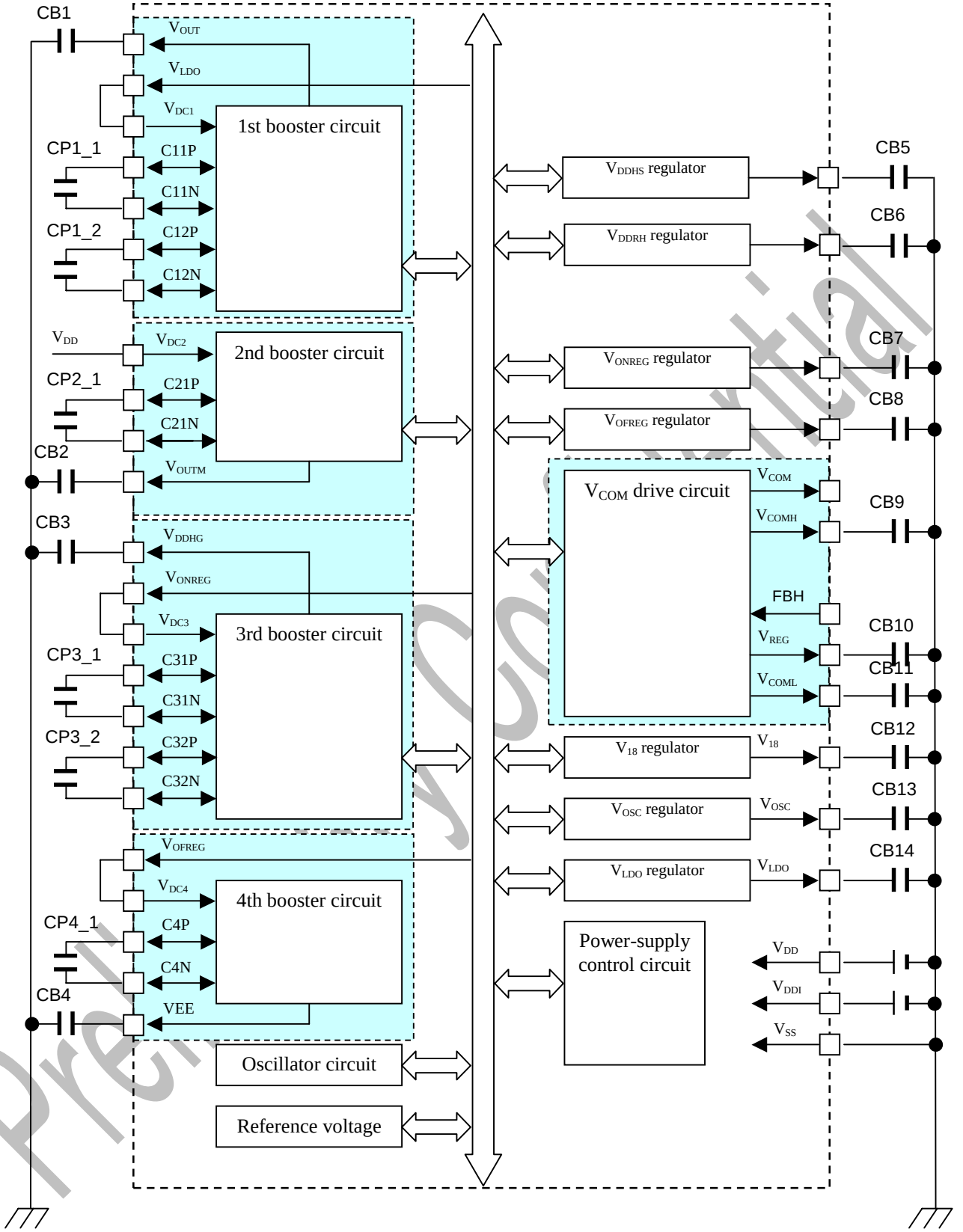
8-18-9. External-Component Wiring Diagram

◇ Example wiring of an external circuit

Specification: V_{COM} generator circuit (internal resister for V_{COMH} adjustment or external resister for V_{COMW} adjustment)

Example: When (V_{DD} = 2.85 V (T.B.D), the respective voltages under no load are as follows:

V_{LDO} = 2.0 [V] (Regulator output)
V_{REG} = 3.5 [V] (Regulator output, set by electronic volume control)
V_{OUT} = $2 \times V_{LDO}$ = 4.0 [V] or $V_{OUT} = 3 \times V_{LDO}$ = 6.0 [V]
V_{OUTM} = $-1 \times (V_{DD}$ = –2.85 [V]
V_{DDHG} = $3 \times V_{ONREG}$ = 12 [V] (3 times boosting, VDC3 = VONREG and electronic volume set to 4V)
V_{EE} = $-1 \times (V_{DDHG} - V_{OFREG}) + V_{OFREG}$ = –12 [V] (VDC4 = VOFREG and electronic volume set to 2V)



◇ Recommended capacitance values

Circuit name	Capacitor name	Capacitance value [uF]	Maximum voltage biased at both ends of the capacitor
1st booster circuit	CP1_1	1.0 to 2.2	
	CP1_2	1.0 to 2.2	
	CB1	1.0 to 2.2	V_{OUT}
2nd booster circuit	CP2_1	1.0 to 2.2	
	CB2	1.0 to 2.2	V_{OUTM}
3rd booster circuit	CP3_1	1.0 to 2.2	
	CP3_2	1.0 to 2.2	
	CB3	1.0 to 2.2	V_{DDHG}
4th booster circuit	CP4_1	1.0 to 2.2	
	CB4	1.0 to 2.2	V_{EE}
V_{COM} generator circuit	CB9	1.0 to 2.2	V_{COMH}
	CB10	0.1	V_{REG}
	CB11	1.0 to 2.2	V_{COML}
Regulator	CB5	1.0 to 2.2	V_{DDHS}
	CB6	1.0 to 2.2	V_{DDRH}
	CB7	1.0	V_{ONREG}
	CB8	1.0	V_{OFREG}
	CB12	1.0 to 2.2	V_{18}
	CB13	1.0 to 2.2	V_{OSC}
	CB14	1.0 to 2.2	V_{LDO}

The maximum voltages here refer to the maximum voltages for the case of V_{REG} = 3.5V that can be set using the internal electronic variable resistor. V_{REG} fluctuations are not included.

The capacitance values shown above are recommended values. When selecting capacitors, verify the indicated quality of the capacitor in relation to the actual LCD module in order to ensure that the set capacitance values are conducive to stable LCD drive voltages.

Use the B characteristics of the capacitor.

◇ Recommended wiring-resistance values when COG-mounted

Pin type	Pin name	Pin No.	Resistance value
Power-supply pin	V_{DDI}		10Ω or less
	V_{SS}		10Ω or less
	V_{DD}		10Ω or less
	V_{18}		10Ω or less
	V_{CORE}		10Ω or less
Booster pin	1st booster pins (V_{LDO}, V_{DC1}, C11P, C11N C12P, C12N, V_{OUT})		10Ω or less
	2nd booster pins (V_{OUTM},C21P,C21N, V_{DC2})		20Ω or less
	3rd booster pins (C31P,C31N,C32P,C32N V_{DDHG}, V_{ONREG}, V_{DC3})		30Ω or less
	4th booster pins (C4P,C4N V_{EE}, V_{OFREG}, V_{DC4})		30Ω or less
Built-in power supply	V_{DDHS}, V_{DDRH}		30Ω or less
V_{COM}	V_{COM} generator pins (V_{COMH}, V_{COML})		20Ω or less
Other logic-signal pins	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, D0-D17, etc.		100Ω or less

Shown above are the recommended values, not requirements for the designed operation. The booster pins affect the efficiency of power conversion; the lower the resistance values, the greater the efficiency.

The wiring to the FBH pin has a high-impedance, and should therefore be of the shortest possible distance to prevent it from

being affected by noise. In addition, make sure it is not wired across other signal lines.

For all other pins, resistance values of 100Ω or less are recommended.

8-19. Gray-Scale-Voltage Generator Circuit

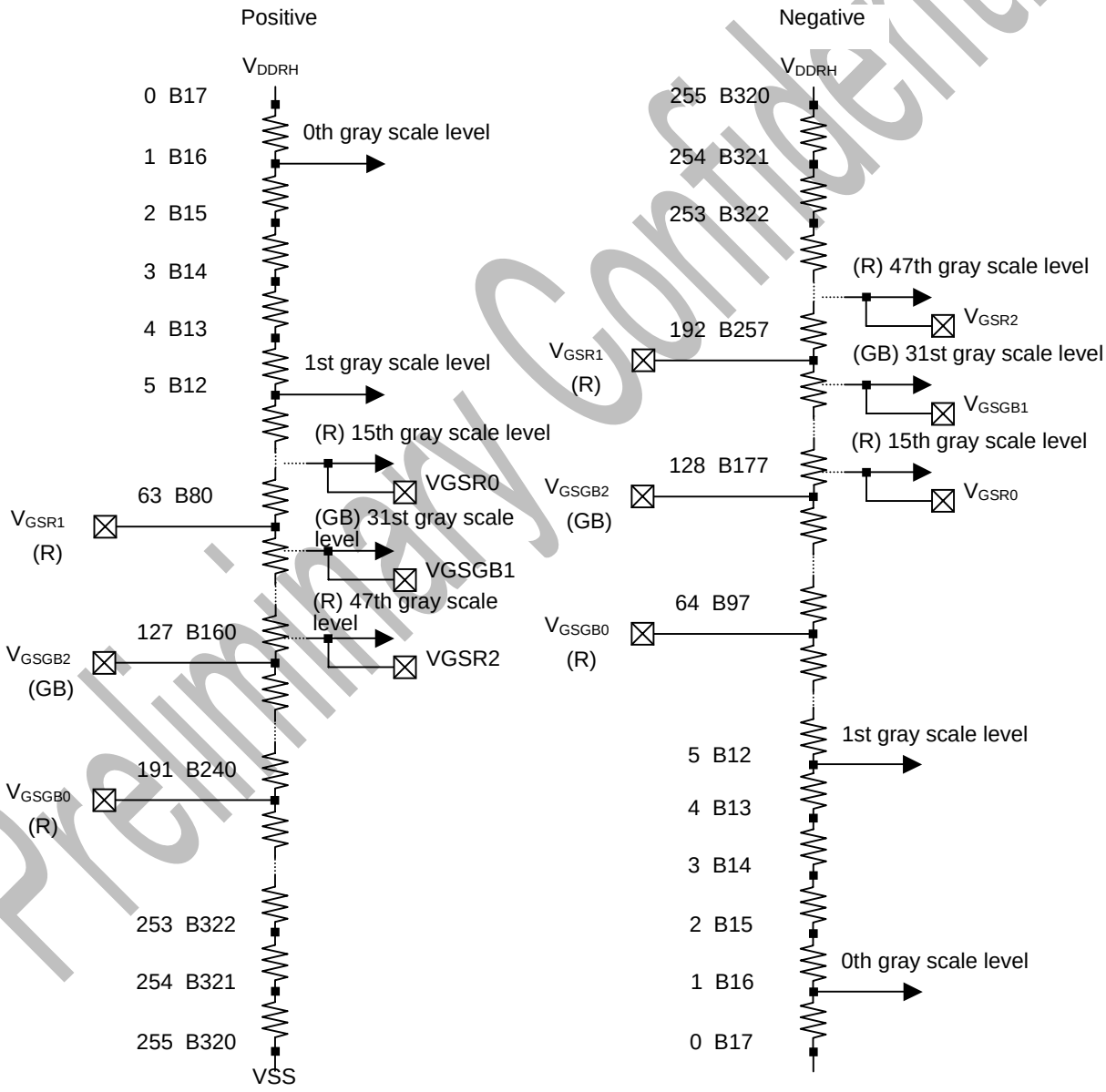
The gray scale voltages are 65 discrete voltages selected from among those derived from voltage divisions using a ladder resistor, as shown below. Sequentially beginning with the 0th gray scale level, write a 1 to the bit for each resistor-ladder position to be selected. Always make sure a total of 65 bits have been set to 1.

Example settings

D7	D6	D5	D4	D3	D2	D1	D0
B17	B16	B15	B14	B13	B12	B11	B10

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1

In the example settings here, select the voltage at resistor-ladder position 1 for the 0th gray scale level, and at resistor-ladder position 5 for the 1st gray scale level.



9. Commands

9-1. Command Table

◇ Command Level 1: Normal Command

No.	Command	HEX	Description	Type	Para	Com/Para			Para Reset		Com Exe	Cont in	ROM	Ref
						Reg	Act1	Act2	Hard	Soft				
1	NOP	00	No operation	1	-	Com	Dir	-	-	-	-	Y	-	-
2	SWRESET	01	Sotware reset	1	-	Com			-	-	Reset-Seq	N	-	-
			(When Sleep in)				Dir	-						
3	RDDIDIF	04	Read display identification information	2	4	Com	Dir	-	-	-	-	Y	Y	Y
4	RDDST	09	Read display status	2	5	Com	Dir	-	Y	Y	-	Y	-	-
5	RDDPM	0A	Read display power mode	2	2	Com	Dir	-	Y	Y	-	Y	-	-
6	RDDMADCTL	0B	Read display MADCTL	2	2	Com	Dir	-	Y	Y	-	Y	-	-
7	RDDCOLMOD	0C	Read display pixel format	2	2	Com	Dir	-	Y	Y	-	Y	-	-
8	RDDIM	0D	Read display image mode	2	2	Com	Dir	-	Y	Y	-	Y	-	-
9	RDDSM	0E	Read display Signal mode	2	2	Com	Dir	-	Y	Y	-	Y	-	-
10	RDDSDR	0F	Read display self diagnostic result	2	2	Com	Dir	-	Y	Y	-	Y	-	-
11	SLPIN	10	Sleep in	1	-	Com	DVS	-	-	-	3V *1	N	-	-
12	SLPOUT	11	Sleep out	1	-	Com	Dir	-	-	-	4V *1	N	-	-
13	PTLON	12	Partial mode on	1	-	Com	DVS	-	-	-	3V *1	N	-	-
14	NORON	13	Normal display mode on	1	-	Com	DVS	-	-	-	2V *1	N	-	-
15	DISINOFF	20	Display inversion off	1	-	Com	DVS	-	-	-	2V	N	-	-
16	DISINV	21	Display inversion on	1	-	Com	DVS	-	-	-	2V	N	-	-
17	GAMSET	26	Gamma set	2	1	P1	DVS	-	Y	Y	2V	N	-	-
18	DISOFF	28	Display off	1	-	Com	DVS	-	-	-	2V *1	N	-	-
19	DISON	29	Display on	1	-	Com	DVS	-	-	-	2V *1	N	-	-
20	CASET	2A	Column address set	5	4		Dir	-	Y	Y	-	Y	-	-
			(Column start address)			P2								
			(Column end address)			P4								
21	PASET	2B	Page address set	5	4		Dir	-	Y	Y	-	Y	-	-
			(Page start address)			P2								
			(Page end address)			P4								
22	RAMWR	2C	Memory write	3	-	Com	Dir	Dir	-	-	-	Y	-	-
23	RGBSET	2D	Color set	2	128	Each	Dir	Dir	Y	N	-	N	-	-
24	RAMRD	2E	Memory read	2	-	Com	Dir	Dir	-	-	-	Y	-	-
25	PTLAR	30	Partial area	3	4	P4	DVS	-	Y	Y	2V	N	-	-
26	VSCRDEF	33	Vertical scrolling definition	3	6	P6	DVS	-	Y	Y	2V	N	-	-
27	TEOFF	34	Tering effect line off	1	-	Com	DVS	-			2V	N	-	-
28	TEON	35	Tearing effect line on	4	1	P1	DVS	-	Y	Y	2V	N	-	-
29	MADCTL	36	Memory access control	2	1	P1			Y	N		N	-	-
			(B7-6)				Dir	LVS			-			
			(B5)				Dir	LVS			-			
			(B4-0)				DVS	LVS			2V			
30	VSCRSADD	37	Vertical scrolling start address	4	2	P2	DVS	-	Y	Y	2V *1	N	-	-
31	IDMOFF	38	Idle mode off	1	-	Com	DVS	-	-	-	4V *1	N	-	-
32	IDMON	39	Idle mode on	1	-	Com	DVS	-	-	-	4V *1	N	-	-
33	COLMOD	3A	Interface pixel format	2	1	P1	Dir	LVS	Y	N	-	Y	-	-
34	RDDATM	C4	Read display assemble test mode	2	3	Com	Dir	-	Y	Y	-	Y	-	-
35	RDID1	DA	Read ID1	2	2	Com	Dir	-	-	-	-	Y	Y	Y
36	RDID2	DB	Read ID2	2	2	Com	Dir	-	-	-	-	Y	Y	Y
37	RDID3	DC	Read ID3	2	2	Com	Dir	-	-	-	-	Y	Y	Y

*1: Refer to Section 8-7-2, “Display-Mode Transition Diagram.”

◇ Command Level 2: SENOP Area Command

No.	Command	HEX	Description	Type	Para	Com/Para			Para Reset		Com Exe	Cont in	ROM	Ref
						Reg	Act1	Act2	Hard	Soft				
38	DISCTL	B0	Display control	5	20		Dir	-	Y	Y	-	N	Y	Y
			(VBP)			P1								
			(Display Line)			P4								
			(VFP)			P6								
			(Others)			Each								
39	E2RCTL	B2	EEPROM control	2	2	Each	Dir	-	-	-	-	N	Y	Y
40	GCPSET0P R	F0	Gamma curve set 0	2	32	Each	Dir	-	-	-	-	N	Y	Y
41	GCPSET0N R	F1	Gamma curve set 0	2	32	Each	Dir	-	-	-	-	N	Y	Y
42	GCPSET0P GB	F2	Gamma curve set 0	2	32	Each	Dir	-	-	-	-	N	Y	Y
43	GCPSET0N GB	F3	Gamma curve set 0	2	32	Each	Dir	-	-	-	-	N	Y	Y
44	GCPSET1P R	F4	Gamma curve set 1	2	32	Each	Dir	-	-	-	-	N	Y	Y
45	GCPSET1N R	F5	Gamma curve set 1	2	32	Each	Dir	-	-	-	-	N	Y	Y
46	GCPSET1P GB	F6	Gamma curve set 1	2	32	Each	Dir	-	-	-	-	N	Y	Y
47	GCPSET1N GB	F7	Gamma curve set 1	2	32	Each	Dir	-	-	-	-	N	Y	Y
48	GCPSET2P R	F8	Gamma curve set 2	2	32	Each	Dir	-	-	-	-	N	Y	Y
49	GCPSET2N R	F9	Gamma curve set 2	2	32	Each	Dir	-	-	-	-	N	Y	Y
50	GCPSET2P GB	FA	Gamma curve set 2	2	32	Each	Dir	-	-	-	-	N	Y	Y
51	GCPSET2N GB	FB	Gamma curve set 2	2	32	Each	Dir	-	-	-	-	N	Y	Y
52	GCPSET3P	FC	Gamma curve set 3	2	32	Each	Dir	-	-	-	-	N	Y	Y
53	GCPSET3N	FD	Gamma curve set 3	2	32	Each	Dir	-	-	-	-	N	Y	Y
54	EPCTIN	B3	EEPROM control	2	1	Each	Dir	-	-	-	* 1	N	Y	Y
55	INIESC	B6	Initial escape	1	-	Com	Dir	-	-	-	-	Y	-	-
56	NOP2	B7	No operation2	1	-	Com	Dir	-	-	-	-	Y	-	-
57	MADDEF	B8	MADCTL Definition	2	1	P1			Y	N		N	Y	Y
			(B7-6)				Dir	-			-			
			(B5)				Dir	-			-			
			(B4-0)				DVS	-			2V			
58	STREAD2	B9	Read status2	1	2	Com	Dir	-	-	-	-	Y	-	-
59	LCDCDADEF	BB	LCDC I/F Display area definition	5	8		-	LVS	Y	Y	-	Y	-	-
			(Page start address)			P2								
			(Column start address)			P4								
			(Page end address)			P6								
			(Column end address)			P8								
60	VSYNCOUT	BC	External VXYNC disable	1	-	Com	DVS	-	-	-	1V	N	-	-
61	VSYNCIN	BD	External VXYNC enable	1	-	Com	DVS	-	-	-	1V	N	-	-
62	EVRSET	BE	EVR set	4	10	Each	Dir	-	Y	Y	-	N	-	-
63	MDLDEF	C0	LCD Module definition	2	3	Each	Dir	-	Y	Y	-	Y	Y	Y
64	PWRDEF	C1	Power definition	2	13	Each	Dir	-	-	-	-	N	Y	Y
65	IFMOD	C2	Interface mode select	2	1	Each	Dir	-	Y	N	-	Y	-	-
66	LCDCIF	D0	LCDC Interface	2	1	Each	Dir	-	Y	Y	-	N	-	-
67	EXVSYNCDEF	D1	External VSYNC definition	2	1	Each	DVS	-	Y	Y	1V	N	Y	Y
68	VPTLAR	C7	Vertical partial area	3	8		DVS	-	Y	Y	2V	N	-	-
69	VPTLIN	C8	Vertical partial mode in	1	-	Com	DVS	-	Y	Y	3V* 2	N	-	-
70	VPTLOUT	C9	Vertical partial mode out	1	-	Com	DVS	-	Y	Y	3V* 2	N	-	-

*1: Refer to Section 8-14, “EEPROM Control Function.”

◇ Command Level 3: Test Command

No.	Command	HEX	Description	Type	Para	Com/Para			Para Reset		Com Exe	Cont In	ROM	Ref
						Reg	Act1	Act2	Hard	Soft				
71	TESTOPT	C5	Test mode option	2	1	P1	Dir	-	Y	Y	-	Y	-	Esc
72	TESTPKG	CA	Test PKG-Mode On	1	-	Com	Dir	-	-	-	-	N	-	-
73	TESTREG	CB	Test mode Register read	4	3	P3	Dir	-	Y	Y	-	Y	-	Esc
74	TESTFSE	CC	Test mode Fuse	2	8	P1	Dir	-	Y	Y	-	Y	-	Esc
75	TESTMOD	CE	Test mode	2	1	P1	Dir	-	Y	Y	-	Y	-	Esc
76	TESTSUP	CF	Test mode TEst-support	2	1	P1	Dir	-	Y	Y	-	Y	-	Esc

- Type (Command Type)

  Command type

  Refer to Section 8-1-8, “Command Recognition and Parameter/Display Data Latch”

- Para (Parameter)

  Number of parameters

- Com/Para (Command/Parameter)

  “Reg (Register)” refers to the timing at which a parameter is stored in a register.

  It indicates how a previously input parameter or command will be handled when $\overline{CS}$ goes HIGH or another command is input during parameter input.

  P* indicates that when parameter P* is input, the parameter is stored in the internal register at that point in time.

  Each indicates that when any parameter is input, the parameter is stored in the internal register at that point in time.

  “Act1 (Action1)” refers to the timing at which the driver starts executing a recognized command.

  Dir (Direct) indicates that the command is executed on the rising edge of WR for command input (or the falling edge of $\overline{RD}$ for read).

  DVS (Display V-Sync) indicates that the command is executed synchronously with the frame next to that in which the command was input.

  DHS (Display H-Sync) indicates that the command is executed synchronously with the line next to that in which the command was input.

  “Act2 (Action2)” refers to the timing at which the driver starts executing a recognized command when the LCDC interface is being used.

  Dir (Direct) indicates that the command is executed on the rising edge of WR for command input.

  LVS (LCDC V-Sync) indicates that the command is executed in the LCDC vertical sync next to that in which the command was input.

  The commands marked with – in the table are not directly involved in VRAM accesses made from the LCDC interface. Therefore, the execution timing of these commands is the same as that for “Act1.”

- Para Reset (Parameter Reset)

  “Hard (Hardware reset)” refers to a hardware reset.

  “Soft (Software reset)” refers to a software reset.

  Y: The parameter is set to the initial value.

  N: The parameter retains its previous state without being set to the initial value.

  –: The parameter does not have an initial value.

  Refer to Section 8-4, “Reset.”

- Com Exe (Command Execution)

  Refers to the interval from when a command is input until a series of operations of the command (one frame displayed on the screen) is completed. A dash (–) denotes that the command does not have any particular series of operations or sequences.

  It includes a latch time of 1 V (Max.), which is the length of time before command execution starts after the command was input.

- Cont in (Continuation input)

  Successive writes of the same command. N: Prohibited; Y: Allowed.

- ROM (EEPROM)

  Parameters stored in the EEPROM

- Ref (Refresh)

  Parameters loaded when refreshed. Y: Loaded.

  Esc (Escape) refers to the parameters that are escaped when refreshed.

9-2. Command Details

The S1D19122 interprets and executes a command using only the internal timing, without relying on external clocks.

Note that $\overline{RD}$ and $\overline{WR}$ shown in the table are the read/write signals for the 80-series MPU parallel interface. These signals are described below.

0	Refers to stable LOW level	1	Refers to stable HIGH level
↑	Refers to rising edge of signal	↓0	Refers to falling edge of signal and subsequent stable LOW level
*	Refers to invalid bit. However, the bit must be stably HIGH or LOW.		

9-2-1. NOP (No Operation: 00h)

If NOP is received during a VRAM write or read, the write or read operation is terminated.

If NOP is received while a command that has a parameter value is being input, the parameter input state is terminated at the time NOP is received. The parameters input subsequently have no effect.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
NOP	0	1	↑	0	0	0	0	0	0	0	0	00	No operation

9-2-2. SWRESET (Software Reset: 01h)

This command executes a software reset. After power-on, a hardware reset should always be executed once.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
SWRESET	0	1	↑	0	0	0	0	0	0	0	1	01	Software reset

Refer to Section 8-4, “Reset.”

Refer to Section 8-13-1, “Auto Display-Off Sequence.”

9-2-3. RDDIDIF (Read Display Identification Information: 04h)

This command reads out the contents of ID1, ID2, and ID3 simultaneously.

When the LCDC interface is active while the parallel interface is being used, this command is interpreted as NOP.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDDIDIF	0	1	↑	0	0	0	0	0	1	0	0	04	Read display identification information
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	Manufacture ID								xx	Manufacture ID (RDID1)
P2	1	↓0	1	Module version								xx	Module version (RDID2)
P3	1	↓0	1	Module ID								xx	Module ID (RDID3)

9-2-4. RDDST (Read Display Status: 09h)

This command and the parameters that follow enable monitoring of the internal status of the IC. The status is read out immediately after $\overline{RD}$ input.

In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDDST	0	1	↑	0	0	0	0	1	0	0	1	09	Read display status
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	B31	B30	B29	B28	B27	B26	B25	B24	xx	Status
P2	1	↓0	1	B23	B22	B21	B20	B19	B18	B17	B16	xx	Status
P3	1	↓0	1	B15	B14	B13	B12	B11	B10	B9	B8	xx	Status
P4	1	↓0	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	Status

Bit	Description	Status	
B31	Booster Voltage Status	0:Off	1:On
B30	Page Address Order	0:Top to Bottom	1:Bottom to Top
B29	Column Address Order	0:Left to Right	1:Right to Left
B28	Page/Column Order	0:Column Scan	1:Page Scan
B27	Memory Scan Direction	0:Top to Bottom	1:Bottom to Top
B26	RGB/BGR Order	0:RGB	1:BGR
B25	Not Defined	0:Always	
B24	Not Defined	0:Always	
B23	Memory Scan & LCD Scan Direction	0: Agreement	1: Disagreement
B22	Color Mode		011: 4096 Colors
B21		101: 64K Colors	110: 262K Colors
B20		111: 16.8M Colors	Others: Not Defined
B19	Idle Mode On/Off	0:Off	1:On
B18	Partial Mode On/Off	0:Off	1:On
B17	Sleep In/Out	0:In	1:Out
B16	Display Normal Mode On/Off	0:Off	1:On
B15	Vertical Scrolling On/Off	0:Off	1:On
B14	Not Defined	0:Always	
B13	Inversion On/Off	0:Off	1:On
B12	Not Defined	0:Always	
B11	Not Defined	0:Always	
B10	Display On/Off	0:Off	1:On
B9	Tearing Effect Line On/Off	0:Off	1:On
B8	Not Defined	0:Always	
B7	Gamma Curve Selection	00: GC0	01: GC1
B6		10: GC2	11: GC3
B5	Tearing Effect Line Output Mode	0:Mode1	1:Mode2
B4	Not Defined	0:Always	
B3	Not Defined	0:Always	
B2	Not Defined	0:Always	
B1	Not Defined	0:Always	
B0	Not Defined	0:Always	

B30-23: MADCTL, B22-20: COLMOD

9-2-5. RDDPM (Read Display Power Mode: 0Ah)

This command enables monitoring of the internal status of the IC.

In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDDPM	0	1	↑	0	0	0	0	1	0	1	0	0A	Read display power mode
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	Status data

Bit	Description	Status	
B7	Booster Voltage Status	0:Off	1:On
B6	Idle Mode On/Off	0:Off	1:On
B5	Partial Mode On/Off	0:Off	1:On
B4	Sleep In/Out	0:In	1:Out
B3	Display Normal Mode On/Off	0:Off	1:On
B2	Display On/Off	0:Off	1:On
B1	Not Defined	0:Always	
B0	Not Defined	0:Always	

9-2-6. RDDMADCTL (Read Display MADCTL: 0Bh)

This command enables monitoring of the internal status of the IC.

In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDDMADCTL	0	1	↑	0	0	0	0	1	0	1	1	0B	Read display MADCTL
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	Status data

Bit	Description	Status	
B7	Page Address Order	0:Top to Bottom	1:Bottom to Top
B6	Column Address Order	0:Left to Right	1:Right to Left
B5	Page/Column Order	0:Column Scan	1:Page Scan
B4	Memory Scan Direction	0:Top to Bottom	1:Bottom to Top
B3	RGB/BGR Order	0:RGB	1:BGR
B2	Not Defined	0:Always	
B1	Not Defined	0:Always	
B0	Memory Scan & LCD Scan Direction	0: Agreement	1: Disagreement

9-2-7. RDDCOLMOD (Read Display Pixel Format: 0Ch)

This command enables monitoring of the internal status of the IC.

In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDDCOLMOD	0	1	↑	0	0	0	0	1	1	0	0	0C	Read display pixel format
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	Status data

Bit	Description	Status	
B7	Not Defined	0:Always	
B6	Not Defined	0:Always	
B5	Not Defined	0:Always	
B4	Not Defined	0:Always	
B3	Not Defined	0:Always	
B2	Color Mode		011: 4096 Colors
B1		101: 64K Colors	110: 262K Colors
B0		111: 16.8M Colors	Others: Not Defined

9-2-8. RDDIM (Read Display Image Mode: 0Dh)

This command enables monitoring of the internal status of the IC.

In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDDIM	0	1	↑	0	0	0	0	1	1	0	1	0D	Read display image mode
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	Status data

Bit	Description	Status	
B7	Vertical Scrolling On/Off	0:Off	1:On
B6	Not Defined	0:Always	
B5	Inversion On/Off	0:Off	1:On
B4	Not Defined	0:Always	
B3	Not Defined	0:Always	
B2	Gamma Curve Selection	000: GC0	001: GC1
B1		010: GC2	011: GC3
B0		Others: Not Defined	

9-2-9. RDDSM (Read Display Signal Mode: 0Eh)

This command enables monitoring of the internal status of the IC.

In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDDSM	0	1	↑	0	0	0	0	1	1	1	0	0E	Read display Signal mode
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	Status data

Bit	Description	Status	
B7	Tearing Effect Line On/Off	0:Off	1:On
B6	Tearing Effect Line output mode	0:Mode1	1:Mode2
B5	Not Defined	0:Always	
B4	Not Defined	0:Always	
B3	Not Defined	0:Always	
B2	Not Defined	0:Always	
B1	Not Defined	0:Always	
B0	Not Defined	0:Always	

9-2-10. RDDSDR (Read Display Self-Diagnostic Result: 0Fh)

This command enables monitoring of the internal status of the IC. Refer to Section 7, “Mounting and Wiring the IC on the Panel.” In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDDSDR	0	1	↑	0	0	0	0	1	1	1	1	0F	Read display self diagnostic result
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	Status data

Bit	Description	Status	
B7	Register Loading Detection	No problem: Status Inversion	
B6	Functionally Detection	No problem: Status Inversion	
B5	Chip Attachment Detection	No problem: Status Inversion	
B4	Display Glass Break Detection	No problem: Status Inversion	
B3	Not Defined	0:Always	
B2	Not Defined	0:Always	
B1	Not Defined	0:Always	
B0	Not Defined	0:Always	

9-2-11. SLPIN (Sleep In: 10h)

This command places the LCD module in a sleep state. SLPIN stops the oscillator circuit.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
SLPIN	0	1	↑	0	0	0	1	0	0	0	0	10	Sleep in

Refer to Section 8-7-4, “Display-Off Sequence.”

9-2-12. SLPOUT (Sleep Out: 11h)

This commands releases the LCD module from a sleep state. The oscillator circuit starts oscillating upon recognition of the sleep-out command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
SLPOUT	0	1	↑	0	0	0	1	0	0	0	1	11	Sleep out

Refer to Section 8-7-3, “Display-On Sequence.”

9-2-13. PTLON (Partial Mode On: 12h)

This command places the LCD module in partial-display mode. Use this display mode when the screen needs to be partially displayed (divided by line) for the purpose of reducing the power consumption of the chip.

The LCD module is made to exit partial display through the use of the NORON command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
PTLON	0	1	↑	0	0	0	1	0	0	1	0	12	Partial mode on

Refer to Section 8-8, “Display-Mode Switching Function.”

Refer to Section 8-11, “Partial-Display Function.”

9-2-14. NORON (Normal Display Mode On: 13h)

This command returns the LCD module to normal display mode.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
NORON	0	1	↑	0	0	0	1	0	0	1	1	13	Normal display mode on

The LCD module exits whichever mode it is in: partial display or scroll display.

Refer to Section 8-8, “Display-Mode Switching Function.”

9-2-15. DISINOFF (Display Inversion Off: 20h)

This command returns the LCD module from inverted display to normal display. The VRAM content does not change.

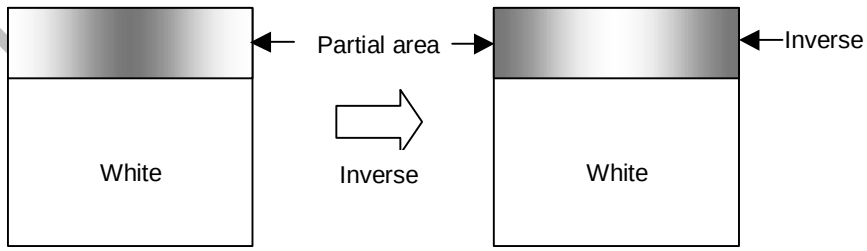
Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
DISINOFF	0	1	↑	0	0	1	0	0	0	0	0	20	Display inversion off

9-2-16. DISINV (Display Inversion On: 21h)

This command places the LCD module in inverted display. The VRAM content does not change.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
DISINV	0	1	↑	0	0	1	0	0	0	0	1	21	Display inversion on

The display-off area cannot be inverted during partial display. The LCD module is returned to normal display using the DISINOFF command.



9-2-17. GAMSET (Gamma Set: 26h)

This command and the parameters that follow enable selection of a gamma curve.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GAMSET	0	1	↑	0	0	1	0	0	1	1	0	26	Gamma set
P1	1	0	↑	B7	B6	B5	B4	B3	B2	B1	B0	xx	Gamma curve

P1: A gamma curve can be selected from a maximum of four types: GC0, GC1, GC2, or GC3.

B7	B6	B5	B4	B3	B2	B1	B0	Gamma curve
0	0	0	0	0	0	0	1	GC0
0	0	0	0	0	0	1	0	GC1
0	0	0	0	0	1	0	0	GC2
0	0	0	0	1	0	0	0	GC3

If any value outside the valid range is input by GAMSET, the command input is ignored and the LCD module retains its current state.

9-2-18. DISOFF (Display Off: 28h)

This command turns off the display in the entire display area.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
DISOFF	0	1	↑	0	0	1	0	1	0	0	0	28	Display off

Refer to Section 8-7-4, “Display-Off Sequence.”

9-2-19. DISON (Display On: 29h)

This command turns on the display in the entire display area. This command, if input during sleep, has no effect and the display is not turned on; however, the DISON register is turned on.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
DISON	0	1	↑	0	0	1	0	1	0	0	1	29	Display on

Refer to Section 8-7-3, “Display-On Sequence.”

9-2-20. CASET (Column Address Set: 2Ah)

This command and the parameters that follow enable specification of a column address area of the video memory when it is accessed.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
CASET	0	1	↑	0	0	1	0	1	0	1	0	2A	Column address set
P1	1	1	↑	*	*	*	*	*	*	*	SC8	xx	Start column (upper)
P2	1	1	↑	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	xx	Start column (lower)
P3	1	1	↑	*	*	*	*	*	*	*	EC8	xx	End column (upper)
P4	1	1	↑	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	xx	End column (lower)

Refer to Section 8-6, “Address Control Circuit and Video Memory.”

9-2-21. PASET (Page Address Set: 2Bh)

This command and the parameters that follow enable specification of a page address area of the video memory when it is accessed.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
PASET	0	1	↑	0	0	1	0	1	0	1	1	2B	Page adderss set
P1	1	1	↑	*	*	*	*	*	*	*	SP8	xx	Start page (upper)
P2	1	1	↑	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	xx	Start page (lower)
P3	1	1	↑	*	*	*	*	*	*	*	EP8	xx	End page (upper)
P4	1	1	↑	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	xx	End page (lower)

Refer to Section 8-6, “Address Control Circuit and Video Memory.”

9-2-22. RAMWR (Memory Write: 2Ch)

When the MPU writes data to the display memory, the memory is placed in a data-entry state by this command. The content of the video memory is rewritten by writing data to it immediately following this command. The address pointer moves according to the display-data format.

When the LCDC interface is active while the parallel interface is being used, this command is interpreted as NOP.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RAMWR	0	1	↑	0	0	1	0	1	1	0	0	2C	Memory write
Data	1	1	↑	Write data								xx	Write data

Refer to Section 8-6, “Address Control Circuit and Video Memory.”

9-2-23. RGBSET (Color Set: 2Dh)

This command and the parameters that follow enable the selection of gray scale levels in 65K, 4096, or 262K color mode. MDLDEF command can be selected 16.8M or 262K-color LUT.

◇16.8M-color mode (16.8M-color LUT)

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex		Description	
RGBSET	0	1	↑	0	0	1	0	1	1	0	1	2D	262KColor	65KColor	4096Color
P1	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(000000)	R(00000)	R(0000)
P2	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(000001)	R(00001)	R(0001)
:													:	:	:
P15	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(001110)	R(01110)	R(1110)
P16	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(001111)	R(01111)	R(1111)
P17	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(010000)	R(10000)	—
P18	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(010001)	R(10001)	—
:													:	:	:
P31	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(011110)	R(11110)	—
P32	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(011111)	R(11111)	—
P33	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(100000)	—	—
P34	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(100001)	—	—
:													:		
P63	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(111110)	—	—
P64	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(111111)	—	—
P65	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(000000)	G(000000)	G(0000)
P66	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(000001)	G(000001)	G(0001)
:													:	:	:
P79	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(001110)	G(001110)	G(1110)
P80	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(001111)	G(001111)	G(1111)
P81	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(010000)	G(010000)	—
P82	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(010001)	G(010001)	—
:													:	:	:
P127	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(111110)	G(111110)	—
P128	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(111111)	G(111111)	—
P129	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(000000)	B(00000)	B(0000)
P130	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(000001)	B(00001)	B(0001)
:													:	:	:
P143	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(001110)	B(01110)	B(1110)
P144	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(001111)	B(01111)	B(1111)
P145	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(010000)	B(10000)	—
P146	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(010001)	B(10001)	—
:													:	:	—
P159	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(011110)	B(11110)	—
P160	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(011111)	B(11111)	—
P161	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0		B(100000)	—	—
P162	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0		B(100001)	—	—
:													:		
P191	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(111110)	—	—
P192	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(111111)	—	—

In 262K color mode, set the R, G, and B gradations for P1-P64, P65-P128, and P129-P192, respectively.

In 65K color mode, set the R, G, and B gradations for P1-P32, P65-P128, and P12-P160, respectively. For the R and B gradations, set 32 gray scale levels selected from among 64 gray scale levels; for the G gradation, set 64 gray scale levels selected from among 64 gray scale levels. Input dummy data in the undefined areas (P33-P64 and P161-P192).

In 4096-color mode, set the R, G, and B gradations for P1-P16, P65-P80, and P129-P144, respectively. For each of the R, G, and B gradations, set 16 gray scale levels selected from among 64 gray scale levels. Input dummy data in the undefined areas (P17-P64, P81-P128, and P145-P192).

The command and parameters thus set are converted to data by an LUT before being written into the VRAM.

◇262K-color mode (262K-color LUT)

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex		Description
RGBSET	0	1	↑	0	0	1	0	1	1	0	1	2D	65KColor	4096Color
P1	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(00000)	R(0000)
P2	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(00001)	R(0001)
:													:	:
P15	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(01110)	R(1110)
P16	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(01111)	R(1111)
P17	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(10000)	—
P18	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(10001)	—
:													:	:
P31	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(11110)	—
P32	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	R(11111)	—
P33	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(000000)	G(0000)
P34	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(000001)	G(0001)
:													:	:
P47	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(001110)	G(1110)
P48	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(001111)	G(1111)
P49	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(010000)	—
P50	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(010001)	—
:													:	:
P95	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(111110)	—
P96	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	G(111111)	—
P97	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(00000)	B(0000)
P98	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(00001)	B(0001)
:													:	:
P111	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(01110)	B(1110)
P112	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(01111)	B(1111)
P113	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(10000)	—
P114	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(10001)	—
:													:	:
P127	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(11110)	—
P128	1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0	xx	B(11111)	—

In 65K color mode, set the R, G, and B gradations for P1-P32, P65-P128, and P12-P160, respectively. For the R and B gradations, set 32 gray scale levels selected from among 64 gray scale levels; for the G gradation, set 64 gray scale levels selected from among 64 gray scale levels. Input dummy data in the undefined areas (P33-P64 and P161-P192).

In 4096-color mode, set the R, G, and B gradations for P1-P16, P65-P80, and P129-P144, respectively. For each of the R, G, and B gradations, set 16 gray scale levels selected from among 64 gray scale levels. Input dummy data in the undefined areas (P17-P64, P81-P128, and P145-P192).

The command and parameters thus set are converted to data by an LUT before being written into the VRAM.

9-2-24. RAMRD (Memory Read: 2Eh)

When the MPU reads data from the display memory, the memory is placed in a data-readout state by this command. Data can be read out after one dummy read cycle is performed immediately following this command. The address pointer moves according to the display-data format.

When the LCDC interface is active while the parallel interface is being used, this command is interpreted as NOP.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RAMRD	0	1	↑	0	0	1	0	1	1	1	0	2E	Memory read
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
Data	1	↓0	1	Read data								xx	Read data

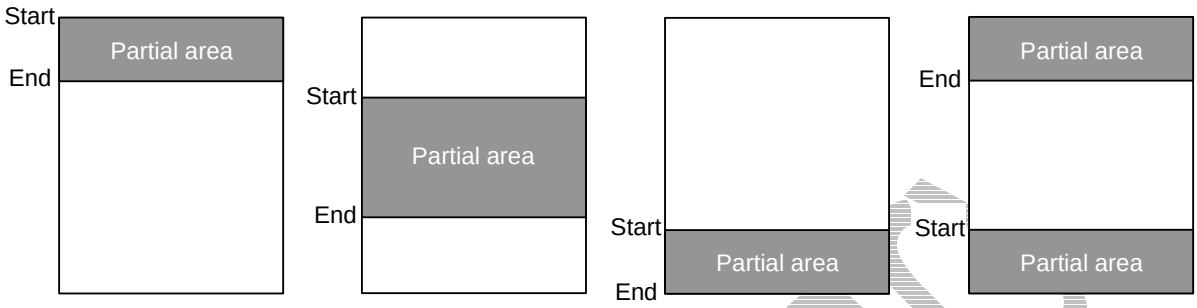
Refer to Section 8-6, “Address Control Circuit and Video Memory.”

9-2-25. PTLAR (Partial Area: 30h)

This command sets a partial-display area.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
PTLAR	0	1	↑	0	0	1	1	0	0	0	0	30	Partial area
P1	1	1	↑	*	*	*	*	*	*	*	SR8	xx	Start line (upper)
P2	1	1	↑	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	xx	Start line (lower)
P3	1	1	↑	*	*	*	*	*	*	*	ER8	xx	End line (upper)
P4	1	1	↑	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	xx	End line (lower)

Set the partial-display start line and end line. Count the start line from 0.



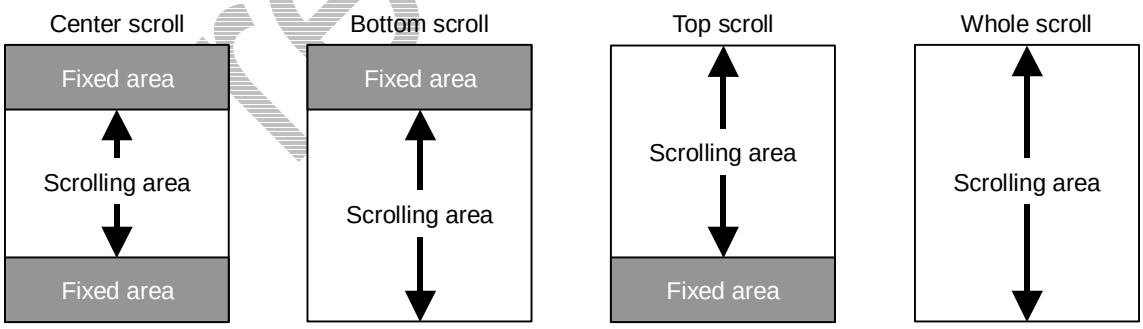
Refer to Section 8-9-5, “Partial/Scroll Areas and Scan Direction.”

Refer to Section 8-11, “Partial-Display Function.”

9-2-26. VSCRDEF (Vertical Scrolling Definition: 33h)

This command and the parameters that follow enable a vertical scroll area to be set.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
VSCRDEF	0	1	↑	0	0	1	1	0	0	1	1	33	Vertical scrolling definition
P1	1	1	↑	*	*	*	*	*	*	*	TF8	xx	Top fixed line number (U)
P2	1	1	↑	TF7	TF6	TF5	TF4	TF3	TF2	TF1	TF0	xx	Top fixed line number (L)
P3	1	1	↑	*	*	*	*	*	*	*	SA8	xx	Scrolling area number (U)
P4	1	1	↑	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	xx	Scrolling area number (L)
P5	1	1	↑	*	*	*	*	*	*	*	BF8	xx	Bottom fixed line number (U)
P6	1	1	↑	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0	xx	Bottom fixed line number (L)



Refer to Section 8-9-5, “Partial/Scroll Areas and Scan Direction.”

Refer to Section 8-10, “Area Scroll Display Function.”

9-2-27. TEOFF (Tearing-Effect Line Off: 34h)

This command deasserts the TE output that is the display timing output signal for the LCD panel, pulling it LOW.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
TEOFF	0	1	↑	0	0	1	1	0	1	0	0	34	Tearing effect line off

9-2-28. TEON (Tearing-Effect Line On: 35h)

This command and the parameters that follow assert TE output that is the display timing output signal for the LCD panel.

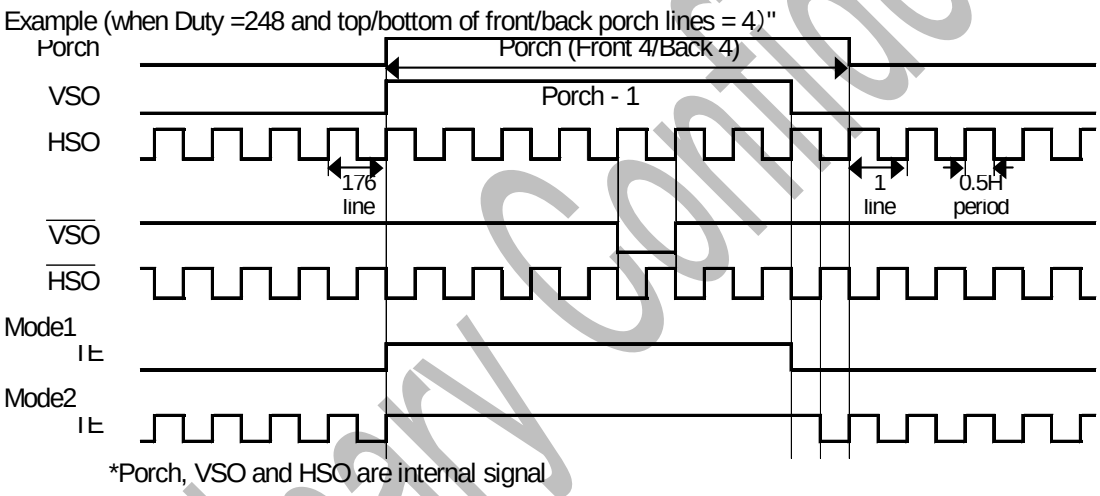
Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
TEON	0	1	↑	0	0	1	1	0	1	0	1	35	Tearing effect line on
P1	1	1	↑	*	*	*	*	*	*	*	B0	xx	Tearing effect mode

B0: Selects TE mode

B0	TE mode
0	Mode 1 (A VSO signal is output as TE output.)
1	Mode 2 (A merged signal of VSO and HSO is output as TE output.)

Refer to Section 8-17-2, “Display Synchronous Data Transfer by TE Signal.”

◇ TE signal



9-2-29. MADCTL (Memory Access Control: 36h)

This command and the parameters that follow are used to set the state of the video memory when it is accessed from the MPU, and the video memory state and common driver scan direction when data is read out to the LCD.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
MADCTL	0	1	↑	0	0	1	1	0	1	1	0	36	Memory access control
P1	1	1	↑	B7	B6	B5	B4	B3	*	*	B0	xx	Parameter

B0, B4: Changes the order of VRAM-to-LCD readout lines and changes the LCD scan direction

B4	B0	VRAM-to-LCD readout	LCD scan direction	Display state
0	0	Top to Bottom	Top to Bottom	Normal
0	1	Top to Bottom	Bottom to Top	Top/bottom inverted
1	0	Bottom to Top	Bottom to Top	Normal
1	1	Bottom to Top	Top to Bottom	Top/bottom inverted

B3: RGB array

The RGB array for the source output can be changed in accordance with the color-filter array on the LCD panel. The destination to which the display data written into the display memory is output can be changed. The position of G cannot be changed.

B3	RGB array
0	RGB, RGB, RGB, ⋯
1	BGR, BGR, BGR, ⋯

Refer to Section 8-15, “Versatile LCD Support.”

B5: VRAM access scan direction (host to VRAM)

When the MPU accesses the VRAM successively, this bit selects the vertical or horizontal address for address increment.

Refer to Section 8-6, “Address Control Circuit and Video Memory.”

B5	Scan direction
0	Horizontal direction
1	Vertical direction

B6: Horizontal address-0 position (host to VRAM)

This bit determines the position of horizontal address 0 of the video memory.

B6	Position of horizontal address 0
0	Left edge
1	Right edge

B7: Vertical address-0 position (host to VRAM)

This bit determines the position of vertical address 0 of the video memory.

B7	Position of vertical address 0
0	Top
1	Bottom

Refer to Section 8-9, “Command Definition Independent of the IC Mount Position.”

9-2-30. VSCRSADD (Vertical-Scrolling Start Address: 37h)

This command and the parameters that follow are used to set the VRAM address within the scroll area from which a vertical scroll starts.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
VSCRSADD	0	1	↑	0	0	1	1	0	1	1	1	37	Vertical scrolling start address
P1	1	1	↑	*	*	*	*	*	*	*	SP8	xx	Scroll start address(U)
P2	1	1	↑	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	xx	Scroll start address(L)

Do not set this address outside the scroll area. Execute the VSCRDEF command before issuing this command. Scrolling is enabled by setting the display start address.

Refer to Section 8-8, “Display-Mode Switching Function.”

Refer to Section 8-10, “Area Scroll Display Function.”

9-2-31. IDMOFF (Idle Mode Off: 38h)

When this command is input, the display mode is changed from 2-gray-scale-level display to 256-gray-scale-level display.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
IDMOFF	0	1	↑	0	0	1	1	1	0	0	0	38	Idle mode off

Refer to Section 8-8, “Display-Mode Switching Function.”

9-2-32. IDMON (Idle Mode On: 39h)

When this command is input, the display mode is changed to 2-gray-scale-level display, in which the amount of power consumed by the chip is reduced.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
IDMON	0	1	↑	0	0	1	1	1	0	0	1	39	Idle mode on

The MSB data is used for 2-gray-scale-level display. Input the IDMOFF command to exit this state.

Refer to Section 8-8, “Display-Mode Switching Function.”

9-2-33. COLMOD (Interface Pixel Format: 3Ah)

This command and the parameters that follow are used to set the color mode.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
COLMOD	0	1	↑	0	0	1	1	1	0	1	0	3A	Interface pixel format
P1	1	1	↑	*	*	*	*	*	B2	B1	B0	xx	Color

◇In case of 16.8M colors mode

B2	B1	B0	Color mode	Bit / Pixel	LUT
0	0	0	Undefined	-	-
0	0	1	Undefined	-	-
0	1	0	Undefined	-	-
0	1	1	4096 colors	12 Bit / Pixel	Used
1	0	0	Undefined	-	-
1	0	1	65K colors	16 Bit / Pixel	Used
1	1	0	262K colors	18 Bit / Pixel	Unused
1	1	1	16.8M colors	24 Bit / Picel	Unused

The LUT (lookup table) is set using RGBSET.

It is set 16.8M colors mode when it sets to undefined color mode.

◇In case of 262K colors mode

B2	B1	B0	Color mode	Bit / Pixel	LUT
0	0	0	Undefined	-	-
0	0	1	Undefined	-	-
0	1	0	Undefined	-	-
0	1	1	4096 colors	12 Bit / Pixel	Used
1	0	0	Undefined	-	-
1	0	1	65K colors	16 Bit / Pixel	Used
1	1	0	262K colors	18 Bit / Pixel	Unused
1	1	1	Undefined	-	-

The LUT (lookup table) is set using RGBSET.

It is set 262K colors mode when it sets to undefined color mode.

9-2-34. RDDATM (Read Display Assemble Test Mode: C4h)

This command enables monitoring of the LCD-module self-diagnosis result and the 513th byte of EEPROM data.

In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDDATM	0	1	↑	1	1	0	0	1	0	0	0	C4	Read display assemble test mode
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	B15	B14	B13	B12	B11	B10	B9	B8	xx	Status data
P2	1	↓0	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	Status data

Bit	Description	Status	
B15	Chip Attachment Detection (Left-Top Assemble Gap)	0:NG	1:No problem
B14	Chip Attachment Detection (Left-Bottom Assemble Gap)	0:NG	1:No problem
B13	Chip Attachment Detection (Left-Top/Left-side Bump Short)	0:NG	1:No problem
B12	Chip Attachment Detection (Right-Top Assemble Gap)	0:NG	1:No problem
B11	Chip Attachment Detection (Right-Bottom Assemble Gap)	0:NG	1:No problem
B10	Chip Attachment Detection (Right-Top/Right-side Bump Short)	0:NG	1:No problem
B9	Not Defined	0:Always	
B8	Glass Break Check	0:NG	1:No problem
B7	EEPROM Data	Address 513	Bit D7
B6	EEPROM Data	Address 513	Bit D6
B5	EEPROM Data	Address 513	Bit D5
B4	EEPROM Data	Address 513	Bit D4
B3	EEPROM Data	Address 513	Bit D3
B2	EEPROM Data	Address 513	Bit D2
B1	EEPROM Data	Address 513	Bit D1
B0	EEPROM Data	Address 513	Bit D0

Refer to Chapter 7, “Mounting and Wiring the IC on the Panel.”

9-2-35. RDID1 (Read ID1: DAh)

This command reads out the content of ID1, which is stored on an EEPROM. If no EEPROMs are found, 29h is output.
In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDID1	0	1	↑	1	1	0	1	1	0	1	0	DA	Read ID1
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	Manufacture ID								xx	Manufacture ID

9-2-36. RDID2 (Read ID2: DBh)

This command reads out the content of ID2, which is stored on an EEPROM. If no EEPROMs are found, 00h is output.
In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDID2	0	1	↑	1	1	0	1	1	0	1	1	DB	Read ID2
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	Module version								xx	Module version

9-2-37. RDID3 (Read ID3: DCh)

This command reads out the content of ID3, which is stored on an EEPROM. If no EEPROMs are found, 00h is output.
In case of the parallel interface and LCDC interfaces mode, this command is effective as the NOP command.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
RDID3	0	1	↑	1	1	0	1	1	1	0	0	DC	Read ID3
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	Module ID								xx	Module ID

9-2-38. DISCTL (Display Control: B0h)

This command and the parameters that follow are used to set display control.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
DISCTL	0	1	↑	1	0	1	1	0	0	0	0	B0	Display control
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	Vertical Back Porch
P2	1	1	↑	*	*	*	*	*	*	*	B20	xx	Display Line (U)
P3	1	1	↑	B37	B36	B35	B34	B33	B32	B31	B30	xx	Display Line (L)
P4	1	1	↑	B47	B46	B45	B44	B43	B42	B41	B40	xx	Vertical Front Porch
P5	1	1	↑	B57	B56	B55	B54	B53	B52	B51	B50	xx	1H period
P6	1	1	↑	*	*	*	B64	B63	B62	B61	B60	xx	Drive Mode
P7	1	1	↑	B77	B76	B75	B74	B73	B72	B71	B70	xx	PreBuffer On Timing
P8	1	1	↑	B87	B86	B85	B84	B83	B82	B81	B80	xx	PreBuffer Off Timing
P9	1	1	↑	B97	B96	B95	B94	B93	B92	B91	B90	xx	Revise On Timing
P10	1	1	↑	B107	B106	B105	B104	B103	B102	B101	B100	xx	Revise Off Timing
P11	1	1	↑	B117	B116	B115	B114	B113	B112	B111	B110	xx	DAC On Timing
P12	1	1	↑	B127	B126	B125	B124	B123	B122	B121	B120	xx	DAC Off Timing
P13	1	1	↑	B137	B136	B135	B134	B133	B132	B131	B130	xx	Gate On Timing
P14	1	1	↑	B147	B146	B145	B144	B143	B142	B141	B140	xx	Gate Off Timing
P15	1	1	↑	B157	B156	B155	B154	B153	B152	B151	B150	xx	Gamma Off Timing
P16	1	1	↑	B167	B166	B165	B164	B163	B162	B161	B160	xx	Inversion Mode
P17	1	1	↑	B177	B176	B175	B174	B173	B172	B171	B170	xx	SDR Drive Mode
P18	1	1	↑	B187	B186	B185	B184	B183	B182	B181	B180	xx	Idle Refresh Mode
P19	1	1	↑	*	B196	B195	B194	B193	B192	B191	B190	xx	Idle Drive Mode
P20	1	1	↑	B207	B206	B205	B204	B203	B202	B201	B200	xx	Idle VFPLine

Make sure all settings are made before SLPOUT. Do not change the settings while in display mode.

P1: Sets the vertical back-porch interval (VBP)

Set the back-porch interval of the vertical sync signal for the TFT drive. If the back-porch interval to be set is 5H, set 5 for this parameter.

B17	B16	B15	B14	B13	B12	B11	B10	Back-porch interval	Accepted setting range
0	0	0	0	0	1	0	1	e.g.) 5H	1 to 255

P2: Sets the upper byte indicating the number of display lines (VDISP)

B27	B26	B25	B24	B23	B22	B21	B20	Number of display lines	Accepted setting range
0	0	0	0	0	0	0	0	e.g.) 0	0

P3: Sets the lower byte indicating the number of display lines (VDISP)

If the number of display lines to be set is 240, set 240 for this parameter.

B37	B36	B35	B34	B33	B32	B31	B30	Number of display lines	Accepted setting range
1	0	1	1	0	0	1	1	eg.) 240 line	1 to 240

Refer to Section 8-6-1, “VRAM Access Scan Direction and VRAM Address Mapping.”

P4: Sets the vertical front-porch interval (VFP)

Set the front-porch interval of the vertical sync signal for the TFT drive. If the front-porch interval to be set is 10H, set 10 for this parameter.

B47	B46	B45	B44	B43	B42	B41	B40	Vertical front-porch interval	Accepted setting range
0	0	0	0	1	0	1	0	e.g.) 10H	1 to 255

P5: Sets the number of clock cycles that comprise the 1H interval

Set the 1H interval that serves as the fundamental timing of the TFT drive based on the number of fundamental clock cycles (internal oscillator circuit or external clock input). If the number of 1H clock cycles to be set is 100, set 100 for this parameter.

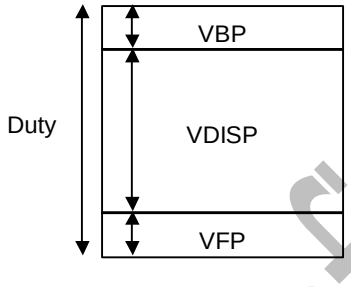
B57	B56	B55	B54	B53	B52	B51	B50	1H interval	Accepted setting range
0	1	1	0	0	1	0	0	e.g.) 100 clock cycles	33 to 255

The drive duty is determined by the vertical back porch, the number of display lines, and the vertical front porch that have been set.

1 / Duty = VBP + VDISP + VFP

In addition, the refresh rate of display (frame frequency) must be taken into consideration when setting the 1H interval and the drive duty.

Refer to Section 8-9-4, “LCD Readout Scan Direction and Gate Scan Direction.”



B64: Specifies whether the gamma resistor should be separated

B64	Gamma-resistor separation
0	The gamma resistor remains connected during the 1H interval.
1	The gamma resistor is separated with P15 timing during the 1H interval. The gamma resistor is connected again at the beginning of the next 1H.

B63-B62: Sets the source drive mode

Set the prebuffer operation mode for source drive during the 1H interval.

B63	B62	Source drive mode
0	0	Prebuffer drive → Gray scale correction drive → DAC drive
0	1	Prebuffer drive → Gray scale correction drive
1	0	Prebuffer drive → DAC drive
1	1	Prohibited

B61-B60: Sets the precharge method

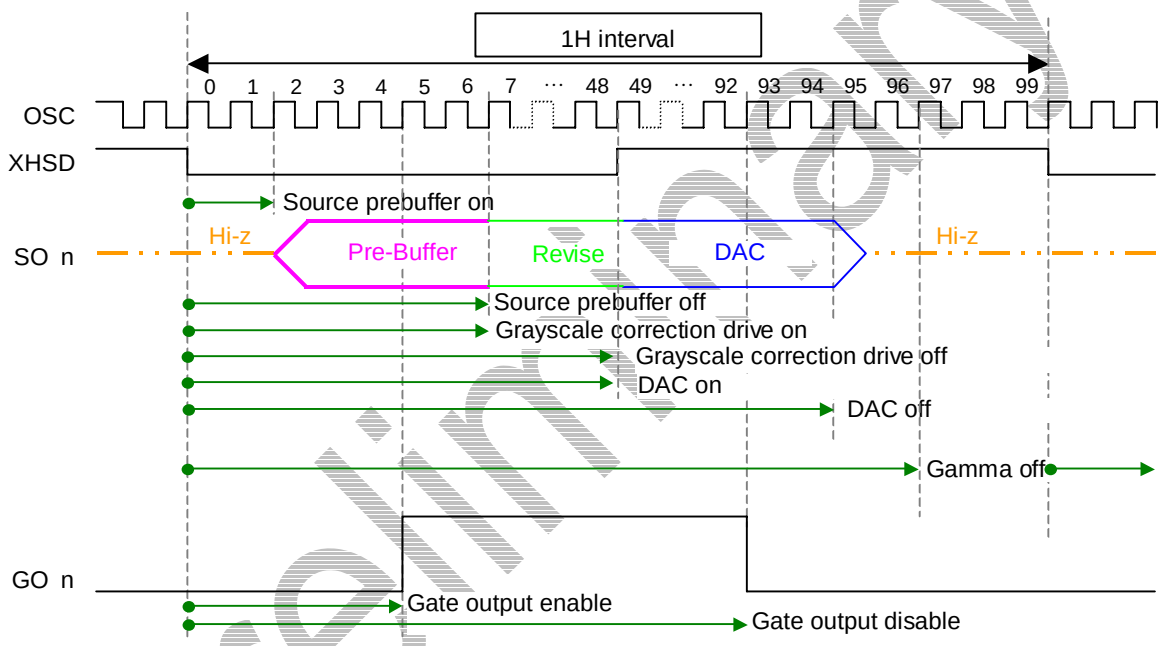
Set the method for precharging the source lines at a constant voltage before the gray scale voltages for the source drive are output.

B61	B60	Precharge mode
0	0	Precharge mode 1
0	1	Precharge mode 2
1	0	Not precharged
1	1	Prohibited

P7-P15: Sets the TFT drive method

Setting the drive timing enables setting of the most suitable output timing for the characteristics of the LCD panel connected. Set each timing based on the number of clock cycles from the top of the line.

Bit	Accepted setting range	Symbol	Description
(B57-B50)	1 to 255	1HWD	1H interval
B77-B70	1 to 255	SOON	Source output prebuffer on
B87-B80	1 to 255	SOOF	Source output prebuffer off
B97-B90	1 to 255	SRON	Source gray scale correction drive on
B107-B100	1 to 255	SROF	Source gray scale correction drive off
B117-B110	1 to 255	DAON	DAC drive on
B127-B120	1 to 255	DAOF	DAC drive off
B137-B130	1 to 255	GOEN	Gate output enable
B147-B140	1 to 255	GODS	Gate output disable
B157-B150	1 to 255	GMOF	Gamma-resistor separation



However, each set value must maintain the relationship specified below.

$0 < SOON < SOOF \leq SRON < SROF \leq DAON < DAOF \leq GMOF < 1HWD$

$0 < GOEN < GODS < 1HWD$

The $\overline{HSD}$ signal is output at a 50% duty cycle in the 1H interval. If the set value is an odd number, the LOW-level width is 1 clock cycle shorter.

P16: Alternating drive

B162-B160: Sets alternating-drive mode

B162	B161	B160	Alternating-drive mode	V_{COM}
0	0	0	Frame-inversion drive	Rectangular
0	0	1	Prohibited	-
0	1	0	Line-inversion drive	Rectangular
0	1	1	Prohibited	-
1	0	0	Prohibited	-
1	0	1	Prohibited	-
1	1	0	Prohibited	-
1	1	1	Prohibited	-

B163: Specifies the operation polarity of the adder for the FRC function

B163	FRC operation
0	FRC adder operation, normal
1	FRC adder operation, reversed

B166-B164: Sets the number of inverted lines during line-inversion driving to (number of lines – 1). The settings of these bits have no effect during frame-inversion driving.

B166	B165	B164	Number of inverted lines	Accepted setting range
0	1	1	e.g.) 4 lines	0 to 7

B167: Specifies the TFT panel used

B167	TFTLCD
0	Normally White
1	Normally Black

B177-B176: Sets the damping resistance of the source driver

B177	B176	Damping resistance
0	0	Prohibited
0	1	20kΩ
1	0	30kΩ
1	1	12kΩ

B175: Specifies whether the settings of power-consumption mode should be used for the gray scale correction circuit

B175	Settings of power-consumption mode
0	Disable the settings of B174, 173, 172, and 171.
1	Enable the settings of B174, 173, 172, and 171.

If it is necessary to set B174-173 or B172-171 described below to other than (0,0), set B175 to 1 and B27 for EVRSET to 1. This setting may help reduce the power consumption in the chip, depending on the gamma curves. Before making this setting, however, examine the display condition to confirm its effectiveness.

B174-B173: Sets the power-consumption mode of the gray scale correction circuit during intermediate gray scale display

B174	B173	Power consumption
0	*	Large (recommended)
1	0	Small (test mode)
1	1	Medium (test mode)

If it is necessary to set B174 to other than 1, set the above-mentioned B175 to 1 and B27 for EVRSET to 1.

B172-B171: Sets the power-consumption mode of the source prebuffer during intermediate gray scale display

B172	B171	Power consumption
0	*	Large (recommended)
1	0	Small (test mode)
1	1	Medium (test mode)

If it is necessary to set B172 to other than 1, set the above-mentioned B175 to 1 and B27 for EVRSET to 1.

B170: Sets the drive capacity of the source driver

B170	Source-driver drive capacity
0	Normal capacity
1	High drive capacity

B187: Sets the drive mode of the display area and non-display area for partial display

B187	Display area	Non-display area (during refresh)	Non-display area (during non-refresh)
0	Frame inverted	Frame inverted	Frame inverted
1	Depends on the set drive mode	Depends on the set drive mode	Hi-Z

If used in combination with Idle, however, this drive mode depends on how B186 is set below.

B186: Sets the drive mode of the display during Idle

B186	Display area
0	Frame inverted
1	Depends on the set drive mode

B185-B180: Sets the refresh period of the partial non-display area

B185	B184	B183	B182	B181	B180	Refresh period	Accepted setting range
0	0	0	1	0	0	e.g.) 5 frames	0 to 63

Set to the number (refresh periods – 1). B180 is fixed at 0 regardless of what value is set. Therefore, refresh is only possible in odd-numbered frames.

B196: Setting B196 to 1 causes the electronic VOL data is sent again to the power supply circuit in each 1H.

B196	Electronic VOL data refresh
0	Non refresh
1	Refresh in each 1H

B195: Setting B192 to 1 causes the source timing in which the booster power supply is connected with gamma resistance is selected.

B195	Gamma connected timing
0	BP start timing
1	Display start timing

B194-B193: Sets the drive mode in the porch interval

B194	B193	Frequency division setting
0	0	Depends on the set drive mode
0	1	Frame inverted
1	*	Settings prohibited

B192-B190: Setting B192 to 1 causes the source prebuffer drive interval to be reduced by a fixed value when a clock frequency divide ratio for Idle display is set for B191-B190.

B192	Prebuffer drive interval
0	As set
1	Set value – fixed value

B191	B190	Fixed value
0	0	0
0	1	2
1	0	4
1	1	8

B191-B190: Sets the clock frequency divide ratio for Idle display

B191	B190	Frequency divide ratio
0	0	1/1
0	1	1/2
1	0	1/4
1	1	1/8

P20: Sets the value to the number of VFP lines in IDLE mode

This setting enables the power consumption of the chip to be lowered by reducing the frame frequency in IDLE mode.

B207	B206	B205	B204	B203	B202	B201	B200	VFP added value	Accepted setting range
0	1	1	0	0	1	0	0	e.g.) 100 lines	1 to 255

9-2-39. E2RCTL (EEPROM Control: B2h)

This command and the parameters that follow are used to set EEPROM control.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
E2RCTL	0	1	↑	1	0	1	1	0	0	1	0	B2	EEPROM control
P1	1	1	↑	B17	*	*	B14	*	*	*	*	xx	Setup
P2	1	1	↑	*	*	*	*	*	*	*	*	xx	Reserved

B14: Shortens the initialize interval to set using DISCTL.

B14	Initialize shortening
0	No shortening
1	Shortening

B17: Normally, when INISEL = HIGH, readout to EEPROM is performed by SLPOUT command; this bit disables such EEPROM readout.

B17	EEPROM readout setting
0	Normal operation
1	Disables EEPROM readout when INISEL = HIGH

9-2-40. GCPSET0P R (Gamma Curve Set 0: F0h)

This command and the parameters that follow are used to set the position of the positive GC0.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET0P R	0	1	↑	1	1	1	1	0	0	0	0	F0	Gamma curve set 0
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the positive GC0 (red)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-41. GCPSET0N R (Gamma Curve Set 0: F1h)

This command and the parameters that follow are used to set the position of the negative GC0.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET0N R	0	1	↑	1	1	1	1	0	0	0	1	F1	Gamma curve set 0
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the negative GC0 (red)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-42. GCPSET0P GB (Gamma Curve Set 0: F2h)

This command and the parameters that follow are used to set the position of the positive GC0.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET0P GB	0	1	↑	1	1	1	1	0	0	1	0	F2	Gamma curve set 0
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the positive GC0 (green/blue)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-43. GCPSET0N GB (Gamma Curve Set 0: F3h)

This command and the parameters that follow are used to set the position of the negative GC0.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET0N GB	0	1	↑	1	1	1	1	0	0	1	1	F3	Gamma curve set 0
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the negative GC0 (green/blue)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

The setting procedure is as follows: Sequentially, beginning with the 0th gray scale level, write data “1” to the bit for each resistor-ladder position selected. 65 bits in total must be set to 1.

9-2-44. GCPSET1P R (Gamma Curve Set 1: F4h)

This command and the parameters that follow are used to set the position of the positive GC1.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET1P R	0	1	↑	1	1	1	1	0	1	0	0	F4	Gamma curve set 1
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the positive GC1 (red)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-45. GCPSET1N R (Gamma Curve Set 1: F5h)

This command and the parameters that follow are used to set the position of the negative GC1.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET1N R	0	1	↑	1	1	1	1	0	1	0	1	F5	Gamma curve set 1
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	Xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	Xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	Xx	(P327) – (P320)

P1-P32: Sets the negative GC1 (red)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-46. GCPSET1P GB (Gamma Curve Set 1: F6h)

This command and the parameters that follow are used to set the position of the positive GC1.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET1P GB	0	1	↑	1	1	1	1	0	1	1	0	F6	Gamma curve set 1
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the positive GC1 (green/blue)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-47. GCPSET1N GB (Gamma Curve Set 1: F7h)

This command and the parameters that follow are used to set the position of the negative GC1.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET1N GB	0	1	↑	1	1	1	1	0	1	1	1	F7	Gamma curve set 1
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the negative GC1 (green/blue)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-48. GCPSET2P R (Gamma Curve Set 2: F8h)

This command and the parameters that follow are used to set the position of the positive GC2.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET2P R	0	1	↑	1	1	1	1	1	0	0	0	F8	Gamma curve set 2
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the positive GC2 (red)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-49. GCPSET2N R (Gamma Curve Set 2: F9h)

This command and the parameters that follow are used to set the position of the negative GC2.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET2N R	0	1	↑	1	1	1	1	1	0	0	1	F9	Gamma curve set 2
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the negative GC2 (red)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-50. GCPSET2P GB (Gamma Curve Set 2: FAh)

This command and the parameters that follow are used to set the position of the positive GC2.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET2P GB	0	1	↑	1	1	1	1	1	0	1	0	FA	Gamma curve set 2
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the positive GC2 (green/blue)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-51. GCPSET2N GB (Gamma Curve Set 2: FBh)

This command and the parameters that follow are used to set the position of the negative GC2.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET2N GB	0	1	↑	1	1	1	1	1	0	1	1	FB	Gamma curve set 2
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the negative GC2 (green/blue)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-52. GCPSET3P (Gamma Curve Set 3: FCh)

This command and the parameters that follow are used to set the position of the positive GC3.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET3P	0	1	↑	1	1	1	1	1	1	0	0	FC	Gamma curve set 3
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the positive GC3 (red/green/blue)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-53. GCPSET3N (Gamma Curve Set 3: FDh)

This command and the parameters that follow are used to set the position of the negative GC3.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
GCPSET3N	0	1	↑	1	1	1	1	1	1	0	1	FD	Gamma curve set 3
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	(P17) – (P10)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	(P27) – (P20)
:													
P32	1	1	↑	B327	B326	B325	B324	B323	B322	B321	B320	xx	(P327) – (P320)

P1-P32: Sets the negative GC3 (red/green/blue)

Always make sure that 65 bits in total have been set to 1. The set value takes effect after SLPOUT.

9-2-54. EPCTIN (EEPROM Control: B3h)

This command and the parameters are used to enter EEPROM control mode.

The parameters are used to select read/write mode, and transfer the access code. Immediately after the input of these parameters, the S1D19122 outputs the BCK, BDATA, and BRST signals, or enters pin control mode.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
EPCTIN	0	1	↑	1	0	1	1	0	0	1	1	B3	EEPROM control
P1	1	1	↑	*	*	*	*	*	*	B11	B10	xx	Read/Write mode
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	Address

B11-B10: Selects the control method and read/write mode

B11	B10	Read/write
1	0	Read
0	1	Write (1 address)
1	1	Page write (4 addresses)

◇ Pin control method

Controlled directly by the $\overline{WR}$ ($\overline{RD}$, A0) and D0 pins

◇ In write mode

Write mode can be used for pin control only. The S1D19122 assigns the signals it received via the $\overline{WR}$ ($\overline{RD}$, A0) and D0 pins to the BRST, BCK, and BDATA pins. This enables the EEPROM to be controlled using external devices.

◇ During read

EEPROM read is controlled by the $\overline{WR}$ ($\overline{RD}$, A0) and D0 pins, as in write mode described above.

B23-B20: Access-code input

In both read and write modes, an access code is output from the BDATA pin according to the $\overline{WR}$ ($\overline{RD}$, A0) input timing.

Reference: Access code

B27	B26	B25	B24	B23	B22	B21	B20	Access start address
*	0	0	0	0	0	0	0	0
				:				:
*	1	1	1	1	1	1	1	127

Refer to Section 8-14, “EEPROM Control Function.”

9-2-55. INIESC (Initial Escape: B6h)

This command is used to exit initialize/refresh operation.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
INIESC	0	1	↑	1	0	1	1	0	1	1	0	B6	Initial escape

If this command is issued during initialize operation, the initialize operation under way is aborted.

If initialization is aborted using this command, the commands that would otherwise be set by EEPROM readout should be set by the user by issuing each command manually.

9-2-56. NOP2 (No Operation 2: B7h)

This command is irrelevant to the driver operation.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
NOP2	0	1	↑	1	0	1	1	0	1	1	1	B7	No operation2

9-2-57. MADDEF (MADCTL Definition: B8h)

This command and the parameters that follow define the method by which the parameter value of MADCTL will be used inside the IC.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
MADDEF	0	1	↑	1	0	1	1	1	0	0	0	B8	MADCTL definition
P1	1	1	↑	B7	B6	B5	B4	B3	*	*	B0	xx	Parameter

The LCD-module manufacturer should disclose the set value of MADCTL, the top/bottom and left/right definitions of which will not change irrespective of the difference in IC mount positions on the LCD panel, or should ensure that the set value is written in the EEPROM.

P1:

B7 to B3, B0: Defines the method by which each bit of MADCTL (parameter) will be used inside the IC

The set value of MADCTL actually used inside the IC is derived by exclusive OR'ing each bit in the MADCTL and MADDEF parameters together.

Refer to Section 8-9, "Command Definition Independent of the IC Mount Position."

B2: Switch "R and B" data which write to VRAM

B2	RAM write function
0	No switch R data <->B data
1	R data <-> B data switch

Note:

* In case of read function, R and B switch function is not available.

* Readout data is switched between R and D after writing RAM data, when set to "B2 = 1" .

◇ In case of RG-gamma and B-gamma adjustment selected

MADDEF B2 = "1": selects switch between R data and B data

RAM and source output circuit are fixed. Then gamma R and gamma GB are gamma RG and gamma B combination.

Source output circuit and connection of pins need to set to RGB and BGR array contrary to usually.

Ex) RGB array: MADDEF B2 = "1" and MADCTL B3 = "1"

BGR array: MADDEF B2 = "1" and MADCTL B3 = "0"

*Gamma adjustment can be changed to RG/B gamma from R/GB gamma if used this function.

9-2-58. STREAD2 (Read Status 2: B9h)

This command enables monitoring of the internal status.

When the LCDC interface is active while the parallel interface is being used, this command is interpreted as NOP.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
STREAD2	0	1	↑	1	0	1	1	1	0	0	1	B9	Read status2
DD	1	↓0	1	DD	DD	DD	DD	DD	DD	DD	DD	xx	Dummy read
P1	1	↓0	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	Status data

Bit	Description	Status	
B7	Oscillator circuit	0:Off	1:On
B6	Internal operation for the LCD drive	0: Not operating	1: Operating
B5	Power-supply-on sequence	0: Not operating	1: Operating
B4	Power-supply stabilization period	0: Not stable	1: Stable
B3	Power-supply-off sequence	0: Not operating	1: Operating
B2	—	—	—
B1	—	—	—
B0	EEPROM access status	0: Not accessed	1: Accessed

9-2-59. LCDCDADEF (LCDC Interface Display Area Definition: BBh)

This command and the parameters that follow enable simultaneous specification of the page and column areas of the video memory when accessed from the LCDC side.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
LCDCDADEF	0	1	↑	1	0	1	1	1	0	1	1	BB	LCDC I/F Display area definition
P1	1	1	↑	*	*	*	*	*	*	*	SP8	xx	Start page (upper)
P2	1	1	↑	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	xx	Start page (lower)
P3	1	1	↑	*	*	*	*	*	*	*	SC8	xx	Start column (upper)
P4	1	1	↑	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	xx	Start column (lower)
P5	1	1	↑	*	*	*	*	*	*	*	EP8	xx	End page (upper)
P6	1	1	↑	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	xx	End page (lower)
P7	1	1	↑	*	*	*	*	*	*	*	EC8	xx	End column (upper)
P8	1	1	↑	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	xx	End column (lower)

Refer to Section 8-6, “Address Control Circuit and Video Memory.”

9-2-60. VSYNCOUT (External VSYNC Disable: BCh)

This command is used to exit external VSYNC synchronized display mode.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
VSYNCOUT	0	1	↑	1	0	1	1	1	1	0	0	BC	External VSYNC disable

Refer to Section 8-17-3, “Display Synchronous Data Transfer by External VSYNC.”

9-2-61. VSYNCIN (External VSYNC Enable: BDh)

This command is used to enter external VSYNC synchronized display mode.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
VSYNCIN	0	1	↑	1	0	1	1	1	1	0	1	BD	External VSYNC enable

Refer to Section 8-17-3, “Display Synchronous Data Transfer by External VSYNC.”

9-2-62. EVRSET (EVR Set: BEh)

This command and the parameters that follow set internal power-supply control.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
EVRSET	0	1	↑	1	0	1	1	1	1	1	0	BE	EVR set
P1	1	1	↑	*	*	*	*	*	B12	B11	B10	xx	V_{LDO}
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	V_{DDHS}
P3	1	1	↑	B37	B36	B35	B34	B33	B32	B31	B30	xx	V_{COMH}
P4	1	1	↑	*	*	*	B44	B43	B42	B41	B40	xx	V_{COMW}
P5	1	1	↑	*	*	*	B54	B53	B52	B51	B50	xx	V_{DDRH}
P6	1	1	↑	*	*	*	B64	B63	B62	B61	B60	xx	V_{ONREG}
P7	1	1	↑	*	*	*	B74	B73	B72	B71	B70	xx	V_{OFREG}
P8	1	1	↑	*	*	*	*	*	*	*	*	xx	Not defined
P9	1	1	↑	*	*	*	*	*	*	*	*	xx	Not defined
P10	1	1	↑	*	*	*	*	*	*	*	*	xx	Not defined

Make sure these settings are made before SLPOUT. Do not change the settings while in display mode. The set value takes effect after SLPOUT.

P1: Turns the V_{LDO} (main reference voltage) regulator on/off and sets the 1st-booster multiplying factor

Bit	Description	Status	
B2	Sets V_{LDO} power-supply output when the 1st booster is set to ×3	0:2.0V	1:2.07V
B1	Sets the 1st-booster multiplying factor	0: ×2	1: ×3
B0	Sets V_{LDO} power-supply operation	0: Idle	1: Operating

P2: Sets the output voltage of the V_{DDHS} (source drive voltage) regulator

B27: Selects definition of settings for V_{DDHS} output voltage.

B27	V_{DDHS} output-voltage control
0	Set value in B24-B20 is effective
1	V_{DDHS} = V_{DDRH} set voltage + offset voltage (set value of B26-B25)

B26-B25: Sets an offset voltage that is used to set the V_{DDHS} output voltage

B26	B25	Offset-voltage setting
0	0	0.3V
0	1	0.5V
1	0	0.7V
1	1	Setting prohibited

B24-B20: Sets the output voltage of the V_{DDHS} (source drive voltage) regulator

P3: Sets the output voltage of the V_{COMH} (common electrode HIGH voltage) regulator

P4: Sets the output voltage of the V_{COMW} (common electrode amplitude) voltage regulator

P5: Sets the output voltage of the V_{DDRH} (gamma generation voltage) regulator

P6: Sets the output voltage of the V_{ONREG} (3rd booster voltage) regulator

P7: Sets the output voltage of the V_{OFREG} (4th booster voltage) regulator

P8: Not defined

P9: Not defined

P10: Not defined

Use the electronic volume control to set the output voltage of each voltage regulator. Refer to the table on the next page for the output voltage of each regulator.

◇ Relationship between electronic volume control and regulator output voltages

EVR	V_{COMH}	V_{COMW}	V_{DDRH}	V_{DDHS}	V_{ONREG}	V_{OFREG}
0	2	1.5	2.4	2.4	2.4	2.4
1	2.02	1.55	2.5	2.5	2.5	2.5
2	2.04	1.6	2.6	2.6	2.6	2.6
3	2.06	1.65	2.7	2.7	2.7	2.7
4	2.08	1.7	2.8	2.8	2.8	2.8
5	2.1	1.75	2.9	2.9	2.9	2.9
6	2.12	1.8	3	3	3	3
7	2.14	1.85	3.1	3.1	3.1	3.1
8	2.16	1.9	3.2	3.2	3.2	3.2
9	2.18	1.95	3.3	3.3	3.3	3.3
10	2.2	2	3.4	3.4	3.4	3.4
11	2.22	2.05	3.5	3.5	3.5	3.5
12	2.24	2.1	3.6	3.6	3.6	3.6
13	2.26	2.15	3.7	3.7	3.7	3.7
14	2.28	2.2	3.8	3.8	3.8	3.8
15	2.3	2.25	3.9	3.9	3.9	3.9
16	2.32	2.3	4	4	4	4
17	2.34	2.35	4.1	4.1	4.1	4.1
18	2.36	2.4	4.2	4.2	4.2	4.2
19	2.38	2.45	4.3	4.3	4.3	4.3
20	2.4	2.5	4.4	4.4	4.4	4.4
21	2.42	2.55	4.5	4.5	4.5	4.5
22	2.44	2.6	4.6	4.6	4.6	4.6
23	2.46	2.65	4.7	4.7	4.7	4.7
24	2.48	2.7	4.8	4.8	4.8	4.8
25	2.5	2.75	4.9	4.9	4.9	4.9
26	2.52	2.8	5	5	5	5
27	2.54	2.85	5.1	5.1	5.1	5.1
28	2.56	2.9	5.2	5.2	5.2	5.2
29	2.58	2.95	5.3	5.3	5.3	5.3
30	2.6	3	5.4	5.4	5.4	5.4
31	2.62	3.05	5.5	5.5	5.5	5.5
32	2.64					
33	2.66					
34	2.68					
35	2.7					
36	2.72					
37	2.74					
38	2.76					
39	2.78					
40	2.8					
41	2.82					
42	2.84					
43	2.86					
44	2.88					
45	2.9					
46	2.92					
47	2.94					
48	2.96					
49	2.98					
50	3					
51	3.02					
52	3.04					
53	3.06					
54	3.08					
55	3.1					
56	3.12					
57	3.14					
58	3.16					
59	3.18					
60	3.2					
61	3.22					
62	3.24					
63	3.26					

EVR	V_{COMH}
64	3.28
65	3.3
66	3.32
67	3.34
68	3.36
69	3.38
70	3.4
71	3.42
72	3.44
73	3.46
74	3.48
75	3.5
76	3.52
77	3.54
78	3.56
79	3.58
80	3.6
81	3.62
82	3.64
83	3.66
84	3.68
85	3.7
86	3.72
87	3.74
88	3.76
89	3.78
90	3.8
91	3.82
92	3.84
93	3.86
94	3.88
95	3.9
96	3.92
97	3.94
98	3.96
99	3.98
100	4
101	4.02
102	4.04
103	4.06
104	4.08
105	4.1
106	4.12
107	4.14
108	4.16
109	4.18
110	4.2
111	4.22
112	4.24
113	4.26
114	4.28
115	4.3
116	4.32
117	4.34
118	4.36
119	4.38
120	4.4
121	4.42
122	4.44
123	4.46
124	4.48
125	4.5
126	4.52
127	4.54

EVR	V_{COMH}
128	4.56
129	4.58
130	4.6
131	4.62
132	4.64
133	4.66
134	4.68
135	4.7
136	4.72
137	4.74
138	4.76
139	4.78
140	4.8
141	4.82
142	4.84
143	4.86
144	4.88
145	4.9
146	4.92
147	4.94
148	4.96
149	4.98
150	5

9-2-63. MDLDEF (LCD Module Definition: C0h)

This command and the parameters that follow are used to set the LCD module.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
MDLDEF	0	1	↑	1	1	0	0	0	0	0	0	C0	LCD Module definition
P1	1	1	↑	B17	B16	B15	B14	B13	B12	B11	B10	xx	IC
P2	1	1	↑	*	*	*	B24	*	*	*	B20	xx	
P3	1	1	↑	*	*	*	*	*	*	*	B30	xx	
P4	1	1	↑	*	*	*	*	*	*	*	*	xx	
P5	1	1	↑	*	*	*	*	*	*	*	*	xx	

B17-B10: Used for correction of the IC

Input the value shown below.

B17	B16	B15	B14	B13	B12	B11	B10	IC correction
0	0	0	0	0	0	0	0	Sets the correction (fixed value)

Sets it to 0Eh(00 1110), when parallel interface is used.

Sets it to 0Fh(00 1111), when serial interface is used.

B20: Selects the default value of LUT

B20	LUT default value
0	16.8M color LUT
1	262K color LUT

B24: Selects the read type during parallel interface

B24	Read type
0	Read type 1 (display-data format)
1	Read type 2 (262K color mode)

B30: Reduces the length of the power-supply on/off sequence (Test function)

B30	Power-supply on/off sequence
0	Normal
1	Test mode

* This does not mean that the length of the actual power-supply generation period is reduced.

9-2-64. PWRDEF (Power Definition: C1h)

This command and the parameters that follow define the internal power-supply on/off sequence and set the internal regulator capacity.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
PWRDEF	0	1	↑	1	1	0	0	0	0	0	1	C1	Power definition
P1	1	1	↑	*	*	B15	B14	B13	B12	B11	B10	xx	C.P Movement
P2	1	1	↑	*	*	B25	B24	B23	B22	B21	B20	xx	C.P Clock
P3	1	1	↑	B37	B36	B35	B34	B33	B32	B31	B30	xx	Basic Voltage
P4	1	1	↑	B47	B46	B45	B44	B43	B42	B41	B40	xx	Regulater ON/OFF
P5	1	1	↑	*	B56	B55	B54	B53	B52	B51	B50	xx	Regulater Set 1 (FBH, V_{COM})
P6	1	1	↑	*	*	*	*	B63	B62	B61	B60	xx	Regulater Set 2 (REG)
P7	1	1	↑	*	B76	B75	B74	B73	B72	B71	B70	xx	Regulater Set 3 (V_{OFREG} BST)
P8	1	1	↑	B87	B86	B85	B84	B83	B82	B81	B80	xx	Regulater Set 4 (V_{COMH} CU)
P9	1	1	↑	B97	B96	B95	B94	B93	B92	B91	B90	xx	Regulater Set 5 (V_{COML} CU)
P10	1	1	↑	B107	B106	B105	B104	B103	B102	B101	B100	xx	ONseq wait 1
P11	1	1	↑	B117	B116	B115	B114	B113	B112	B111	B110	xx	ONseq wait 2
P12	1	1	↑	B127	B126	B125	B124	B123	B122	B121	B120	xx	ONseq wait 3
P13	1	1	↑	*	*	*	*	*	*	*	*	xx	Not defined

Make sure these settings are made before SLPOUT. Do not change the settings while in display mode. The set value takes effect after SLPOUT.

B15: Sets power-save mode of the source-driver bias circuit

B15	Power save
0	Power save
1	Operating

B14: Sets soft start

B14	Soft start
0	Available
1	N/A

B13-B10: Sets the operation of the booster circuit

Bit	Description	Status	
B13	4th-booster-circuit operation	0: Forcibly stopped	1: Normal operation
B12	3rd-booster-circuit operation	0: Forcibly stopped	1: Normal operation
B11	2nd-booster-circuit operation	0: Forcibly stopped	1: Normal operation
B10	1st-booster-circuit operation	0: Forcibly stopped	1: Normal operation

B25-B23: Sets the 3rd/4th-booster clock interval

B25	B24	B23	Booster clock interval
0	0	0	Setting prohibited
0	0	1	1H × 4
0	1	0	1H × 2
0	1	1	1H × 1
1	0	0	1H / 2
1	0	1	1H / 4
1	1	0	1H / 8
1	1	1	1H / 16

B22-B20: Sets the 1st-/2nd-booster clock interval

B22	B21	B20	Booster clock interval
0	0	0	Setting prohibited
0	0	1	1H × 4
0	1	0	1H × 2
0	1	1	1H × 1
1	0	0	1H / 2
1	0	1	1H / 4
1	1	0	1H / 8
1	1	1	1H / 16

B37-B34: Sets operation of the regulator/bias current

Bit	Description	Status	
B37	V_{REG}	0: Forcibly stopped	1: Normal operation
B36	V_{LDO}	0: Forcibly stopped	1: Normal operation
B35	IBAS	0: Forcibly stopped	1: Normal operation
B34	V_{OSC}	0: Forcibly stopped	1: Normal operation

B33-B32: Sets the amount of bias current used for the reference power supply

B33	B32	Amount of reference current
0	0	0.3μA (small type)
0	1	0.37μA (type)
1	0	0.43μA (type)
1	1	0.5μA (large type)

B31-B30: Sets the work function and the reference power supply

B33	B32	Combination
0	0	Work function
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Setting prohibited

B47-B40: Sets operation of the regulator

Bit	Description	Status	
B47	V_{COM}	0: Forcibly stopped	1: Normal operation
B46	V_{COML}	0: Forcibly stopped	1: Normal operation
B45	V_{COMH}	0: Forcibly stopped	1: Normal operation
B44	V_{COMW}	0: Forcibly stopped	1: Normal operation
B43	V_{OFREG}	0: Forcibly stopped	1: Normal operation
B42	V_{ONREG}	0: Forcibly stopped	1: Normal operation
B41	V_{DDRH}	0: Forcibly stopped	1: Normal operation
B40	V_{DDHS}	0: Forcibly stopped	1: Normal operation

B56: Selects a V_{COMH}-adjusting circuit

B56	V_{COMH} adjustment selection
0	Internal circuit
1	External circuit (FBH used)

B55: Sets the V_{COML} drive capacity

B55	V_{COML} drive capacity
0	Normal capacity
1	High drive capacity

B54: Sets the V_{COML} low-power mode

B54	V_{COML} low-power mode
0	Normal mode
1	Low-power mode

B53: Sets the V_{COML} phase-compensation capacitance

B53	V_{COML} phase-compensation capacitance
0	Connects the phase-compensation capacitance
1	Disconnects the phase-compensation capacitance

B52: Sets the V_{COMH} drive capacity

B52	V_{COMH} drive capacity
0	Normal capacity
1	High drive capacity

B51: Sets the V_{COMH} low-power mode

B51	V_{COMH} low-power mode
0	Normal mode
1	Low-power mode

B50: Sets the V_{COMH} phase-compensation capacitance

B50	V_{COMH} phase-compensation capacitance
0	Connects the phase-compensation capacitance
1	Disconnects the phase-compensation capacitance

B63-B60: Sets low-power-mode operation of the regulator

Bit	Description	Status	
B63	V_{DDRH}	0: Normal operation	1: Low-power mode
B62	V_{DDHS}	0: Normal operation	1: Low-power mode
B61	V_{OFREG}	0: Normal operation	1: Low-power mode
B60	V_{ONREG}	0: Normal operation	1: Low-power mode

B76-B70: Sets the V_{OFREG} capacity-increase interval

B77	B76	B75	B74	B73	B72	B71	B70	V_{OFREG} capacity-increase interval	Accepted setting range
0	0	1	0	0	0	0	0	e.g.) 32 lines	1 to 127

(Set value – 1) × number of lines

Set this parameter based on the number of lines.

B87-B80: Sets the V_{COMH} capacity-increase interval

B87	B86	B85	B84	B83	B82	B81	B80	V_{COMH} capacity-increase interval	Accepted setting range
0	0	0	1	0	0	0	0	e.g.) 16 clock cycles	1 to 255

(Set value – 1) × number of clocks

Set this parameter based on the number of internal oscillator clock cycles.

B97-B90: Sets the V_{COML} capacity-increase interval

B97	B96	B95	B94	B93	B92	B91	B90	V_{COML} capacity-increase interval	Accepted setting range
0	0	0	1	0	0	0	0	e.g.) 16 clock cycles	1 to 255

(Set value – 1) × number of clocks

Set this parameter based on the number of internal oscillator clock cycles.

B107-B100: Sets the 1st/2nd booster startup wait time from the start of oscillation by the number of lines

B107	B106	B105	B104	B103	B102	B101	B100	Wait time	Accepted setting range
0	0	0	0	0	1	0	0	e.g.) 4 lines	1 to 255

B117-B110: Sets the regulator-circuit operation wait time from the start of 1st/2nd booster operation by the number of lines

B117	B116	B115	B114	B113	B112	B111	B110	Wait time	Accepted setting range
0	0	0	0	0	1	0	0	e.g.) 4 lines	1 to 255

B127-B120: Sets the 3rd/4th booster stabilization time from V_{REG} startup by the number of lines

B127	B126	B125	B124	B123	B122	B121	B120	Wait time	Accepted setting range
0	0	0	0	0	1	0	0	e.g.) 4 lines	1 to 255

9-2-65. IFMOD (Interface Mode Select: C2h)

This command and the parameters that follow are used to select the interface mode.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
IFMOD	0	1	↑	1	1	0	0	0	0	1	0	C2	Inerface mode select
P1	1	1	↑	*	*	*	B4	*	B2	B1	B0	xx	Interface mode

B2-B0: Sets the display-data bit width

When a serial interface is used, the display-data bit width is fixed to 8 bits regardless of what value is set.

B2	B1	B0	Display-data bit width
0	0	0	8 Bit
0	0	1	9 Bit
0	1	0	12 Bit
0	1	1	16 Bit
1	0	0	18 Bit
1	0	1	24 Bit
1	1	0	Undefined
1	1	1	Undefined

B4: Selects the display-data format during 16.8M-color-mode 16-bit interface, 262K-color-mode 12-bit interface, and 4096-color-mode 8-bit interface

B4	RGB array	Display-data format		
		16.8M	262K	4096
0	RG, BR, GB	16Bit 888 2/3	12Bit 666 2/3	8Bit 444 2/3
1	RG, B*	16Bit 888 1/2	12Bit 666 1/2	8Bit 444 1/2

* Settings during other than 16.8M-color-mode 16-bit interface, 262K-color-mode 12-bit interface, and 4096-color-mode 8-bit interface have no effect.

9-2-66. LCDCIF (LCDC Interface: D0h)

This command and the parameters that follow enable or disable the LCDC interface. Settings made here are effective only when a parallel interface is in use. This command and the subsequent parameter must be issued within the blank interval of the LCDC interface.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
LCDCIF	0	1	↑	1	1	0	1	0	0	0	0	D0	LCDC Interface
P1	1	1	↑	*	*	*	*	*	*	*	B0	xx	Enable / Disable

B0: Enables or disables the LCDC interface

B0	LCDC I/F
0	Disable
1	Enable

* When this command is set to enable, use of the parallel interface is subject to limitations.

Refer to Section 8-2, "LCDC Interface."

9-2-67. EXVSYNCDEF (External VSYNC Definition: D1h)

This command and the parameters that follow enable settings to be made for external VSYNC synchronization.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
EXVSYNCDEF	0	1	↑	1	1	0	1	0	0	0	1	D1	External VSYNC definition
P1	1	1	↑	*	*	*	*	*	B2	B1	B0	xx	Adjust1

B2-B0: Corrects the display-scan start time during external VSYNC synchronization

This setting enables setting of a wait interval before display scan starts after external VSYNC synchronization is achieved. This setting can be made in a range of 0 (display starts immediately after synchronization) to 7 (display starts 7 lines of wait interval after synchronization).

B2	B1	B0	Correction of the display-scan start time	Accepted setting range
0	1	0	e.g.) 2 lines	0 to 7

Refer to Section 8-17-3, “Display Synchronous Data Transfer by External VSYNC.”

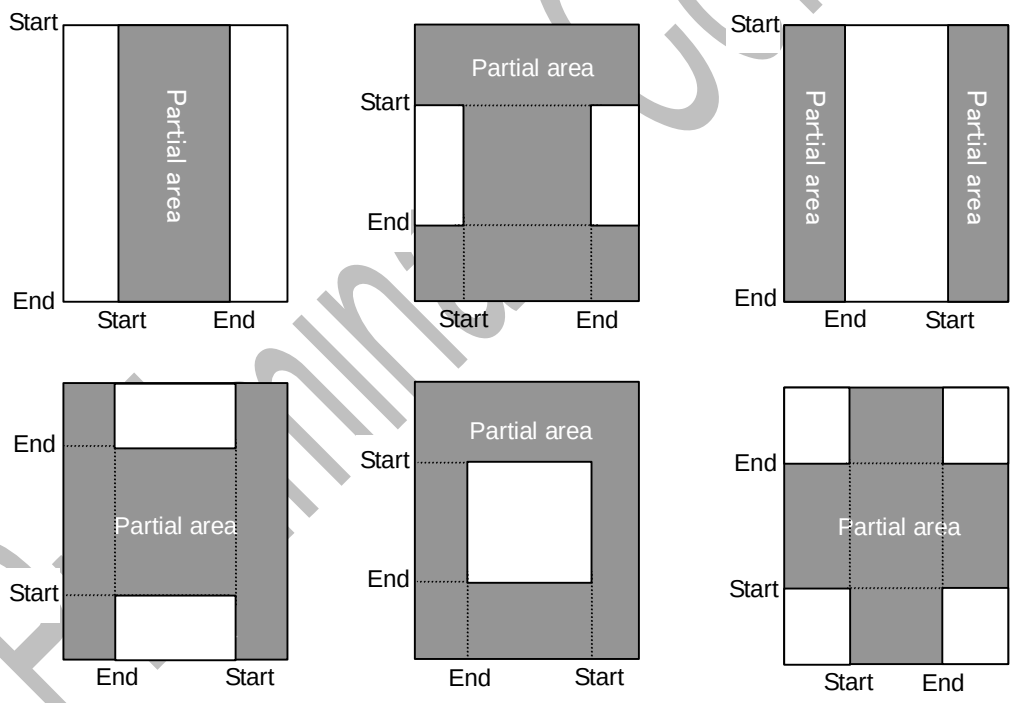
9-2-68. VPTLAR (Vertical Partial Area: C7h)

Issuing this command sets the vertical partial area.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
VPTLAR	0	1	↑	1	1	0	0	0	1	1	1	C7	Vertical partial area
P1	1	1	↑	*	*	*	*	*	*	*	B10	xx	Start line (upper)
P2	1	1	↑	B27	B26	B25	B24	B23	B22	B21	B20	xx	Start line (lower)
P3	1	1	↑	*	*	*	*	*	*	*	B30	xx	End line (upper)
P4	1	1	↑	B47	B46	B45	B44	B43	B42	B41	B40	xx	End line (lower)
P5	1	1	↑	*	*	*	*	*	*	*	B50	xx	Start column (upper)
P6	1	1	↑	B67	B66	B65	B64	B63	B62	B61	B60	xx	Start column (lower)
P7	1	1	↑	*	*	*	*	*	*	*	B70	xx	End column (upeer)
P8	1	1	↑	B87	B86	B85	B84	B83	B82	B81	B80	xx	End column (lower)

Set the start and end lines and the start and end columns of partial display.

Count the start line and start column beginning with 0.



9-2-69. VPTLIN (Vertical Partial Mode In: C8h)

Issuing this command places the driver in vertical partial mode.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
VPTLIN	0	1	↑	1	1	0	0	1	0	0	0	C8	Vertical partial mode in

9-2-70. VPTLOUT (Vertical Partial Mode Out: C9h)

Issuing this command releases the driver from vertical partial mode.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
VPTLOUT	0	1	↑	1	1	0	0	1	0	0	1	C9	Vertical partial mode out

9-2-71. TESTOPT (Test Mode Option: C5h)

This command sets various test modes. As this command is used to test the IC, its operation is not inspected at shipment.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
TESTOPT	0	1	↑	1	1	0	0	0	1	0	1	C5	Test mode option
P1	1	1	↑	B7	B6	B5	B4	B3	B2	B1	*	XX	Test mode option flag

* Effective only when TMONI = HIGH

Bit	Description	Status	
B7	PKG test-pin setting mode	0: Normal operation	1: Test operation
B6	Source-data scan mode	0: Normal operation	1: Test operation
B5	Gate-driver output inversion mode	0: Normal operation	1: Test operation
B4	Internal-oscillator OS1-pin output mode	0: Normal operation	1: Test operation
B3	FUSE-setting TESTFSE data mode	0: Normal operation	1: Test operation
B2	AC-correction test mode	0: Normal operation	1: Test operation
B1	DISON & gamma-circuit data-access time shortening mode	0: Normal operation	1: Test operation

9-2-72. TESTPKG (Test PKG-Mode On: CAh)

Issuing this command enters PKG test mode (in which the source prebuffer function of non-wire-bonded pins is forcibly disabled). As this command is used to test the IC, its operation is not inspected at shipment.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
TESTPKG	0	1	↑	1	1	0	0	1	0	1	0	CA	Test PKG-Mode On

* Effective only when TMONI = HIGH

(1) The pin state is determined by the MSB of the memory data. 0: Bonded pin; 1: Unbonded pin

* LCD address 0 is read.

(2) The PKG test state is entered using TESTPKG.

(3) 2 CLK input from the OS1 pin (LOW state).

* The command does not function unless TMONI = HIGH.

* This mode is not reset by SWRESET.

9-2-73. TESTREG (Test Mode Register Read: CBh)

This command and the parameters that follow set the test mode of the IC.

As this command is used to test the IC, its operation is not inspected at shipment.

When the LCDC interface is active while the parallel interface is being used, this command is interpreted as NOP.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
TESTREG	0	1	↑	1	1	0	0	1	0	1	1	CB	Test mode Register read
P1	1	1	↑	B7	B6	B5	B4	B3	B2	B1	B0	xx	Read register number
P2	1	↓0	1	Read data								xx	Read data
P3	1	↓0	1	Read data								xx	Read data
:	1	↓0	1	Read data								xx	Read data

* Effective only when TMONI = HIGH

B7-B0: Specifies the register number from which to start reading registers

No	Mapped register	No	Mapped register	No	Mapped register	No	Mapped register
1	CASET P1	26	P6	51	P7	76	P2
2	P2	27	P7	52	Empty	77	P3
3	P3	28	P8	53	Empty	78	P4
4	P4	29	P9	54	XVSYNCDEF P1	79	P5
5	PASET P1	30	P10	55	MDLDEF P1	80	P6
6	P2	31	P11	56	P2	81	P7
7	P3	32	P12	57	Empty	82	P8
8	P4	33	P13	58	Empty	83	VPTLAR P1
9	PTLAR P1	34	P14	59	Empty	84	P2
10	P2	35	P15	60	Empty	85	P3
11	P3	36	P16	61	PWRDEF P1	86	P4
12	P4	37	P17	62	P2	87	P5
13	VSCRDEF P1	38	P18	63	P3	88	P6
14	P2	39	P19	64	P4	89	P7
15	P3	40	P20	65	P5	90	P8
16	P4	41	E2RCTL P1	66	P6	91	TOH FUSE table
17	P5	42	Empty	67	P7	92	TOH FUSE value
18	P6	43	MADDEF P1	68	P8	93	LCDCDADEF P1
19	VSCRSADD P1	44	Empty	69	P9	94	P2
20	P2	45	EVRSET P1	70	P10	95	P3
21	DISCTL P1	46	P2	71	P11	96	P4
22	P2	47	P3	72	P12	97	P5
23	P3	48	P4	73	P13	98	P6
24	P4	49	P5	74	Empty	99	P7
25	P5	50	P6	75	TESTFSE P1	100	P8

9-2-74. TESTTFSE (Test Mode Fuse: CCh)

This command and the parameters that follow set the Fuse value in IC test mode.

As this command is used to test the IC, its operation is not inspected at shipment. For command issuance and settings to be effective, the TMONI pin must be held HIGH.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
TESTFSE	0	1	↑	1	1	0	0	1	1	0	0	CC	Test mode Fuse
P1	1	1	↑	*	*	B15	B14	B13	B12	B11	B10	xx	Basic Voltage W.F
P2	1	1	↑	*	*	B25	B24	B23	B22	B21	B20	xx	Basic Voltage Vth
P3	1	1	↑	*	*	*	*	B33	B32	B31	B30	xx	IBIAS
P4	1	1	↑	*	*	*	B44	B43	B42	B41	B40	xx	OSC
P5	1	1	↑	*	*	*	B54	B53	B52	B51	B50	xx	AC tOH
P6	1	1	↑	*	*	*	B64	B63	B62	B61	B60	xx	SDR IBIAS
P7	1	1	↑	*	B76	B75	B74	B73	B72	B71	B70	xx	Discharge Control 1
P8	1	1	↑	*	B86	B85	B84	B83	B82	B81	B80	xx	Discharge Control 2

B15-B10: Sets the fuse for the reference voltage (work function)

B15	B14	B13	B12	B11	B10	Fuse for adjusting the work function
0	0	0	1	0	0	e.g.) 4

B25-B20: Sets the fuse for the reference voltage (Vth)

B25	B24	B23	B22	B21	B20	Fuse for adjusting Vth
0	0	0	1	0	0	e.g.) 4

B33-B30: Sets the fuse for the bias current

B33	B32	B31	B30	Fuse for adjusting the bias current
0	1	0	0	e.g.) 4

B44-B40: Sets the fuse for internal oscillation

B44	B43	B42	B41	B40	Fuse for adjusting the internal oscillation
0	0	1	0	0	e.g.) 4

B54-B50: Sets the fuse for adjusting the read disable time delay

B54	B53	B52	B51	B50	Fuse for adjusting TOH
0	0	1	0	0	e.g.) 4

B64-B60: Sets the fuse for the source-driver bias current

B64	B63	B62	B61	B60	Fuse for adjusting the source-driver bias current
0	0	1	0	0	e.g.) 4

B65-B60: Sets the fuse for the source-driver bias current

B65	B64	B63	B62	B61	B60	Fuse for adjusting the source-driver bias current
0	0	0	1	0	0	e.g.) 4

B76-B70: Sets discharge control

Bit	Description	Status	
B76	V_{DDHS}	0: Normal operation	1: Discharge prohibited
B75	V_{COM}	0: Normal operation	1: Discharge prohibited
B74	V_{COML}	0: Normal operation	1: Discharge prohibited
B73	V_{COMH}	0: Normal operation	1: Discharge prohibited
B72	V_{ONREG}	0: Normal operation	1: Discharge prohibited
B71	V_{OFREG}	0: Normal operation	1: Discharge prohibited
B70	V_{DDRH}	0: Normal operation	1: Discharge prohibited

B86-B80: Sets discharge control

Bit	Description	Status	
B86	V_{REG}	0: Normal operation	1: Discharge prohibited
B85	V_{CORE}	0: Normal operation	1: Discharge prohibited
B84	V_{OSC}	0: Normal operation	1: Discharge prohibited
B83	V_{EE}	0: Normal operation	1: Discharge prohibited
B82	V_{DDHG}	0: Normal operation	1: Discharge prohibited
B81	V_{OUTM}	0: Normal operation	1: Discharge prohibited
B80	V_{OUT}	0: Normal operation	1: Discharge prohibited

9-2-75. TESTMOD (Test Mode: CEh)

This command and the parameters that follow set the test mode of the IC.

As this command is used to test the IC, its operation is not inspected at shipment. For command issuance and settings to be effective, the TMONI pin must be held HIGH.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
TESTMOD	0	1	↑	1	1	0	0	1	1	1	0	CE	Test mode
P1	1	1	↑	*	B6	B5	B4	B3	B2	B1	B0	xx	Test output select

B6-B0: Sets test-pin (TS8-0) assignments

B6-B0	TEST8	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
0	Hi-Z								
1	M_CAC_L[8:0]								
2	M_CAC_R[8:0]								
3	M_CEN_L	M_CAC_L[7:0]							
4	M_CEN_R	M_CAC_R[7:0]							
5	M_CEN_L	M_RAC_L[7:0]							
6	M_CEN_R	M_RAC_R[7:0]							
7	M_RLINE	M_RAL[7:0]							
8	M_CEN_L	M_MR_W_L[7:0]							
9	M_CEN_L	M_MG_W_L[7:0]							
10	M_CEN_L	M_MB_W_L[7:0]							
11	M_CEN_R	M_MR_W_R[7:0]							
12	M_CEN_R	M_MG_W_R[7:0]							
13	M_CEN_R	M_MB_W_R[7:0]							
14	M_CEN_L	M_MR_R_L[7:0]							
15	M_CEN_L	M_MG_R_L[7:0]							
16	M_CEN_L	M_MB_R_L[7:0]							
17	M_CEN_R	M_MR_R_R[7:0]							
18	M_CEN_R	M_MG_R_R[7:0]							
19	M_CEN_R	M_MB_R_R[7:0]							
20	0	0	0	XwrPrlSrl	M_RLINE	M_CEN_L	M_ACTB_L	M_CEN_R	M_ACTB_R
21	G_OEV	G_GAD[7:0]							
22	R_ST	R_CK	WR_GB[6:0]						
23	R_ST	R_CK	WR_R[6:0]						
24	P_POL	R_ENB8	R_ENB7	R_ENB6	R_ENB5	R_ENB4	R_ENB3	R_ENB2	R_ENB1
25	R_GMSWEN	R_DIS	S_XDACON	S_PS2	S_PS1	S_XENCONNE	S_XENPRE	S_PREEN2	S_PREEN1
26	S_DTLH	S_FRCF0	S_FRCF1	S_FRCL0	S_FRCL1	S_XFRCR	S_POL	S_DISINVL2	S_POLU6
27	S_COL8	S_COM	S_PSCLK	S_PTV	S_XPTH	S_ENACTPS2	S_FPSR2R2	S_ENACTPS	S_FPSR2R
28	P_LAT	P_INDEX3	P_INDEX2	P_INDEX1	P_INDEX0	P_DATA[3:0]			
29	P_VCUH	P_XSLOSC	P_XSLVREF	P_XSLLD	P_XSLREG	P_XSLHS	P_XSLRH	P_XSLON	P_XSLOF
30	P_VCUL	P_XSLCOMW	P_XSLCOMH	P_XSLCOML	P_XSLCOM	P_XSLP1	P_XSLP2	P_XSLP3	P_XSLP4
31	P_CLK11	P_CLK21	P_CLK31	P_CLK41	P_CLK12	P_CLK22	P_CLK32	P_CLK42	BST3
32	0	Gm0_PR_16H[7:0]							
33	0	Gm0_PR_48H[7:0]							
34	0	Empty							
35	0	Empty							
36	0	Empty							
37	0	Empty							
38	0	Empty							
39	0	Empty							
40	0	Empty							
41	0	Empty							
42	0	Empty							
43	0	Empty							
44	0	Empty							
45	0	Empty							

46	0	Empty							
47	0	Empty							
48	0	Empty							
49	0	Empty							
50	0	Empty							
51	0	Empty							
52	0	Empty							
53	0	Empty							
54	0	Empty							
55	0	Empty							
56	0	Empty							
57	0	Empty							
58	0	Empty							
59	0	Empty							
60	0	Val16[7:0]							
61	0	Val48[7:0]							
62	P_POL	Gam16[7:0]							
63	P_POL	Gam48[7:0]							
64	0	0	0	0	0	0	P_POL	FlgR2RPS1Auto	FlgR2RPS2Auto
65	R_CK	R_D_R[7:0]							
66	R_ST	R_D_GB[7:0]							
67	0	0	0	0	0	0	0	0	0
68	0	0	0	0	0	0	0	0	0
69	0	0	0	0	0	0	0	0	0
70	0	0	0	0	0	0	0	0	0

9-2-76. TESTSUP (Test Mode Test Support: CFh)

This command and the parameters that follow set the test mode of the IC.

As this command is used to test the IC, its operation is not inspected at shipment. For command issuance and settings to be effective, the TMONI pin must be held HIGH.

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
TESTSUP	0	1	↑	1	1	0	0	1	1	1	1	CF	Test mode Test-support
P1	1	1	↑	*	*	*	*	B3	B2	B1	B0	xx	Default is 00h

B2-B0: These bits enable setting of the IC measurement mode.

B3-B0	Test mode
0	Normal
1	Source Output All-H
2	Source Output All-L
3	Source Output [HHHLLLHHHLLL....]
4	Source Output [LLLHHHLLLHHH....]
5	Source Output All-Short
6	Gate Output [HLLLHLLL....]
7	Gate Output [LHLLLHLL....]
8	Gate Output [LLHLLLHL....]
9	Gate Output [LLLHLLLH....]
10	Gate Output [HLHLHLHL....]
11	Gate Output [LHLHLHLH....]
12	Gamma-wire Voltage Connection Force ON
13	Gamma-wire Voltage Connection Force OFF
14	Gate Output [HHLLHHLL....]
15	Gate Output [LLHHLLHH....]

10. Absolute-Maximum Ratings

Item	Symbol	Rating Value	Unit
Power-supply voltage (1)	V_{DDI}	–0.3 to + 7.0	V
Power-supply voltage (2)	V_{DD}	–0.3 to + 7.0	V
Power-supply voltage (3)	V_{OUT}	–0.3 to + 7.0	V
Power-supply voltage (4)	V_{OUTM}	–7.0 to + 0.3 *3	V
Power-supply voltage (5)	V_{DDHS}	–0.3 to + 6.0	V
Power-supply voltage (6)	V_{DDRH}	–0.3 to + 6.0	V
Power-supply voltage (7)	V_{CORE}	–0.3 to + 2.5	V
Power-supply voltage (8)	V_{DDHG}	–0.3 to + 18.0	V
Power-supply voltage (9)	V_{EE}	–18.0 to + 0.3	V
Power-supply voltage (10)	V_{ONREG}	–0.3 to + 7.0	V
Power-supply voltage (11)	V_{OFREG}	–0.3 to + 7.0	V
Power-supply voltage (12)	V_{COMH}	–0.3 to + 7.0	V
Power-supply voltage (13)	V_{COML}	–7.0 to + 0.5	V
Input voltage	V_{IN}	–0.5 to power-supply block + 0.5 *1	V
Output voltage	V_{OUT}	–0.5 to power-supply block + 0.5 *2	V
Operating temperature	T_{opr}	–40 to + 85	°C
Storage temperature 1	T_{stg1}	–65 to + 150	°C

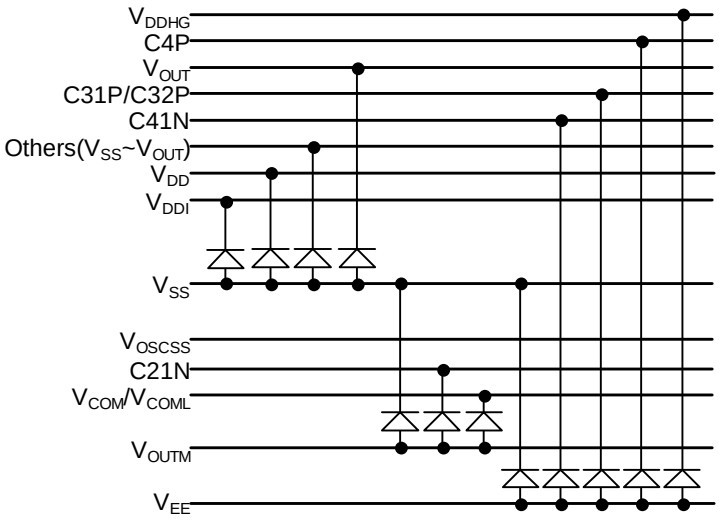
* All voltages are referenced to V_{SS} = 0 V.
* Storage temperature 1 applies for a bare chip.
* If the LSI is used under conditions exceeding the absolute-maximum ratings, it may be permanently damaged. The LSI should normally be used under conditions conforming to the electrical characteristics stipulated herein. If these conditions are not satisfied, the LSI may operate erratically or its reliability may be adversely affected.
* The power-supply voltages (3) to (13) cannot be sourced from external power supplies.
* The LCDdrive voltages must always satisfy the condition $V_{DDHG} \geq V_{OUT} \geq V_{SS} \geq V_{OUTM} \geq V_{EE}$. Note also that if, while the LCDdrive voltage is being applied,

*1: The term “power-supply block” as used here refers to either V_{DDI} or V_{DD}. For the relationship between each pin and the power supply used, refer to Chapter 6, “Pin Description.”

*2: The term “power-supply block” as used here refers to one of V_{DDI}, V_{OSC}, V_{DDHG}, V_{DDHS}, V_{SS}, or V_{EE}. For the relationship between each pin and the power supply used, refer to Chapter 6, “Pin Description.”

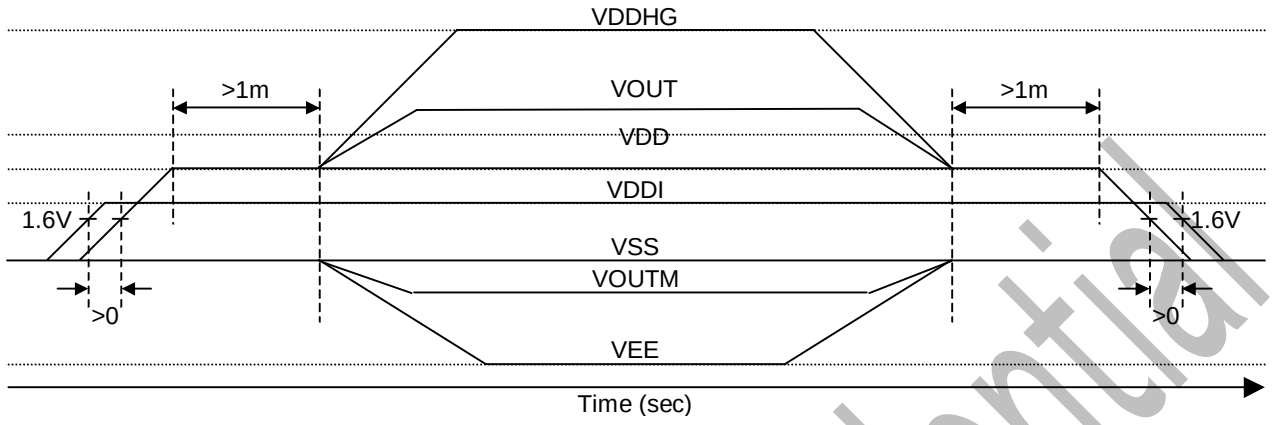
*3: Absolute maximum rating of VDD to VOUTM voltage is 7V.

◇ Diodes for protection between voltages

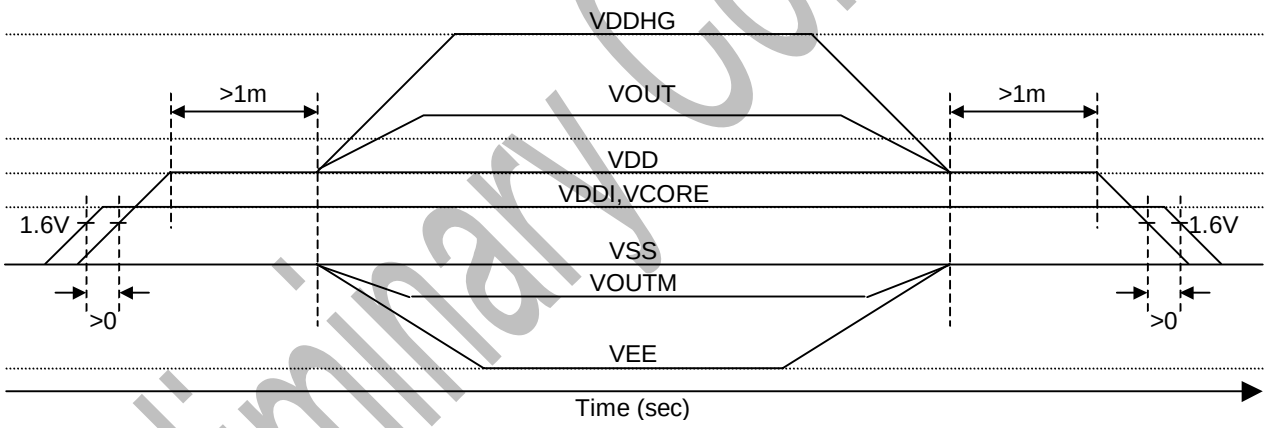


◇ Power-on/power-off sequences

In case of internal regulator (V18) is used for VCORE power supply



In case of VCORE voltage input externally



11. Electrical Characteristics

11-1. DC Characteristics

Referenced to V_{DDI} = 1.8 V, V_{DD} = 2.3 V, V_{SS} = 0 V, and T_a = –40°C to 85°C unless otherwise noted

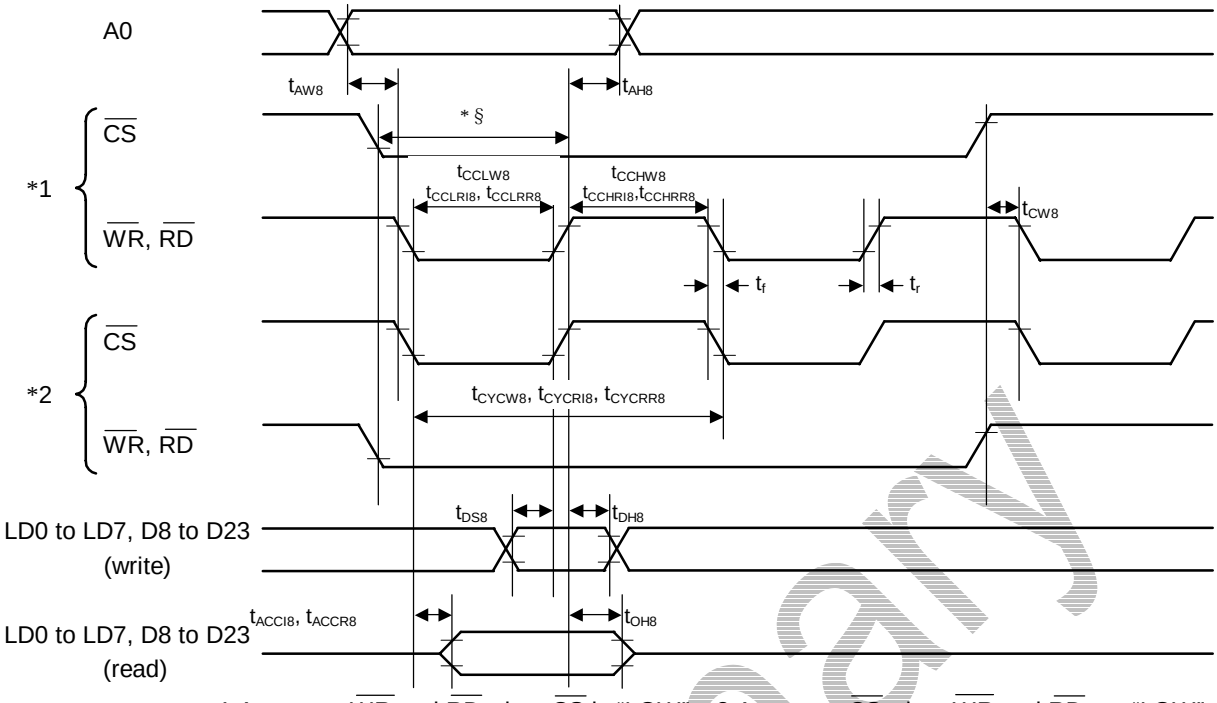
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
Power-supply voltage (1)	V_{DDI}		1.65	1.8	3.3	V	V_{DDI}
Power-supply voltage (2)	V_{DD}		2.3	-	3.3	V	V_{DD}
Power-supply voltage (3)	V_{OUT}		4.6	-	6.3	V	V_{OUT}
Power-supply voltage (4)	V_{OUTM}		-6.3	-	0	V	V_{OUTM} *7
Power-supply voltage (5)	V_{DDHS}		2.4	-	5.5	V	V_{DDHS}
Power-supply voltage (6)	V_{DDRH}		2.4	-	5.5	V	V_{DDRH}
Power-supply voltage (7)	V_{DDHG}		7.0	-	16.0	V	V_{DDHG}
Power-supply voltage (8)	V_{EE}		-16.0	-	-5.0	V	V_{EE}
Power-supply voltage (9)	V_{ONREG}		2.4	-	5.5	V	V_{ONREG}
Power-supply voltage (10)	V_{OFREG}		1.0	-	4.1	V	V_{OFREG}
Power-supply voltage (11)	V_{COMH}		2.0	-	5.6	V	V_{COMH}
Power-supply voltage (12)	V_{COML}		V_{OUTM}	-	0.0	V	V_{COML}
High-level input voltage	V_{IHC}		0.7 V_{DDI}	-	V_{DDI}	V	* 1-1
Low-level input voltage	V_{ILC}		0.0	-	0.3 V_{DDI}	V	* 1-1
High-level output voltage	V_{OH}	I_{OH} = -1.0 mA	V_{DDI} -0.4	-	V_{DDI}	V	* 2-1
Low-level output voltage	V_{OL}	I_{OL} = +1.0 mA	0.0	-	0.4	V	* 2-1
Input current	ILI1	GNDL ≤ VIN ≤ V_{DDI}	-	-	1.0	µA	* 1-1
Output-voltage deviation	ΔVs	T_a = 25°C	-	±4~6	±10	mV	SO1 to SO960
1st-booster capacity (internal resistor)	RVOUT1	V_{DD} = 2.8V V_{DC1} = V_{DD}	-	6.5	100	Ω	V_{OUT}
2nd-booster capacity (internal resistor)	RVOUT2	V_{DD} = 2.8V V_{DC2} = V_{DD}	-	280	420	Ω	V_{OUTM}
3rd-booster capacity (internal resistor)	RVOUT3	V_{DD} = 2.8V V_{ONREG} = 5V V_{DC3} = V_{ONREG}	-	720	1080	Ω	V_{DDHG}
4th-booster capacity (internal resistor)	RVOUT4	V_{DD} = 2.8V V_{OFREG} = 5V V_{DC4} = V_{OFREG} V_{DC5} = 0V	-	1040	1560	Ω	V_{EE}
Static current	IDDQ1	Power-save state *3-1 T_a = 25 °C	-	-	5	µA	V_{SS}
Static current	IDDQ2	Power-on state *3-1 T_a = 25 °C	-	-	5	µA	V_{SS}
Operating current	IDDOP1	MPU access * 4-1,4-2 T_a = 25 °C, Display OFF	-	0.83	1.6	mA	V_{SS}
Operating current	IDDOP2	MPU no access * 4-1,4-2 T_a = 25 °C, Display ON	-	3.8	7.4	mA	V_{SS}
Input capacitance	CI	Freq. = 1 MHz	-	-	15	pF	* 1-1 to 1-2
Output capacitance	CO	T_a = 25 °C chip alone	-	-	15	pF	* 2-1 to 2-2
Internal oscillator frequency	Fosc	T_a = 25 °C	0.97	1.00	1.03	MHz	* 5
External input clock frequency	FoscI	T_a = 25 °C	0.90	1.00	1.10	MHz	* 6

Supplementary explanation of DC characteristics

* 1-1	Input (V_{DDI} block)	• P/S, MPUSEL, OSSEL, INISEL, RESSEL, IF16BIT, VOLSET, LCPOS1, LCPOS0, $\overline{RES}$, $\overline{CS}$, A0, $\overline{RD}$, $\overline{WR}$, VSYNC, HSYNC, ENA, DCK • D[23:0]SD (I/O input mode), LD[7:0]LSD (I/O input mode) • OS1(I/O input mode), TMONI, TSBIEN,TSBICK • LIOSWI, RIOSWI, LOPENSWI, LSHTSWI, LSHTSWI1, ROPENSWI, RSHTSWI, RSHTSWI1, GLSCHKI
* 1-2	Input (V_{DD} block)	• VSTBY, BDATA(I/O input mode), PTEST1, PTEST2
* 2-1	Output (V_{DDI} block)	• D[23:0]SD (I/O output mode), LD[7:0]LSD (I/O output mode), TE, OS1(I/O input mode) • TEST[8:0] • LIOSWO, RIOSWO, LOPENSWO, LSHTSWO, LSHTSWO1, ROPENSWO, RSHTSWO, RSHTSWO1, GLSCHKO
* 2-2	Output (V_{DD} block)	• POFF, BCK, BDATA(I/O input mode), BRST, BDO, TRI
* 3-1	Power-save state:	V_{DDI} = 1.8V, V_{DD} = 2.75V, V_{SS} = 0V
	Power-on state:	V_{DDI} =1.8V, V_{DD} =2.75V, V_{SS} = 0V V_{DDHS} = 5.5V, V_{DDHG} = 16.0V, V_{EE} = -16V
* 4-1	• Frame frequency = 60 Hz; Duty cycle = 1/240	
* 4-2	• “MPU access” refers to successive writes of display data at a cycle time of 1000 ns (1 MHz). The display data consists of intermediate gray scale data.	
* 4-3	• V_{DDHG} = 15 V; V_{DDHS} = 3.8 V; V_{SS} = 0 V; V_{EE} = –13.9 V	
* 5	• Complete built-in RC oscillator circuit	
* 6	• 1.0MHz ± 10%	
* 7	• V_{DD} - V_{OUTM} voltage should be 6.3 V or less	
* 8	• V_{DDHG} - V_{EE} voltage should be 30 V or less	
* 9	• V_{COMH} - V_{COML} voltage should be 6.3 V or less	

11-2. AC Characteristics

11-2-1. Read/Write Characteristics (80-series MPU parallel interface)



*1 Access at $\overline{WR}$ and $\overline{RD}$ when $\overline{CS}$ is "LOW". *2 Access at $\overline{CS}$ when $\overline{WR}$ and $\overline{RD}$ are "LOW".

Ta = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CW8}	$\overline{CS}$ - $\overline{WR}$, $\overline{RD}$ time	7	-	-	ns	-
A0	t_{AH8}	Address hold time	7	-	-	ns	-
	t_{AW8}	Address setup time	7	-	-	ns	
$\overline{WR}$	t_{CYCW8}	Write cycle	74	-	-	ns	-
	t_{CCHW8}	Control pulse width A	22	-	-	ns	
	t_{CCLW8}	Control pulse width B	22	-	-	ns	
$\overline{RD}$	t_{CYCRI8}	Read cycle (ID)	140	-	-	ns	When read ID data
	t_{CCHRI8}	Control pulse width A (ID)	45	-	-	ns	
	t_{CCLRI8}	Control pulse width B (ID)	35	-	-	ns	
	t_{CYCRR8}	Read cycle (VR)	200	-	-	ns	When read from VRAM
	t_{CCHRR8}	Control pulse width A (VR)	75	-	-	ns	
	t_{CCLRR8}	Control pulse width B (VR)	135	-	-	ns	
LD0 to LD7, D8 to D23	t_{DS8}	Data setup time	7	-	-	ns	-
	t_{DH8}	Data hold time	7	-	-	ns	
	t_{ACCI8}	Read access time (ID)	-	-	30	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{ACCR8}	Read access time (VR)	-	-	130	ns	
	t_{OH8}	Output disable time	25	-	70	ns	

MV pin, Ta = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

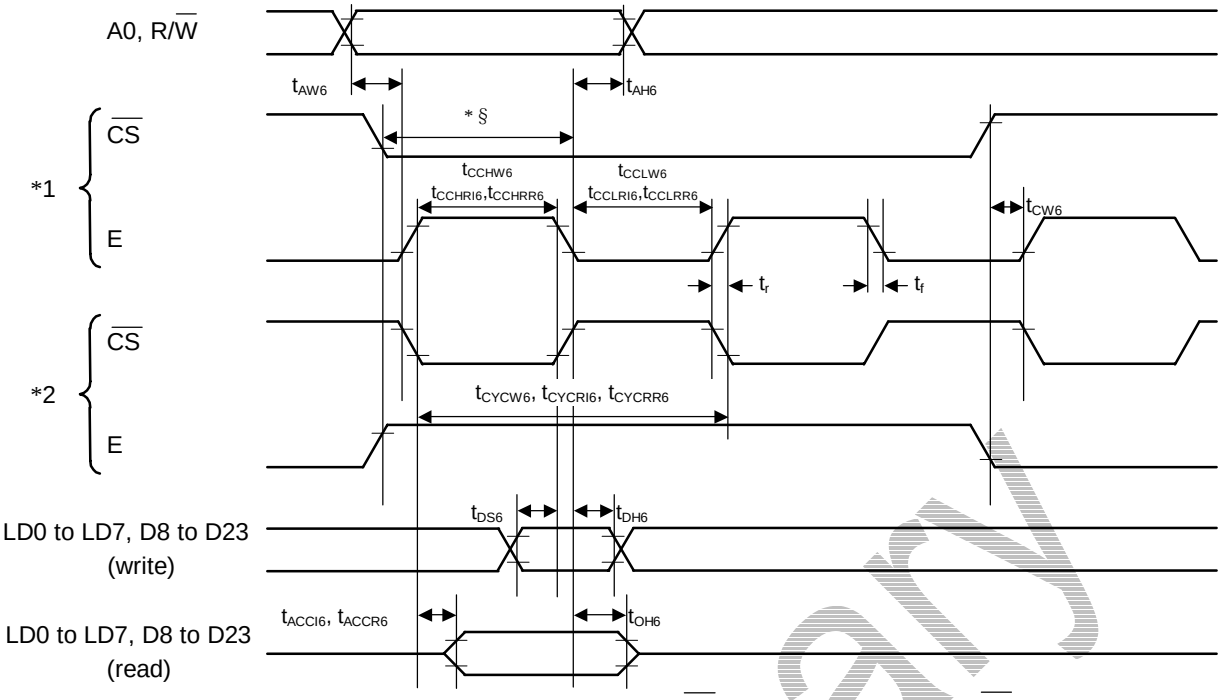
Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CW8}	$\overline{CS}$ - $\overline{WR}$, $\overline{RD}$ time	7	-	-	ns	-
A0	t_{AH8}	Address hold time	7	-	-	ns	-
	t_{AW8}	Address setup time	7	-	-	ns	
$\overline{WR}$	t_{CYCW8}	Write cycle	80	-	-	ns	-
	t_{CCHW8}	Control pulse width A	22	-	-	ns	
	t_{CCLW8}	Control pulse width B	28	-	-	ns	
$\overline{RD}$	t_{CYCRI8}	Read cycle (ID)	140	-	-	ns	When read ID data
	t_{CCHRI8}	Control pulse width A (ID)	45	-	-	ns	
	t_{CCLRI8}	Control pulse width B (ID)	35	-	-	ns	
	t_{CYCRR8}	Read cycle (VR)	200	-	-	ns	When read from VRAM
	t_{CCHRR8}	Control pulse width A (VR)	45	-	-	ns	
	t_{CCLRR8}	Control pulse width B (VR)	135	-	-	ns	
LD0 to LD7, D8 to D23	t_{DS8}	Data setup time	7	-	-	ns	-
	t_{DH8}	Data hold time	7	-	-	ns	
	t_{ACCI8}	Read access time (ID)	-	-	55	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{ACCR8}	Read access time (VR)	-	-	130	ns	
	t_{OH8}	Output disable time	15	-	70	ns	

MV pin, Ta = -40 to 85 °C, V_{DDI} = 2.3 to 3.3V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CW8}	$\overline{CS}$ - $\overline{WR}$, $\overline{RD}$ time	7	-	-	ns	-
A0	t_{AH8}	Address hold time	7	-	-	ns	-
	t_{AW8}	Address setup time	7	-	-	ns	
$\overline{WR}$	t_{CYCW8}	Write cycle	80	-	-	ns	-
	t_{CCHW8}	Control pulse width A	22	-	-	ns	
	t_{CCLW8}	Control pulse width B	28	-	-	ns	
$\overline{RD}$	t_{CYCRI8}	Read cycle (ID)	140	-	-	ns	When read ID data
	t_{CCHRI8}	Control pulse width A (ID)	45	-	-	ns	
	t_{CCLRI8}	Control pulse width B (ID)	35	-	-	ns	
	t_{CYCRR8}	Read cycle (VR)	200	-	-	ns	When read from VRAM
	t_{CCHRR8}	Control pulse width A (VR)	45	-	-	ns	
	t_{CCLRR8}	Control pulse width B (VR)	135	-	-	ns	
LD0 to LD7, D8 to D23	t_{DS8}	Data setup time	7	-	-	ns	-
	t_{DH8}	Data hold time	7	-	-	ns	
	t_{ACCI8}	Read access time (ID)	-	-	35	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{ACCR8}	Read access time (VR)	-	-	130	ns	
	t_{OH8}	Output disable time	15	-	70	ns	

- The rise and fall times of input signals (t_r, t_f) are stipulated as 15 ns or less.
- The t_{ACC8} timings are stipulated relative to 20% and 80% of V_{DDI} – GND.
- The t_{OH8} timings are stipulated relative to intergration point of V_{DDI} – GND.
- Other timings are stipulated relative to 30% and 70% of V_{DDI} – GND.
- t_{CCLW8} and t_{CCLR8} are stipulated for an interval in which $\overline{CS}$ = LOW and $\overline{WR}$, $\overline{RD}$ = LOW overlap.
- The A0 timing is stipulated with respect to an interval in which $\overline{CS}$ = LOW and $\overline{WR}$, $\overline{RD}$ = LOW overlap.
- *§: For write, t_{CCLW8} or more; for read, t_{CCLR8} or more

11-2-2. Read/Write Characteristics (68-series MPU parallel interface)



*1 Access at E when $\overline{CS}$ is "LOW". *2 Access at $\overline{CS}$ when E is "HIGH".

T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CW6}	$\overline{CS}$ -E time	7	-	-	ns	-
A0, R/$\overline{W}$ ($\overline{WR}$)	t_{AH6}	Address hold time	7	-	-	ns	-
	t_{AW6}	Address setup time	7	-	-	ns	
E ($\overline{RD}$)	t_{CYCW6}	Write cycle	74	-	-	ns	-
	t_{CCLW6}	Control pulse width A	22	-	-	ns	
	t_{CCHW6}	Control pulse width B	22	-	-	ns	
	t_{CYCRI6}	Read cycle (ID)	140	-	-	ns	When read ID data
	t_{CCLRI6}	Control pulse width A (ID)	45	-	-	ns	
	t_{CCHRI6}	Control pulse width B (ID)	35	-	-	ns	
	t_{CYCRR6}	Read cycle (VR)	200	-	-	ns	When read from VRAM
	t_{CCLRR6}	Control pulse width A (VR)	45	-	-	ns	
	t_{CCHRR6}	Control pulse width B (VR)	135	-	-	ns	
LD0 to LD7, D8 to D23	t_{DS6}	Data setup time	7	-	-	ns	-
	t_{DH6}	Data hold time	7	-	-	ns	
	t_{ACCI6}	Read access time (ID)	-	-	30	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{ACCR6}	Read access time (VR)	-	-	130	ns	
	t_{OH6}	Output disable time	25	-	70	ns	

MV pin, T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

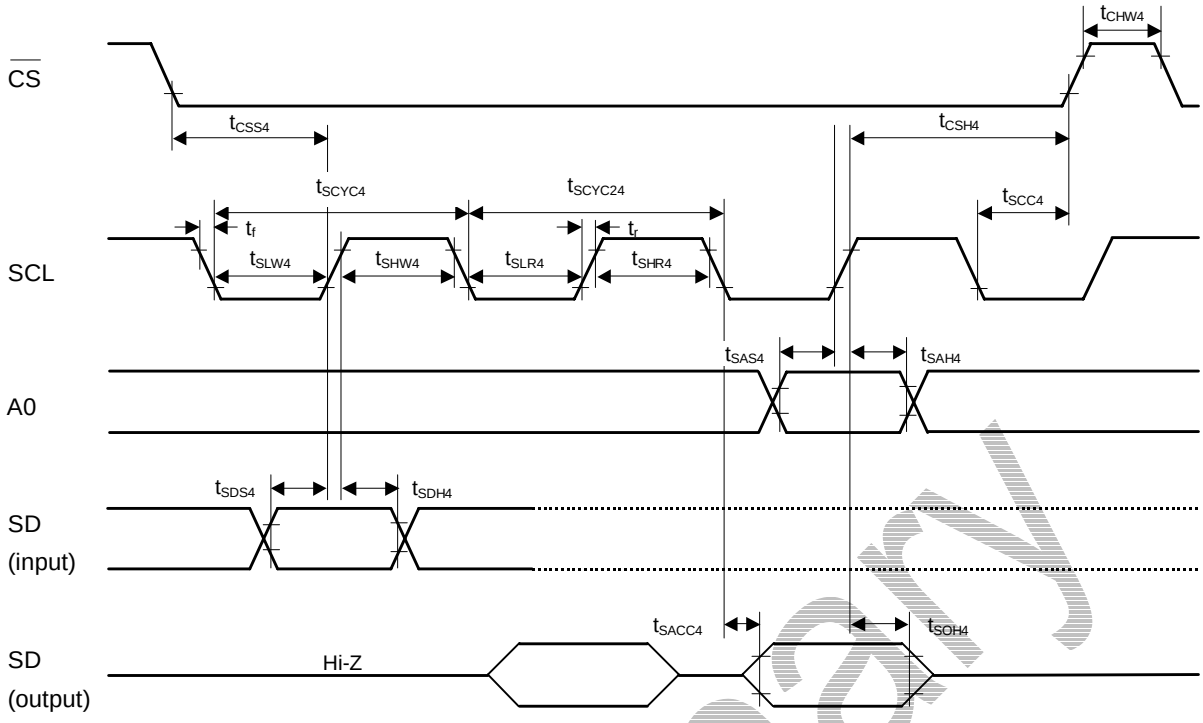
Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CW6}	$\overline{CS}$ -E time	7	-	-	ns	-
A0, R/$\overline{W}$ ($\overline{WR}$)	t_{AH6}	Address hold time	7	-	-	ns	-
	t_{AW6}	Address setup time	7	-	-	ns	
E ($\overline{RD}$)	t_{CYCW6}	Write cycle	84	-	-	ns	-
	t_{CCLW6}	Control pulse width A	22	-	-	ns	
	t_{CCHW6}	Control pulse width B	32	-	-	ns	
	t_{CYCRI6}	Read cycle (ID)	140	-	-	ns	When read ID data
	t_{CCLRI6}	Control pulse width A (ID)	45	-	-	ns	
	t_{CCHRI6}	Control pulse width B (ID)	35	-	-	ns	
	t_{CYCRR6}	Read cycle (VR)	200	-	-	ns	When read from VRAM
	t_{CCLRR6}	Control pulse width A (VR)	45	-	-	ns	
	t_{CCHRR6}	Control pulse width B (VR)	135	-	-	ns	
LD0 to LD7, D8 to D23	t_{DS6}	Data setup time	7	-	-	ns	-
	t_{DH6}	Data hold time	7	-	-	ns	
	t_{ACCI6}	Read access time (ID)	-	-	55	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{ACCR6}	Read access time (VR)	-	-	130	ns	
	t_{OH6}	Output disable time	15	-	70	ns	

MV pin, T_a = -40 to 85 °C, V_{DDI} = 2.3 to 3.3V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CW6}	$\overline{CS}$ -E time	7	-	-	ns	-
A0, R/$\overline{W}$ ($\overline{WR}$)	t_{AH6}	Address hold time	7	-	-	ns	-
	t_{AW6}	Address setup time	7	-	-	ns	
$\overline{E}$ ($\overline{RD}$)	t_{CYCW6}	Write cycle	84	-	-	ns	-
	t_{CCLW6}	Control pulse width A	22	-	-	ns	
	t_{CCHW6}	Control pulse width B	32	-	-	ns	
	t_{CYCRI6}	Read cycle (ID)	140	-	-	ns	When read ID data
	t_{CCLRI6}	Control pulse width A (ID)	45	-	-	ns	
	t_{CCHRI6}	Control pulse width B (ID)	35	-	-	ns	
	t_{CYCRR6}	Read cycle (VR)	200	-	-	ns	When read from VRAM
	t_{CCLRR6}	Control pulse width A (VR)	45	-	-	ns	
	t_{CCHRR6}	Control pulse width B (VR)	135	-	-	ns	
LD0 to LD7, D8 to D23	t_{DS6}	Data setup time	7	-	-	ns	-
	t_{DH6}	Data hold time	7	-	-	ns	
	t_{ACCI6}	Read access time (ID)	-	-	35	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{ACCR6}	Read access time (VR)	-	-	130	ns	
	t_{OH6}	Output disable time	15	-	70	ns	

- The rise and fall times of input signals (t_r, t_f) are stipulated as 15 ns or less.
- The t_{ACC6} timings are stipulated relative to 20% and 80% of V_{DDI} – GND.
- The t_{OH6} timings are stipulated relative to intergration point of V_{DDI} – GND.
- Other timings are stipulated relative to 30% and 70% of V_{DDI} – GND.
- t_{CCLW6} and t_{CCLR6} are stipulated for an interval in which $\overline{CS}$ = LOW and E = HIGH overlap.
- The A0 timing is stipulated with respect to an interval in which $\overline{CS}$ = LOW and E = HIGH overlap.
- *§: For write, t_{CCLW6} or more; for read, t_{CCLR6} or more

11-2-3. Read/Write Characteristics (4-wire, 8-bit data serial interface)



T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CSS4}	$\overline{CS}$ setup time	30	-	-	ns	-
	t_{CSH4}	$\overline{CS}$ hold time	40	-	-	ns	
	t_{CHW4}	$\overline{CS}$ -pulse HIGH width	30	-	-	ns	
	t_{SCC4}	SCL- $\overline{CS}$ time	15	-	-	ns	
A0	t_{SAH4}	Address hold time	10	-	-	ns	-
	t_{SAS4}	Address setup time	10	-	-	ns	
SCL ($\overline{WR}$)	t_{SCYCW4}	Write clock cycle	74	-	-	ns	-
	t_{SHW4}	Clock-pulse HIGH width	22	-	-	ns	
	t_{SLW4}	Clock-pulse LOW width	22	-	-	ns	
	$t_{SCYCRI4}$	Read clock cycle	120	-	-	ns	When read ID data
	t_{SHRI4}	Clock-pulse HIGH width (ID)	45	-	-	ns	
	t_{SLRI4}	Clock-pulse LOW width (ID)	45	-	-	ns	
	$t_{SCYCRR4}$	Read clock cycle	200	-	-	ns	When read from VRAM
	t_{SHRR4}	Clock-pulse HIGH width (VR)	45	-	-	ns	
	t_{SLRR4}	Clock-pulse LOW width (VR)	145	-	-	ns	
LSD	t_{SDS4}	Data setup time	10	-	-	ns	-
	t_{SDH4}	Data hold time	10	-	-	ns	
	t_{SACCI4}	Read access time (ID)	10	-	45	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{SACCR4}	Read access time (VR)	10	-	14	ns	
	t_{SOH4}	Output disable time	20	-	45	ns	

MV pin, T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

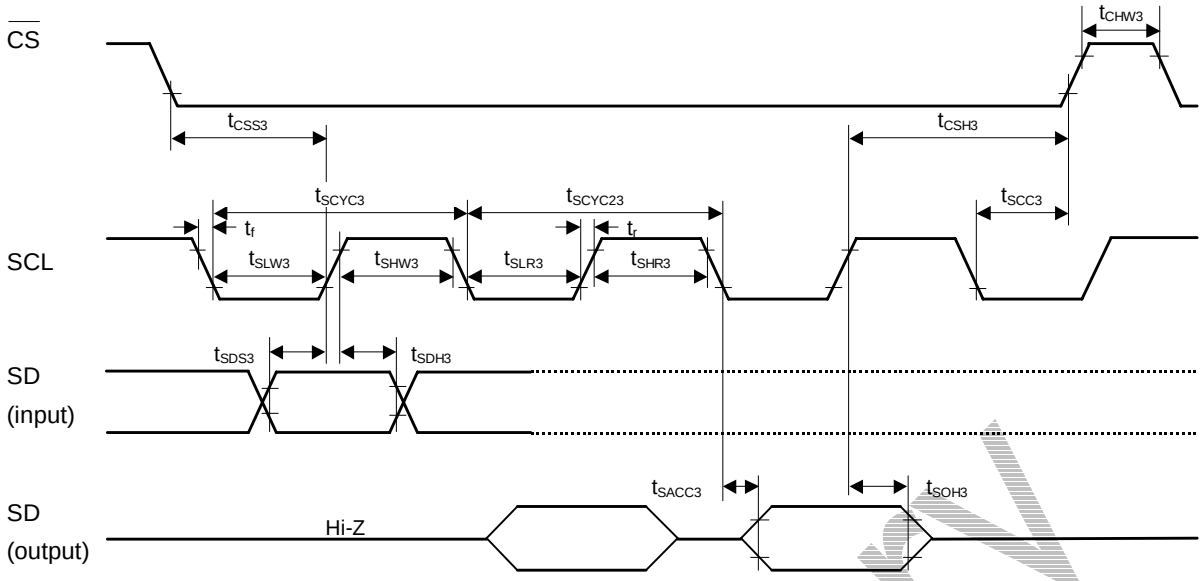
Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CSS4}	$\overline{CS}$ setup time	30	-	-	ns	-
	t_{CSH4}	$\overline{CS}$ hold time	40	-	-	ns	
	t_{CHW4}	$\overline{CS}$ -pulse HIGH width	30	-	-	ns	
	t_{SCC4}	SCL- $\overline{CS}$ time	15	-	-	ns	
A0	t_{SAH4}	Address hold time	10	-	-	ns	-
	t_{SAS4}	Address setup time	10	-	-	ns	
SCL ($\overline{WR}$)	t_{SCYCW4}	Write clock cycle	74	-	-	ns	-
	t_{SHW4}	Clock-pulse HIGH width	22	-	-	ns	
	t_{SLW4}	Clock-pulse LOW width	22	-	-	ns	
	$t_{SCYCRI4}$	Read clock cycle	120	-	-	ns	When read ID data
	t_{SHRI4}	Clock-pulse HIGH width (ID)	45	-	-	ns	
	t_{SLRI4}	Clock-pulse LOW width (ID)	45	-	-	ns	
	$t_{SCYCRR4}$	Read clock cycle	200	-	-	ns	When read from VRAM
	t_{SHRR4}	Clock-pulse HIGH width (VR)	45	-	-	ns	
	t_{SLRR4}	Clock-pulse LOW width (VR)	145	-	-	ns	
SD	t_{SDS4}	Data setup time	10	-	-	ns	-
	t_{SDH4}	Data hold time	10	-	-	ns	
	t_{SACCI4}	Read access time (ID)	5	-	55	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{SACCR4}	Read access time (VR)	5	-	14	ns	
	t_{SOH4}	Output disable time	15	-	60	ns	

MV pin, T_a = -40 to 85 °C, V_{DDI} = 2.3 to 3.3V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CSS4}	$\overline{CS}$ setup time	30	-	-	ns	-
	t_{CSH4}	$\overline{CS}$ hold time	40	-	-	ns	
	t_{CHW4}	$\overline{CS}$ -pulse HIGH width	30	-	-	ns	
	t_{SCC4}	SCL- $\overline{CS}$ time	15	-	-	ns	
A0	t_{SAH4}	Address hold time	10	-	-	ns	-
	t_{SAS4}	Address setup time	10	-	-	ns	
SCL ($\overline{WR}$)	t_{SCYCW4}	Write clock cycle	74	-	-	ns	-
	t_{SHW4}	Clock-pulse HIGH width	22	-	-	ns	
	t_{SLW4}	Clock-pulse LOW width	22	-	-	ns	
	$t_{SCYCRI4}$	Read clock cycle	120	-	-	ns	When read ID data
	t_{SHRI4}	Clock-pulse HIGH width (ID)	45	-	-	ns	
	t_{SLRI4}	Clock-pulse LOW width (ID)	45	-	-	ns	
	$t_{SCYCRR4}$	Read clock cycle	200	-	-	ns	When read from VRAM
	t_{SHRR4}	Clock-pulse HIGH width (VR)	45	-	-	ns	
	t_{SLRR4}	Clock-pulse LOW width (VR)	145	-	-	ns	
SD	t_{SDS4}	Data setup time	10	-	-	ns	-
	t_{SDH4}	Data hold time	10	-	-	ns	
	t_{SACCI4}	Read access time (ID)	5	-	35	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{SACCR4}	Read access time (VR)	5	-	14	ns	
	t_{SOH4}	Output disable time	15	-	55	ns	

- The rise and fall times of input signals (t_r,t_f) are stipulated as 15 ns or less.
- The t_{SACC4} timings are stipulated relative to 20% and 80% of V_{DDI} – GND.
- The t_{SOH4} timings are stipulated relative to intergration point of V_{DDI} – GND.
- Other timings are stipulated relative to 30% and 70% of V_{DDI} – GND.

11-2-4. Read/Write Characteristics (3-wire, 9-bit data serial interface)



T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CSS3}	$\overline{CS}$ setup time	30	-	-	ns	-
	t_{CSH3}	$\overline{CS}$ hold time	40	-	-	ns	
	t_{CHW3}	$\overline{CS}$ -pulse HIGH width	30	-	-	ns	
	t_{SCC3}	SCL $\overline{CS}$ time	15	-	-	ns	
SCL (A0)	t_{SCYCW3}	Write clock cycle	74	-	-	ns	-
	t_{SHW3}	Clock-pulse HIGH width	22	-	-	ns	
	t_{SLW3}	Clock-pulse LOW width	22	-	-	ns	
	$t_{SCYCRI3}$	Read clock cycle	120	-	-	ns	When read ID data
	t_{SHRI3}	Clock-pulse HIGH width (ID)	45	-	-	ns	
	t_{SLRI3}	Clock-pulse LOW width (ID)	45	-	-	ns	
	$t_{SCYCRR3}$	Read clock cycle	200	-	-	ns	When read from VRAM
	t_{SHRR3}	Clock-pulse HIGH width (VR)	45	-	-	ns	
	t_{SLRR3}	Clock-pulse LOW width (VR)	145	-	-	ns	
LSD	t_{SDS3}	Data setup time	10	-	-	ns	-
	t_{SDH3}	Data hold time	10	-	-	ns	
	t_{SACCI3}	Read access time (ID)	5	-	55	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{SACCR3}	Read access time (VR)	5	-	145	ns	
	t_{SOH3}	Output disable time	15	-	60	ns	

MV pin, T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

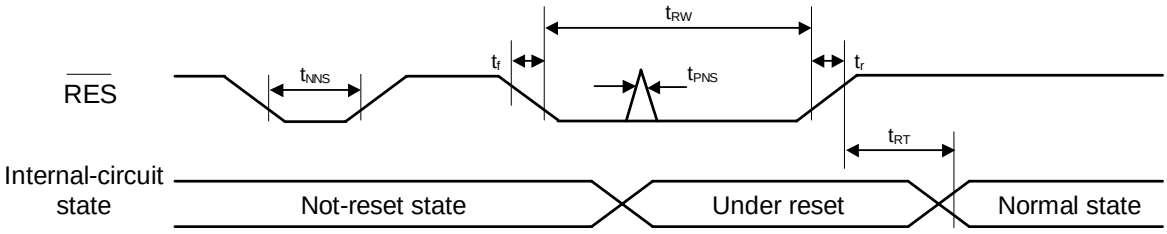
Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CSS3}	$\overline{CS}$ setup time	30	-	-	ns	-
	t_{CSH3}	$\overline{CS}$ hold time	40	-	-	ns	
	t_{CHW3}	$\overline{CS}$ -pulse HIGH width	30	-	-	ns	
	t_{SCC3}	SCL $\overline{CS}$ time	15	-	-	ns	
SCL (A0)	t_{SCYCW3}	Write clock cycle	74	-	-	ns	-
	t_{SHW3}	Clock-pulse HIGH width	22	-	-	ns	
	t_{SLW3}	Clock-pulse LOW width	22	-	-	ns	
	$t_{SCYCRI3}$	Read clock cycle	120	-	-	ns	When read ID data
	t_{SHRI3}	Clock-pulse HIGH width (ID)	45	-	-	ns	
	t_{SLRI3}	Clock-pulse LOW width (ID)	45	-	-	ns	
	$t_{SCYCRR3}$	Read clock cycle	200	-	-	ns	When read from VRAM
	t_{SHRR3}	Clock-pulse HIGH width (VR)	45	-	-	ns	
	t_{SLRR3}	Clock-pulse LOW width (VR)	145	-	-	ns	
SD	t_{SDS3}	Data setup time	10	-	-	ns	-
	t_{SDH3}	Data hold time	10	-	-	ns	
	t_{SACCI3}	Read access time (ID)	5	-	55	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{SACCR3}	Read access time (VR)	5	-	145	ns	
	t_{SOH3}	Output disable time	15	-	60	ns	

MV pin, T_a = -40 to 85 °C, V_{DDI} = 2.3 to 3.3V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{CS}$	t_{CSS3}	$\overline{CS}$ setup time	30	-	-	ns	-
	t_{CSH3}	$\overline{CS}$ hold time	40	-	-	ns	
	t_{CHW3}	$\overline{CS}$ -pulse HIGH width	30	-	-	ns	
	t_{SCC3}	SCL $\overline{CS}$ time	15	-	-	ns	
SCL (A0)	t_{SCYCW3}	Write clock cycle	74	-	-	ns	-
	t_{SHW3}	Clock-pulse HIGH width	22	-	-	ns	
	t_{SLW3}	Clock-pulse LOW width	22	-	-	ns	
	$t_{SCYCRI3}$	Read clock cycle	120	-	-	ns	When read ID data
	t_{SHRI3}	Clock-pulse HIGH width (ID)	45	-	-	ns	
	t_{SLRI3}	Clock-pulse LOW width (ID)	45	-	-	ns	
	$t_{SCYCRR3}$	Read clock cycle	200	-	-	ns	When read from VRAM
	t_{SHRR3}	Clock-pulse HIGH width (VR)	45	-	-	ns	
	t_{SLRR3}	Clock-pulse LOW width (VR)	145	-	-	ns	
SD	t_{SDS3}	Data setup time	10	-	-	ns	-
	t_{SDH3}	Data hold time	10	-	-	ns	
	t_{SACCI3}	Read access time (ID)	5	-	35	ns	Max condition CL = 30 pF Min condition CL = 8 pF
	t_{SACCR3}	Read access time (VR)	5	-	145	ns	
	t_{SOH3}	Output disable time	15	-	55	ns	

- The rise and fall times of input signals (t_r,t_f) are stipulated as 15 ns or less.
- The t_{SACC3} timings are stipulated relative to 20% and 80% of V_{DDI} – GND.
- The t_{SOH3} timings are stipulated relative to intergration point of V_{DDI} – GND.
- Other timings are stipulated relative to 30% and 70% of V_{DDI} – GND.

11-2-5. Reset Timing Characteristics

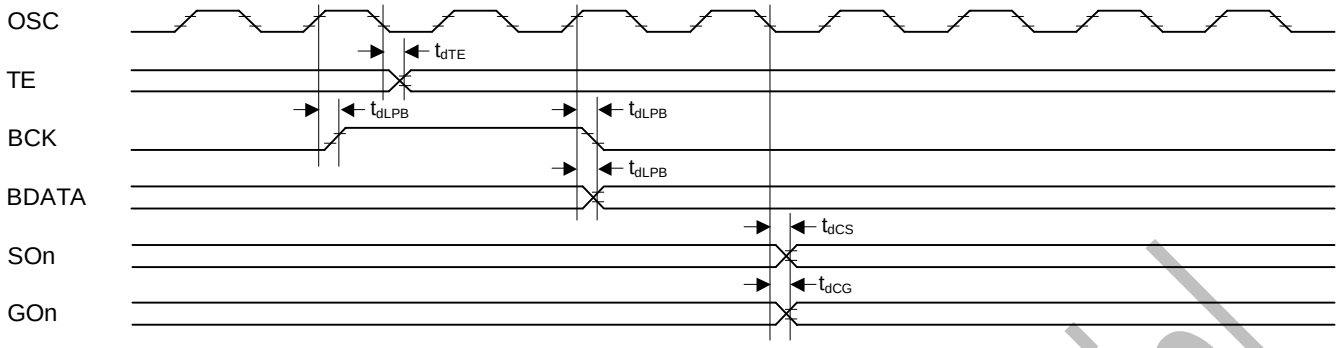


T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
$\overline{RES}$	t_{RW}	Reset pulse width	9	-	-	µs	-
	t_{RT}	Reset release time (when EEPROM is used)	5	-	-	ms	
		Reset release time (when EEPROM is unused)	5	-	-	µs	
	t_{NNS}	Negative-direction dead pulse width	-	-	5	µs	-
	t_{PNS}	Positive-direction dead pulse width	-	-	20	ns	-

- The rise and fall times of input signals (t_r,t_f) are stipulated as 15 ns or less.
- Stipulated relative to 30% and 70% of V_{DDI} – GND
- At the negative-direction dead pulse width of 5 µs (Max.) stipulated above, pulses applied to the $\overline{RES}$ pin with a duration of 5 us do not cause any reaction due to noise or the like.
- At the positive-direction dead pulse width of 20 ns (Max.) stipulated above, pulses applied to the $\overline{RES}$ pin with a duration of 20 ns do not cause any reaction due to noise or the like.
- The reset operation is indeterminate if the asserted duration of $\overline{RES}$ is 5 µs to 9 µs.

11-2-6. Output Timing Characteristics



T_a = -40 to 85°C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

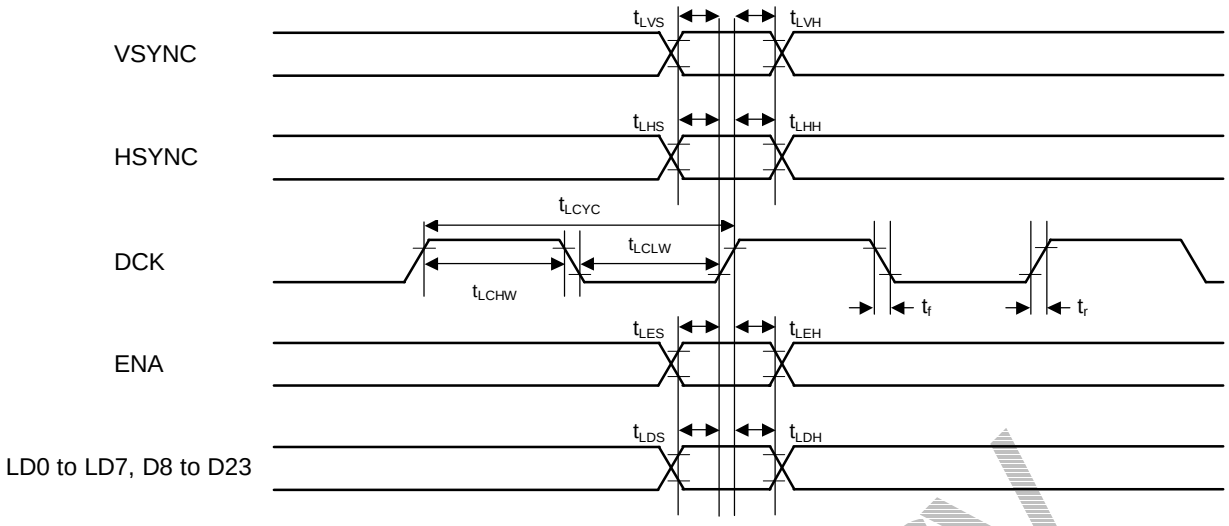
Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
TE	tdTE	TE output delay	-	-	120	ns	CL = 30 pF
DY	tdDY	DY output delay	-	-	120	ns	CL = 30 pF
HSYNCO	tdHS	HSYNCO output delay	-	-	120	ns	CL = 30 pF
BCK, BDATA	tdLPB	BCK, BDATA output delay	-	-	120	ns	CL = 30 pF
SOn	tdCS	SOn output delay	-	4.9	-	µs	CL = 20 pF
GOn	tdCG	GOn output delay	-	-	100	µs	CL = 20 pF

T_a = -40 to 85°C, V_{DDI} = 2.3 to 3.3V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
TE	tdTE	TE output delay	-	-	120	ns	CL = 30 pF
DY	tdDY	DY output delay	-	-	120	ns	CL = 30 pF
HSYNCO	tdHS	HSYNCO output delay	-	-	120	ns	CL = 30 pF
BCK, BDATA	tdLPB	BCK, BDATA output delay	-	-	120	ns	CL = 30 pF
SOn	tdCS	SOn output delay	-	4.9	-	µs	CL = 20 pF
GOn	tdCG	GOn output delay	-	-	100	µs	CL = 20 pF

- The Typ. conditions are V_{DDI} = 1.8 V and V_{DD} = 2.7 V.
- The output-signal timings are stipulated relative to 20% and 80% of the voltage between each power supply and GND.

11-2-7. Write Characteristics (LCDC Interface)



T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
VSYNC	t_{LVS}	VSYNC setup time	7	-	-	ns	
	t_{LVH}	VSYNC hold time	7	-	-	ns	
HSYNC	t_{LHS}	HSYNC setup time	7	-	-	ns	
	t_{LHH}	HSYNC hold time	7	-	-	ns	
DCK	t_{LCYC}	Write cycle	55	-	-	ns	
		Write cycle*1	50			ns	
	t_{LCHW}	DCK-pulse HIGH width	17.5	-	-	ns	-
		DCK-pulse HIGH width*1	15			ns	
	t_{LCLW}	DCK-pulse LOW width	17.5	-	-	ns	
		DCK-pulse LOW width*1	15			ns	
ENA	t_{LES}	ENA setup time	7	-	-	ns	-
	t_{LEH}	ENA hold time	7	-	-	ns	
LD0 to LD7, D8 to D23	t_{LDS}	Data setup time	7	-	-	ns	-
	t_{LDH}	Data hold time	7	-	-	ns	

MV pin, T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V, V_{DD} = 2.3 to 3.3V

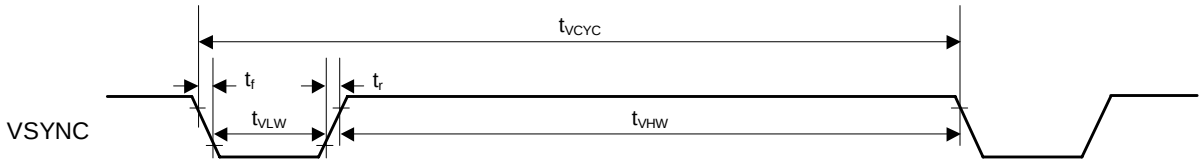
Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
VSYNC	t_{LVS}	VSYNC setup time	7	-	-	ns	
	t_{LVH}	VSYNC hold time	7	-	-	ns	
HSYNC	t_{LHS}	HSYNC setup time	7	-	-	ns	
	t_{LHH}	HSYNC hold time	7	-	-	ns	
DCK	t_{LCYC}	Write cycle	55	-	-	ns	
		Write cycle*1	50			ns	
	t_{LCHW}	DCK-pulse HIGH width	17.5	-	-	ns	-
		DCK-pulse HIGH width*1	15			ns	
	t_{LCLW}	DCK-pulse LOW width	17.5	-	-	ns	
		DCK-pulse LOW width*1	15			ns	
ENA	t_{LES}	ENA setup time	7	-	-	ns	-
	t_{LEH}	ENA hold time	7	-	-	ns	
LD0 to LD7, D8 to D23	t_{LDS}	Data setup time	7	-	-	ns	-
	t_{LDH}	Data hold time	7	-	-	ns	

MV pin, T_a = -40 to 85 °C, V_{DDI} = 2.3 to 3.3V, V_{DD} = 2.3 to 3.3V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
VSYNC	t_{LVS}	VSYNC setup time	7	-	-	ns	
	t_{LVH}	VSYNC hold time	7	-	-	ns	
HSYNC	t_{LHS}	HSYNC setup time	7	-	-	ns	
	t_{LHH}	HSYNC hold time	7	-	-	ns	
DCK	t_{LCYC}	Write cycle	55	-	-	ns	
		Write cycle*1	50			ns	
	t_{LCHW}	DCK-pulse HIGH width	17.5	-	-	ns	-
		DCK-pulse HIGH width*1	15			ns	
	t_{LCLW}	DCK-pulse LOW width	17.5	-	-	ns	
		DCK-pulse LOW width*1	15			ns	
ENA	t_{LES}	ENA setup time	7	-	-	ns	-
	t_{LEH}	ENA hold time	7	-	-	ns	
LD0 to LD7, D8 to D23	t_{LDS}	Data setup time	7	-	-	ns	-
	t_{LDH}	Data hold time	7	-	-	ns	

- The rise and fall times of input signals (tr, tf) are stipulated as 10ns or less.
- *1: This applies to the 8-bit 888 1/3 display-data format.
- The VSYNC/HSYNC cycle times depend on the number of data bytes transferred. For the VSYNC cycle time during external VSYNC synchronization, however, refer to the next section.
- Other timings are stipulated relative to 30% and 70% of V_{DDI} – GND.

11-2-8. Vertical Synchronizing Signal Timing Characteristics (External VSYNC Synchronizing)



T_a = -40 to 85 °C, V_{DDI} = 1.65 to 1.95V

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measurement Condition
VSYNC	t_{VCYC}	VSYNC cycle	1F+2H	-	-	-	-
	t_{VLW}	VSYNC pulse LOW width	1H	-	1F-1H	-	
	t_{VHW}	VSYNC pulse HIGH width	3H	-	-		

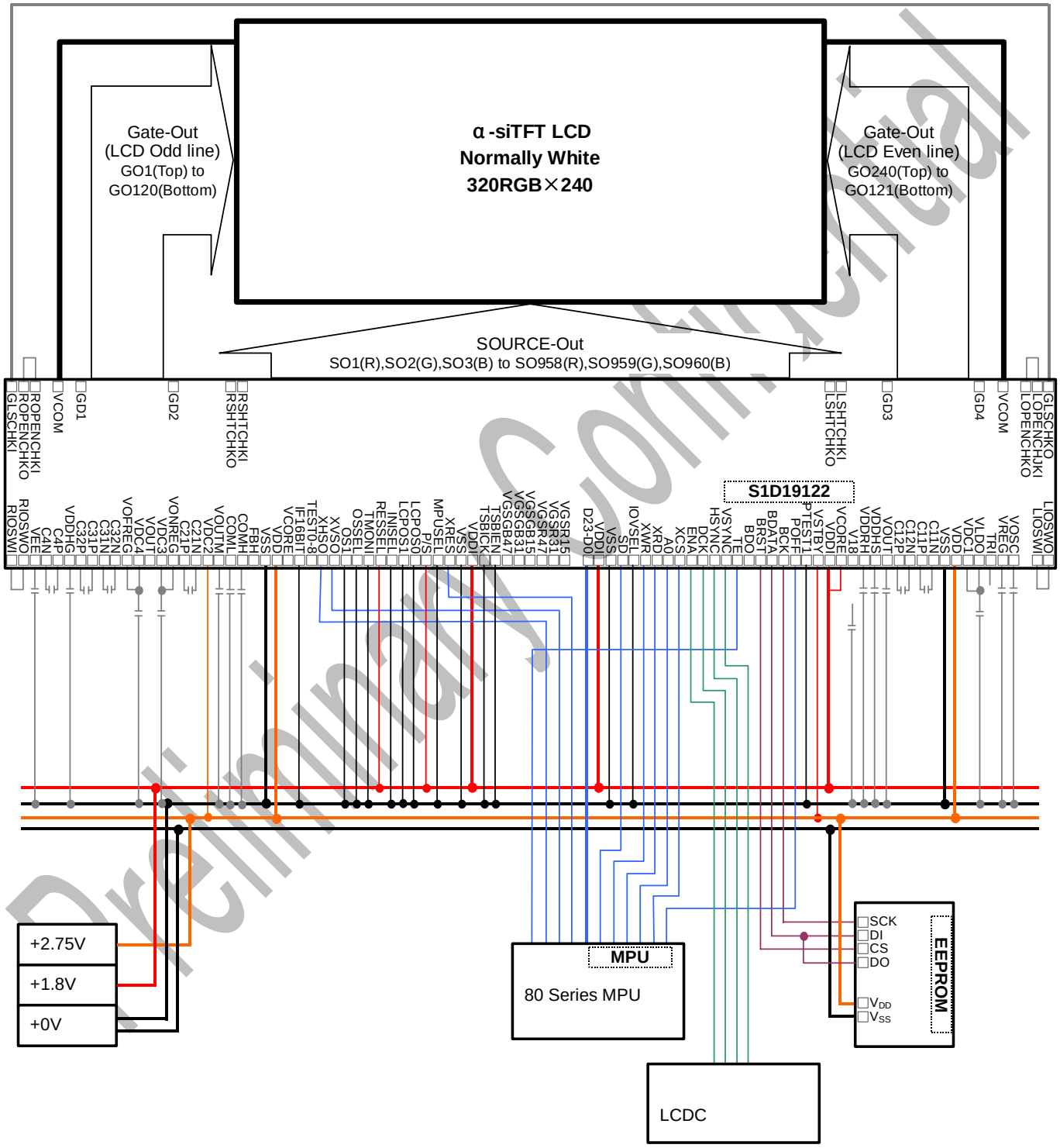
- The rise and fall times of input signals (t_r, t_f) are stipulated as 10ns or less.
- Stipulated relative to 30% and 70% of V_{DDI} – GND.
- These timing characteristics are stipulated for operation during external VSYNC synchronization.
- (F) denotes a 1-frame equivalent time in internally synchronized operation, and (H) denotes a 1-line equivalent time in internally synchronized operation.

12. Actual Example of Usage

This section describes the procedure for using the commands of the S1D19122, using a typical application of the IC as an example.

12-1. Preconditions

The description given here is premised on the assumption that a 320 × 240 TFT LCD module similar to that shown below is used.
(1/240 duty 240-line display LCPOS1=LOW, LCPOS0=LOW)



The power-supply V_{CORE} for the internal logic is externally sourced with V_{DDI} = 1.8 V. To allow the V_{18} power supply to be turned off, V_{STBY} is connected to V_{DD}.

12-2. Actual Example of Usage

12-2-1. At Power-On

(1) Turn system power supply on (V_{CC}).

(2) Always be sure to reset the IC in the hardware after power-on. Refer to Section 8-4-4, “Reset State.”

(3) Wait until IC is initialized.

(4) Input command to change settings. (e.g., to change the scan direction or address-0 position, or set the color mode)

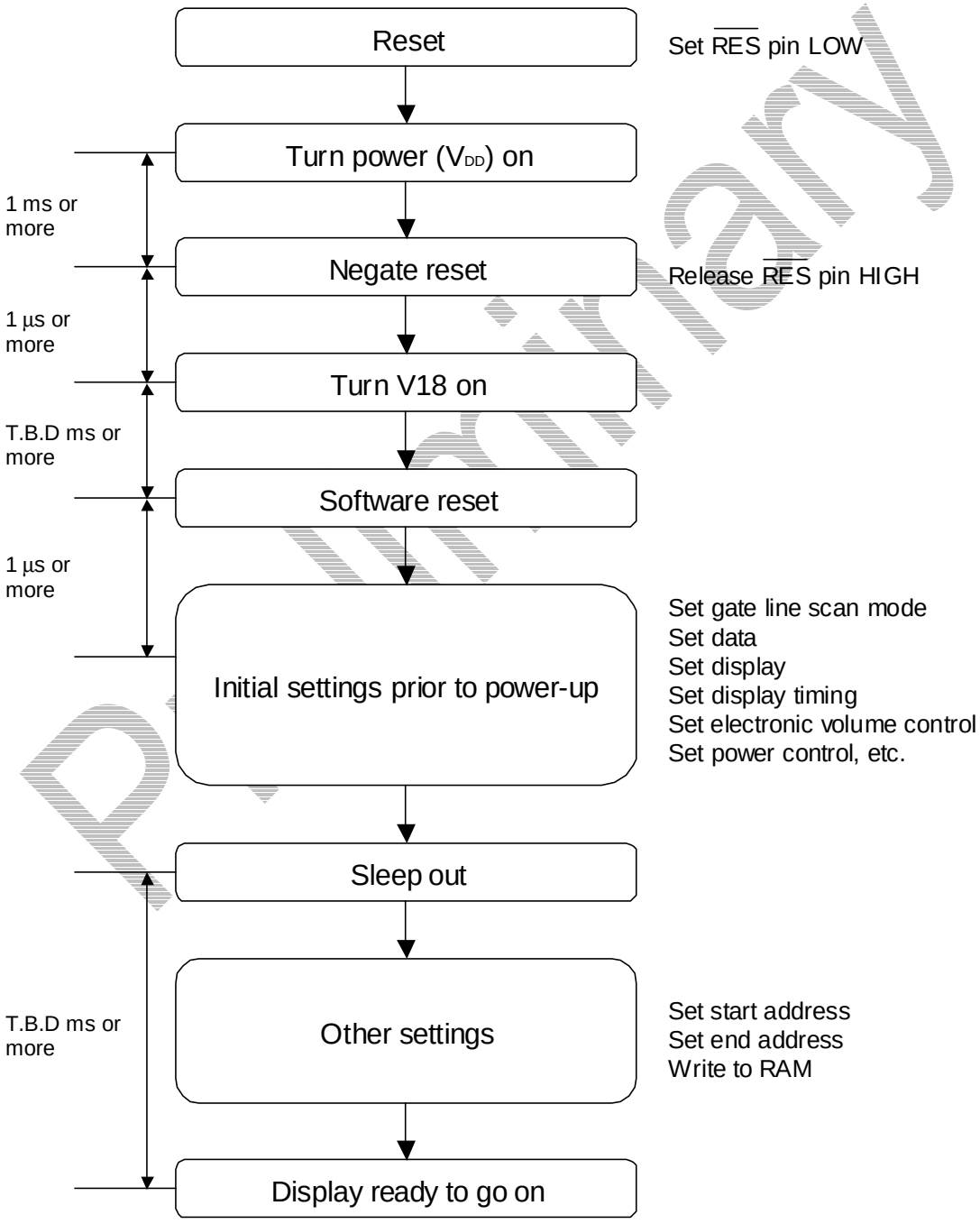
(5) Sleep out (e.g., by issuing SLPOUT)

(6) Set VRAM access area. (e.g., by issuing CASET, PASET, and DADEF)

(7) Input display data. (e.g., input RAMWR write data)

(8) Turn display on. (e.g., issue DISON)

*: For sleep and display on/off, be sure to follow the necessary sequence.



Once the display-ready state is achieved, the display on the LCD panel can be turned on anytime. If a display-on command is received before this state is reached, the command will be automatically delayed until the display is ready to turn on.

12-2-2. During Display (partly rewriting the display content)

(1) During display
(2) Set VRAM access area (e.g., by issuing CASET, PASET, and DADEF)
(3) Input display data (e.g., input RAMWR write data)

12-2-3. During Display (switching to partial display)

(1) During normal display
(2) Set partial area (e.g., by issuing PTLAR)
(3) Partial display (e.g., by issuing PTLON)

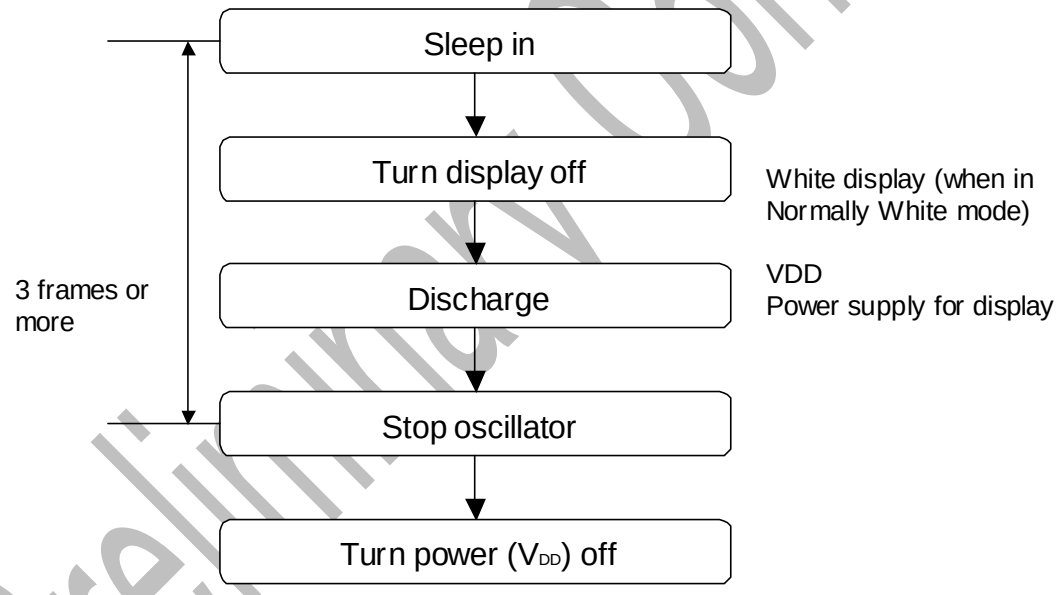
12-2-4. During Display (switching to scroll display)

(1) During normal display
(2) Set scroll area (e.g., by issuing VSCRDEF)
(3) Scroll display (e.g., by entering the VSCRSADD scroll start address)

12-2-5. At Power-Off

(1) During display
(2) Turn display off (e.g., by issuing DISOFF)
(3) Sleep in (e.g., by issuing SLPIN)
(4) Hold power supply for 40 ms
(5) Turn power off

*: For sleep and display on/off, be sure to follow the necessary sequence.



Note: To turn the power supply on again, perform the above procedure beginning with reset in the power-on sequence.

13. Reference Information

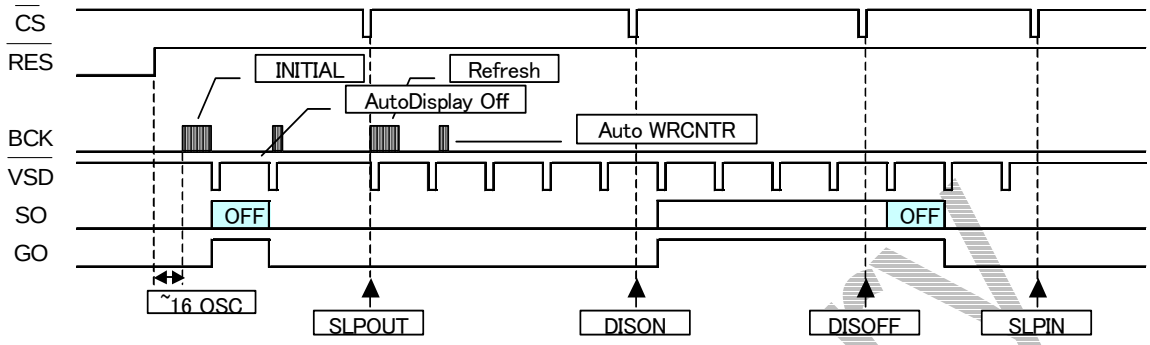
13-1. Timing Diagrams

13-1-1. Timing Diagram 1

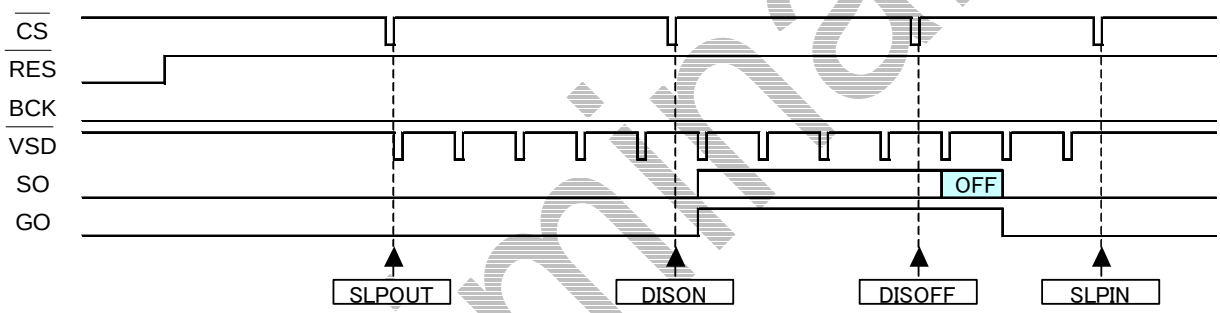
The device operation after reset release and the basic display operation of the IC are shown below.

◇ When EEPROM is used (INISEL = HIGH, RESSEL = HIGH)

If RESSEL = LOW, auto display-off operation (Auto Display Off) is not performed.



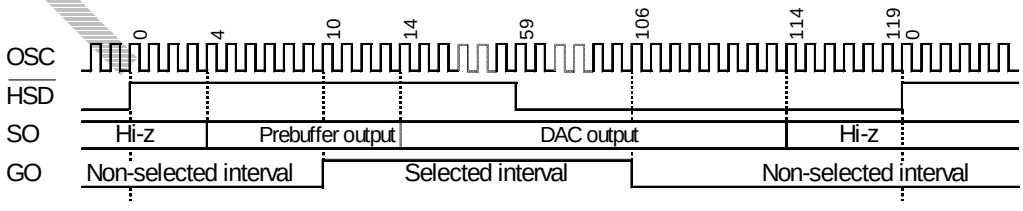
◇ When EEPROM is not used (INISEL = LOW)



13-1-2. Timing Diagram 2

The relationship between the number of clock cycles and the source and gate outputs during a 1H interval is shown below.

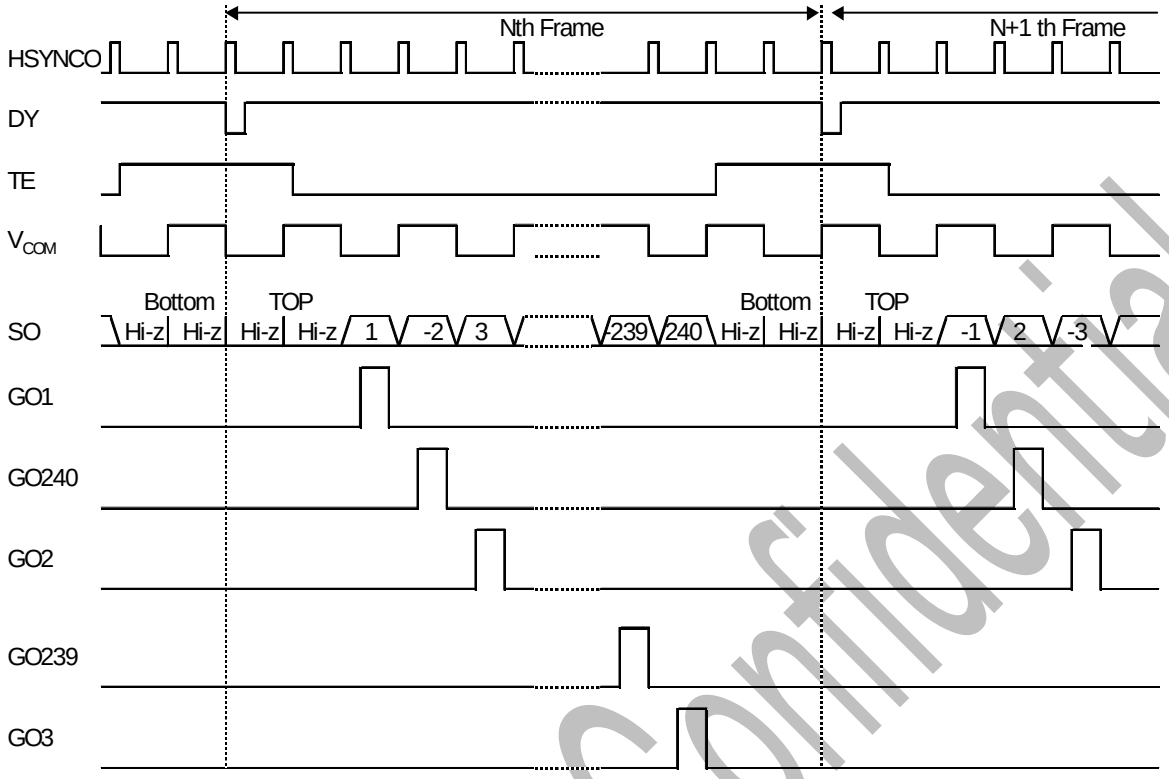
Example: The 1H interval is set to 120 clock cycles
The source output timing is set to 4.
The source prebuffer-off timing is set to 14.
The source output-off timing is set to 114.
The gate output enable timing is set to 8.
The gate output disable timing is set to 106.



13-1-3. Timing Diagram 3

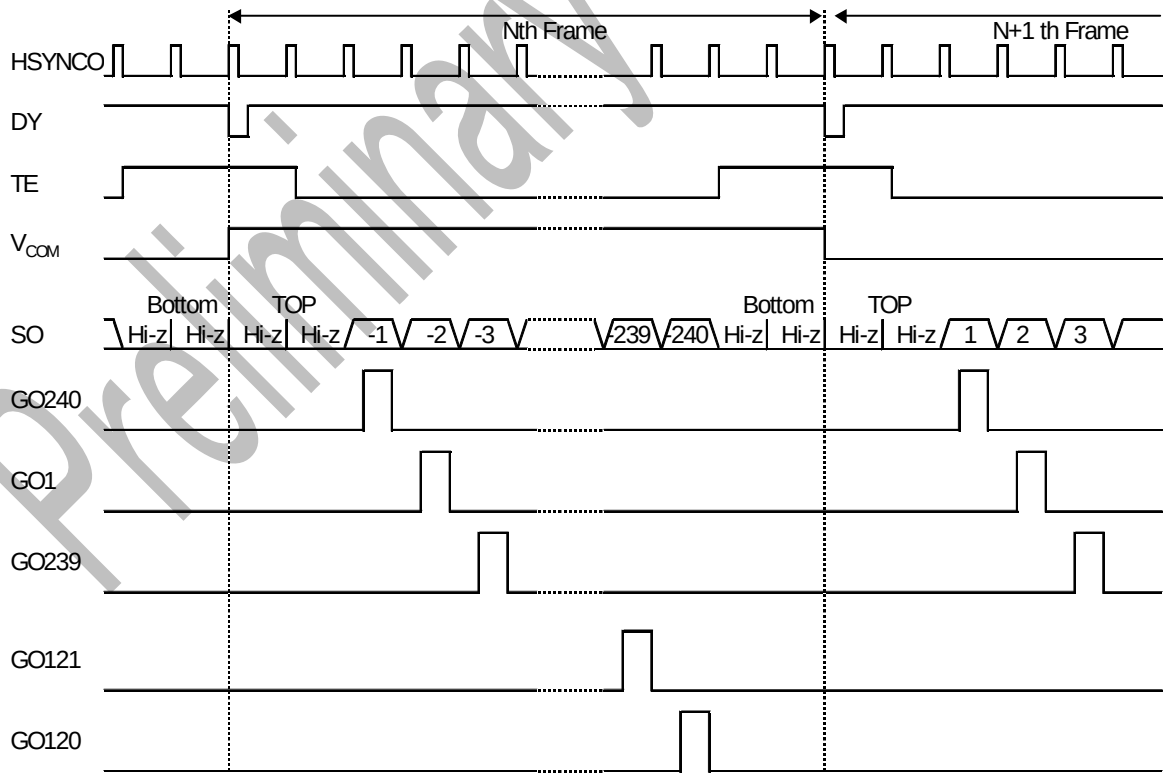
The waveform during V_{COM} square/line inversion drive is as shown below.

Example: LCPOS1 = LOW; LCPOS0 = LOW; 1/244 duty cycle; number of display lines = 240; number of top OFF lines = 2 (number of bottom OFF lines = 2); normal display (NORON)



The waveform during V_{COM} square/frame inversion drive is as shown below.

Example: LCPOS1 = LOW; LCPOS0 = HIGH; 1/244 duty cycle; number of display lines = 240; number of top OFF lines = 2 (number of bottom OFF lines = 2); normal display (NORON)



14. Precautions

Regarding the development specification presented herein, please note the following:

(1) The development specification may be changed for improvements without prior notice.

(2) The development specification does not implicitly or otherwise grant a license to use or guarantee the use of the patent rights or other intellectual property rights owned by third parties or by Seiko Epson Corporation.

The example applications shown in the development specification are provided only to aid the reader in understanding the product described herein; Seiko Epson assumes no responsibility for problems associated with circuits or the like arising from the use of said example applications.

The following precautions should be observed when using the S1D19122.

Handling Precautions Relating to Light

Due to the principle of solar cells, semiconductor devices are generally subject to a change in characteristics when light is irradiated upon them. Therefore, if the IC described herein comes in contact with light, it may operate erratically. If the light to which the IC is exposed is not sufficiently strong to cause erratic operation, it will not show the characteristic changes over time.

(1) When the IC is to be used in an actual system, design the system and mount the IC in it in such a way that the IC will be effectively shielded from light.

(2) In the inspection process, make sure the system is designed and the IC is mounted in it in such a way that the IC will be effectively shielded from light.

(3) Light shielding should be considered for the surface and back, as well as both sides of the IC chip.

Handling Precautions Relating to External Noise, etc.

(1) Although the S1D19122 holds the command-actuated operating state and keeps the display data intact, excessive external noise or the like entering it may cause its internal state to change. When designing a system and mounting the IC in it, incorporate preventive measures to suppress the generation of or minimize the influence of noise.

(2) To protect the IC against sudden noise, it is recommended that the operating state of the IC be periodically refreshed in software (e.g., by resetting the commands and retransferring the display data).

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
HEADQUARTERS
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-800-228-3964 FAX: +1-408-922-0238

SALES OFFICES
West
1960 E.Grand Avenue Flr 2
El Segundo, CA 90245, U.S.A.
Phone: +1-800-249-7730 FAX: +1-310-955-5400

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-800-853-3588 FAX: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 210
Wakefield, MA 01880, U.S.A.
Phone: +1-800-922-7667 FAX: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-332-0020 FAX: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH
HEADQUARTERS
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

DÜSSELDORF BRANCH OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-2171-5045-0 FAX: +49-2171-5045-10

FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-1-64862350 FAX: +33-1-64862355

BARCELONA BRANCH OFFICE
Barcelona Design Center
Edificio Testa, C/Alcalde Barnils 64-68, Modulo C 2a planta
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490 FAX: +34-93-544-2491

UK & IRELAND BRANCH OFFICE
8 The Square, Stockley Park, Uxbridge
Middx UB11 1FW, UNITED KINGDOM
Phone: +44-1295-750-216/+44-1342-824451
FAX: +44-89-14005 446/447

Scotland Design Center
Integration House, The Alba Campus
Livingston West Lothian, EH54 7EG, SCOTLAND
Phone: +44-1506-605040 FAX: +44-1506-605041

ASIA

EPSON (CHINA) CO., LTD.
23F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110
Phone: +886-2-8786-6688 FAX: +886-2-8786-6677

HSINCHU OFFICE
No. 99, Jiangong Road,
Hsinchu City 300
Phone: +886-3-573-9900 FAX: +886-3-573-9169

EPSON SINGAPORE PTE., LTD.
401 Commonwealth Drive, #07-01
Haw Par Technocentre, SINGAPORE 149598
Phone: +65-6586-3100 FAX: +65-6472-4291

SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

GUMI OFFICE
2F, Grand B/D, 457-4 Songjeong-dong,
Gumi-City, KOREA
Phone: +82-54-454-6027 FAX: +82-54-454-6093

SEIKO EPSON CORPORATION
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC Marketing Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

Document Code: **410258800**
First Issue September 2005
Printed July 2005 in JAPAN