

32 x 32 1.5 GBIT/S DIFFERENTIAL CROSSPOINT SWITCH

S2025

FEATURES

- 32 x 32 differential crosspoint switch
- Full broadcast switching capability
- Differential 10K PECL data path
- Configurable differential output driver enables
- Up to 1.5 Gbit/s NRZ data rate
- TTL configuration controls
- Reconfigurable without disturbing operation
- 196-pin LDCC package

APPLICATIONS

- Internet switches
- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

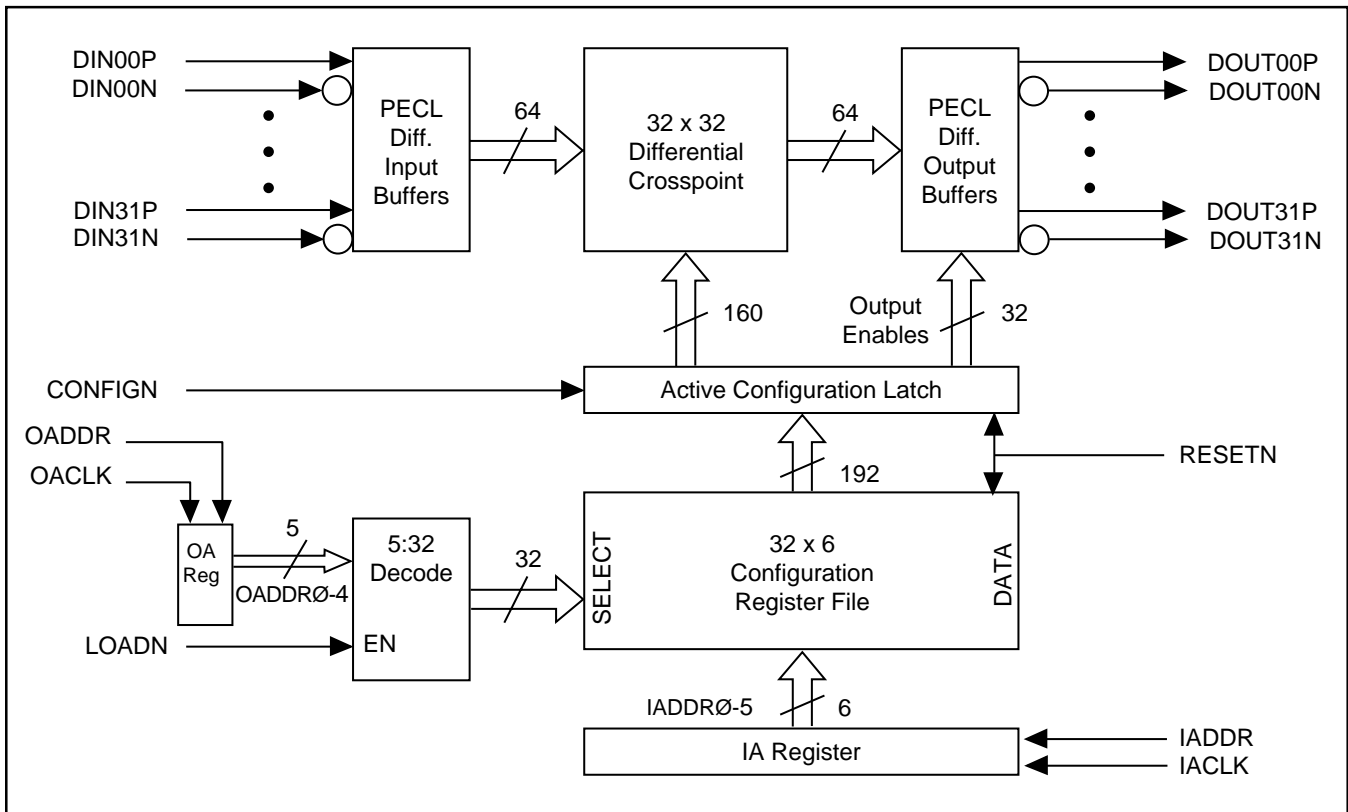
GENERAL DESCRIPTION

The S2025 is a very high-speed 32 x 32 differential crosspoint switch with full broadcast capability. Any of its 32 differential PECL input signal pairs can be connected to any or all of its 32 differential PECL output signal pairs. In addition, the S2025 includes configurable differential output driver enables that allow it to be expanded to larger differential crosspoint switch structures.

The differential 10K PECL logic data path makes the part ideal for high-speed applications. The differential nature of the data path is retained throughout the crosspoint structure, to minimize data distortion and to handle NRZ data rates up to 1.5 gigabits per second.

TTL configuration controls simplify interfacing to slower speed circuitry. Once a new configuration has been entered into the configuration register file, the S2025 can be completely reconfigured in only 6 ns without disturbing switch operations.

Figure 1. Functional Block Diagram



DATA TRANSFER

For each configured connection between a differential input pair and an enabled output pair, any data appearing at the input pair will be passed immediately through to the output pair.

RECONFIGURATION

The S2025 can be selectively reconfigured one output pair at a time, or any number of output pairs can be reconfigured simultaneously. Configuration data is stored in 32 registers, one register for each output pair. As shown in Figure 1, the configuration data is passed in parallel from all 32 registers to a latch which holds the active switch configuration. This two-stage arrangement allows one or more output pairs to be reconfigured simultaneously.

Each configuration register in the configuration Register File (CRF) holds 6 bits. Five bits are used to select which input pair will be connected to the output pair and one bit is used to enable or disable the output pair driver.

To connect an output pair to a given input pair, the output pair to be reconfigured is selected using bits OADDR0-4 of the OA register. These bits are set using the OADDR and OACLK inputs. The OACLK input, with 100 MHz maximum frequency, can load the OA shift register through the OADDR input, with the OADDR4 (MSB) entering first, followed by the OADDR3, and so on. With

the configuration register selected, the desired input selection is provided on the bits IADDR0-4 of the IA register. Whether or not the output pair is to be enabled is provided on the bit IADDR5 (1 = enable, 0 = disable) of the same register. The bits IADDR0-5 are set using the IADDR and IACLK inputs. The IACLK input, with 100 MHz maximum frequency, can load the IA shift register through the IADDR input, with the IADDR5 entering first, followed by the IADDR4 (MSB), and so on. The IADDR0-5 information will be stored into the selected configuration register by the LOADN strobe.

When the differential switch is to be reconfigured, the S2025 minimizes the time required through the use of an active configuration latch. While the switch is operational, and prior to the time at which it must be reconfigured, a new configuration can be loaded into the output pair configuration registers. Once the 32 output pair configuration registers contain the desired connection and output pair driver enable information, the contents of the registers are transferred in parallel to the active configuration latch by the CONFIGN strobe. This allows multiple connections to be simultaneously changed.

The configuration latch can be made transparent by tying the CONFIGN input to a logic 0. When this is done, changes strobed into the output pair configuration registers by the LOADN input pair will be passed immediately to the switch.

Figure 2. Data Transfer Waveforms

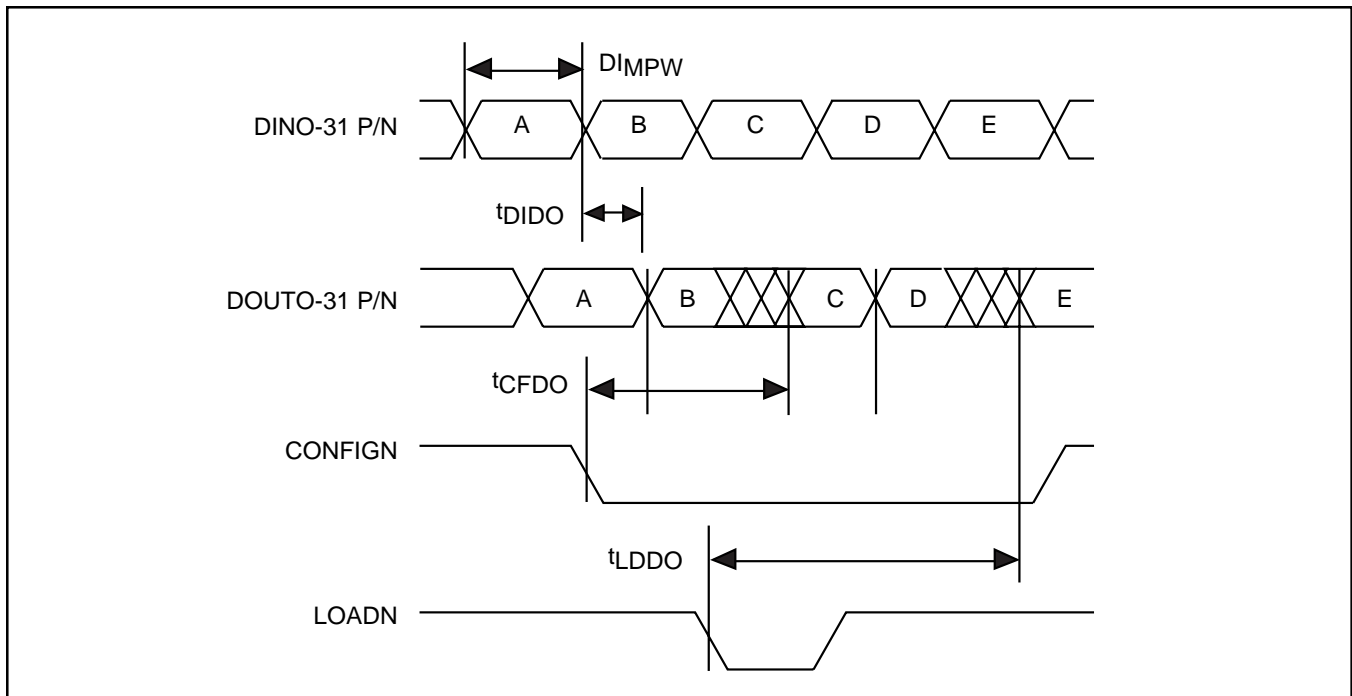
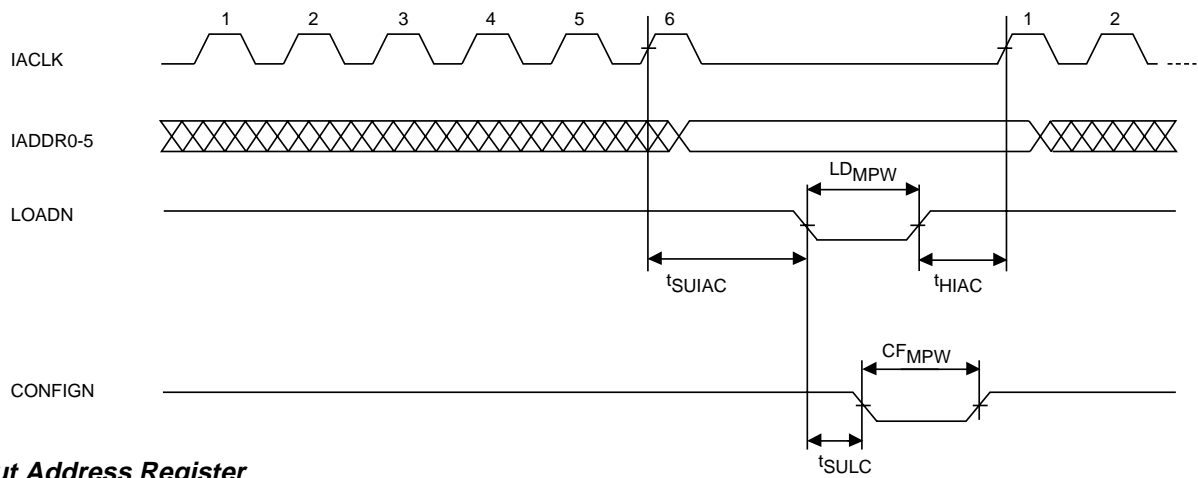
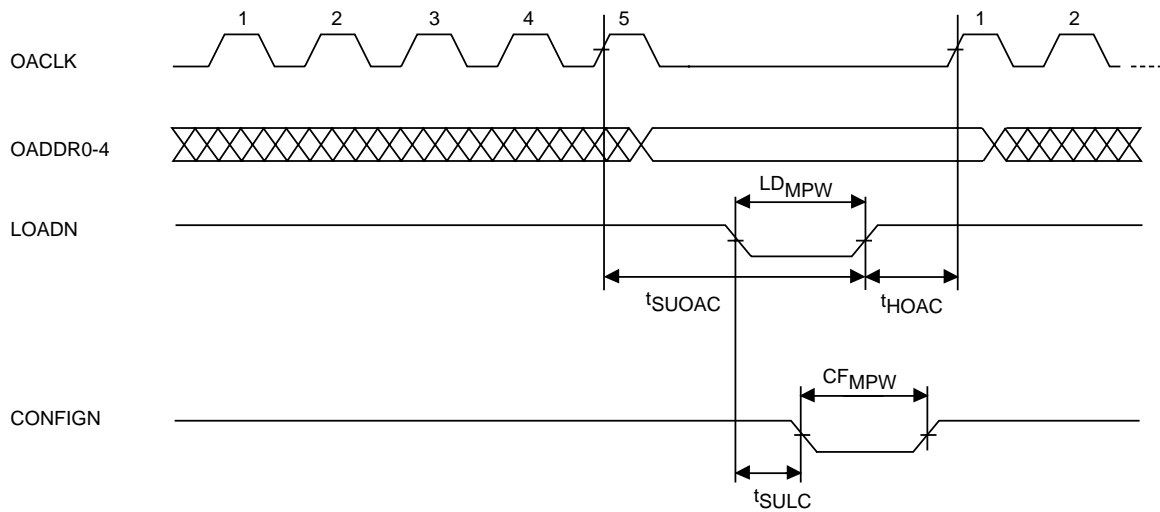


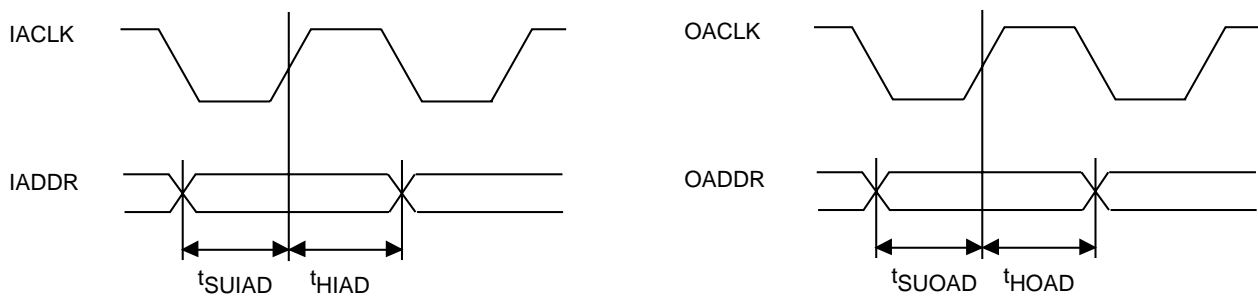
Figure 3. Reconfiguration Waveforms



a. Input Address Register



b. Output Address Register



c. Clock Timing

Reset Behavior

When the RESETN input pair is asserted, the S2025 assumes a configuration where all the differential output drivers are disabled. Individual output drivers then remain disabled until they are explicitly reconfigured to be enabled.

Table 1. Data Transfer Timing¹

Symbol	Description	Min.	Max.	Units
t_{DIDO}	Propagation delay from DIN0–31 P/N to DOUT0–31 P/N		3	ns
t_{CFDO}	Propagation delay from falling edge of CONFIGN to DOUT0–31 P/N valid		6	ns
t_{LDDO}	Propagation delay from falling edge of LOADN to DOUT0–31 P/N valid (When CONFIGN is held low)		8	ns
D_{IMPW}	Pulse width of DIN0–31 P/N	0.650		ns
F_{MAX}	Data rate	1500		Mbit/s

Table 2. Reconfiguration Timing²

Symbol	Description	Min.	Max.	Units
t_{SUIAD}	Setup time of IADDR before rising edge of IACLK	2		ns
t_{HIAD}	Hold time of IADDR after rising edge of IACLK	1		ns
t_{SUIAC}	Setup time of IACLK before falling edge of LOADN	1		ns
t_{HIAC}	Hold time of IACLK after rising edge of LOADN	2		ns
t_{SUOAD}	Setup time of OADDR before rising edge of OACLK	2		ns
t_{HOAD}	Hold time of OADDR after rising edge of OACLK	1		ns
t_{SUOAC}	Setup time of OACLK before falling edge of LOADN	2		ns
t_{HOAC}	Hold time of OACLK after rising edge of LOADN	2		ns
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	1		ns
LD_{MPW}	Pulse width low of LOADN	4.5		ns
CF_{MPW}	Pulse width low of CONFIGN	4.5		ns
F_{MAX}	IACLK, OACLK maximum frequency	100		MHz

1. All timing measured from the $V_{CC} - 1.3V$ point on the signals.
2. All timing measured from the 1.5V point on the signals.

Table 3. S2025 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DIN31P	Diff. PECL	Input Pairs	99	Input data. Differential. Can be used as single-ended input pairs with V_{BB} tied to one side of each differential pair.
DIN31N			100	
DIN30P			45	
DIN30N			48	
DIN29P			101	
DIN29N			103	
DIN28P			43	
DIN28N			44	
DIN27P			104	
DIN27N			107	
DIN26P			42	
DIN26N			41	
DIN25P			105	
DIN25N			110	
DIN24P			39	
DIN24N			37	
DIN23P			106	
DIN23N			111	
DIN22P			38	
DIN22N			33	
DIN21P			109	
DIN21N			115	
DIN20P			31	
DIN20N			36	
DIN19P			116	
DIN19N			112	
DIN18P			29	
DIN18N			32	
DIN17P			118	
DIN17N			117	
DIN16P			23	
DIN16N			30	
DIN15P			121	
DIN15N			119	
DIN14P	27			
DIN14N	21			
DIN13P	127			
DIN13N	125			
DIN12P	20			
DIN12N	19			
DIN11P	129			
DIN11N	128			
DIN10P	18			
DIN10N	15			
DIN9P	134			
DIN9N	130			
DIN8P	13			
DIN8N	14			
DIN7P	137			
DIN7N	131			
DIN6P	12			
DIN6N	11			

Table 3. S2025 Pin Assignment and Descriptions (continued)

Pin Name	Level	I/O	Pin #	Description
DIN5P DIN5N DIN4P DIN4N DIN3P DIN3N DIN2P DIN2N DIN1P DIN1N DIN0P DIN0N	Diff. PECL	I	140 141 9 8 143 142 6 7 146 145 3 5	Differential PECL input data. Differential inputs can be used as single-ended inputs with VBB tied to one side of each differential input pair.
OADDR	TTL	I	160	Serial data input to the Output Address Shift Register
OACLK	TTL	I	181	Output Address Shift Register is loaded on the rising edge of OACLK.
IADDR	TTL	I	86	Serial data input to the Input Address Shift Register. IADDR5 is the output buffer enable bit (1 = enable, 0 = disable).
IACLK	TTL	I	65	Input Address Shift Register is loaded on the rising edge of IACLK.
LOADN	TTL	I	135	Load strobe, active Low. When low, stores the configuration data in IA register into the configuration register file.
CONFIGN	TTL	I	139	Configuration strobe, active Low. When low, parallel loads the contents of the configuration register file into the active configuration latch.
RESETN	TTL	I	136	Reset. Active Low. Resets all the output enable bits in the configuration register file and in the active configuration latch.
DOUT31P DOUT31N DOUT30P DOUT30N DOUT29P DOUT29N DOUT28P DOUT28N DOUT27P DOUT27N DOUT26P DOUT26N	Diff. PECL	O	96 94 92 93 89 91 87 90 85 83 82 80	Output data. Differential.

Table 3. S2025 Pin Assignment and Descriptions (continued)

Pin Name	Level	I/O	Pin #	Description
DOUT25P	Diff. PECL	O	79	Output data. Differential.
DOUT25N			78	
DOUT24P			70	
DOUT24N			77	
DOUT23P			68	
DOUT23N			72	
DOUT22P			66	
DOUT22N			69	
DOUT21P			64	
DOUT21N			62	
DOUT20P			59	
DOUT20N			61	
DOUT19P			58	
DOUT19N			57	
DOUT18P			55	
DOUT18N			56	
DOUT17P			52	
DOUT17N			54	
DOUT16P			47	
DOUT16N			49	
DOUT15P			1	
DOUT15N			2	
DOUT14P			194	
DOUT14N			192	
DOUT13P			190	
DOUT13N			191	
DOUT12P			188	
DOUT12N			189	
DOUT11P			185	
DOUT11N			187	
DOUT10P			183	
DOUT10N			184	
DOUT9P	179			
DOUT9N	180			
DOUT8P	176			
DOUT8N	177			
DOUT7P	169			
DOUT7N	175			
DOUT6P	174			
DOUT6N	167			
DOUT5P	166			
DOUT5N	164			
DOUT4P	163			
DOUT4N	161			
DOUT3P	157			
DOUT3N	159			
DOUT2P	156			
DOUT2N	155			
DOUT1P	154			
DOUT1N	152			
DOUT0P	153			
DOUT0N	150			

Table 3. S2025 Pin Assignment and Descriptions (continued)

Pin Name	Level	I/O	Pin #	Description
VCC	+5V	–	4, 10, 16, 22, 28, 34, 40, 46, 51, 53, 60, 67, 71, 74, 81, 88, 95, 97, 102, 108, 114, 120, 126, 132, 138, 144, 149, 151, 158, 165, 168, 172, 178, 186, 193, 195	Core and ECL I/O Power Supplies
TTLGND	GND	–	50, 98, 148, 196	TTL Ground
ECLGND	GND	–	17, 24, 25, 26, 35, 63, 73, 75, 76, 84, 113, 122, 123, 124, 133, 162, 170, 171, 173, 182	Core Ground

Figure 4. S2025 Pinout

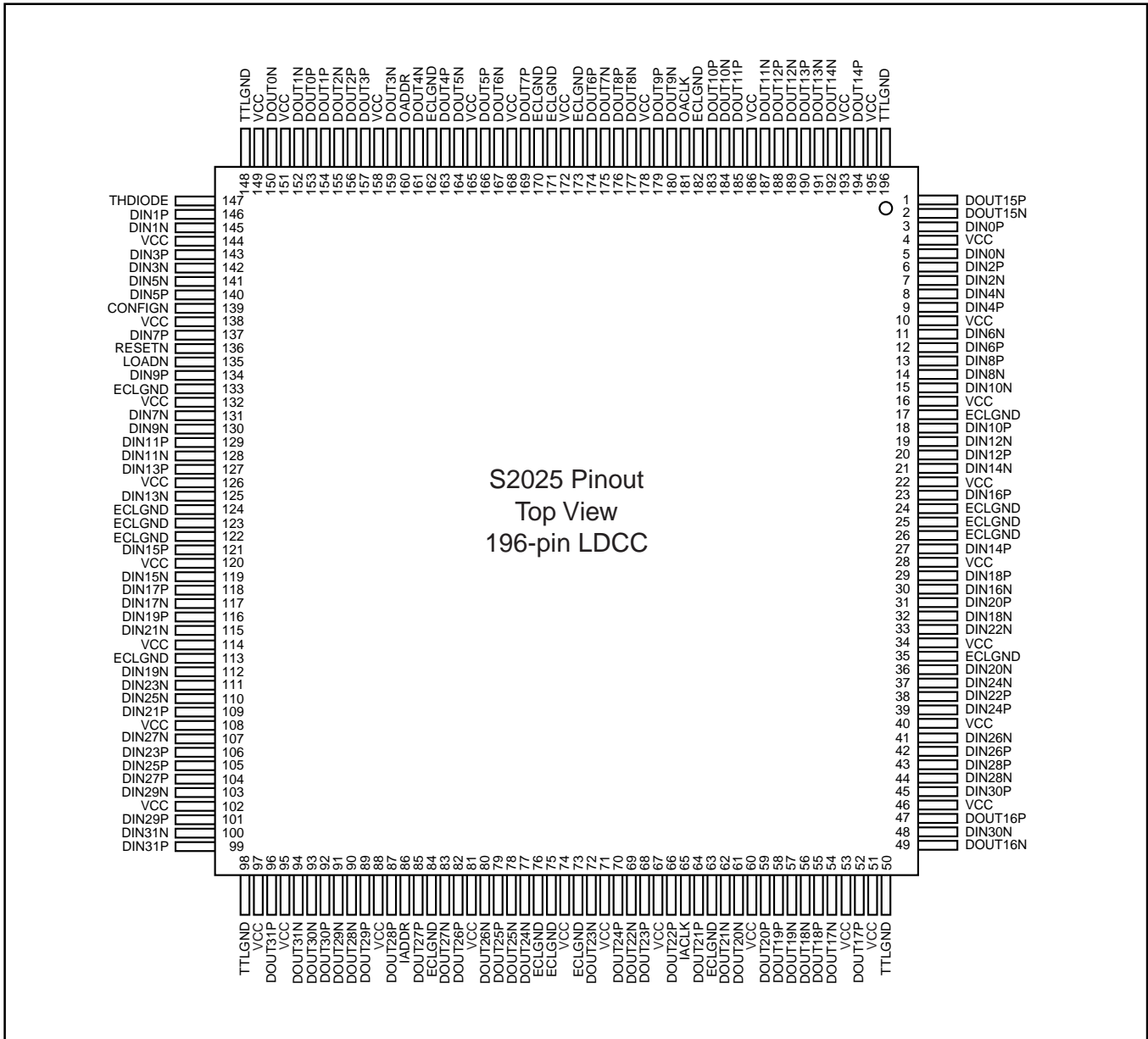
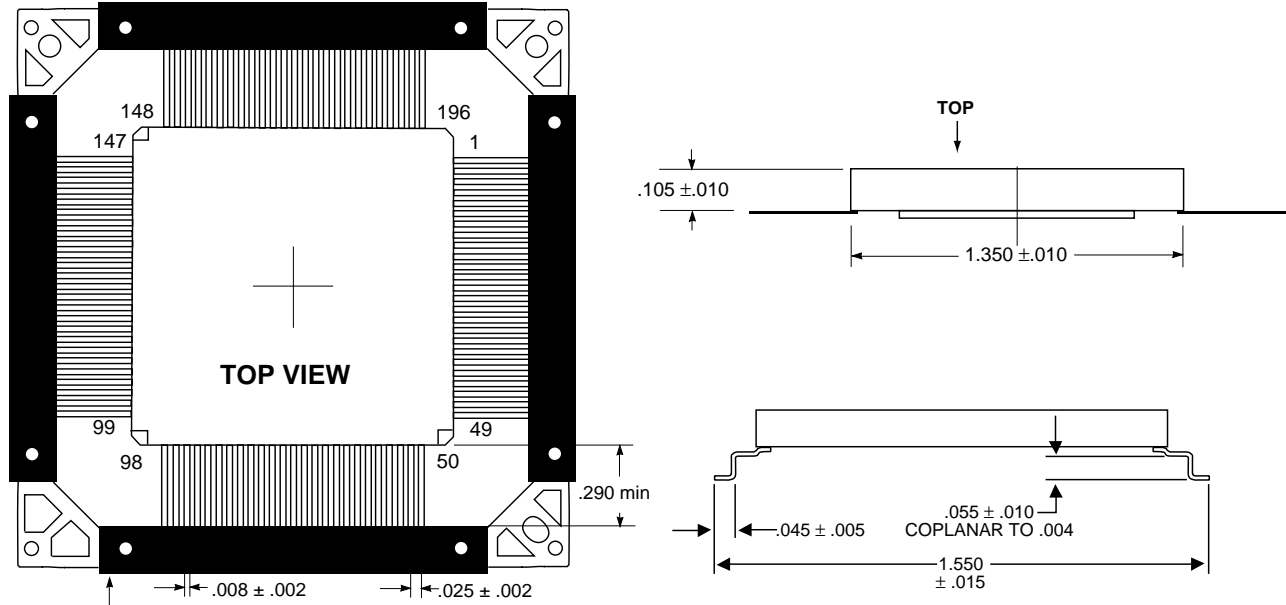


Figure 5. 196-Pin LDCC Package



Non-conductive Tie-bar*

All dimensions nominal in inches.

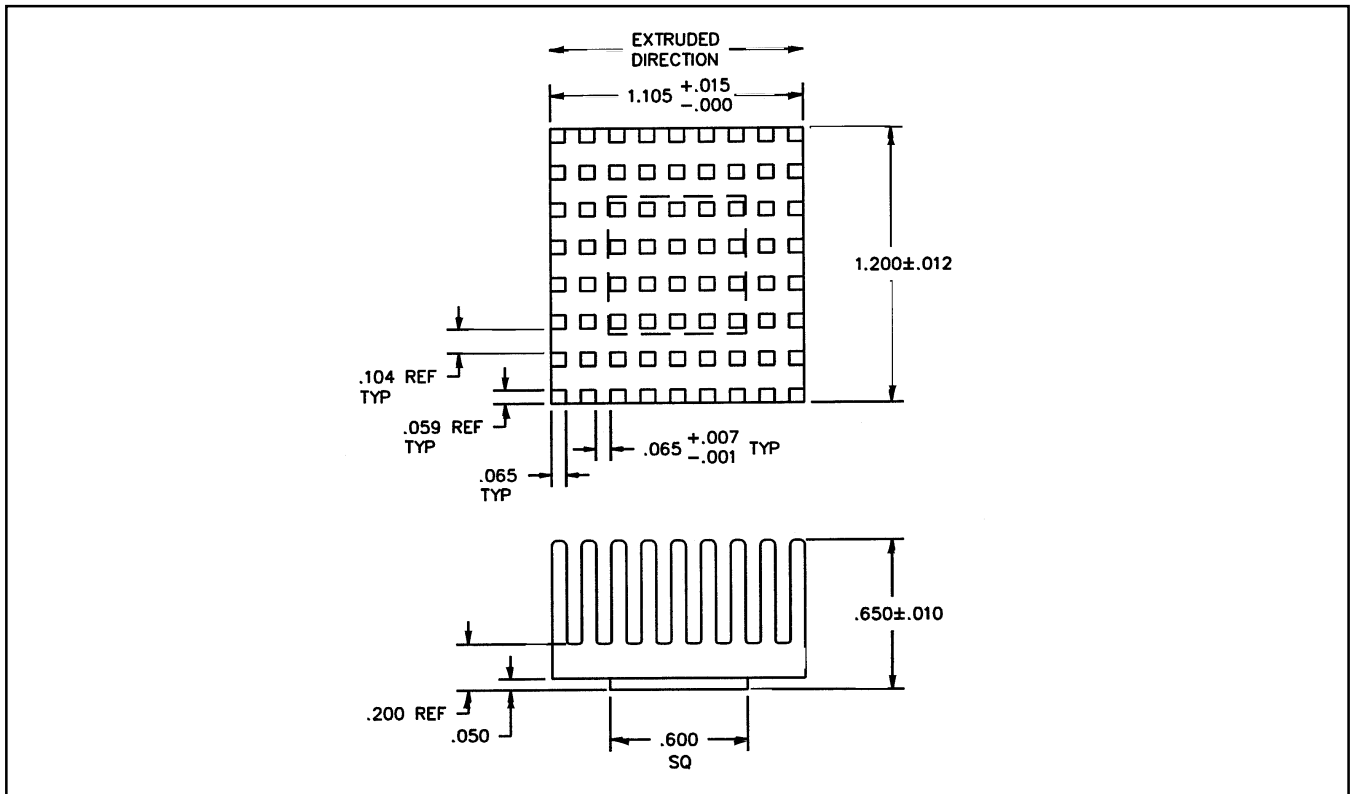
* Trim non-conductive tie-bar prior to board attachment

Thermal Management

Symbol	Description	Airflow	Value	Units
Θ_{jc}	Thermal resistance from junction to case		2.3	$^{\circ}\text{C}/\text{W}$
Θ_{ja}	Thermal resistance from junction to ambient	Still air	25.6	$^{\circ}\text{C}/\text{W}$
Θ_{ja}	Thermal resistance from junction to ambient with heatsink	800 LFPM	3.53	$^{\circ}\text{C}/\text{W}$

Note: S2025 requires an AMCC heatsink 45-17 with an airflow of 800 LFPM for operation over commercial temperatures.

Figure 6. AMCC Heat Sink 45-17



THERMAL MANAGEMENT GUIDELINES

Because of the relatively high power dissipation of the S2025 device, thermal management is a key design consideration. The junction temperature (T_j) of the device must not exceed 150°C for it to operate within its specifications. There are a number of ways to implement thermal management, depending upon the system requirements and applications. AMCC is offering the following two methods as guidelines to ensure proper operation of the S2025.

1. Convection—Heat Sink with Forced Air Flow

AMCC offers the standard heat sink 45-17 for impingement cooling (air flow forced directly to the face of the heat sink). This method is similar to the fan/heat-sink devices used on new, high-performance, and high-power microprocessors. The dimensions of the heat sink are given in Figure 6.

Considering the junction-to-case, and case-to-ambient thermal resistivities, one can estimate the amount of required air flow and the maximum ambient temperature (T_a) in order to keep the T_j below the critical limit of 150°C. Table 4 lists these values for 45-17 and 45-24 heat sinks when $T_j = 150^\circ\text{C}$.

Table 4. Maximum Ambient Temperatures

T_a °C (max) (H/S 45-17)	Air Flow (LFPM)
30	200
50	400
60	600
70	800

2. Conduction—Liquid Cooling Methods

Passive cooling schemes, such as Aavid Engineering's Oasis technology may also be used to ensure low junction temperature. Oasis uses Flourinert, a liquid that boils around 57°C, to transfer heat from the hot device to a condenser, where the vaporized Flourinert is cooled, becomes liquid again, and returns to the hot device. The S2025 case temperature would not exceed 57°C, as long as the cooling system is functioning properly. In such case, using the following equation, one could calculate the maximum anticipated T_j to be around 85°C.

$$T_j = T_c + (Pd \times 2)$$

(T_c is the case temperature in °C, and
 Pd is the dissipated power in Watts.)

For more information on Oasis technology, please contact:

Aavid Engineering Incorporated
 Oasis Products Group
 One Kool Path/P.O. Box 400
 Laconia, NH 03247-0400
 Tel: 603/528-3400
 FAX: 603/528-1478

Table 5. Absolute Maximum Ratings

Supply Voltage V_{CC}	7.0V
PECL Input Voltage	$V_{CC} - 2.5V$ to V_{CC}
PECL Output Source Current (continuous)	-50mA DC
TTL Input Voltage	5.5V
Operating Junction Temperature T_j	+150°C
Storage Temperature	-65°C to +150°C

Table 6. Recommended Operating Conditions

Parameter	Min	Nom	Max	Units
Supply Voltage V_{CC}	4.75	5.0	5.25	V
Ambient Temperature	0		70	°C
Junction Temperature			150	°C
I_{CC}		1950	2600	mA

Table 7. TTL Input DC Characteristics

Symbol	Parameter	Conditions	Commercial 0° to 70°C			Unit
			Min	Typ ²	Max	
V_{IH}^1	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all input pairs	2.0			V
V_{IL}^1	Input LOW Voltage	Guaranteed Input LOW Voltage for all input pairs			0.8	V
V_{IK}	Input Clamp Diode Voltage	$V_{CC} = \text{MIN}, I_{IN} = -18 \text{ mA}$		-0.8	-1.2	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{MAX}, V_{IN} = 2.7V$			50	μA
I_I	Input HIGH Current at Max.	$V_{CC} = \text{MAX}, V_{IN} = V_{CC} + 0.3V$			1	mA
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}, V_{IN} = 0.5V$			-0.4	mA

1. Typical limits are at 25°C, $V_{CC} = 5.0V$.

2. These input levels provide a zero noise immunity and should only be tested in a static, noise-free environment.

Figure 7. Differential Input Voltage

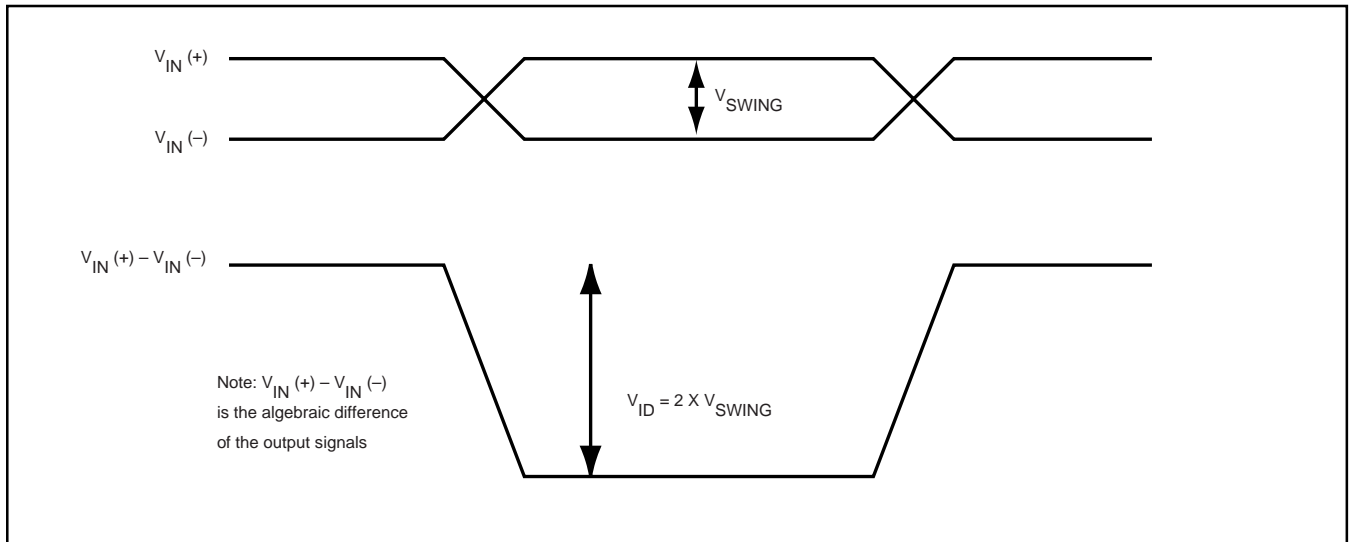


Table 8. PECL DC Characteristics³

Symbol	Min	Typ	Max	Units
V_{IH}^2	$V_{CC} - 1145$		$V_{CC} - 600$	mV
V_{IL}^2	$V_{CC} - 2000$		$V_{CC} - 1400$	mV
V_{BIAS}^2		$V_{CC} - 1300$		mV
I_{IH}^2			30	μA
I_{IL}^2			-.5	μA

1. Internal bias point.
2. Single ended connection.
3. DC is considered to be an input signal between 0 Hz and 1 KHz.

Table 9. Differential PECL Characteristics

Symbol	Min	Typ	Max	Units
V_{ID}^1	500		2800	mV

1. Differential input voltage – algebraic difference

Figure 8. Differential Output Voltage

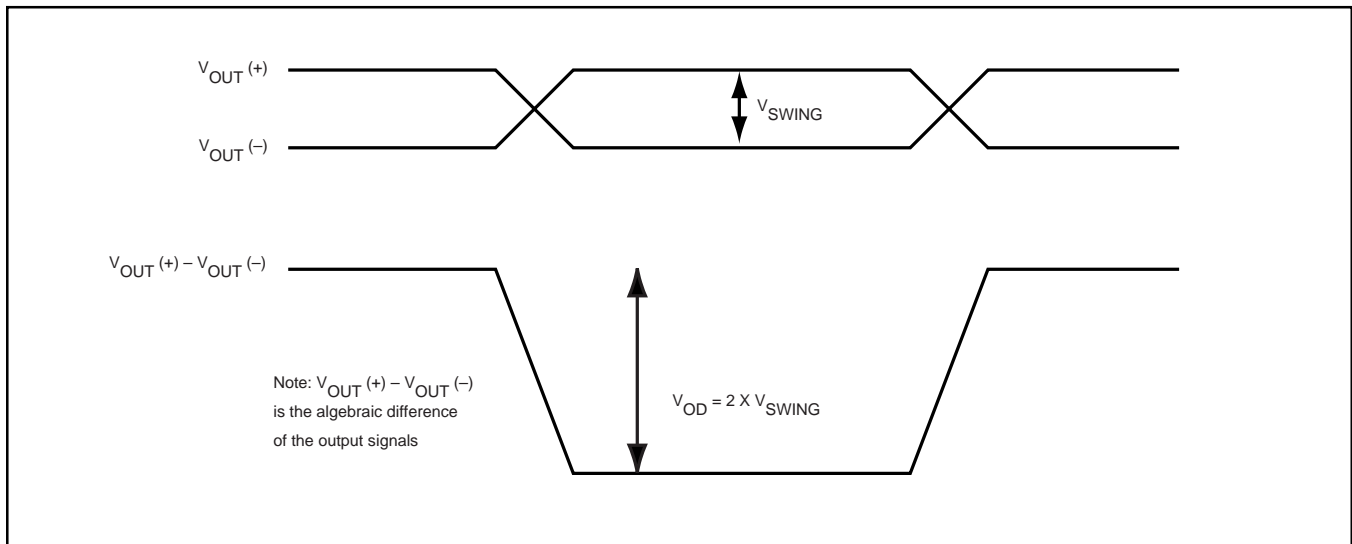


Table 10. PECL DC Characteristics²

Symbol	Min	Typ	Max	Units
V_{OH}^1	$V_{CC}-1095$		$V_{CC}-695$	mV
V_{OL}^1	$V_{CC}-1900$		$V_{CC}-1365$	mV
I_{OH}		20		mA
I_{OL}		5		mA

1. All outputs are loaded with 50Ω to $V_{CC} - 2V$.
2. DC is considered to be an output signal between 0Hz and 1KHz.

Table 11. Differential PECL Characteristics

Symbol	Min	Typ	Max	Units
V_{OD}^1	700		2330	mV

1. Differential input voltage – algebraic difference.

EXPANDING TO A 64 X 64 SWITCH

The S2025 includes configurable differential output pair driver enables that allow it to be expanded to form a 64 x 64 differential crosspoint switch.

As shown in Figure 9, four S2025 devices can be used to form a 64 x 64 differential crosspoint switch. Each of the 64 pairs of differential outputs are connected to output pairs on two different S2025 devices.

Similarly, each of the 64 pairs of differential outputs are connected to output pairs on two different S2025 devices. The configuration register files of the two devices are then programmed to enable only one of the two connected output pairs at once.

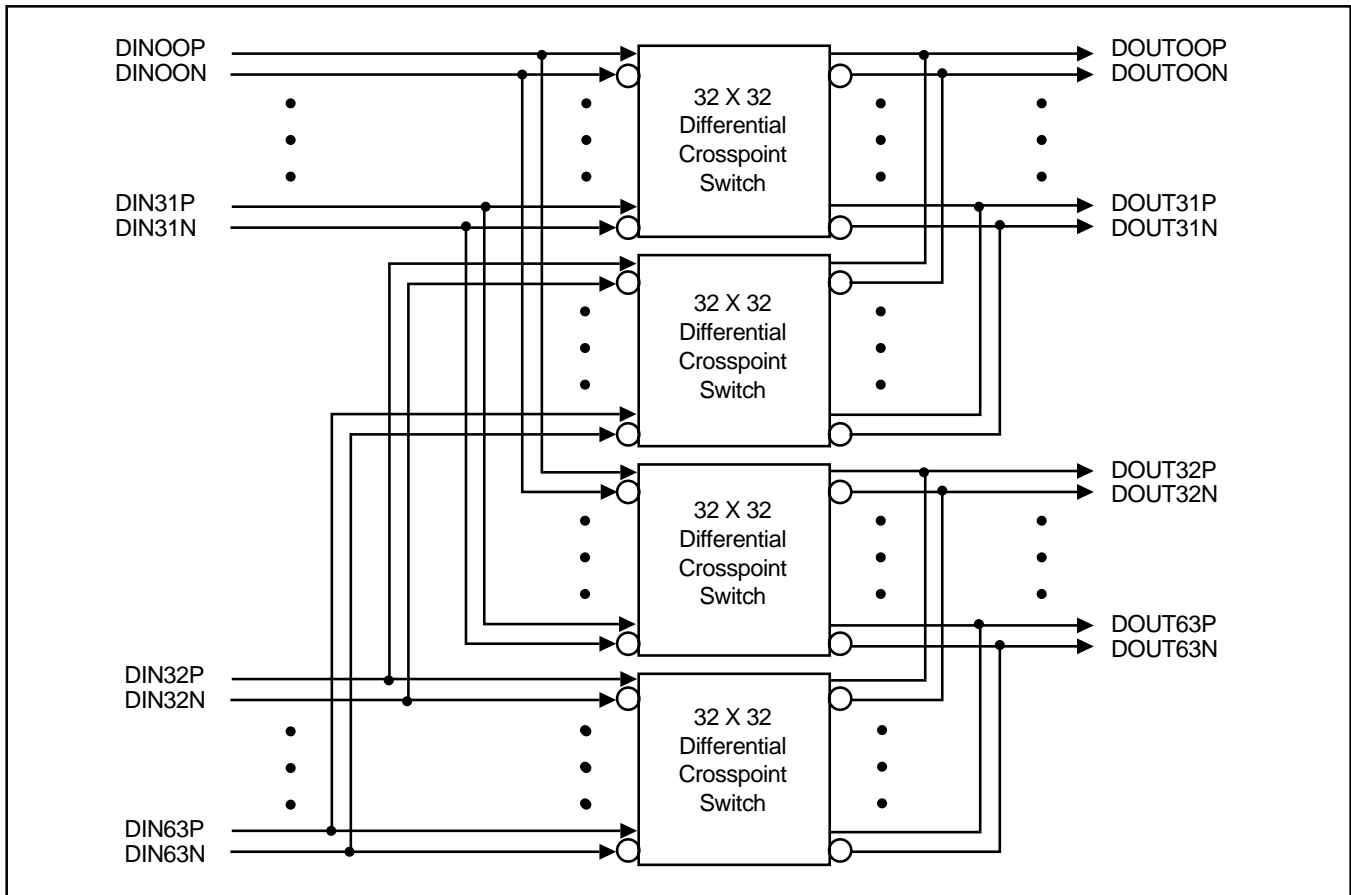
With the interconnection scheme shown in Figure 9, any of the 64 output pairs can be connected to any of the 64 input pairs.

To avoid power-up output pair contention, the Reset condition for the S2025 assumes a configuration where all the differential output pairs are disabled.

Normal high-speed PECL routing and termination practices are required for all PECL connections. For maximum data throughput, reflected signals from impedance mismatches at the package/pcb boundary, as well as those due to poor placement of terminating impedances must be minimized. Care also must be taken during board layout to position the devices for the shortest possible trace lengths when connecting differential outputs together.

Larger differential crosspoint switch structures can also be built using the S2025's ability to selectively enable and disable its differential output pair drivers.

Figure 9. Expanding to a 64 x 64 Switch



Ordering Information

Prefix	Device	Package
S – Integrated Circuit	2025	C – 8, 800MBPS, 196 LDCC lead formed with Heatsink unattached C – 15, 1.5GBPS, 196 LDCC lead formed with Heatsink unattached

X
Prefix

XXXX
Device

X
Package



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