



16 Mbit (2 M x 8-Bit/1 M x 16-Bit), 3 V Boot Sector Flash

This product has been retired and is not recommended for designs. For new and current designs, S29AL016J supercedes S29AL016D. This is the factory-recommended migration path. Please refer to the S29AL016J data sheet for specifications and ordering information.

Distinctive Characteristics

Architectural Advantages

- Single Power Supply Operation
 - Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
- Manufactured on 200 nm Process Technology
 - Fully compatible with 200 nm Am29LV160D and MBM29LV160E devices
- Flexible Sector Architecture
 - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
 - One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
- Sector Protection Features
 - A hardware method of locking a sector to prevent any program or erase operations within that sector
 - Sectors can be locked in-system or via programming equipment
 - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- Unlock Bypass Program Command
 - Reduces overall programming time when issuing multiple program command sequences
- Top or Bottom Boot Block Configurations Available
- Compatibility with JEDEC standards
 - Pinout and software compatible with single-power supply Flash
 - Superior inadvertent write protection

Performance Characteristics

- High Performance
 - Access times as fast as 70 ns
 - Extended temperature range (-40°C to +125°C)
- Ultra Low Power Consumption (typical values at 5 MHz)

- 200 nA Automatic Sleep mode current
- 200 nA standby mode current
- 9 mA read current
- 20 mA program/erase current
- Cycling Endurance: 1,000,000 cycles per sector typical
- Data Retention: 20 years typical

Package Options

- 48-ball FBGA
- 48-pin TSOP
- 44-pin SOP

Software Features

- CFI (Common Flash Interface) Compliant
 - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- Erase Suspend/Erase Resume
 - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- Data# Polling and Toggle Bits
 - Provides a software method of detecting program or erase operation completion

Hardware Features

- Ready/Busy# Pin (RY/BY#)
 - Provides a hardware method of detecting program or erase cycle completion
- Hardware Reset Pin (RESET#)
 - Hardware method to reset the device to reading array data

General Description

The S29AL016D is a 16 Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in 48-ball FBGA, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. A 12.0 V V_{PP} or 5.0 V_{CC} are not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 70 ns and 90 ns allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The S29AL016D is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

Spansion's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

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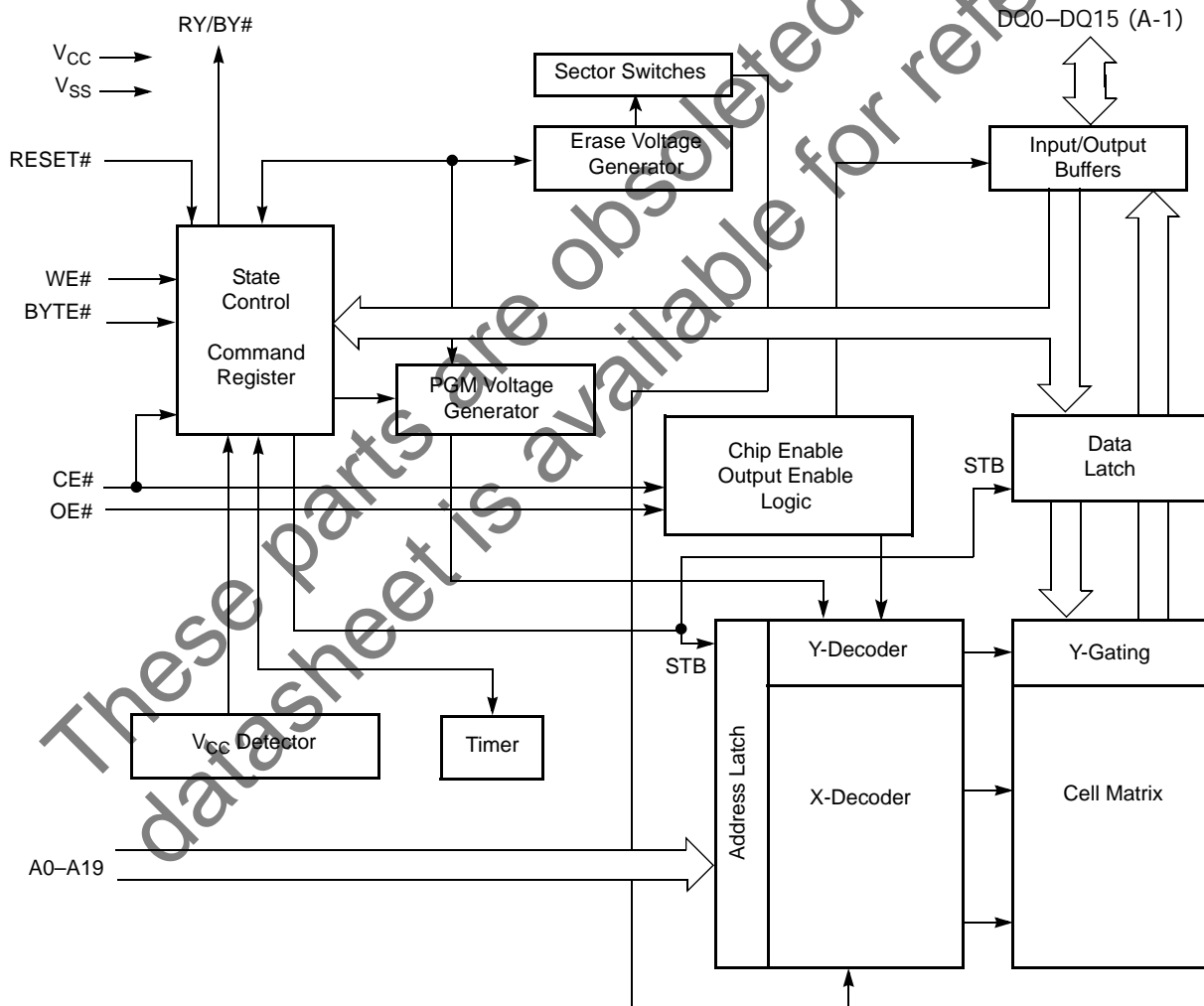
1. Product Selector Guide

| Family Part Number | | S29AL016D | |
|--------------------------------------|--|-----------|----|
| Speed Option | Voltage Range: $V_{CC} = 2.7\text{--}3.6\text{ V}$ | 70 | 90 |
| Max access time, ns (t_{ACC}) | | 70 | 90 |
| Max CE# access time, ns (t_{CE}) | | 70 | 90 |
| Max OE# access time, ns (t_{OE}) | | 30 | 35 |

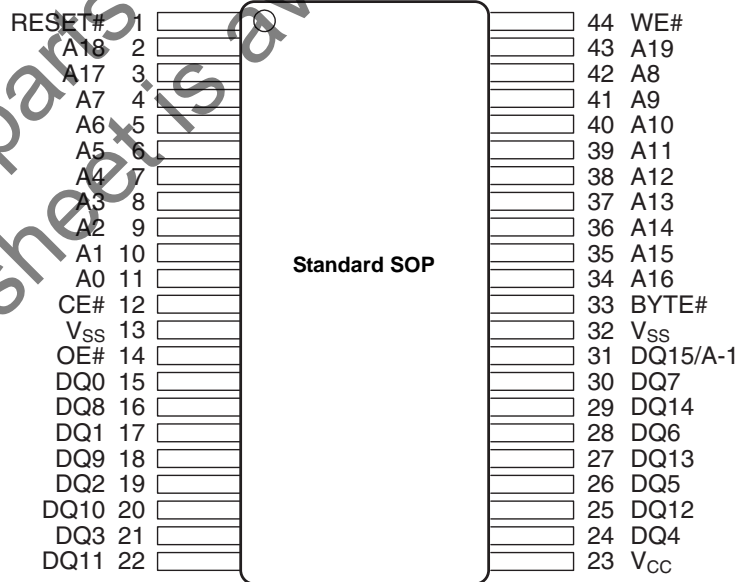
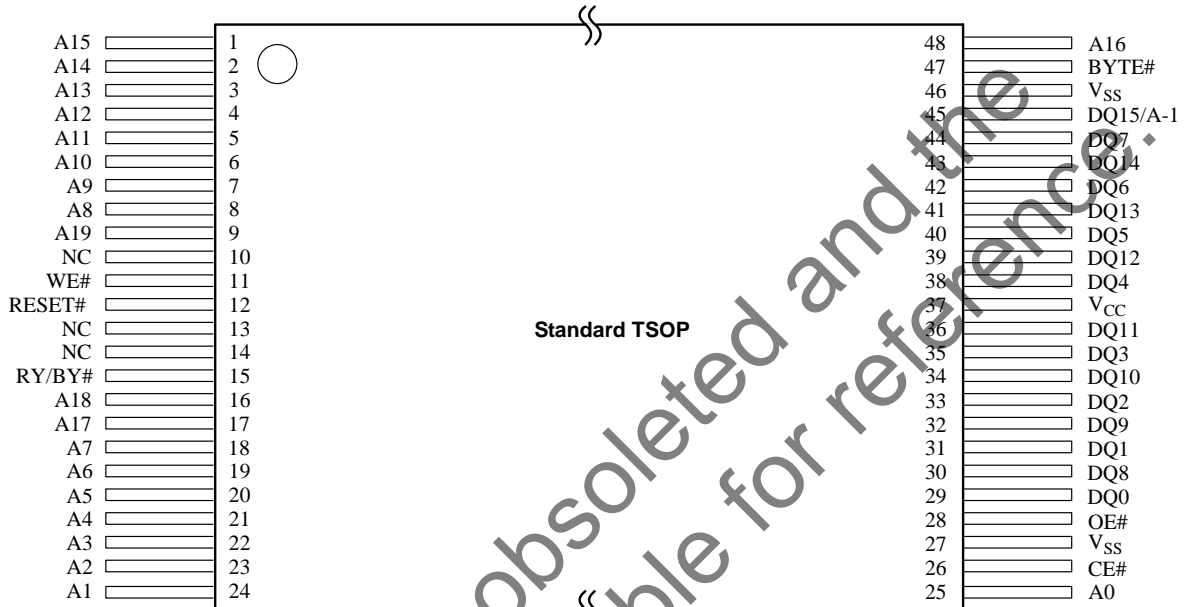
Note

See [AC Characteristics](#) on page 37 for full specifications.

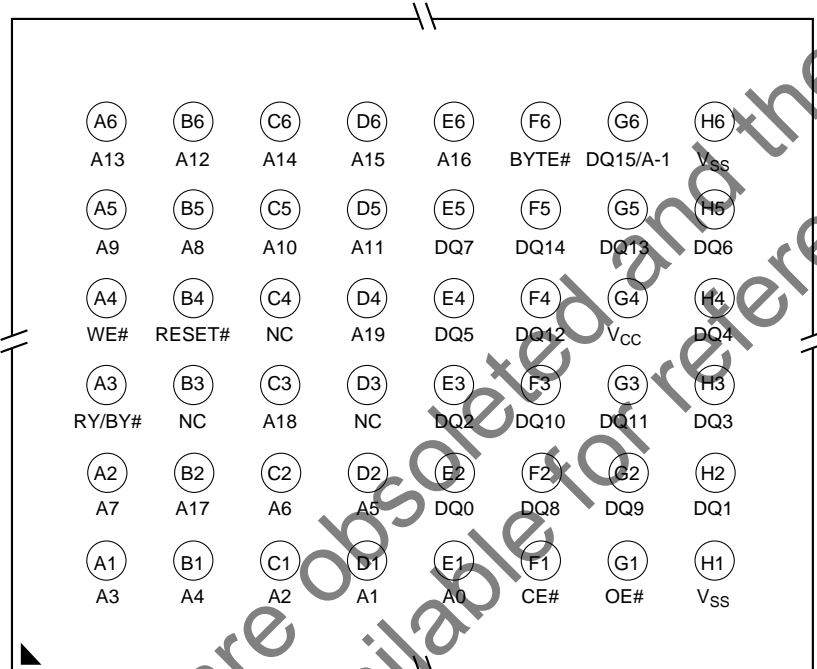
2. Block Diagram



3. Connection Diagrams



FBGA
Top View, Balls Facing Down



3.1 Special Handling Instructions

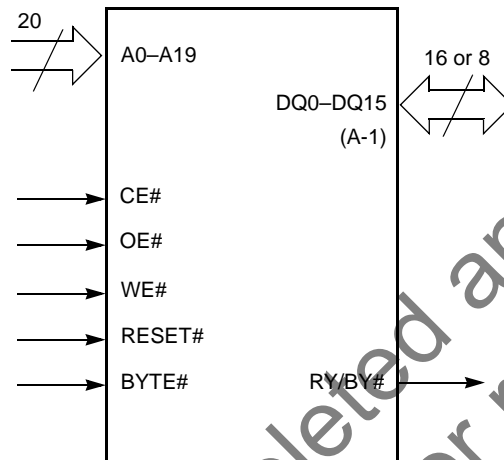
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4. Pin Configuration

| | |
|-----------------|--|
| A0–A19 | 20 addresses |
| DQ0–DQ14 | 15 data inputs/outputs |
| DQ15/A-1 | DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode) |
| BYTE# | Selects 8-bit or 16-bit mode |
| CE# | Chip enable |
| OE# | Output enable |
| WE# | Write enable |
| RESET# | Hardware reset pin |
| RY/BY# | Ready/Busy output |
| V _{CC} | 3.0 volt-only single power supply (see Product Selector Guide on page 4 for speed options and voltage supply tolerances) |
| V _{SS} | Device ground |
| NC | Pin not connected internally |

5. Logic Symbol

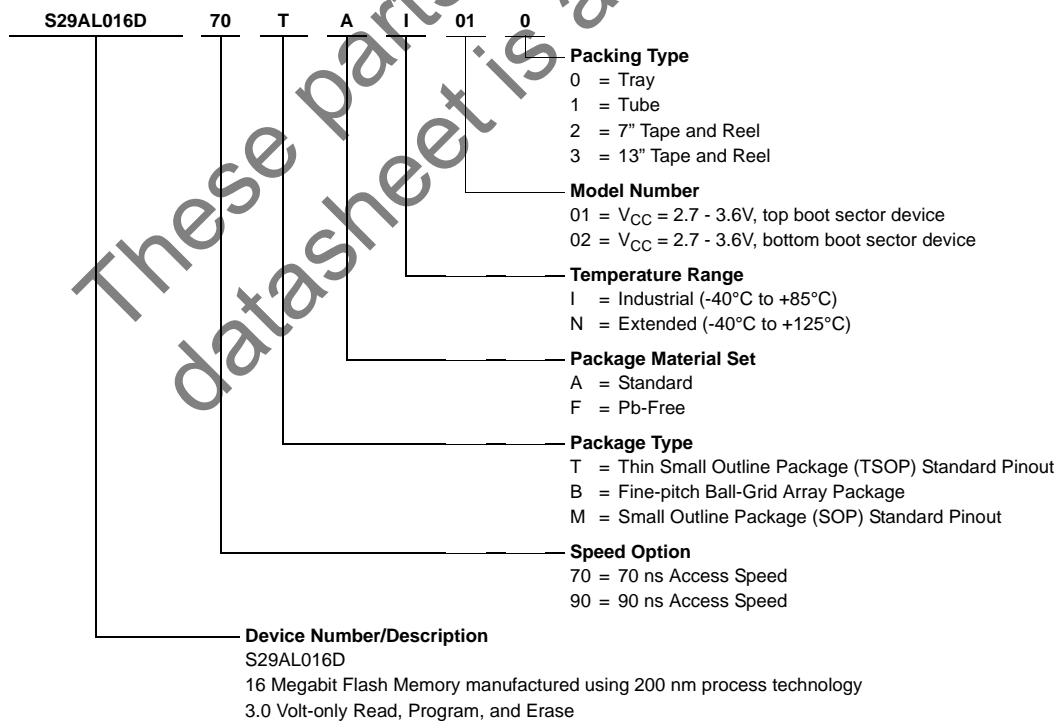


6. Ordering Information

This product has been retired and is not recommended for designs. For new and current designs, S29AL016J supercedes S29AL016D. This is the factory-recommended migration path. Please refer to the S29AL016J data sheet for specifications and ordering information.

6.1 S29AL016D Standard Products

Spanion standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



| S29AL016D Valid Combinations | | | | | | |
|------------------------------|--------------|---|--------------|---------------------|---------------------|----------------|
| Device Number | Speed Option | Package Type, Material, and Temperature Range | Model Number | Packing Type | Package Description | |
| S29AL016D | 70, 90 | TAI, TFI, TAN, TFN | 01, 02 | 0, 3 (Note 1) | TS048 (Note 3) | TSOP |
| | | BAI, BFI, BAN, BFN | | 0, 2, 3 (Note 1) | VBK048 (Note 4) | Fine Pitch BGA |
| | | MAI, MFI, MAN, MFN | | 0, 1, 3 (Note 2) | SO044 (Note 3) | SOP |

Notes

1. Type 0 is standard. Specify other options as required.
2. Type 1 is standard. Specify other options as required.
3. TSOP and SOP package markings omit packing type designator from ordering part number.
4. BGA package marking omits leading S29 and packing type designator from ordering part number.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

7. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

These parts are obsoleted and the datasheet is available for reference.

S29AL016D Device Bus Operations

| Operation | CE# | OE# | WE# | RESET# | Addresses (Note 1) | DQ0– DQ7 | DQ8–DQ15 | |
|----------------------------|----------------------------|-----|-----|----------------------------|--|------------------|----------------------------|----------------------------------|
| | | | | | | | BYTE# = V _{IH} | BYTE# = V _{IL} |
| Read | L | L | H | H | A _{IN} | D _{OUT} | D _{OUT} | DQ8–DQ14 = High-Z, DQ15 = A-1 |
| Write | L | H | L | H | A _{IN} | D _{IN} | D _{IN} | |
| Standby | V _{CC} ± 0.3 V | X | X | V _{CC} ± 0.3 V | X | High-Z | High-Z | High-Z |
| Output Disable | L | H | H | H | X | High-Z | High-Z | High-Z |
| Reset | X | X | X | L | X | High-Z | High-Z | High-Z |
| Sector Protect (Note 2) | L | H | L | V _{ID} | Sector Address, A6 = L, A1 = H, A0 = L | D _{IN} | X | X |
| Sector Unprotect (Note 2) | L | H | L | V _{ID} | Sector Address, A6 = H, A1 = H, A0 = L | D _{IN} | X | X |
| Temporary Sector Unprotect | X | X | X | V _{ID} | A _{IN} | D _{IN} | D _{IN} | High-Z |

Legend

L = Logic Low = V_{IL}
H = Logic High = V_{IH}
V_{ID} = 12.0 ± 0.5 V
X = Don't Care
A_{IN} = Address In
D_{IN} = Data In
D_{OUT} = Data Out

Notes

- Addresses are A19:A0 in word mode (BYTE# = V_{IH}), A19:A-1 in byte mode (BYTE# = V_{IL}).
- The sector protect and sector unprotect functions may also be implemented via programming equipment. See [Sector Protection/Unprotection on page 14](#).

7.1 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic 1, the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic 0, the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

7.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered. See [Reading Array Data on page 22](#) for more information. Refer to the AC [Read Operations on page 37](#) for timing specifications and to [Figure 17.1 on page 37](#) for the timing diagram. I_{CC1} in [DC Characteristics on page 33](#) represents the active current specification for reading array data.

7.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. See [Word/Byte Configuration on page 9](#) for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. [Word/Byte Program Command Sequence on page 23](#) has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. [Table on page 11](#) and [Table on page 13](#) indicate the address space that each sector occupies. A “sector address” consists of the address bits required to uniquely select a sector. The [Command Definitions on page 22](#) has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to [Autoselect Mode on page 14](#) and [Autoselect Command Sequence on page 23](#) for more information.

I_{CC2} in [DC Characteristics on page 33](#) represents the active current specification for the write mode. [AC Characteristics on page 37](#) contains timing specification tables and timing diagrams for write operations.

7.4 Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to [Write Operation Status on page 28](#) for more information, and to [AC Characteristics on page 37](#) for timing diagrams.

7.5 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH} .) If CE# and RESET# are held at V_{IH} , but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} and I_{CC4} represents the standby current specification shown in the table in [DC Characteristics on page 33](#).

7.6 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{ACC} + 30$ ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the [DC Characteristics on page 33](#) represents the automatic sleep mode current specification.

7.7 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin to V_{IL} for at least a period of t_{RP} , the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory. If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a 0 (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded

Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is 1), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH} . Refer to the tables in [AC Characteristics on page 37](#) for RESET# parameters and to [Figure 17.2 on page 38](#) for the timing diagram.

7.8 Output Disable Mode

When the OE# input is at V_{IH} , output from the device is disabled. The output pins are placed in the high impedance state.

Sector Address Tables (Top Boot Device)

| Sector | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | Sector Size (Kbytes/ Kwords) | Address Range (in hexadecimal) | |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|------------------------------|--------------------------------|-----------------|
| | | | | | | | | | | Byte Mode (x8) | Word Mode (x16) |
| SA0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 000000–00FFFF | 00000–07FFF |
| SA1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 010000–01FFFF | 08000–0FFFF |
| SA2 | 0 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 020000–02FFFF | 10000–17FFF |
| SA3 | 0 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 030000–03FFFF | 18000–1FFFF |
| SA4 | 0 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 040000–04FFFF | 20000–27FFF |
| SA5 | 0 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 050000–05FFFF | 28000–2FFFF |
| SA6 | 0 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 060000–06FFFF | 30000–37FFF |
| SA7 | 0 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 070000–07FFFF | 38000–3FFFF |
| SA8 | 0 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 080000–08FFFF | 40000–47FFF |
| SA9 | 0 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 090000–09FFFF | 48000–4FFFF |
| SA10 | 0 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 0A0000–0AFFFF | 50000–57FFF |
| SA11 | 0 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 0B0000–0BFFFF | 58000–5FFFF |
| SA12 | 0 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 0C0000–0CFFFF | 60000–67FFF |
| SA13 | 0 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 0D0000–0DFFFF | 68000–6FFFF |
| SA14 | 0 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 0E0000–0EFFFF | 70000–77FFF |
| SA15 | 0 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 0F0000–0FFFFF | 78000–7FFFF |
| SA16 | 1 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 100000–10FFFF | 80000–87FFF |
| SA17 | 1 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 110000–11FFFF | 88000–8FFFF |
| SA18 | 1 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 120000–12FFFF | 90000–97FFF |
| SA19 | 1 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 130000–13FFFF | 98000–9FFFF |
| SA20 | 1 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 140000–14FFFF | A0000–A7FFF |
| SA21 | 1 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 150000–15FFFF | A8000–AFFFF |
| SA22 | 1 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 160000–16FFFF | B0000–B7FFF |
| SA23 | 1 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 170000–17FFFF | B8000–BFFFF |
| SA24 | 1 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 180000–18FFFF | C0000–C7FFF |
| SA25 | 1 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 190000–19FFFF | C8000–CFFFF |
| SA26 | 1 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 1A0000–1AFFFF | D0000–D7FFF |
| SA27 | 1 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 1B0000–1BFFFF | D8000–DFFFF |
| SA28 | 1 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 1C0000–1CFFFF | E0000–E7FFF |
| SA29 | 1 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 1D0000–1DFFFF | E8000–EFFFF |
| SA30 | 1 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 1E0000–1EFFFF | F0000–F7FFF |
| SA31 | 1 | 1 | 1 | 1 | 1 | 0 | X | X | 32/16 | 1F0000–1F7FFF | F8000–FBFFF |
| SA32 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 8/4 | 1F8000–1F9FFF | FC000–FCFFF |
| SA33 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 8/4 | 1FA000–1FBFFF | FD000–FDFFF |
| SA34 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | 16/8 | 1FC000–1FFFFF | FE000–FFFFF |

Note

Address range is A19:A-1 in byte mode and A19:A0 in word mode. See [Word/Byte Configuration on page 9](#).

Sector Address Tables (Bottom Boot Device)

| Sector | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | Sector Size (Kbytes/ Kwords) | Address Range (in hexadecimal) | |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|------------------------------------|--------------------------------|-----------------|
| | | | | | | | | | | Byte Mode (x8) | Word Mode (x16) |
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 16/8 | 000000–003FFF | 00000–01FFF |
| SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 004000–005FFF | 02000–02FFF |
| SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 006000–007FFF | 03000–03FFF |
| SA3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | 008000–00FFFF | 04000–07FFF |
| SA4 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | 010000–01FFFF | 08000–0FFFF |
| SA5 | 0 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 020000–02FFFF | 10000–17FFF |
| SA6 | 0 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 030000–03FFFF | 18000–1FFFF |
| SA7 | 0 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 040000–04FFFF | 20000–27FFF |
| SA8 | 0 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 050000–05FFFF | 28000–2FFFF |
| SA9 | 0 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 060000–06FFFF | 30000–37FFF |
| SA10 | 0 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 070000–07FFFF | 38000–3FFFF |
| SA11 | 0 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 080000–08FFFF | 40000–47FFF |
| SA12 | 0 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 090000–09FFFF | 48000–4FFFF |
| SA13 | 0 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 0A0000–0AFFFF | 50000–57FFF |
| SA14 | 0 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 0B0000–0BFFFF | 58000–5FFFF |
| SA15 | 0 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 0C0000–0CFFFF | 60000–67FFF |
| SA16 | 0 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 0D0000–0DFFFF | 68000–6FFFF |
| SA17 | 0 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 0E0000–0EFFFF | 70000–77FFF |
| SA18 | 0 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 0F0000–0FFFFF | 78000–7FFFF |
| SA19 | 1 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 100000–10FFFF | 80000–87FFF |
| SA20 | 1 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 110000–11FFFF | 88000–8FFFF |
| SA21 | 1 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 120000–12FFFF | 90000–97FFF |
| SA22 | 1 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 130000–13FFFF | 98000–9FFFF |
| SA23 | 1 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 140000–14FFFF | A0000–A7FFF |
| SA24 | 1 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 150000–15FFFF | A8000–AFFFF |
| SA25 | 1 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 160000–16FFFF | B0000–B7FFF |
| SA26 | 1 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 170000–17FFFF | B8000–BFFFF |
| SA27 | 1 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 180000–18FFFF | C0000–C7FFF |
| SA28 | 1 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 190000–19FFFF | C8000–CFFFF |
| SA29 | 1 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 1A0000–1AFFFF | D0000–D7FFF |
| SA30 | 1 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 1B0000–1BFFFF | D8000–DFFFF |
| SA31 | 1 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 1C0000–1CFFFF | E0000–E7FFF |
| SA32 | 1 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 1D0000–1DFFFF | E8000–EFFFF |
| SA33 | 1 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 1E0000–1EFFFF | F0000–F7FFF |
| SA34 | 1 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 1F0000–1FFFFF | F8000–FFFFF |

Sector Address Tables (Bottom Boot Device)

| Sector | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | Sector Size (Kbytes/ Kwords) | Address Range (in hexadecimal) | |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|------------------------------|--------------------------------|-----------------|
| | | | | | | | | | | Byte Mode (x8) | Word Mode (x16) |
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 16/8 | 000000–003FFF | 00000–01FFF |
| SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 8/4 | 004000–005FFF | 02000–02FFF |
| SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 8/4 | 006000–007FFF | 03000–03FFF |
| SA3 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | 32/16 | 008000–00FFFF | 04000–07FFF |
| SA4 | 0 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 010000–01FFFF | 08000–0FFFF |
| SA5 | 0 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 020000–02FFFF | 10000–17FFF |
| SA6 | 0 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 030000–03FFFF | 18000–1FFFF |
| SA7 | 0 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 040000–04FFFF | 20000–27FFF |
| SA8 | 0 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 050000–05FFFF | 28000–2FFFF |
| SA9 | 0 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 060000–06FFFF | 30000–37FFF |
| SA10 | 0 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 070000–07FFFF | 38000–3FFFF |
| SA11 | 0 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 080000–08FFFF | 40000–47FFF |
| SA12 | 0 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 090000–09FFFF | 48000–4FFFF |
| SA13 | 0 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 0A0000–0AFFFF | 50000–57FFF |
| SA14 | 0 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 0B0000–0BFFFF | 58000–5FFFF |
| SA15 | 0 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 0C0000–0CFFFF | 60000–67FFF |
| SA16 | 0 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 0D0000–0DFFFF | 68000–6FFFF |
| SA17 | 0 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 0E0000–0EFFFF | 70000–77FFF |
| SA18 | 0 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 0F0000–0FFFFF | 78000–7FFFF |
| SA19 | 1 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 100000–10FFFF | 80000–87FFF |
| SA20 | 1 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 110000–11FFFF | 88000–8FFFF |
| SA21 | 1 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 120000–12FFFF | 90000–97FFF |
| SA22 | 1 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 130000–13FFFF | 98000–9FFFF |
| SA23 | 1 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 140000–14FFFF | A0000–A7FFF |
| SA24 | 1 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 150000–15FFFF | A8000–AFFFF |
| SA25 | 1 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 160000–16FFFF | B0000–B7FFF |
| SA26 | 1 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 170000–17FFFF | B8000–BFFFF |
| SA27 | 1 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 180000–18FFFF | C0000–C7FFF |
| SA28 | 1 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 190000–19FFFF | C8000–CFFFF |
| SA29 | 1 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 1A0000–1AFFFF | D0000–D7FFF |
| SA30 | 1 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 1B0000–1BFFFF | D8000–DFFFF |
| SA31 | 1 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 1C0000–1CFFFF | E0000–E7FFF |
| SA32 | 1 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 1D0000–1DFFFF | E8000–EFFFF |
| SA33 | 1 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 1E0000–1EFFFF | F0000–F7FFF |
| SA34 | 1 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 1F0000–1FFFFF | F8000–FFFFF |

Note

Address range is A19:A-1 in byte mode and A19:A0 in word mode. See the [Word/Byte Configuration](#) on page 9.

7.9 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table . In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table on page 11 and Table on page 13). Table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table on page 27. This method does not require V_{ID} . See *Command Definitions* on page 22 for details on using the autoselect mode.

S29AL016D Autoselect Codes (High Voltage Method)

| Description | Mode | CE# | OE# | WE# | A19 to A12 | A11 to A10 | A9 | A8 to A7 | A6 | A5 to A4 | A3 to A2 | A1 | A0 | DQ8 to DQ15 | DQ7 to DQ0 |
|--|------|-----|-----|-----|------------|------------|----------|----------|----|----------|----------|----|----|-------------|-------------------|
| Manufacturer ID: Spansion | | L | L | H | X | X | V_{ID} | X | L | X | L | L | L | X | 01h |
| Device ID: S29AL016D (Top Boot Block) | Word | L | L | H | | | | X | L | X | L | L | H | 22h | C4h |
| | Byte | L | L | H | X | X | V_{ID} | X | L | X | L | L | H | X | C4h |
| Device ID: S29AL016D (Bottom Boot Block) | Word | L | L | H | | | | X | L | X | L | L | H | 22h | 49h |
| | Byte | L | L | H | X | X | V_{ID} | X | L | X | L | L | H | X | 49h |
| Sector Protection Verification | | L | L | H | SA | X | V_{ID} | X | L | X | L | H | L | X | 01h (protected) |
| | | | | | | | | | | | | | | X | 00h (unprotected) |

Legend

L = Logic Low = V_{IL}
H = Logic High = V_{IH}
SA = Sector Address
X = Don't care

Note

The autoselect codes may also be accessed in-system via command sequences. See Table on page 27.

7.10 Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected. Spansion offers the option of programming and protecting sectors at its factory prior to shipping the device through Spansion's ExpressFlash™ Service. Contact a Spansion representative for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode* on page 14 for details.

Sector protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure on page 16 shows the algorithms and Figure 17.12 on page 44 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

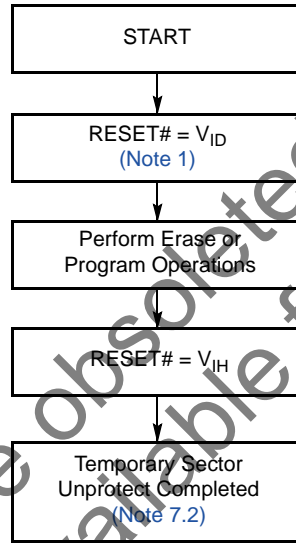
The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only Spansion flash devices. Details on this method are provided in a supplement, publication number 21468. Contact a Spansion representative to request a copy.

7.11 Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID} . During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again.

Figure 7.1 shows the algorithm, and Figure 17.11 on page 43 shows the timing diagrams, for this feature.

Figure 7.1 Temporary Sector Unprotect Operation



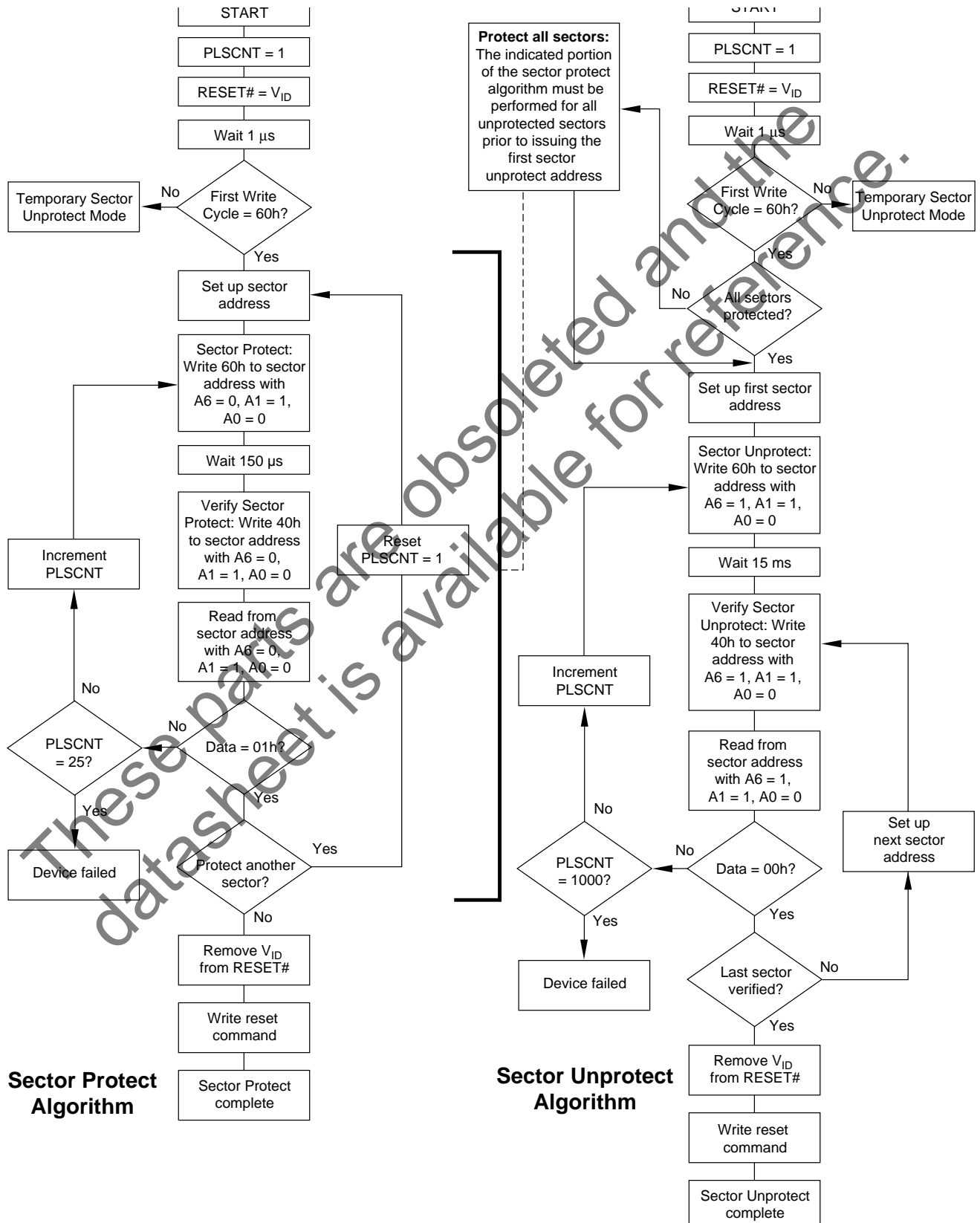
Notes

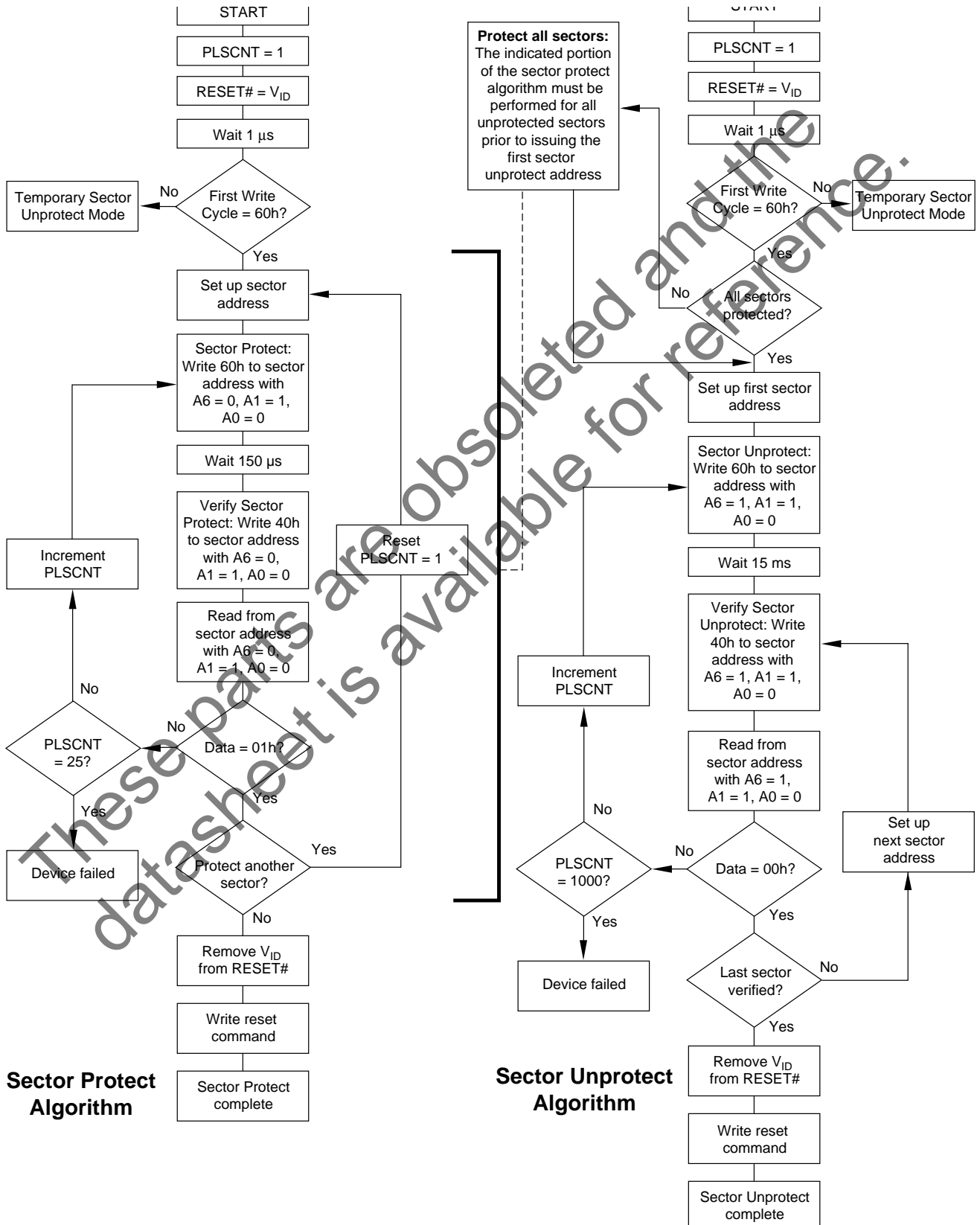
1. All protected sectors unprotected.
2. All previously protected sectors are protected once again.

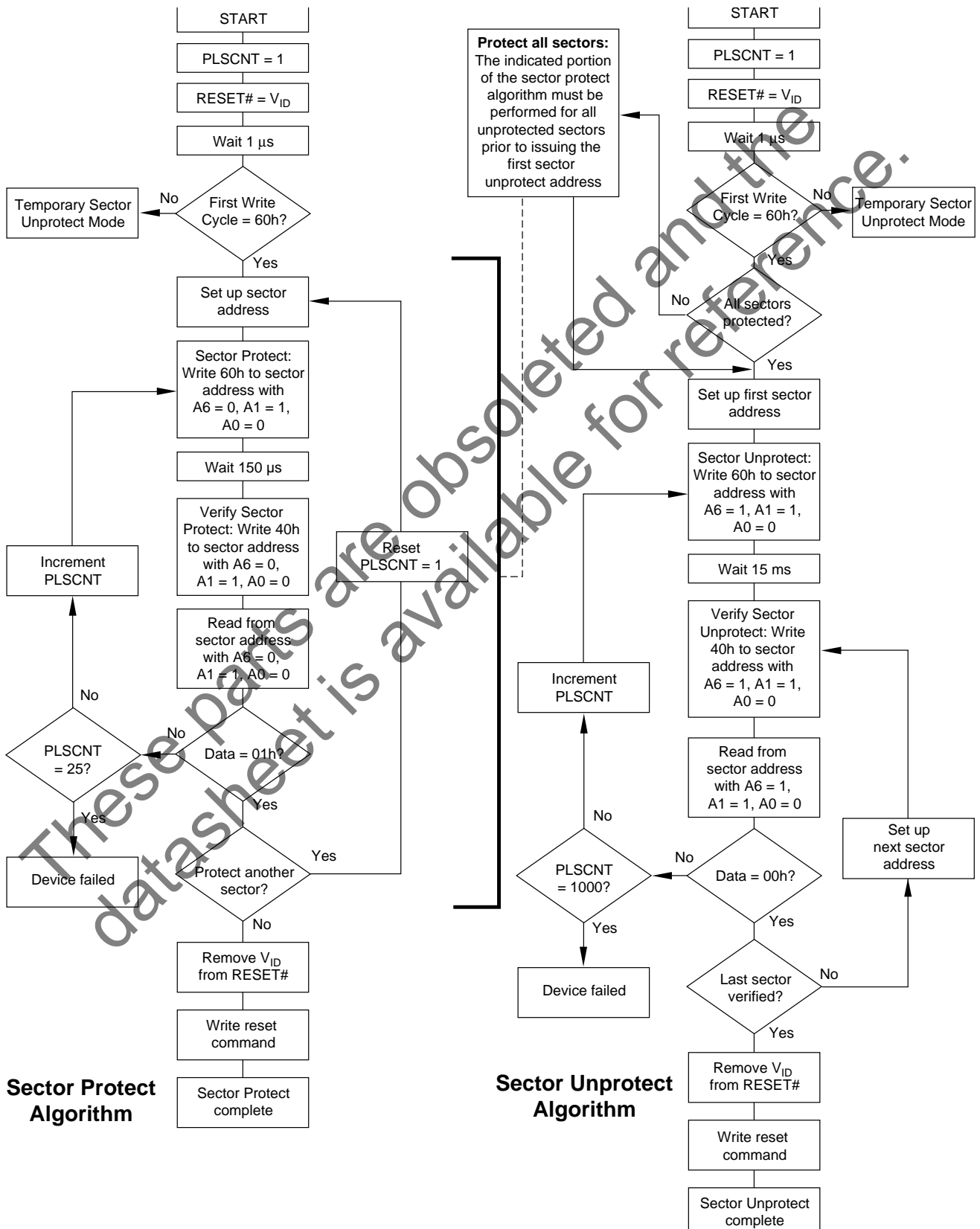
Figure 7.2 In-System Sector Protect/Unprotect Algorithms

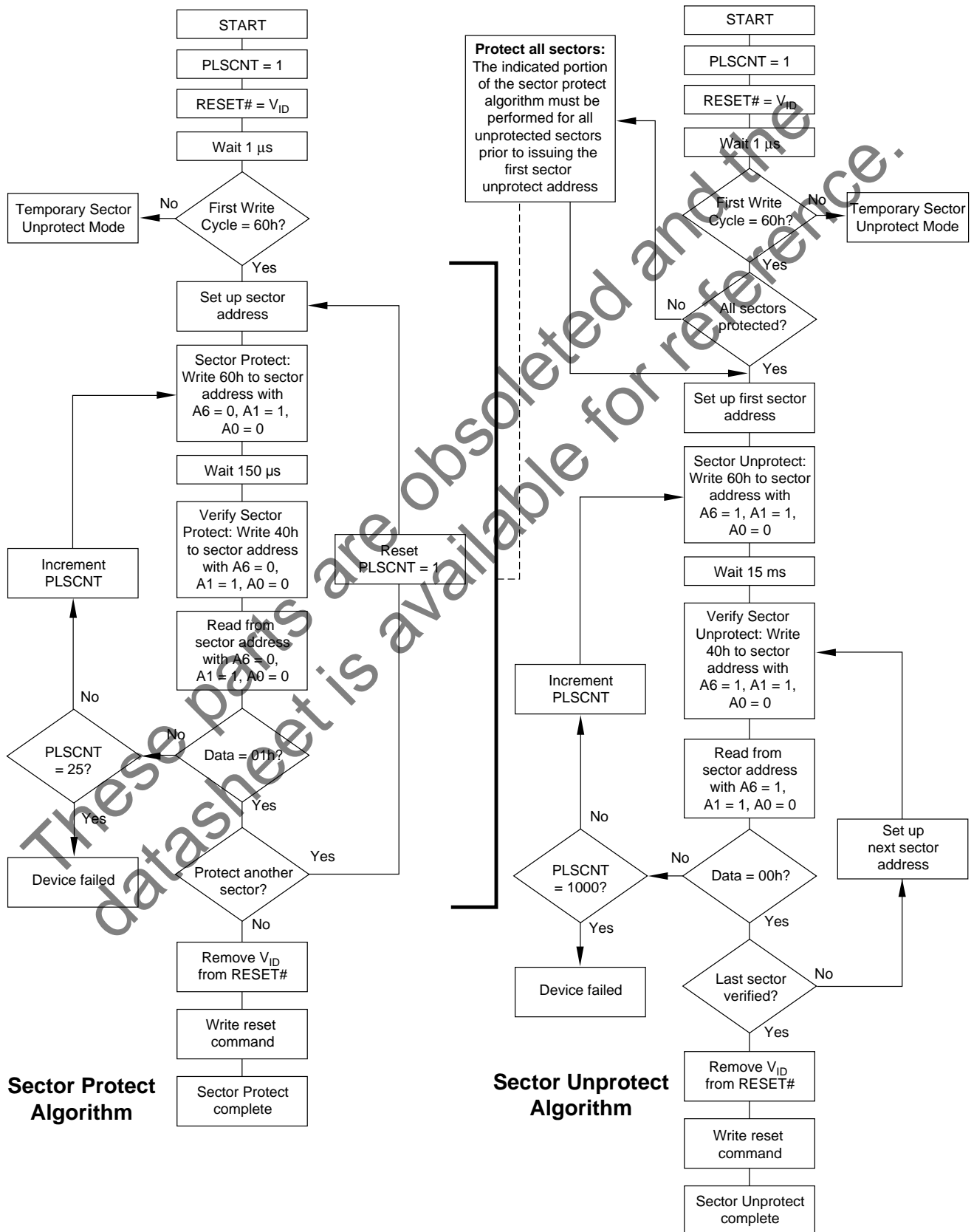
3.

These parts are obsolete and the datasheet is available for reference.









8. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table to Table on page 21. In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table to Table on page 21. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at <http://www.amd.com/products/nvd/overview/cfi.html>. Alternatively, contact a Spansion representative for copies of these documents.

CFI Query Identification String

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|-----------------------|-----------------------|-------------------------|--|
| 10h 11h 12h | 20h 22h 24h | 0051h 0052h 0059h | Query Unique ASCII string "QRY" |
| 13h 14h | 26h 28h | 0002h 0000h | Primary OEM Command Set |
| 15h 16h | 2Ah 2Ch | 0040h 0000h | Address for Primary Extended Table |
| 17h 18h | 2Eh 30h | 0000h 0000h | Alternate OEM Command Set (00h = none exists) |
| 19h 1Ah | 32h 34h | 0000h 0000h | Address for Alternate OEM Extended Table (00h = none exists) |

System Interface String

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|-----------------------|-----------------------|-------|---|
| 1Bh | 36h | 0027h | V _{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt |
| 1Ch | 38h | 0036h | V _{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt |
| 1Dh | 3Ah | 0000h | V _{PP} Min. voltage (00h = no V _{PP} pin present) |
| 1Eh | 3Ch | 0000h | V _{PP} Max. voltage (00h = no V _{PP} pin present) |
| 1Fh | 3Eh | 0004h | Typical timeout per single byte/word write 2 ^N μs |
| 20h | 40h | 0000h | Typical timeout for Min. size buffer write 2 ^N μs (00h = not supported) |
| 21h | 42h | 000Ah | Typical timeout per individual block erase 2 ^N ms |
| 22h | 44h | 0000h | Typical timeout for full chip erase 2 ^N ms (00h = not supported) |
| 23h | 46h | 0005h | Max. timeout for byte/word write 2 ^N times typical |
| 24h | 48h | 0000h | Max. timeout for buffer write 2 ^N times typical |
| 25h | 4Ah | 0004h | Max. timeout per individual block erase 2 ^N times typical |
| 26h | 4Ch | 0000h | Max. timeout for full chip erase 2 ^N times typical (00h = not supported) |

Device Geometry Definition

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|--------------------------|--------------------------|----------------------------------|---|
| 27h | 4Eh | 0015h | Device Size = 2 ^N byte |
| 28h 29h | 50h 52h | 0002h 0000h | Flash Device Interface description (refer to CFI publication 100) |
| 2Ah 2Bh | 54h 56h | 0000h 0000h | Max. number of byte in multi-byte write = 2 ^N (00h = not supported) |
| 2Ch | 58h | 0004h | Number of Erase Block Regions within device |
| 2Dh 2Eh 2Fh 30h | 5Ah 5Ch 5Eh 60h | 0000h 0000h 0040h 0000h | Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100) |
| 31h 32h 33h 34h | 62h 64h 66h 68h | 0001h 0000h 0020h 0000h | Erase Block Region 2 Information |
| 35h 36h 37h 38h | 6Ah 6Ch 6Eh 70h | 0000h 0000h 0080h 0000h | Erase Block Region 3 Information |
| 39h 3Ah 3Bh 3Ch | 72h 74h 76h 78h | 001Eh 0000h 0000h 0001h | Erase Block Region 4 Information |

Primary Vendor-Specific Extended Query

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|-----------------------|-----------------------|-------------------------|--|
| 40h 41h 42h | 80h 82h 84h | 0050h 0052h 0049h | Query-unique ASCII string "PRI" |
| 43h | 86h | 0031h | Major version number, ASCII |
| 44h | 88h | 0030h | Minor version number, ASCII |
| 45h | 8Ah | 0000h | Address Sensitive Unlock 0 = Required, 1 = Not Required |
| 46h | 8Ch | 0002h | Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write |
| 47h | 8Eh | 0001h | Sector Protect 0 = Not Supported, X = Number of sectors per group |
| 48h | 90h | 0001h | Sector Temporary Unprotect 00 = Not Supported, 01 = Supported |
| 49h | 92h | 0004h | Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29LV800A mode |
| 4Ah | 94h | 0000h | Simultaneous Operation 00 = Not Supported, 01 = Supported |
| 4Bh | 96h | 0000h | Burst Mode Type 00 = Not Supported, 01 = Supported |
| 4Ch | 98h | 0000h | Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page |

8.1 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to [Table on page 27](#) for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

8.1.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO} , the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO} . The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO} .

8.1.2 Write Pulse *Glitch* Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

8.1.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL} , CE# = V_{IH} or WE# = V_{IH} . To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

8.1.4 Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

9. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. [Table on page 27](#) defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in [AC Characteristics on page 37](#).

9.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See [Erase Suspend/Erase Resume Commands on page 25](#) for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See [Reset Command on page 22](#).

See also [Requirements for Reading Array Data on page 9](#) for more information. The [Read Operations on page 37](#) provides the read parameters, and [Figure 17.1 on page 37](#) shows the timing diagram.

9.2 Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

9.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. [Table on page 27](#) shows the address and data requirements. This method is an alternative to that shown in [Table on page 14](#), which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in word mode (or 04h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to [Table on page 11](#) and [Table on page 13](#) for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

9.4 Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. [Table on page 27](#) shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See [Write Operation Status on page 28](#) for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a 0 back to a 1.** Attempting to do so may halt the operation and set DQ5 to 1, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still 0. Only erase operations can convert a 0 to a 1.

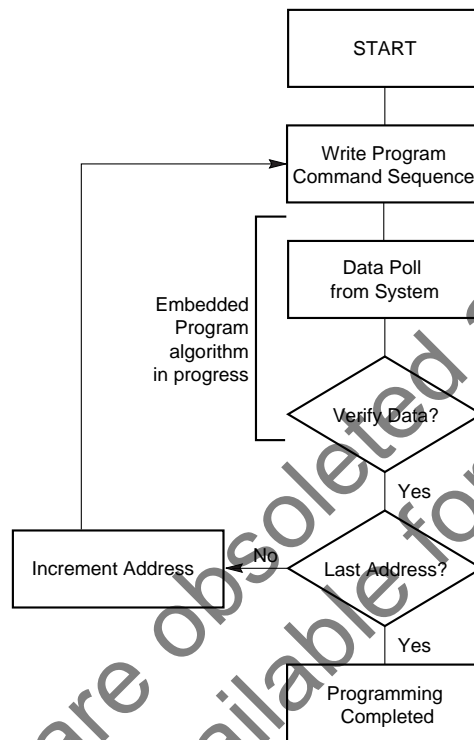
9.5 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. [Table on page 27](#) shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

[Figure 9.1 on page 24](#) illustrates the algorithm for the program operation. See [Erase/Program Operations on page 40](#) for parameters, and to [Figure 17.5 on page 40](#) for timing diagrams.

Figure 9.1 Program Operation



Note
See [Table on page 27](#) for program command sequence.

9.6 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. [Table on page 27](#) shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See [Write Operation Status on page 28](#) for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

[Figure 9.2 on page 26](#) illustrates the algorithm for the erase operation. See [Erase/Program Operations on page 40](#) for parameters, and [Figure 17.6 on page 41](#) for timing diagrams.

9.7 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. [Table on page 27](#) shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 μ s begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 μ s, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 μ s, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See [DQ3: Sector Erase Timer on page 31](#).) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to [Write Operation Status on page 28](#) for information on these status bits.)

[Figure 9.2 on page 26](#) illustrates the algorithm for the erase operation. Refer to [Erase/Program Operations on page 40](#) for parameters, and to [Figure 17.6 on page 41](#) for timing diagrams.

9.8 Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 μ s time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are *don't-cares* when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 μ s to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

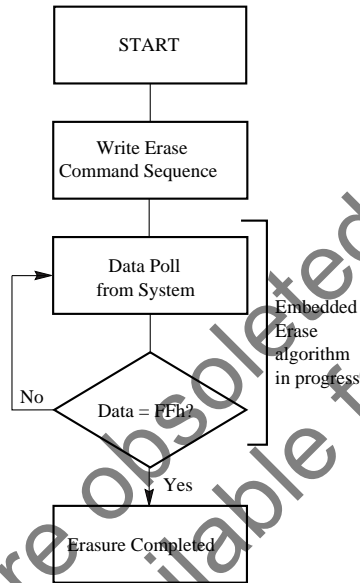
After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See [Write Operation Status on page 28](#) for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See [Write Operation Status on page 28](#) for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See [Autoselect Command Sequence on page 23](#) for more information.

The system must write the Erase Resume command (address bits are *don't care*) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Figure 9.2 Erase Operation



Notes

1. See Table on page 27 for erase command sequence.
2. See DQ3: Sector Erase Timer on page 31 for more information.

These parts are obsolete and the datasheet is available for reference.

10. Command Definitions

S29AL016D Command Definitions

| Command Sequence (Note 1) | | | Cycles | Bus Cycles (Notes 2–5) | | | | | | | | | | | | |
|---------------------------------|--------------------------------|------|--------|------------------------|------|--------|------|-------|------|-------------|----------|-------|------|-------|------|--|
| | | | | First | | Second | | Third | | Fourth | | Fifth | | Sixth | | |
| | | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | |
| Read (Note 6) | | | 1 | RA | RD | | | | | | | | | | | |
| Reset (Note 7) | | | 1 | XXX | F0 | | | | | | | | | | | |
| Autoselect (Note 8) | Manufacturer ID | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X00 | 01 | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | | |
| | Device ID, Top Boot Block | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X01 | 22C4 | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | X02 | C4 | | | | | |
| | Device ID, Bottom Boot Block | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X01 | 2249 | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | X02 | 49 | | | | | |
| | Sector Protect Verify (Note 9) | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | (SA) X02 | XX00 | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | (SA) X04 | 00 01 | | | | | |
| CFI Query (Note 10) | | Word | 1 | 55 | 98 | | | | | | | | | | | |
| | | Byte | | AA | | | | | | | | | | | | |
| Program | | Word | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | | |
| Unlock Bypass | | Word | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | | |
| Unlock Bypass Program (Note 11) | | | 2 | XXX | A0 | PA | PD | | | | | | | | | |
| Unlock Bypass Reset (Note 12) | | | 2 | XXX | 90 | XXX | 00 | | | | | | | | | |
| Chip Erase | | Word | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 | |
| | | Byte | | AAA | | 555 | | AAA | | AAA | | 555 | | AAA | | |
| Sector Erase | | Word | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 | |
| | | Byte | | AAA | | 555 | | AAA | | AAA | | 555 | | | | |
| Erase Suspend (Note 13) | | | 1 | XXX | B0 | | | | | | | | | | | |
| Erase Resume (Note 14) | | | 1 | XXX | 30 | | | | | | | | | | | |

Legend

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A19–A12 uniquely select any sector.

Notes

- See Table on page 9 for description of bus operations.
- All values are in hexadecimal.
- Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.
- Data bits DQ15–DQ8 are don't cares for unlock and command cycles.
- Address bits A19–A11 are don't cares for unlock and command cycles, unless SA or PA required.
- No unlock or command cycles required when reading array data.
- The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).
- The fourth cycle of the autoselect command sequence is a read cycle.
- The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.
- Command is valid when device is ready to read array data or when device is in autoselect mode.
- The Unlock Bypass command is required prior to the Unlock Bypass Program command.
- The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode. F0 is also acceptable.

13. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.

14. The Erase Resume command is valid only during the Erase Suspend mode.

11. Write Operation Status

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. [Table on page 32](#) and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

11.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 μ s, then the device returns to reading array data.

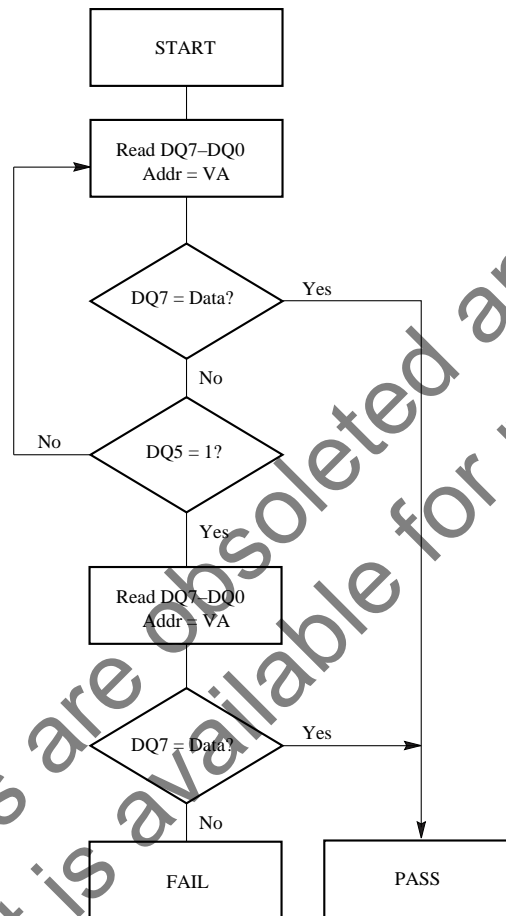
During the Embedded Erase algorithm, Data# Polling produces a 0 on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a 1 on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to 1; prior to this, the device outputs the *complement*, or 0. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 μ s, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. [Figure 17.8 on page 42](#), illustrates this.

[Table on page 32](#) shows the outputs for Data# Polling on DQ7. [Figure 11.2 on page 31](#) shows the Data# Polling algorithm.

Figure 11.1 Data# Polling Algorithm



Notes

1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.

11.2 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table on page 32 shows the outputs for RY/BY#. Figures Figure 17.1 on page 37, Figure 17.2 on page 38, Figure 17.5 on page 40 and Figure 17.6 on page 41 shows RY/BY# for read, reset, program, and erase operations, respectively.

11.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 μ s, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see [DQ7: Data# Polling on page 28](#)).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 μ s after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

[Table on page 32](#) shows the outputs for Toggle Bit I on DQ6. [Figure 11.2 on page 31](#) shows the toggle bit algorithm in flowchart form, and [Reading Toggle Bits DQ6/DQ2 on page 30](#) explains the algorithm. [Figure 17.9 on page 42](#) shows the toggle bit timing diagrams. [Figure 17.10 on page 43](#) shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on [DQ2: Toggle Bit II on page 30](#).

11.4 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to [Table on page 32](#) to compare outputs for DQ2 and DQ6.

[Figure 11.2 on page 31](#) shows the toggle bit algorithm in flowchart form, and the section [Reading Toggle Bits DQ6/DQ2 on page 30](#) explains the algorithm. See also the [DQ6: Toggle Bit I on page 30](#) subsection. [Figure 17.9 on page 42](#) shows the toggle bit timing diagram. [Figure 17.10 on page 43](#) shows the differences between DQ2 and DQ6 in graphical form.

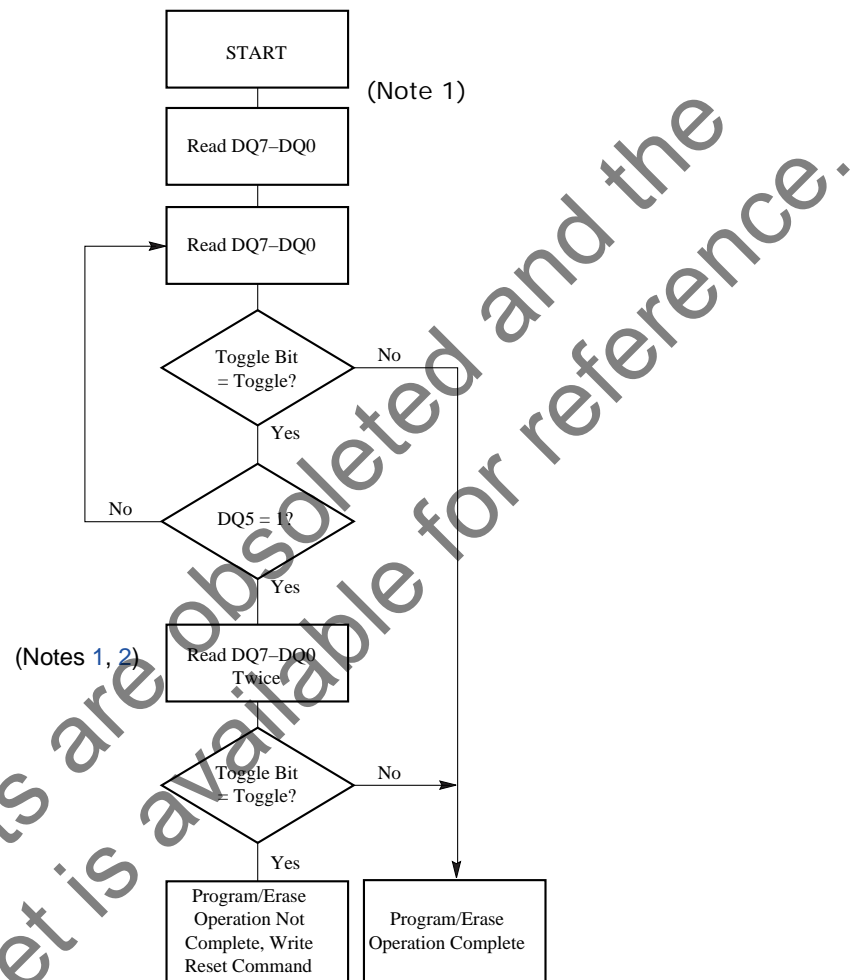
11.5 Reading Toggle Bits DQ6/DQ2

Refer to [Figure 11.2 on page 31](#) for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of [Figure 11.2 on page 31](#)).

Figure 11.2 Toggle Bit Algorithm



Notes

1. Read toggle bit twice to determine whether or not it is toggling. See text.
2. Recheck toggle bit because it may stop toggling as DQ5 changes to 1. See text.

11.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a 1. This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a 1 to a location that is previously programmed to 0. **Only an erase operation can change a 0 back to a 1.** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a 1.

Under both these conditions, the system must issue the reset command to return the device to reading array data.

11.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from 0 to 1. The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 μs. See also [Sector Erase Command Sequence on page 25](#).

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is 1, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is 0, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table shows the outputs for DQ3.

Write Operation Status

| Operation | | DQ7 (Note 2) | DQ6 | DQ5 (Note 1) | DQ3 | DQ2 (Note 2) | RY/BY# |
|--------------------|---|-----------------|-----------|-----------------|------|-----------------|--------|
| Standard Mode | Embedded Program Algorithm | DQ7# | Toggle | 0 | N/A | No toggle | 0 |
| | Embedded Erase Algorithm | 0 | Toggle | 0 | 1 | Toggle | 0 |
| Erase Suspend Mode | Reading within Erase Suspended Sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| | Reading within Non-Erase Suspended Sector | Data | Data | Data | Data | Data | 1 |
| | Erase-Suspend-Program | DQ7# | Toggle | 0 | N/A | N/A | 0 |

Notes

- DQ5 switches to 1 when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See [DQ5: Exceeded Timing Limits on page 31](#) for more information.
- DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

12. Absolute Maximum Ratings

| | |
|--|----------------------------------|
| Storage Temperature Plastic Packages | -65°C to +150°C |
| Ambient Temperature with Power Applied | -65°C to +125°C |
| Voltage with Respect to Ground | |
| V _{CC} (Note 1) | -0.5 V to +4.0 V |
| A9, OE#, and RESET# (Note 2) | -0.5 V to +12.5 V |
| All other pins (Note 1) | -0.5 V to V _{CC} +0.5 V |
| Output Short Circuit Current (Note 3) | 200 mA |

Notes

- Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. See [Figure 13.1 on page 33](#). Maximum DC voltage on input or I/O pins is V_{CC}+0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC}+2.0 V for periods up to 20 ns. See [Figure 13.2 on page 33](#).
- Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. See [Figure 13.1 on page 33](#). Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
- No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

13. Operating Ranges

Industrial (I) Devices

Ambient Temperature (T_A) -40°C to +85°C

Extended (N) Devices

Ambient Temperature (T_A) -40°C to +125°C

V_{CC} Supply Voltages

V_{CC} for standard voltage range 2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Figure 13.1 Maximum Negative Overshoot Waveform

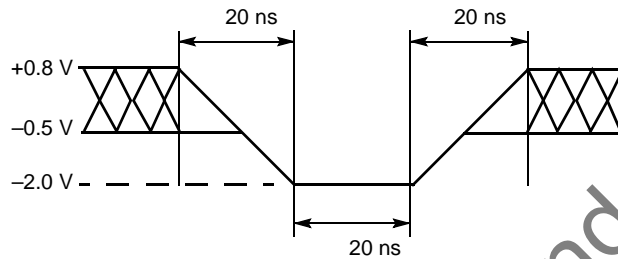
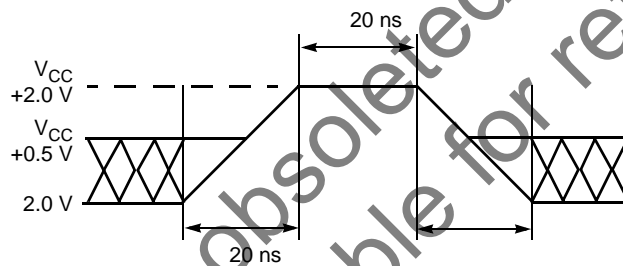


Figure 13.2 Maximum Positive Overshoot Waveform



14. DC Characteristics

14.1 CMOS Compatible

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|-----------|---|--|--------|-----|-----------|---------|
| I_{LI} | Input Load Current | $V_{IN} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC\ max}$ | | | ± 1.0 | μA |
| I_{LIT} | A9 Input Load Current | $V_{CC} = V_{CC\ max}$; A9 = 12.5 V | | | 35 | |
| I_{LO} | Output Leakage Current | $V_{OUT} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC\ max}$ | | | ± 1.0 | |
| I_{CC1} | V_{CC} Active Read Current (Notes 1, 2) | CE# = V_{IL} , OE# = V_{IH} , Byte Mode | 10 MHz | 15 | 30 | mA |
| | | | 5 MHz | 9 | 16 | |
| | | | 1 MHz | 2 | 4 | |
| | | CE# = V_{IL} , OE# = V_{IH} , Word Mode | 10 MHz | 18 | 35 | |
| | | | 5 MHz | 9 | 16 | |
| | | | 1 MHz | 2 | 4 | |
| I_{CC2} | V_{CC} Active Write Current (Notes 2, 3, 5) | CE# = V_{IL} , OE# = V_{IH} | | 20 | 35 | mA |
| I_{CC3} | V_{CC} Standby Current (Notes 2, 4) | CE#, RESET# = $V_{CC} \pm 0.3 V$ | 0.2 | 5 | | μA |
| I_{CC4} | V_{CC} Standby Current During Reset (Notes 2, 4) | RESET# = $V_{SS} \pm 0.3 V$ | 0.2 | | | μA |
| I_{CC5} | Automatic Sleep Mode (Notes 2, 4, 6) | $V_{IH} = V_{CC} \pm 0.3 V$; $V_{IL} = V_{SS} \pm 0.3 V$ | 0.2 | | | μA |

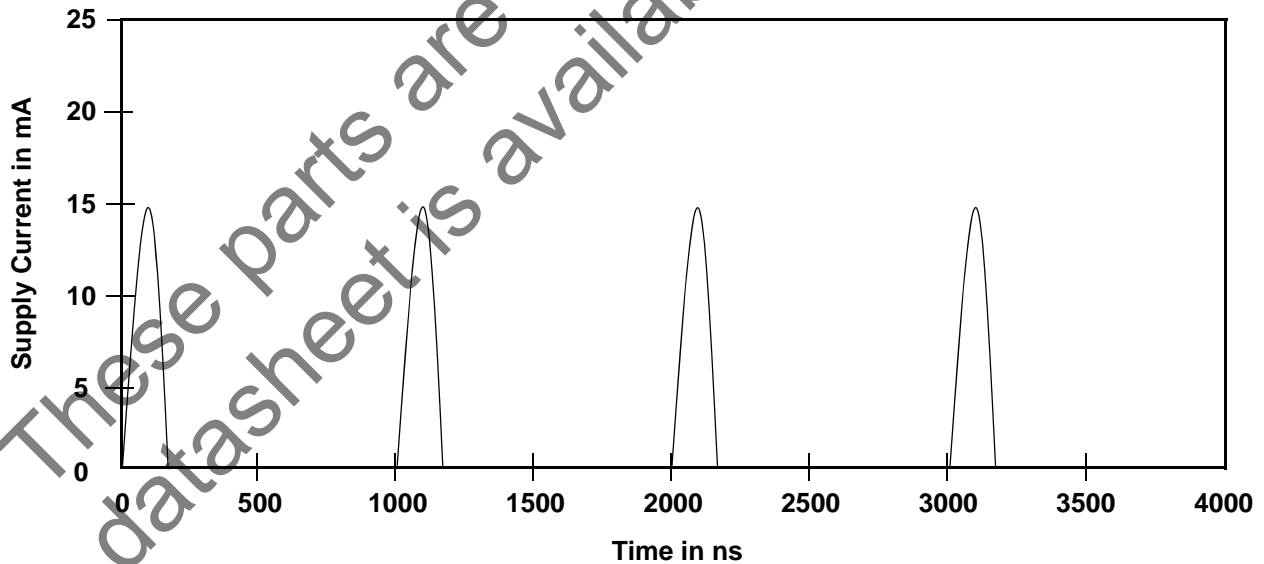
| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|------------------|---|--|-----------------------|-----|-----------------------|------|
| V _{IL} | Input Low Voltage | | -0.5 | | 0.8 | V |
| V _{IH} | Input High Voltage | | 0.7 x V _{CC} | | V _{CC} + 0.3 | |
| V _{ID} | Voltage for Autoselect and Temporary Sector Unprotect | V _{CC} = 3.3 V | 11.5 | | 12.5 | |
| V _{OL} | Output Low Voltage | I _{OL} = 4.0 mA, V _{CC} = V _{CC min} | | | 0.45 | |
| V _{OH1} | Output High Voltage | I _{OH} = -2.0 mA, V _{CC} = V _{CC min} | 2.4 | | | |
| V _{OH2} | | I _{OH} = -100 μA, V _{CC} = V _{CC min} | V _{CC} -0.4 | | | |
| V _{LKO} | Low V _{CC} Lock-Out Voltage | | 2.3 | | 2.5 | |

Notes

1. The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.
2. Maximum I_{CC} specifications are tested with V_{CC} = V_{CCmax}.
3. I_{CC} active while Embedded Erase or Embedded Program is in progress.
4. At extended temperature range (>+85°C), typical current is 5 μA and maximum current is 10 μA.
5. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.
Typical sleep mode current is 200 nA.
6. Not 100% tested.

14.2 Zero Power Flash

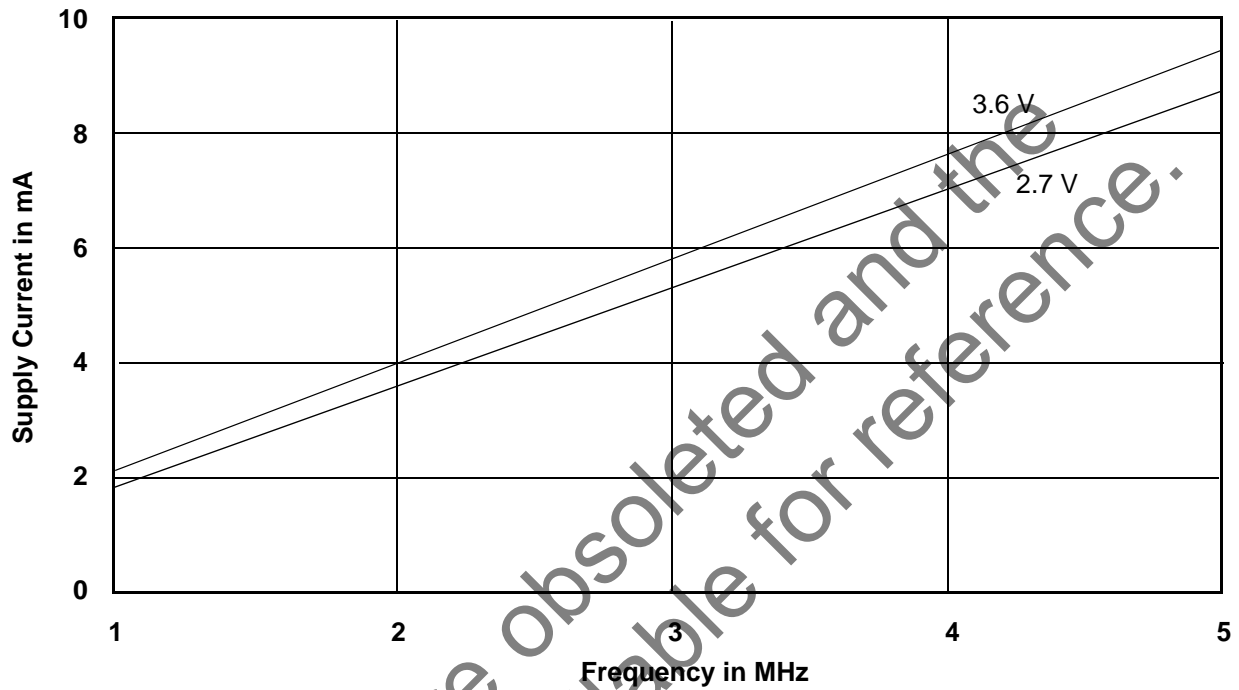
Figure 14.1 I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note

Addresses are switching at 1 MHz

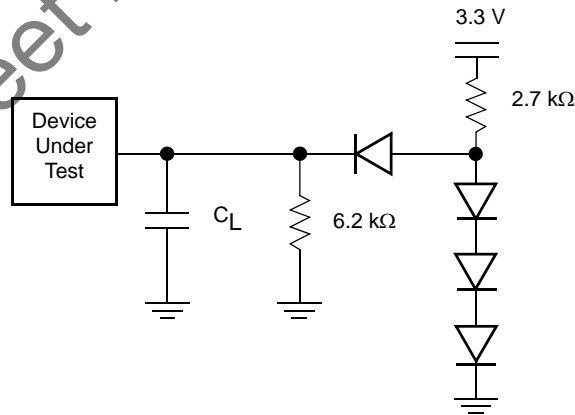
Figure 14.2 Typical I_{CC1} vs. Frequency



Note
 $T = 25^{\circ}C$

15. Test Conditions

Figure 15.1 Test Setup



Note
 Diodes are 1N3064 or equivalent.

Test Specifications

| Test Condition | 70 | 90 | Unit |
|---|-----------------|-----|------|
| Output Load | 1 TTL gate | | |
| Output Load Capacitance, C_L (including jig capacitance) | 30 | 100 | pF |
| Input Rise and Fall Times | 5 ns | | |
| Input Pulse Levels | 0.0 or V_{CC} | | |
| Input timing measurement reference levels | 0.5 V_{CC} | | |
| Output timing measurement reference levels | 0.5 V_{CC} | | |

16. Key to Switching Waveforms





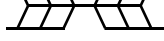
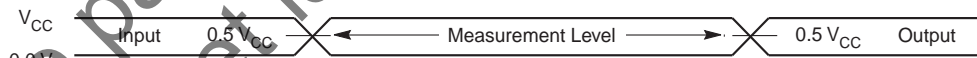
| Waveform | Inputs | Outputs |
|---|----------------------------------|--|
|  | Steady | |
|  | Changing from H to L | |
|  | Changing from L to H | |
|  | Don't Care, Any Change Permitted | Changing, State Unknown |
|  | Does Not Apply | Center Line is High Impedance State (High Z) |

Figure 16.1 Input Waveforms and Measurement Levels



These parts are obsolete and the datasheet is available for reference.

17. AC Characteristics

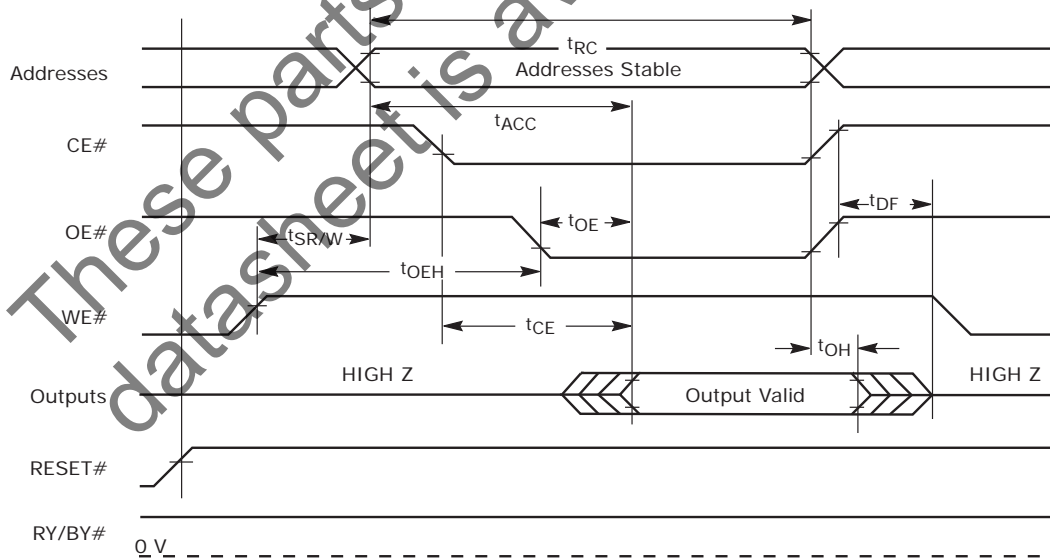
17.1 Read Operations

| Parameter | | Description | Test Setup | Speed Options | | Unit | |
|------------|------------|--|--|---------------|----|------|----|
| JEDEC | Std | | | 70 | 90 | | |
| t_{AVAV} | t_{RC} | Read Cycle Time (Note 1) | Min | 70 | 90 | ns | |
| t_{AVQV} | t_{ACC} | Address to Output Delay | CE# = V _{IL} OE# = V _{IL} | Max | 70 | | 90 |
| t_{ELQV} | t_{CE} | Chip Enable to Output Delay | OE# = V _{IL} | Max | 70 | | 90 |
| t_{GLQV} | t_{OE} | Output Enable to Output Delay | | Max | 80 | | 35 |
| t_{EHQZ} | t_{DF} | Chip Enable to Output High Z (Note 1) | | Max | 16 | | |
| t_{GHQZ} | t_{DF} | Output Enable to Output High Z (Note 1) | | Max | 16 | | |
| | $t_{SR/W}$ | Latency Between Read and Write Operations | | Min | 20 | | |
| | t_{OEh} | Output Enable Hold Time (Note 1) | Read | Min | 0 | | |
| | | Toggle and Data# Polling | Min | 10 | | | |
| t_{AXQX} | t_{OH} | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1) | Min | 0 | | | |

Notes

1. Not 100% tested.
2. See Figure 15.1 on page 35 and Table on page 36 for test specifications.

Figure 17.1 Read Operations Timings

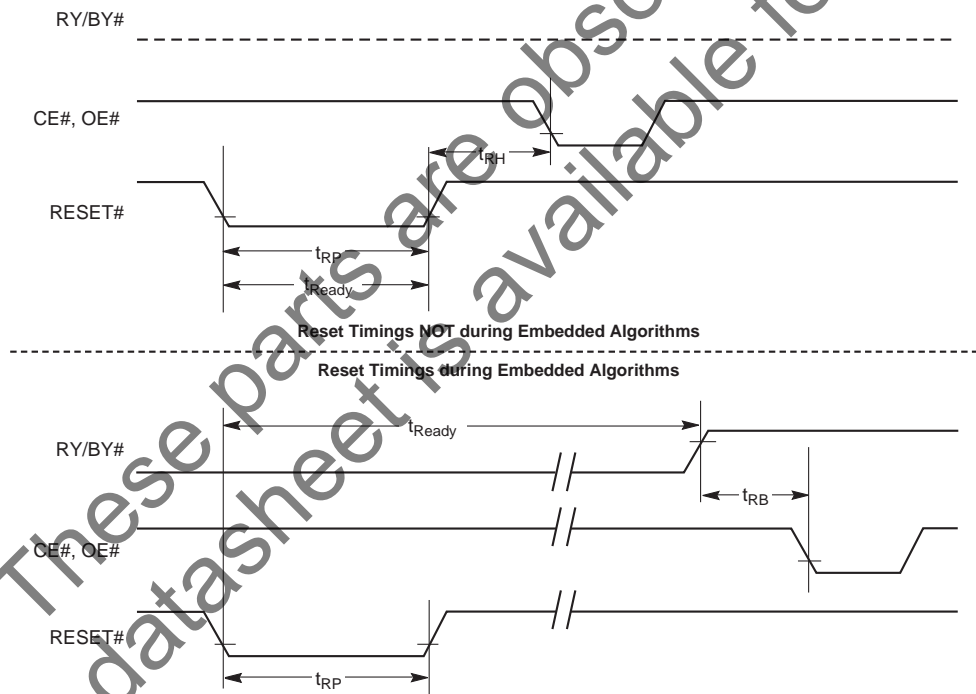


17.2 Hardware Reset (RESET#)

| Parameter | | Description | Test Setup | All Speed Options | Unit |
|-----------|--------------------|---|------------|-------------------|---------------|
| JEDEC | Std | | | | |
| | t_{READY} | RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note) | Max | 20 | μs |
| | t_{READY} | RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note) | Max | 500 | ns |
| | t_{RP} | RESET# Pulse Width | Min | 500 | |
| | t_{RH} | RESET# High Time Before Read (See Note) | | 50 | |
| | t_{RPD} | RESET# Low to Standby Mode | | 20 | μs |
| | t_{RB} | RY/BY# Recovery Time | | 0 | ns |

Note
Not 100% tested.

Figure 17.2 RESET# Timings



17.3 Word/Byte Configuration (BYTE#)

| Parameter | | Description | | Speed Options | | Unit |
|-----------|-----------------------------------|---------------------------------------|-----|---------------|----|------|
| JEDEC | Std | | | 70 | 90 | |
| | $t_{\text{ELFL}}/t_{\text{ELFH}}$ | CE# to BYTE# Switching Low or High | Max | 5 | ns | |
| | t_{FLQZ} | BYTE# Switching Low to Output HIGH Z | Max | 16 | | |
| | t_{FHQV} | BYTE# Switching High to Output Active | Min | 70 90 | | |

Figure 17.3 BYTE# Timings for Read Operations

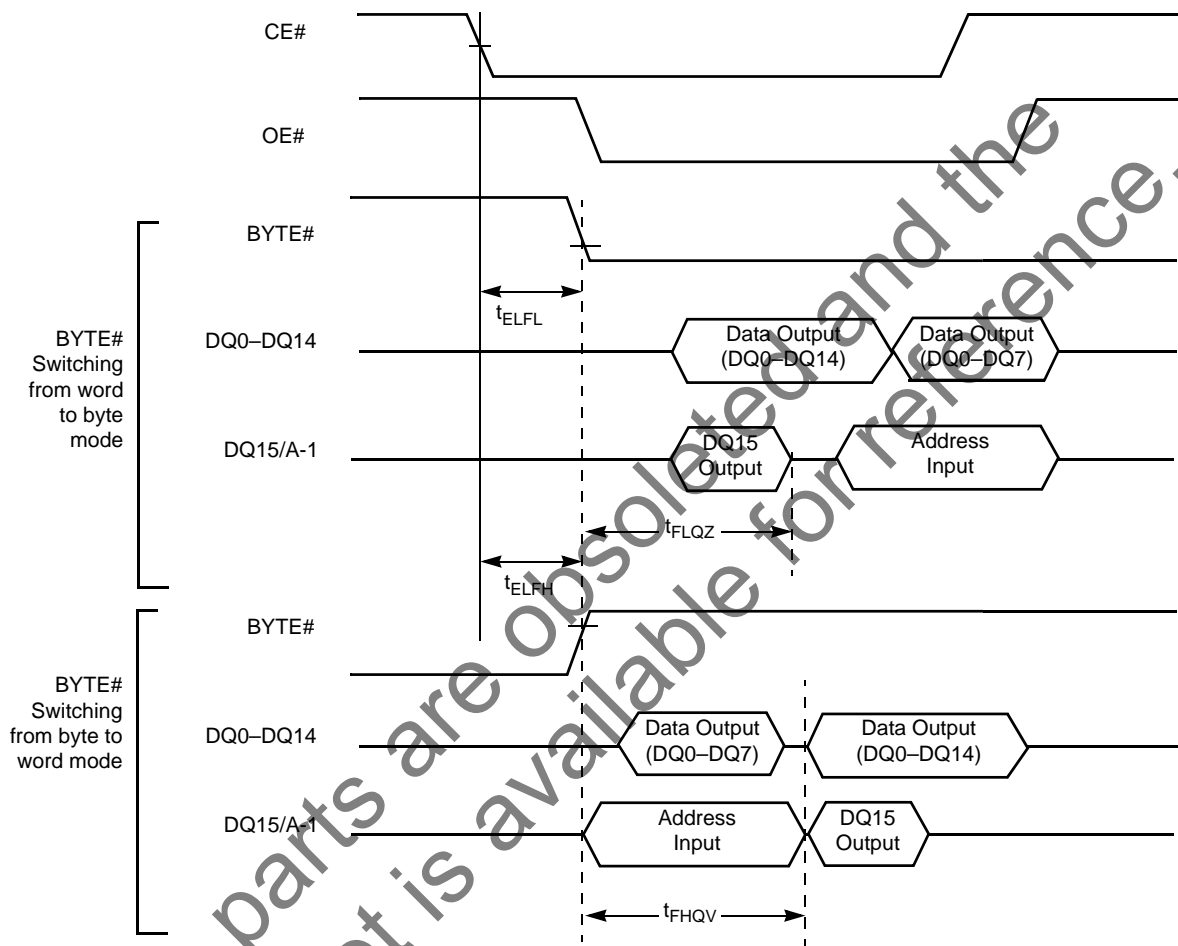
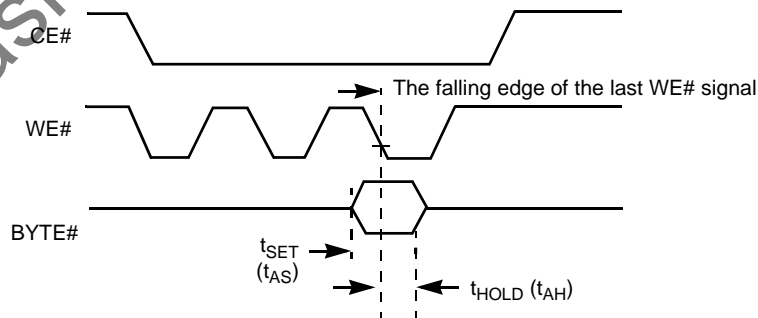


Figure 17.4 BYTE# Timings for Write Operations



Note
Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.

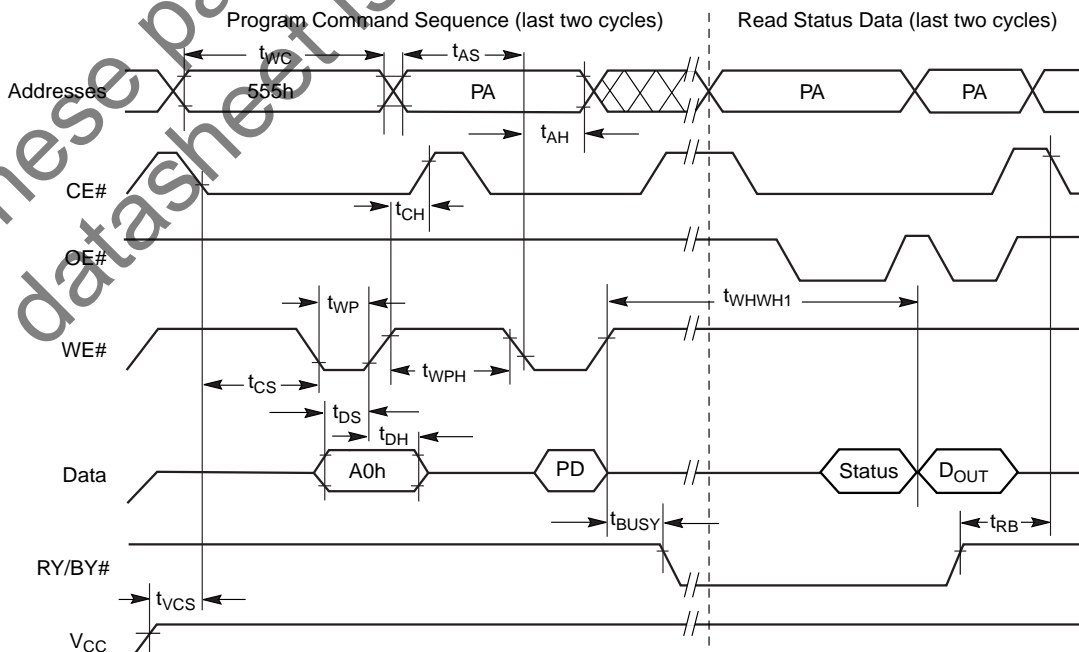
17.4 Erase/Program Operations

| Parameter | | Description | | Speed Options | | Unit | | |
|-------------|-------------|---|-----|---------------|-----|---------|------|---------|
| JEDEC | Std | | | 70 | 90 | | | |
| t_{AVAV} | t_{WC} | Write Cycle Time (Note 1) | 70 | 90 | Min | ns | | |
| t_{AVWL} | t_{AS} | Address Setup Time | 0 | | | | | |
| t_{WLAX} | t_{AH} | Address Hold Time | 45 | | | | | |
| t_{DVWH} | t_{DS} | Data Setup Time | 35 | 45 | | | | |
| t_{WHDX} | t_{DH} | Data Hold Time | 0 | | | | | |
| | t_{OES} | Output Enable Setup Time | 0 | | | | | |
| t_{GHWL} | t_{GHWL} | Read Recovery Time Before Write (OE# High to WE# Low) | 0 | | | | | |
| t_{ELWL} | t_{CS} | CE# Setup Time | 0 | | | | | |
| t_{WHEH} | t_{CH} | CE# Hold Time | 0 | | | | | |
| t_{WLWH} | t_{WP} | Write Pulse Width | 35 | | | | | |
| t_{WHWL} | t_{WPH} | Write Pulse Width High | 30 | | | | | |
| | $t_{SR/W}$ | Latency Between Read and Write Operations | 20 | | | | Min | ns |
| t_{WHWH1} | t_{WHWH1} | Programming Operation (Note 2) | 5 | | | | Byte | μ s |
| | | | 7 | | | | Word | μ s |
| t_{WHWH2} | t_{WHWH2} | Sector Erase Operation (Note 2) | 0.7 | | | sec | | |
| | t_{VCS} | V_{CC} Setup Time (Note 1) | 50 | | Min | μ s | | |
| | t_{RB} | Recovery Time from RY/BY# | 0 | | | ns | | |
| | t_{BUSY} | Program/Erase Valid to RY/BY# Delay | 90 | | Max | ns | | |

Notes

- Not 100% tested.
- See *Erase and Programming Performance* on page 45 for more information.

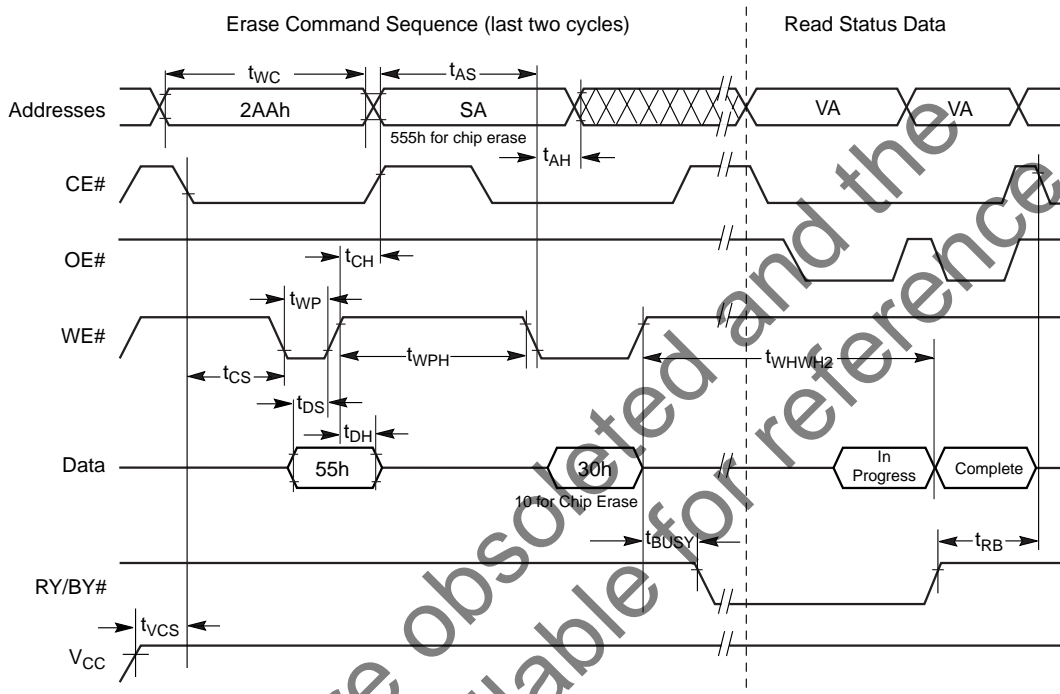
Figure 17.5 Program Operation Timings



Notes

- PA = program address, PD = program data, D_{OUT} is the true data at the program address.
- Illustration shows device in word mode.

Figure 17.6 Chip/Sector Erase Operation Timings



Notes

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see [Write Operation Status on page 28](#)).
2. Illustration shows device in word mode.

Figure 17.7 Back to Back Read/Write Cycle Timing

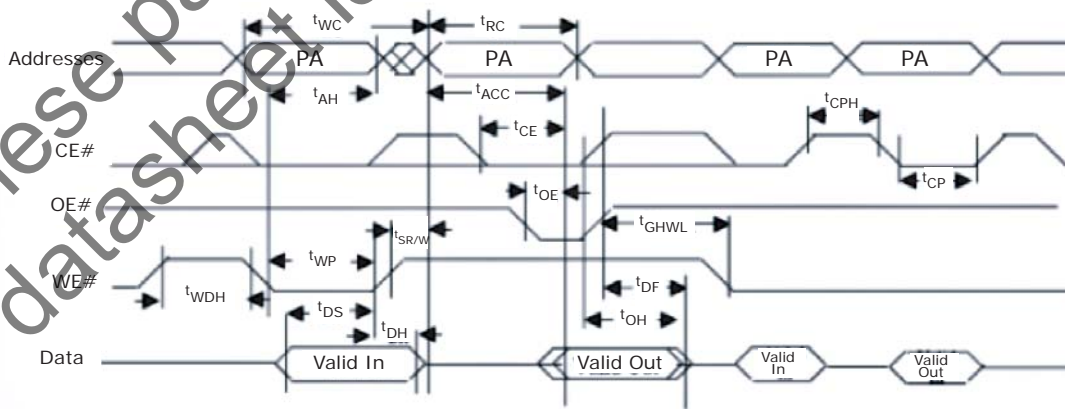
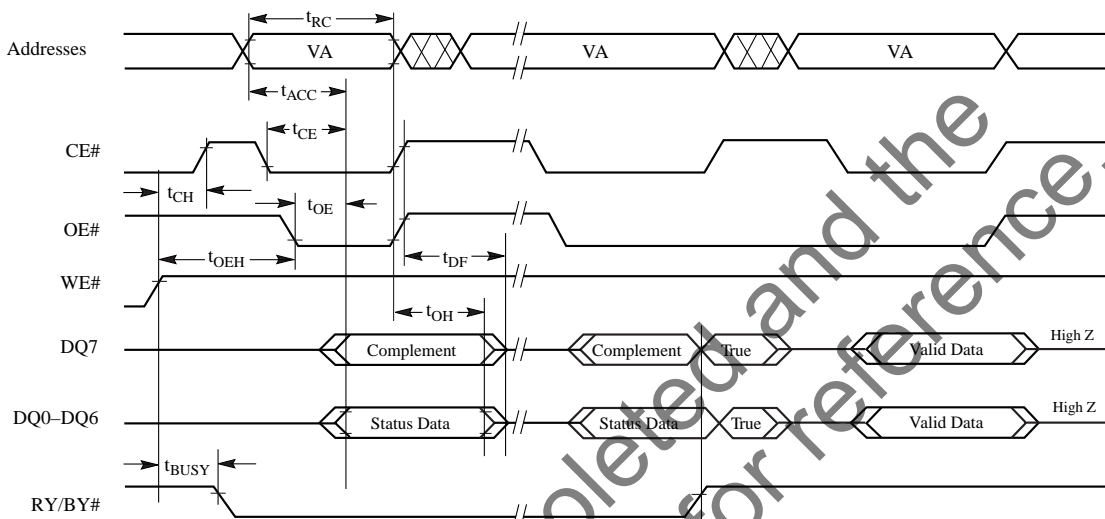


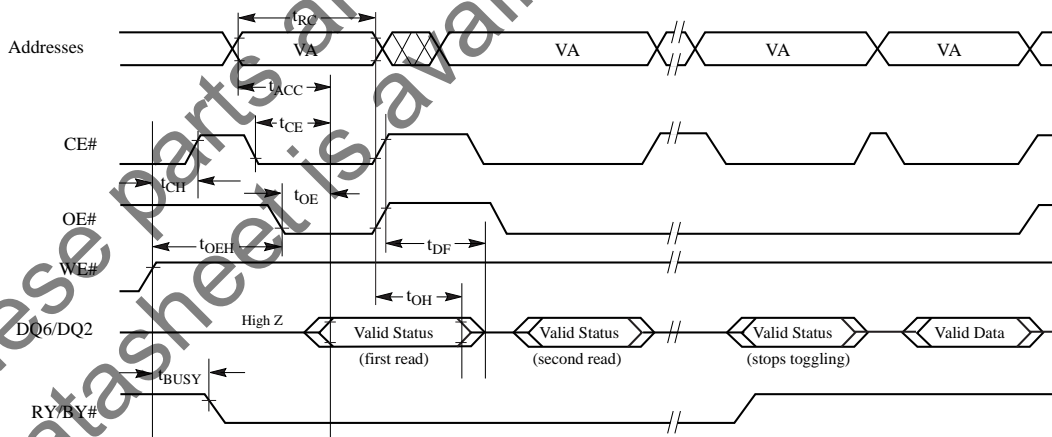
Figure 17.8 Data# Polling Timings (During Embedded Algorithms)



Note

VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

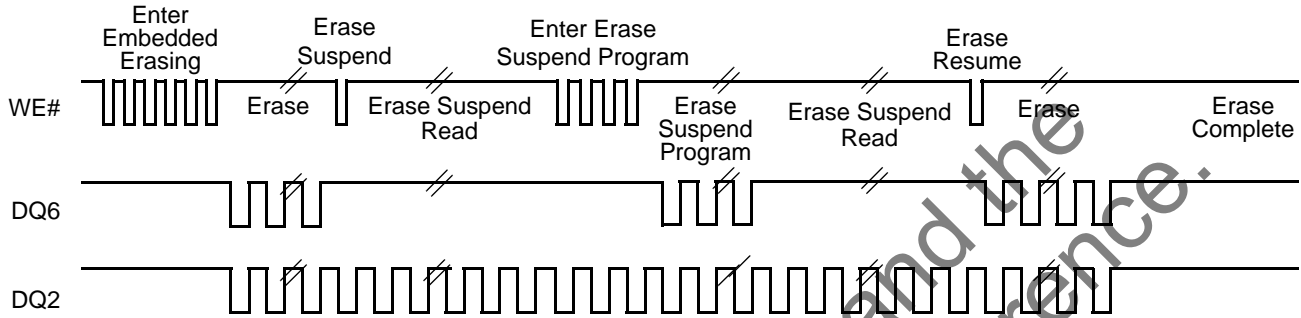
Figure 17.9 Toggle Bit Timings (During Embedded Algorithms)



Note

VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 17.10 DQ2 vs. DQ6 for Erase and Erase Suspend Operations



Note

The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.

17.5 Temporary Sector Unprotect

| Parameter | | Description | All Speed Options | Unit |
|-----------|-------------------|--|-------------------|------|
| JEDEC | Std | | | |
| | t _{VIDR} | V _{ID} Rise and Fall Time (See Note) | Min 500 | ns |
| | t _{RSP} | RESET# Setup Time for Temporary Sector Unprotect | Min 4 | µs |

Note

Not 100% tested.

Figure 17.11 Temporary Sector Unprotect/Timing Diagram

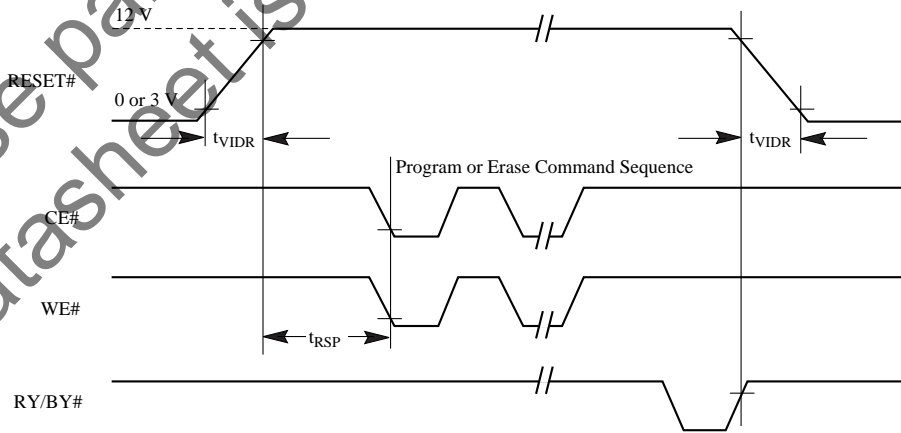
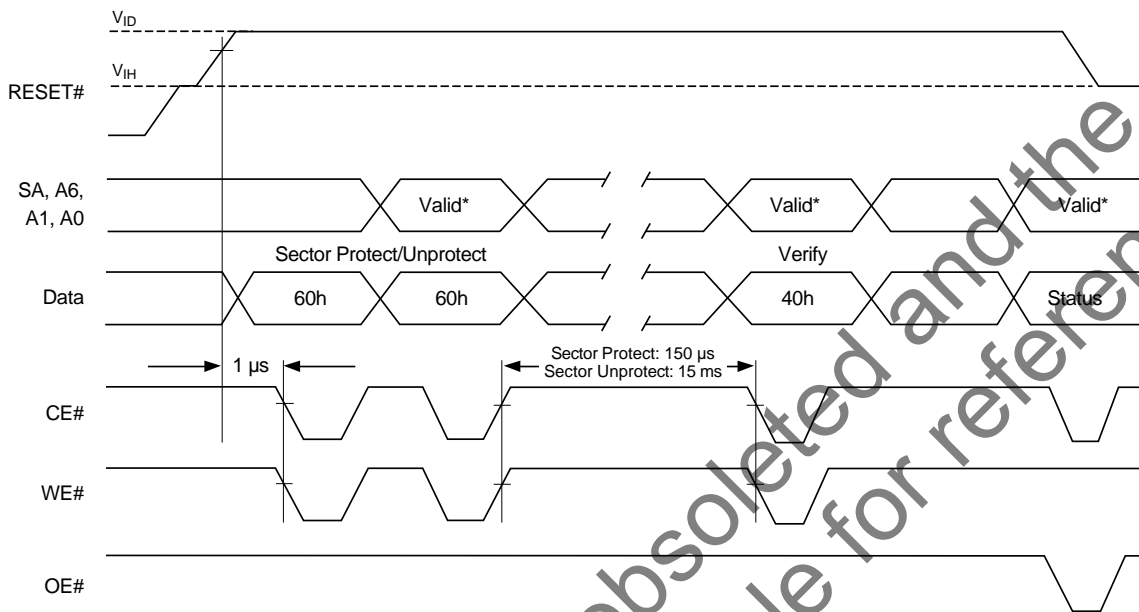


Figure 17.12 Sector Protect/Unprotect Timing Diagram



Note
For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

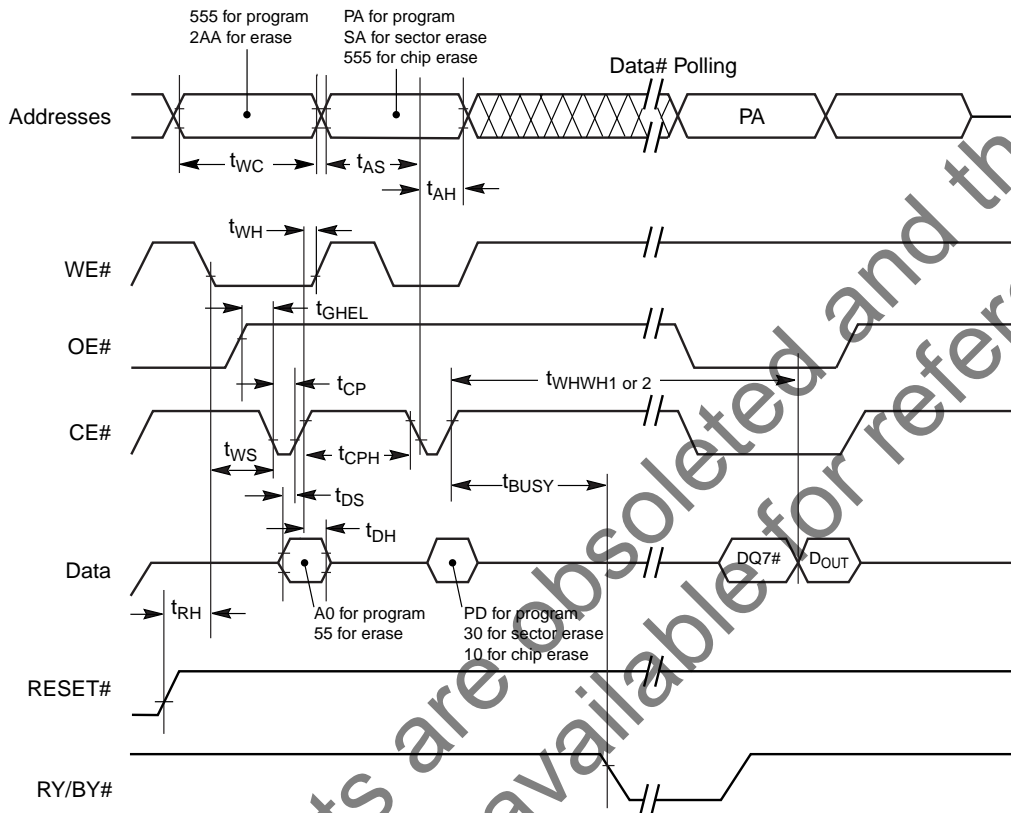
17.6 Alternate CE# Controlled Erase/Program Operations

| Parameter | | Description | | Speed Options | | Unit |
|--------------------|--------------------|---|------|---------------|----|------|
| JEDEC | Std | | | 70 | 90 | |
| t _{AVAV} | t _{WC} | Write Cycle Time (Note 1) | Min | 70 | 90 | ns |
| t _{AVEL} | t _{AS} | Address Setup Time | Min | 0 | | ns |
| t _{ELAX} | t _{AH} | Address Hold Time | Min | 45 | 45 | ns |
| t _{DVEH} | t _{DS} | Data Setup Time | Min | 35 | 45 | ns |
| t _{EHDX} | t _{DH} | Data Hold Time | Min | 0 | | ns |
| | t _{OES} | Output Enable Setup Time | Min | 0 | | ns |
| t _{GHEL} | t _{GHEL} | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0 | | ns |
| t _{WLEL} | t _{WS} | WE# Setup Time | Min | 0 | | ns |
| t _{EHWH} | t _{WH} | WE# Hold Time | Min | 0 | | ns |
| t _{ELEH} | t _{CP} | CE# Pulse Width | Min | 35 | 35 | ns |
| t _{EHEL} | t _{CPH} | CE# Pulse Width High | Min | 30 | | ns |
| | t _{SRW} | Latency Between Read and Write Operations | Min | 20 | | ns |
| t _{WHWH1} | t _{WHWH1} | Programming Operation (Note 2) | Byte | Typ | | 5 |
| | | | Word | Typ | | 7 |
| t _{WHWH2} | t _{WHWH2} | Sector Erase Operation (Note 2) | Typ | 0.7 | | sec |

Notes

1. Not 100% tested.
2. See Erase and Programming Performance on page 45 for more information.

Figure 17.13 Alternate CE# Controlled Write Operation Timings



Notes

1. PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.
2. Figure indicates the last two bus cycles of the command sequence.
3. Word mode address used as an example.

18. Erase and Programming Performance

| Parameter | Typ (Note 1) | Max (Note 2) | Unit | Comments |
|--------------------------------|--------------|--------------|------|--|
| Sector Erase Time | 0.7 | 10 | s | Excludes 00h programming prior to erasure (Note 4) |
| Chip Erase Time | 25 | | s | |
| Byte Programming Time | 7 | 210 | μs | Excludes system level overhead (Note 5) |
| Word Programming Time | 7 | 210 | μs | |
| Chip Programming Time (Note 3) | Byte Mode | 11 | s | |
| | Word Mode | 7.2 | 21.6 | |

Notes

1. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0 V, 100,000 cycles, checkerboard data pattern.
2. Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table on page 27 for further information on command definitions.
6. The device has a minimum erase and program cycle endurance of 100,000 cycles per sector.

19. TSOP, SO, and BGA Pin Capacitance

| Parameter Symbol | Parameter Description | Test Setup | Package | Typ | Max | Unit |
|------------------|-------------------------|----------------------|----------|-----|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = 0 | TSOP, SO | 6 | 7.5 | pF |
| | | | BGA | 4.2 | 5.0 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0 | TSOP, SO | 8.5 | 12 | pF |
| | | | BGA | 5.4 | 6.5 | pF |
| C _{IN2} | Control Pin Capacitance | V _{IN} = 0 | TSOP, SO | 7.5 | 9 | pF |
| | | | BGA | 3.9 | 4.7 | pF |

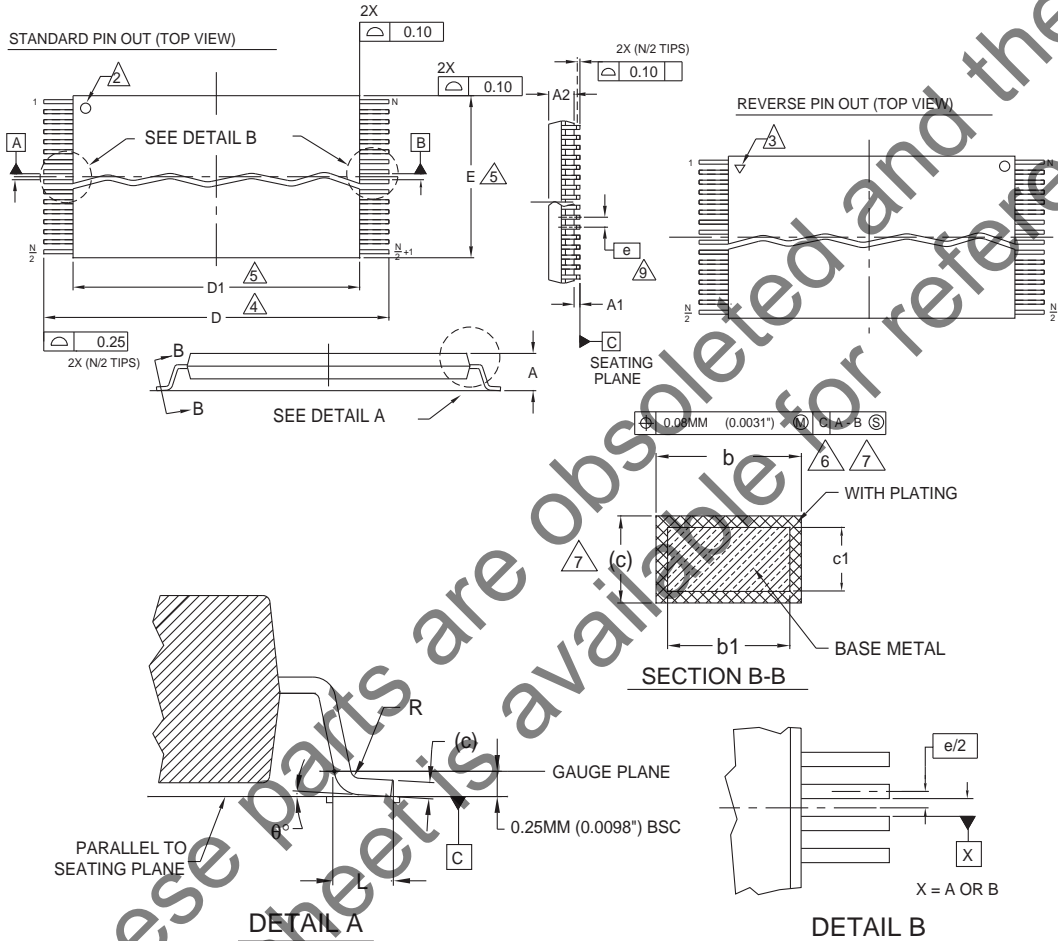
Notes

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz.

These parts are obsoleted and the datasheet is available for reference.

20. Physical Dimensions

20.1 TS 048—48-Pin Standard TSOP



| Jedec | MO-142 (D) DD | | |
|--------|---------------|-------|-------|
| Symbol | MIN | NOM | MAX |
| A | — | — | 0.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 19.80 | 20.00 | 20.20 |
| D1 | 18.30 | 18.40 | 18.50 |
| E | 11.90 | 12.00 | 12.10 |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | — | 8° |
| R | 0.08 | — | 0.20 |
| N | 48 | | |

NOTES:

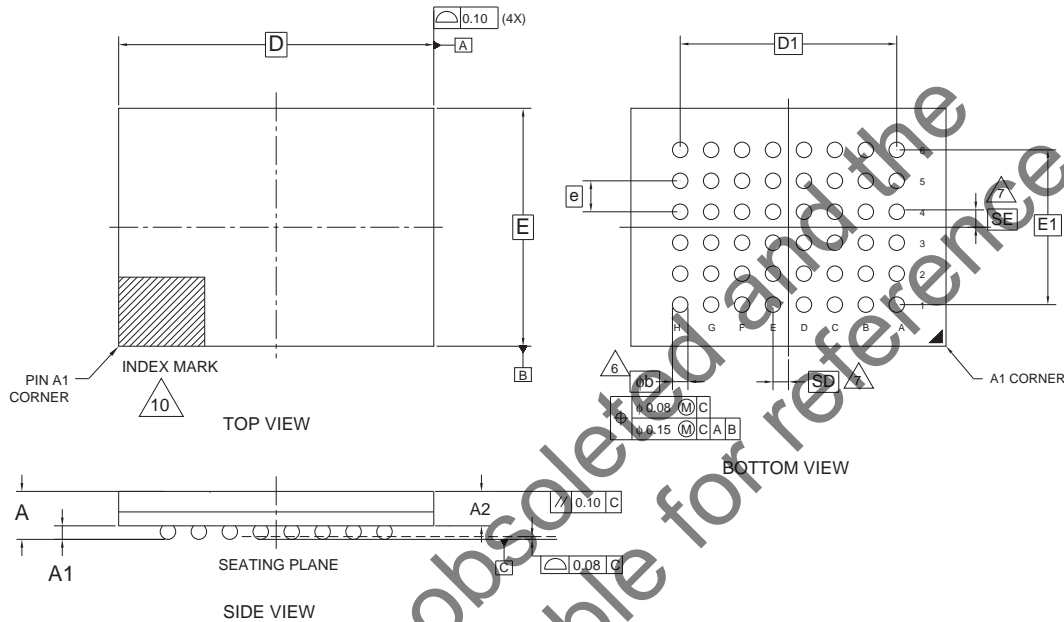
- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
- 2. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE UP).
- 3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
- 4. TO BE DETERMINED AT THE SEATING PLANE [C]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
- 5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15mm (.0059") PER SIDE.
- 6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
- 7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
- 8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
- 9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

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Note

For reference only. BSC is an ANSI standard for Basic Space Centering.

20.2 VBK048—48-Ball Fine-Pitch Ball Grid Array (FBGA) 8.15 mm x 6.15 mm



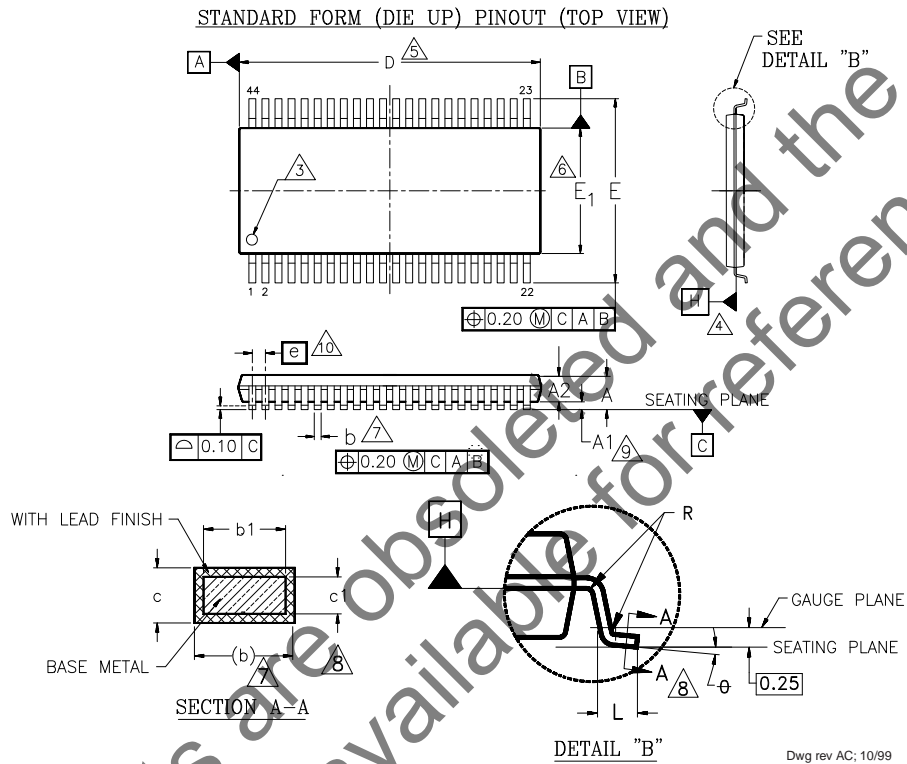
| PACKAGE | VBK 048 | | | |
|---------|-------------------------------|-----|------|-----------------------------|
| JEDEC | N/A | | | |
| | 8.15 mm x 6.15 mm NOM PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | | 1.00 | OVERALL THICKNESS |
| A1 | 0.18 | | --- | BALL HEIGHT |
| A2 | 0.62 | | 0.76 | BODY THICKNESS |
| D | 8.15 BSC. | | | BODY SIZE |
| E | 6.15 BSC. | | | BODY SIZE |
| D1 | 5.60 BSC. | | | BALL FOOTPRINT |
| E1 | 4.00 BSC. | | | BALL FOOTPRINT |
| MD | 8 | | | ROW MATRIX SIZE D DIRECTION |
| ME | 6 | | | ROW MATRIX SIZE E DIRECTION |
| N | 48 | | | TOTAL BALL COUNT |
| φb | 0.35 | | 0.43 | BALL DIAMETER |
| e | 0.80 BSC. | | | BALL PITCH |
| SD, SE | 0.40 BSC. | | | SOLDER BALL PLACEMENT |
| | --- | | | DEPOPULATED SOLDER BALLS |

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
N IS THE TOTAL NUMBER OF SOLDER BALLS.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- NOT USED.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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20.3 SO044—44-Pin Small Outline Package (SOP) 28.20 mm x 13.30 mm



| PACKAGE | SO 044 | | |
|---------|---------------|-------|-------|
| JEDEC | MO-180 (A) AA | | |
| SYMBOL | MIN | NOM | MAX |
| A | — | — | 2.80 |
| A1 | 0.15 | 0.23 | 0.35 |
| A2 | 2.17 | 2.30 | 2.45 |
| b | 0.35 | — | 0.50 |
| b1 | 0.35 | 0.40 | 0.45 |
| c | 0.10 | — | 0.21 |
| c1 | 0.10 | 0.15 | 0.18 |
| D | 28.00 | 28.20 | 28.40 |
| E | 15.70 | 16.00 | 16.30 |
| E1 | 13.10 | 13.30 | 13.50 |
| e | 1.27 BSC | | |
| L | 0.60 | 0.80 | 1.00 |
| R | 0.09 | — | — |
| theta | 0° | 4° | 8° |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm).
2. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. PIN 1 IDENTIFIER FOR STANDARD FORM (DIE UP) OR REVERSE FORM (DIE DOWN) PINOUTS.
4. DATUMS A AND B AND DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END.
6. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT EXCEED 0.15 mm PER SIDE. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07 mm AT LEAST MATERIAL CONDITION.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIPS.
9. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.
10. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
11. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THEIR SEATING PLANE.

21. Revision Summary

Spansion Publication Number: S29AL016D_00

21.1 Revision A (May 4, 2004)

Initial Release.

21.2 Revision A1 (July 28, 2004)

Ordering Information

Updated ordering information: model number, speed options, and valid combinations for TSOP and BGA packages.

DC Characteristics

Updated Max information for I_{CC2}.

Physical Dimensions

Updated VBK048 and TS048 drawings.

21.3 Revision A2 (December 17, 2004)

Data Sheet Type

Changed from Advance Information to Preliminary.

Ordering Information

Updated ordering information: Small Outline Package options

Physical Dimensions

Added SO044 Package.

21.4 Revision A3 (June 1, 2005)

Global

Updated status to full data sheet.

Ordering Information

Added tube and tray packing types.

Added Extended Temperature range.

Valid Combinations Table

Added two designators to packing types.

Added package types for extended temperature.

Added Note for this table.

Operating Ranges

Added Extended Temperature range information.

Erase and Programming Performance

Changed Byte Programming Time values for Typical and Maximum.

Pin Capacitance Table

Added SO package to Pin Capacitance table.

Global

Updated Trademark.

21.5 Revision A4 (June 17, 2005)

Ordering Information

Changed packing type from “1, 3” to “0, 1, 3”

21.6 Revision A5 (May 22, 2006)

AC Characteristics

Added t_{SRW} parameter to read and erase/program operations tables. Added back-to-back read/write cycle timing diagram. Changed maximum value for t_{DF} and t_{FLQZ} .

21.7 Revision A6 (September 7, 2007)

Command Definitions Table

Changed the 2nd cycle data of the Unlock Bypass Reset command from 'F0' to '00'.

21.8 Revision A7 (November 27, 2007)

Figure: Read Operations Timings

Updated figure

21.9 Revision A8 (February 27, 2009)

Global

Added obsolescence information to Cover Sheet, Distinctive Characteristics, and Ordering Information sections of data sheet.

Document History Page

| Document Title: S29AL016D 16 Mbit (2 M x 8-Bit/1 M x 16-Bit), 3 V Boot Sector Flash | | | | |
|---|---------|-----------------|-----------------|---|
| Document Number: 002-01232 | | | | |
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | - | RYSU | 05/04/2004 | Initial release |
| | | | 07/28/2004 | Ordering Information Updated ordering information: model number, speed options, and valid combinations for TSOP and BGA packages. DC Characteristics Updated Max information for ICC2. Physical Dimensions Updated VBK048 and TS048 drawings. |

Document History Page (Continued)

| Document Title: S29AL016D 16 Mbit (2 M x 8-Bit/1 M x 16-Bit), 3 V Boot Sector Flash | | | | |
|---|---------|-----------------|-----------------|--|
| Document Number: 002-01232 | | | | |
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | - | RYSU | 12/17/2004 | Data Sheet Type Changed from Advance Information to Preliminary. Ordering Information Updated ordering information: Small Outline Package options Physical Dimensions Added SO044 Package. |
| | | | 06/01/2005 | Global Updated status to full data sheet. Ordering Information Added tube and tray packing types. Added Extended Temperature range. Valid Combinations Table Added two designators to packing types. Added package types for extended temperature. Added Note for this table. Operating Ranges Added Extended Temperature range information. Erase and Programming Performance Changed Byte Programming Time values for Typical and Maximum. Pin Capacitance Table Added SO package to Pin Capacitance table. Global Updated Trademark. |
| | | | 06/17/2005 | Ordering Information Changed packing type from "1, 3" to "0, 1, 3" |
| ** | - | RYSU | 05/22/2006 | AC Characteristics Added tSR/W parameter to read and erase/program operations tables. Added back-to-back read/write cycle timing diagram. Changed maximum value for tDF and tFLQZ. |
| | | | 09/07/2007 | Command Definitions Table Changed the 2nd cycle data of the Unlock Bypass Reset command from 'F0' to '00'. |
| | | | 11/27/2007 | Figure: Read Operations Timings Updated figure |
| | | | 02/27/2009 | Global Added obsolescence information to Cover Sheet, Distinctive Characteristics, and Ordering Information sections of data sheet. |
| *A | 5034596 | RYSU | 12/07/2015 | Updated to Cypress Template |

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These parts are obsoleted and the datasheet is available for reference.

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