S29PL127H/S29PL129H

for Multi-Chip Products (MCP)

128 Megabit (8 M x 16-Bit) CMOS 3.0 Volt-only, Simultaneous Read/Write Page Mode Flash Memory

Datasheet

PRELIMINARY

Distinctive Characteristics

ARCHITECTURAL ADVANTAGES

- **128 Mbit Page Mode device**
  - Page size of 8 words: Fast page read access from random locations within the page
- **Dual Chip Enable Inputs (S29PL129 only)**
  - Each CE# input controls a 64 Mbit address space
- **Single power supply operation**
  - Full Voltage range: 2.7 to 3.6 volt read, erase, and program operations for battery-powered applications
- **Simultaneous Read/Write Operation**
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency switching from write to read operations
- **Flexible Bank Architecture**
  - 4 separate banks, with up to two simultaneous operations per device

S29PL127H:

  - Bank A: 16 Mbit (4 Kw x 8 and 32 Kw x 31)
  - Bank B: 48 Mbit (32 Kw x 96)
  - Bank C: 48 Mbit (32 Kw x 96)
  - Bank D: 16 Mbit (4 Kw x 8 and 32 Kw x 31)

S29PL129H:

  - Bank 1A: 48 Mbit (32 Kw x 96)
  - Bank 1B: 16 Mbit (4 Kw x 8 and 32 Kw x 31)
  - Bank 2A: 16 Mbit (4 Kw x 8 and 32 Kw x 31)
  - Bank 2B: 48 Mbit (32 Kw x 96)
- **SecSi™ (Secured Silicon) Sector region**
  - Up to 128 words accessible through a command sequence
  - Up to 64 factory-locked words
  - Up to 64 customer-lockable words
- **Both top and bottom boot blocks in one device**
- **Manufactured on 130 nm process technology**
- **Data retention: 20-years typical**
- **Cycling Endurance: 1 million cycles per sector**

PERFORMANCE CHARACTERISTICS

- **High Performance**
  - Page access times as fast as 30 ns
  - Random access times as fast as 70 ns
- **Power consumption (typical values at 10 MHz)**
  - 45 mA active read current
  - 15 mA program/erase current
  - 1 µA typical standby mode current

SOFTWARE FEATURES

- **Software command-set compatible with JEDEC 42.4 standard**
  - Backward compatible with Am29F and Am29LV families
- **CFI (Common Flash Interface) compliant**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend / Erase Resume**
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- **Ready/Busy# pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - Hardware method to reset the device to reading array data
- **WP#/ ACC (Write Protect/Acceleration) input**
  - At V_{IL}, hardware level protection for the first and last two 4K word sectors.
  - At V_{IH}, allows removal of sector protection
  - At V_{HH}, provides accelerated programming in a factory setting
- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password
- **Package options**
  - Multi Chip Packages (MCP)

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General Description

The S29PL127H/S29PL129H is a 128 Mbit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory device organized as 8 Mwords. The device is offered in various multi-chip packages. The word-wide data (x16) appears on DQ15-DQ0. This device can be programmed in-system or in standard EPROM programmers. A 12.0 V V_{PP} is not required for write or erase operations.

The device offers fast page access times of 30 ns, with corresponding random access times of 70 ns allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls. Simultaneous Read/Write Operation with Zero Latency. Dual Chip Enables allow access to two 64 Mbit partitions of the 128 Mbit memory space (S29PL129H only).

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.

The device can be organized in both top and bottom sector configurations. The banks are organized as follows:

Chip Enable Configuration (S29PLI27H)	
Bank	**Sectors**
A	I6 Mbit (4 Kw x 8 and 32 Kw x 3I)
B	48 Mbit (32 Kw x 96)
C	48 Mbit (32 Kw x 96)
D	I6 Mbit (4 Kw x 8 and 32 Kw x 3I)

Chip Enable Configuration (S29PLI29H)	
CEI# Control	**CE2# Control**
Bank IA I6 Mbit (4 Kw x 8 and 32 Kw x 3I)	**Bank 2A** 48 Mbit (32 Kw x 96)
Bank IB 48 Mbit (32 Kw x 96)	**Bank 2B** I6 Mbit (4 Kw x 8 and 32 Kw x 3I)

Page Mode Features

The page size is 8 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the SecSi Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

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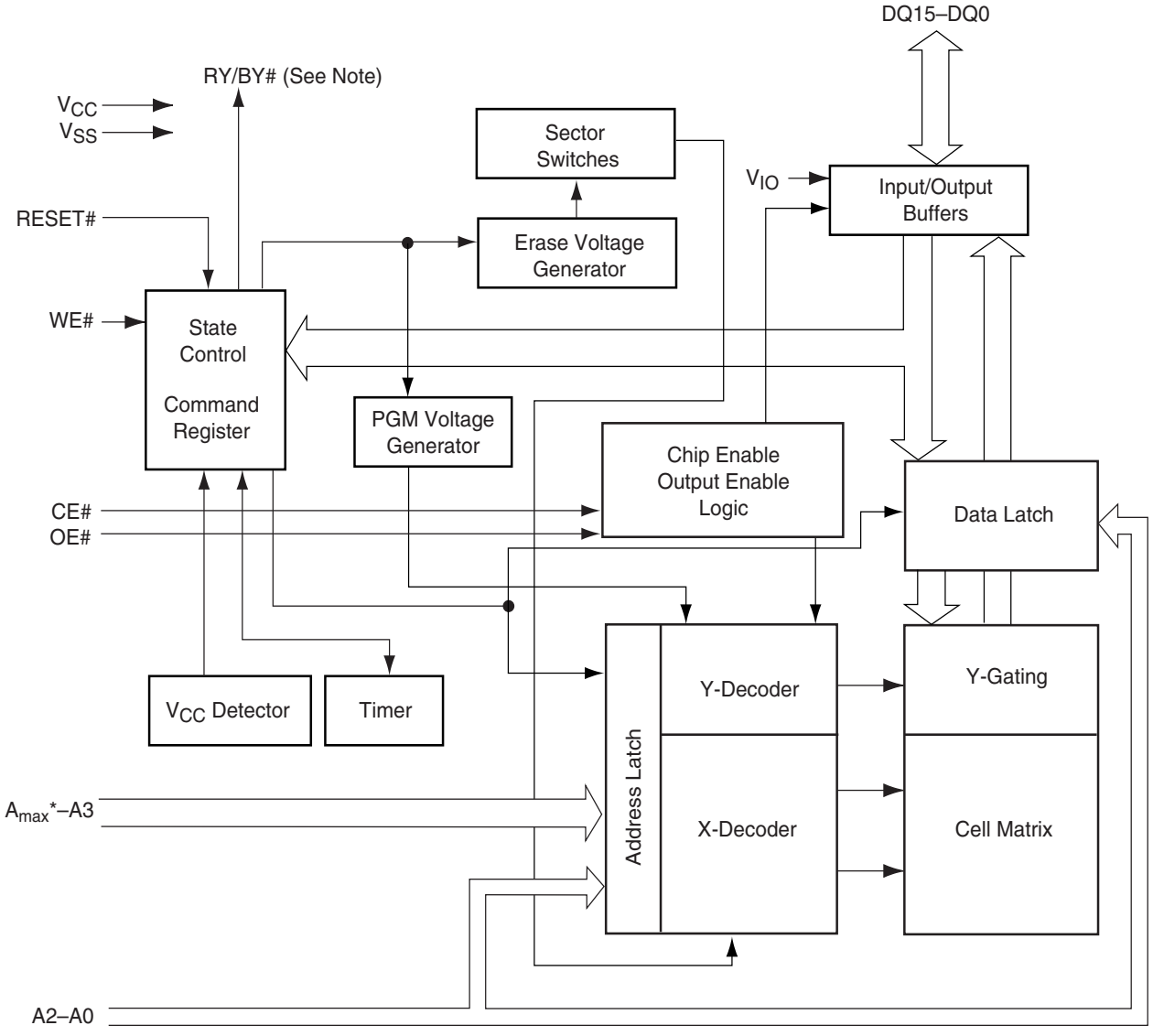
PRODUCT SELECTOR GUIDE

Part Number		S29PLI27H/S29PLI29H
Speed Option	V_{CC},V_{IO} = 2.7–3.6 V	70
Max Access Time, ns (t_{ACC})		70
Max CE# Access, ns (t_{CE})		
Max Page Access, ns (t_{PACC})		30
Max OE# Access, ns (t_{OE})		

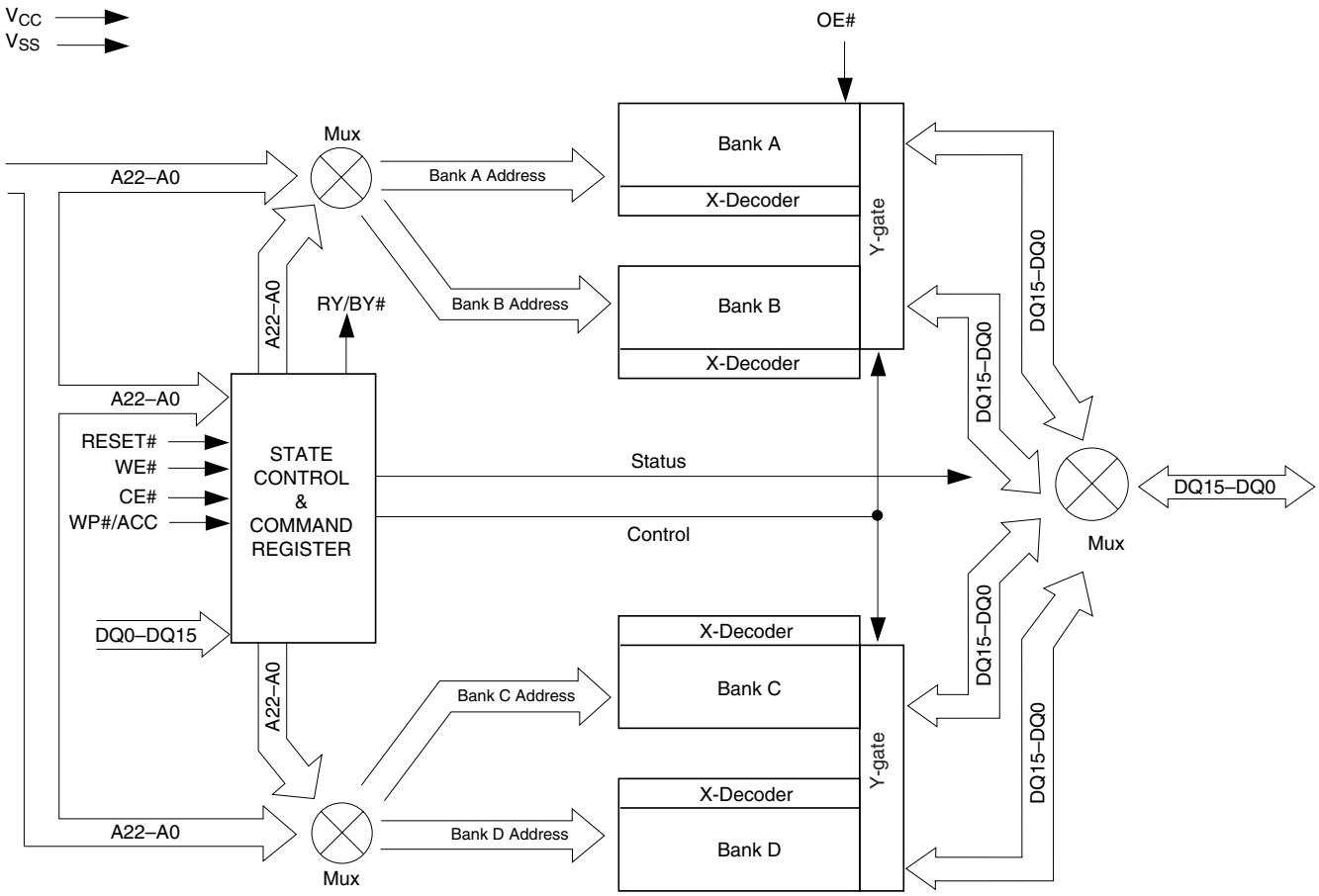
Block Diagram



Note:RY/BY# is an open drain output.

** A_{max}= Amax (S29PL127H only) or A21 (S29PL129H only)*

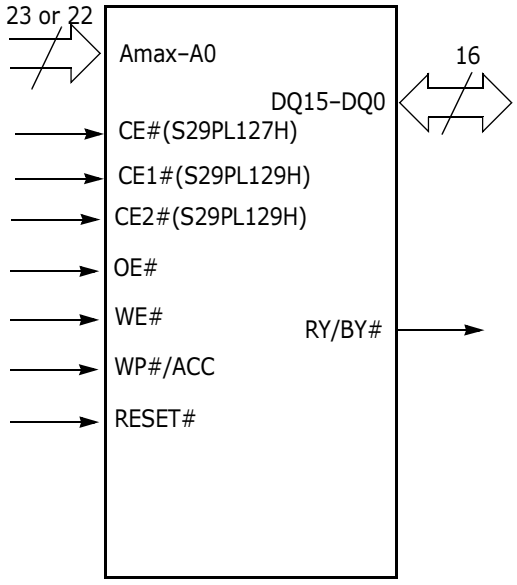
SIMULTANEOUS OPERATION BLOCK DIAGRAM



PIN DESCRIPTION

Amax–A0	=	23 or 22-bit address bus for 128 Mb device
DQ15–DQ0	=	16-bit data inputs/outputs/float
CE#	=	Chip Enable Input (S29PL127H)
CE1#, CE2#	=	Chip Enable Inputs (S29PL129H)
OE#	=	Output Enable Input
WE#	=	Write Enable
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally
RY/BY#	=	Ready/Busy output and open drain. When RY/BY#= V_{IH}, the device is ready to accept read operations and commands. When RY/BY#= V_{OL}, the device is either executing an embedded algorithm or the device is executing a hardware reset operation.
WP#/ACC	=	Write Protect/Acceleration Input. When WP/ACC#= V_{IL}, the highest and lowest two 4K-word sectors are write protected regardless of other sector protection configurations. When WP/ACC#= V_{IH}, these sector are unprotected unless the DYB or PPB is programmed. When WP/ACC#= 12V, program and erase operations are accelerated.
V_{CC}	=	Chip Power Supply (2.7 V to 3.6 V)
RESET#	=	Hardware Reset Pin

Logic Symbol



DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. S29PL127H/S29PL129H Device Bus Operations

Operation	CE# (Note 3)	OE#	WE#	RESET#	WP#/ACC	Addresses (Amax–A0)	DQI5–DQ0
Read	L	L	H	H	X	A_{IN}	D_{OUT}
Write	L	H	L	H	X	A_{IN}	D_{IN}
Standby	$V_{IO}\pm$ 0.3 V	X	X	$V_{IO}\pm$ 0.3 V	X (Note 2)	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z
Reset	X	X	X	L	X	X	High-Z
Temporary Sector Unprotect (High Voltage)	X	X	X	V_{ID}	X	A_{IN}	D_{IN}

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 8.5–9.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the High Voltage Sector Protection section.*
2. *WP#/ACC must be high when writing to sectors 0, 1, 268, or 269. (S29PL127H); or SA1-133, SA1-134, SA2-0, or SA2-1 (S29PL129H).*
3. *For S29PL129H, CE1# and CE2# must not be Low simultaneously.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the OE# and appropriate CE# pins to V_{IL}. CE# is the power control. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to the AC Characteristics table for timing specifications and to Figure 11 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Random Read (Non-Page Read)

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable

access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Address bits Amax–A3 select an 8 word page, and address bits A2–A0 select a specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted (CE#=V_{IH}), the reassertion of CE# for subsequent access has access time of t_{ACC} or t_{CE}. Here again, CE# selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping Amax–A3 constant and changing A2–A0 to select the specific word within that page.

Table 2. Page Select

Word	A2	AI	A0
Word 0	0	0	0
Word I	0	0	I
Word 2	0	I	0
Word 3	0	I	I
Word 4	I	0	0
Word 5	I	0	I
Word 6	I	I	0
Word 7	I	I	I

Simultaneous Operation

In addition to the conventional features (read, program, erase-suspend read, and erase-suspend program), the device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation). The bank can be selected by bank addresses (Amax–A20) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

Table 3. Bank Select (S29PLI27H)

Bank	A22–A20
Bank A	000
Bank B	001, 010, 011
Bank C	100, 101, 110
Bank D	111

Table 4. Bank Select (S29PLI29H)

Bank	CE1#	CE2#	A21–A20
Bank 1A	0	1	00, 01, 10
Bank 1B	0	1	11
Bank 2A	1	0	00
Bank 2B	1	0	01, 10, 11

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The "Word Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 4 indicates the address space that each sector occupies. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "sector address" refers to the address bits required to uniquely select a sector. The "Command Definitions" section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin should be raised to V_{CC} when not in*

use. That is, the WP#/ACC pin should not be left floating or unconnected; inconsistent behavior of the device may result.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Command Sequence section for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{IO} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{IO} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the CMOS standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 150 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at V_{IH} before the device reduces current to the stated sleep mode specification. I_{CC5} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 15 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins (except for RY/BY#) are placed in the highest Impedance state

Table 5. S29PLI27H Sector Architecture

Bank	Sector	Sector Address (A22-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank A	SA0	00000000000	4	000000h–000FFFh
	SAI	00000000001	4	001000h–001FFFh
	SA2	00000000010	4	002000h–002FFFh
	SA3	00000000011	4	003000h–003FFFh
	SA4	00000000100	4	004000h–004FFFh
	SA5	00000000101	4	005000h–005FFFh
	SA6	00000000110	4	006000h–006FFFh
	SA7	00000000111	4	007000h–007FFFh
	SA8	00000001XXX	32	008000h–00FFFFh
	SA9	00000010XXX	32	010000h–017FFFh
	SAI0	00000011XXX	32	018000h–01FFFFh
	SAII	00000100XXX	32	020000h–027FFFh
	SAI2	00000101XXX	32	028000h–02FFFFh
	SAI3	00000110XXX	32	030000h–037FFFh
	SAI4	00000111XXX	32	038000h–03FFFFh
	SAI5	00001000XXX	32	040000h–047FFFh
	SAI6	00001001XXX	32	048000h–04FFFFh
	SAI7	00001010XXX	32	050000h–057FFFh
	SAI8	00001011XXX	32	058000h–05FFFFh
	SAI9	00001100XXX	32	060000h–067FFFh
	SA20	00001101XXX	32	068000h–06FFFFh
	SA2I	00001110XXX	32	070000h–077FFFh
	SA22	00001111XXX	32	078000h–07FFFFh
	SA23	00010000XXX	32	080000h–087FFFh
	SA24	00010001XXX	32	088000h–08FFFFh
	SA25	00010010XXX	32	090000h–097FFFh
	SA26	00010011XXX	32	098000h–09FFFFh
	SA27	00010100XXX	32	0A0000h–0A7FFFh
	SA28	00010101XXX	32	0A8000h–0AFFFFh
	SA29	00010110XXX	32	0B0000h–0B7FFFh
	SA30	00010111XXX	32	0B8000h–0BFFFFh
	SA3I	00011000XXX	32	0C0000h–0C7FFFh
	SA32	00011001XXX	32	0C8000h–0CFFFFh
	SA33	00011010XXX	32	0D0000h–0D7FFFh
	SA34	00011011XXX	32	0D8000h–0DFFFFh
	SA35	00011100XXX	32	0E0000h–0E7FFFh
	SA36	00011101XXX	32	0E8000h–0EFFFFh
	SA37	00011110XXX	32	0F0000h–0F7FFFh
	SA38	00011111XXX	32	0F8000h–0FFFFFh

Table 5. S29PLI27H Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank B	SA39	00I00000XXX	32	I00000h–I07FFFh
	SA40	00I0000IXXX	32	I08000h–I0FFFFh
	SA4I	00I000I0XXX	32	I10000h–I17FFFh
	SA42	00I000IIXXX	32	I18000h–IIFFFFh
	SA43	00I00I00XXX	32	I20000h–I27FFFh
	SA44	00I00I0IXXX	32	I28000h–I2FFFFh
	SA45	00I00II0XXX	32	I30000h–I37FFFh
	SA46	00I00IIIXXX	32	I38000h–I3FFFFh
	SA47	00I0I000XXX	32	I40000h–I47FFFh
	SA48	00I0I00IXXX	32	I48000h–I4FFFFh
	SA49	00I0I0I0XXX	32	I50000h–I57FFFh
	SA50	00I0I0IIXXX	32	I58000h–I5FFFFh
	SA5I	00I0II00XXX	32	I60000h–I67FFFh
	SA52	00I0II0IXXX	32	I68000h–I6FFFFh
	SA53	00I0III0XXX	32	I70000h–I77FFFh
	SA54	00I0IIIIXXX	32	I78000h–I7FFFFh
	SA55	00II0000XXX	32	I80000h–I87FFFh
	SA56	00II000IXXX	32	I88000h–I8FFFFh
	SA57	00II00I0XXX	32	I90000h–I97FFFh
	SA58	00II00IIXXX	32	I98000h–I9FFFFh
	SA59	00II0I00XXX	32	IA0000h–IA7FFFh
	SA60	00II0I0IXXX	32	IA8000h–IAFFFFh
	SA6I	00II0II0XXX	32	IB0000h–IB7FFFh
	SA62	00II0IIIXXX	32	IB8000h–IBFFFFh
	SA63	00III000XXX	32	IC0000h–IC7FFFh
	SA64	00III00IXXX	32	IC8000h–ICFFFFh
	SA65	00III0I0XXX	32	ID0000h–ID7FFFh
	SA66	00III0IIXXX	32	ID8000h–IDFFFFh
	SA67	00IIII00XXX	32	IE0000h–IE7FFFh
	SA68	00IIII0IXXX	32	IE8000h–IEFFFFh
	SA69	00IIIII0XXX	32	IF0000h–IF7FFFh
	SA70	00IIIIIIXXX	32	IF8000h–IFFFFFh
	SA7I	0I000000XXX	32	200000h–207FFFh
	SA72	0I00000IXXX	32	208000h–20FFFFh
	SA73	0I0000I0XXX	32	210000h–217FFFh
	SA74	0I0000IIXXX	32	218000h–21FFFFh
	SA75	0I000I00XXX	32	220000h–227FFFh
	SA76	0I000I0IXXX	32	228000h–22FFFFh
	SA77	0I000II0XXX	32	230000h–237FFFh
	SA78	0I000IIIXXX	32	238000h–23FFFFh

Table 5. S29PLI27H Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-AI2)	Sector Size (Kwords)	Address Range (x16)
Bank B	SA79	0100I000XXX	32	240000h–247FFFh
	SA80	0100I001XXX	32	248000h–24FFFFh
	SA8I	0100I010XXX	32	250000h–257FFFh
	SA82	0100I011XXX	32	258000h–25FFFFh
	SA83	0100I100XXX	32	260000h–267FFFh
	SA84	0100I101XXX	32	268000h–26FFFFh
	SA85	0100I110XXX	32	270000h–277FFFh
	SA86	0100IIIIXXX	32	278000h–27FFFFh
	SA87	0101I000XXX	32	280000h–287FFFh
	SA88	0101I001XXX	32	288000h–28FFFFh
	SA89	0101I010XXX	32	290000h–297FFFh
	SA90	0101I011XXX	32	298000h–29FFFFh
	SA9I	0101I100XXX	32	2A0000h–2A7FFFh
	SA92	0101I101XXX	32	2A8000h–2AFFFFh
	SA93	0101I110XXX	32	2B0000h–2B7FFFh
	SA94	0101I111XXX	32	2B8000h–2BFFFFh
	SA95	0101II000XXX	32	2C0000h–2C7FFFh
	SA96	0101II001XXX	32	2C8000h–2CFFFFh
	SA97	0101II010XXX	32	2D0000h–2D7FFFh
	SA98	0101II011XXX	32	2D8000h–2DFFFFh
	SA99	0101III00XXX	32	2E0000h–2E7FFFh
	SAI00	0101III01XXX	32	2E8000h–2EFFFFh
	SAI0I	0101IIII0XXX	32	2F0000h–2F7FFFh
	SAI02	0101IIIIIXXX	32	2F8000h–2FFFFFh
	SAI03	0110000XXX	32	300000h–307FFFh
	SAI04	0110001XXX	32	308000h–30FFFFh
	SAI05	0110010XXX	32	310000h–317FFFh
	SAI06	0110011XXX	32	318000h–31FFFFh
	SAI07	0110100XXX	32	320000h–327FFFh
	SAI08	0110101XXX	32	328000h–32FFFFh
	SAI09	0110110XXX	32	330000h–337FFFh
	SAII0	0110111XXX	32	338000h–33FFFFh
	SAIII	0111I000XXX	32	340000h–347FFFh
	SAII2	0111I001XXX	32	348000h–34FFFFh
	SAII3	0111I010XXX	32	350000h–357FFFh
	SAII4	0111I011XXX	32	358000h–35FFFFh
	SAII5	0111I100XXX	32	360000h–367FFFh
	SAII6	0111I101XXX	32	368000h–36FFFFh
	SAII7	0111I110XXX	32	370000h–377FFFh
	SAII8	0111IIIIXXX	32	378000h–37FFFFh

Table 5. S29PLI27H Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-A12)	Sector Size (Kwords)	Address Range (x16)
Bank B	SAI19	011110000XXX	32	380000h–387FFFh
	SAI20	011110001XXX	32	388000h–38FFFFh
	SAI21	011110010XXX	32	390000h–397FFFh
	SAI22	011110011XXX	32	398000h–39FFFFh
	SAI23	011110100XXX	32	3A0000h–3A7FFFh
	SAI24	011110101XXX	32	3A8000h–3AFFFFh
	SAI25	011110110XXX	32	3B0000h–3B7FFFh
	SAI26	011110111XXX	32	3B8000h–3BFFFFh
	SAI27	011111000XXX	32	3C0000h–3C7FFFh
	SAI28	011111001XXX	32	3C8000h–3CFFFFh
	SAI29	011111010XXX	32	3D0000h–3D7FFFh
	SAI30	011111011XXX	32	3D8000h–3DFFFFh
	SAI31	011111100XXX	32	3E0000h–3E7FFFh
	SAI32	011111101XXX	32	3E8000h–3EFFFFh
	SAI33	011111110XXX	32	3F0000h–3F7FFFh
	SAI34	011111111XXX	32	3F8000h–3FFFFFh
Bank C	SAI35	100000000XXX	32	400000h–407FFFh
	SAI36	100000001XXX	32	408000h–40FFFFh
	SAI37	100000010XXX	32	410000h–417FFFh
	SAI38	100000011XXX	32	418000h–41FFFFh
	SAI39	100001000XXX	32	420000h–427FFFh
	SAI40	100001001XXX	32	428000h–42FFFFh
	SAI41	100001010XXX	32	430000h–437FFFh
	SAI42	100001011XXX	32	438000h–43FFFFh
	SAI43	100001000XXX	32	440000h–447FFFh
	SAI44	100001001XXX	32	448000h–44FFFFh
	SAI45	100001010XXX	32	450000h–457FFFh
	SAI46	100001011XXX	32	458000h–45FFFFh
	SAI47	100001100XXX	32	460000h–467FFFh
	SAI48	100001101XXX	32	468000h–46FFFFh
	SAI49	100001110XXX	32	470000h–477FFFh
	SAI50	100001111XXX	32	478000h–47FFFFh
	SAI51	100100000XXX	32	480000h–487FFFh
	SAI52	100100001XXX	32	488000h–48FFFFh
	SAI53	100100010XXX	32	490000h–497FFFh
	SAI54	100100011XXX	32	498000h–49FFFFh
	SAI55	100101000XXX	32	4A0000h–4A7FFFh
	SAI56	100101001XXX	32	4A8000h–4AFFFFh
	SAI57	100101110XXX	32	4B0000h–4B7FFFh
	SAI58	100101111XXX	32	4B8000h–4BFFFFh

Table 5. S29PLI27H Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-A12)	Sector Size (Kwords)	Address Range (x16)
Bank C	SAI59	100110000XXX	32	4C0000h–4C7FFFh
	SAI60	100110010XXX	32	4C8000h–4CFFFFh
	SAI61	100110100XXX	32	4D0000h–4D7FFFh
	SAI62	100110110XXX	32	4D8000h–4DFFFFh
	SAI63	100111000XXX	32	4E0000h–4E7FFFh
	SAI64	100111010XXX	32	4E8000h–4EFFFFh
	SAI65	100111100XXX	32	4F0000h–4F7FFFh
	SAI66	100111110XXX	32	4F8000h–4FFFFFh
	SAI67	101000000XXX	32	500000h–507FFFh
	SAI68	101000010XXX	32	508000h–50FFFFh
	SAI69	101000100XXX	32	510000h–517FFFh
	SAI70	101000110XXX	32	518000h–51FFFFh
	SAI71	101001000XXX	32	520000h–527FFFh
	SAI72	101001010XXX	32	528000h–52FFFFh
	SAI73	101001100XXX	32	530000h–537FFFh
	SAI74	101001110XXX	32	538000h–53FFFFh
	SAI75	101010000XXX	32	540000h–547FFFh
	SAI76	101010010XXX	32	548000h–54FFFFh
	SAI77	101010100XXX	32	550000h–557FFFh
	SAI78	101010110XXX	32	558000h–15FFFFh
	SAI79	101011000XXX	32	560000h–567FFFh
	SAI80	101011010XXX	32	568000h–56FFFFh
	SAI81	101011100XXX	32	570000h–577FFFh
	SAI82	101011110XXX	32	578000h–57FFFFh
	SAI83	101100000XXX	32	580000h–587FFFh
	SAI84	101100010XXX	32	588000h–58FFFFh
	SAI85	101100100XXX	32	590000h–597FFFh
	SAI86	101100110XXX	32	598000h–59FFFFh
	SAI87	101101000XXX	32	5A0000h–5A7FFFh
	SAI88	101101010XXX	32	5A8000h–5AFFFFh
	SAI89	101101100XXX	32	5B0000h–5B7FFFh
	SAI90	101101110XXX	32	5B8000h–5BFFFFh
	SAI91	101110000XXX	32	5C0000h–5C7FFFh
	SAI92	101110010XXX	32	5C8000h–5CFFFFh
	SAI93	101110100XXX	32	5D0000h–5D7FFFh
	SAI94	101110110XXX	32	5D8000h–5DFFFFh
	SAI95	101111000XXX	32	5E0000h–5E7FFFh
	SAI96	101111010XXX	32	5E8000h–5EFFFFh
	SAI97	101111100XXX	32	5F0000h–5F7FFFh
	SAI98	101111110XXX	32	5F8000h–5FFFFFh

Table 5. S29PLI27H Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank C	SAI99	II000000XXX	32	600000h–607FFFh
	SA200	II00000IXXX	32	608000h–60FFFFh
	SA20I	II0000I0XXX	32	610000h–617FFFh
	SA202	II0000IIXXX	32	618000h–61FFFFh
	SA203	II000I00XXX	32	620000h–627FFFh
	SA204	II000I0IXXX	32	628000h–62FFFFh
	SA205	II000II0XXX	32	630000h–637FFFh
	SA206	II000IIIXXX	32	638000h–63FFFFh
	SA207	II001000XXX	32	640000h–647FFFh
	SA208	II00I00IXXX	32	648000h–64FFFFh
	SA209	II00I0I0XXX	32	650000h–657FFFh
	SA2I0	II00I0IIXXX	32	658000h–65FFFFh
	SA2II	II00II00XXX	32	660000h–667FFFh
	SA2I2	II00II0IXXX	32	668000h–66FFFFh
	SA2I3	II00III0XXX	32	670000h–677FFFh
	SA2I4	II00IIIIXXX	32	678000h–67FFFFh
	SA2I5	II0I0000XXX	32	680000h–687FFFh
	SA2I6	II0I000IXXX	32	688000h–68FFFFh
	SA2I7	II0I00I0XXX	32	690000h–697FFFh
	SA2I8	II0I00IIXXX	32	698000h–69FFFFh
	SA2I9	II0I0I00XXX	32	6A0000h–6A7FFFh
	SA220	II0I0I0IXXX	32	6A8000h–6AFFFFh
	SA22I	II0I0II0XXX	32	6B0000h–6B7FFFh
	SA222	II0I0IIIXXX	32	6B8000h–6BFFFFh
	SA223	II0II000XXX	32	6C0000h–6C7FFFh
	SA224	II0II00IXXX	32	6C8000h–6CFFFFh
	SA225	II0II0I0XXX	32	6D0000h–6D7FFFh
	SA226	II0II0IIXXX	32	6D8000h–6DFFFFh
	SA227	II0III00XXX	32	6E0000h–6E7FFFh
	SA228	II0III0IXXX	32	6E8000h–6EFFFFh
	SA229	II0IIII0XXX	32	6F0000h–6F7FFFh
	SA230	II0IIIIIXXX	32	6F8000h–6FFFFFh

Table 5. S29PLI27H Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank D	SA23I	IIII00000XXX	32	700000h–707FFFh
	SA232	IIII0000IXXX	32	708000h–70FFFFh
	SA233	IIII0001OXXX	32	710000h–717FFFh
	SA234	IIII0001IXXX	32	718000h–71FFFFh
	SA235	IIII0010OXXX	32	720000h–727FFFh
	SA236	IIII0010IXXX	32	728000h–72FFFFh
	SA237	IIII0011OXXX	32	730000h–737FFFh
	SA238	IIII0011IXXX	32	738000h–73FFFFh
	SA239	IIII0100OXXX	32	740000h–747FFFh
	SA240	IIII0100IXXX	32	748000h–74FFFFh
	SA24I	IIII0101OXXX	32	750000h–757FFFh
	SA242	IIII0101IXXX	32	758000h–75FFFFh
	SA243	IIII0110OXXX	32	760000h–767FFFh
	SA244	IIII0110IXXX	32	768000h–76FFFFh
	SA245	IIII0111OXXX	32	770000h–777FFFh
	SA246	IIII0111IXXX	32	778000h–77FFFFh
	SA247	IIII1000OXXX	32	780000h–787FFFh
	SA248	IIII1000IXXX	32	788000h–78FFFFh
	SA249	IIII1001OXXX	32	790000h–797FFFh
	SA250	IIII1001IXXX	32	798000h–79FFFFh
	SA25I	IIII1010OXXX	32	7A0000h–7A7FFFh
	SA252	IIII1010IXXX	32	7A8000h–7AFFFFh
	SA253	IIII1011OXXX	32	7B0000h–7B7FFFh
	SA254	IIII1011IXXX	32	7B8000h–7BFFFFh
	SA255	IIII1100OXXX	32	7C0000h–7C7FFFh
	SA256	IIII1100IXXX	32	7C8000h–7CFFFFh
	SA257	IIII1101OXXX	32	7D0000h–7D7FFFh
	SA258	IIII1101IXXX	32	7D8000h–7DFFFFh
	SA259	IIIII1100XXX	32	7E0000h–7E7FFFh
	SA260	IIIII1101XXX	32	7E8000h–7EFFFFh
	SA26I	IIIIII1110XXX	32	7F0000h–7F7FFFh
	SA262	IIIIIIII000	4	7F8000h–7F8FFFh
	SA263	IIIIIIII001	4	7F9000h–7F9FFFh
	SA264	IIIIIIII010	4	7FA000h–7FAFFFh
	SA265	IIIIIIII011	4	7FB000h–7FBFFFh
	SA266	IIIIIIII100	4	7FC000h–7FCFFFh
	SA267	IIIIIIII101	4	7FD000h–7FDFFFh
	SA268	IIIIIIII110	4	7FE000h–7FEFFFh
	SA269	IIIIIIII111	4	7FF000h–7FFFFFh

Table 6. S29PLI29H Sector Architecture

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank IA	SAI-0	0	I	0000000XXX	32	000000h–007FFFh
	SAI-I	0	I	000000IXXX	32	008000h–00FFFFh
	SAI-2	0	I	00000I0XXX	32	0I0000h–0I7FFFh
	SAI-3	0	I	00000IIXXX	32	0I8000h–0IFFFFh
	SAI-4	0	I	0000I00XXX	32	020000h–027FFFh
	SAI-5	0	I	0000I0IXXX	32	028000h–02FFFFh
	SAI-6	0	I	0000II0XXX	32	030000h–037FFFh
	SAI-7	0	I	0000IIIXXX	32	038000h–03FFFFh
	SAI-8	0	I	000I000XXX	32	040000h–047FFFh
	SAI-9	0	I	000I00IXXX	32	048000h–04FFFFh
	SAI-I0	0	I	000I0I0XXX	32	050000h–057FFFh
	SAI-II	0	I	000I0IIXXX	32	058000h–05FFFFh
	SAI-I2	0	I	000II00XXX	32	060000h–067FFFh
	SAI-I3	0	I	000II0IXXX	32	068000h–06FFFFh
	SAI-I4	0	I	000III0XXX	32	070000h–077FFFh
	SAI-I5	0	I	000IIIIXXX	32	078000h–07FFFFh
	SAI-I6	0	I	00I0000XXX	32	080000h–087FFFh
	SAI-I7	0	I	00I000IXXX	32	088000h–08FFFFh
	SAI-I8	0	I	00I00I0XXX	32	090000h–097FFFh
	SAI-I9	0	I	00I00IIXXX	32	098000h–09FFFFh
	SAI-20	0	I	00I0I00XXX	32	0A0000h–0A7FFFh
	SAI-2I	0	I	00I0I0IXXX	32	0A8000h–0AFFFFh
	SAI-22	0	I	00I0II0XXX	32	0B0000h–0B7FFFh
	SAI-23	0	I	00I0IIIXXX	32	0B8000h–0BFFFFh
	SAI-24	0	I	00II000XXX	32	0C0000h–0C7FFFh
	SAI-25	0	I	00II00IXXX	32	0C8000h–0CFFFFh
	SAI-26	0	I	00II0I0XXX	32	0D0000h–0D7FFFh
	SAI-27	0	I	00II0IIXXX	32	0D8000h–0DFFFFh
	SAI-28	0	I	00III00XXX	32	0E0000h–0E7FFFh
	SAI-29	0	I	00III0IXXX	32	0E8000h–0EFFFFh
	SAI-30	0	I	00IIII0XXX	32	0F0000h–0F7FFFh
	SAI-3I	0	I	00IIIIIXXX	32	0F8000h–0FFFFFh
	SAI-32	0	I	0I00000XXX	32	I00000h–I07FFFh
	SAI-33	0	I	0I0000IXXX	32	I08000h–I0FFFFh
	SAI-34	0	I	0I000I0XXX	32	I10000h–I17FFFh
	SAI-35	0	I	0I000IIXXX	32	I18000h–I1FFFFh
	SAI-36	0	I	0I00I00XXX	32	I20000h–I27FFFh
	SAI-37	0	I	0I00I0IXXX	32	I28000h–I2FFFFh

Table 6. S29PLI29H Sector Architecture (Continued)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (x16)
Bank IA	SAI-38	0	I	0I00II0XXX	32	I30000h–I37FFFh
	SAI-39	0	I	0I00IIIXXX	32	I38000h–I3FFFFh
	SAI-40	0	I	0I0I000XXX	32	I40000h–I47FFFh
	SAI-4I	0	I	0I0I00IXXX	32	I48000h–I4FFFFh
	SAI-42	0	I	0I0I0I0XXX	32	I50000h–I57FFFh
	SAI-43	0	I	0I0I0IIXXX	32	I58000h–I5FFFFh
	SAI-44	0	I	0I0II00XXX	32	I60000h–I67FFFh
	SAI-45	0	I	0I0II0IXXX	32	I68000h–I6FFFFh
	SAI-46	0	I	0I0III0XXX	32	I70000h–I77FFFh
	SAI-47	0	I	0I0IIIIXXX	32	I78000h–I7FFFFh
	SAI-48	0	I	0II0000XXX	32	I80000h–I87FFFh
	SAI-49	0	I	0II000IXXX	32	I88000h–I8FFFFh
	SAI-50	0	I	0II00I0XXX	32	I90000h–I97FFFh
	SAI-5I	0	I	0II00IIXXX	32	I98000h–I9FFFFh
	SAI-52	0	I	0II0I00XXX	32	IA0000h–IA7FFFh
	SAI-53	0	I	0II0I0IXXX	32	IA8000h–IAFFFFh
	SAI-54	0	I	0II0II0XXX	32	IB0000h–IB7FFFh
	SAI-55	0	I	0II0IIIXXX	32	IB8000h–IBFFFFh
	SAI-56	0	I	0III000XXX	32	IC0000h–IC7FFFh
	SAI-57	0	I	0III00IXXX	32	IC8000h–ICFFFFh
	SAI-58	0	I	0III0I0XXX	32	ID0000h–ID7FFFh
	SAI-59	0	I	0III0IIXXX	32	ID8000h–IDFFFFh
	SAI-60	0	I	0IIII00XXX	32	IE0000h–IE7FFFh
	SAI-6I	0	I	0IIII0IXXX	32	IE8000h–IEFFFFh
	SAI-62	0	I	0IIIII0XXX	32	IF0000h–IF7FFFh
	SAI-63	0	I	0IIIIIIXXX	32	IF8000h–IFFFFFh
	SAI-64	0	I	I000000XXX	32	200000h–207FFFh
	SAI-65	0	I	I00000IXXX	32	208000h–20FFFFh
	SAI-66	0	I	I0000I0XXX	32	210000h–217FFFh
	SAI-67	0	I	I0000IIXXX	32	218000h–21FFFFh
	SAI-68	0	I	I000I00XXX	32	220000h–227FFFh
	SAI-69	0	I	I000I0IXXX	32	228000h–22FFFFh
	SAI-70	0	I	I000II0XXX	32	230000h–237FFFh
	SAI-7I	0	I	I000IIIXXX	32	238000h–23FFFFh
	SAI-72	0	I	I001000XXX	32	240000h–247FFFh
	SAI-73	0	I	I00I00IXXX	32	248000h–24FFFFh
	SAI-74	0	I	I00I0I0XXX	32	250000h–257FFFh
	SAI-75	0	I	I00I0IIXXX	32	258000h–25FFFFh
	SAI-76	0	I	I00II00XXX	32	260000h–267FFFh
	SAI-77	0	I	I00II0IXXX	32	268000h–26FFFFh

Table 6. S29PLI29H Sector Architecture (Continued)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (x16)
Bank IA	SAI-78	0	I	I00III0XXX	32	270000h–277FFFh
	SAI-79	0	I	I00IIIIXXX	32	278000h–27FFFFh
	SAI-80	0	I	I0I0000XXX	32	280000h–287FFFh
	SAI-8I	0	I	I0I000IXXX	32	288000h–28FFFFh
	SAI-82	0	I	I0I00I0XXX	32	290000h–297FFFh
	SAI-83	0	I	I0I00IIXXX	32	298000h–29FFFFh
	SAI-84	0	I	I0I0I00XXX	32	2A0000h–2A7FFFh
	SAI-85	0	I	I0I0I0IXXX	32	2A8000h–2AFFFFh
	SAI-86	0	I	I0I0II0XXX	32	2B0000h–2B7FFFh
	SAI-87	0	I	I0I0IIIXXX	32	2B8000h–2BFFFFh
	SAI-88	0	I	I0II000XXX	32	2C0000h–2C7FFFh
	SAI-89	0	I	I0II00IXXX	32	2C8000h–2CFFFFh
	SAI-90	0	I	I0II0I0XXX	32	2D0000h–2D7FFFh
	SAI-9I	0	I	I0II0IIXXX	32	2D8000h–2DFFFFh
	SAI-92	0	I	I0III00XXX	32	2E0000h–2E7FFFh
	SAI-93	0	I	I0III0IXXX	32	2E8000h–2EFFFFh
	SAI-94	0	I	I0IIII0XXX	32	2F0000h–2F7FFFh
	SAI-95	0	I	I0IIIIIXXX	32	2F8000h–2FFFFFh

Table 6. S29PLI29H Sector Architecture (Continued)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (x16)
Bank IB	SAI-96	0	I	II00000XXX	32	300000h–307FFFh
	SAI-97	0	I	II0000IXXX	32	308000h–30FFFFh
	SAI-98	0	I	II000I0XXX	32	310000h–317FFFh
	SAI-99	0	I	II000IIXXX	32	318000h–31FFFFh
	SAI-100	0	I	II00I00XXX	32	320000h–327FFFh
	SAI-101	0	I	II00I0IXXX	32	328000h–32FFFFh
	SAI-102	0	I	II00II0XXX	32	330000h–337FFFh
	SAI-103	0	I	II00IIIXXX	32	338000h–33FFFFh
	SAI-104	0	I	II0I000XXX	32	340000h–347FFFh
	SAI-105	0	I	II0I00IXXX	32	348000h–34FFFFh
	SAI-106	0	I	II0I0I0XXX	32	350000h–357FFFh
	SAI-107	0	I	II0I0IIXXX	32	358000h–35FFFFh
	SAI-108	0	I	II0II00XXX	32	360000h–367FFFh
	SAI-109	0	I	II0II0IXXX	32	368000h–36FFFFh
	SAI-110	0	I	II0III0XXX	32	370000h–377FFFh
	SAI-111	0	I	II0IIIIXXX	32	378000h–37FFFFh
	SAI-112	0	I	III0000XXX	32	380000h–387FFFh
	SAI-113	0	I	III000IXXX	32	388000h–38FFFFh
	SAI-114	0	I	III00I0XXX	32	390000h–397FFFh
	SAI-115	0	I	III00IIXXX	32	398000h–39FFFFh
	SAI-116	0	I	III0I00XXX	32	3A0000h–3A7FFFh
	SAI-117	0	I	III0I0IXXX	32	3A8000h–3AFFFFh
	SAI-118	0	I	III0II0XXX	32	3B0000h–3B7FFFh
	SAI-119	0	I	III0IIIXXX	32	3B8000h–3BFFFFh
	SAI-120	0	I	IIII000XXX	32	3C0000h–3C7FFFh
	SAI-121	0	I	IIII00IXXX	32	3C8000h–3CFFFFh
	SAI-122	0	I	IIII0I0XXX	32	3D0000h–3D7FFFh
	SAI-123	0	I	IIII0IIXXX	32	3D8000h–3DFFFFh
	SAI-124	0	I	IIIII00XXX	32	3E0000h–3E7FFFh
	SAI-125	0	I	IIIII0IXXX	32	3E8000h–3EFFFFh
	SAI-126	0	I	IIIIII0XXX	32	3F0000h–3F7FFFh
	SAI-127	0	I	IIIIIII000	4	3F8000h–3F8FFFh
	SAI-128	0	I	IIIIIII001	4	3F9000h–3F9FFFh
	SAI-129	0	I	IIIIIII0I0	4	3FA000h–3FAFFFh
	SAI-130	0	I	IIIIIII0II	4	3FB000h–3FBFFFh
	SAI-131	0	I	IIIIIIII00	4	3FC000h–3FCFFFh
	SAI-132	0	I	IIIIIIII0I	4	3FD000h–3FDFFFh
	SAI-133	0	I	IIIIIIII0	4	3FE000h–3FEFFFh
	SAI-134	0	I	IIIIIIIII	4	3FF000h–3FFFFFh

Table 6. S29PLI29H Sector Architecture (Continued)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (x16)
Bank 2A	SA2-0	I	0	0000000000	4	000000h–000FFFh
	SA2-1	I	0	0000000001	4	001000h–001FFFh
	SA2-2	I	0	0000000010	4	002000h–002FFFh
	SA2-3	I	0	0000000011	4	003000h–003FFFh
	SA2-4	I	0	0000000100	4	004000h–004FFFh
	SA2-5	I	0	0000000101	4	005000h–005FFFh
	SA2-6	I	0	0000000110	4	006000h–006FFFh
	SA2-7	I	0	0000000111	4	007000h–007FFFh
	SA2-8	I	0	000000IXXX	32	008000h–00FFFFh
	SA2-9	I	0	00000I0XXX	32	010000h–017FFFh
	SA2-10	I	0	00000IIXXX	32	018000h–01FFFFh
	SA2-11	I	0	0000I00XXX	32	020000h–027FFFh
	SA2-12	I	0	0000I0IXXX	32	028000h–02FFFFh
	SA2-13	I	0	0000II0XXX	32	030000h–037FFFh
	SA2-14	I	0	0000IIIXXX	32	038000h–03FFFFh
	SA2-15	I	0	000I000XXX	32	040000h–047FFFh
	SA2-16	I	0	000I00IXXX	32	048000h–04FFFFh
	SA2-17	I	0	000I0I0XXX	32	050000h–057FFFh
	SA2-18	I	0	000I0IIXXX	32	058000h–05FFFFh
	SA2-19	I	0	000II00XXX	32	060000h–067FFFh
	SA2-20	I	0	000II0IXXX	32	068000h–06FFFFh
	SA2-21	I	0	000III0XXX	32	070000h–077FFFh
	SA2-22	I	0	000IIIIXXX	32	078000h–07FFFFh
	SA2-23	I	0	00I0000XXX	32	080000h–087FFFh
	SA2-24	I	0	00I000IXXX	32	088000h–08FFFFh
	SA2-25	I	0	00I00I0XXX	32	090000h–097FFFh
	SA2-26	I	0	00I00IIXXX	32	098000h–09FFFFh
	SA2-27	I	0	00I0I00XXX	32	0A0000h–0A7FFFh
	SA2-28	I	0	00I0I0IXXX	32	0A8000h–0AFFFFh
	SA2-29	I	0	00I0II0XXX	32	0B0000h–0B7FFFh
	SA2-30	I	0	00I0IIIXXX	32	0B8000h–0BFFFFh
	SA2-31	I	0	00II000XXX	32	0C0000h–0C7FFFh
	SA2-32	I	0	00II00IXXX	32	0C8000h–0CFFFFh
	SA2-33	I	0	00II0I0XXX	32	0D0000h–0D7FFFh
	SA2-34	I	0	00II0IIXXX	32	0D8000h–0DFFFFh
	SA2-35	I	0	00III00XXX	32	0E0000h–0E7FFFh
	SA2-36	I	0	00III0IXXX	32	0E8000h–0EFFFFh
	SA2-37	I	0	00IIII0XXX	32	0F0000h–0F7FFFh
	SA2-38	I	0	00IIIIIXXX	32	0F8000h–0FFFFFh

Table 6. S29PLI29H Sector Architecture (Continued)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (x16)
Bank 2B	SA2-39	I	0	0I00000XXX	32	I00000h–I07FFFh
	SA2-40	I	0	0I0000IXXX	32	I08000h–I0FFFFh
	SA2-41	I	0	0I000I0XXX	32	I10000h–I17FFFh
	SA2-42	I	0	0I000IIXXX	32	I18000h–IIFFFFh
	SA2-43	I	0	0I00I00XXX	32	I20000h–I27FFFh
	SA2-44	I	0	0I00I0IXXX	32	I28000h–I2FFFFh
	SA2-45	I	0	0I00II0XXX	32	I30000h–I37FFFh
	SA2-46	I	0	0I00IIIXXX	32	I38000h–I3FFFFh
	SA2-47	I	0	0I0I000XXX	32	I40000h–I47FFFh
	SA2-48	I	0	0I0I00IXXX	32	I48000h–I4FFFFh
	SA2-49	I	0	0I0I0I0XXX	32	I50000h–I57FFFh
	SA2-50	I	0	0I0I0IIXXX	32	I58000h–I5FFFFh
	SA2-51	I	0	0I0II00XXX	32	I60000h–I67FFFh
	SA2-52	I	0	0I0II0IXXX	32	I68000h–I6FFFFh
	SA2-53	I	0	0I0III0XXX	32	I70000h–I77FFFh
	SA2-54	I	0	0I0IIIIXXX	32	I78000h–I7FFFFh
	SA2-55	I	0	0II0000XXX	32	I80000h–I87FFFh
	SA2-56	I	0	0II000IXXX	32	I88000h–I8FFFFh
	SA2-57	I	0	0II00I0XXX	32	I90000h–I97FFFh
	SA2-58	I	0	0II00IIXXX	32	I98000h–I9FFFFh
	SA2-59	I	0	0II0I00XXX	32	IA0000h–IA7FFFh
	SA2-60	I	0	0II0I0IXXX	32	IA8000h–IAFFFFh
	SA2-61	I	0	0II0II0XXX	32	IB0000h–IB7FFFh
	SA2-62	I	0	0II0IIIXXX	32	IB8000h–IBFFFFh
	SA2-63	I	0	0III000XXX	32	IC0000h–IC7FFFh
	SA2-64	I	0	0III00IXXX	32	IC8000h–ICFFFFh
	SA2-65	I	0	0III0I0XXX	32	ID0000h–ID7FFFh
	SA2-66	I	0	0III0IIXXX	32	ID8000h–IDFFFFh
	SA2-67	I	0	0IIII00XXX	32	IE0000h–IE7FFFh
	SA2-68	I	0	0IIII0IXXX	32	IE8000h–IEFFFFh
	SA2-69	I	0	0IIIII0XXX	32	IF0000h–IF7FFFh
	SA2-70	I	0	0IIIIIIXXX	32	IF8000h–IFFFFFh
	SA2-71	I	0	I000000XXX	32	200000h–207FFFh
	SA2-72	I	0	I00000IXXX	32	208000h–20FFFFh
	SA2-73	I	0	I0000I0XXX	32	210000h–217FFFh
	SA2-74	I	0	I0000IIXXX	32	218000h–21FFFFh
	SA2-75	I	0	I000I00XXX	32	220000h–227FFFh
	SA2-76	I	0	I000I0IXXX	32	228000h–22FFFFh
	SA2-77	I	0	I000II0XXX	32	230000h–237FFFh
	SA2-78	I	0	I000IIIXXX	32	238000h–23FFFFh

Table 6. S29PLI29H Sector Architecture (Continued)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank 2B	SA2-79	I	0	I001000XXX	32	240000h–247FFFh
	SA2-80	I	0	I001001XXX	32	248000h–24FFFFh
	SA2-81	I	0	I001010XXX	32	250000h–257FFFh
	SA2-82	I	0	I001011XXX	32	258000h–25FFFFh
	SA2-83	I	0	I001100XXX	32	260000h–267FFFh
	SA2-84	I	0	I001101XXX	32	268000h–26FFFFh
	SA2-85	I	0	I001110XXX	32	270000h–277FFFh
	SA2-86	I	0	I001111XXX	32	278000h–27FFFFh
	SA2-87	I	0	I010000XXX	32	280000h–287FFFh
	SA2-88	I	0	I010001XXX	32	288000h–28FFFFh
	SA2-89	I	0	I010010XXX	32	290000h–297FFFh
	SA2-90	I	0	I010011XXX	32	298000h–29FFFFh
	SA2-91	I	0	I010100XXX	32	2A0000h–2A7FFFh
	SA2-92	I	0	I010101XXX	32	2A8000h–2AFFFFh
	SA2-93	I	0	I010110XXX	32	2B0000h–2B7FFFh
	SA2-94	I	0	I010111XXX	32	2B8000h–2BFFFFh
	SA2-95	I	0	I011000XXX	32	2C0000h–2C7FFFh
	SA2-96	I	0	I011001XXX	32	2C8000h–2CFFFFh
	SA2-97	I	0	I011010XXX	32	2D0000h–2D7FFFh
	SA2-98	I	0	I011011XXX	32	2D8000h–2DFFFFh
	SA2-99	I	0	I011100XXX	32	2E0000h–2E7FFFh
	SA2-I00	I	0	I011101XXX	32	2E8000h–2EFFFFh
	SA2-I01	I	0	I011110XXX	32	2F0000h–2F7FFFh
	SA2-I02	I	0	I011111XXX	32	2F8000h–2FFFFFh
	SA2-I03	I	0	I100000XXX	32	300000h–307FFFh
	SA2-I04	I	0	I100001XXX	32	308000h–30FFFFh
	SA2-I05	I	0	I100010XXX	32	310000h–317FFFh
	SA2-I06	I	0	I100011XXX	32	318000h–31FFFFh
	SA2-I07	I	0	I100100XXX	32	320000h–327FFFh
	SA2-I08	I	0	I100101XXX	32	328000h–32FFFFh
	SA2-I09	I	0	I100110XXX	32	330000h–337FFFh
	SA2-I10	I	0	I100111XXX	32	338000h–33FFFFh
	SA2-I11	I	0	I101000XXX	32	340000h–347FFFh
	SA2-I12	I	0	I101001XXX	32	348000h–34FFFFh
	SA2-I13	I	0	I101010XXX	32	350000h–357FFFh
	SA2-I14	I	0	I101011XXX	32	358000h–35FFFFh
	SA2-I15	I	0	I101100XXX	32	360000h–367FFFh
	SA2-I16	I	0	I101101XXX	32	368000h–36FFFFh
	SA2-I17	I	0	I101110XXX	32	370000h–377FFFh
	SA2-I18	I	0	I101111XXX	32	378000h–37FFFFh

Table 6. S29PLI29H Sector Architecture (Continued)

Bank	Sector	CEI#	CE2#	Sector Address (A2I-AI2)	Sector Size (Kwords)	Address Range (x16)
Bank 2B	SA2-II9	I	0	III0000XXX	32	380000h–387FFFh
	SA2-I20	I	0	III000IXXX	32	388000h–38FFFFh
	SA2-I2I	I	0	III00I0XXX	32	390000h–397FFFh
	SA2-I22	I	0	III00IIXXX	32	398000h–39FFFFh
	SA2-I23	I	0	III0I00XXX	32	3A0000h–3A7FFFh
	SA2-I24	I	0	III0I0IXXX	32	3A8000h–3AFFFFh
	SA2-I25	I	0	III0II0XXX	32	3B0000h–3B7FFFh
	SA2-I26	I	0	III0IIIXXX	32	3B8000h–3BFFFFh
	SA2-I27	I	0	IIII000XXX	32	3C0000h–3C7FFFh
	SA2-I28	I	0	IIII00IXXX	32	3C8000h–3CFFFFh
	SA2-I29	I	0	IIII0I0XXX	32	3D0000h–3D7FFFh
	SA2-I30	I	0	IIII0IIXXX	32	3D8000h–3DFFFFh
	SA2-I3I	I	0	IIIII00XXX	32	3E0000h–3E7FFFh
	SA2-I32	I	0	IIIII0IXXX	32	3E8000h–3EFFFFh
	SA2-I33	I	0	IIIIII0XXX	32	3F0000h–3F7FFFh
	SA2-I34	I	0	IIIIIIIXXX	32	3F8000h–3FFFFFh

Table 7. SecSi™ Sector Addresses

	Sector Size	Address Range
S29PLI27H/S29PLI29H	I28 words	000000h–00007Fh
Factory-Locked Area	64 words	000000h-00003Fh
Customer-Lockable Area	64 words	000040h-00007Fh

Table 8. S29PLI27H Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A22-AI2	Sector/ Sector Block Size
SA0	00000000000	4 Kwords
SA1	00000000001	4 Kwords
SA2	00000000010	4 Kwords
SA3	00000000011	4 Kwords
SA4	00000000100	4 Kwords
SA5	00000000101	4 Kwords
SA6	00000000110	4 Kwords
SA7	00000000111	4 Kwords
SA8-SA10	00000001XXX 00000010XXX 00000011XXX	96 (3x32) Kwords
SA11-SA14	00001XXXXX	128 (4x32) Kwords
SA15-SA18	00010XXXXX	128 (4x32) Kwords
SA19-SA22	00011XXXXX	128 (4x32) Kwords
SA23-SA26	00100XXXXX	128 (4x32) Kwords
SA27-SA30	00101XXXXX	128 (4x32) Kwords
SA31-SA34	00110XXXXX	128 (4x32) Kwords
SA35-SA38	00111XXXXX	128 (4x32) Kwords
SA39-SA42	01000XXXXX	128 (4x32) Kwords
SA43-SA46	01001XXXXX	128 (4x32) Kwords
SA47-SA50	01010XXXXX	128 (4x32) Kwords
SA51-SA54	01011XXXXX	128 (4x32) Kwords
SA55-SA58	01100XXXXX	128 (4x32) Kwords
SA59-SA62	01101XXXXX	128 (4x32) Kwords
SA63-SA66	01110XXXXX	128 (4x32) Kwords
SA67-SA70	01111XXXXX	128 (4x32) Kwords
SA71-SA74	10000XXXXX	128 (4x32) Kwords
SA75-SA78	10001XXXXX	128 (4x32) Kwords
SA79-SA82	10010XXXXX	128 (4x32) Kwords
SA83-SA86	10011XXXXX	128 (4x32) Kwords
SA87-SA90	10100XXXXX	128 (4x32) Kwords
SA91-SA94	10101XXXXX	128 (4x32) Kwords
SA95-SA98	10110XXXXX	128 (4x32) Kwords
SA99-SA102	10111XXXXX	128 (4x32) Kwords
SA103-SA106	11000XXXXX	128 (4x32) Kwords
SA107-SA110	11001XXXXX	128 (4x32) Kwords
SA111-SA114	11010XXXXX	128 (4x32) Kwords
SA115-SA118	11011XXXXX	128 (4x32) Kwords
SA119-SA122	11100XXXXX	128 (4x32) Kwords
SA123-SA126	11101XXXXX	128 (4x32) Kwords
SA127-SA130	11110XXXXX	128 (4x32) Kwords

Sector	A22-AI2	Sector/ Sector Block Size
SA131-SA134	11111XXXXX	128 (4x32) Kwords
SA135-SA138	100000XXXXX	128 (4x32) Kwords
SA139-SA142	100001XXXXX	128 (4x32) Kwords
SA143-SA146	100010XXXXX	128 (4x32) Kwords
SA147-SA150	100011XXXXX	128 (4x32) Kwords
SA151-SA154	100100XXXXX	128 (4x32) Kwords
SA155-SA158	100101XXXXX	128 (4x32) Kwords
SA159-SA162	100110XXXXX	128 (4x32) Kwords
SA163-SA166	100111XXXXX	128 (4x32) Kwords
SA167-SA170	101000XXXXX	128 (4x32) Kwords
SA171-SA174	101001XXXXX	128 (4x32) Kwords
SA175-SA178	101010XXXXX	128 (4x32) Kwords
SA179-SA182	101011XXXXX	128 (4x32) Kwords
SA183-SA186	101100XXXXX	128 (4x32) Kwords
SA187-SA190	101101XXXXX	128 (4x32) Kwords
SA191-SA194	101110XXXXX	128 (4x32) Kwords
SA195-SA198	101111XXXXX	128 (4x32) Kwords
SA199-SA202	110000XXXXX	128 (4x32) Kwords
SA203-SA206	110001XXXXX	128 (4x32) Kwords
SA207-SA210	110010XXXXX	128 (4x32) Kwords
SA211-SA214	110011XXXXX	128 (4x32) Kwords
SA215-SA218	110100XXXXX	128 (4x32) Kwords
SA219-SA222	110101XXXXX	128 (4x32) Kwords
SA223-SA226	110110XXXXX	128 (4x32) Kwords
SA227-SA230	110111XXXXX	128 (4x32) Kwords
SA231-SA234	111000XXXXX	128 (4x32) Kwords
SA235-SA238	111001XXXXX	128 (4x32) Kwords
SA239-SA242	111010XXXXX	128 (4x32) Kwords
SA243-SA246	111011XXXXX	128 (4x32) Kwords
SA247-SA250	111100XXXXX	128 (4x32) Kwords
SA251-SA254	111101XXXXX	128 (4x32) Kwords
SA255-SA258	111110XXXXX	128 (4x32) Kwords
SA259-SA261	111111100XXX 111111101XXX 111111110XXX	96 (3x32) Kwords
SA262	111111111000	4 Kwords
SA263	111111111001	4 Kwords
SA264	111111111010	4 Kwords
SA265	111111111011	4 Kwords
SA266	111111111100	4 Kwords
SA267	111111111101	4 Kwords
SA268	111111111110	4 Kwords
SA269	111111111111	4 Kwords

Table 9. S29PLI29H Boot Sector/Sector Block Addresses for Protection/Unprotection CEI# Control

Sector Group	A2I-I2	Sector/Sector Block Size
SAI-0–SAI-3	00000XXXXX	I28 (4x32) Kwords
SAI-4–SAI-7	0000IXXXXX	I28 (4x32) Kwords
SAI-8–SAI-II	000I0XXXXX	I28 (4x32) Kwords
SAI-I2–SAI-I5	000IIXXXXX	I28 (4x32) Kwords
SAI-I6–SAI-I9	00I00XXXXX	I28 (4x32) Kwords
SAI-20–SAI-23	00I0IXXXXX	I28 (4x32) Kwords
SAI-24–SAI-27	00II0XXXXX	I28 (4x32) Kwords
SAI-28–SAI-3I	00IIIXXXXX	I28 (4x32) Kwords
SAI-32–SAI-35	0I000XXXXX	I28 (4x32) Kwords
SAI-36–SAI-39	0I00IXXXXX	I28 (4x32) Kwords
SAI-40–SAI-43	0I0I0XXXXX	I28 (4x32) Kwords
SAI-44–SAI-47	0I0IIXXXXX	I28 (4x32) Kwords
SAI-48–SAI-5I	0II00XXXXX	I28 (4x32) Kwords
SAI-52–SAI-55	0II0IXXXXX	I28 (4x32) Kwords
SAI-56–SAI-59	0III0XXXXX	I28 (4x32) Kwords
SAI-60–SAI-63	0IIIIXXXXX	I28 (4x32) Kwords
SAI-64–SAI-67	I0000XXXXX	I28 (4x32) Kwords
SAI-68–SAI-7I	I000IXXXXX	I28 (4x32) Kwords
SAI-72–SAI-75	I00I0XXXXX	I28 (4x32) Kwords
SAI-76–SAI-79	I00IIXXXXX	I28 (4x32) Kwords
SAI-80–SAI-83	I0I00XXXXX	I28 (4x32) Kwords
SAI-84–SAI-87	I0I0IXXXXX	I28 (4x32) Kwords
SAI-88–SAI-9I	I0II0XXXXX	I28 (4x32) Kwords
SAI-92–SAI-95	I0IIIXXXXX	I28 (4x32) Kwords
SAI-96–SAI-99	II000XXXXX	I28 (4x32) Kwords
SAI-I00–SAI-I03	II00IXXXXX	I28 (4x32) Kwords
SAI-I04–SAI-I07	II0I0XXXXX	I28 (4x32) Kwords
SAI-I08–SAI-III	II0IIXXXXX	I28 (4x32) Kwords
SAI-II2–SAI-II5	III00XXXXX	I28 (4x32) Kwords
SAI-II6–SAI-II9	III0IXXXXX	I28 (4x32) Kwords
SAI-I20–SAI-I23	IIII0XXXXX	I28 (4x32) Kwords
SAI-I24	IIII00XXX	32 Kwords
SAI-I25	IIII0IXXX	32 Kwords
SAI-I26	IIII0XXX	32 Kwords
SAI-I27	IIIIII000	4 Kwords
SAI-I28	IIIIII001	4 Kwords
SAI-I29	IIIIII0I0	4 Kwords
SAI-I30	IIIIII0II	4 Kwords
SAI-I3I	IIIIIII00	4 Kwords
SAI-I32	IIIIIII0I	4 Kwords
SAI-I33	IIIIIII0	4 Kwords
SAI-I34	IIIIIIIII	4 Kwords

Table I0. S29PLI29H Boot Sector/Sector Block Addresses for Protection/Unprotection CE2# Control

Sector Group	A2I-I2	Sector/Sector Block Size
SA2-0	0000000000	4 Kwords
SA2-I	0000000001	4 Kwords
SA2-2	0000000010	4 Kwords
SA2-3	0000000011	4 Kwords
SA2-4	0000000100	4 Kwords
SA2-5	0000000101	4 Kwords
SA2-6	0000000110	4 Kwords
SA2-7	0000000111	4 Kwords
SA2-8	000000IXXX	32 Kwords
SA2-9	00000I0XXX	32 Kwords
SA2-I0	00000IIXXX	32 Kwords
SA2-II - SA2-I4	0000IXXXXX	I28 (4x32) Kwords
SA2-I5 - SA2-I8	000I0XXXXX	I28 (4x32) Kwords
SA2-I9 - SA2-22	000IIXXXXX	I28 (4x32) Kwords
SA2-23 - SA2-26	00I00XXXXX	I28 (4x32) Kwords
SA2-27 - SA2-30	00I0IXXXXX	I28 (4x32) Kwords
SA2-3I - SA2-34	00II0XXXXX	I28 (4x32) Kwords
SA2-35 - SA2-38	00IIIXXXXX	I28 (4x32) Kwords
SA2-39 - SA2-42	0I000XXXXX	I28 (4x32) Kwords
SA2-43 - SA2-46	0I00IXXXXX	I28 (4x32) Kwords
SA2-47 - SA2-50	0I0I0XXXXX	I28 (4x32) Kwords
SA2-5I - SA2-54	0I0IIXXXXX	I28 (4x32) Kwords
SA2-55 - SA2-58	0II00XXXXX	I28 (4x32) Kwords
SA2-59 - SA2-62	0II0IXXXXX	I28 (4x32) Kwords
SA2-63 - SA2-66	0III0XXXXX	I28 (4x32) Kwords
SA2-67 - SA2-70	0IIIIXXXXX	I28 (4x32) Kwords
SA2-7I - SA2-74	I0000XXXXX	I28 (4x32) Kwords
SA2-75 - SA2-78	I000IXXXXX	I28 (4x32) Kwords
SA2-79 - SA2-82	I00I0XXXXX	I28 (4x32) Kwords
SA2-83 - SA2-86	I00IIXXXXX	I28 (4x32) Kwords
SA2-87 - SA2-90	I0I00XXXXX	I28 (4x32) Kwords
SA2-9I - SA2-94	I0I0IXXXXX	I28 (4x32) Kwords
SA2-95 - SA2-98	I0II0XXXXX	I28 (4x32) Kwords
SA2-99 - SA2-I02	I0IIIXXXXX	I28 (4x32) Kwords
SA2-I03 - SA2-I06	II000XXXXX	I28 (4x32) Kwords
SA2-I07 - SA2-II0	II00IXXXXX	I28 (4x32) Kwords
SA2-III - SA2-II4	II0I0XXXXX	I28 (4x32) Kwords
SA2-II5 - SA2-II8	II0IIXXXXX	I28 (4x32) Kwords
SA2-II9 - SA2-I22	III00XXXXX	I28 (4x32) Kwords
SA2-I23 - SA2-I26	III0IXXXXX	I28 (4x32) Kwords
SA2-I27 - SA2-I30	IIII0XXXXX	I28 (4x32) Kwords
SA2-I3I - SA2-I34	IIIIIXXXXX	I28 (4x32) Kwords

Sector Protection

The S29PL127H/S29PL129H features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase operations in sectors 0, 1, 268, and 269 (S29PL127H); or sectors SA1-133, SA1-134, SA2-0, SA2-1 (S29PL129H).

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the Persistent Sector Protection method is desired, programming the **Persistent Sector Protection Mode Locking Bit** permanently sets the device to the Persistent Sector Protection mode. If the Password Sector Protection method is desired, programming the **Password Mode Locking Bit** permanently sets the device to the Password Sector Protection mode. It is not possible to switch between the two protection modes once a locking bit has been set. **One of the two modes must be selected when the device is first programmed.** This prevents a program or virus from later setting the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. Optional Spansion programming services enable and protecting sectors at the factory prior to shipping the device. Contact the local sales office for details.

It is possible to determine whether a sector is protected or unprotected.

Persistent Sector Protection

The Persistent Sector Protection method replaces the 12 V controlled protection method in previous AMD flash devices. This new method provides three different sector protection states:

- **Persistently Locked**—The sector is protected and cannot be changed.
- **Dynamically Locked**—The sector is protected and can be changed by a simple command.
- **Unlocked**—The sector is unprotected and can be changed by a simple command.

To achieve these states, three types of "bits" are used:

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings).

All 4 Kword boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the **PPB Write Command**.

The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to preprogram all of the sector PPBs prior to PPB erasure. Otherwise, a previously erased sector PPBs can potentially be over-erased. **The flash device does not have a built-in means of preventing sector PPBs over-erasure**.

Persistent Protection Bit Lock (PPB Lock)

The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to "1", the PPBs cannot be changed. When cleared ("0"), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is "0". Each DYB is individually modifiable through the DYB Write Command.

When the parts are first shipped, the PPBs are cleared, the DYBs are cleared, and PPB Lock is defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on the DYBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPBs cleared, the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Write command sequences, the DYBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called **Dynamic Locked or Unlocked** states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are non-volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to "1". Setting the PPB Lock disables all program and erase commands to the non-volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed; for example, to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP#/ACC write protect pin adds a final level of hardware protection to sectors 0, 1, 268, and 269 (S29PL127H); SA1-133, SA1-134, SA2-0, and SA2-1 (S29PL129H). When this pin is low it is not possible to change the contents of these sectors. These sectors generally hold system boot code. The WP#/ACC pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected.

If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic sectors switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

The best protection is achieved by executing the PPB lock bit set command early in the boot code, and protect the boot code by holding WP#/ACC = V_{IL}.

Table II. Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DYB are changeable
0	0	I	Unprotected—PPB not changeable, DYB is changeable
0	I	0	Protected—PPB and DYB are changeable
I	0	0	
I	I	0	
0	I	I	Protected—PPB not changeable, DYB is changeable
I	0	I	
I	I	I	

Table 11 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DYB, PPB, and PPB lock for a given sector can be verified by writing a DYB/PPB/PPB lock verify command to the device.

Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences

between the Persistent Sector Protection and the Password Sector Protection Mode:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the **locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2 μs delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. The password may be correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

1. Permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.

2. Disables *all further commands* to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see "Password Verify Command"). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting sectors 0, 1, 268, and 269 (S29PL127H); SA1-133, SA1-134, SA2-0, and SA2-1 (S29PL129H). without using V_{ID}. This function is provided by the WP# pin and overrides the previously discussed High Voltage Sector Protection method.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword sectors on both ends of the flash array independent of whether it was previously protected or unprotected.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether sectors 0, 1, 268, and 269 were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in High Voltage Sector Protection.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1" when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (V_{ID}) to be placed on the RESET# pin. Refer to Figure 1 for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

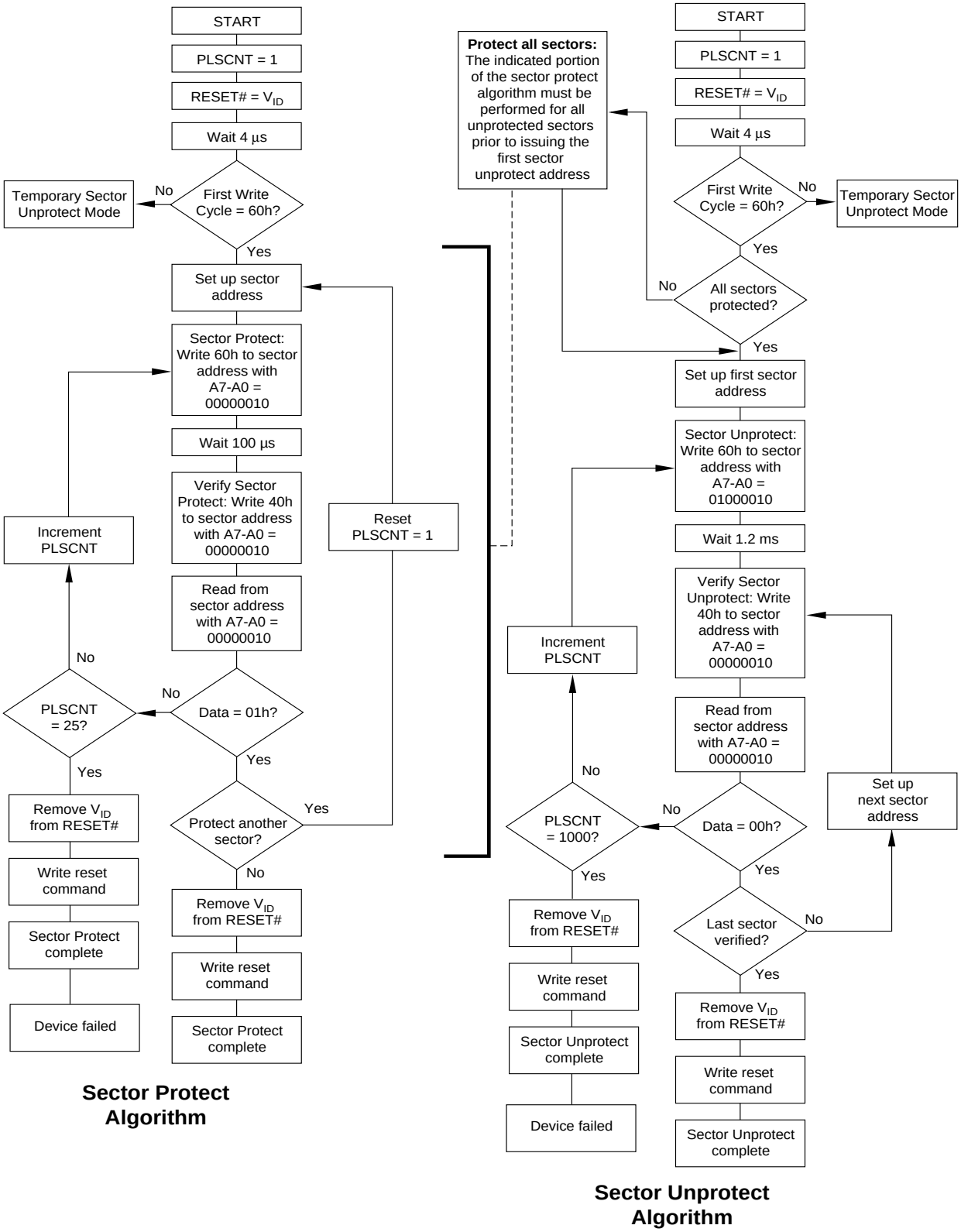
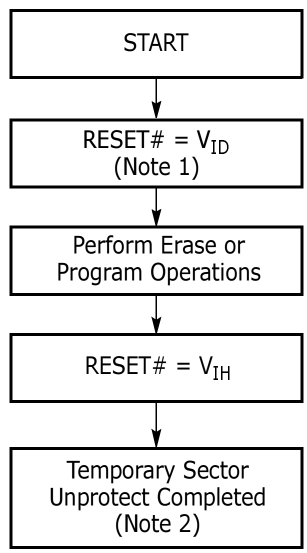


Figure I. In-System Sector Protection/ Sector Unprotection Algorithms

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 2 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature. While PPB lock is set, the device cannot enter the Temporary Sector Unprotection Mode.



Notes:

1. *All protected sectors unprotected If WP#/ACC = V_{IL}, sectors 0, 1, 268, 269 will remain protected (S29PL127H), or sectors SA1-133, SA1-134, SA2-0, SA2-1 (S29PL129H).*
2. *All previously protected sectors are protected once again.*

Figure 2. Temporary Sector Unprotect Operation

SecSi™ (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN) The 128-word SecSi sector is divided into 64 factory-lockable words that can be programmed and locked by the customer. The SecSi sector is located at addresses 000000h-00007Fh in both Persistent Protection mode and Password Protection mode. It uses indicator bits (DQ6, DQ7) to indicate the factory-locked and customer-locked status of the part.

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi™ Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following

a hardware reset, the device reverts to sending commands to the normal address space. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Factory-Locked Area (64 words)

The factory-locked area of the SecSi Sector (000000h-00003Fh) is locked when the part is shipped, whether or not the area was programmed at the factory. The SecSi Sector Factory-locked Indicator Bit (DQ7) is permanently set to a "1". Optional Spansion programming services can program the factory-locked area with a random ESN, a customer-defined code, or any combination of the two. Because only the factory can program and protect the factory-locked area, this method ensures the security of the ESN once the product is shipped to the field. Contact the local sales office for details on using Spansion programming services.

Customer-Lockable Area (64 words)

The customer-lockable area of the SecSi Sector (000040h-00007Fh) is shipped unprotected, which allows the customer to program and optionally lock the area as appropriate for the application. The SecSi Sector Customer-locked Indicator Bit (DQ6) is shipped as "0" and can be permanently locked to "1" by issuing the SecSi Protection Bit Program Command. The SecSi Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the SecSi Sector.

The Customer-lockable SecSi Sector area can be protected using one of the following procedures:

- Follow the SecSi Sector protection Agorithm as shown in Figure 3. This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.

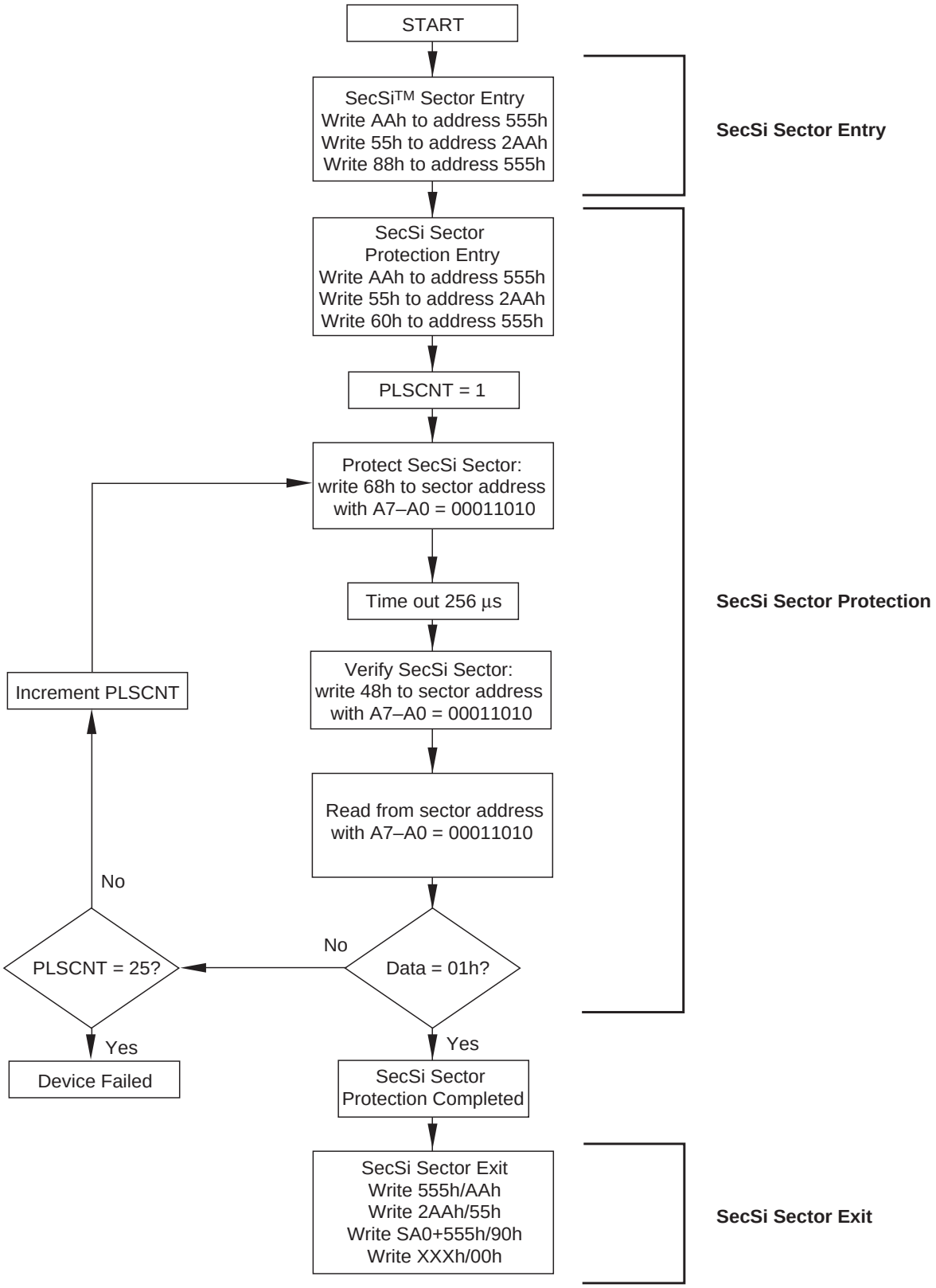


Figure 3. SecSi Sector Protection Algorithm

- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 4.

Once the SecSi Sector is locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing the remainder of the array.

The SecSi Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

SecSi Sector Protection Bits

The SecSi Sector Protection Bits prevent programming of the SecSi Sector memory area. Once set, the SecSi Sector memory area contents are non-modifiable.

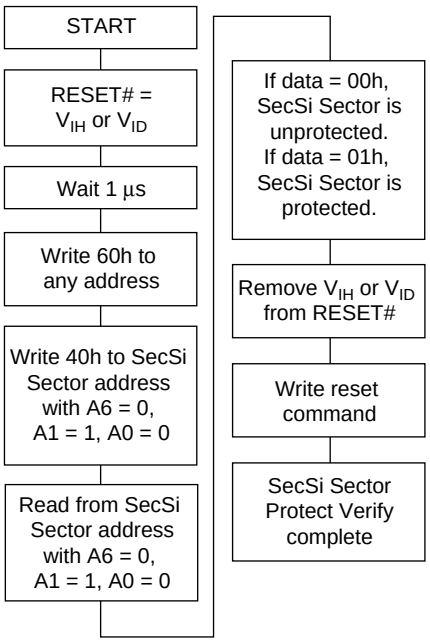


Figure 4. SecSi Sector Protect Verify

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on OE#, CE#, or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 12–15. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 12–15. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, at http://www.amd.com/flash/cfi. Contact your local sales office for copies of these documents.

Table I2. CFI Query Identification String

Addresses	Data	Description
I0h I1h I2h	005Ih 0052h 0059h	Query Unique ASCII string "QRY"
I3h I4h	0002h 0000h	Primary OEM Command Set
I5h I6h	0040h 0000h	Address for Primary Extended Table
I7h I8h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
I9h IAh	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table I3. System Interface String

Addresses	Data	Description
IBh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: I00 millivolt
ICh	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: I00 millivolt
IDh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
IEh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
IFh	0004h	Typical timeout per single byte/word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
2Ih	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table I4. Device Geometry Definition

Addresses	Data	Description
27h	00I8h	Device Size = 2^N byte
28h 29h	000Ih 0000h	Flash Device Interface description (refer to CFI publication I00)
2Ah 2Bh	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region I Information (refer to the CFI specification or CFI publication I00)
3Ih 32h 33h 34h	00FDh 0000h 0000h 000Ih	Erase Block Region 2 Information (refer to the CFI specification or CFI publication I00)
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication I00)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication I00)

Table 15. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string "PRI"
43h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	000Ch	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0007h	Sector Protect/Unprotect scheme 01 =29F040 mode, 02 = 29F016 mode, 03 = 29F400, 04 = 29LV800 mode
4Ah	00E7h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors excluding Bank 1
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 00h = Uniform device, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Both Top and Bottom
50h	0001h	Program Suspend 0 = Not supported, 1 = Supported
57h	0004h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks
58h	0027h	Bank 1 Region Information X = Number of Sectors in Bank 1
59h	0060h	Bank 2 Region Information X = Number of Sectors in Bank 2
5Ah	0060h	Bank 3 Region Information X = Number of Sectors in Bank 3
5Bh	0027h	Bank 4 Region Information X = Number of Sectors in Bank 4

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 16 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The AC Characteristics table provides the read parameters, and Figure 12 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 16 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA). Table 4 shows the address range and bank number associated with each sector.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter SecSi™ Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. The SecSi Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 16 shows the address and data requirements for both command sequences. See also "SecSi™ (Secured Silicon) Sector Flash Memory Region" for further information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 16 shows the address and data requirements for the program command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may

cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

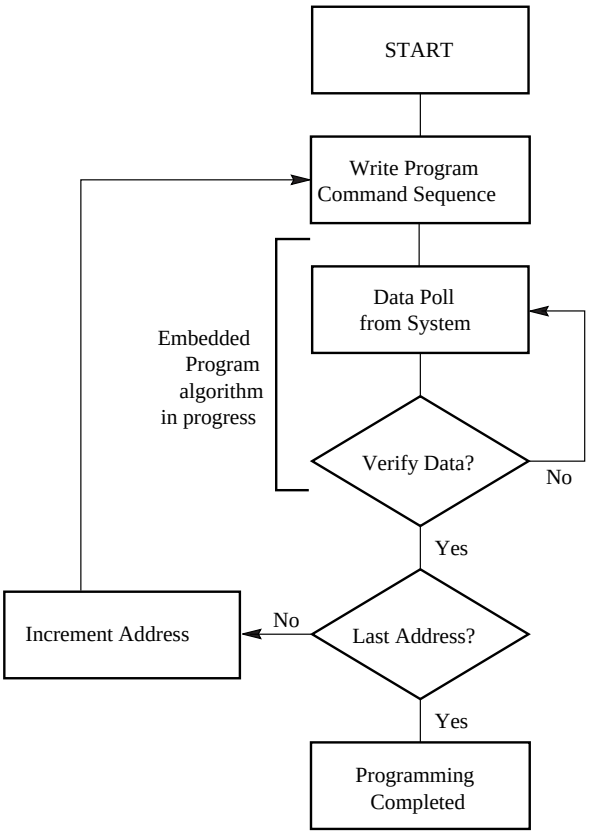
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program data to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 16 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. (See Table 14)

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the WP#/ACC pin must not be at V_{HH} any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

Figure 5 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 for timing diagrams.



Note: See Table 16 for program command sequence.

Figure 5. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 16 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. *Note that SecSi Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.* However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command.Table 16 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

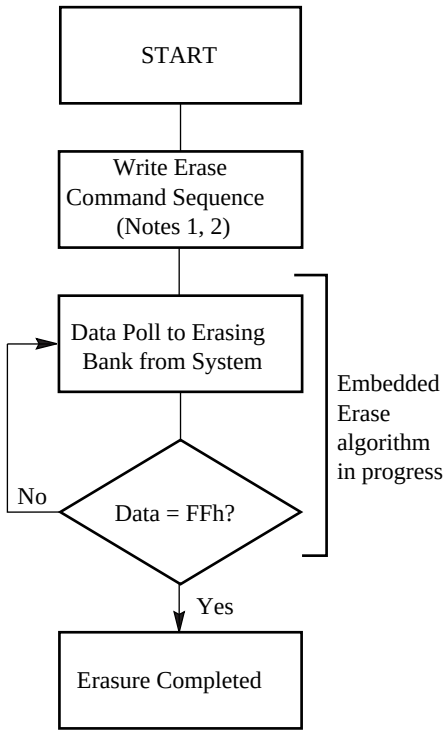
After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** The system must rewrite the command sequence and any additional addresses and commands. *Note that SecSi Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.



Notes:

1. *See Table 16 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 6. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 80 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase suspend command.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2

together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Word Program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to the Autoselect Command Sequence section for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don't care). The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. Four Password Program commands are required to program the password. The system must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a "0". The password is all ones when shipped from the factory. All 64-bit password combinations are valid as a password.

Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F's onto the DQ data bus.

The Password Verify command is permitted if the SecSi sector is enabled. Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A1-A0) are valid during the Password Verify. Writing the Read/Reset command returns the device back to normal operation.

Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. Once programmed, the Password Protection Mode Locking Bit cannot be erased! If the Password Protection Mode Locking Bit is verified as pro-

gram without margin, the Password Protection Mode Locking Bit Program command can be executed to improve the program margin. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. Exiting the Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. *If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin.* By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

SecSi Sector Protection Bit Program Command

The SecSi Sector Protection Bit Program Command programs the SecSi Sector Protection Bit, which prevents the SecSi sector memory from being cleared. *If the SecSi Sector Protection Bit is verified as programmed without margin, the SecSi Sector Protection Bit Program Command should be reissued to improve program margin.* Exiting the V_{CC}-level SecSi Sector Protection Bit Program Command is accomplished by writing the Read/Reset command.

PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched into the DYBs. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the Read/Reset command (only in the Persistent Protection Mode).

DYB Write Command

The DYB Write command is used to set or clear a DYB for a given sector. The high order address bits (Amax–A12) are issued at the same time as the code 01h or 00h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are cleared at power-up or hardware reset.Exiting the DYB Write command is accomplished by writing the Read/Reset command.

Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

Once the Password Unlock command is entered, the RY/BY# indicates that the device is busy. Approximately 1 µs is required for each portion of the unlock. Once the first portion of the password unlock completes (RY/BY# is not low or DQ6 does not toggle when read), the next part of the password is written. The system must thus monitor RY/BY# or the status bits to confirm when to write the next portion of the password. Seven cycles are required to successfully clear the PPB Lock Bit.

PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (Amax–A12) are written at the same time as the program command 60h with A6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

The PPB Program command does not follow the Embedded Program algorithm.

All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased without margin, the erase command should be reissued to improve the program margin.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

DYB Write Command

The DYB Write command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

PPB Lock Bit Set Command

The PPB Lock Bit set command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

PPB Status Command

The programming of the PPB for a given sector can be verified by writing a PPB status verify command to the device.

PPB Lock Bit Status Command

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device.

Sector Protection Status Command

The programming of either the PPB or DYB for a given sector or sector group can be verified by writing a Sector Protection Status command to the device.

Note that there is no single command to independently verify the programming of a DYB for a given sector group.

Command Definitions Tables

Table 16. Memory Array Command Definitions

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)		1	RA	RD										
Reset (6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	(BA)X00	01				
	Device ID (10)	6	555	AA	2AA	55	555	90	(BA)X01	7E	(BA)X0E	20	(BA)X0F	00
	SecSi Sector Factory Protect (8)	4	555	AA	2AA	55	555	90	X03	(see note 8)				
	Sector Group Protect Verify (9)	4	555	AAA	2AA	55	555	90	(SA)X02	XX00/ XX01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (11)		1	BA	B0										
Program/Erase Resume (12)		1	BA	30										
CFI Query (13)		1	55	98										
Accelerated Program (14)		2	XX	A0	PA	PD								
Unlock Bypass Entry (14)		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (14)		2	XX	A0	PA	PD								
Unlock Bypass Erase (14)		2	XX	80	XX	10								
Unlock Bypass CFI (13, 14)		1	XX	98										
Unlock Bypass Reset (14)		2	XXX	90	XXX	00								

Legend:

BA = Address of bank switching to autoselect mode, bypass mode, or erase operation. Determined by Amax:A20, see Tables 4 and 3 for more detail.

PA = Program Address (Amax:A0). Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

RA = Read Address (Amax:A0).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (Amax:A12) for verifying (in autoselect mode) or erasing.

WD = Write Data. See "Configuration Register" definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when bank is reading array data.*
6. *The Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).*
7. *Fourth cycle of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Autoselect Command Sequence section for more information.*
8. *The data is C0h for factory and customer locked and 80h for factory locked.*
9. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
10. *Device ID must be read across cycles 4, 5, and 6.*
11. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/Erase Suspend command is valid only during a sector erase operation, and requires bank address.*
12. *Program/Erase Resume command is valid only during Erase Suspend mode, and requires bank address.*
13. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
14. *Unlock Bypass Entry command is required prior to any Unlock Bypass operation. Unlock Bypass Reset command is required to return to the reading array.*

Command Definitions Tables

Table 17. Sector Protection Command Definitions

Command (Notes)	Cycles	Bus Cycles (Notes 1-4)													
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0												
SecSi Sector Entry	3	555	AA	2AA	55	555	88								
SecSi Sector Exit	4	555	AA	2AA	55	555	90	XX	00						
SecSi Protection Bit Program (5, 6)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD(0)		
SecSi Protection Bit Status	5	555	AA	2AA	55	555	60	OW	48	OW	RD(0)				
Password Program (5, 7, 8)	4	555	AA	2AA	55	555	38	XX[0-3]	PD[0-3]						
Password Verify (6, 8, 9)	4	555	AA	2AA	55	555	C8	PWA[0-3]	PWD[0-3]						
Password Unlock (7, 10, 11)	7	555	AA	2AA	55	555	28	PWA[0]	PWD[0]	PWA[1]	PWD[1]	PWA[2]	PWD[2]	PWA[3]	PWD[3]
PPB Program (5, 6, 12)	6	555	AA	2AA	55	555	60	(SA)WP	68	(SA)WP	48	(SA)WP	RD(0)		
PPB Status	4	555	AA	2AA	55	555	90	(SA)WP	RD(0)						
All PPB Erase (5, 6, 13, 14)	6	555	AA	2AA	55	555	60	WP	60	(SA)	40	(SA)WP	RD(0)		
PPB Lock Bit Set	3	555	AA	2AA	55	555	78								
PPB Lock Bit Status (15)	4	555	AA	2AA	55	555	58	SA	RD(1)						
DYB Write (7)	4	555	AA	2AA	55	555	48	SA	XI						
DYB Erase (7)	4	555	AA	2AA	55	555	48	SA	X0						
DYB Status (6)	4	555	AA	2AA	55	555	58	SA	48						
PPMLB Program (5, 6, 12)	6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD(0)		
PPMLB Status (5)	5	555	AA	2AA	55	555	60	PL	48	PL	RD(0)				
SPMLB Program (5, 6, 12)	6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD(0)		
SPMLB Status (5)	5	555	AA	2AA	55	555	60	SL	48	SL	RD(0)				

Legend:

DYB = Dynamic Protection Bit

OW = Address (A7:A0) is (00011010)

PD[3:0] = Password Data (1 of 4 portions)

PPB = Persistent Protection Bit

PWA = Password Address. A1:A0 selects portion of password.

PWD = Password Data being verified.

PL = Password Protection Mode Lock Address (A7:A0) is (00001010)

RD(0) = Read Data DQ0 for protection indicator bit.

RD(1) = Read Data DQ1 for PPB Lock status.

SA = Sector Address where security command applies. Address bits Amax:A12 uniquely select any sector.

SL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)

WP = PPB Address (A7:A0) is (00000010) (Note16)

X = Don't care

PPMLB = Password Protection Mode Locking Bit

SPMLB = Persistent Protection Mode Locking Bit

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *The reset command returns device to reading array.*
6. *Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.*
7. *Data is latched on the rising edge of WE#.*
8. *Entire command sequence must be entered for each portion of password.*
9. *Command sequence returns FFh if PPMLB is set.*
10. *The password is written over four consecutive cycles, at addresses 0-3.*
11. *A 2 µs timeout is required between any two portions of password.*
12. *A 100 µs timeout is required between cycles 4 and 5.*
13. *A 1.2 ms timeout is required between cycles 4 and 5.*
14. *Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 18 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

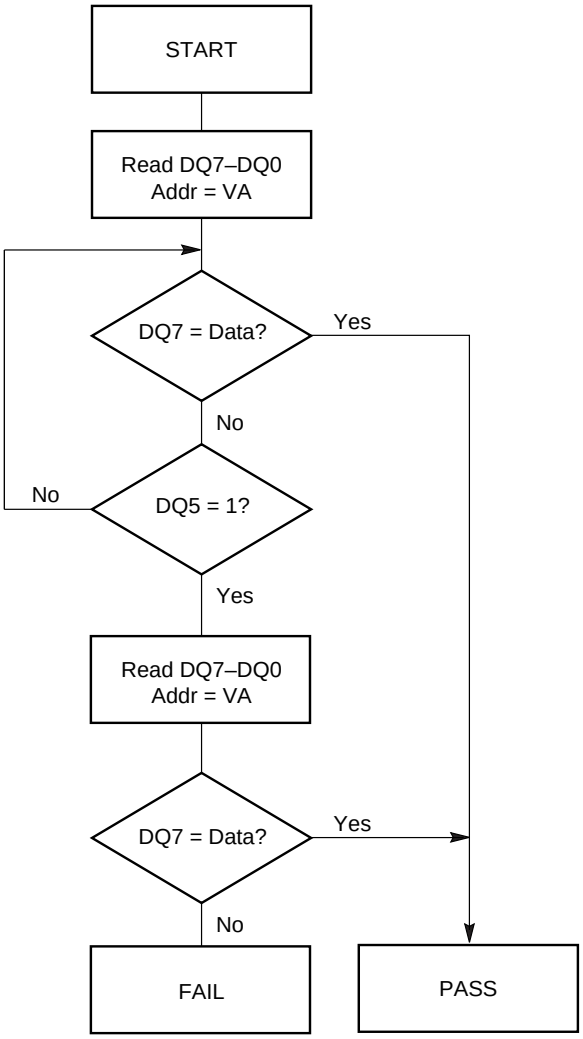
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 400 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 will appear on successive read cycles.

Table 18 shows the outputs for Data# Polling on DQ7. Figure 7 shows the Data# Polling algorithm. Figure 20 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 7. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 18 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 400 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 18 shows the outputs for Toggle Bit I on DQ6. Figure 8 shows the toggle bit algorithm. Figure 21 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

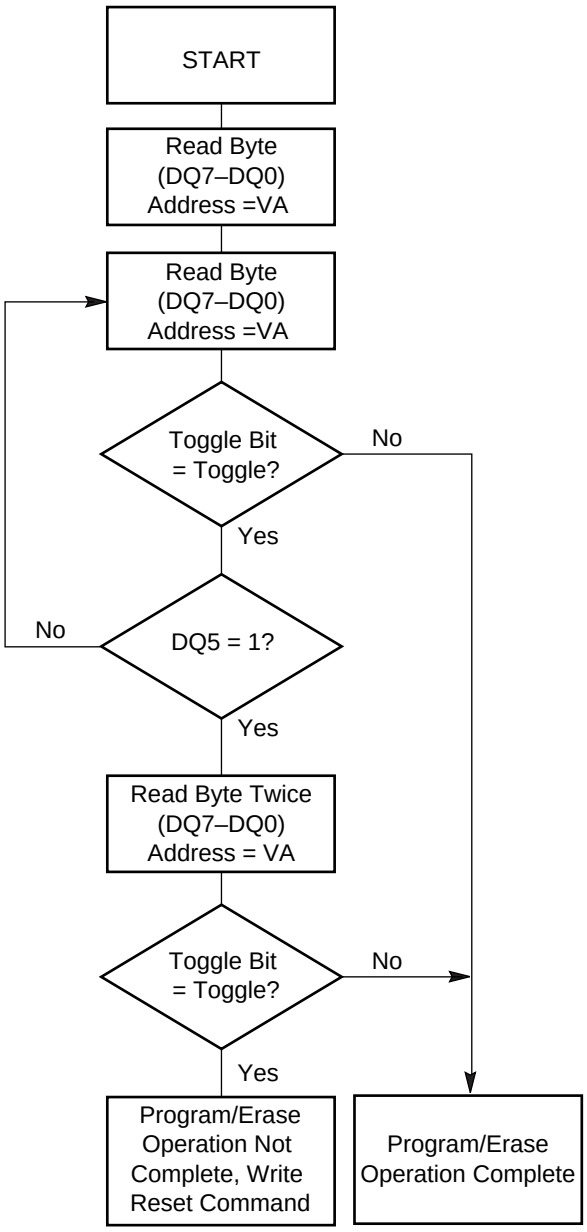
DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively

erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 18 to compare outputs for DQ2 and DQ6.

Figure 8 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 21 shows the toggle bit timing diagram. Figure 22 shows the differences between DQ2 and DQ6 in graphical form.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 8. Toggle Bit Algorithm

Reading Toggle Bits DQ6/DQ2

Refer to Figure 8 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle

bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 8).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 18 shows the status of DQ3 relative to the other status bits.

Table 18. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages. . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

OE# and RESET# (Note 2) . . . . . –0.5 V to +13.0 V

WP#/ACC (Note 2). . . . . –0.5 V to +10.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3). . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 9. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 10.*
2. *Minimum DC input voltage on pins OE#, RESET#, and WP#/ACC is –0.5 V. During voltage transitions, OE#, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pin OE#, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

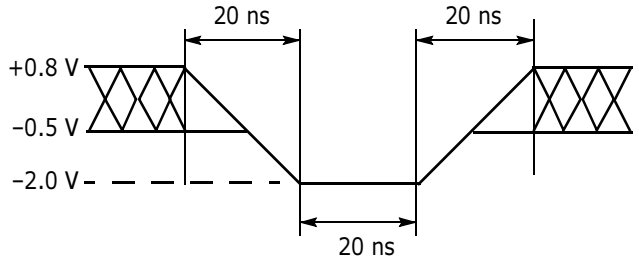


Figure 9. Maximum Negative Overshoot Waveform

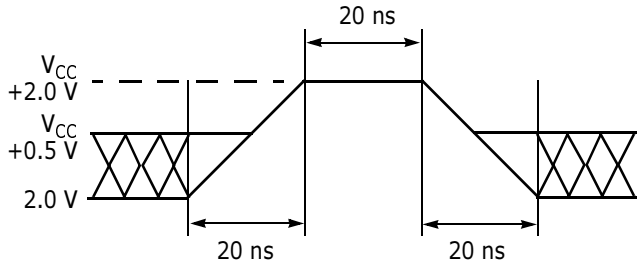


Figure 10. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) –40°C to +85°C

Supply Voltages

V_{CC} . . . . . 2.7–3.6 V

V_{IO} (see Note) . . . . . 1.65–1.95 V or 2.7–3.6 V

Note: For all AC and DC specifications, V_{IO} = V_{CC}; contact the local sales office for other V_{IO} options.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

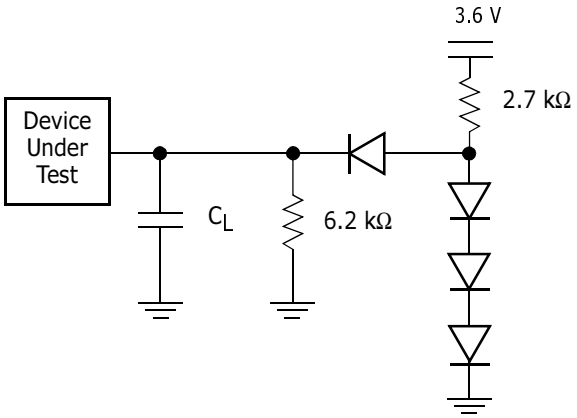
CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\,max}$				±1.0	µA
I_{LIT}	OE#, RESET# Input Load Current	$V_{CC} = V_{CC\,max}$; V_{ID}= 12.5 V				35	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\,max}$; V_{ID}= 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, OE# = V_{IH} $V_{CC} = V_{CC\,max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	OE# = V_{IH}, $V_{CC} = V_{CC\,max}$ (Note 1)	5 MHz		20	30	mA
			10 MHz		45	55	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3)	OE# = V_{IH}, WE# = V_{IL}			15	25	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, CE2#, RESET#, WP/ACC# = $V_{IO} \pm 0.3$ V			1	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = $V_{SS} \pm 0.3$ V			1	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH} = V_{IO} \pm 0.3$ V; $V_{IL} = V_{SS} \pm 0.3$ V			1	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current (Notes 1, 2)	OE# = V_{IH}			21	45	mA
I_{CC7}	V_{CC} Active Read-While-Erase Current (Notes 1, 2)	OE# = V_{IH}			21	45	mA
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current (Notes 2, 5)	OE# = V_{IH}			17	25	mA
V_{IL}	Input Low Voltage	V_{IO} = 1.65–1.95 V		–0.4		0.4	V
		V_{IO} = 2.7–3.6 V		–0.5		0.8	V
V_{IH}	Input High Voltage	V_{IO} = 1.65–1.95 V		V_{IO}–0.4		V_{IO}+0.4	V
		V_{IO} = 2.7–3.6 V		2.0		V_{CC}+0.3	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 3.0 V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\,min}$, V_{IO} = 1.65–1.95 V				0.1	V
		I_{OL} = 2.0 mA, $V_{CC} = V_{CC\,min}$, V_{IO} = 2.7–3.6 V				0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\,min}$, V_{IO} = 1.65–1.95 V		V_{IO}–0.1			V
		I_{OH} = –2.0 mA, $V_{CC} = V_{CC\,min}$, V_{IO} = 2.7–3.6 V		2.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 5)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 5 mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 150 ns. Typical sleep mode current is 1 mA.*
5. *Not 100% tested.*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 11. Test Setup

Table 19. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

Note: *For 70 pF output load capacitance, 2 ns will be added to certain read-only operation parameters.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

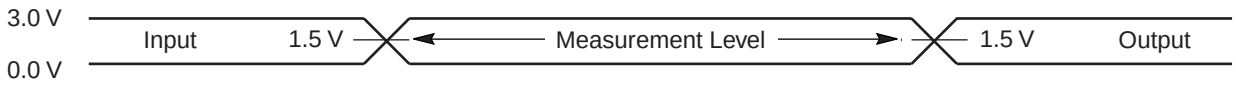


Figure 12. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read-Only Operations – S29PLI27H

Parameter		Description		Test Setup		All Speeds	Unit
JEDEC	Std.						
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CEI#, OE# = V_{IL}	Max	70	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	ns
	t_{PACC}	Page Access Time			Max	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1, 3)			Max	16	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 3)			Max	16	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CEI# or OE#, Whichever Occurs First (Notes 3)			Min	5	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0	ns
			Toggle and Data# Polling		Min	10	ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 19 for test specifications*
3. *Measurements performed by placing a 50 ohm termination on the data pin with a bias of $V_{CC}/2$. The time from OE# high to the data bus driven to $V_{CC}/2$ is taken as t_{DF}.*

Read-Only Operations –S29PLI29H

Parameter		Description		Test Setup		All Speeds	Unit
JEDEC	Std.						
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay (Note 3)		CEI#, OE# = V_{IL}	Max	70	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay (Note 4)		OE# = V_{IL}	Max	70	ns
	t_{PACC}	Page Access Time			Max	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1, 5, 6)			Max	16	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 5)			Max	16	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CEI#/CE2# or OE#, Whichever Occurs First (Notes 5, 6)			Min	5	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0	ns
			Toggle and Data# Polling		Min	10	ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 19 for test specifications*
3. *Valid CE1#/CE2# conditions: (CE1# = V_{IL}, CE2# = V_{IH}) or (CE1# = V_{IH}, CE2# = V_{IL}).*
4. *Valid CE1#/CE2# transitions: (CE1# = CE2# = V_{IH}) to (CE1# = V_{IL}, CE2# = V_{IH}) or (CE1# = V_{IH}, CE2# = V_{IL}).*
5. *Measurements performed by placing a 50 ohm termination on the data pin with a bias of $V_{CC}/2$. The time from OE# high to the data bus driven to $V_{CC}/2$ is taken as t_{DF}.*
6. *Valid CE1#/CE2# transitions: (CE1# = V_{IL}, CE2# = V_{IH}) or (CE1# = V_{IH}, CE2# = V_{IL}) to (CE1# = CE2# = V_{IH}).*

AC CHARACTERISTICS

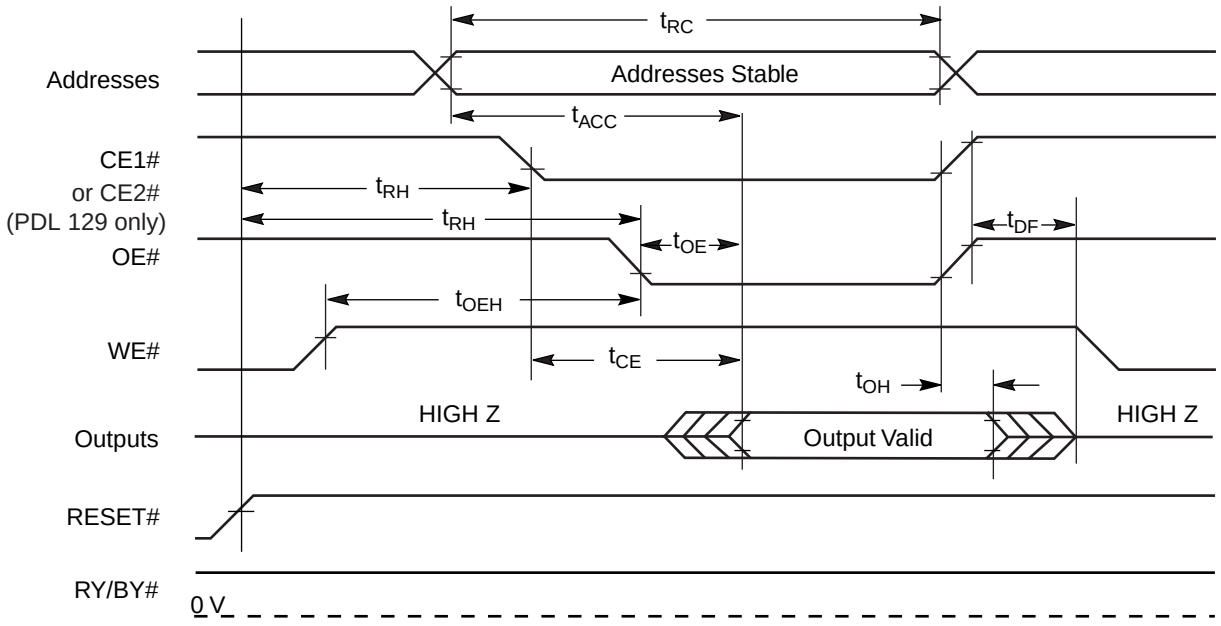


Figure I3. Read Operation Timings

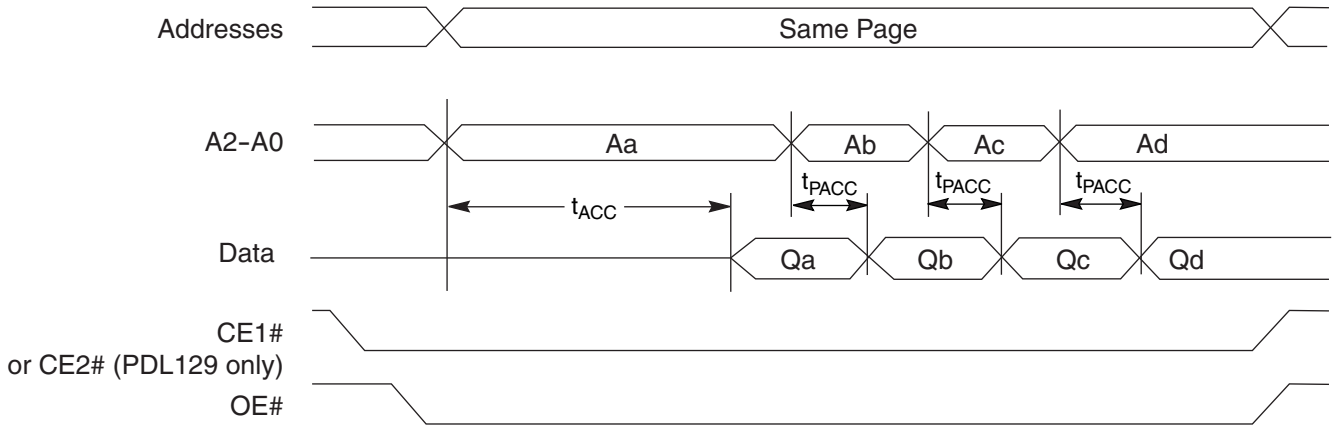


Figure I4. Page Read Operation Timings

Notes: *During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}*

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

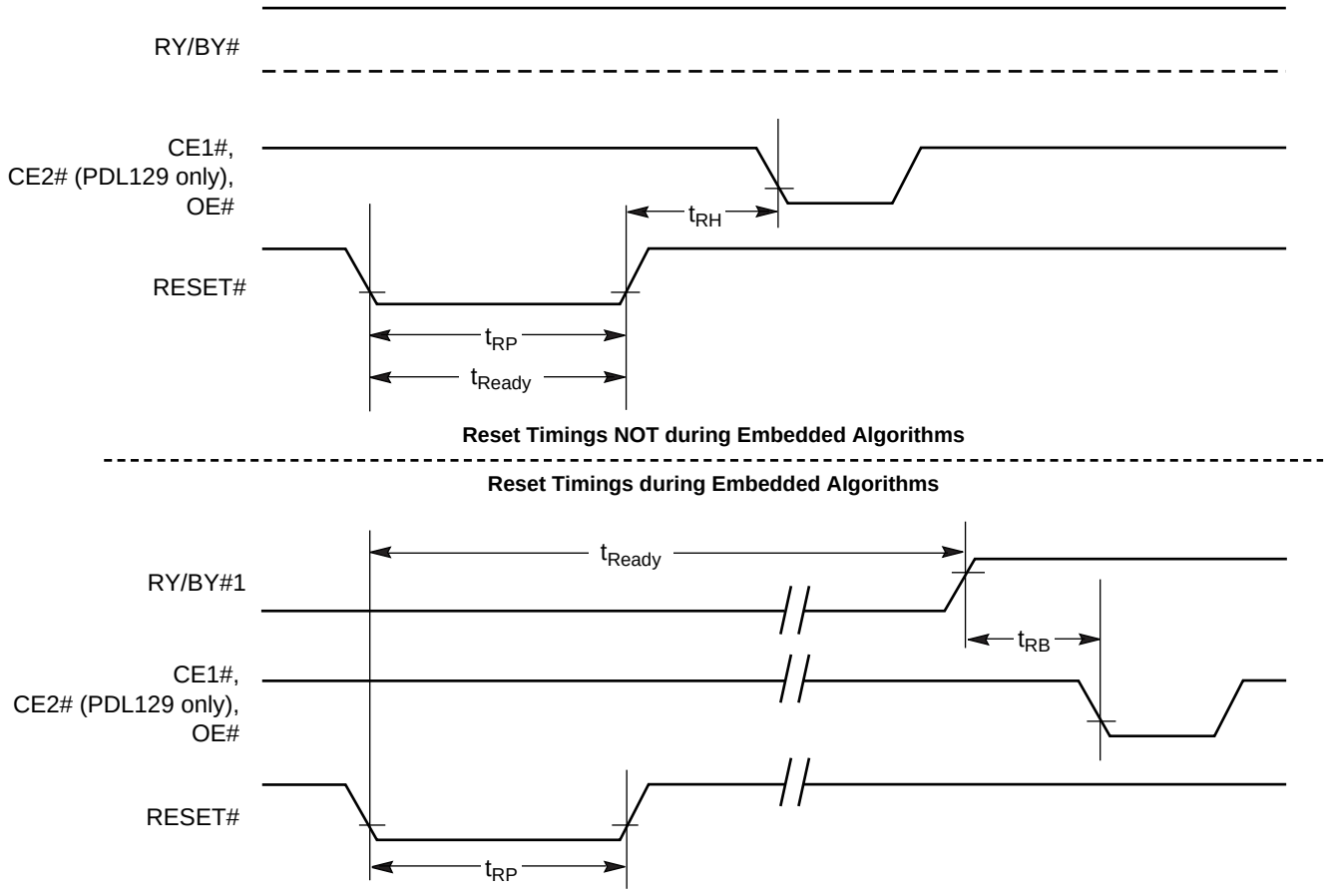


Figure 15. Reset Timings

AC CHARACTERISTICS

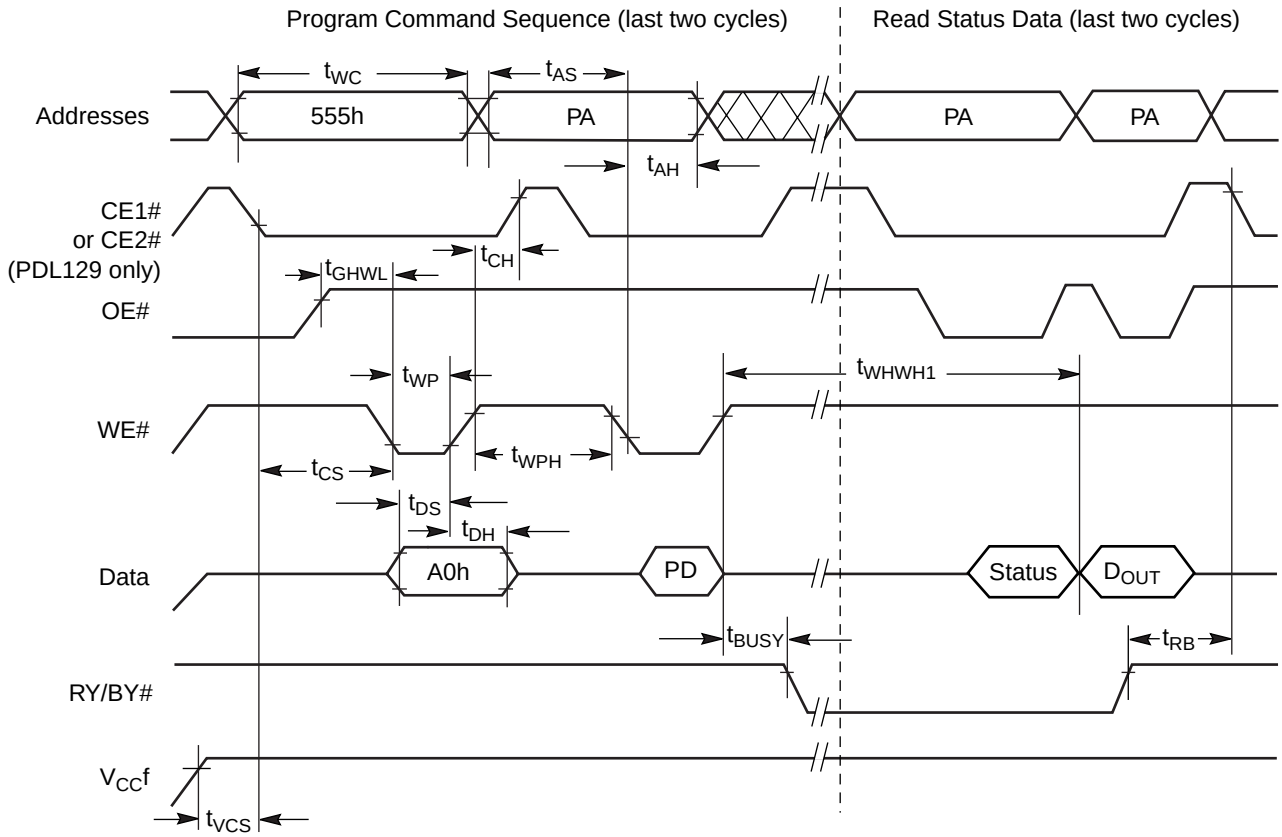
Erase and Program Operations

Parameter		Description			All Speeds	Unit
JEDEC	Std					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	ns
	t_{AHT}	Address Hold Time From CEI#f or OE# high during toggle bit polling		Min	0	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	30	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time (CEI# to WE#)		Min	0	ns
t_{ELWL}	t_{CS}	CEI# Setup Time		Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time (CEI# to WE#)		Min	0	ns
t_{WHEH}	t_{CH}	CEI# Hold Time		Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	40	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	25	ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0	ns
t_{WHWHI}	t_{WHWHI}	Programming Operation (Note 2)	Word	Typ	6	µs
t_{WHWHI}	t_{WHWHI}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	4	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5	sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50	µs
	t_{RB}	Write Recovery Time from RY/BY#		Min	0	ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Max	90	ns

Notes:

1. *Not 100% tested.*
2. *See the "Flash Erase And Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*
3. *For PL129H during CE1# transitions the other CE1# pin = V_{IH}.*

Figure 16. Program Operation Timings

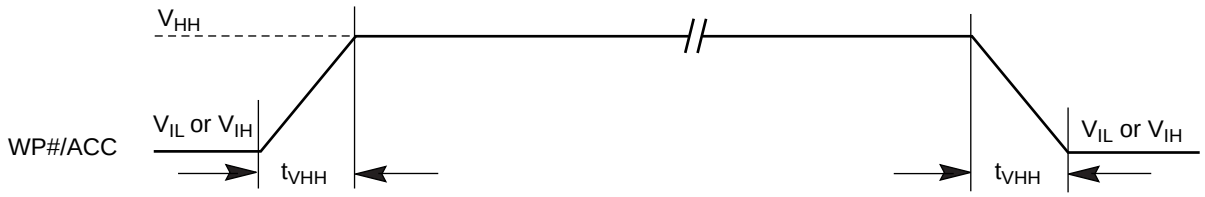
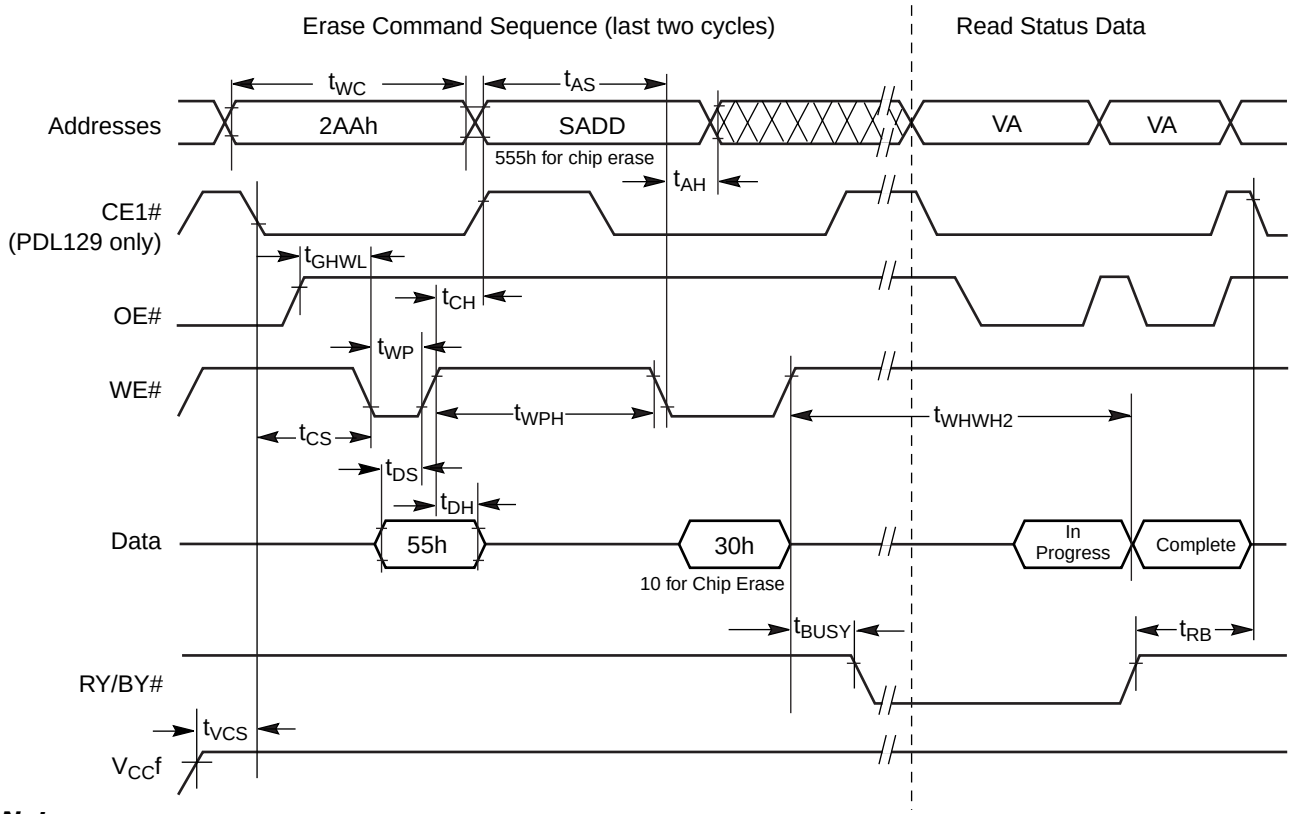


Figure 17. Accelerated Program Timing Diagram

AC CHARACTERISTICS



Notes:

1. *SADD = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Flash Write Operation Status".*
2. *For PL129H during CE1# transitions the other CE1# pin = V_{IH}.*

Figure 18. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS

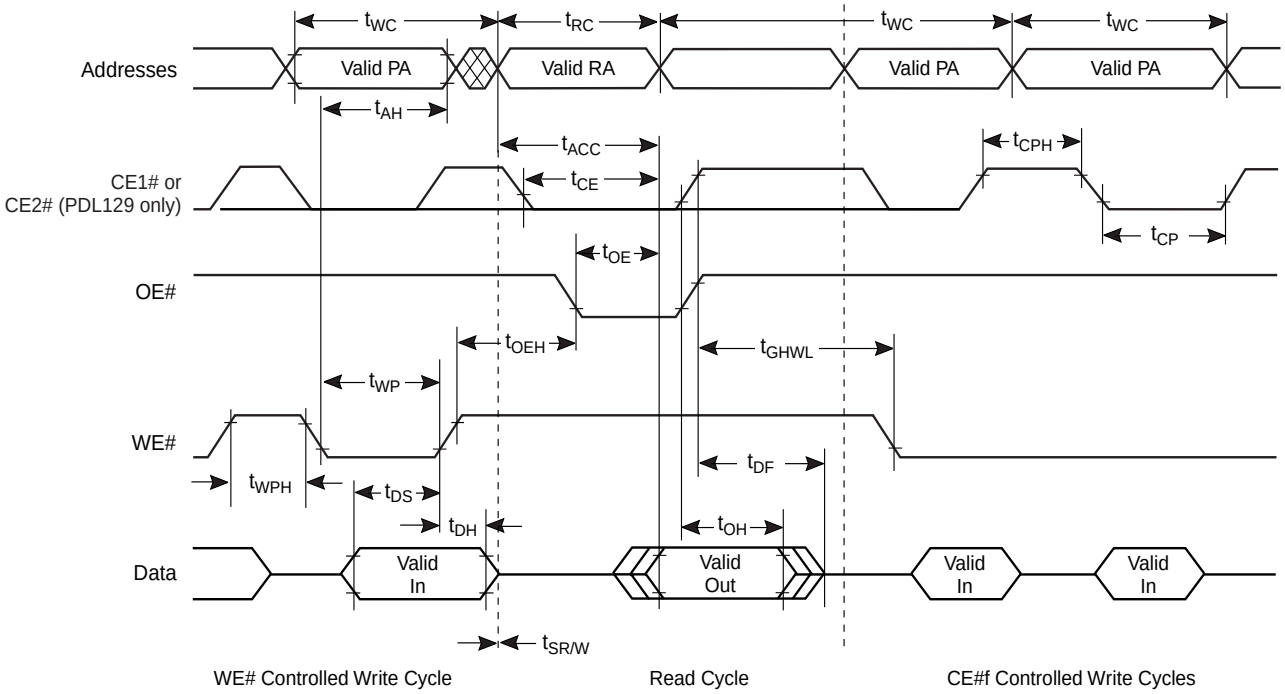
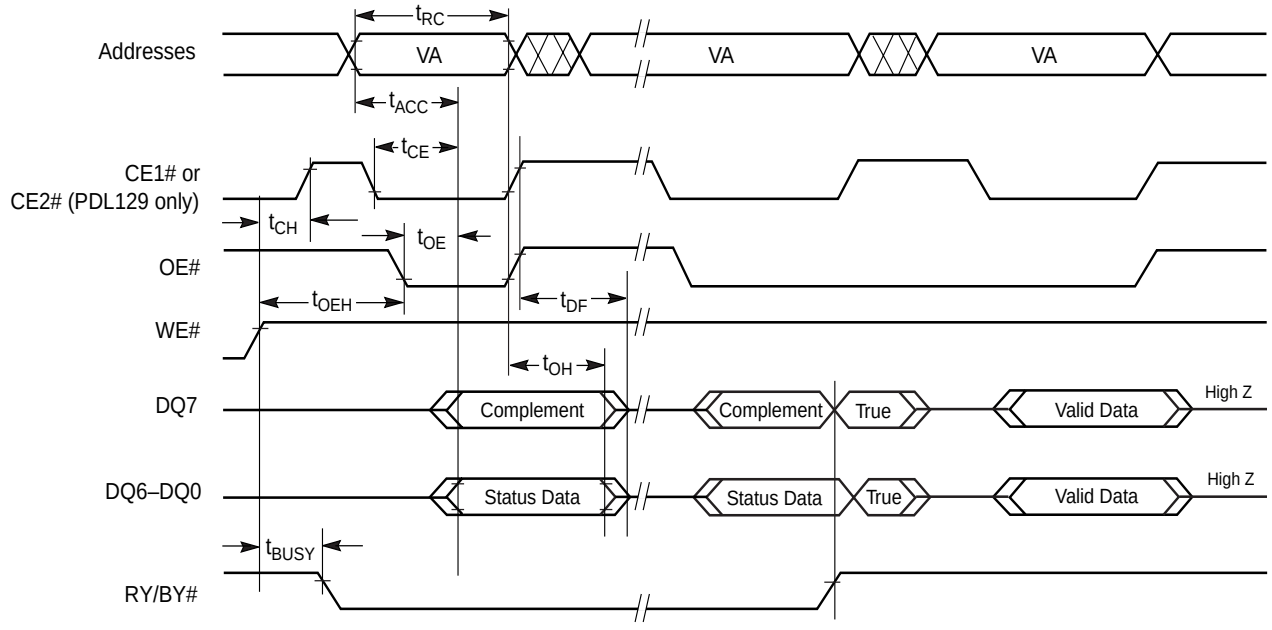


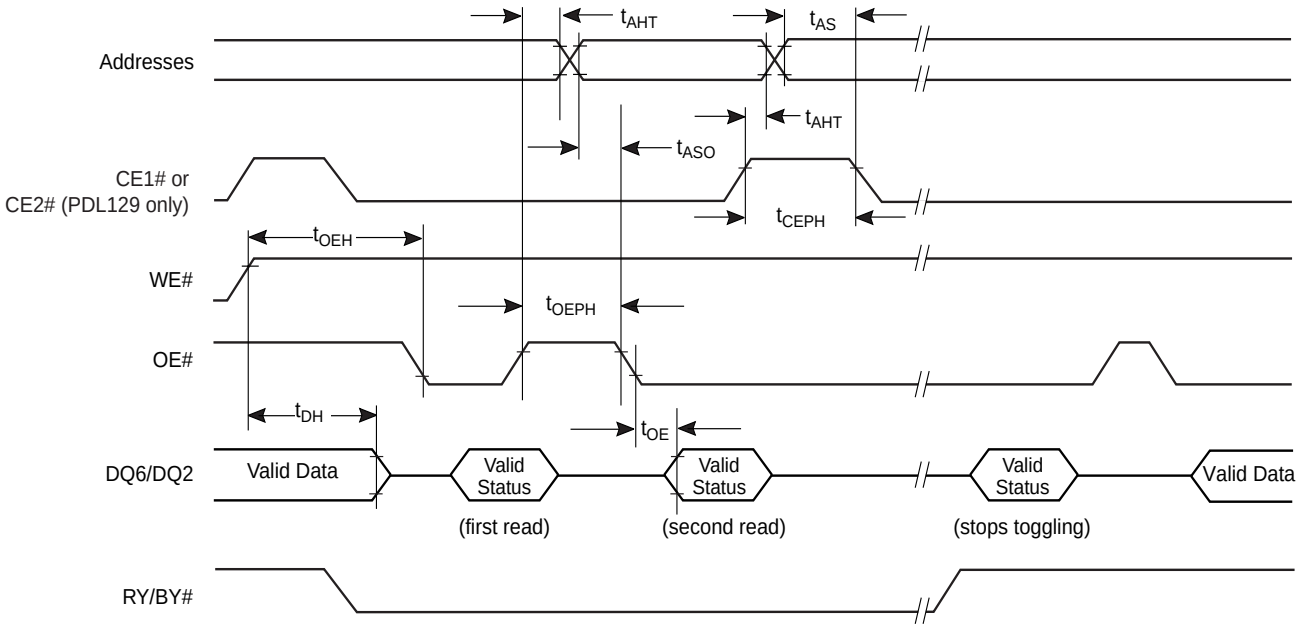
Figure 19. Back-to-back Read/Write Cycle Timings



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

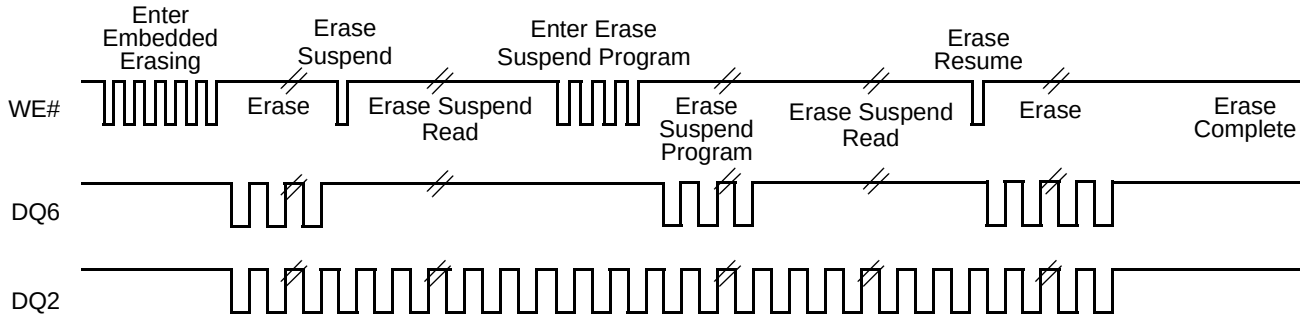
Figure 20. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 21. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE1# to toggle DQ2 and DQ6.*

Figure 22. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

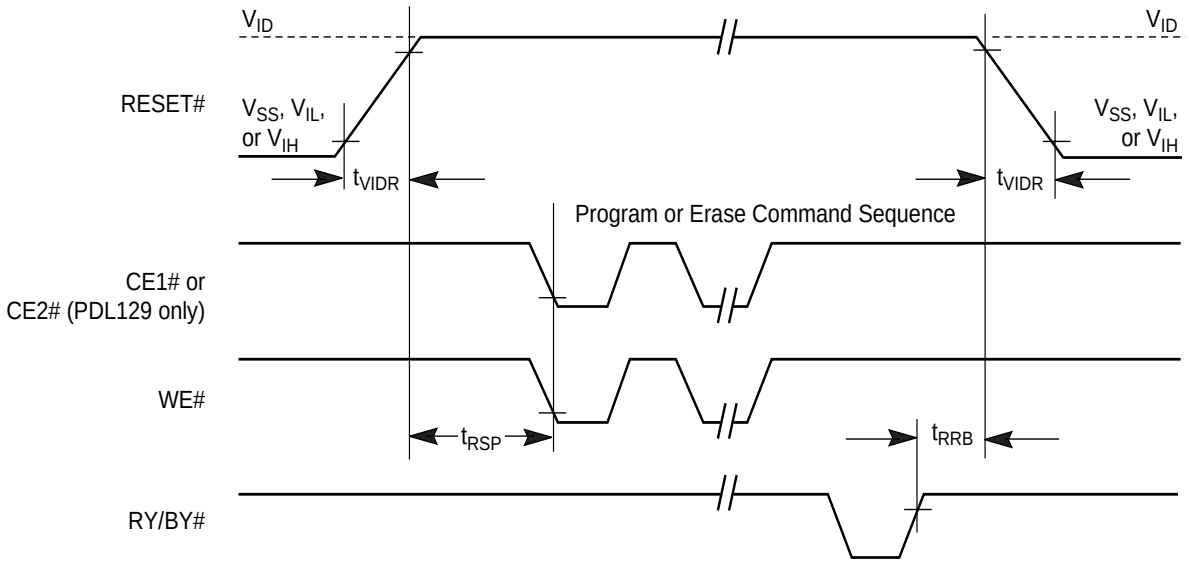
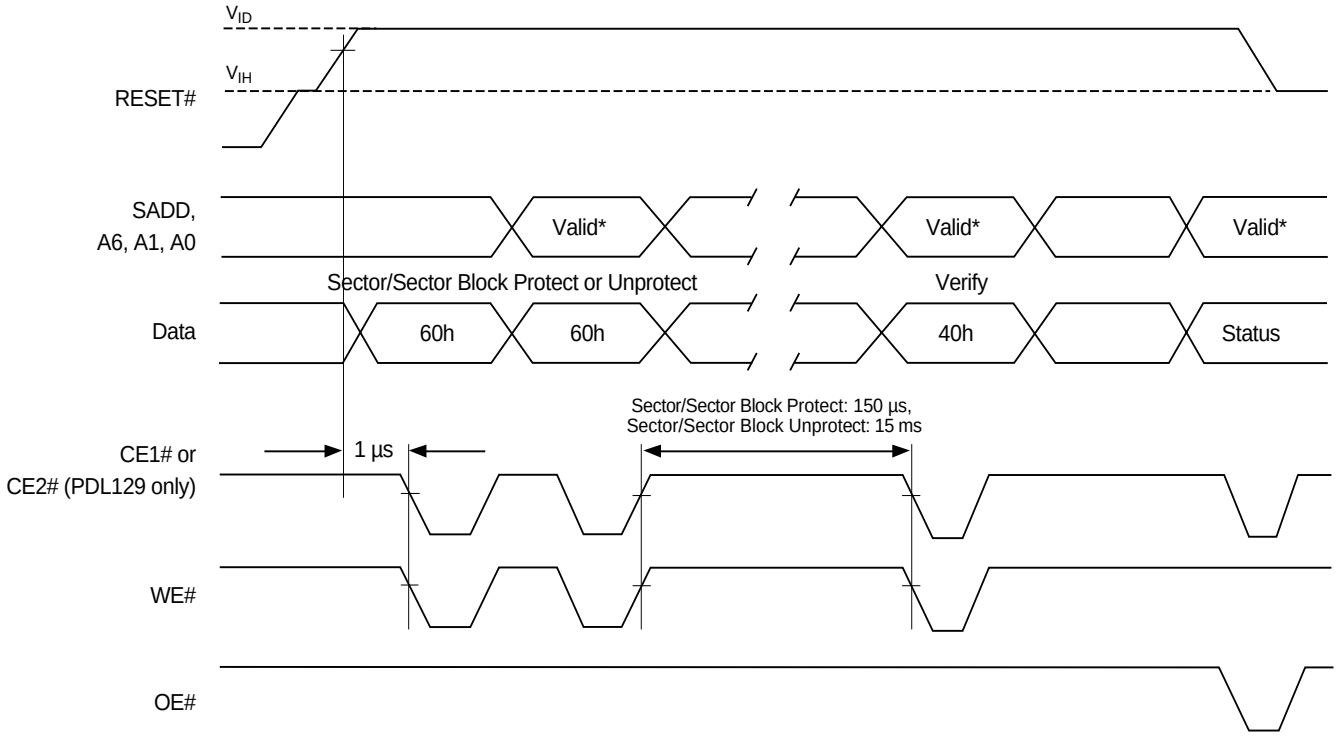


Figure 23. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS



1. *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0, SADD = Sector Address.*
2. *For PL129H during CE1# transitions the other CE1# pin = V_{IH}.*

Figure 24. Sector/Sector Block Protect and Unprotect Timing Diagram

AC CHARACTERISTICS

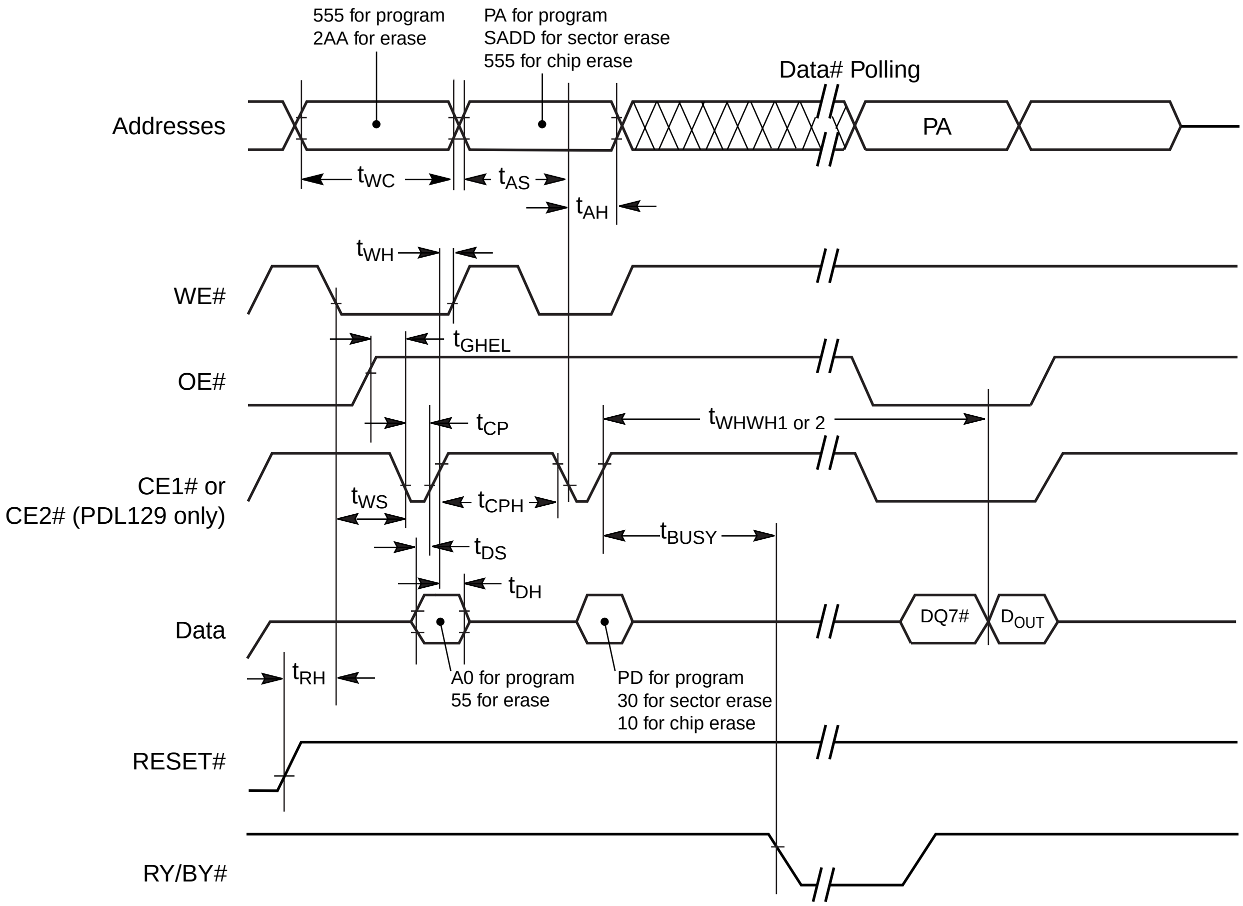
Alternate CE# Controlled Erase and Program Operations

Parameter		Description			All Speeds	Unit
JEDEC	Std					
t_{AVAV}	t_{WC}	Write Cycle Time (Note I)		Min	66	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	30	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0	ns
t_{ELEH}	t_{CP}	CE#f Pulse Width		Min	40	ns
t_{EHEL}	t_{CPH}	CE#f Pulse Width High		Min	25	ns
t_{WHWHI}	t_{WHWHI}	Programming Operation (Note 2)	Word	Typ	6	µs
t_{WHWHI}	t_{WHWHI}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	4	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.4	sec

Notes:

1. *Not 100% tested.*
2. *See the "Flash Erase And Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SADD = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*

Figure 25. Flash Alternate CE# Controlled Write (Erase/Program) Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	0.4	5	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	108		sec	
Word Program Time	7	210	µs	Excludes system level overhead (Note 5)
Accelerated Word Program Time	4	120	µs	
Chip Program Time (Note 3)	50	200	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25 °C, V_{CC} = 3.0 V; 100,000 cycles; checkerboard data pattern. All values are subject to change.*
2. *Under worst case conditions of 90 °C, V_{CC} = 2.7 V; 1,000,000 cycles. All values are subject to change.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 16 for further information on command definitions.*
6. *The device has a minimum cycling endurance of 1,000,000 cycles.*

Latchup Characteristics

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	13 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

BGA Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	3.9	4.7	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

REVISION SUMMARY

Revision A (February 05, 2004)

Initial release.

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