S30MS-P ORNAND™Flash Family

S30MS01GP, S30MS512P

1Gb/512Mb, x8/x16, 1.8 Volt NAND Interface Memory Based on MirrorBit™ Technology

Data Sheet *(Preliminary)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S30MS-P_00 **Revision** A **Amendment** 7 **Issue Date** August 4, 2006

Notice On Data Sheet Designations

Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion LLC is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion LLC therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local sales office.

S30MS-P ORNAND™ Flash Family

S30MS01GP, S30MS512P

1Gb/512Mb, x8/x16, 1.8 Volt NAND Interface Memory Based on MirrorBit™ Technology

Data Sheet *(Preliminary)*

Distinctive Characteristics

- **Single Power Supply Operation**
  - 1.8 volt read, erase, and program operations
  - V_{CC} = 1.7 to 1.95V
- **Manufactured on 90 nm MirrorBit™ Process Technology**
- **Bus widths - x8 and x16**
- **Page Size**
  - Full Page Read
    2K + 64 Byte
  - Partial Page Read
    512 + 16 Byte
- **Block (erase unit) Architecture**
  - Number of Blocks
    1Gb: 1K blocks
    512Mb: 512 blocks
  - Block Size
    128K + 4K Byte
- **Compatibility with NAND Flash I/O**
  - Provides pinout and command set compatibility with single-power supply NAND flash
- **High-Performance Cache Register**
  - Cache Register matches page size to improve programming throughput
- **100,000 Program/Erase Cycles per Sector Typical**
- **10-Year Data Retention Typical**
- **Operating Temperature Ranges**
  - Wireless (-25°C to +85°C)
- **Package options**
  - 48-pin TSOP
  - 137-ball FBGA MCP Compatible
- **100% Valid Blocks**

Performance Characteristics

Read Access Times (Maximum)	
Full Page Random Access	25 µs
Partial Page Random Access	8 µs
Serial Read	25ns

Current Consumption (typical)	
Read Current	40 mA
Erase Current	60 mA
Program Current	60 mA
Standby Current	10 uA

Read, Program and Erase Performance (typical)		
	x8	**x16**
Program	2.3 MB/s	2.4 MB/s
Erase	2.7 MB/s	2.7 MB/s
Full Page Read	26.7 MB/s	40.1 MB/s
Partial Page Read	24.3 MB/s	34.9 MB/s

Legend:
b = bit, B = Byte, K = 1024, M = 1048576

Publication Number S30MS-P_00 **Revision** A **Amendment** 7 **Issue Date** August 4, 2006

Contents

Tables

Figures

1. General Description

The S30MS-P is a 1.8V single voltage flash memory product manufactured using 90 nm MirrorBit™ technology. The S30MS01GP is a 1Gb device, organized as 64M Words or 128MB. The S30MS512P is a 512Mb device, organized as 32M Words or 64MB.

The S30MS-P family of devices offer advantages such as:

- Fast write and sustained write speed suitable for data storage applications
- Fast read speed and reliability suitable for demanding code storage applications
- Proven MirrorBit™ technology

The devices are offered in a 48-pin TSOP, or FBGA MCP-compatible packages. Each device has separate chip enable (CE#) controls for the FBGA package.

The S30MS-P is a byte/word serial-type memory device that utilizes the I/O pins for both address and data input/output, as well as for command input. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state disks, pictures storage for still cameras, cellular phones, and other systems that require high-density non-volatile data storage.

Typical application requirements are shown in the table below with reference to the ORNAND capabilities.

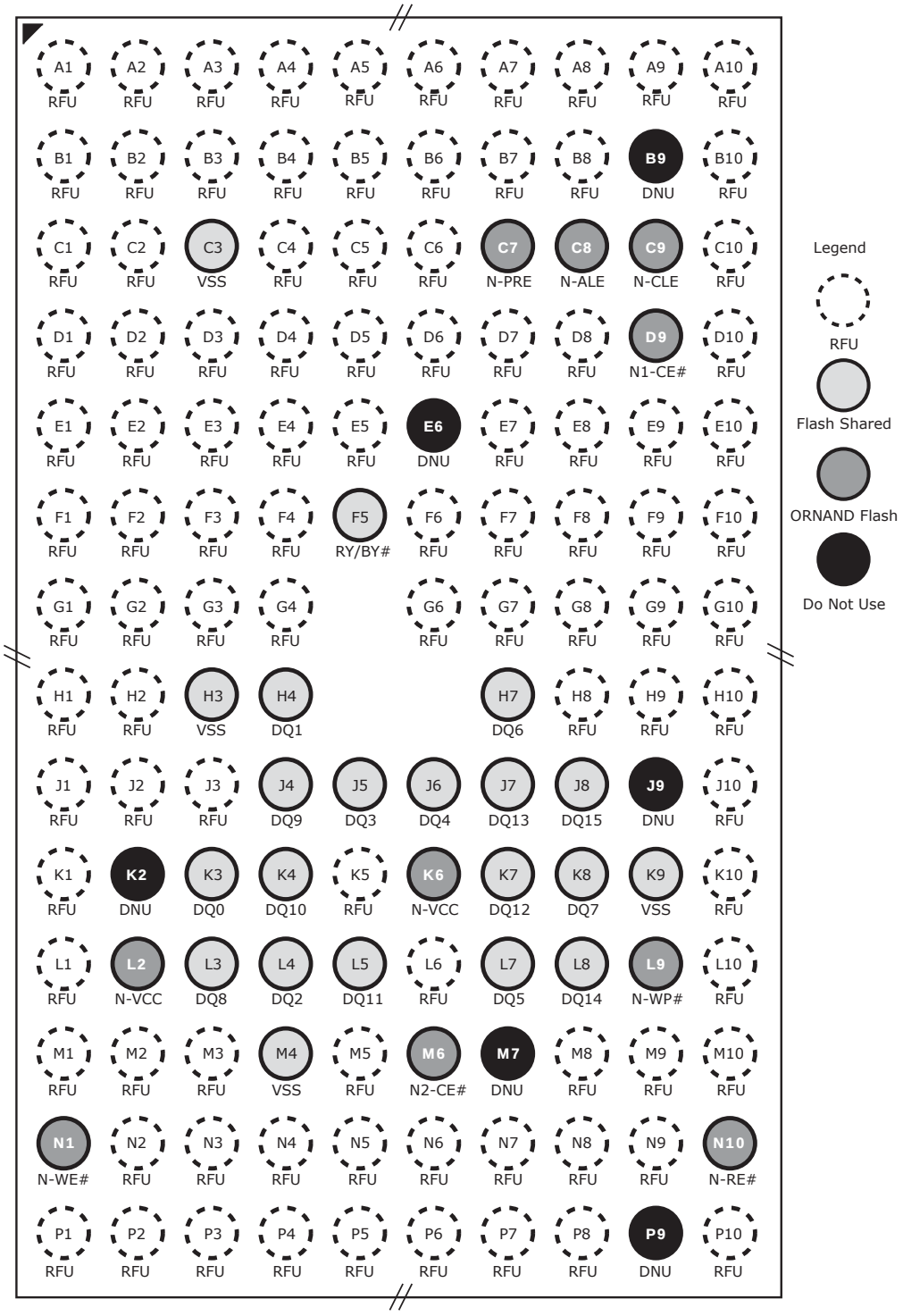
Application	Minimum Requirements	Spansion ORNAND
2G Network	14.4 Kbps (1.8 KB/sec)	✓
3G Network	2 Mbps (250 KB/sec)	✓
3.5G Network (HSPDA)	2.5 MB/sec	✓
Full Speed USB	1.5 MB/sec	✓
MP3 Playback	320 Kbps (40 KB/sec)	✓
MPEG2 (H.262)	3 MB/sec	✓
MPEG4 (H.264)	1 MB/sec	✓
WiMax	0.25 MB/sec	✓

The devices include the following features:

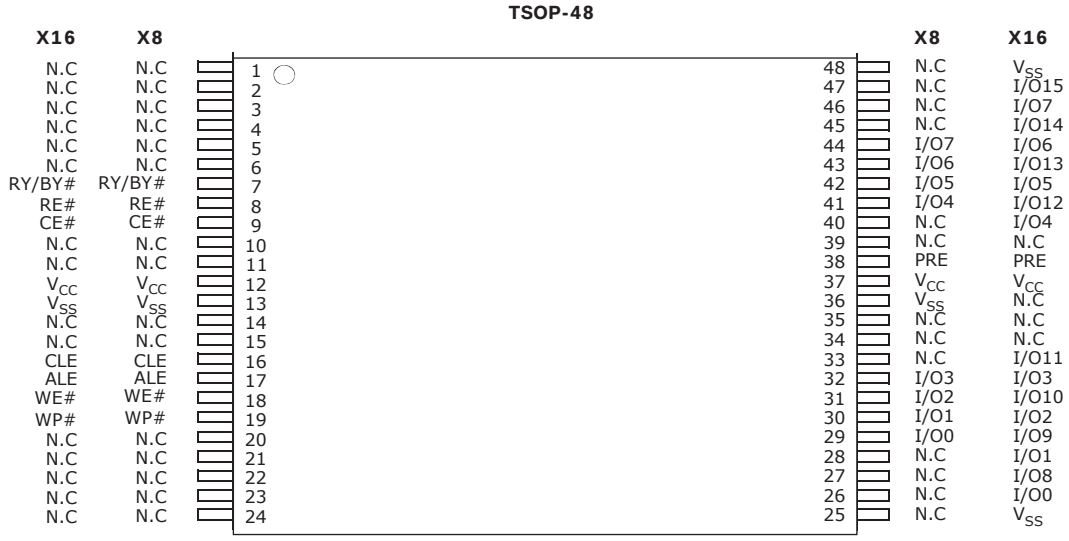
- Automatic page 0 read, allows access of the data in page 0 without command and address input of read command after power-up
- Chip Enable Don't Care support for direct connection with microcontrollers
- Compatible with NAND Flash command set. Commands are written to the device using standard microprocessor write timing. Write cycles provide commands, addresses and data
- Initiation of program and erase functions through command sequences. Once a program or erase operation begins, the host system should only poll for status or monitor the Ready/Busy# (RY/BY#) output to determine whether the operation is complete
- Manufactured using MirrorBit™ flash technology resulting in the highest levels of quality, reliability, and cost effectiveness

2. Connection Diagrams

2.1 137-Ball MS01GP MCP-Compatible FBGA Pinout

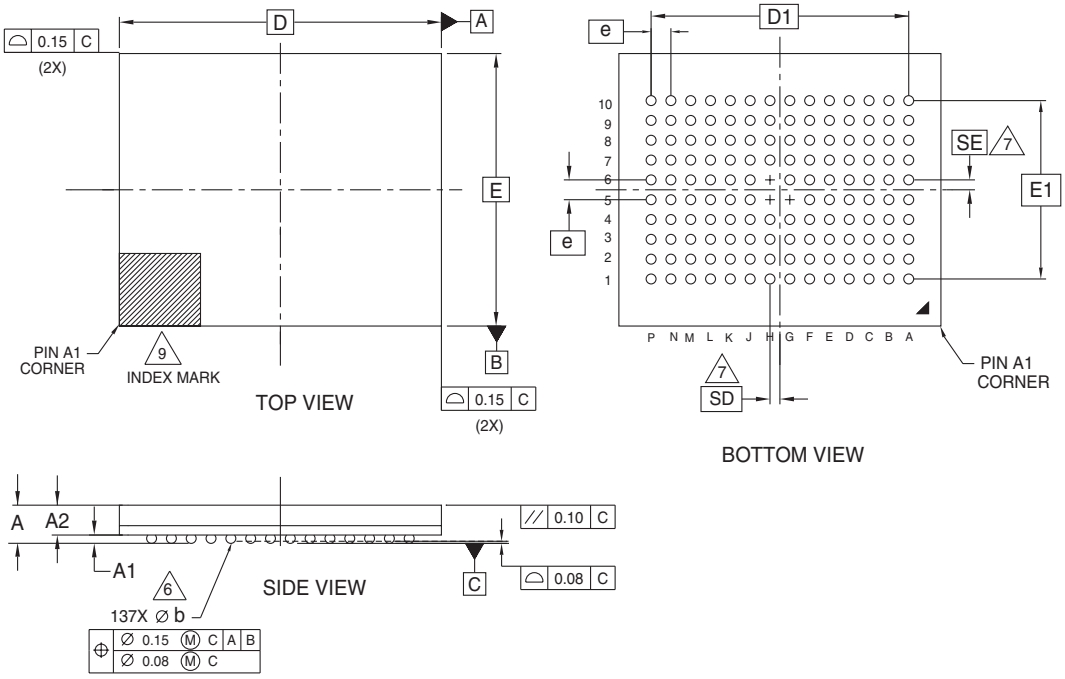


2.2 MS01GP and MS512P 48-Pin TSOP Pinout



3. Physical Dimensions

3.1 VBP137—137-Ball Fine Pitch Ball Grid Array (FBGA)



PACKAGE	VBP 137			
JEDEC	N/A			
	13.00 mm x 11.00 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.00	OVERALL THICKNESS
A1	0.17	---	---	BALL HEIGHT
A2	0.60	---	0.76	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	10.40 BSC.			BALL FOOTPRINT
E1	7.20 BSC.			BALL FOOTPRINT
MD	14			ROW MATRIX SIZE D DIRECTION
ME	10			ROW MATRIX SIZE E DIRECTION
N	137			TOTAL BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
e	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	G5,H5,H6			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

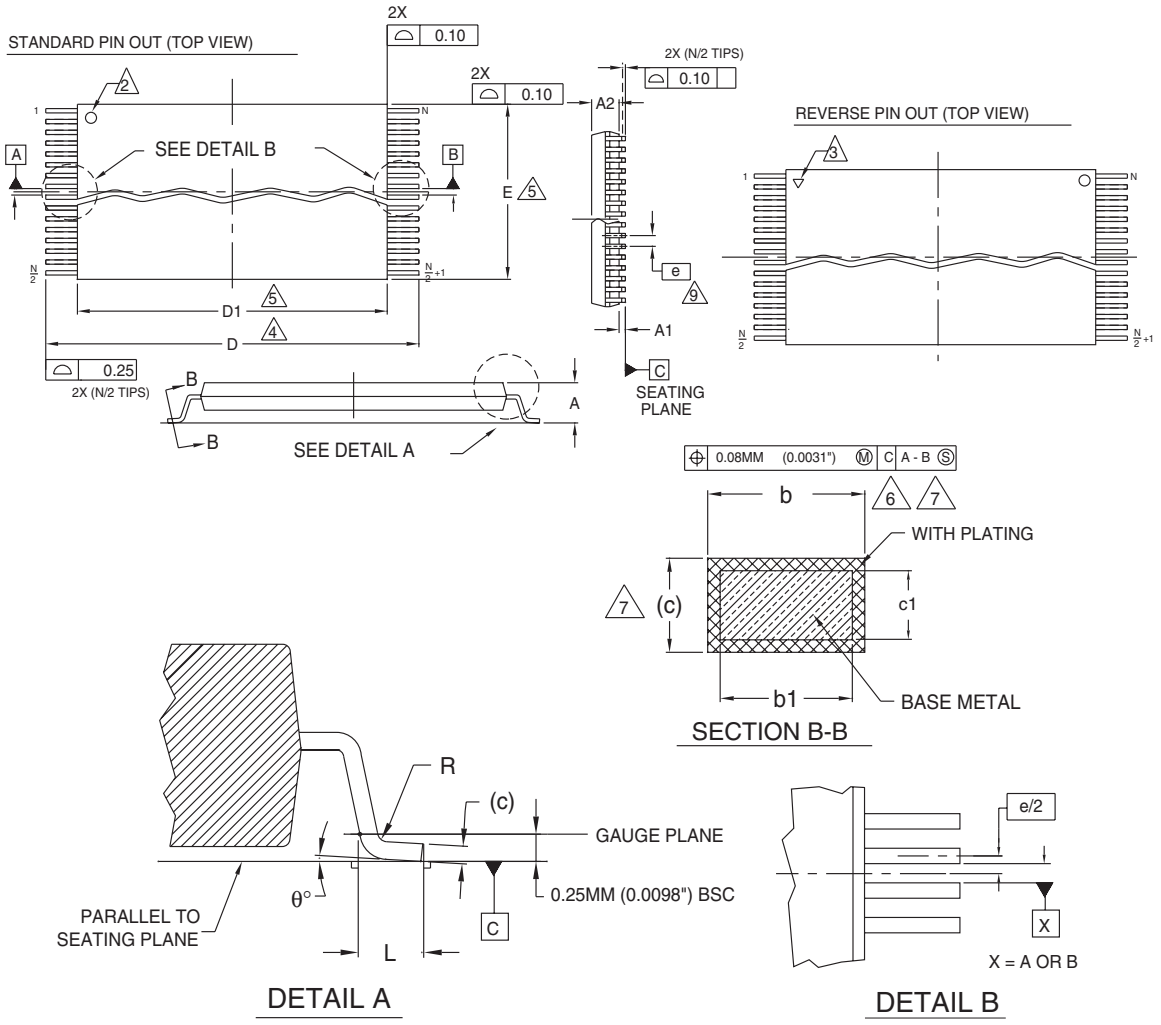
   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3549 \ 16-038.25 \ 2.16.6

3.2 48-Pin TSOP



Package	TS/TSR 048		
Jedec	MO-142 (D) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

3355 \ 16-038.10c

4. Pin Names and Descriptions

4.1 Pin Names and Functions

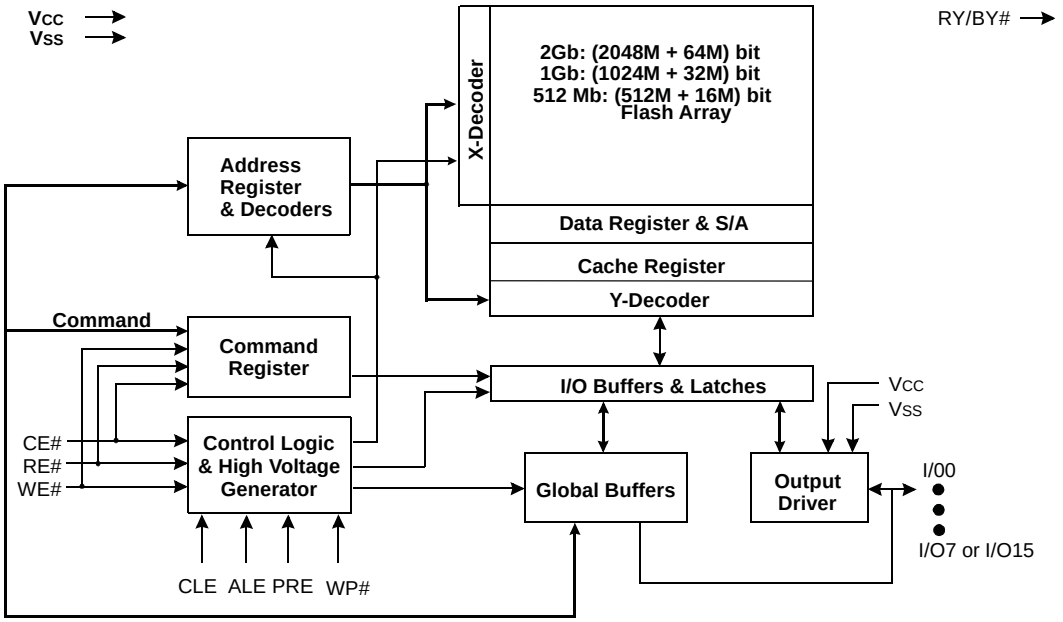
Pin Name	Pin Function
I/O0 to I/O15	Data Input/Output
CLE	Command Latch Enable
ALE	Address Latch Enable
CE#, CE1#, CE2#	Chip Enable
RE#	Read Enable
WE#	Write Enable
WP#	Write Protect
PRE	Power on Read Enable
RY/BY#	Ready/Busy Output
V_{CC}	Power
V_{SS}	Ground
N.C.	No Connection

4.2 Pin Descriptions

The device is a byte/word serial access memory that utilizes time-sharing input of address information. The device pin-outs are configured as shown in *137-Ball MS01GP MCP-Compatible FBGA Pinout* on page 5.

Pin	Description
CLE	**Command Latch Enable**: The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the WE# signal while CE# is low and CLE is High.
ALE	**Address Latch Enable**: The ALE signal is used to control loading of either address information or input data into the internal address/data register. Address information is latched on the rising edge of WE# if CE# is low and ALE is High. Input data is latched if CE# is low and ALE is Low.
CE#, CE1#, CE2#	**Chip Enable**: The device enters a low-power Standby mode when the device is in Ready mode. The CE# signal is ignored when the device is in a Busy state (RY/BY# = L), such as during a Page Buffer Load or Erase operation, and will not enter Standby mode even if the CE# input goes high. The CE# signal may be inactive during the Page Buffer write and Page Buffer load of the array data. The 2Gb device has two chip enable pins: CE1# and CE2# (one per die).
WE#	**Write Enable**: The WE# signal is used to control the acquisition of data from the I/O port.
RE#	**Read Enable**: The RE# signal controls serial data output. Data is available t_{REA} after the falling edge of RE#. The internal column address counter is also incremented (Address = Address + 1) on this falling edge.
I/O0 to I/O7	**I/O Port**: The I/O0 to I/O7 pins are used as a port for transferring address, command, and input/output data to and from the device.
I/O8 to I/O15	**I/O Port**: The I/O8 to I/O15 pins are used as a port for transferring input/output data to and from the device in x16 mode only. I/O8 to I/O15 pins must be low level during address and command input.
WP#	**Write Protect**: The WP# signal is used to protect the device from accidental programming or erasing. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.
RY/BY#	**Ready/Busy**:The RY/BY# output signal is used to indicate the operating condition of the device. The RY/BY# signal is in Busy state (RY/BY# = L) during the Program, Erase, and Read operations and return to Ready state (RY/BY# = H) after completion of the operation. The output buffer for this signal is an open drain.
PRE	**Power-on Read Enable**: The PRE controls auto read operation executed during power-on. The power-on auto-read is enabled when PRE pin in tied to V_{CC}.
V_{SS}	**Ground**: V_{SS} is the Ground.
N.C	**No Connection**: Lead is not internally connected.

5. Block Diagram



6. Absolute Maximum Ratings

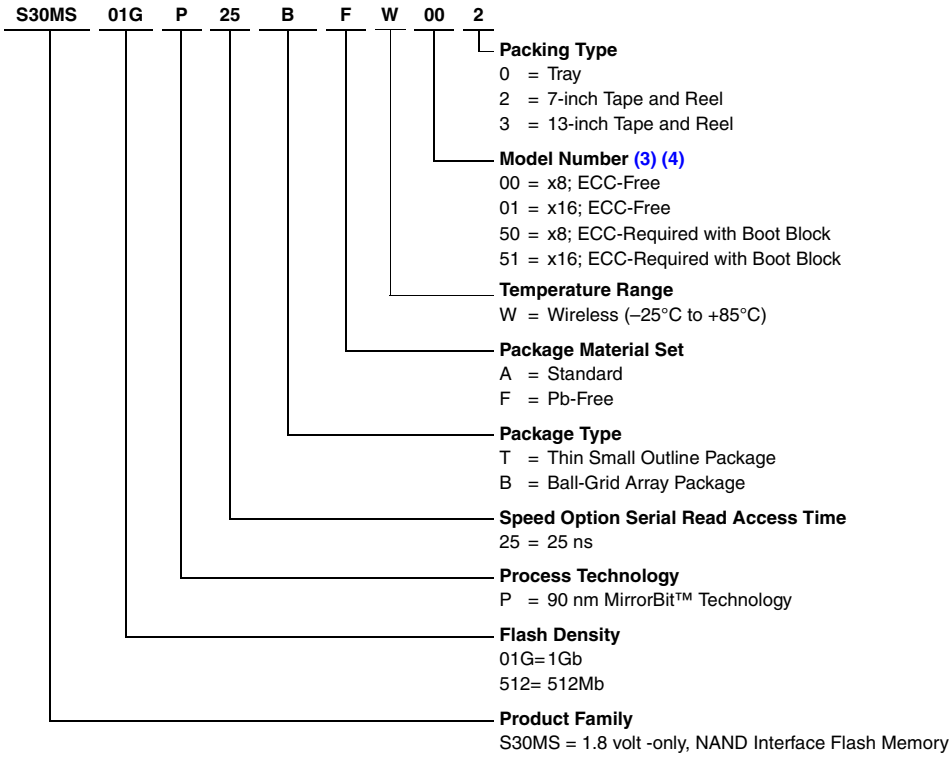
Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	$V_{IN/OUT}$	-0.5 to Vcc + 0.5	V
	V_{CC}	-0.5 to + 2.5	
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70 (Commercial) -40 to +85 (Industrial) -25 to +85 (Wireless)	°C
Temperature under bias	T_{BIAS}	-65 to 125	°C
Short circuit current	I_{OS}	5	mA

Notes:

1. *Minimum DC voltage is -0.6v on input/output pins. During transitions, this level may undershoot to -2.0v for periods <30ns.*
2. *Maximum DC voltage on input/output pins is Vcc+0.3v which, during transitions, may overshoot to Vcc+2.0v for periods < 20ns.*
3. *Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as details in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

7. Ordering Information

The order number is formed by a valid combinations of the following:



7.1 Valid Combinations

Valid Combination list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations					
Base Ordering Part Number	**Speed Option**	**Package Type, Material, and Temperature Range**	**Model Number**	**Packing Type**	**Package Type**
S30MS01GP S30MS512P	25	BAW, BFW	00, 01, 50, 51	0, 3 (Note 1)	137-Ball FBGA
		TAW, TFW			TSOP-48

Notes:

1. *Type 0 is standard. Specify other options as required.*
2. *See the MCP ORNAND data sheet for further package details.*
3. *Model Numbers 50 and 51 must use 2-bit detection, 1-bit correction for applications that require 100% error-free read performance.*
4. *Model Numbers 50 and 51 may have up to 2% invalid blocks.*
5. *Model Numbers 50 and 51 have a boot block (Block 0 is valid upon shipment and error-free through 1000 cycles).*

8. Electrical Specifications

8.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	$V_{IN/OUT}$	–0.5 to V_{CC} + 0.5	V
	V_{CC}	–0.5 to + 2.5	
Storage Temperature	T_{STG}	–65 to +150	°C
Operating Temperature	T_{OPR}	–25 to +85 (Wireless)	°C
Temperature under bias	T_{BIAS}	–65 to +125	°C
Short circuit current	I_{OS}	5	mA

Notes:

1. *Minimum DC voltage is –0.6 V on input/output pins. During transitions, this level may undershoot to –2.0 V for periods <30 ns.*
2. *Maximum DC voltage on input/output pins is V_{CC} +0.3 V which, during transitions, may overshoot to V_{CC}+2.0 V for periods < 20 ns.*
3. *Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

8.2 Capacitance (Ta = 25°C, f = 1 MHz)

Parameter Symbol	Parameter Description	Test Condition	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	—	10	pF
			—	10	pF
C_{IN2}	CE# pin Input Capacitance	V_{IN} = 0	—	17	pF
C_{IN3}	WE# pin Input Capacitance	V_{IN} = 0	—	32	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	—	10	pF
			—	10	pF

Notes:

1. *Test conditions T_a = 25°C, f = 1.0 MHz*
2. *Sampled, not 100% tested.*

8.3 Valid Blocks

Valid Blocks are fully erased when the device is shipped from the factory. To identify blocks that are invalid at the time of shipment, the system must read the lowest address in the first two pages of the spare area. If a non-blank data pattern is read from either of these two addresses, the block is invalid.

Parameter Symbol	Parameter Description	Density	Model Number	Min.	Max.	Unit
N_{VB}	Number of Valid Blocks	512Mb	50, 51	502	512	Blocks
			00, 01	512	512	Blocks
		1Gb	50, 51	1004	1024	Blocks
			00, 01	1024	1024	Blocks

8.4 Recommended DC Operating Conditions

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	1.7	1.8	1.95	V
V_{SS}	Power Supply Voltage	0	0	0	V

8.5 DC Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	V_{CC} active read current (average during read cycle)	t_{RC} = 25 ns, I_{OUT} = 0 mA	—	40	45	mA
I_{CC2}	V_{CC} current during data transfer from memory cell array to Page Buffer	—	—	40	45	mA
I_{CC3}	V_{CC} current during data output	t_{RC} = 25 ns	—	10	20	mA
I_{CC4}	Program current (standard mode)	—	—	60	75	mA
I_{CC5}	Erase Current (standard mode)	—	—	60	75	mA
I_{SB1}	Stand-by Current (TTL)	CE# = V_{IH}, WP# = PRE# = V_{IL}	—	—	1	mA
I_{SB2}	Stand-by Current (CMOS)	CE# = V_{CC} –0.2 V, WP# = PRE# = 0.2 V All other pins = -0.1 V	—	10	60	µA
I_{LI}	Input Leakage Current	V_{IN} = 0 to V_{CC}, V_{CC}= V_{CC} max	—	—	±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to V_{CC}, V_{CC}= V_{CC} max	—	—	±1	µA
V_{IH} (note 1)	Input High Voltage		V_{CC} - 0.4	—	V_{CC} + 0.2	V
V_{IL} (note 2)	Input Low Voltage	—	–0.3	—	0.4	V
V_{OH}	Output High Voltage Level	I_{OH} = –100 µA, V_{CC}= V_{CC}min	V_{CC} - 0.1	—	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = 100 µA, V_{CC}= V_{CC} min	—	—	0.1	V
I_{OL}	Output Low Current (RY/BY#)	V_{OL} = 0.1 V	2	4	—	mA

Notes:

1. *V_{IH} can overshoot to V_{CC} +0.4 V for durations of 20 ns or less.*
2. *V_{IL} can undershoot to –0.4 V for durations of 20 ns or less.*

8.6 AC Characteristics

Parameter Symbols	Description	Min.	Max.	Unit
t_{CLS}	CLE Setup Time	-1	—	ns
t_{CLH}	CLE Hold Time	8	—	ns
t_{CS}	CE# Setup Time	0	—	ns
t_{CH}	CE# Hold Time	8	—	ns
t_{WP}	Write Pulse Width	25	—	ns
t_{ALS}	ALE Setup Time	-1	—	ns
t_{ALH}	ALE Hold Time	8	—	ns
t_{DS}	Data Setup Time	15	—	ns
t_{DH}	Data Hold Time	8	—	ns
t_{WC}	Write Cycle Time	40	—	ns
t_{WH}	WE# High Hold Time	10	—	ns
t_{WW}	WP# High to WE# Low	100	—	ns
t_{RR}	Ready to RE# Falling Edge	20	—	ns
t_{RW}	Ready to WE# Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	17	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	RE# Access Time	—	17	ns
t_{CR}	CE# to RE# Time	10		ns
t_{AR}	ALE to RE# Time	10		ns
t_{CLR}	CLE to RE# Time	10		ns
t_{OH}	Data Output Hold Time	5	—	ns
t_{RHZ}	RE# High to Output High Impedance	—	15	ns
t_{CHZ}	CE# High to Output High Impedance	—	15	ns
t_{REH}	RE# High Hold Time	8	—	ns
t_{IR}	Output High Impedance to RE# Falling Edge	0	—	ns
t_{RHW}	RE# High to WE# Low	30	—	ns
t_{WHC}	WE# High to CE# Low	30	—	ns
t_{WHR}	WE# High to RE# Low	60	—	ns
t_R	Full Page Data Transfer from Memory Cell Array to Register	—	25	µs
	Partial Page Data Transfer from Memory Cell Array to Register	—	8	
t_{RPRE}	Full page Data Transfer to Register During Power On Read	—	50	µs
t_{WB}	WE# High to Busy	—	100	ns
t_{RST}	Device Resetting Time (Read/Program/Erase)	—	1/1/15	µs

8.7 AC Test Conditions

Operating Range	V_{CC} 1.7 V to 1.95 V
Input level	0.0 to V_{CC}
Input comparison level	$V_{CC}/2$
Output data comparison level	$V_{CC}/2$
Load capacitance (C_L)	30 pF
Transition time (t_T) (input rise and fall times)	5 ns

8.8 Program and Erase Characteristics

Symbol	Parameter	Min.	Typ. (Note 4)	Max. (Note 5)	Unit
t_{CBSY1}	Dummy Busy Time for Cache Programming (first 15h) (Note 2)	—	0.4	0.8	µs
t_{CBSY2}	Dummy Busy Time for Cache Programming (next 15h) (Note 3)	—	0.8	4.4	ms
t_{PROG}	Page Programming Time	—	0.8	4.4	ms
t_{PPROG}	Partial Page Programming Time	—	260	1400	µs
N	Number of Programming Cycles on Same Page (Note 1)	—	—	8	
t_{BERASE}	Block Erasing Time	—	50	150	ms

Notes:

1. *One programming cycle per segment. Refer to Page Program on page 27 for more information.*
2. *First cache programming of a sequence.*
3. *Following cache programming of a sequence - second page and following pages.*
4. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 10,000 cycles; checkerboard data pattern.*
5. *Under worst case conditions of 90°C, V_{CC}=1.70 V, 100,000 cycles.*

9. Timing Diagrams

Figure 9.1 Command Input Cycle Timing Diagram

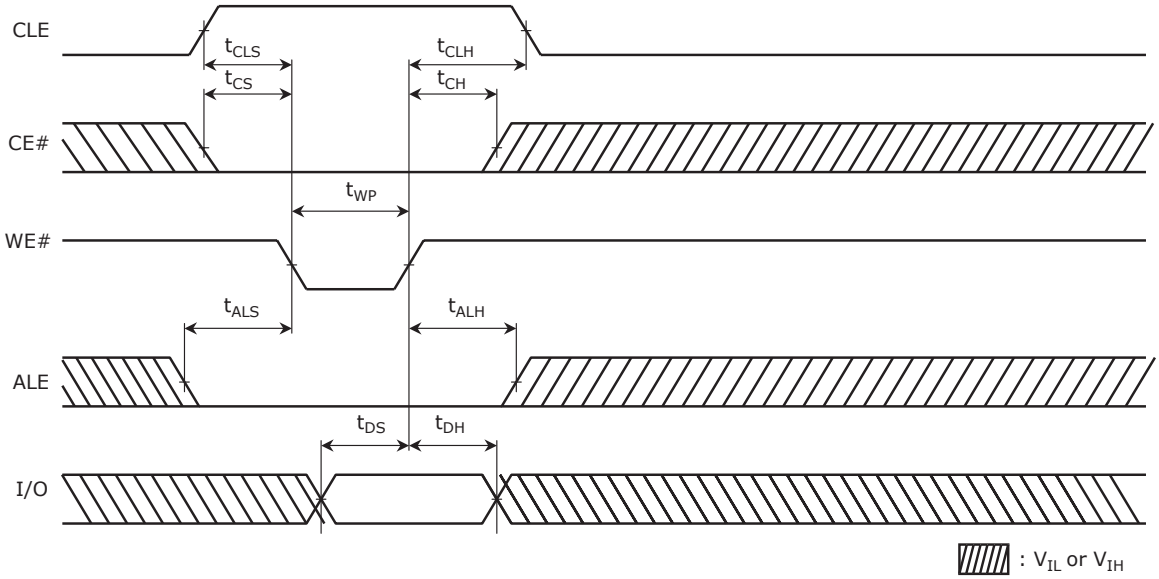


Figure 9.2 Address Input Cycle Timing Diagram

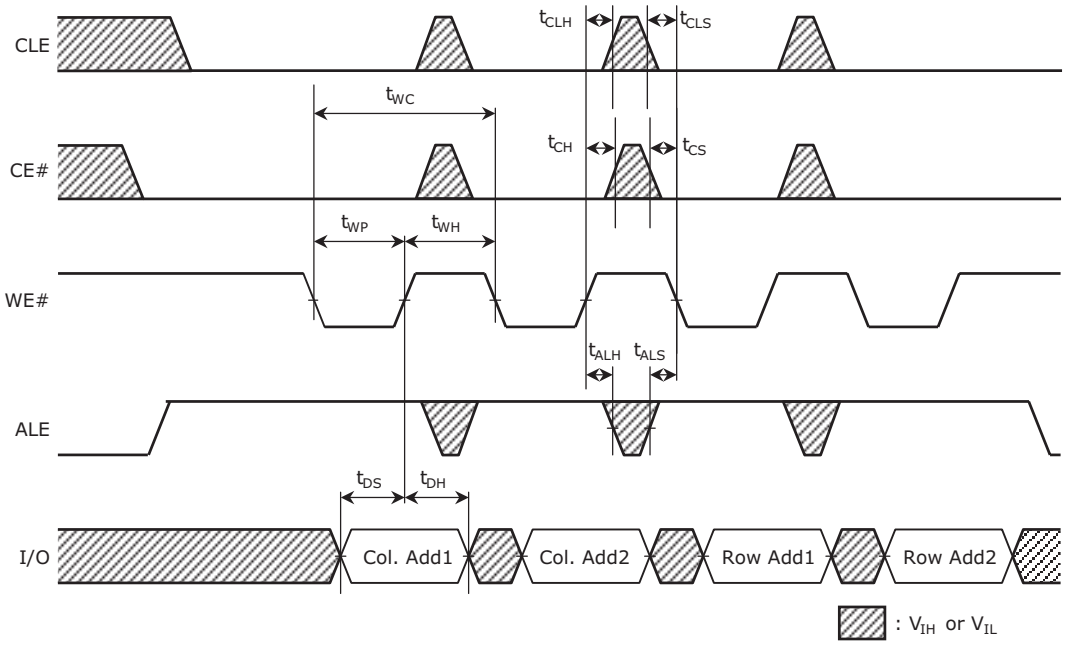


Figure 9.3 Data Input Cycle Timing Diagram

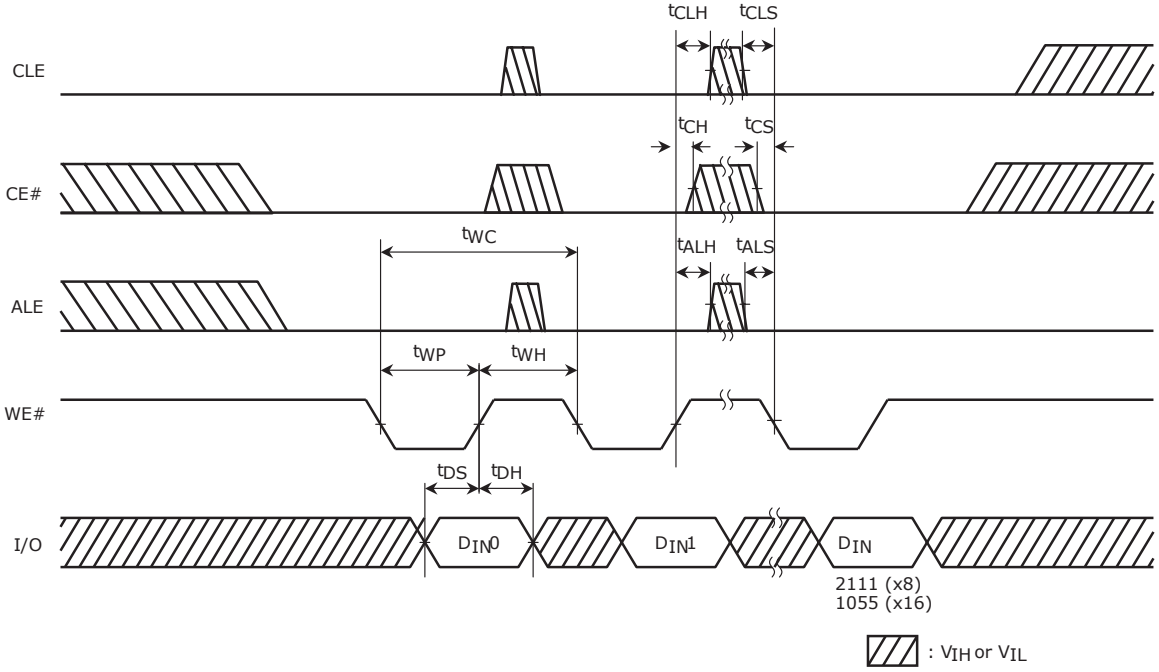


Figure 9.4 Serial Read Cycle Timing Diagram

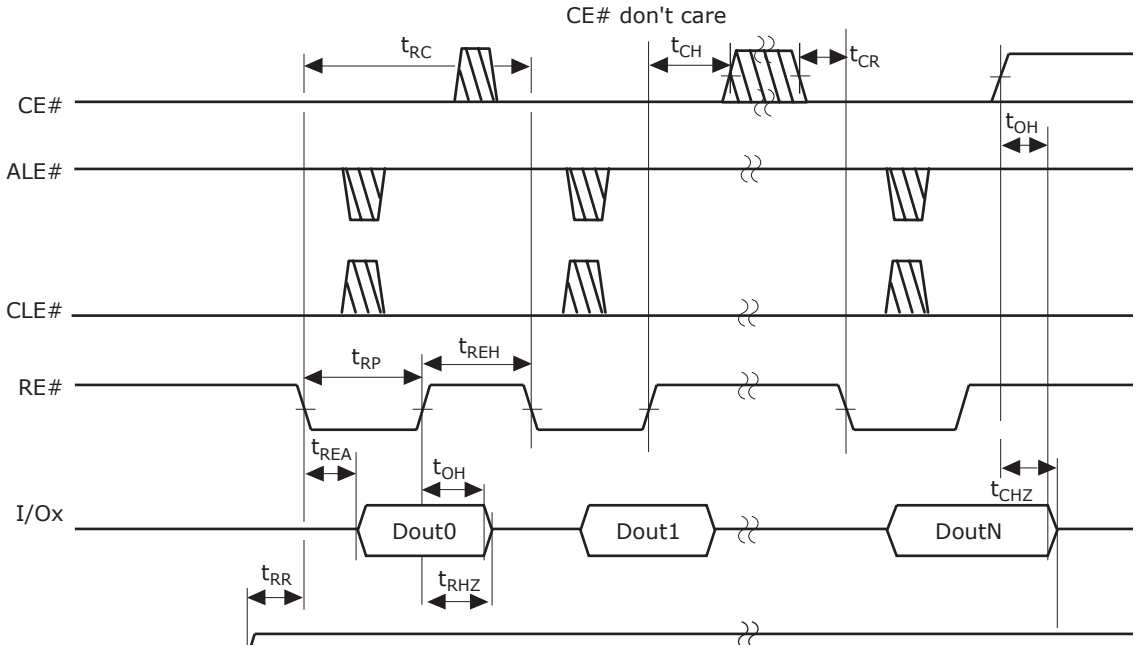


Figure 9.5 Status Read Cycle Timing Diagram

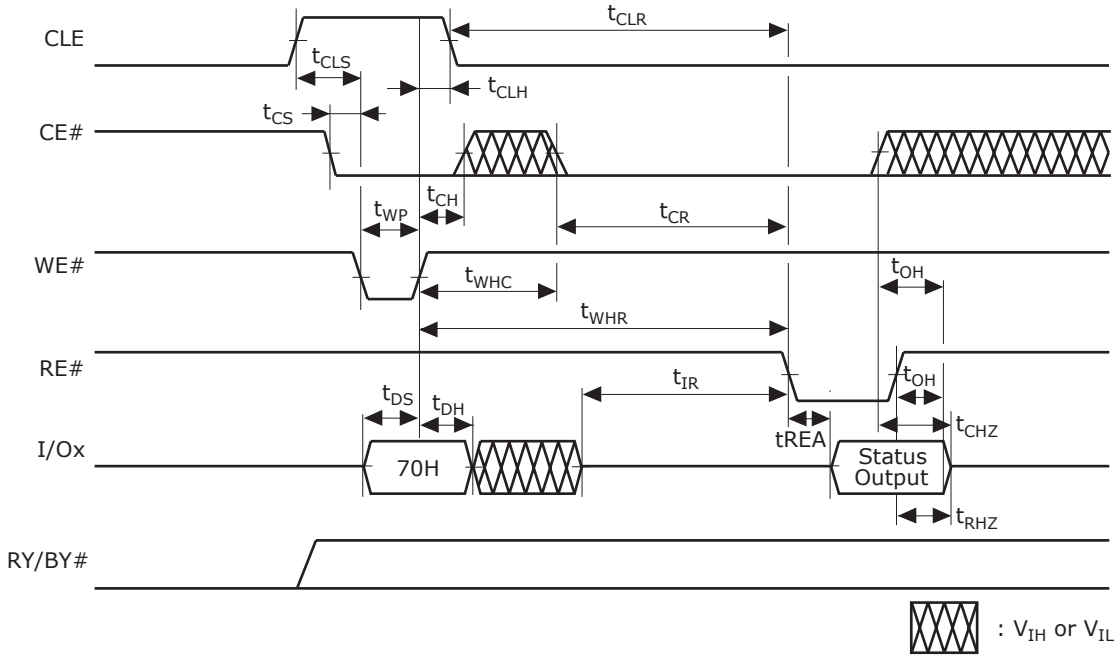


Figure 9.6 Read Cycle Timing Diagram

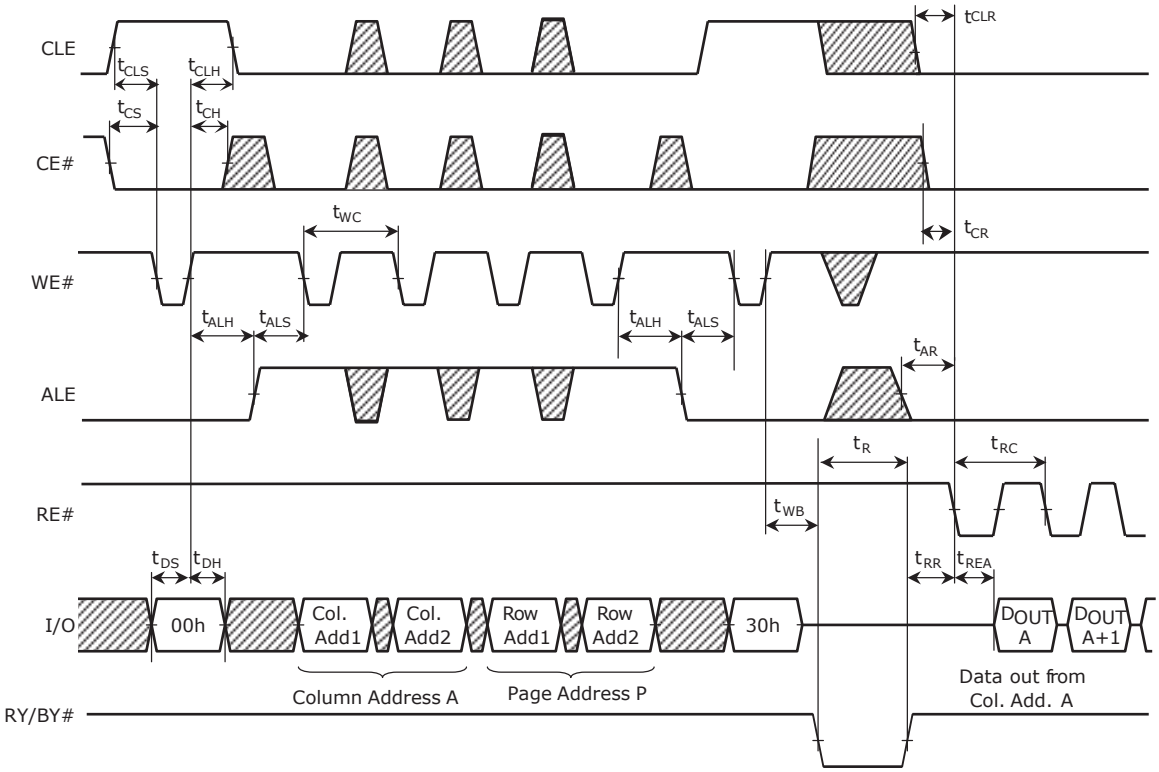


Figure 9.7 Column Address Change in Read Cycle Timing Diagram (1/2)

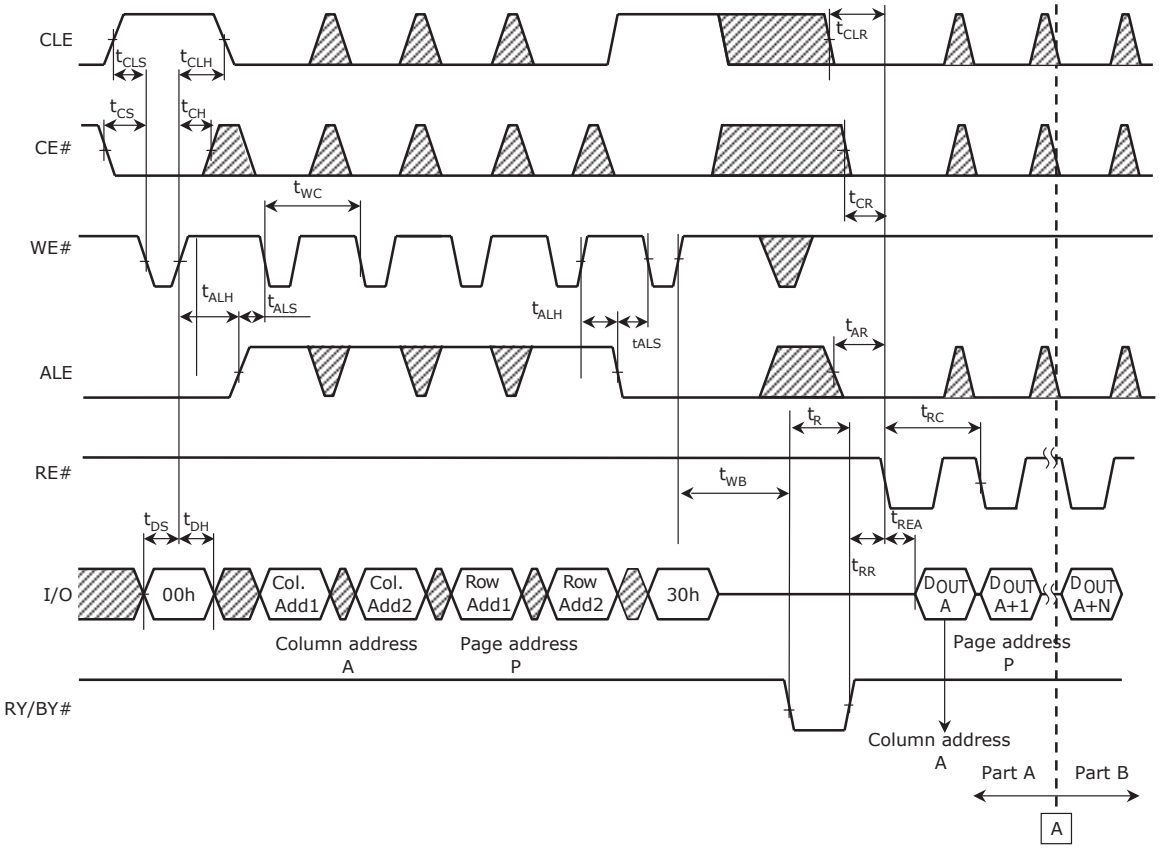


Figure 9.8 Column Address Change in Read Cycle Timing Diagram (2/2)

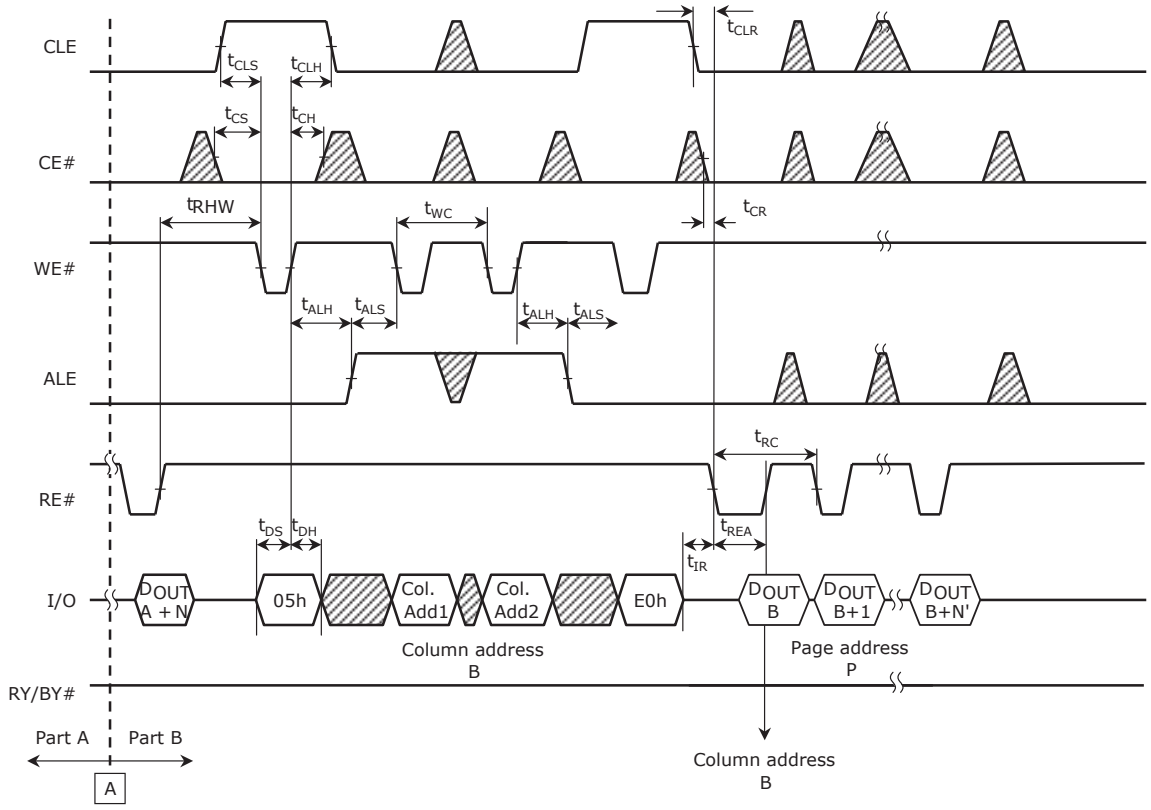


Figure 9.9 Program Operation Timing Diagram

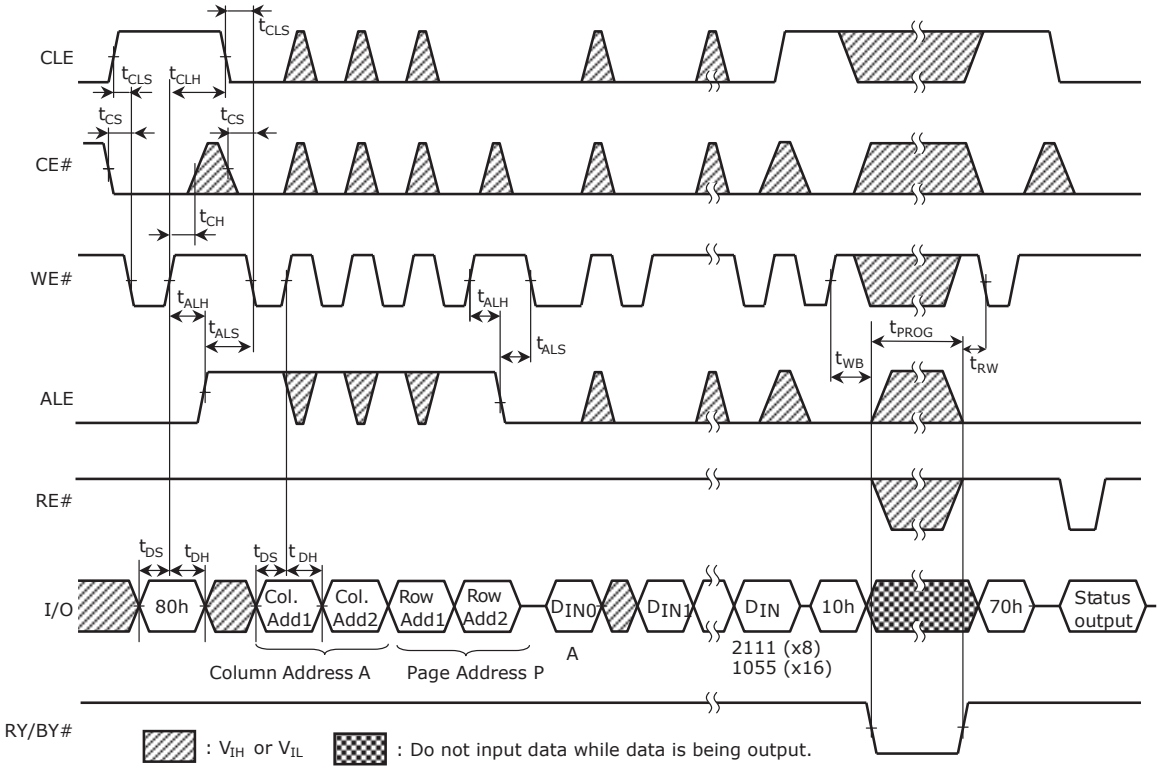
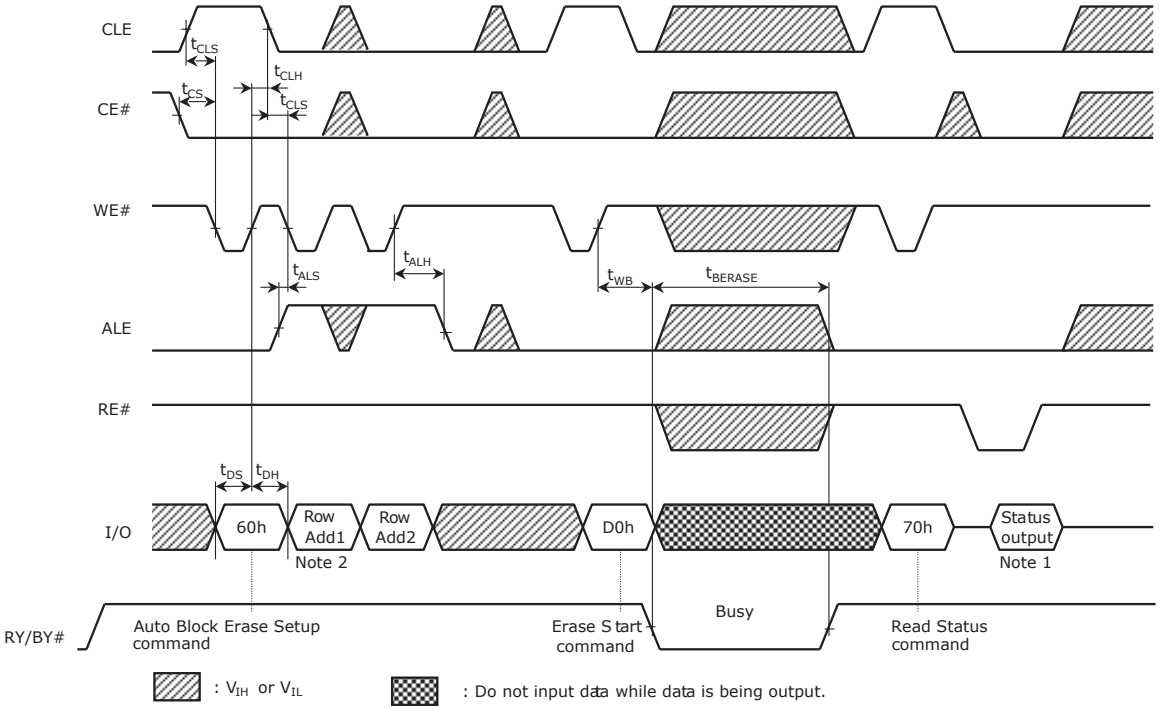


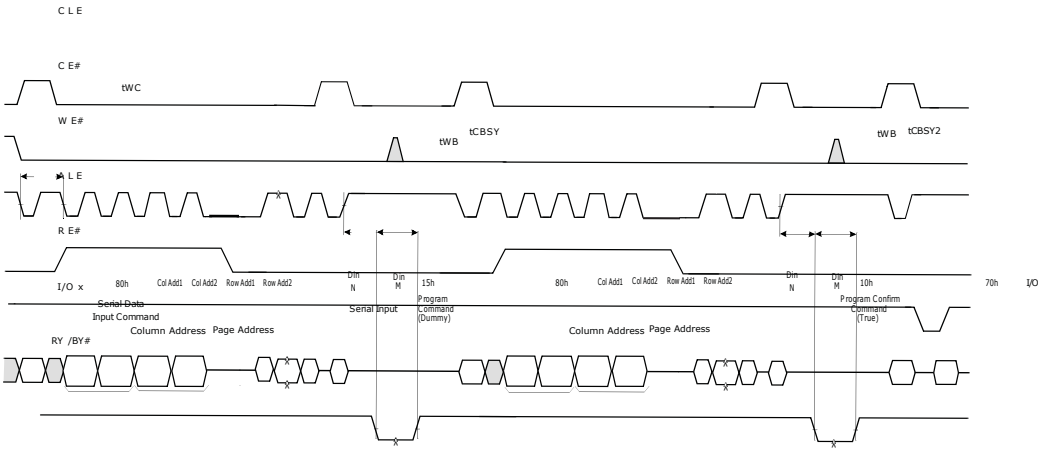
Figure 9.10 Block Erase Timing Diagram



Notes:

1. *If I/O 0 =* 0*, then the erase is successful. If I/O0 =* 1*, then there is an error in the erase.*
2. *Only the block address part of the* Row Address *bytes are used; page address is ignored.*

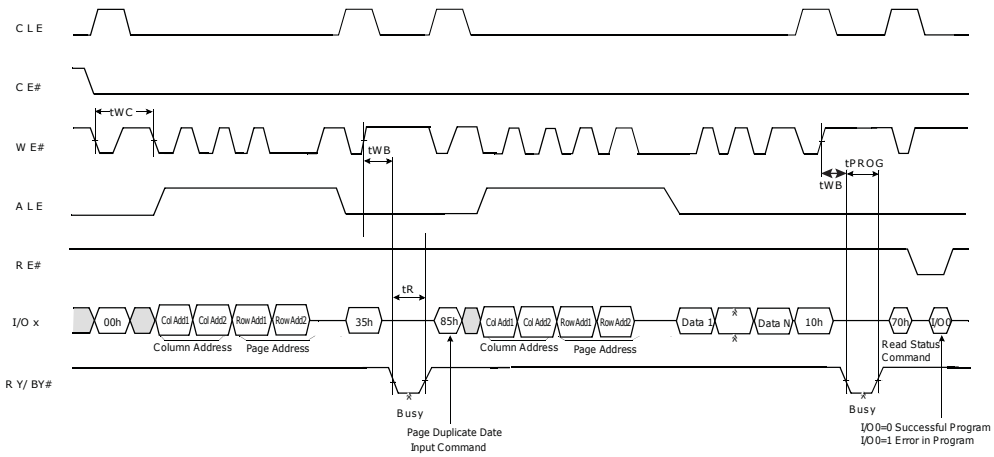
Figure 9.11 Cache Program Operation Timing Diagram



Note:

CE#, CLE, and ALE are Don't care.

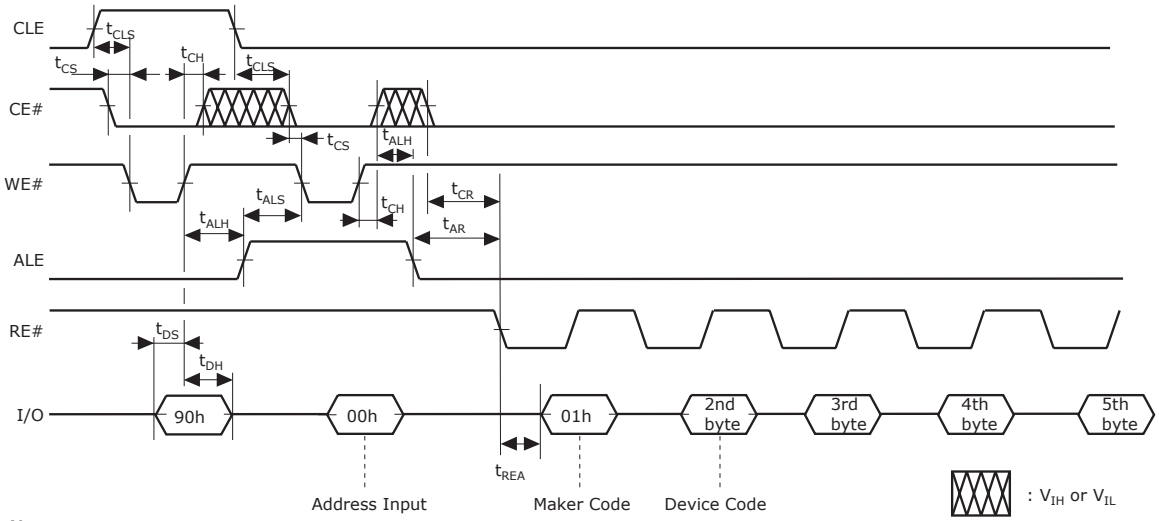
Figure 9.12 Page Duplicate Program Timing Diagram



Note:
CE#, CLE, and ALE are Don't care.

9.1 ID Read

Figure 9.13 ID Read Operation Timing Diagram



Note:
CE#, CLE, and ALE are Don't care.

Table 9.1 ID Byte Settings Summary

Byte	Description		Hex Data
1st Byte	Maker Code		01h
2nd Byte	Device Code 1st Byte	512 Mb (x8)	81h
		512 Mb (x16)	91h
		1 Gb (x8)	A1h
		1 Gb (x16)	B1h
3rd Byte	Device Code 2nd Byte	Model Numbers 50 and 51 (ECC Required)	00h
		Model Numbers 00 and 01	01h
4th Byte	Block Size, Simultaneous Programmed Pages, RFU		00h
5th Byte	Page Size, Spare Size, RFU		22h

Note:
In x16, I/O15 - I/O8 = 00h

Table 9.2 4th ID Byte

Description		I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Block Size: 128 KBytes		X	X	X	X	X	0	0	0
Block Size: 512 KBytes		X	X	X	X	X	0	0	1
Block Size: 2048 KBytes		X	X	X	X	X	0	1	0
Number of simultaneously programmed pages	1	X	X	X	0	0	X	X	X
	2	X	X	X	0	1	X	X	X
	4	X	X	X	1	0	X	X	X
	8	X	X	X	1	1	X	X	X

Table 9.3 5th ID Byte

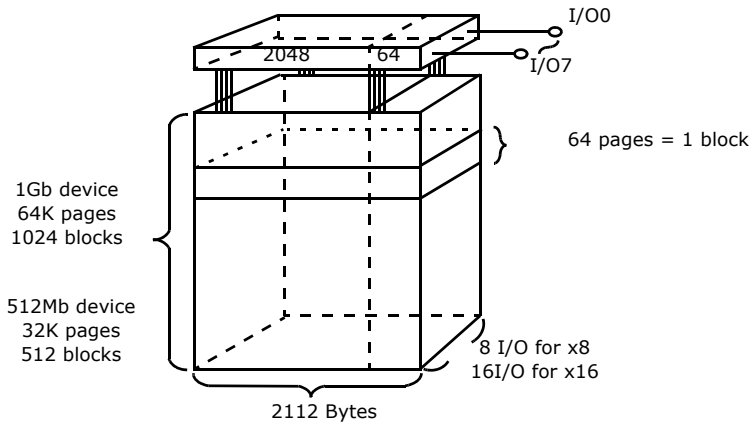
Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size: 512 KBytes	X	X	X	X	X	0	0	0
Page Size: 1024 KBytes	X	X	X	X	X	0	0	1
Page Size: 2048 KBytes	X	X	X	X	X	0	1	0
Page Size: 4096 KBytes	X	X	X	X	X	0	1	1
Page Size: 8192 KBytes	X	X	X	X	X	1	0	0
Spare Size: 0 Bytes	X	X	0	0	0	X	X	X
Spare Size: 8 Bytes	X	X	0	0	1	X	X	X
Spare Size: 16 Bytes	X	X	0	1	0	X	X	X
Spare Size: 32 Bytes	X	X	0	1	1	X	X	X
Spare Size: 64 Bytes	X	X	1	0	0	X	X	X

10. Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

10.1 Array Organization

Figure 10.1 Array Organization



A page consists of 2112 Bytes in which 2048 Bytes are used for main memory storage and 64 Bytes are for redundancy or for other uses.

- 1 page = 2112 Bytes
- 1 block = 2112 Bytes x 64 pages = (128K + 4K) Bytes
- 1Gb density = 2112 Bytes x 64 pages x 1024 blocks

Table 10.1 shows a summary of the addressing for the memory array components.

Table 10.1 Memory Addressing Key

Density	Bus Width	Row Address		Column Address					Blocks
		Block Address	Page Address in Block	Main/Spare Area	Main Page Segment	Main Column Address	Spare Page Segment	Spare Column Address	
1 Gb	x8	A_{27}:A_{18}	A_{17}:A_{12}	A_{11} (0=Main, 1=Spare)	A_{10}:A_9	A_8:A_0	A_5:A_4	A_3:A_0	1024
1 Gb	x16	A_{26}:A_{17}	A_{16}:A_{11}	A_{10} (0=Main, 1=Spare)	A_9:A_8	A_7:A_0	A_4:A_3	A_2:A_0	1024
512 Mb	x8	A_{26}:A_{18}	A_{17}:A_{12}	A_{11} (0=Main, 1=Spare)	A_{10}:A_9	A_8:A_0	A_5:A_4	A_3:A_0	512
512 Mb	x16	A_{25}:A_{17}	A_{16}:A_{11}	A_{10} (0=Main, 1=Spare)	A_9:A_8	A_7:A_0	A_4:A_3	A_2:A_0	512

An address is read through the I/O port over four consecutive clock cycles, as shown in Table 10.2 and Table 10.3. The Notes for Table 10.2 and Table 10.3 are listed below Table 10.3.

Table 10.2 (1Gb) x 8 device

1Gbit	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
2nd Cycle	A_8	A_9	A_{10}	A_{11}	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}
4th Cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}

Table 10.3 (512Mb) x8 Addressing

512Mb	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
2nd Cycle	A_8	A_9	A_{10}	A_{11}	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}
4th Cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	L (Note 1)

Notes:

1. *L = $V_{IL.}$*
2. *A0 to A11:Column address (12 bits for 2,112 Bytes).*
   A12 to A27: Row address, consists of:
   A12 to A17: Page address in block (6 bits for 64 pages).
3. *A18 to A27: Block address (1 Gb device: A18 to A27, 10 bits for 1024 blocks; 512Mb device: A18 to A26, 9 bits for 512 blocks.)*

Table 10.4 (1Gb) x 16 Addressing

1Gb	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8 – I/O15
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	L (Note 1)
2nd Cycle	A_8	A_9	A_{10}	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	L (Note 1)
4th Cycle	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	L (Note 1)

Table 10.5 (512) x 16 Addressing

512Mb	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8 – I/O15
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	L (Note 1)
2nd Cycle	A_8	A_9	A_{10}	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)	L (Note 1)
3rd Cycle	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	L (Note 1)
4th Cycle	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	L (Note 1)	L (Note 1)

Notes:

1. *L = $V_{IL.}$*
2. *A0 to $A1_0$:Column address (11 bits for 1,056 words)*
3. *A11 to A26: Row address, consists of:*
   A11 to A16: Page address in block (6 bits for 64 pages).
   A17 to A26: Block address (1 Gb device: A_{17} to A_{26}: 10 bits for 1024 blocks; 512Mb device: A17 to A25: 9 bits for 512 blocks.)

11. Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read, and Reset are controlled by the thirteen different command operations shown in Table 11.2 on page 25. Address input, command input and data input/output are controlled by the CLE, ALE, CE#, WE#, RE# and WP# signals, as shown in Table 11.1.

Table 11.1 Operation Table

CLE	ALE	CE#	WE#	RE#	PRE	WP#	Mode	
H	L	L	↑	H	X	X	Read Mode	Command Input
L	H	L	↑	H	X	X		Address Input (4 clock cycles)
L	L	X	H	H	X	X	During Read (Busy)	
L	L	L	H	↓	X	X	Sequential Read & Data Output	
H	L	L	↑	H	X	H	Program Mode	Command Input
L	H	L	↑	H	X	H		Address Input (4 clock cycles)
L	L	L	↑	H	X	H	Data Input	
X	X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0 V/V_{CC}	0 V/V_{CC}	Stand-by	

Notes:

1. *H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}*
2. *WP# should be biased to CMOS high or CMOS low for standby.*

Table 11.2 Command Table

Function	1st Cycle	2nd Cycle	Command Accepted During Busy State
Page Read	00h	30h	No
Partial Page Read	00h	31h	No
Read for Page Duplicate	00h	35h	No
ID Read	90h	—	No
Page Program	80h	10h	No
Cache Program	80h	15h	No
Page Duplicate Program	85h	10h	No
Data Input for Column Address Change	85h	—	No
Read for Column Address Change	05h	E0h	No
Block Erase	60h	D0h	No
Reset	FFh	—	Yes
Status Read	70h	—	Yes

Notes:

1. *Random Data Input/Output can be executed in a page or 1/4 page.*
2. *Input of a command other than those specified in Table 11.2 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.*
3. *During the Busy state, input commands are restricted to 70h and FFh.*

Table 11.3 Read Mode Operation Status

Operation	CLE	ALE	CE#	WE#	RE#	I/O0 to I/O15	Power
Output Select	L	L	L	H	L	Data Output	Active
Output Deselect	L	L	X	H	H	High Impedance	Active
Standby	X	X	H	X	X	High Impedance	Standby

Notes:
1. $H = V_{IH}$
2. $L = V_{IL}$
3. $X = V_{IH}$ or V_{IL}

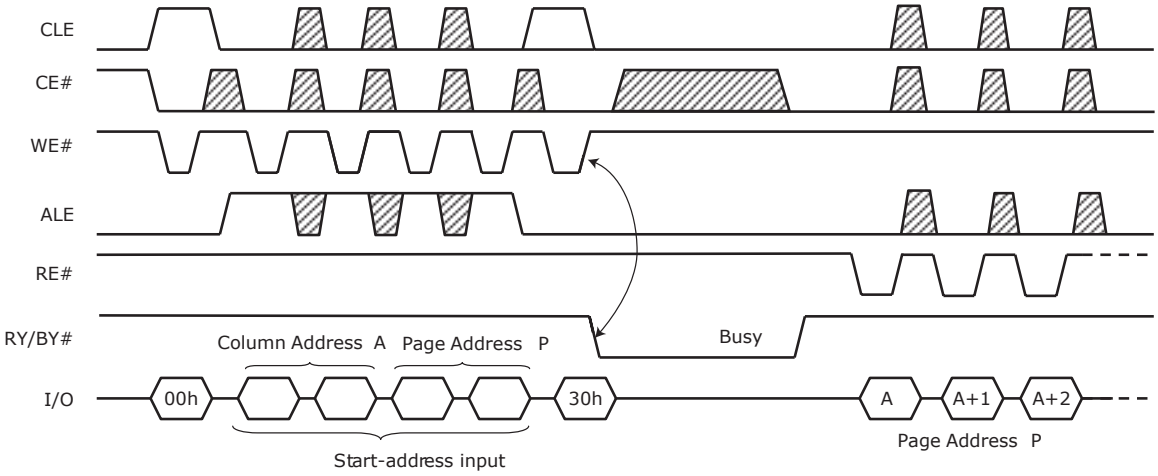
12. Device Operation

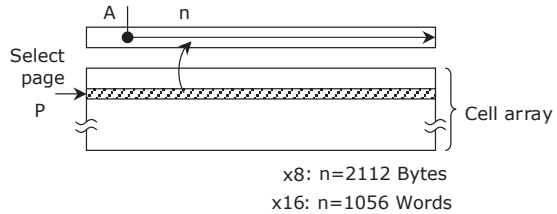
12.1 Read Mode

There are two types of read operations: random read and serial page read. The device defaults to Read mode after power-up or a Reset or may be initiated by writing 00h-30h to the command register along with four address cycles. A partial page read may be initiated by writing 00h-31h to the command register along with the four address cycles. The random data read is enabled by a page or partial page address change. The addressed page of data is loaded into the page register and the completion of the loading process is detected by polling the RY/BY# pin or reading the status register. Once the data is loaded into the page register, it may be read by clocking RE#. The high to low transition of the RE# signal outputs data sequentially, starting with the first selected column address and ending with the last selected column address. Subsequent reads will output the last column address data. See Figure 12.1 for timing details.

The device may output random data in a page instead of the consecutive sequential data upon entering the random data output command. The column address of the next data to be read can be changed to the address which follows the random data output command. The random data output command may be issued multiple times, but must be within the same page.

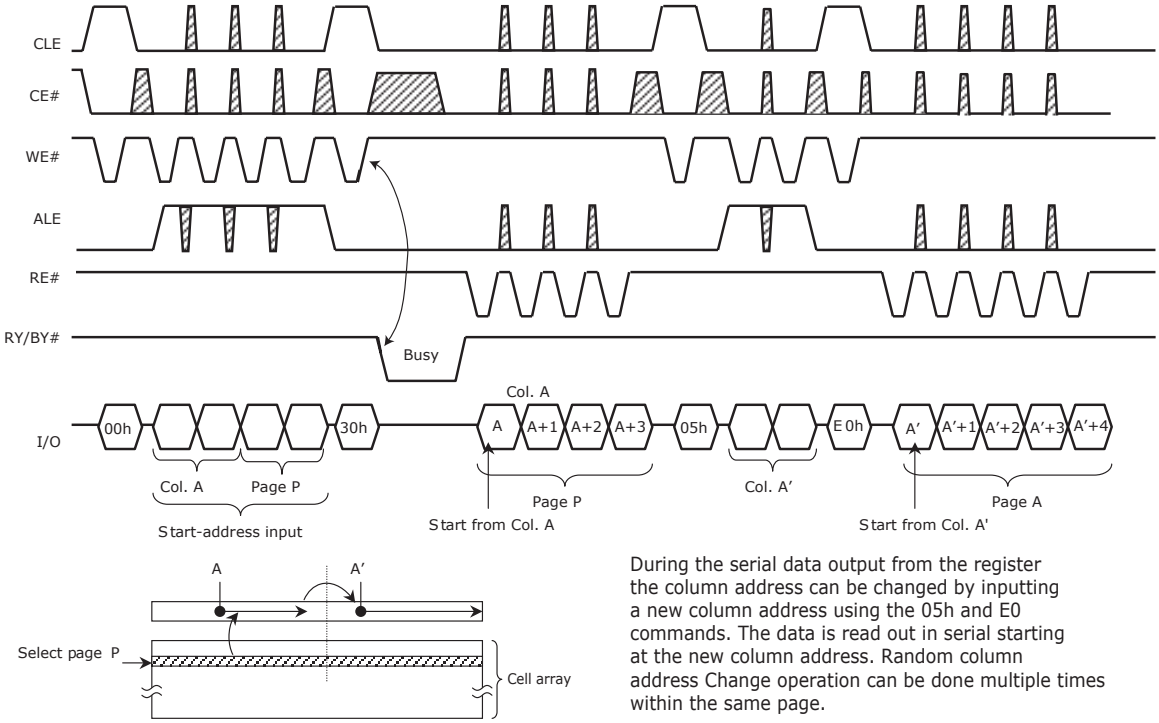
Figure 12.1 Read Mode





A data transfer operation from the cell array to the page buffer starts on the rising edge of WE# in the 30h command input cycle (after the address information has been latched). The device is in Busy state during this transfer period.
After the transfer period the device returns to Ready state. Serial data can be output synchronously with the RE# clock from the start pointer designated in the address input cycle.

Figure 12.2 Column Address Read



12.2 Page Program

The device conducts an Automatic Page Program operation when it receives a 10h Program confirm command after the address and data are input. The sequence of command and address and data input is shown below. (See Figure 12.3.)

Partial page programming is allowed for this device. A page is divisible into eight segments and each segment may be programmed individually or in any combination of segments simultaneously. For example, in x8 devices the first data segment of 512 bytes and the first spare area segment of 16 bytes, are programmable at the same time. Table 12.1 describes the page segments:

Table 12.1 Page Segments

	x8	x16
Data Area	**512 Bytes x 4 Segments / Page**	**512 Bytes x 4 Segments / Page**
1st segment	Column Address 0 to 511	Column Address 0 to 255
2nd segment	Column Address 512 to 1023	Column Address 256 to 511
3rd segment	Column Address 1024 to 1535	Column Address 512 to 767
4th segment	Column Address 1536 to 2047	Column Address 768 to 1023
Spare Area	**16 Bytes x 4 Segments / Page**	**16 Bytes x 4 Segments / Page**
1st segment	Column Address 2048 to 2063	Column Address 1024 to 1031
2nd segment	Column Address 2064 to 2079	Column Address 1032 to 1039
3rd segment	Column Address 2080 to 2095	Column Address 1040 to 1047
4th segment	Column Address 2096 to 2111	Column Address 1048 to 1055

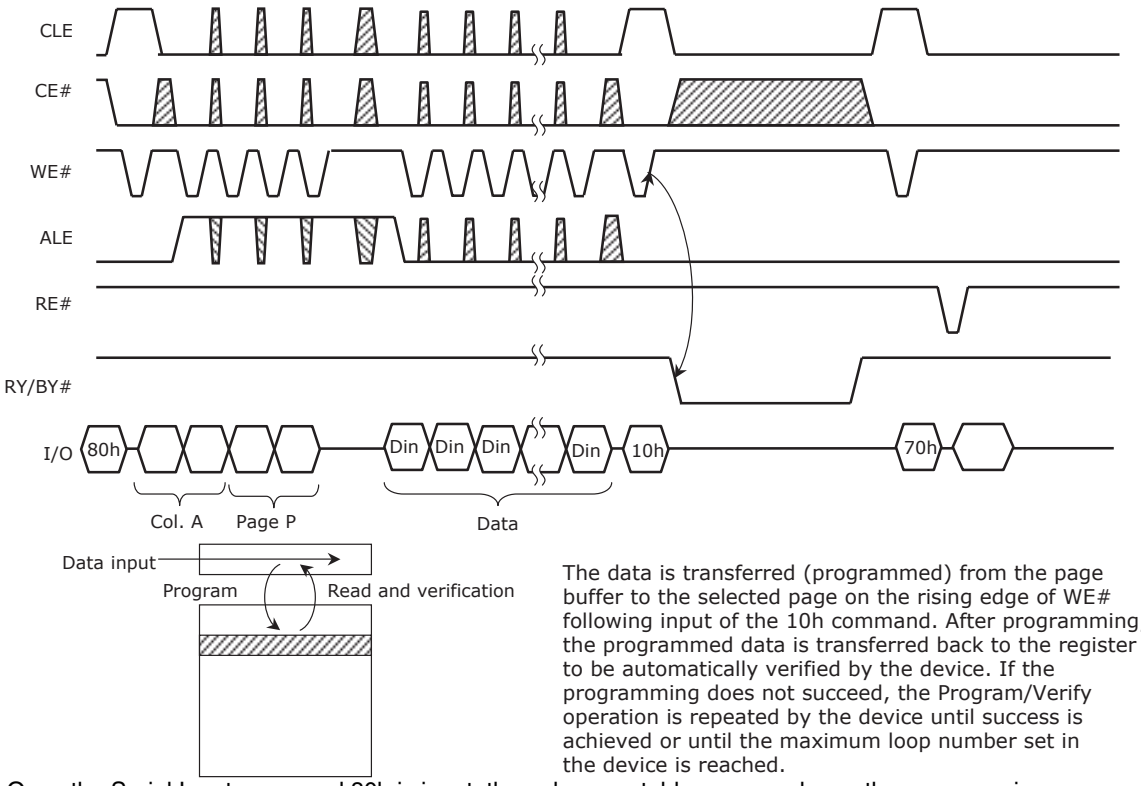
The maximum number of consecutive partial page program operations allowed in the same segment is one. Each of the eight segments may be programmed once before a block erase is required and each of the eight segments is independent with respect to the single program operation allowed.

The device also supports random data programming within a page by using the random data input command (85h). Random data input requires the command to be entered between column addresses during the page program command cycle. Once the new column address is entered, the system can continue the page

program command cycle by entering the page address and the data. The Page Program confirm command (10h) initiates the programming operation.

Once the program operation starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a **program** cycle by monitoring the RY/BY# output, or the Status bit (I/O6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be verified. The internal write verify detects only errors for *1s* that are not successfully programmed to *0s*. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 12.3 Page Program



The data is transferred (programmed) from the page buffer to the selected page on the rising edge of WE# following input of the 10h command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Once the Serial Input command 80h is input, the only acceptable commands are the programming commands 10h, 85h or the Reset command FFh. If any other input command is used, the program operation is not performed and the device must be reset.

Figure 12.4 Serial Input Command Sequence

Note:
If XXX is a command other than 10h, 85h, or FFh, the operation does not execute. When this occurs, the reset command (FFH) must be entered to return the device to a valid state.

12.3 Cache Program

Cache Program is a double buffer scheme for faster programming. The Cache buffer size is identical to the page buffer size (i.e. 2112Byte (x8) or 1056Word (x16) data registers). Data may be written into the cache register while other data stored in the page buffer are programmed into the memory array.

After writing the first set of data up to 2112Byte (x8) or 1056Word (x16) into the cache register, the Cache program command (15h) must be entered instead of the standard Page Program command (10h) in order to free up the cache register and start the internal program operation. To transfer data from the cache register to the data register, the device remains in the Busy state for a short period of time (t_{CBSY}) and has its cache register ready for the next data-input while the internal programming starts with the data loaded into the data

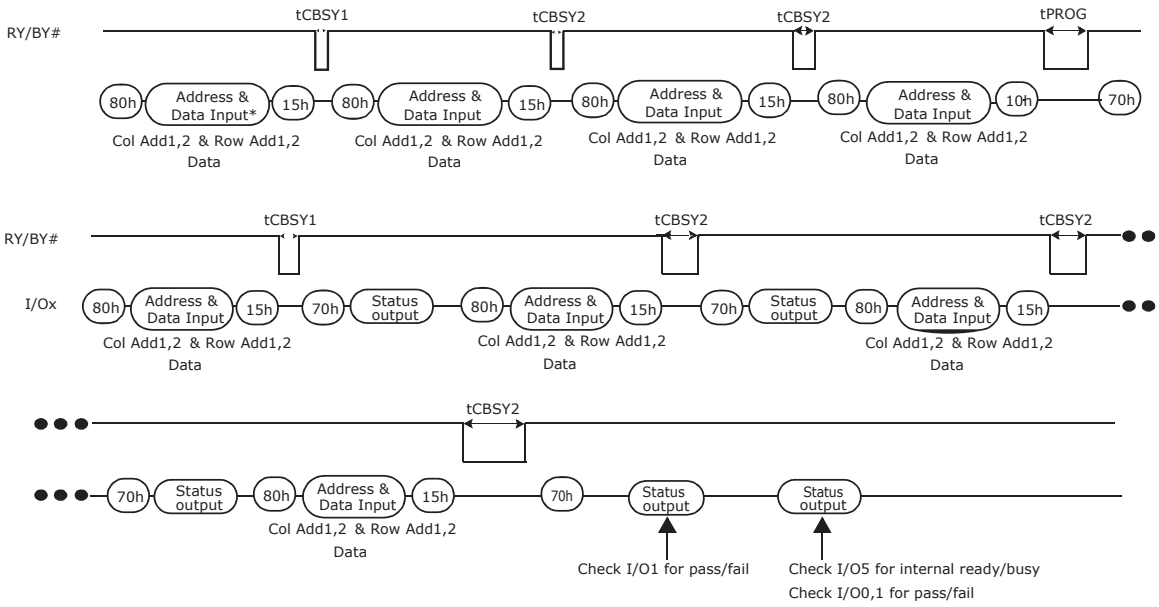
register. The Read Status command (70h) may be issued to verify that the cache register is ready by polling the Cache-Busy status bit (I/O6). Pass/Fail status of the previous page is available upon the return to the Ready state. When the next set of data is input with the Cache Program command, t_{CBSY} is affected by the progress of pending internal programming. The programming of the cache register is initiated only when the pending program cycle is finished and the data register is available for the transfer of data from the cache register. The status bit (I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming.

If the system monitors the progress of programming with RY/BY# only, the last page of the target programming sequence must be programmed with Page Program command (10h). Alternatively, if the last page to be programmed is accomplished using the Cache Program command (15h), status bit (I/O5) must be polled to verify that the last program is actually finished before starting other operations.

Following the Cache Program Command (15h), the pass/fail status information is available as follows:

1. I/O1 returns the status of the previous page (when ready or when the I/O6 bit is changing to a *1*).
2. I/O0 returns the status of the current page (upon true ready, or when the IO5 bit is changing to a *1*).
3. I/O0 and I/O1 may be read together.

Figure 12.5 Cache Program



Note:
Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula: t_{PROG} = Program time of last page + program time of the (last -1) page - (program command time + data loading time of last page).

12.4 Page Duplicate Program

The Page Duplicate program is configured to quickly and efficiently rewrite data stored in one full page (no partial page) without utilizing an external memory. Since the time-consuming serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the block also needs to be copied to the newly assigned free block. A Page Duplicate program operation is performed by first initiating a read operation with command 35h and the address of the source which then duplicates the whole 2112Byte (x8) or 1056Word (x16) data into the internal data buffer. As soon as the device is ready, the Program Confirm command (10h) is required to actually begin the programming operation to the address of the destination page. Once the Page Duplicate Program is finished, any additional partial page programming into the copied pages is prohibited before erasure. The data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 12.6 on page 30. Page data duplicates directly to another Page in a Block.

Figure 12.6 Page Duplicate Program Operation

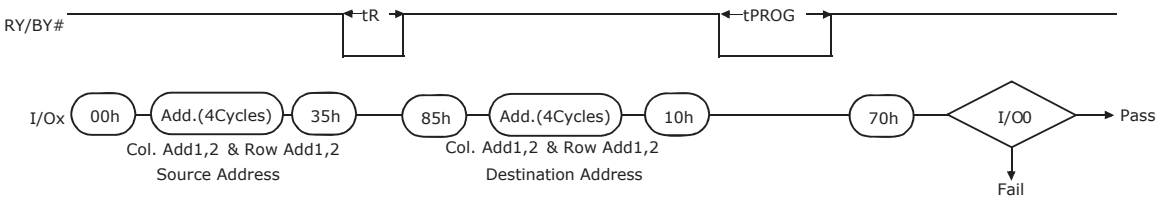
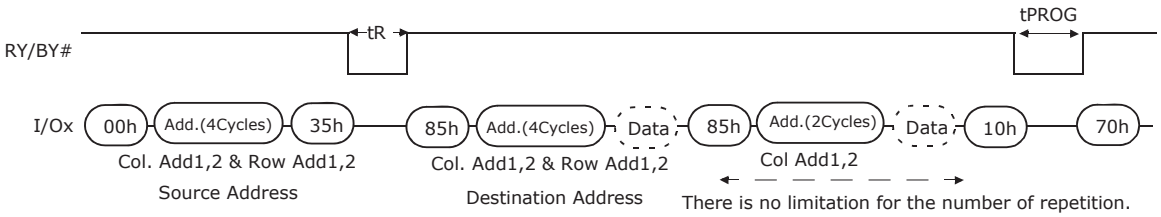


Figure 12.7 Page Duplicate Program Operation with Random Data Input

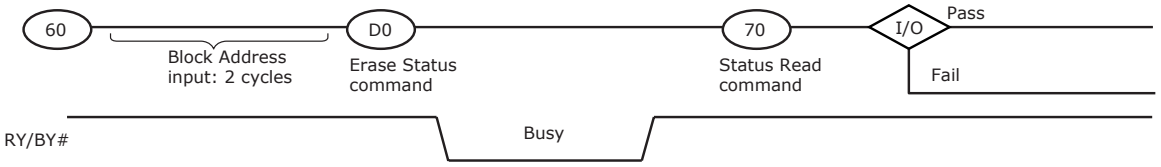


12.5 Block Erase

The Block Erase process starts with the block erase setup command 60h, followed by two cycles of row address, followed by the block erase execute command D0h. Note that the page address part of the row address is ignored.

The Block Erase operation starts on the rising edge of WE# after the Erase Start command D0h which follows the Erase Setup command 60h. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.

Figure 12.8 Block Erase



12.6 Write Operation Status

The device provides a RY/BY# output pin and Status Register bits to determine the status of a write operation. The status register bits can be used to determine which stage the write operation is in.

12.7 Status Read

The device contains a Status Register which may be read to find out whether a program or erase operation is completed, and whether the program or erase operation completed successfully. After writing a 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. The control by two lines allows the system to poll the progress of each device in multiple device connection even if the RY/BY# pins are common wired. RE# or CE# does not have to be toggled for update status. Refer to Table 12.2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles. The Status Register clears after another valid command is entered, excluding a status read. An application example with multiple devices is shown in Figure 12.9.

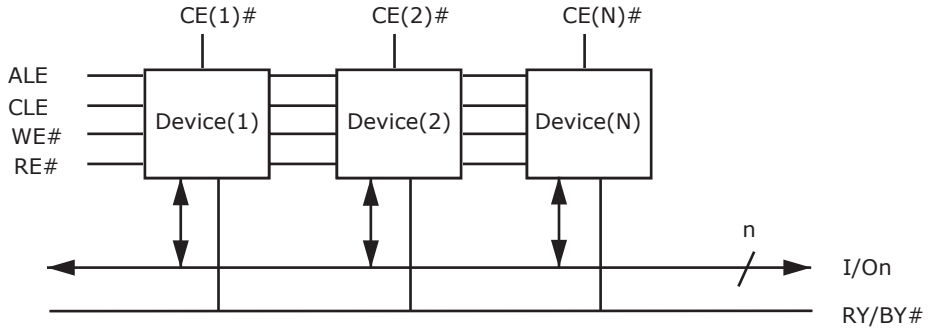
Table 12.2 Status Output Table

I/O	During Program or Erase Operation	Page Program	Block Erase	Cache Program	Read	Definition
I/O0	Reserved	Pass/Fail	Pass/Fail	Pass/Fail(N)	Reserved	0 = Pass; 1 = Fail
I/O1	Reserved	Reserved	Reserved	Pass/Fail(N-1)	Reserved	0 = Pass; 1 = Fail
I/O2	Reserved	Normal	Normal	Normal	Normal	0 = Normal
I/O3	Reserved	Reserved	Reserved	Reserved	Reserved	
I/O4	Reserved	Reserved	Reserved	Reserved	Reserved	
I/O5	Busy	True Ready/Busy	Ready/Busy	True Ready/Busy	Ready/Busy	0 = Busy; 1 = Ready
I/O6	Busy	Cache Ready/Busy	Ready/Busy	Cache Ready/Busy	Ready/Busy	0 = Busy; 1 = Ready
I/O7	Reserved	Write Protect	Write Protect	Write Protect	Write Protect	0 = Protected; 1 = Unprotected

Notes:

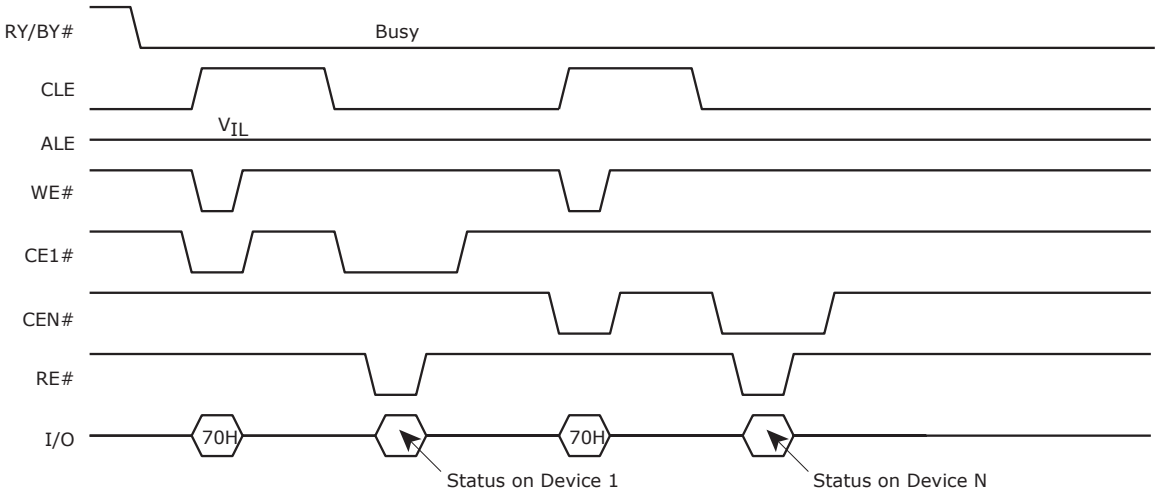
1. *True Ready/Busy represents internal program operation status which is being executed in cache program mode.*
2. *I/Os defined 'Not use' are recommended to be masked out when Read Status in being executed.*

Figure 12.9 Multiple Devices



If the RY/BY# pin signals from multiple devices are wired together as shown in Figure 12.9, the Status Read function can be used to determine the status of each individual device.

Figure 12.10 Status Read Timing Application Example

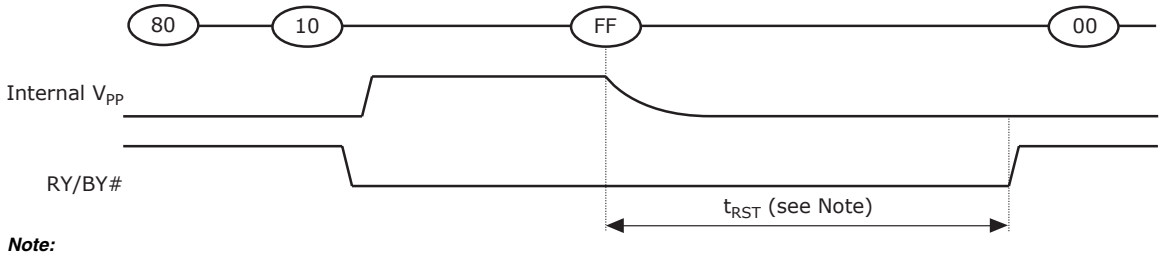


12.8 Reset

The Reset mode aborts all operations in progress including read, erase and program. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters standby. Any attempted memory data alteration is invalidated if interrupted by a reset command.

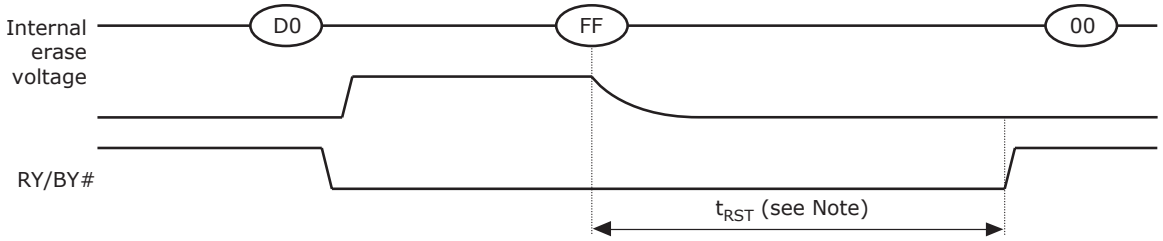
The response to an *FFh* Reset command input during the various device operations is shown in Figure 12.11 to Figure 12.15.

Figure 12.11 Reset (FFh) Command Input During Programming



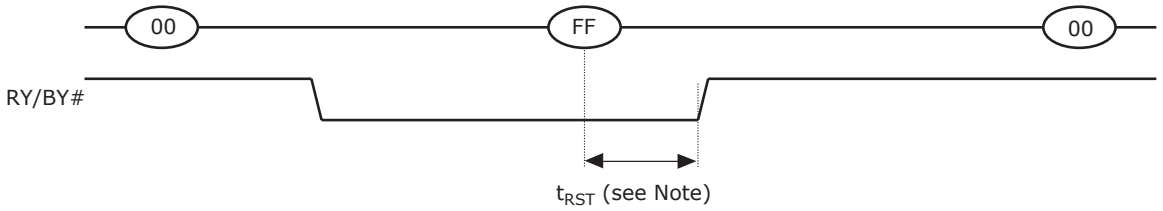
Note:
The reset time (t_{RST}) is not the same for program, erase, and read operations.

Figure 12.12 Reset (FFh) Command Input During Erasing



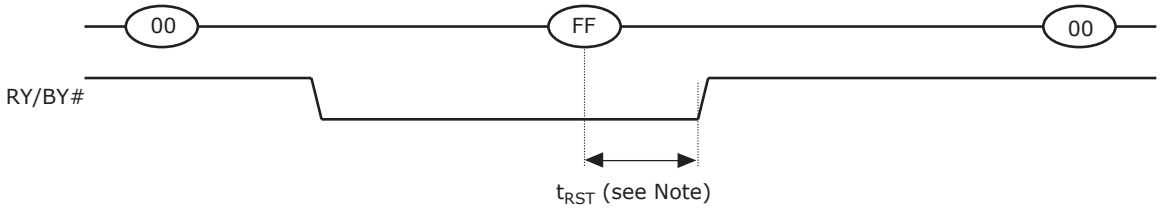
Note:
The reset time (t_{RST}) is not the same for program, erase, and read operations.

Figure 12.13 Reset (FFh) Command Input During a Read Operation



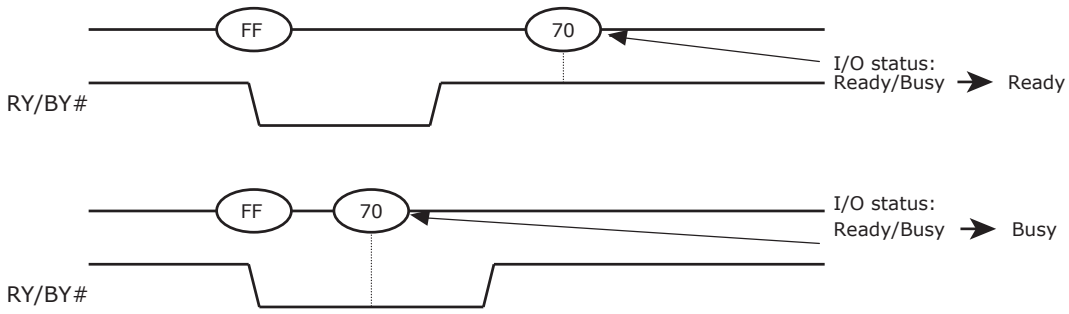
Note:
The reset time (t_{RST}) is not the same for program, erase, and read operations.

Figure 12.14 Reset (FFh) Command During Operations Other Than Program, Erase, or Read



Note:
The reset time (t_{RST}) is not the same for program, erase, and read operations.

Figure 12.15 Status Read Command (70h) Input After a Reset



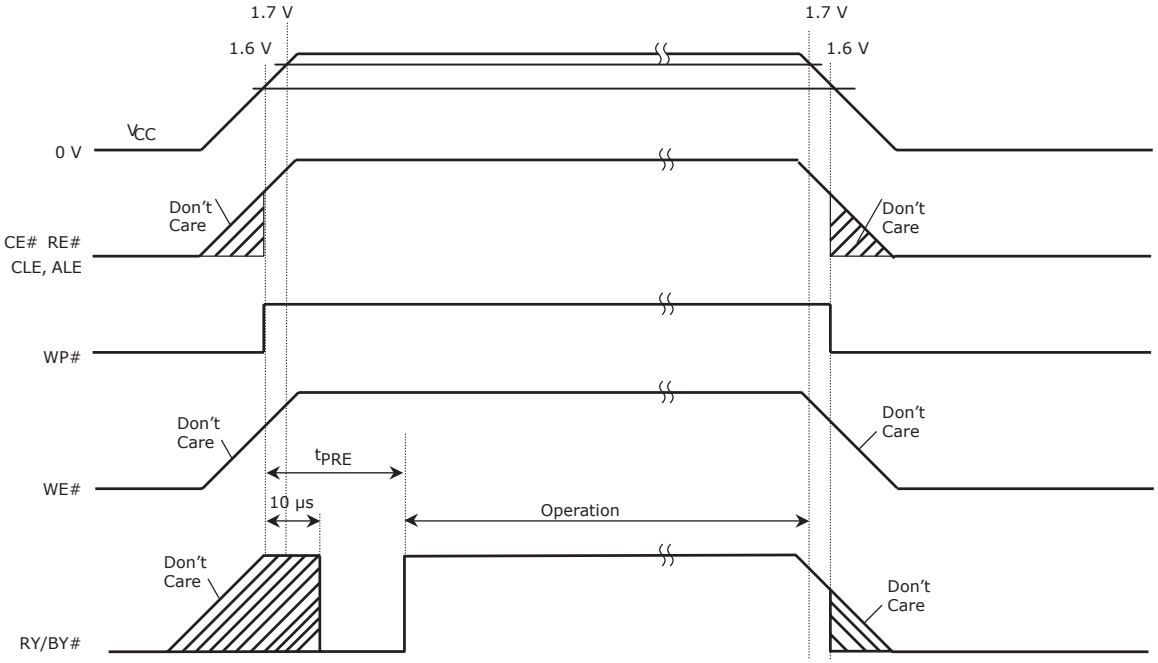
13. Application Notes

13.1 Power On/Off Sequence and Power-On Read Enable

13.1.1 Power-On/Off Sequence

The WP# signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary. The WP# signal may be negated any time after the V_{CC} reaches 1.6 V and the CE# signal is kept high in power up sequence. A reset command issued during the power up sequence is ignored.

Figure 13.1 Power-On/Off Sequence



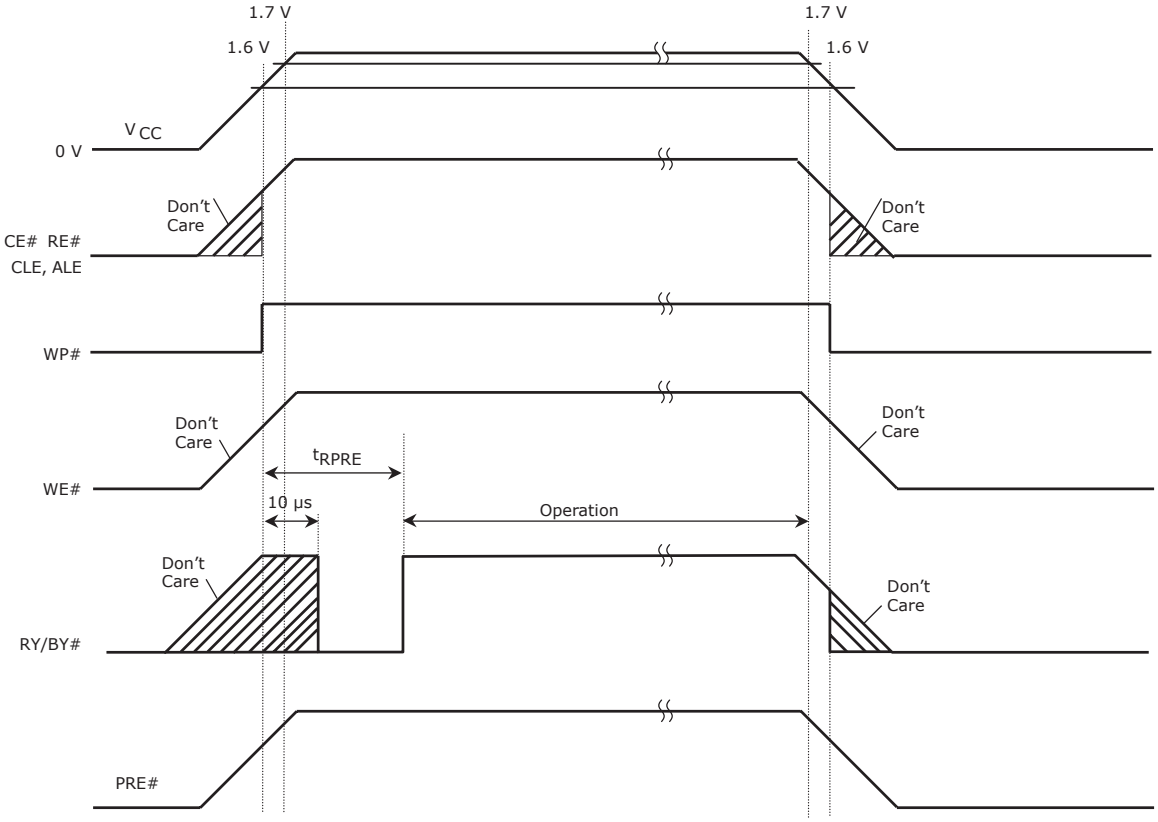
For stable operation, it is recommended to start accessing the device 200 µs after V_{CC} becomes 1.6 V. There is no restriction regarding the V_{CC} ramp rate.

13.1.2 Power-On Read Enable

Power on read is a feature for certain architectures that requires the system to read data from page *0* without a command sequence on power-up. To enable power on read, PRE must be tied to V_{CC} to ensure a simultaneous ramp rate. Please refer to the following waveform. Page zero data is read from the memory array to the page buffer without any command and address input sequence following power-on. The function will be performed when V_{CC} attains about 1.6 V. The PRE pin controls activation of auto-page read function.

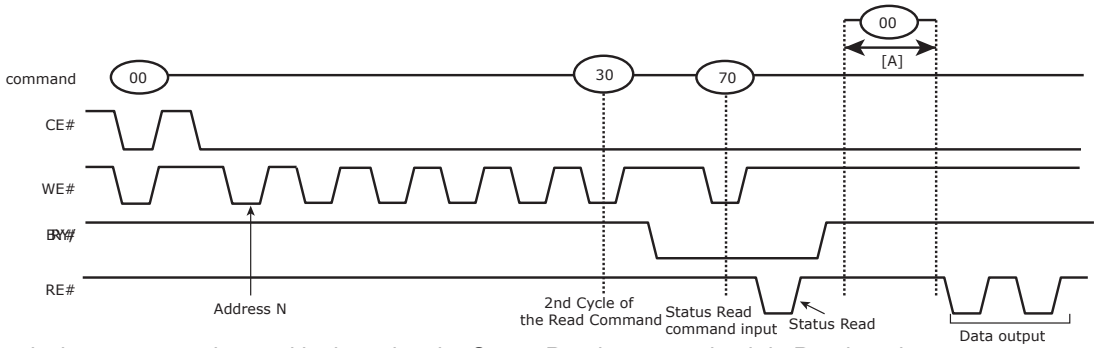
Serial access may begin after t_{RPRE}. A reset command issued during the power-on read enable is acceptable. Figure 13.2 shows the timing diagram.

Figure 13.2 Power-On Auto-read Enable



13.2 Status Read During a Read Operation

Figure 13.3 Status Read During a Read Operation

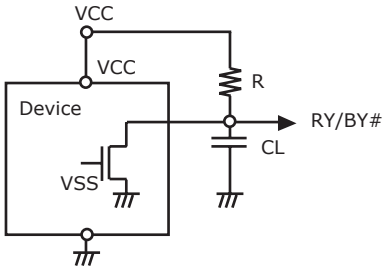


The device status can be read by inputting the Status Read command 70h in Read mode.

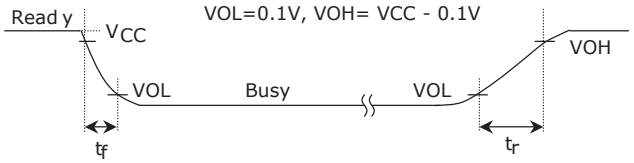
Once the device is set to Status Read mode by a 70h command, the device will not return to Read mode. However, when the Read command 00h is input during [A], the Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

A pull-up resistor must be used for termination because the RY/BY# buffer consists of an open drain circuit.

Figure 13.4 RY/BY#: Termination for the Ready/Busy Pin (RY/BY#)



This data may vary from device to device. We recommend that you use this data as a reference when selecting a resistor value.



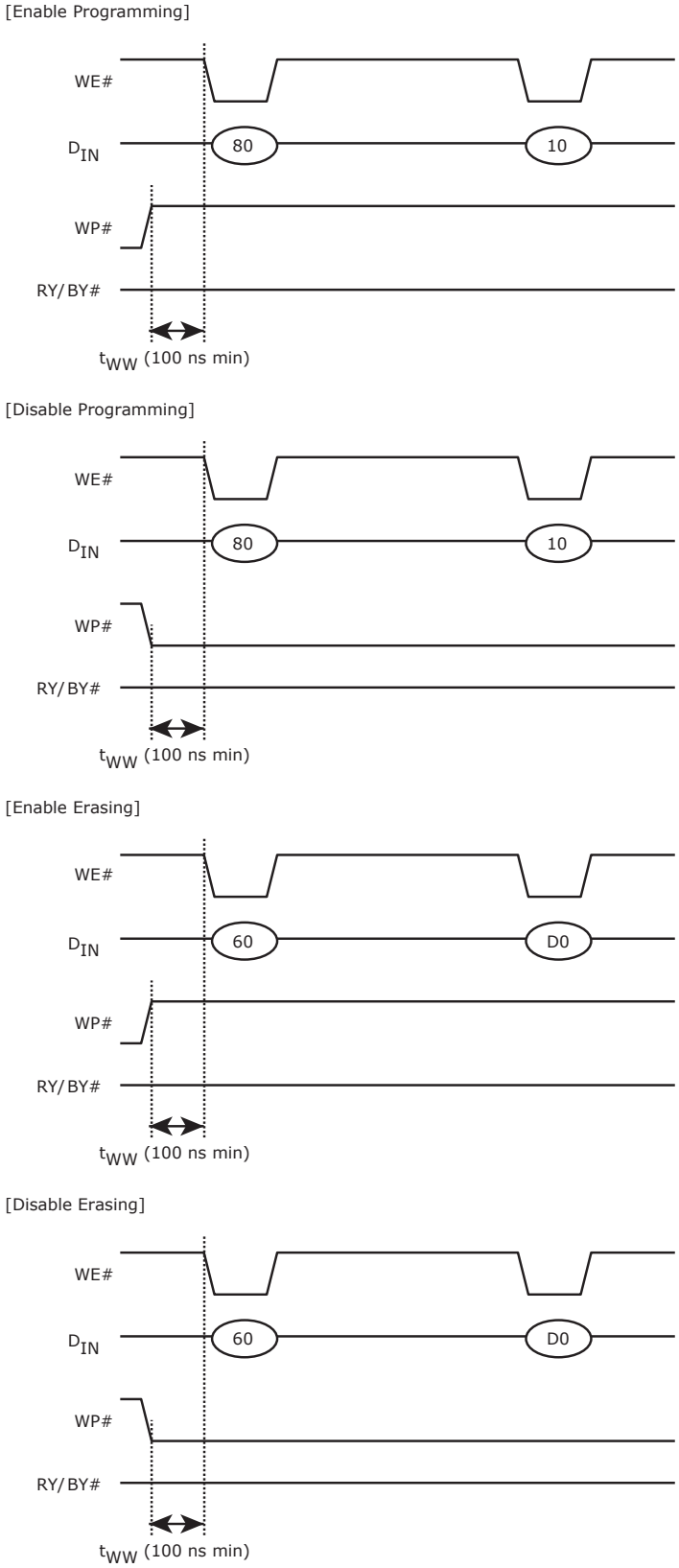
$$R = \frac{VCC\ max - VOL}{IOL + IL}$$

$$= \frac{1.95\ V}{3\ mA + IL}$$

13.2.1 When WP# Signal Goes Low

Holding the WP# pin low protects the device during power transitions. If WP# is low during the program/erase command input period, the device is protected and does not enter the program/erase operation. If WP# is high during the program/erase command input period, the device can execute the program/erase operation. The user should keep the WP# pin either high or low during the complete command & program/erase operation. The operations are enabled and disabled as shown in the following timing diagrams:

Figure 13.5 WP# Signal—Low



13.2.2 CE# Don’t Care Feature

CE# does not need to be continuously asserted across command and address write operations or during busy periods as was required by some earlier generation NAND interface devices.

14. Revision History

Section	Description
Revision A (January 3, 2005)	
	Initial release
Revision A1 (May 16, 2005)	
Performance Characteristics table	Updated specifications.
Program and Erase Performance table	Updated entire table
Connection Diagrams	Updated all diagrams
Block Diagram	Corrected the RY/BY# command
DC Characteristics table	Added standard and low power mode specifications to: I_{CC4} and I_{CC5}
AC Characteristics and Recommended Operating Conditions table	Updated Min. specifications for: t_{WP}, t_{DS}, and t_{DH}
Program and Erase Characteristics table	Updated entire table
ID Definition table	Updated entire table
x8 Array Organization	Updated the figure
x16 Array Organization	Updated the figure
When WP# Signal Goes Low	Updated section
Revision A2 (July 6, 2005)	
Front Page	Added 100% Valid Blocks statement
Ordering Information	Revised and corrected various parameters Added model numbers 02 and 03 Removed Industrial temperature grade
DC Characteristics Table	Revised various parameters
AC Characteristics Table	Revised and added various timing parameters
Program and Erase Characteristics Table	Revised t_{CBSY1} and t_{CBSY2} Corrected P/E Specification
Byte Tables	Removed 7th ID Byte table Updated Device ID Bytes 2, 3, 4, and 5
Pin Names	Removed V_{IO} pin Removed RY/BY#1 and RY/BY#2
Command Table	Added Pipeline Read—Full Page no additional requests command
Pipeline Read	Revised feature description and timing diagram
Reset After Power-on	Removed section
Timing Diagrams	Corrected multiple timing diagrams
Capacitance Table	Updated the entire table
Valid Blocks Table	Updated the entire table
Power-on Read Enable	Added Section and timing diagrams
Revision A3 (September 12, 2005)	
Title	Added ECC-free
Connection Diagrams	Updated entire diagram
Program and Erase Characteristics	Changed various program and erase specifications
Distinctive Characteristics	Changed data retention value
Schematic Cell Layout and Address Assignment	Added the Memory Addressing Key table
Format	Converted Data Sheet to Standard Format
Spansion Xtreme Mode	Updated and Added Content
Revision A4 (November 11, 2005)	

Section	Description
Global	Removed specifications Removed 2 Gb specifications
Distinctive Characteristics	Changed write performance value
Status Read Output table	Updated table
Reset Timing Diagrams	Changed the t_{RST} values
Power On/Off Sequence	Updated section
Revision A5 (December 16, 2005)	
Valid Blocks Table	Updated Table
DC Characteristics	Removed the specifications for low power mode
Serial Read Cycle Timing Diagram	Corrected Reset Pin Signal
Revision A6 (March 22, 2006)	
Xtreme Mode Command Definitions	Defined WP# State during Block Status Read
Ordering Revisions	Added Model Number descriptions to include boot block product
Programming	Clarified notes on Program/Erase Characteristics table
Program and Erase Characteristics	Changed the Dummy Busy Time During Cache Programming
AC Characteristics	Changed the timing for Partial Page Data Transfer to Memory Cell Array to Register (t_R)
Power on Read Enable	Clarified Power on Read Operation
Revision A7 (August 4, 2006)	
Global	Removed all references to Xtreme Mode
Performance Characteristics	Updated tables
Connection Diagrams	Updated diagram
Capacitance	Added the Capacitance Values for WP# and CE# pins
Valid Blocks	Updated table
DC Characteristics	Changed I_{CC4} and I_{CC5}
AC Characteristics	Changed Read Cycle Timing Parameters Changed Timing for Command Latch Enable and Address Latch Enable
Program and Erase Characteristics	Updated table
Timing Diagrams	Corrected Page Transfer Timing on Page Duplicate Program Timing Diagram
Ordering Information	Update Models Numbers for parts that require ECC

Colophon

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for any use that includes fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for any use where chance of failure is intolerable (i.e., submersible repeater and artificial satellite). Please note that Spansion will not be liable to you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the US Export Administration Regulations or the applicable laws of any other country, the prior authorization by the respective government entity will be required for export of those products.

Trademarks and Notice

The contents of this document are subject to change without notice. This document may contain information on a Spansion product under development by Spansion. Spansion reserves the right to change or discontinue work on any product without notice. The information in this document is provided as is without warranty or guarantee of any kind as to its accuracy, completeness, operability, fitness for particular purpose, merchantability, non-infringement of third-party rights, or any other warranty, express, implied, or statutory. Spansion assumes no liability for any damages of any kind arising out of the use of the information in this document.