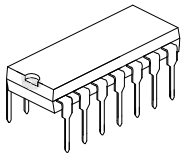
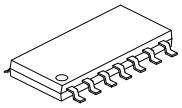
3-CHANNEL SECONDARY SUPERVISOR



DIP-14



SOP-14

■ DESCRIPTION

UTC **S3526** is used for switching power supply system. UTC **S3526** provides protection functions, over-voltage protection, over-current protection, under-voltage protection and power good signal generating.

OVP/UVP (Over-Voltage/Under-Voltage Protection) monitors triple 12V to protect our power supply and PC, FPO goes to high when one of these supply voltages exceeds their normal operation voltage range.

UTC **S3526** OCP (Over Current Protection) monitors IS12A, IS12B and IS12C input current sense by using smart comparator circuit to make the point setting through sense resistor is more exact and easy.

An additional latch protection input pin provides the flexibility for design protection circuit.

UTC **S3526** provides the fault protection latch (FPOB), the power good output (PGO), the PSONB control and the power good input control pin (PGI).

■ FEATURES

* Over/Under-voltage protection
* Over-current protection
* Additional protection input
* Fault protection output with open drain output stage
* Open drain power good output signal for power good input
* 300ms power good delay
* 75ms delay for UV/OC protection
* 38ms PSON control de-bounce
* Wide power supply range (3.8V~16V)
* Special care for AC power off

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
S3526L-D14-T	S3526G-D14-T	DIP-14	Tube
S3526L-S14-R	S3526G-S14-R	SOP-14	Tape Reel

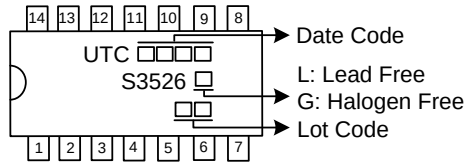
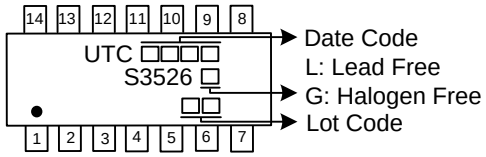
S3526G-D14-T

(1)Packing Type — (1) T: Tube, R: Tape Reel

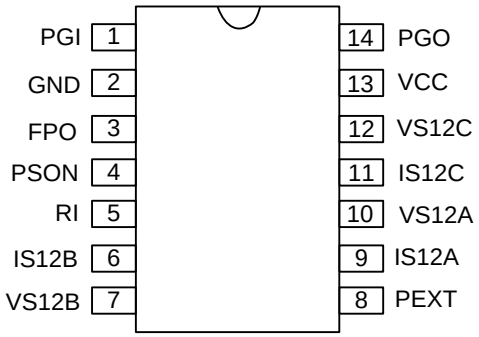
(2)Package Type — (2) D14: DIP-14, S14: SOP-14

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

DIP-14	SOP-14
	

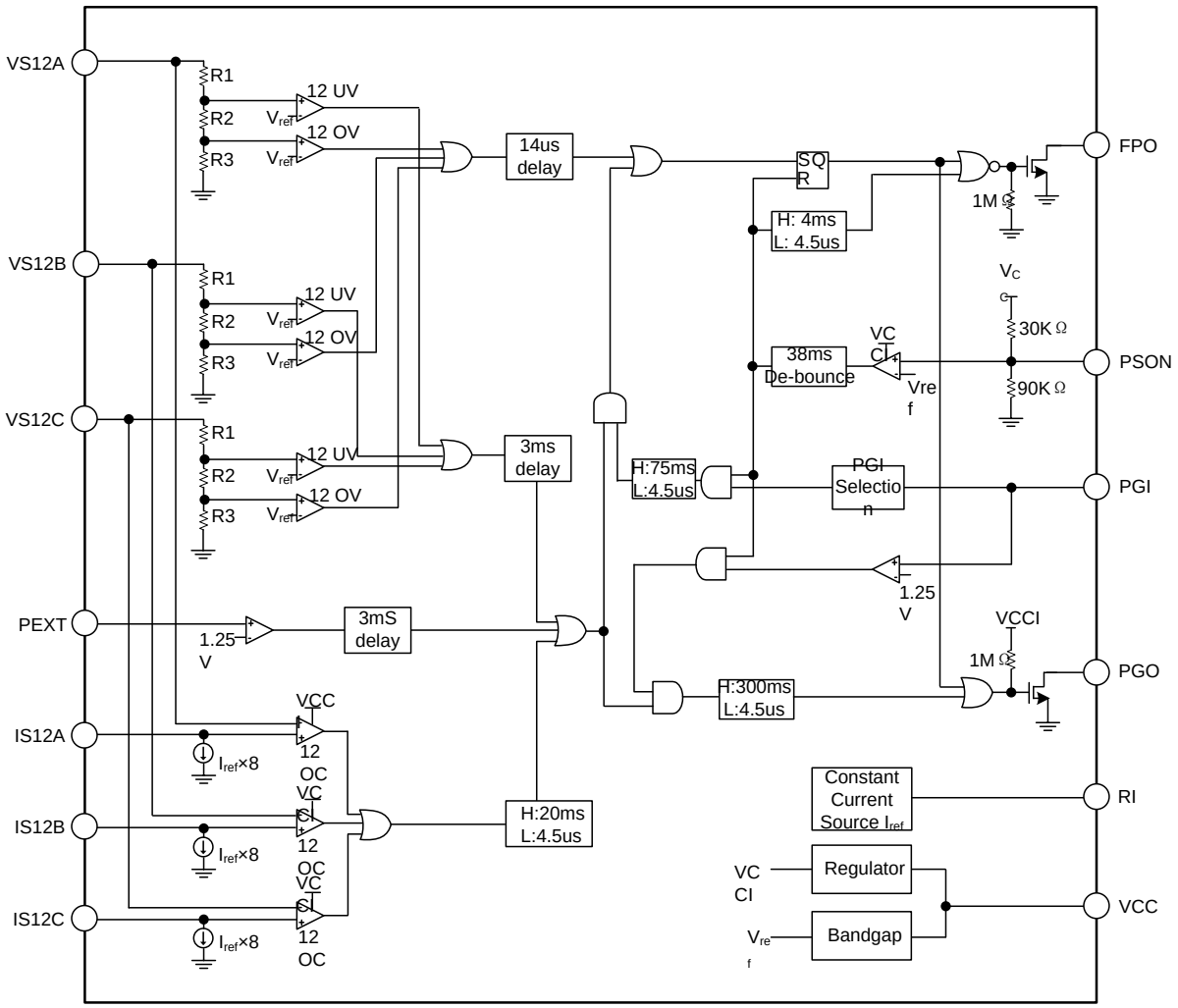
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	PGI	Power good input signal pin
2	GND	Ground
3	FPO	Inverted fault protection output ,open drain output stage
4	PSON	Remote ON/OFF control input pin
5	RI	Current sense setting
6	IS12B	12V(2) over current protection input pin
7	VS12B	12V(2) over/under voltage protection input pin
8	PEXT	External protection detect input pin
9	IS12A	12V(1) over current protection input pin
10	VS12A	12V(1) over/under voltage protection input pin
11	IS12C	12V(3) over current protection input pin
12	VS12C	12V(3) over/under voltage protection input pin
13	V_{CC}	Power supply
14	PGO	Power good output signal pin , open drain output stage

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Note 1)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	V_{CC}	-0.5 ~ +16.0	V
Input Voltage Range	VS12A, VS12B, VS12C, IS12A,IS12B, IS12C	V_{IN}	-0.5 ~ +16.0	V
	PEXT		-0.5 ~ +7.0	V
	PGI		-0.5 ~ +16.0	V
	PSON		-0.5 ~ +V_{CC}+0.5	V
Output Voltage Range	FPO	V_{OUT}	-0.5 ~ +V_{CC}+0.5	V
	PGO		-0.5 ~ V_{CC}+0.5	V
Output Current for RI	R_I	I_{RI}	12.5 ~ 62.5	μA
ESD Susceptibility (Note 2)	PSON, PGO	V_{ESD}	>2K	V
	FPOB, PGI , VS12A, VS12B		>2K	V
	VS12C, IS12A,IS12B, IS12C		>2K	V
	Others		>2K	V
Storage Temperature		T_{STG}	-40~+125	℃
Operating Temperature		T_{OPR}	-30~+90	℃

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Human Body Model (HBM).

■ ELECTRICAL CHARACTERISTICS V_{CC}=12V, T_A = 25℃ (unless otherwise specified)

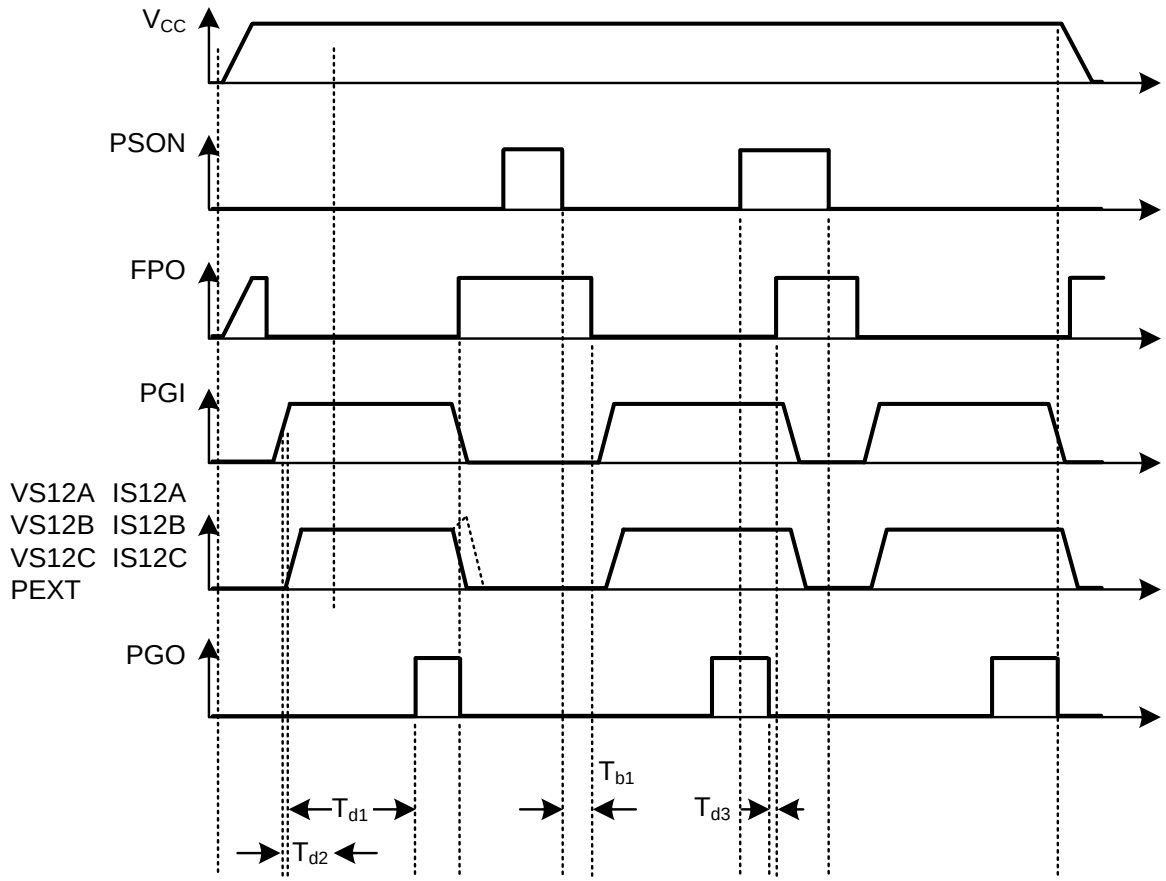
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Section						
Supply Voltage	V_{CC}		3.8	5.0	16.0	V
Supply Current	I_{CC}	V_{PSON}= 5V		4.5	6.0	mA
Power On Reset Threshold Voltage	V_{POR}		3.0	3.4	3.8	V
Power On Reset Hysteresis	V_{HYST}		-0.15	-0.30	-0.45	V
Over-Voltage Section						
VS12A/B/C Over-Voltage Threshold	V_{OV}		13.4	14.0	14.6	V
Under-Voltage Section						
VS12A/B/C Under-Voltage Threshold	V_{UV}		10.3	10.8	11.3	V
PSON, Analog Input						
Threshold Voltage (High)	V_H		1.40	1.50	1.60	V
Threshold Voltage (Low)	V_L		0.85		1.20	V
Leakage Current	I_{PSON}	R_{PSON}=100Ω			550	μA
PGI, Analog Input						
Threshold Voltage for start T_{d1}	V_{TH1}		1.15	1.25	1.35	V
Threshold Voltage for start T_{d2}	V_{TH2}		0.60	0.63	0.75	V
Threshold Voltage for mask UV	V_{TH3}		1.15	1.25	1.35	V
Threshold Voltage for mask OC	V_{TH4}		0.15	0.25	0.35	V
Hysteresis	V_{HYST} (Note 1)		+/-20	+/-50	+/-80	mV
PGO, Open Drain Digital Output						
Leakage Current	I_{LKG}	V_{PGO}=5V			5	μA
Low Level Output Voltage	V_{OL}	I_{SINK}=10mA			0.3	V
Over-Current Section						
VS12A/B/C Offset Voltage	V_{OS}		-5	0	+5	mV
Constant Isink Current	I_{SINK}		140	160	180	μA

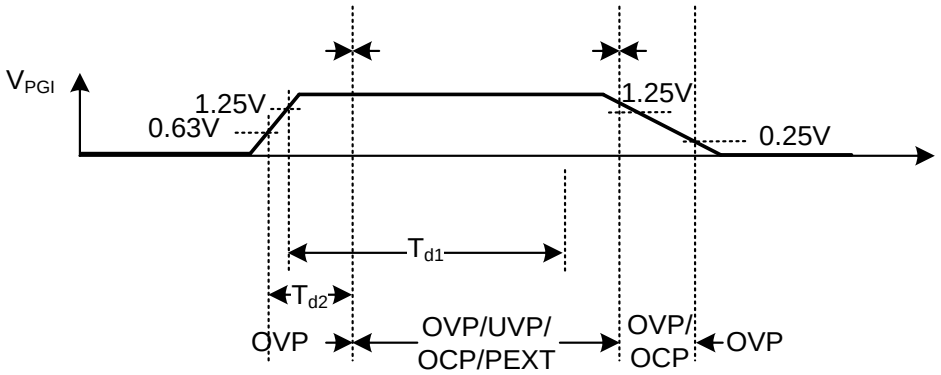
■ ELECTRICAL CHARACTERISTICS V_{CC}=12V, T_A = 25℃ (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FPO, Open Drain Digital Output						
Leakage Current	I_{LKG}	V_{PGO}=5V			5	μA
Low Level Output Voltage	V_{OL}	I_{SINK}=20mA			0.3	V
External Protection Detect Section						
Threshold	V_{TH}		1.20	1.25	1.30	V
Hysteresis	V_{HYST}		+/-20	+/-50	+/-80	mV
Switching Characteristics, V_{CC}=12V, T_A = 25°C						
PGI to PGO Delay Time	T_{d1}		200	300	400	ms
Short Circuit Delay Time	T_{d2}		49	75	100	ms
PGO to FPO Delay Time	T_{d3}		2	4	6	ms
Under Voltage Delay Time	T_{d4}		2.4	3	3.6	ms
Over Current Delay Time	T_{d5}		13	20	27	ms
Over Voltage Delay Time	T_{d6}		9	14	19	μs
PEXT Delay Time	T_{d7}		2.4	3	3.6	ms
PSON De-bounce Time	T_{b1}		24	38	52	ms
PGO Noise De-glitch Time	T_{b2}		47	73	100	μs

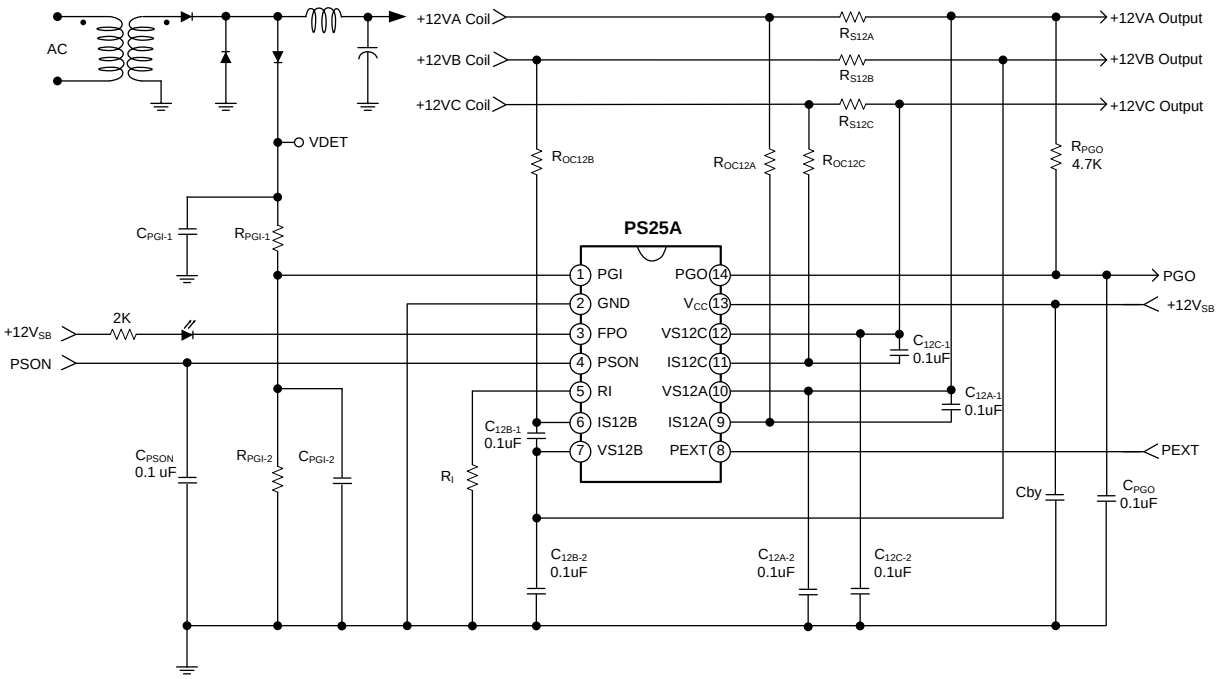
Note: All of the comparator for PGI input in block diagram..

■ TIMING CHART





■ TYPICAL APPLICATION CIRCUIT



Notes 1. Zener diode or resistor or both of them can be used in component X.

2. The bypass capacitor C_{by} suggests to be 0.1μF~ 10μF and layout nearby pin V_{CC}.

3. The recommend sense values of R_{S12A}, R_{S12B} are≥0.002Ω.

4. Over-Current Protection design example:

(1) $I_{ref} = 20\mu A, R_I = \frac{V_{RI}}{I_{RI}} = \frac{1.25}{20u} = 62.5k\Omega$

(2) $R_{S5} = 0.002\Omega, \Delta V_{5V} = 0.002 * I_{5V} = R_{OC5} * 8 * I_{ref}$

(3)If +12V OCP trip point is 20A, $R_{OC5} = \frac{0.002 * 20}{8 * 20u} = 250\Omega$