

**Descriptions**

The S3842, high performance current mode controller, Provides the necessary features to off-line and DC-DC fixed frequency current control applications offering the designer a cost effective solution with minimal external components. Internally protection circuitry includes built-in input and reference under-voltage lockout and current limiting with hysteresis. Also other characteristics of internal circuit provide improved line regulation, enhanced load response, trimmed oscillation for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator and totempole output designed to source and sink high peak current from a capacitive load such as the gate of a power MOSFET.

**Features**

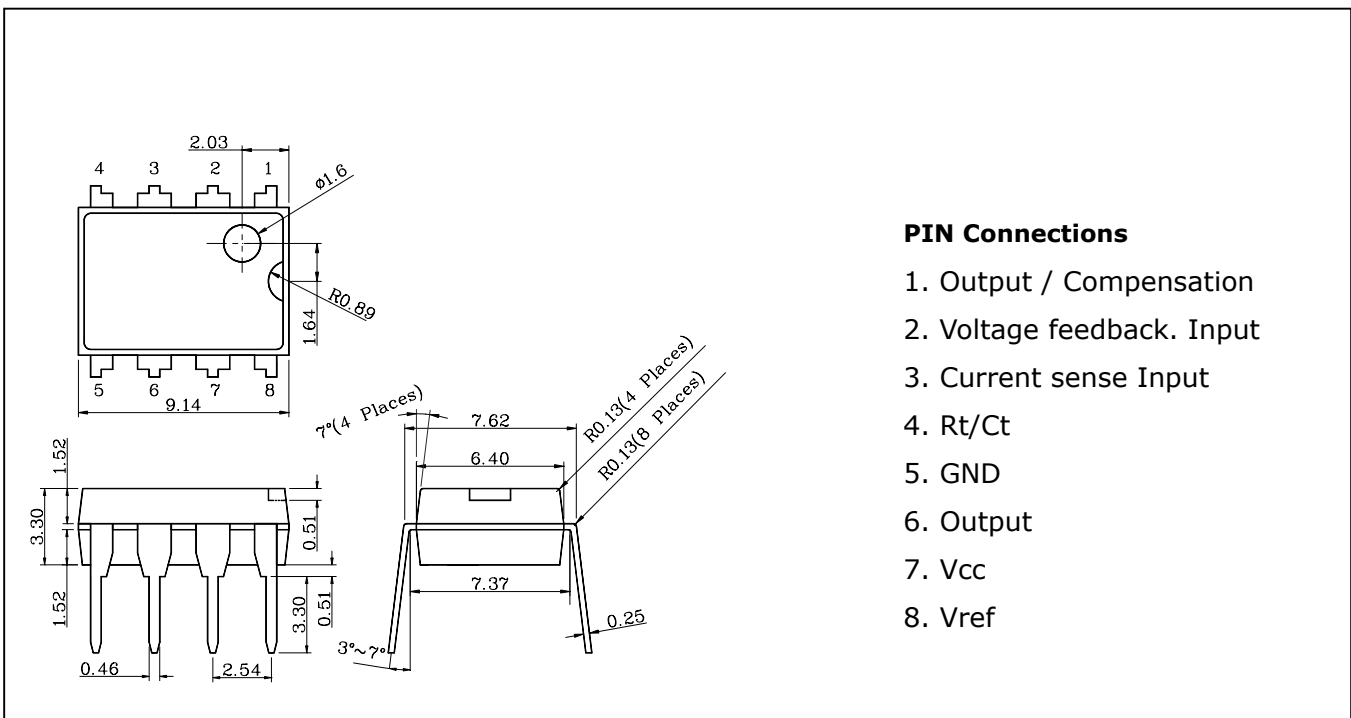
- Optimized for off-line control
- Low start up and operating current
- Pulse by pulse current limiting
- Enhanced load response characteristic
- Current mode operation to 500 kHz
- Under voltage lockout with 6V hysteresis
- Internally trimmed bandgap reference about 5V
- Automatic feed forward compensation

**Ordering Information**

Type NO.	Marking	Package Code
S3842P	S3842P	DIP-8

**Outline Dimensions**

**unit : mm**



## Absolute Maximum Ratings

T<sub>a</sub>=25°C

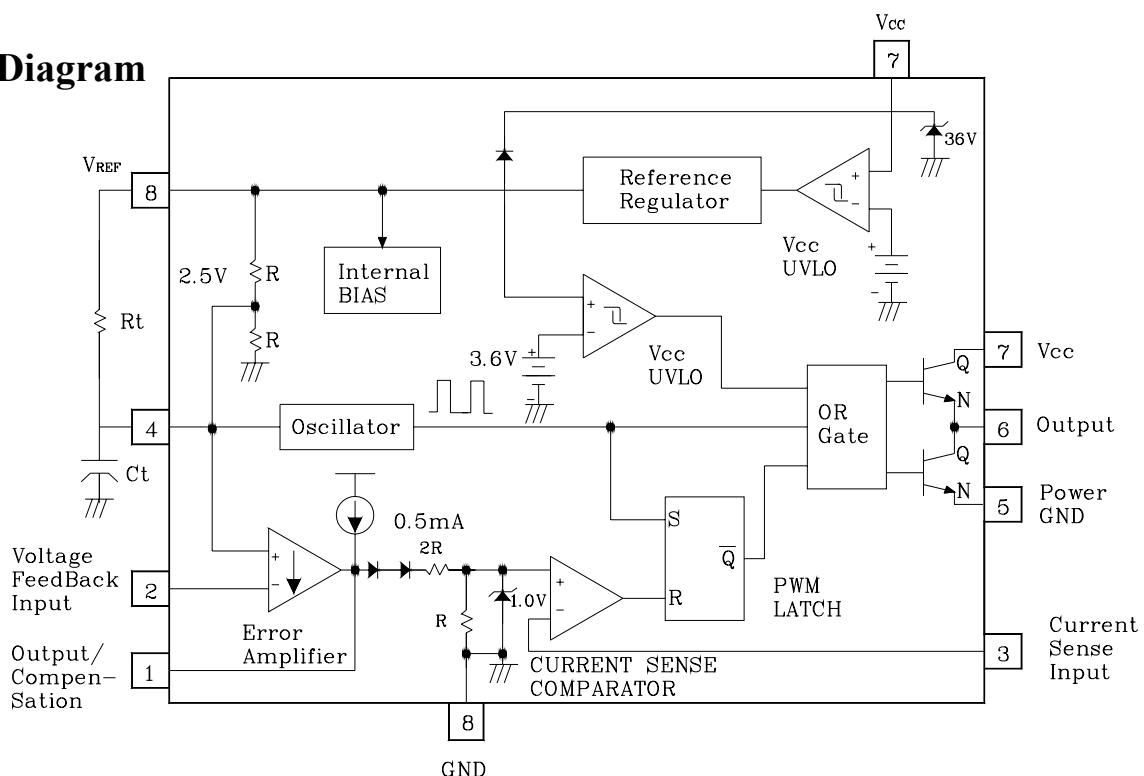
Characteristic	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	30	V
Current Sense and V <sub>fb</sub> Input	V <sub>IN</sub>	-0.3 to V <sub>CC</sub>	V
Total Power Supply and Zener Current	I <sub>CC</sub> + I <sub>Z</sub>	30	mA
Output Sink of Source Current	I <sub>o</sub>	1	A
Error AMP Output Sink Current	I <sub>eo</sub>	10	mA
Operating Ambient Temperature	T <sub>a</sub>	0 to 70	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to 150	°C
Power Dissipation at T <sub>a</sub> ≤ 50°C	P <sub>d</sub>	1	W

note) All voltages are with respect to PIN5, and current are positive into the specified pin.

## PIN Description

PIN NO	Function	Description
1	Compensation	Error amplifier output and is made available for loop compensation.
2	Voltage feedback	Inverting input of error amplifier, normally connected to the switching power supply output through a resistor driver.
3	Current sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output.
4	R <sub>t</sub> /C <sub>t</sub>	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor R <sub>t</sub> to V <sub>ref</sub> and capacitor C <sub>t</sub> to ground.
5	Ground	This pin is the combined control circuitry and power ground.
6	Output	This output directly drives the gate of a power MOSFET. Peak current up to 1.0A are sourced and sunk by this pin.
7	V <sub>CC</sub>	This pin is the positive supply of the control IC.
8	V <sub>ref</sub>	This is the reference output. it provides charging current for capacitor C <sub>t</sub> through resistor R <sub>t</sub> .

## Block Diagram



## Electrical Characteristics

(Unless otherwise stated, these specifications apply for  $0 \leq T_a \leq 70^\circ\text{C}$ ;  $V_{CC} = 15\text{V}$ (Note.4),  $R_L = 10\text{ k}\Omega$ ,  $C_L = 3.3\text{nF}$ )

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>1. Reference Section</b>						
Output Voltage	Vref	$T_a = 25^\circ\text{C}$ , $I_o = 1\text{mA}$	4.90	5.00	5.10	V
Line Regulation	$\Delta V_{\text{ref}}$	$12\text{V} \leq V_{CC} \leq 25\text{V}$	-	6	20	mV
Load Regulation	$\Delta V_{\text{ref}}$	$1\text{mA} \leq I_o \leq 20\text{mA}$	-	6	25	mV
Temperature Stability	$\Delta V_T / \Delta V_T$	(Note 1)	-	0.2	0.4	mV/ $^\circ\text{C}$
Output Noise Voltage	$V_n$	$10\text{Hz} \leq f \leq 10\text{kHz}$ , $T_a = 25^\circ\text{C}$ (Note 1)	-	50	-	$\mu\text{V}$
Long Term Stability	S	$T_a = 125^\circ\text{C}$ , 1000Hrs (Note 1)	-	5	-	mV
Output Short Circuit	$I_{SC}$	-	-30	-100	-180	mA
<b>2. Oscillator Section</b>						
Initial Accuracy	$f_{SC}$	$T_a = 25^\circ\text{C}$	47	52	57	KHz
Voltage Stability	$\Delta f / \Delta V$	$12 \leq V_a \leq 25\text{V}$	-	0.05	1.0	%
Temperature Stability	$\Delta f / \Delta T$	$T_{\text{min}} \leq T_a \leq T_{\text{max}}$ (Note 1)	-	5	-	%
Amplitude	$V_4$	$V_{\text{PIN4}}$ Peak to Peak	-	1.7	-	V
<b>3. Error Amp Section</b>						
Input Voltage	$V_2$	$V_{\text{PIN1}} = 2.5\text{V}$	2.42	2.50	2.58	V
Input Bias Current	$I_b$	-	-	-0.3	-2.0	$\mu\text{A}$
Open Loop Voltage Gain	$A_{V01}$	$2\text{V} \leq V_o \leq 4\text{V}$	65	90	-	dB
Supply Voltage Rejection	SVR	$12\text{V} \leq V_a \leq 25\text{V}$	60	70	-	dB
Output Sink Current	$I_o$	$V_{\text{PIN2}} = 2.7\text{V}$ , $V_{\text{PIN1}} = 1.1\text{V}$	2	6	-	mA
Output Source Current	$I_o$	$V_{\text{PIN2}} = 2.3\text{V}$ , $V_{\text{PIN1}} = 5\text{V}$	-0.5	-0.8	-	mA
$V_{\text{OUT High}}$	$V_{ch}$	$V_{\text{PIN2}} = 2.3\text{V}$ , $R_L = 15\text{ k}\Omega$ to Ground	5	6	-	V
$V_{\text{OUT Low}}$	$V_{c1}$	$V_{\text{PIN2}} = 2.7\text{V}$ , $R_L = 15\text{ k}\Omega$ Pin8	-	0.7	1.1	V
<b>4. Current Sense Section</b>						
Gain	$G_V$	(Note 2 & 3)	2.8	3.0	3.2	V/V
Maximum Input Signal	$V_3$	$V_{\text{PIN1}} = 5\text{V}$ (Note 2)	0.9	1.0	1.1	V
Supply Volt Rejection	SVR	$12 \leq V_a \leq 25\text{V}$ (Note 2)	-	70	-	dB
Input Bias Current	$I_b$	-	-	-2	-10	$\mu\text{A}$
<b>5. Output Section</b>						
Output Low Level	$V_{O1}$	$I_{\text{SINK}} = 20\text{mA}$	-	0.1	0.4	V
		$I_{\text{SINK}} = 200\text{mA}$	-	1.5	2.2	V
Output High Level	$V_{Oh}$	$I_{\text{SOURCE}} = 20\text{mA}$	13.0	13.5	-	V
		$I_{\text{SOURCE}} = 200\text{mA}$	12.0	13.5	-	V
Rise time	$t_r$	$T_a = 25^\circ\text{C}$ , $C_l = 1\text{nF}$ (Note 1)	-	50	150	ns
Fall time	$t_f$	$T_a = 25^\circ\text{C}$ , $C_l = 1\text{nF}$ (Note 1)	-	50	150	ns

**Electrical Characteristics(continued)**

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>6. Under-Voltage Lockout Section</b>						
Start Threshold	$V_{th}$	$V_{PIN7}$ where $V_{PIN8} \geq 4.9V$	14.5	16.0	17.5	V
Min. Operation Voltage After Turn-On	$V_{CC(min)}$	$V_{PIN7}$ where $V_{PIN8} \leq 1V$	8.5	10.0	11.5	V
<b>7. PWM Section</b>						
Maximum Duty Cycle	$DC_{max}$	-	93	97	100	ns
<b>8. Total Standby Section</b>						
Start-Up Current	$I_{st}$	$V_{CC} = 15V$ before turn on	-	0.4	0.7	mA
Operating Supply Current	$I_{CC}$	$V_{PIN2} = V_{PIN3} = 0V$	-	11	20	mA
Zener Voltage	$V_Z$	$I_{CC} = 25mA$	-	36	-	V

NOTE: 1.Thes parameters, although guaranteed,are not 100% tested in production

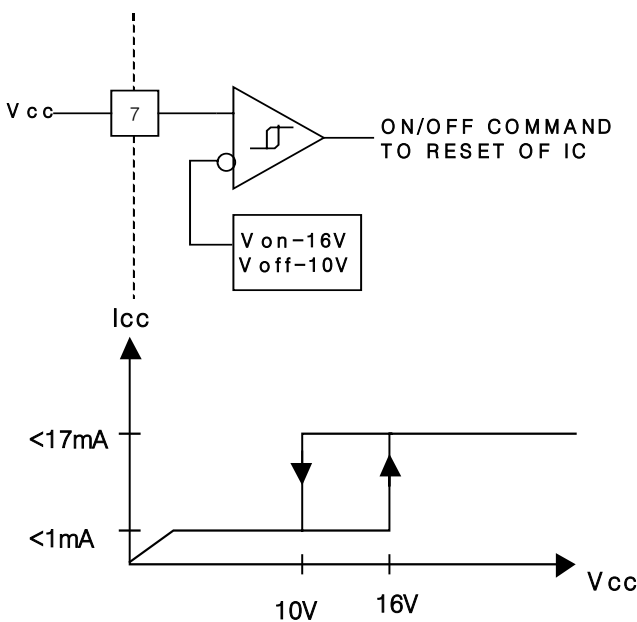
2.Parameter measured at trip piont of latch with  $V_{pin2}=0$

3.Gain defined as :  $A = \Delta V_{PIN1} / \Delta V_{PIN3}$  ;  $0 \leq V_{PIN3} \leq 0.8V$

4.Adjust  $V_{CC}$  above the start threshold before setting at 15V

**Information in Using IC**

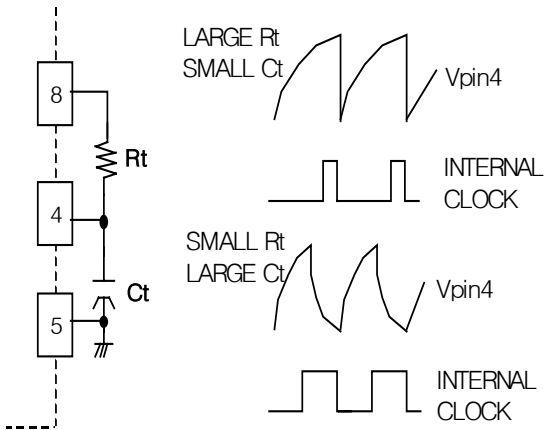
**1. Under voltage Lockout**



To prevent erratic output behavior which activating the power switch with extraneous leakage currents, during under voltage lockout. Output(pin6) should be shunted to ground with a bleeder resistor.

The  $V_{cc}$  comparator upper and lower threshold are 16V/10V. The large hysteresis and low start up currents makes it ideally suited in off-line converter application where efficient bootstrap start-up techniques are required.

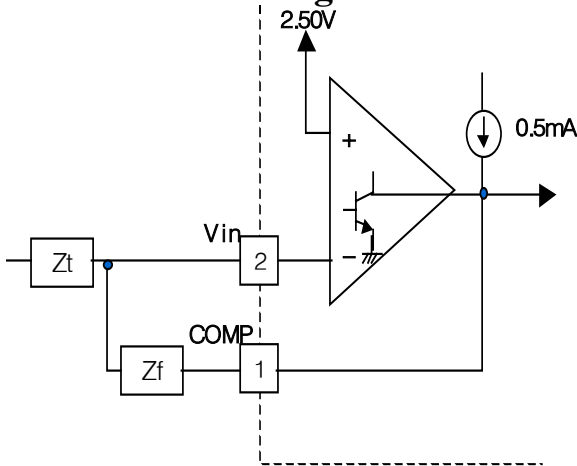
## 2. Oscillator Waveforms and Maximum Duty Cycle



The oscillator frequency is programmed by the values selected for the timing components  $R_t$  and  $C_t$ .  $C_t$  is charged from 5V,  $V_{ref}$ , through resistor  $R_t$  to approximately 2.8V and discharged to 1.2V by an internal current sink.

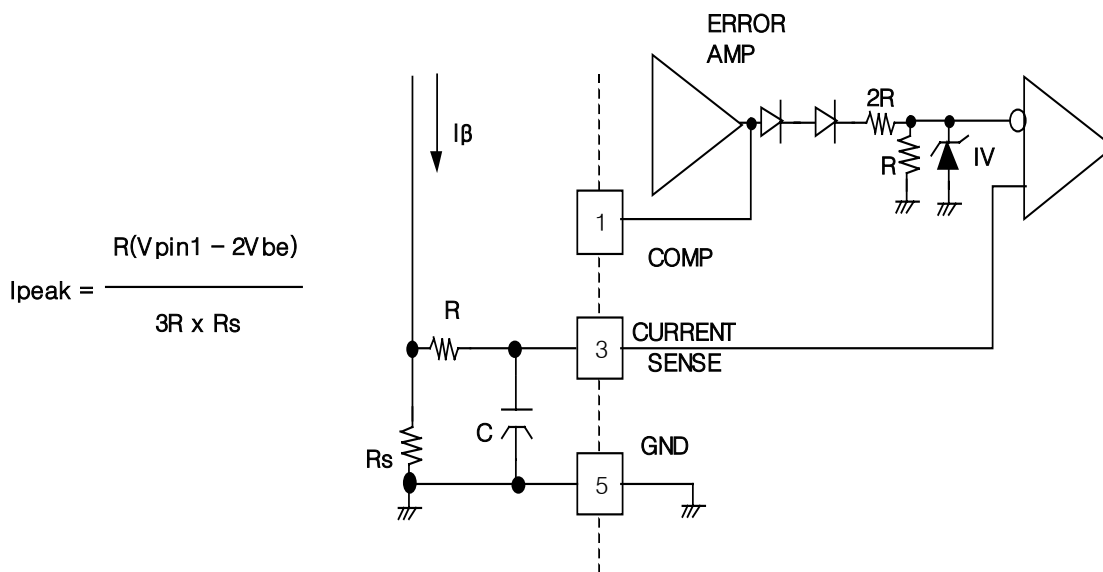
During the discharge of  $C_t$ , the oscillator generates an internal blanking pulse and the center input NOR gate high. This makes output to be in a low state and control the amount of output dead time.

## 3. Error AMP Configuration



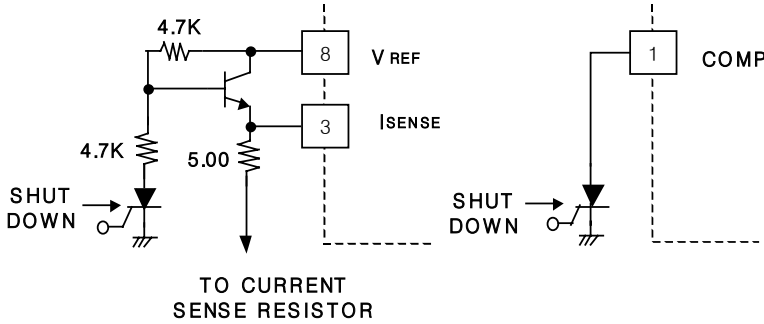
Error amp output (Pin1) is provided for external loop compensation and error amp can source or sink up to 0.5mA. The non-inverting input is internally biased at 2.5V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input (pin2).

## 4. Current Sense Circuit



A normal operating conditions occurs when the power supply output is overloaded or its output voltage to 1.0V. Therefore the maximum peak switch current is  $I_{pk(max)} = 1.0V/R_s$ , and under the normal operating conditions the

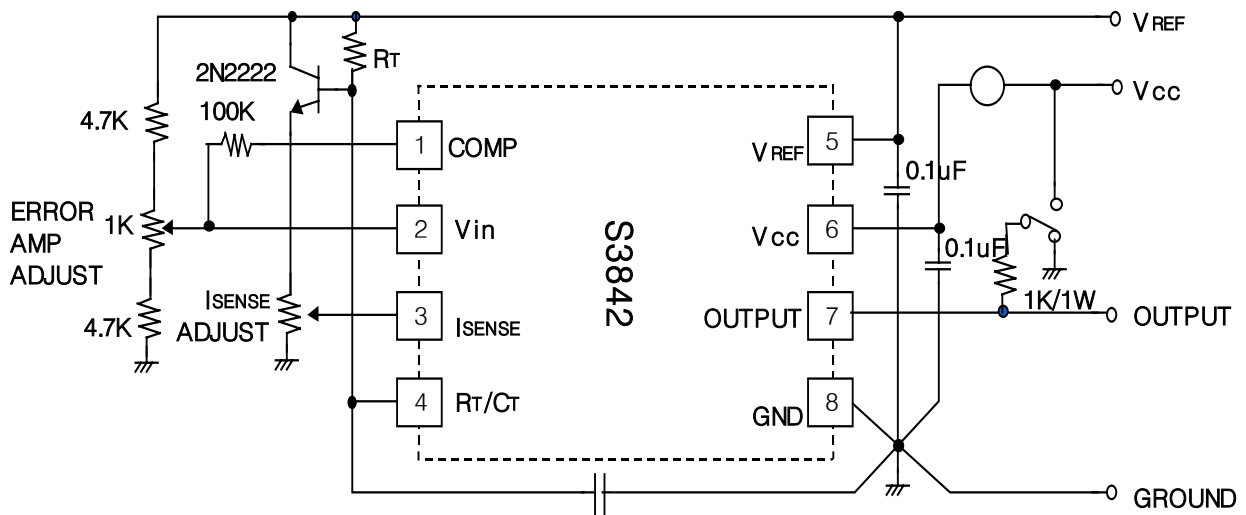
**5. Shutdown Techniques**



Shutdown of the S3842 can be accomplished by two methods; either raise pin3 above 1V or pull pin1 below a voltage two diodes drops above ground. Either causes the output of the PWM method comparator to be high (refer to

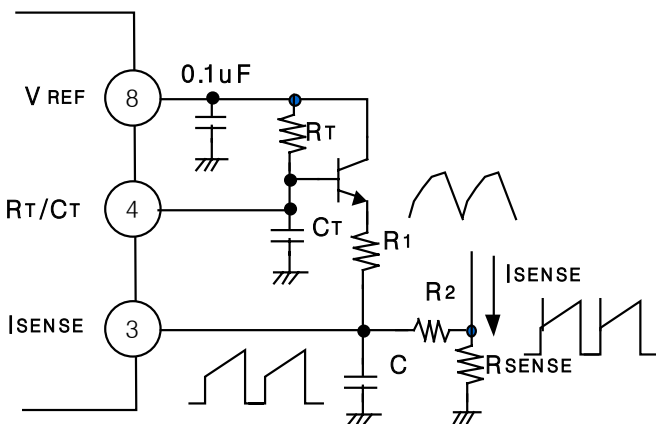
block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which turn off, allowing the SCR to reset.

**6. Open Loop Test**



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin5 in a single point ground. The transistor and 5 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin3.

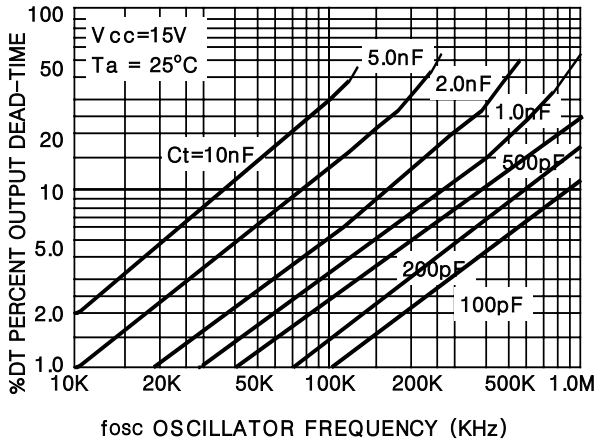
**7. Slope Compensation**



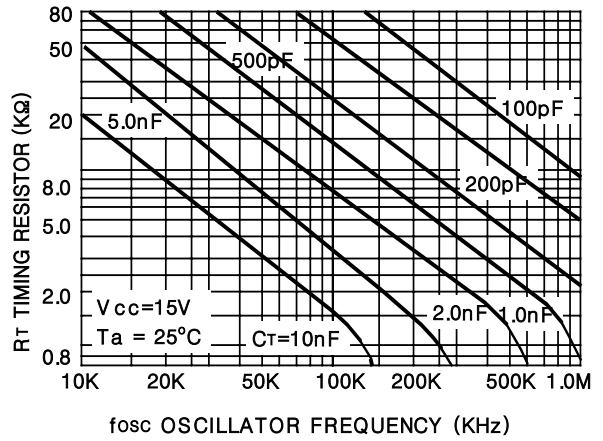
A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycle over 50%. Note that capacitor C, forms a filter with R<sub>2</sub> to suppress the leading edge switch spikes.

Electrical Characteristic Curves

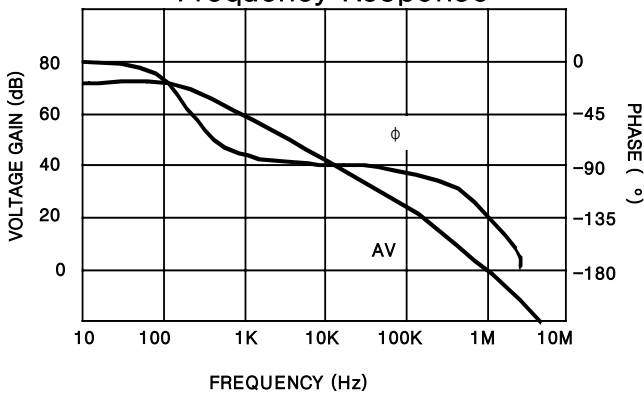
OUTPUT DEAD-TIME vs. OSCILLATOR FREQUENCY



TIMING RESISTOR vs. OSCILLATOR FREQUENCY



Error Amplifier Open-Loop Frequency Response



Output Saturation Characteristics

