AUK Semiconductor

S3842

Current Mode PWM Controller

Descriptions

The S3842, high performance current mode controller, Provides the necessary features to off-line and DC-DC fixed frequency current control applications offering the designer a cost effective solution with minimal external components. Internally protection circuity includes built-in input and reference under-voltage lockout and current limiting with hysteresis.
Also other characteristics of internal circuit provide improved line regulation, enhanced load response, trimmed oscillation for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator and totempole output designed to source and sink high peak current from a capacitive load such as the gate of a power MOSFET.

Features

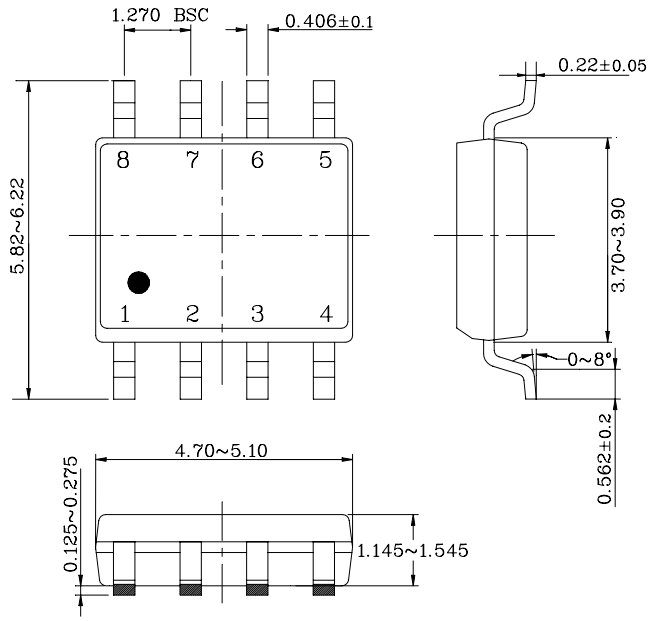
- Optimized for off-line control
- Low start up and operating current
- Pulse by pulse current limiting
- Enhanced load response characteristic
- Current mode operation to 500 ㎑
- Under voltage lockout with 6V hysteresis
- Internally trimmed bandgap reference about 5V
- Automatic feed forward compensation

Ordering Information

Type NO.	Marking	Package Code
S3842	S3842	SOP-8

Outline Dimensions

unit : mm



PIN Connections

1. Output / Compensation
2. Voltage feedback. Input
3. Current sense Input
4. Rt/Ct
5. GND
6. Output
7. Vcc
8. Vref

Absolute Maximum Ratings

Ta=25°C

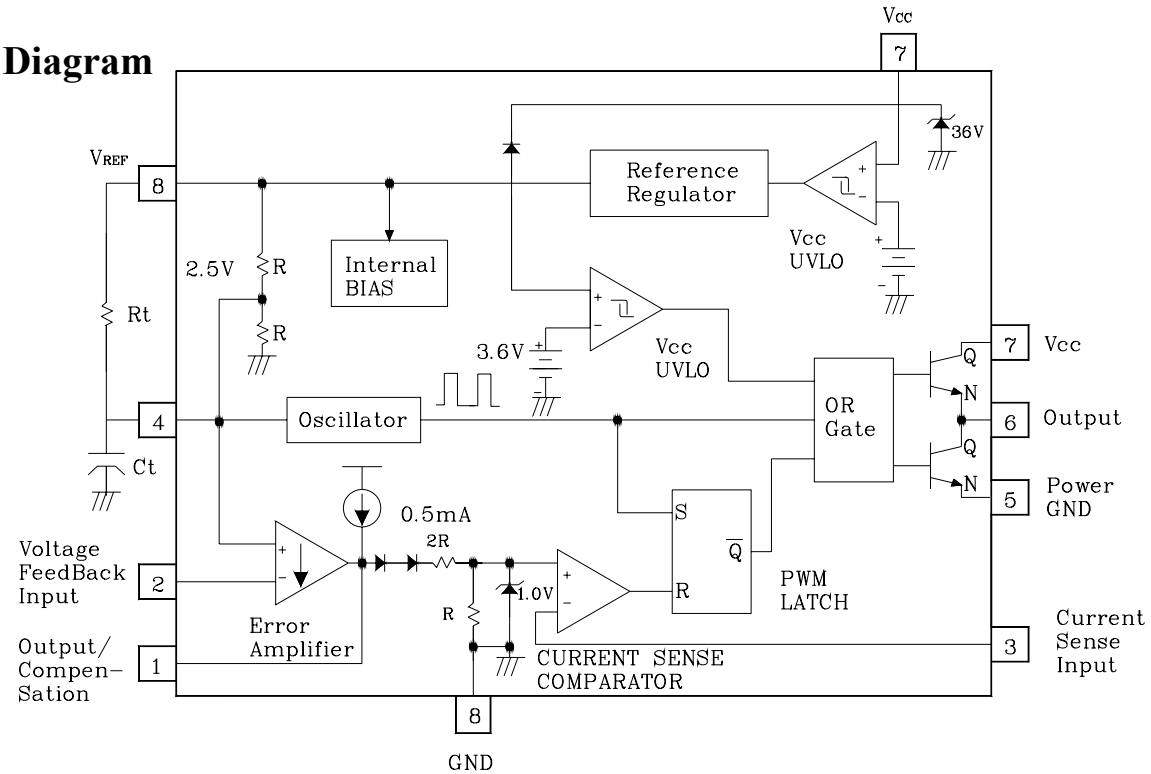
Characteristic	Symbol	Ratings	Unit
Supply voltage	V_{cc}	30	V
Current Sense and V_{fb} Input	V_{IN}	-0.3 to V_{cc}	V
Total Power Supply and Zener Current	I_{CC}+ I_Z	30	mA
Output Sink of Source Current	I_o	1	A
Error AMP Output Sink Current	I_{eo}	10	mA
Operating Ambient Temperature	T_a	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C
Power Dissipation at $T_a \leq 50°C$	P_d	1	W

note) All voltages are with respect to PIN5, and current are positive into the specified pin.

PIN Description

PIN NO	Function	Description
1	Compensation	Error amplifier output and is made available for loop compensation.
2	Voltage feedback	Inverting input of error amplifier, normally connected to the switching power supply output through a resistor driver.
3	Current sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output.
4	R_t/C_t	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor R_t to Vref and capacitor C_t to ground.
5	Ground	This pin is the combined control circuitry and power ground.
6	Output	This output directly drives the gate of a power MOSFET. Peak current up to 1.0A are sourced and sinked by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	Vref	This is the reference output. it provides charging current for capacitor C_t through resistor R_t.

Block Diagram



Electrical Characteristics

(Unless otherwise stated, these specifications apply for $0 \le Ta \le 70°C$; V_{CC} =15V(Note.4), R_L =10 kΩ, C_L =3.3nF)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
1. Reference Section						
Output Voltage	Vref	Ta=25°C, I_O=1mA	4.90	5.00	5.10	V
Line Regulation	△Vref	12V ≤ V_{CC} ≤ 25V	-	6	20	mV
Load Regulation	△Vref	1mA ≤ I_O ≤ 20mA	-	6	25	mV
Temperature Stability	$\triangle V_T / \triangle V_T$	(Note 1)	-	0.2	0.4	mV/°C
Output Noise Voltage	V_n	10Hz ≤ f ≤10KHz,T_a=25°C(Note 1)	-	50	-	uV
Long Term Stability	S	T_a=125°C, 1000Hrs (Note 1)	-	5	-	mV
Output Short Circuit	I_{SC}	-	-30	-100	-180	mA
2. Oscillator Section						
Initial Accuracy	f_{SC}	T_a=25°C	47	52	57	KHz
Voltage Stability	$\triangle f / \triangle V$	12 ≤ V_a ≤25V	-	0.05	1.0	%
Temperature Stability	$\triangle f / \triangle T$	$T_{min} \le T_a \le T_{max}$ (Note 1)	-	5	-	%
Amplitude	V_4	V_{PIN4} Peak to Peak	-	1.7	-	V
3. Error Amp Section						
Input Voltage	V_2	V_{PIN1}=2.5V	2.42	2.50	2.58	V
Input Bias Current	I_b	-	-	-0.3	-2.0	μA
Open Loop Voltage Gain	A_{VO1}	2V ≤ V_O ≤ 4V	65	90	-	dB
Supply Voltage Rejection	SVR	12V ≤ V_a ≤ 25V	60	70	-	dB
Output Sink Current	I_O	V_{PIN2}=2.7V, V_{PIN1}=1.1V	2	6	-	mA
Output Source Current	I_O	V_{PIN2}=2.3V, V_{PIN1}=5V	-0.5	-0.8	-	mA
V_{OUT} High	V_{ch}	V_{PIN2}=2.3V, R_L=15 kΩ to Ground	5	6	-	V
V_{OUT} Low	V_{c1}	V_{PIN2}=2.7V, R_L=15 kΩ Pin8	-	0.7	1.1	V
4. Current Sense Section						
Gain	G_V	(Note 2 & 3)	2.8	3.0	3.2	V/V
Maximum Input Signal	V_3	$V_{PIN\ 1}$=5V (Note 2)	0.9	1.0	1.1	V
Supply Volt Rejection	SVR	12 ≤ V_a ≤ 25V (Note 2)	-	70	-	dB
Input Bias Current	I_b	-	-	-2	-10	μA
5.Output Section						
Output Low Level	V_{OI}	I_{SINK}=20mA	-	0.1	0.4	V
		I_{SINK}=200mA	-	1.5	2.2	V
Output High Level	V_{Oh}	I_{SOURCE}=20mA	13.0	13.5	-	V
		I_{SOURCE}=200mA	12.0	13.5	-	V
Rise time	t_r	T_a=25°C, Cl=1nF (Note 1)	-	50	150	ns
Fall time	t_f	T_a=25°C, Cl=1nF (Note 1)	-	50	150	ns

Electrical Characteristics(continued)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
6. Under-Voltage Lockout Section						
Start Threshold	V_{th}	V_{PIN7} where $V_{PIN8} \geq 4.9V$	14.5	16.0	17.5	V
Min. Operation Voltage After Turn-On	$V_{CC(min)}$	V_{PIN7} where $V_{PIN8} \leq 1V$	8.5	10.0	11.5	V
7. PWM Section						
Maximum Duty Cycle	DC_{max}	-	93	97	100	ns
8. Total Standby Section						
Start-Up Current	I_{st}	V_{CC} = 15V before turn on	-	0.4	0.7	mA
Operating Supply Current	I_{CC}	V_{PIN2}= V_{PIN3}=0V	-	11	20	mA
Zener Voltage	V_Z	I_{CC}=25mA	-	36	-	V

NOTE: 1.Thes parameters, although guaranteed.are not 100% tested in production

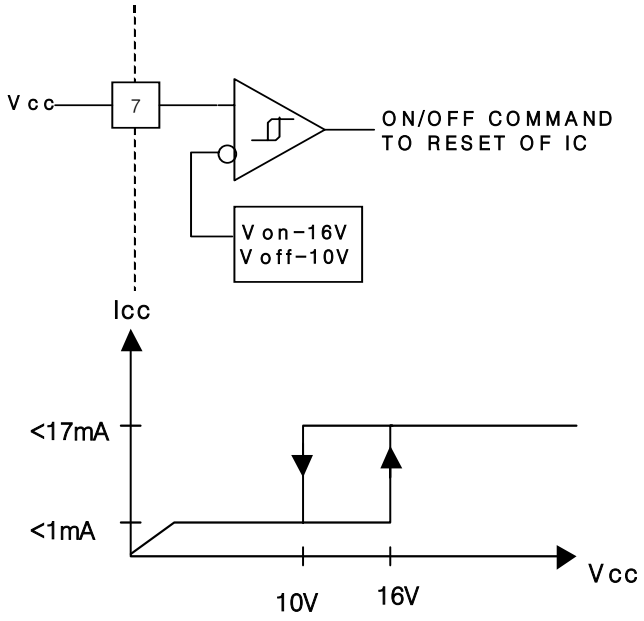
2.Parameter measured at trip piont of latch with V_{pin2}= 0

3.Gain defined as : A =$\triangle V_{PIN1}/\triangle V_{PIN3}$; $0 \leq V_{PIN3} \leq 0.8V$

4.Adjust V_{CC} above the start threshold before setting at 15V

Information in Using IC

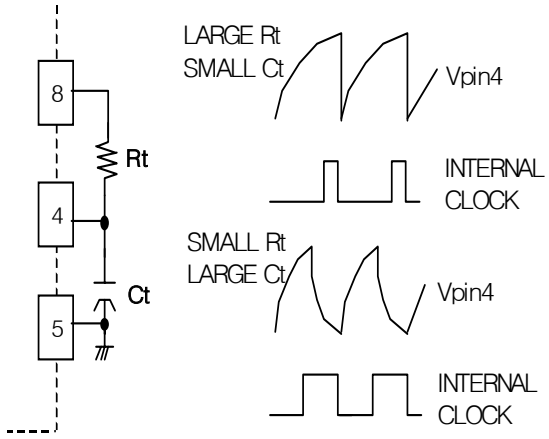
1. Under voltage Lockout



To prevent erratic output behavior which activating the power switch with extraneous leakage currents, during under voltage lockout. Output(pin6) should be shunted to ground with a bleeder resister.

The Vcc comparator upper and lower threshold are 16V/10V. The large hysteresis and low start up currents makes it ideally suited in off-line converter application where efficient bootstrap start-up techniques are required.

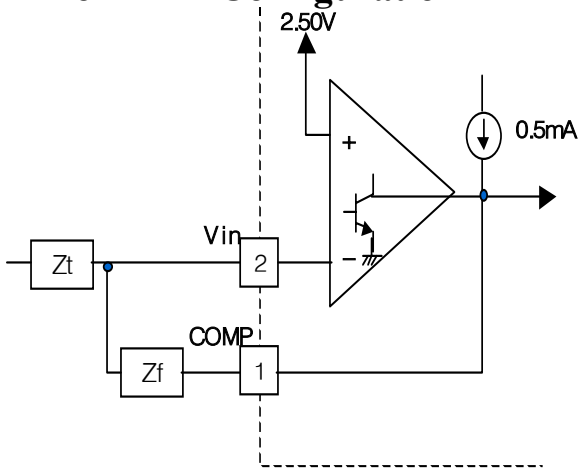
2. Oscillator Waveforms and Maximum Duty Cycle



The oscillator frequency is programmed by the values selected for the timing components Rt and Ct. Ct is charged from 5V, Vref, through resistor Rt to approximately 2.8V and discharged to 1.2V by an internal current sink.

During the discharge of Ct, the oscillator generates an internal blanking pulse and the center input NOR gate high. This makes output to be in a low state and control the amount of output dead time.

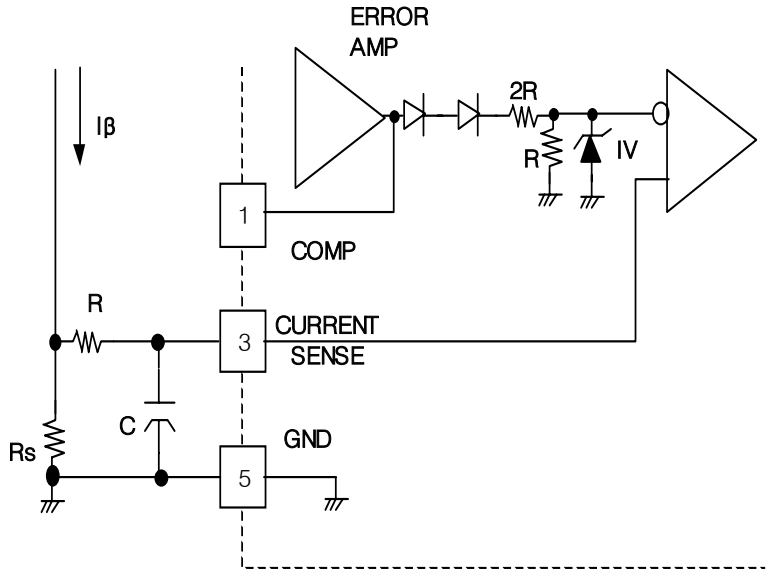
3. Error AMP Configuration



Error amp output(Pin1) is provided for external loop Compensation and error amp can source or sink up to 0.5mA. The non-inverting input is internally biased at 2.5V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input(pin2).

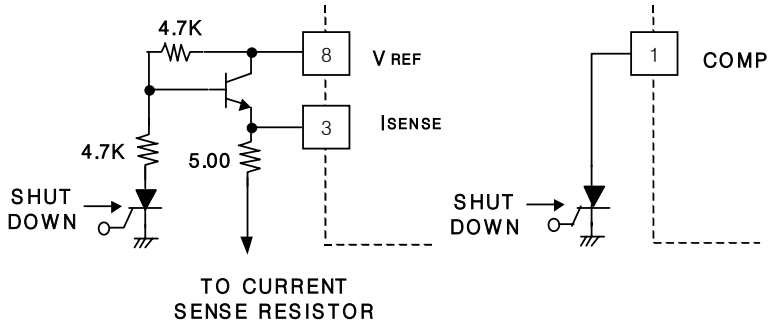
4. Current Sense Circuit

$$Ipeak = \frac{R(Vpin1 - 2Vbe)}{3R \times Rs}$$



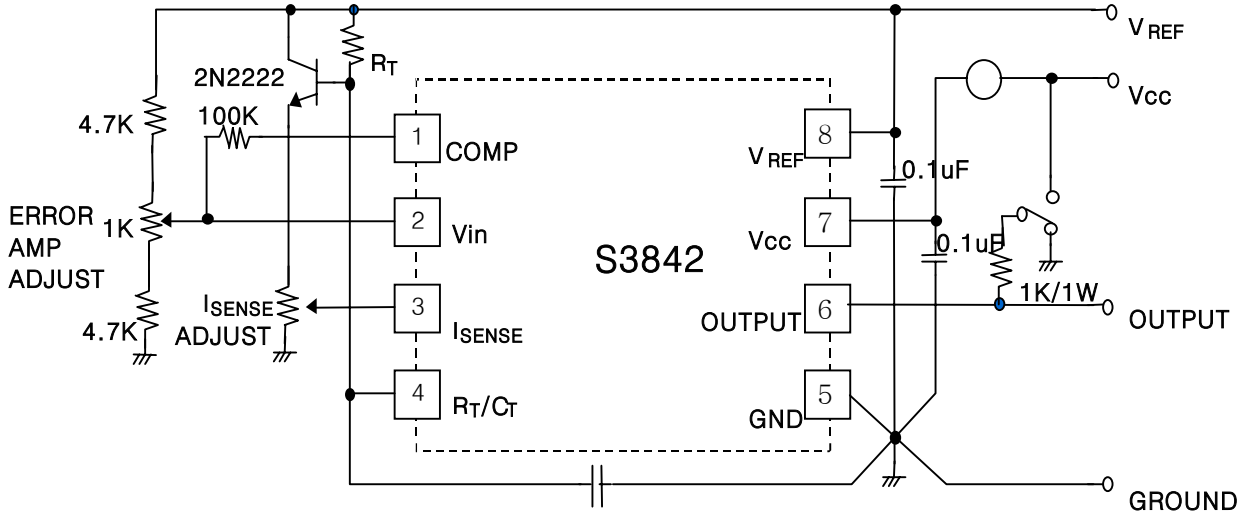
A normal operating conditions occurs when the power supply output is overloaded or if output voltage to 1.0V Therefore the maximum peak switch current is lpk(max)=1.0V/R_s, and under the normal operating conditions the peak inductor current controlled by the voltage at pin1.

5. Shutdown Techniques



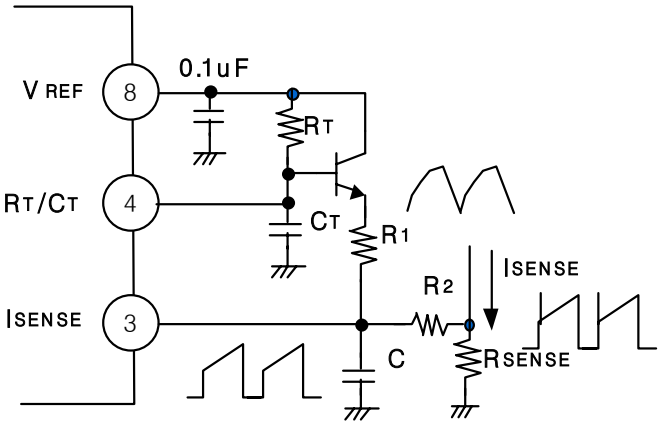
Shutdown of the S3842 can be accomplished by two methods; either raise pin3 above 1V or pull pin1 below a voltage two diodes drops above ground. Either causes the output of the PWM method comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which turn off, allowing the SCR to reset.

6. Open Loop Test



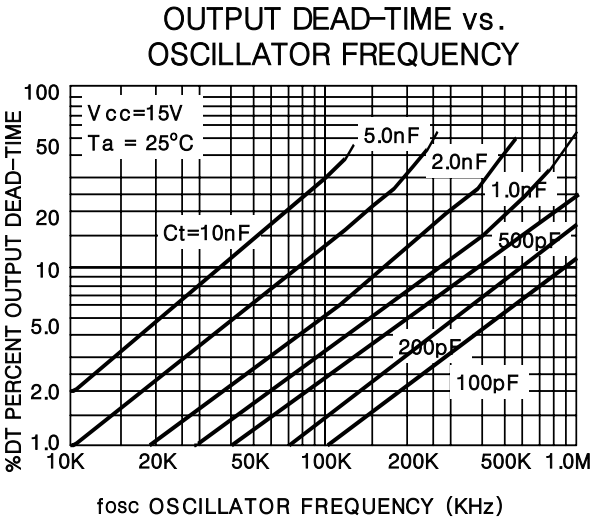
High peak currents associated with capacitive leads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin5 in a single point ground. The transistor and 5 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin3.

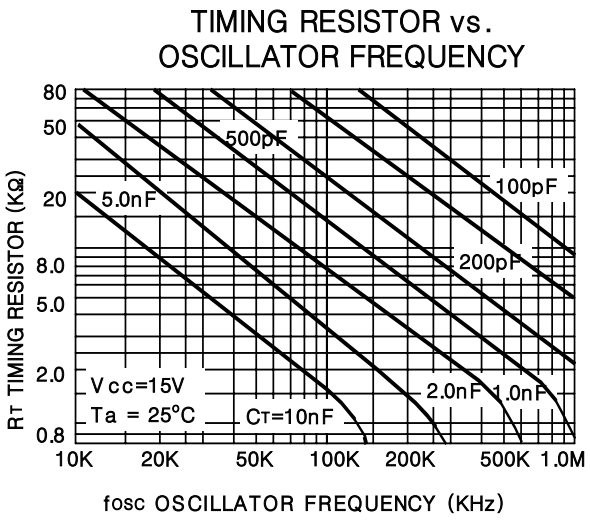
7. Slope Compensation

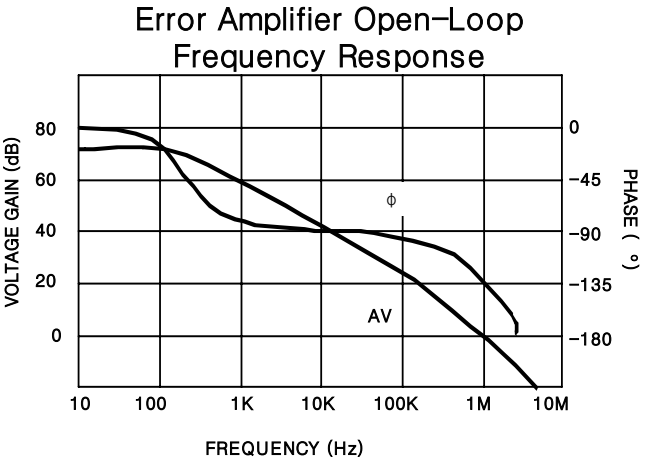


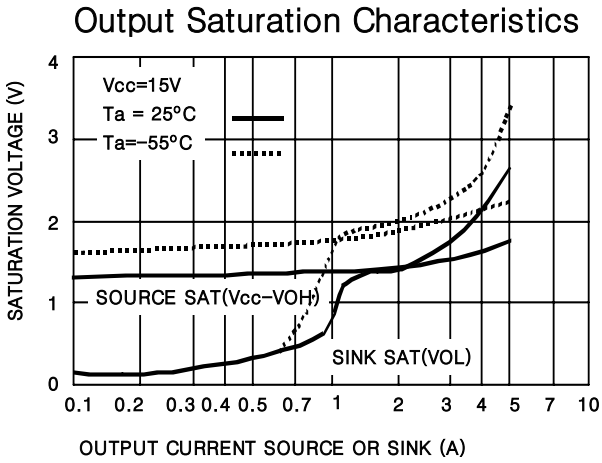
A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycle over 50%. Note that capacitor C, forms a filter with R_2 to suppress the leading edge switch spikes.

Electrical Characteristic Curves









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