1 PRODUCT OVERVIEW

SAM8 PRODUCT FAMILY

Samsung's SAM8 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

— Efficient register-oriented architecture
— Selectable CPU clock sources
— Idle and Stop power-down mode release by interrupt
— Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

S3C8618/C8615/P8615 MICROCONTROLLERS

The S3C8618/C8615/P8615 single-chip 8-bit microcontroller is based on the powerful SAM8 CPU architecture. The internal register file is logically expanded to increase the on-chip register space. The S3C8618/C8615/P8615 have 8/16 K bytes of on-chip program ROM.

Following Samsung's modular design approach, the following peripherals were integrated with the SAM8 core:

— Four programmable I/O ports (total 28 pins)
— One 8-bit basic timer for oscillation stabilization and watchdog functions
— One 8-bit general-purpose timer/counter with selectable clock sources
— One 8-bit counter with selectable clock sources, including Hsync or Csync input
— One 8-bit timer for interval mode
— PWM block with seven 8-bit PWM circuits
— Sync processor block (for Vsync and Hsync I/O, Csync input, and Clamp signal output)
— Multi master IIC-bus with DDC support.

The S3C8618/C8615/P8615 are a versatile microcontroller that is ideal for use in multi-sync monitors or in general-purpose applications that require sophisticated timer/counter, PWM, sync signal processing, and multi-master IIC-bus support with DDC. It is available in a 42-pin SDIP or a 44-pin QFP package.

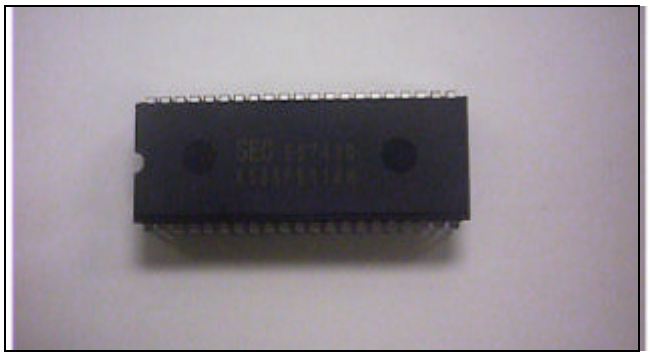


Figure 1-1. S3C8618/C8615/P8615 Microcontrollers

FEATURES

CPU

- SAM8 CPU core

Memory

- 8/16-Kbyte internal program memory (ROM)
- 272-byte general-purpose register area

Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 500 ns minimum (with 12 MHz CPU clock)

Interrupts

- Nine interrupt sources
- Nine interrupt vectors
- Six interrupt levels
- Fast interrupt processing for a select level

General I/O

- Four I/O ports (total 28 pins):

8-Bit Basic Timer

- Programmable timer for oscillation stabilization interval control or watchdog timer functions
- Three selectable internal clock frequencies

Timer/Counters

- One 8-bit general-purpose timer/counter with programmable operating modes and the following clock source options:
  - — Two selectable internal clock frequencies
- One 8-bit timer with interval operating mode
- One 8-bit counter with the following clock source options:
  - — Two selectable internal clock frequencies
  - — Hsync (or Csync) input from the sync processor block
  - — External clock source

Pulse Width Modulator

- Seven 8-bit PWM modules:
  - — 8-bit basic frame
  - — Four push-pull and three n-channel, open-drain output channels
  - — Selectable clock frequencies: 46.875 kHz at 12 MHz fosc.

Sync Processor

- Detection of sync input signals (Vsync-I, Hsync-I, and Csync-I)
- Sync signal separation and output (Hsync-O, Vsync-O, and Clamp-O)
- Pseudo sync signal output
- Programmable clamp signal output

DDC and Multi-Master IIC-Bus

- Serial peripheral interface
- Support for display data channel (DDC)

Oscillator Frequency

- 6 MHz to 12 MHz external crystal oscillator
- Interval Max. 12MHz CPU clock

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 4.5 V to 5.5 V

Package Types

- 42-pin SDIP, 44-pin QFP

BLOCK DIAGRAM

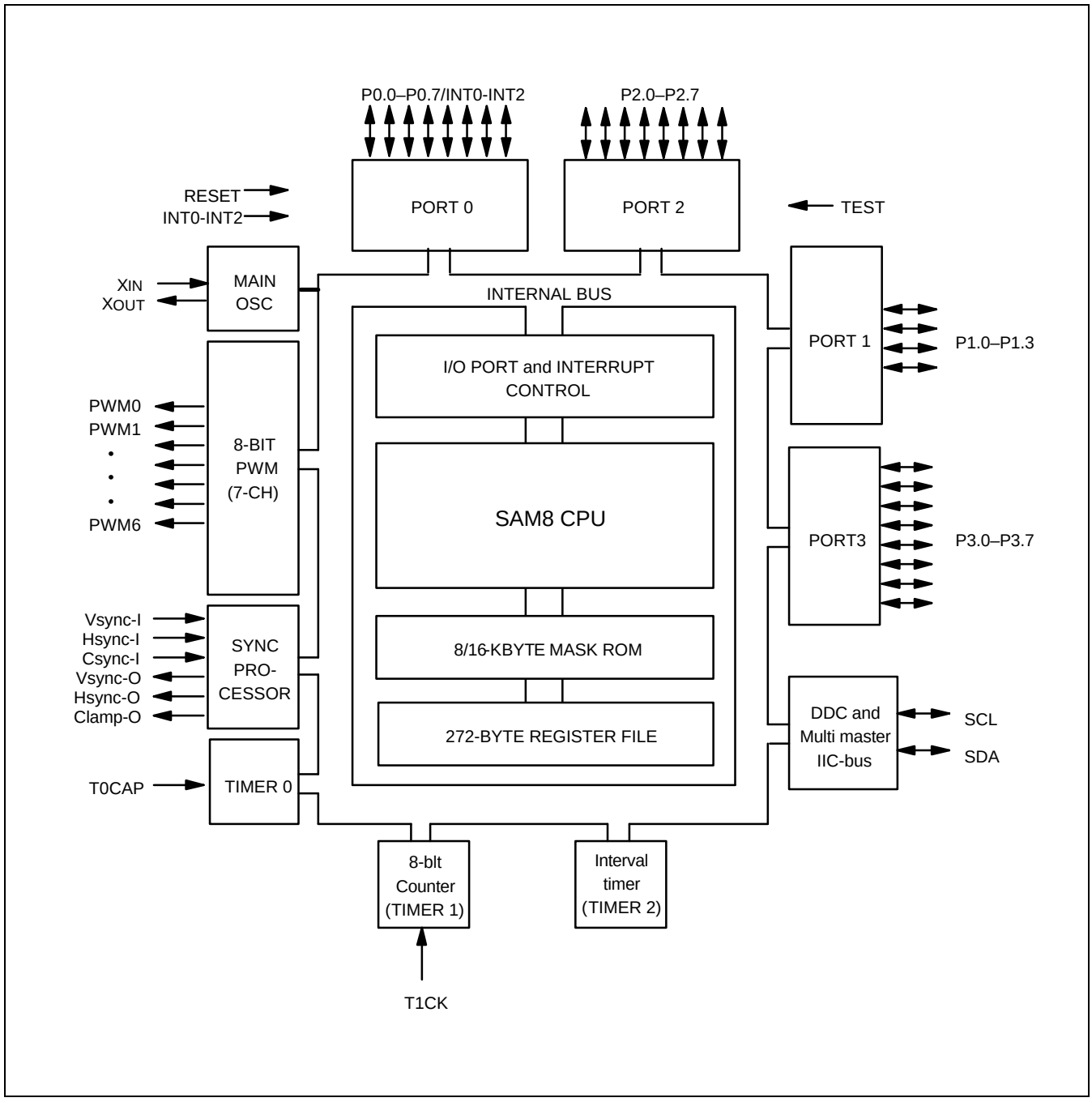


Figure 1-2. Block Diagram

PIN ASSIGNMENTS

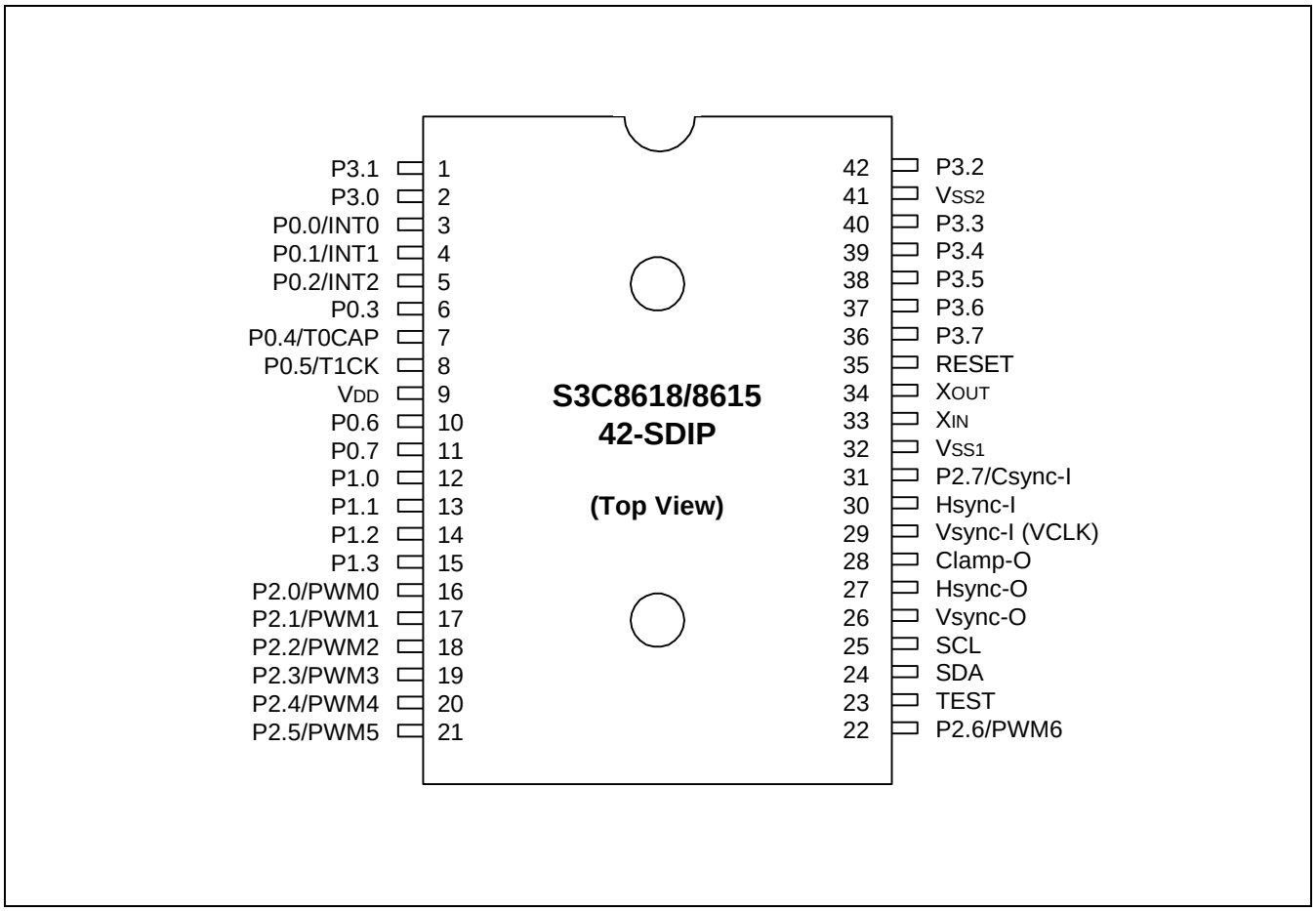


Figure 1-3. Pin Assignment Diagram (42-SDIP Package)

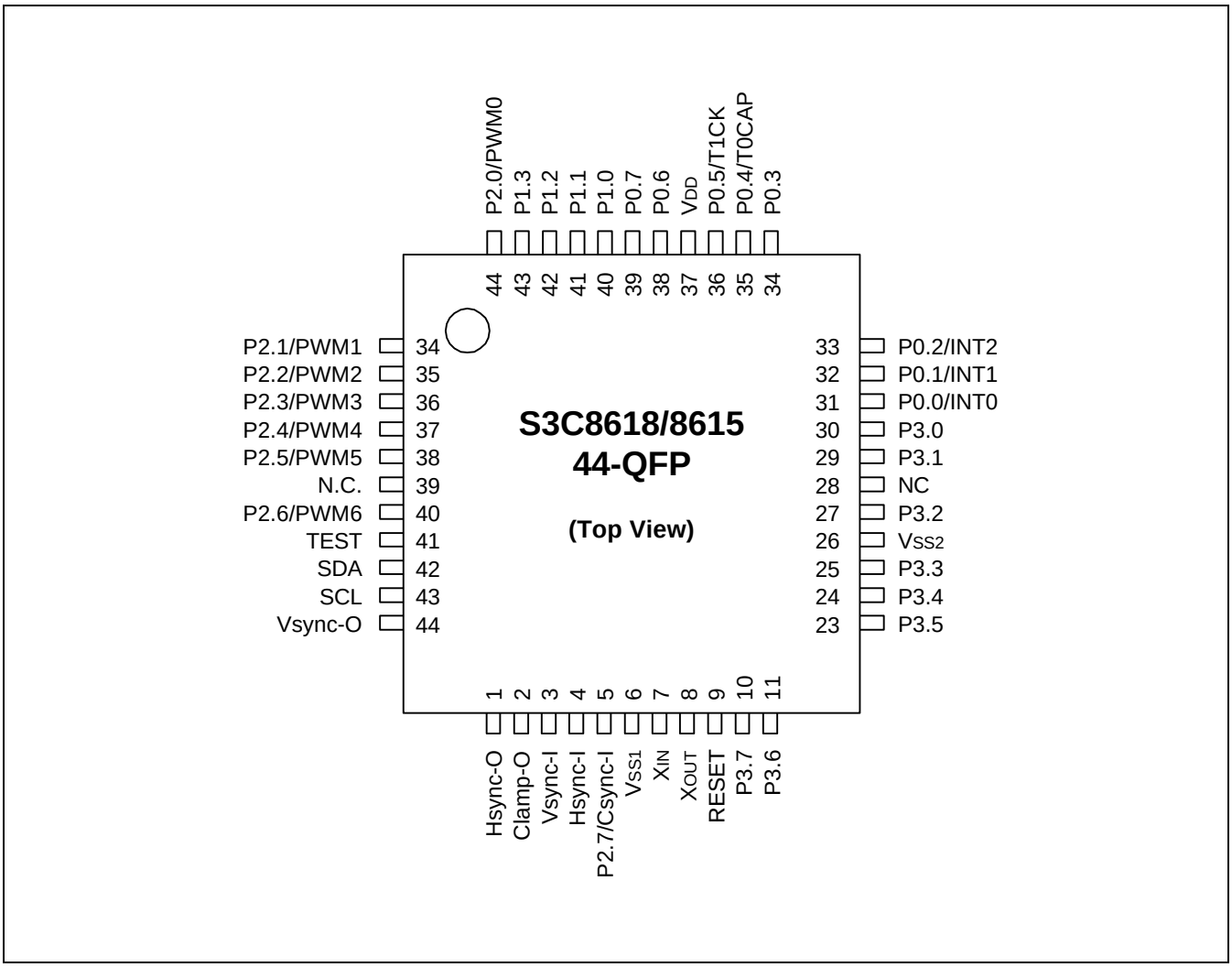


Figure 1-4. Pin Assignment Diagram (44-QFP Package)

PIN DESCRIPTIONS

Table 1-1. S3C8618/C8615/P8615 Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	SDIP Pin Numbers	Shared Functions
P0.0 P0.1 P0.2 P0.3 P0.4 P0.5 P0.6 P0.7	I/O	General-purpose, 8-bit I/O port. Share functions include three external interrupt inputs, I/O for timers 0 and 1. You can selectively configure port 0 pins to input or output mode.	D-1	3 4 5 6 7 8 10 11	INT0 INT1 INT2 T0CAP T1CK
P1.0–P1.3	I/O	General purpose, 8-bit I/O port. You can selectively configure port 1 pins to input or push-pull output mode.	D-1	12–15	–
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	I/O	General purpose, 8-bit I/O port. You can selectively configure port 2 pins to input or output mode. The port 2 pin circuit are designed to push-pull PWM output and Csync signal input.	D-1 D-1 D-1 D-1 E-1 E-1 E-1 D-1	16 17 18 19 20 21 22 31	PWM0 PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 Csync-I
P3.0–P3.7	I/O	General-purpose, 8-bit I/O port. You can selectively configure port 3 pins to input or output mode.	E	2, 1, 42, 40–36	–
Hsync-I Vsync-I Clamp-O Hsync-O Vsync-O SCL SDA	I I O O O I/O I/O	The pins are sync processor signal I/O and IIC-bus clock and data I/O	A A A A A G-3 G-3	30 29 28 27 26 25 24	–
V_{DD} V_{SS1}, V_{SS2}	–	Power supply pins	–	9 32, 41	–
X_{IN}, X_{OUT}	–	System clock input and output pins	–	33, 34	–
RESET	I	System reset pin	B	35	–
TEST	I	Factory test pin input 0 V: normal operation 5 V: factory test mode	–	23	–

NOTE: See 'Pin Circuit Diagrams' on next two pages for detailed information on circuit types A, B, D-1, E, E-1,and G-3.

PIN CIRCUITS

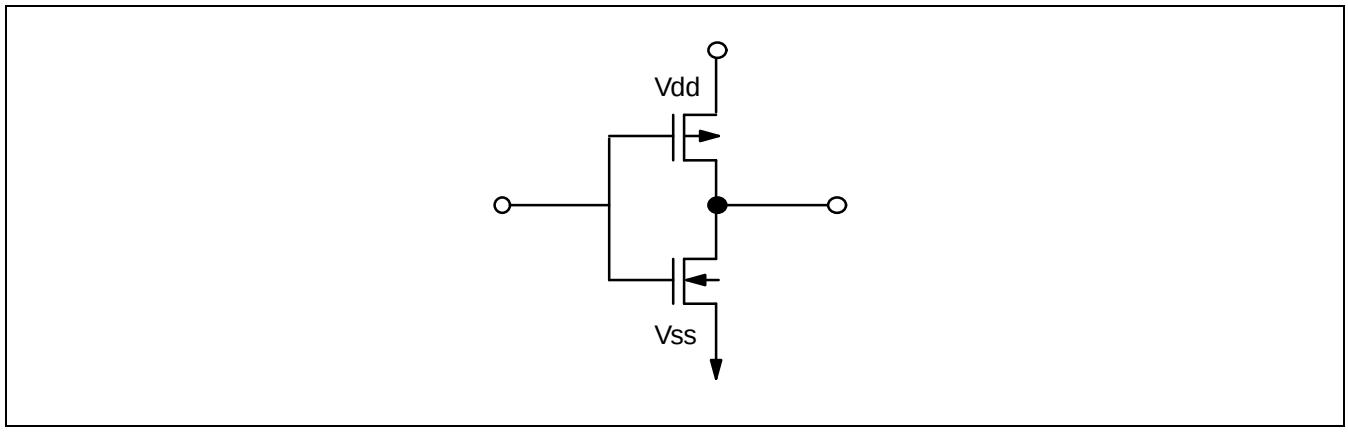


Figure 1-5. Pin Circuit Type A

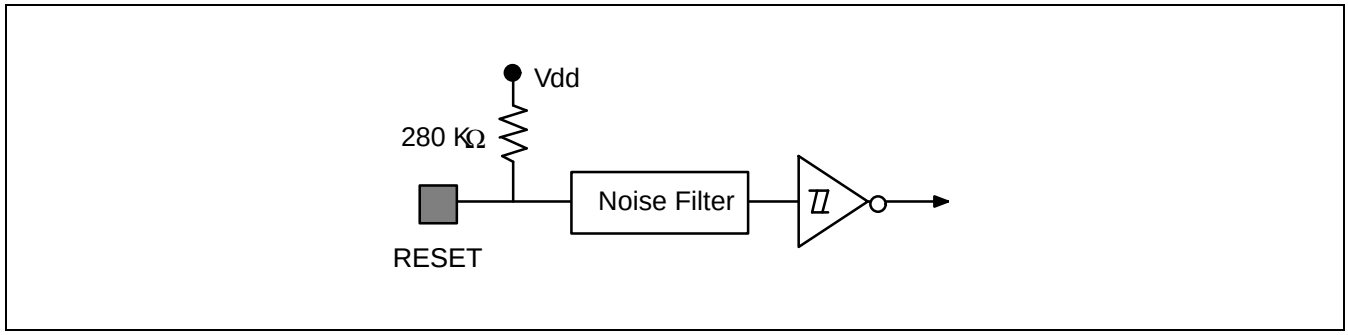


Figure 1-6. Pin Circuit Type B (RESET)

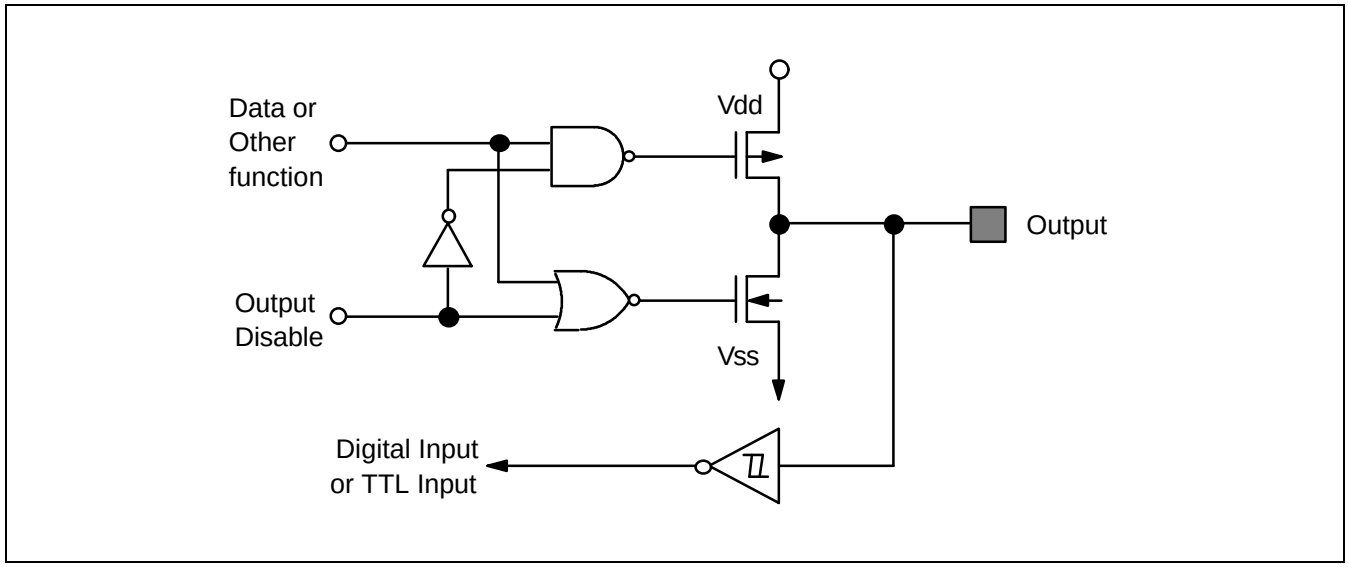


Figure 1-7. Pin Circuit Type D-1

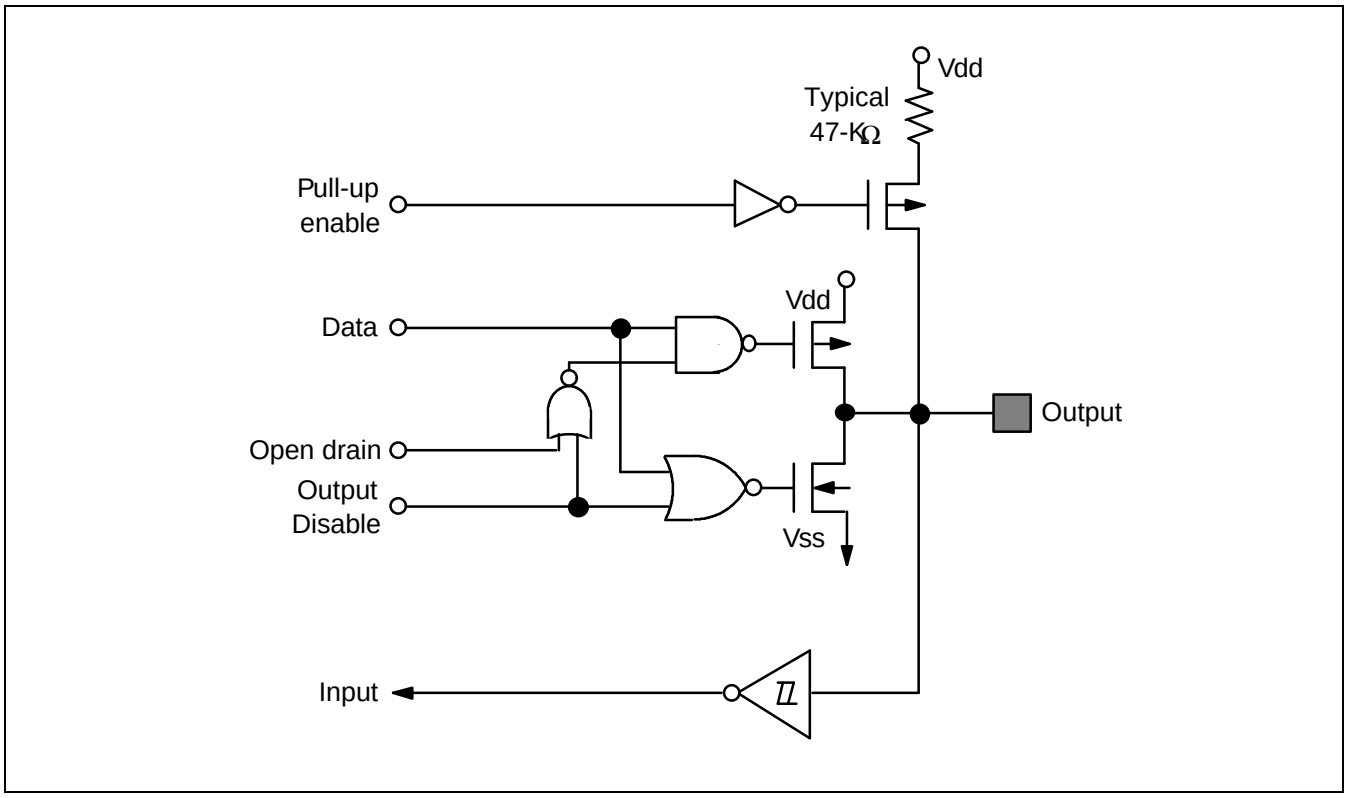


Figure 1-7. Pin Circuit Type E

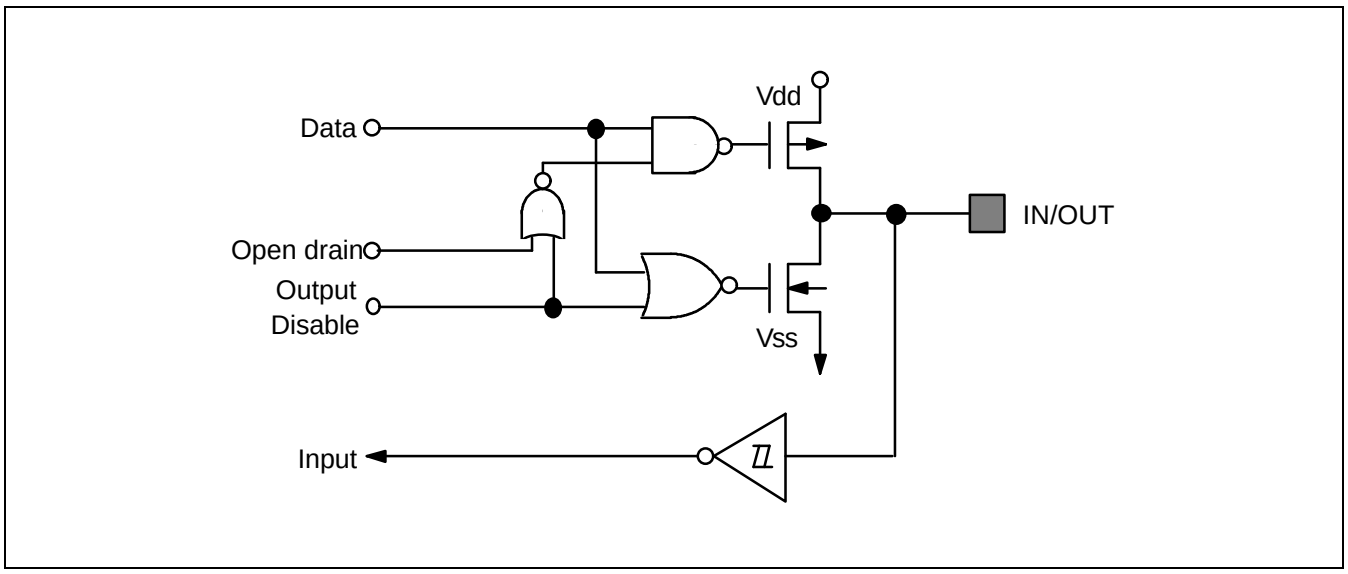


Figure 1-8. Pin Circuit Type E-1

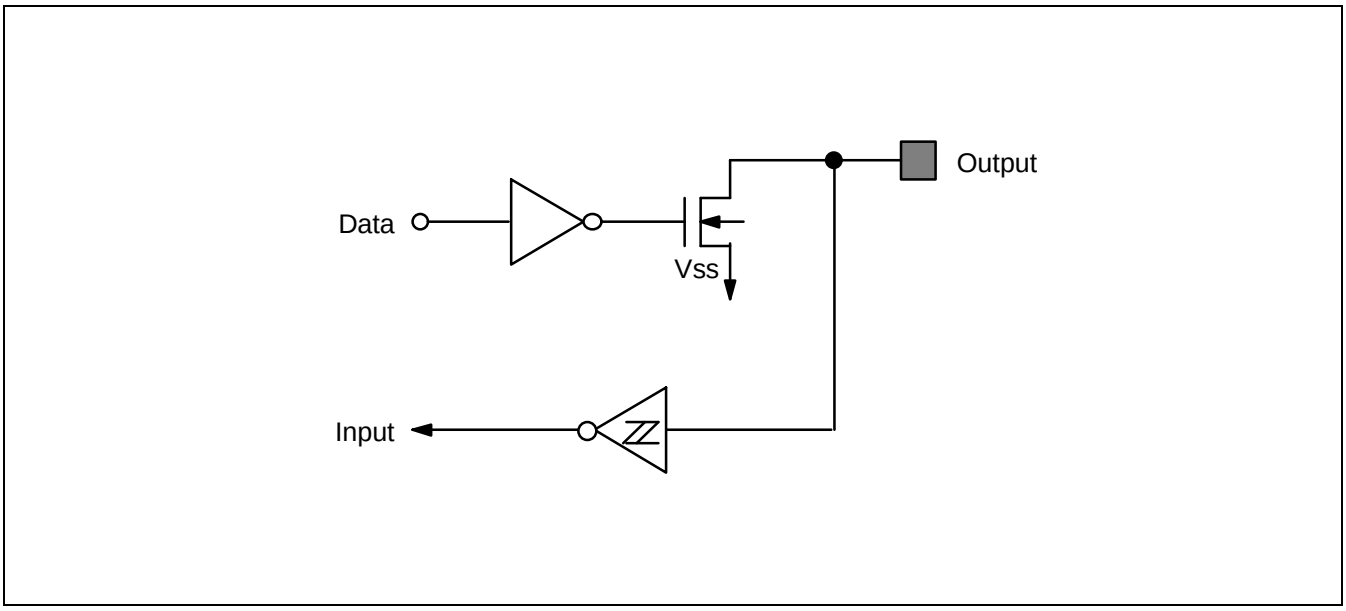


Figure 1-9. Pin Circuit Type G-3

16 ELECTRICAL DATA

OVERVIEW

In this section, S3C8618/C8615 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— D.C. electrical characteristics
— I/O capacitance
— A.C. electrical characteristics
— Oscillation characteristics
— Oscillation stabilization time
— Schmitt trigger characteristics

Table 16-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	– 0.3 to + 7.0	V
Input voltage	V_{I1}	Type C (n-channel, open-drain)	– 0.3 to + 10	V
	V_{I2}	All port pins except V_{I1}	– 0.3 to V_{DD} + 0.3	
Output voltage	V_O	All output pins	– 0.3 to V_{DD} + 0.3	V
Output current High	I_{OH}	One I/O pin active	– 10	mA
		All I/O pins active	– 60	
Output current Low	I_{OL1}	One I/O pin active	+ 30	mA
	I_{OL2}	Total pin current except port 3	+ 100	
	I_{OL3}	Sync-processor I/O pins and IIC-bus clock and data pins	+ 150	
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C

Table 16-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High voltage	V_{IH1}	All input pins except V_{IH2} and V_{IH3}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}, X_{OUT}	V_{DD} – 0.5		V_{DD}	
	V_{IH3}	TTL input (HsyncI, VsyncI and CsyncI)	2.0		V_{DD}	
Input Low voltage	V_{IL1}	All input pins except V_{IL2} and V_{IL3}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}, X_{OUT}			0.4	
	V_{IL3}	TTL input (HsyncI, VsyncI and CsyncI)			0.8	
Output High voltage	V_{OH1}	V_{DD}= 4.5 V to 5.5 V I_{OH} = – 8 mA Port 1 only	V_{DD} – 1.0	–	–	V
	V_{OH2}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 2 mA Ports 0, 2, ClampO, H and VsyncO	V_{DD} – 1.0			
	V_{OH3}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 6 mA, Port 3	V_{DD} – 1.0			

Table 16-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Low voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 8 mA, port 1 only	–	–	0.4	V
	V_{OL2}	I_{OL} = 2 mA Port 0, 2, ClampO, HsyncO and VsyncO			0.4	
	V_{OL3}	I_{OL} = 6 mA Port 3, SCL and SDA			0.4	
Input High leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN}, X_{OUT}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{OUT} only	–	–	20	
	I_{LIH3}	V_{IN} = V_{DD} X_{IN} only	2.5	6	20	
Input Low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT} and RESET	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V; X_{OUT} only	–	–	– 20	
	I_{LIL3}	V_{IN} = 0 V; X_{IN} only	– 2.5	– 6	– 20	
Output High leakage current	I_{LOHL}	V_{OUT} = V_{DD} All output pins except port 1	–	–	3	µA
Output Low leakage current	I_{LOL}	V_{OUT} = 0 V	–	–	– 3	µA
Pull-up resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 4.5 V to 5.5 V Port 3	20	47	80	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 4.5 V to 5.5 V RESET only	150	280	480	
Supply current (note)	I_{DD1}	V_{DD} = 4.5 V to 5.5 V 12 MHz CPU clock	–	15	30	mA
	I_{DD2}	Idle mode; V_{DD} = 4.5 V to 5.5 V 12 MHz CPU clock		5	10	
	I_{DD3}	Stop mode; V_{DD} = 5.0 V		1	10	µA

NOTE: Supply current does not include drawn internal pull–up resistors and external loads of output.

Table 16-3. Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Stop mode	2	–	6	V
Data retention supply current	I_{DDDR}	Stop mode, V_{DDDR} = 2.0 V	–	–	5	µA

NOTES:
1. During the oscillator stabilization wait time (t_{WAIT}), all CPU operations must be stopped.
2. Supply current does not include drawn through internal pull–up resistors and external output current loads.

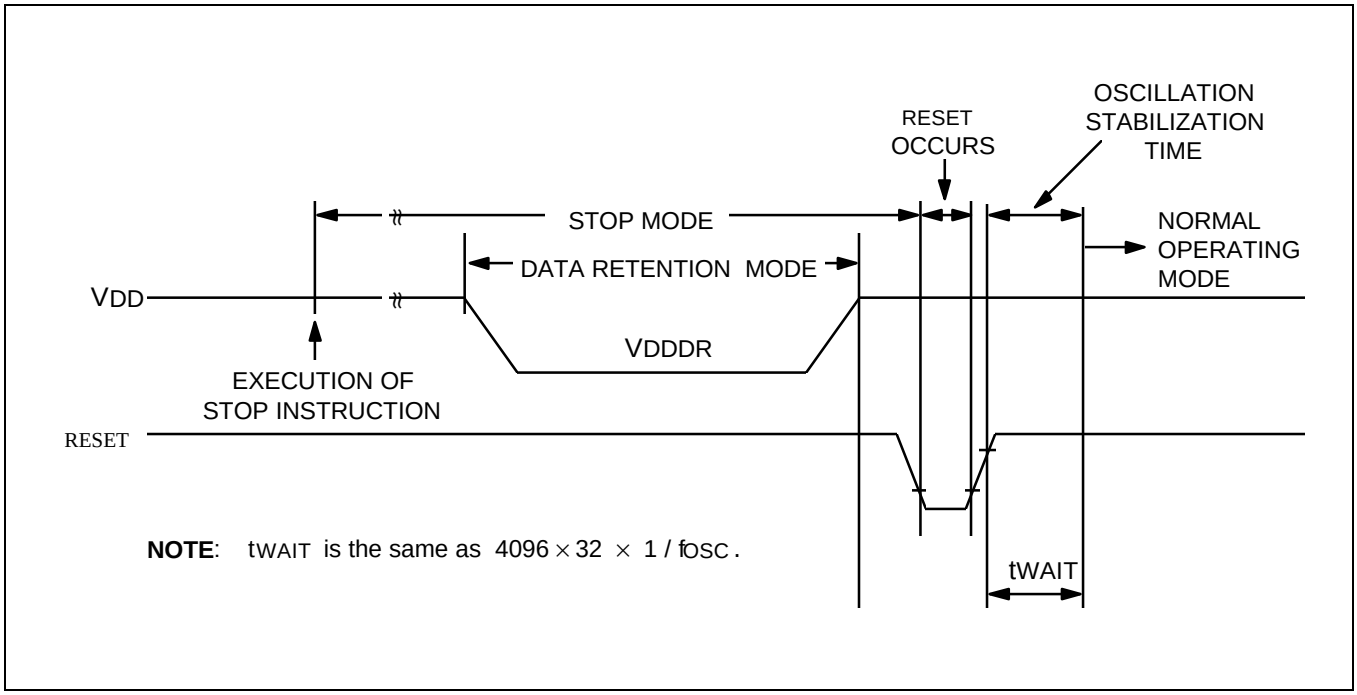


Figure 16-1. Stop Mode Release Timing When Initiated by a Reset

Table 16-4. Input/Output Capacitance

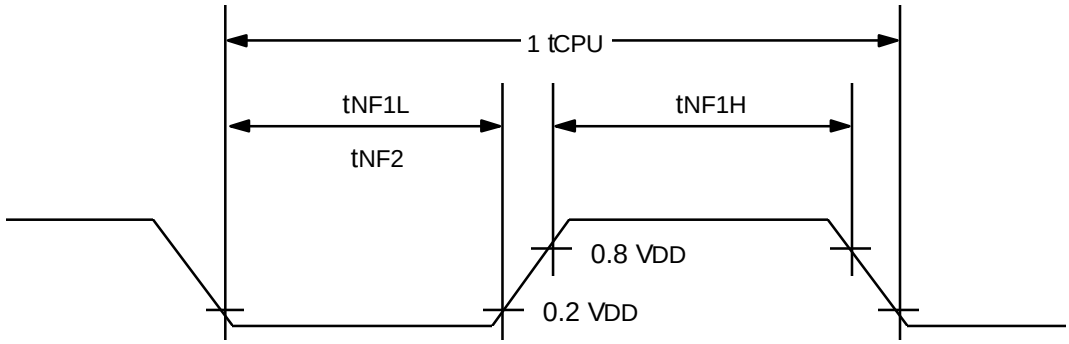
(T_A = – 40 °C to + 85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 16-5. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.5 V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Noise Filter	t_{NF1H}, t_{NF1L}	P0.2–P0.0, T0CAP and T1CK (RC delay)	300	–	–	ns
	t_{NF2}	RESET only (RC delay)	800	–	–	

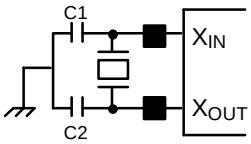
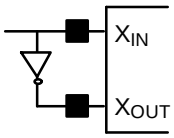


NOTE: The unit tCPU means one CPU clock period.

Figure 16-2. Input Timing Measurement Points for P0.0–P0.2, T0CAP and T1CK

Table 16-6. Oscillation Characteristics

(T_A = – 40 °C + 85 °C)

Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Main crystal or ceramic		V_{DD} = 4.5 V to 5.5 V	6	–	12	MHz
External clock (main)		V_{DD} = 4.5 V to 5.5 V	6	–	12	MHz

NOTE: The maximum oscillator frequency is 12 MHz. If you use an oscillator frequency higher than 12 MHz, you cannot select a non-divided CPU clock using CLKCON settings. That is, you must select one of the divide-by values.

Table 16-7. Recommended Oscillator Constants

(T_A = – 40 °C + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Manufacturer	Product Name	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
		C1	C2	MIN	MAX	
TDK	FCR8.0MC5 (note)	–	–	4.5	5.5	On-chip C Leaded Type
	FCR8.0M5	33	33	4.5	5.5	Leaded Type
	CCR8.0MC5 (note)	–	–	4.5	5.5	On-chip C SMD Type

NOTE: On-chip C: 30 pF ± 20 % built in.

Table 16-8. Oscillation Stabilization Time

(T_A = – 40 °C + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	V_{DD} = 4.5 V to 5.5 V	–	–	20	ms
Ceramic	V_{DD} = 4.5 V to 5.5V	–	–	10	
External clock	X_{IN} input High and Low level width (t_{XH}, t_{XL})	25	–	500	ns

NOTE: Oscillation stabilization time is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is released.

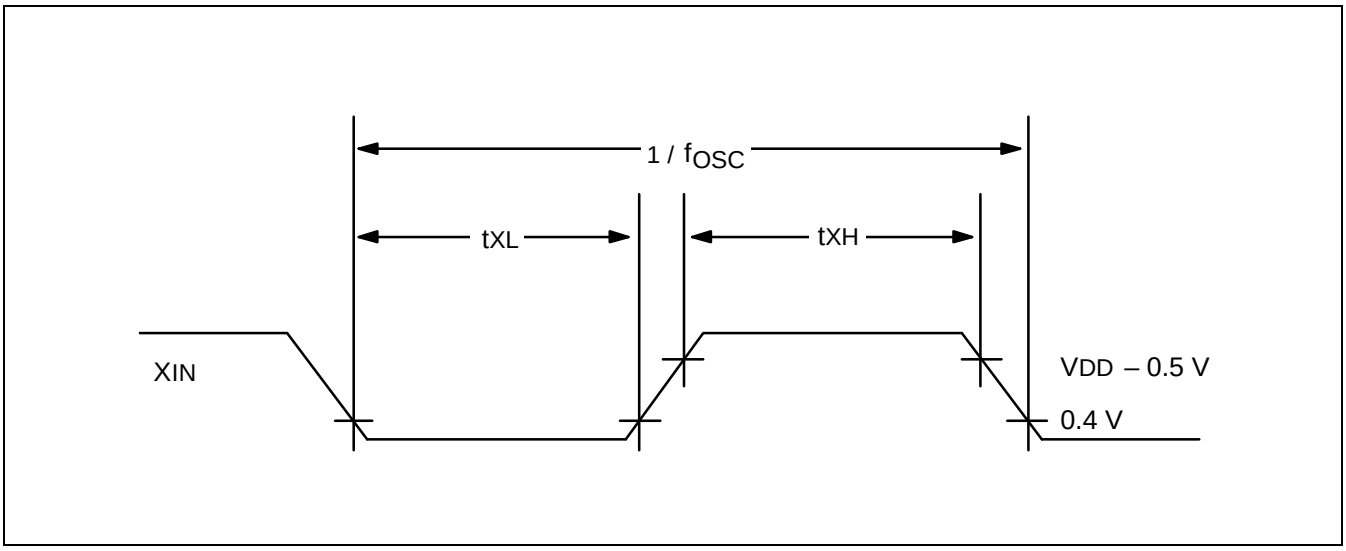


Figure 16-3. Clock Timing Measurement Points for X_{IN}

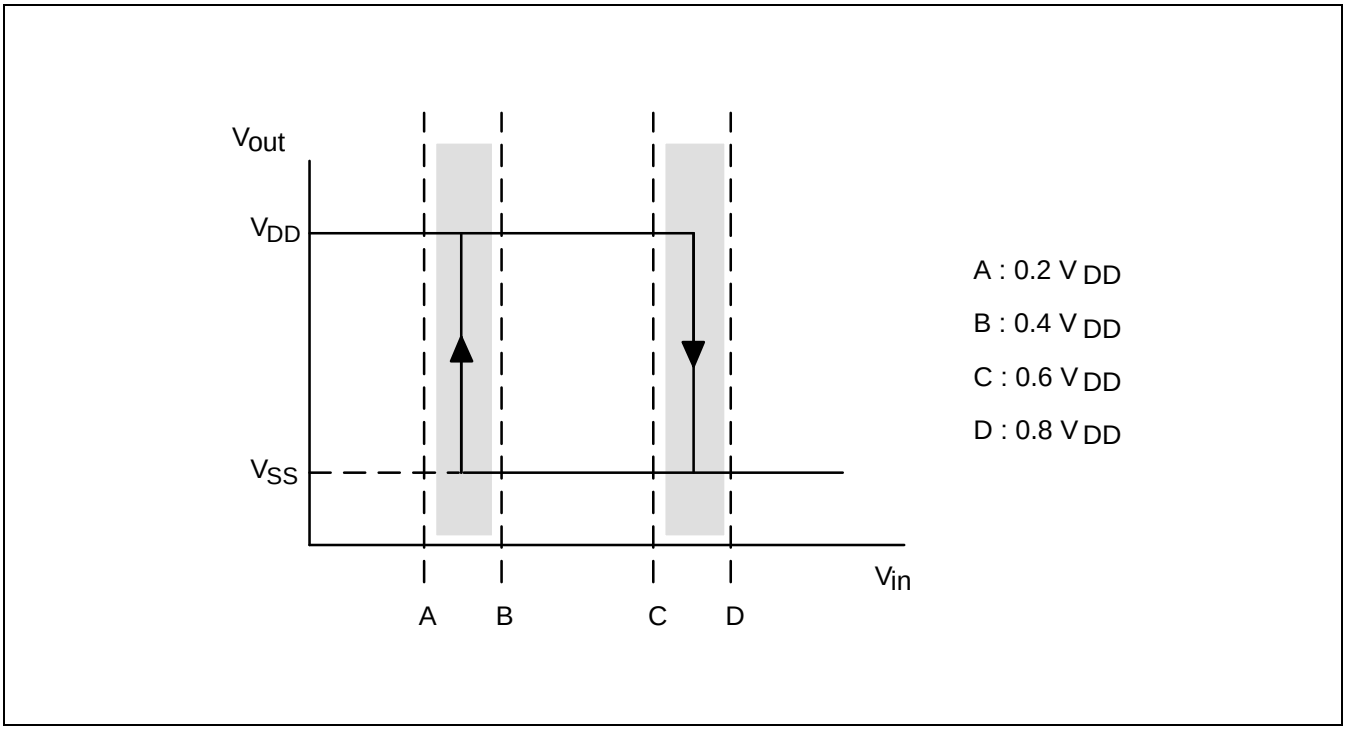


Figure 16-4. Schmitt Trigger Characteristics (Normal Port; except TTL Input)

17 MECHANICAL DATA

OVERVIEW

The S3C8615 microcontroller is available in a 42-pin SDIP package (Samsung part number 42-SDIP-600) and a 44-QFP package (Samsung part number 44-QFP-1010B).

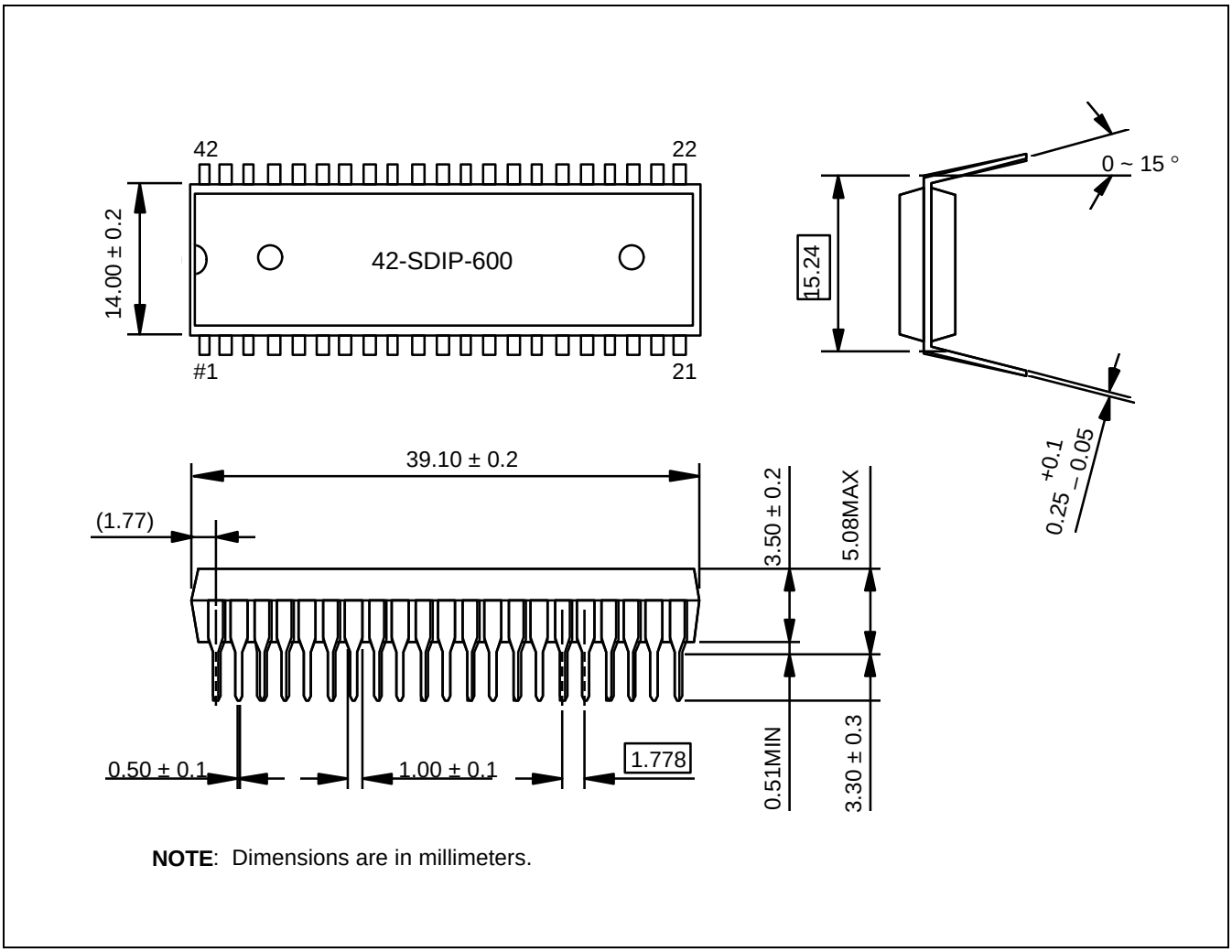
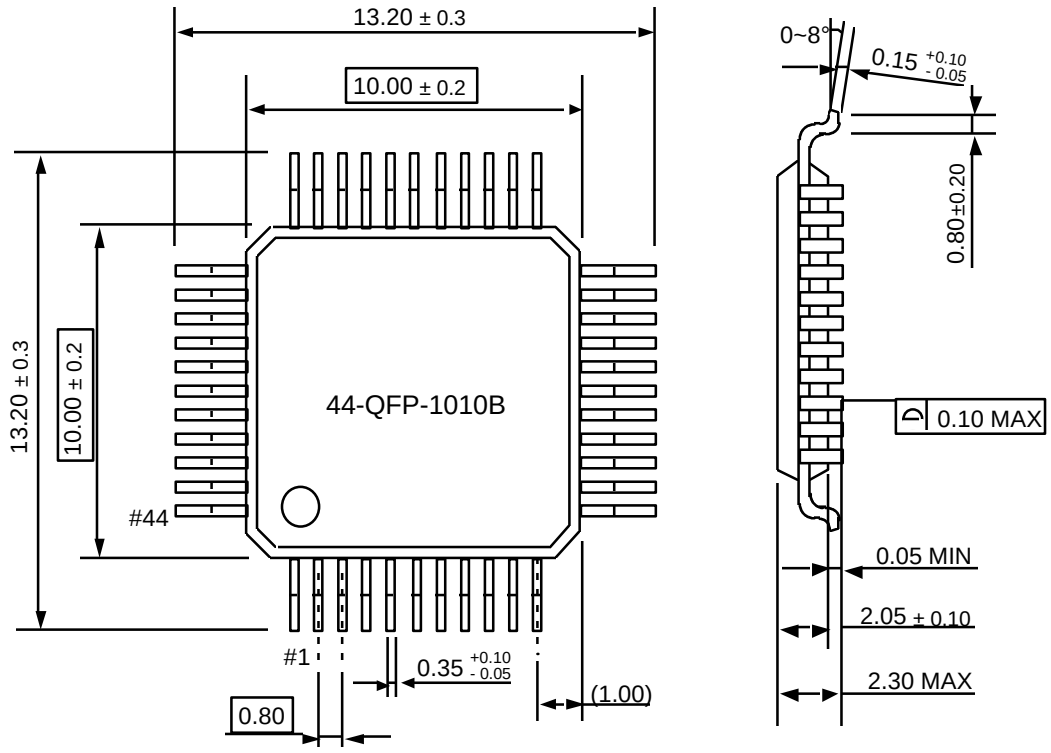


Figure 17-1. 42-Pin SDIP Package Mechanical Data (42-SDIP-600)



NOTE: Dimensions are in millimeters.

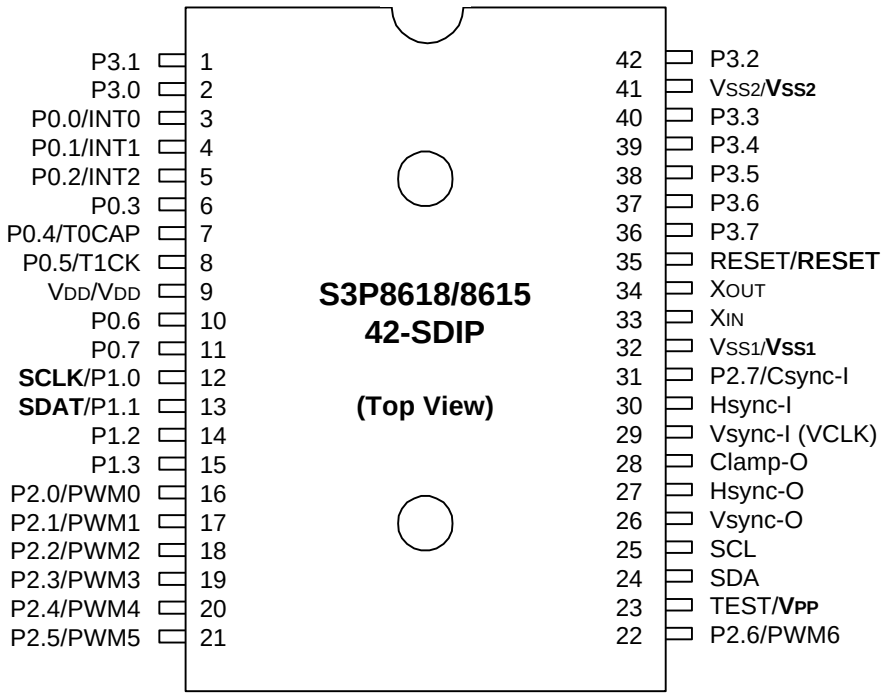
Figure 17-2. 44-Pin QFP Package Mechanical Data (44-QFP-1010B)

18 S3P8615 OTP

OVERVIEW

The S3P8615 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3P8615 microcontrollers. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P8615 is fully compatible with the S3C8618/C8615, both in function and in pin configuration. Because of its simple programming requirements, the S3P8615 is ideal for use as an evaluation chip for the S3C8618/C8615.



NOTE: The bolds indicate an OTP pin name.

Figure 18-1. S3P8615 Pin Assignments (42-SDIP Package)

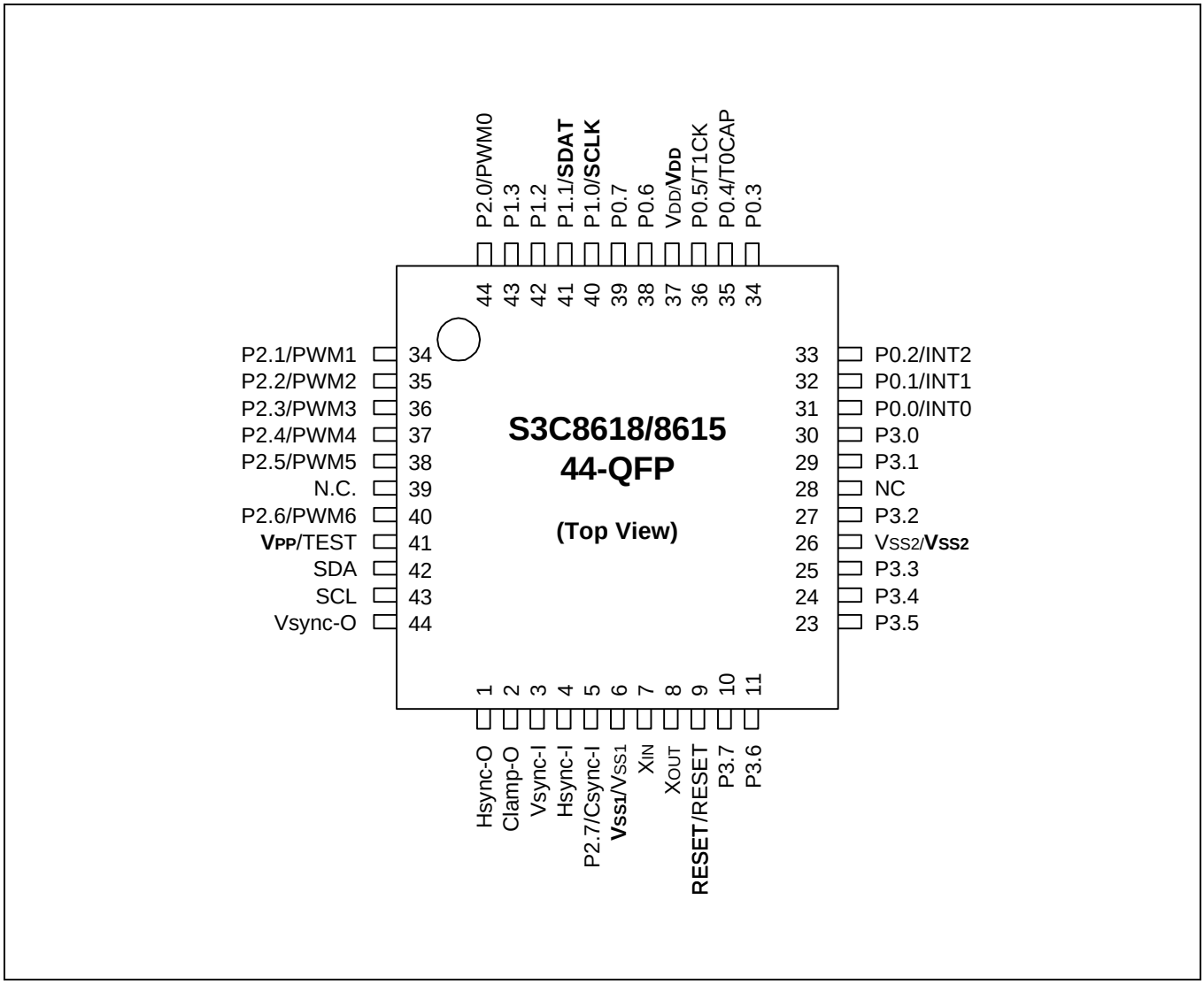


Figure 18-2. S3P8615 Pin Assignments (44-QFP Package)

Table 18-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P1.1	SDAT	13 (*30)	I/O	Serial DATa Pin (Output when reading, Input when writing) Input & Push-pull Output Port can be assigned
P1.0	SCLK	12 (*29)	I	Serial CLocK Pin (Input Only Pin)
TEST	V_{PP} (TEST)	23 (*41)	I	EPROM Cell Writing Power Supply Pin (Indicates OTP Mode Entering) When writing 12.5 V is applied and when reading 5V is applied.(Option)
RESET	RESET	35 (*9)	I	Chip Initialization
$V_{DD}/V_{SS1}/V_{SS2}$	$V_{DD}/V_{SS}/V_{SS}$	9 / 32 / 41 (*26 / 6 / 15)	I	Logic Power Supply Pin. V_{DD} should be tied to 5 V during programming.

NOTE: * means the 44-QFP OTP pin number.

Table 18-2. Comparison of S3P8615 and S3C8618/C8615 Features

Characteristic	S3P8615	S3C8618/C8615
Program Memory	16 K byte EPROM	16 K byte mask ROM
Operating Voltage (V_{DD})	4.5 V to 5.5 V	4.5 V to 5.5V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST)=12.5V	
Pin Configuration	42-SDIP, 44-QFP	42-SDIP, 44-QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the S3P8615, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 18-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/ MEM	ADDRESS (A15–A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

D.C. ELECTRICAL CHARACTERISTICS

Table 18-4. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High leakage current	I_{LIH1}	V_{IN} = V_{DD}; All input pins except X_{IN}, X_{OUT}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD}; X_{OUT} only			20	
	I_{LIH3}	V_{IN} = V_{DD}; X_{IN} only	2.5	6	20	
Input Low leakage current	I_{LIL1}	V_{IN} = 0 V; All input pins except X_{IN}, X_{OUT} and RESET	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V; X_{OUT} only	–	–	– 20	
	I_{LIL3}	V_{IN} = 0 V; X_{IN} only	– 2.5	– 6	– 20	
Output High leakage current	I_{LOH1}	V_{OUT} = V_{DD}	–	–	3	µA
Output Low leakage current	I_{LOL1}	V_{OUT} = 0 V	–	–	– 3	µA
Supply current	I_{DD1}	Normal operating mode; 12 MHz CPU clock	–	15	30	mA
	I_{DD2}	IDLE mode; 12 MHz CPU clock		5	10	
	I_{DD3}	Stop mode; V_{DD} = 5.0 V	–	1	10	µA
Data retention supply voltage	V_{DDDR}	Stop mode	2	–	6	V
Data retention supply voltage	I_{DDDR}	Stop mode; V_{DDDR} = 2V	–	–	5	µA

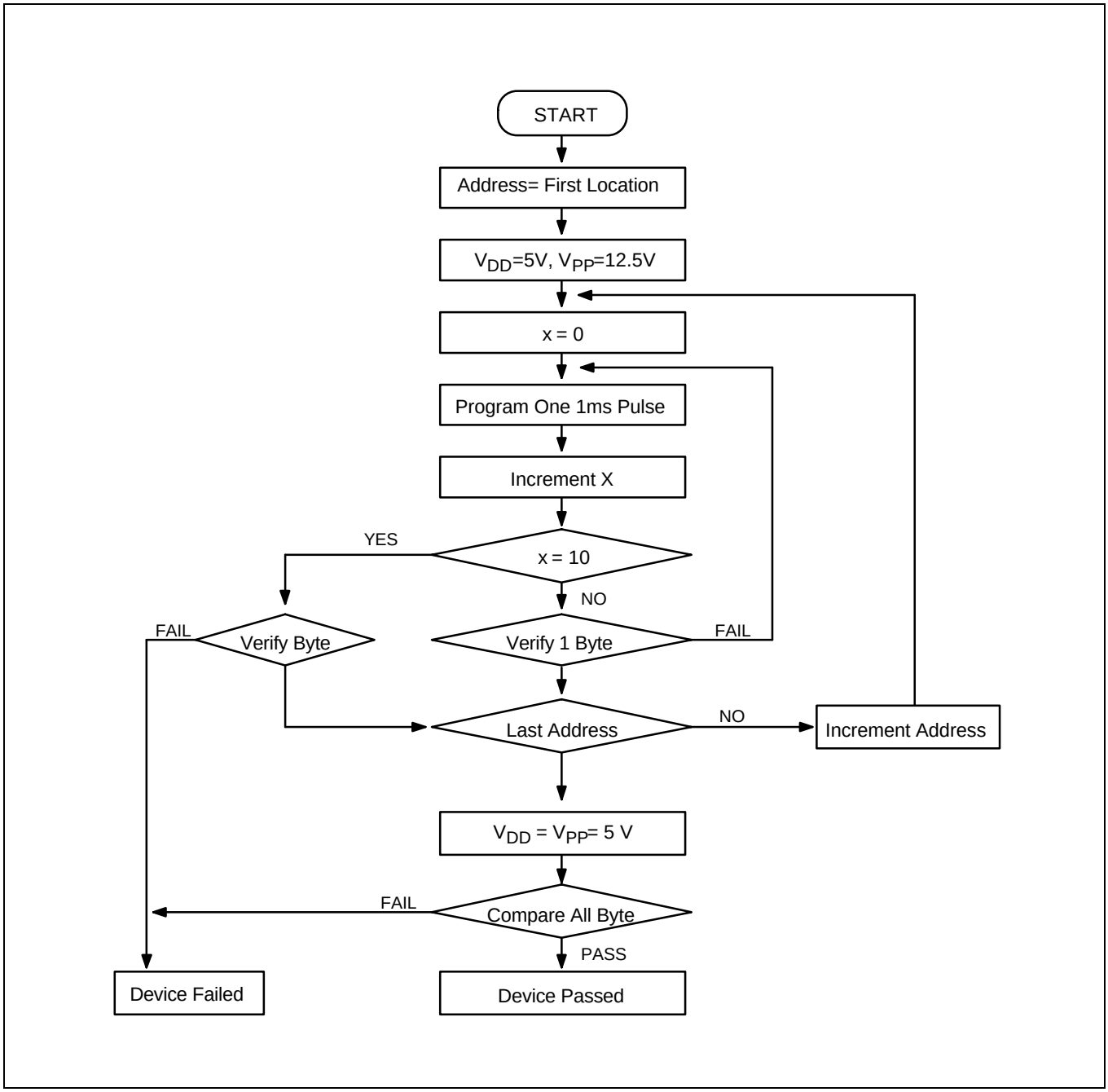


Figure 18-3. OTP Programming Algorithm