S3F49FAX

for Compact Flash

SPECIFICATION

Revision 1.0

HELP DESK
Sejin, Ahn (herlock@sec.samsung.com)
Sanghun, Song (hoontour@samsung.com)

SAMSUNG ELECTRONICS

Table of Contents

1.1 Introduction 2
1.2 Features 3
1.3 Block Diagram 4
2.1 Controller Package Drawing 5
2.2 Controller Pin Assignments and Pin Type 6

Table of Figures

1 S3F49FAX Block Diagram 4
2 S3F49FAX Pin Assignment 5
3 100-TQFP-1414 Package Dimension 26

Table of Tables

1 100-Pin TSOP Pin Assignment 6
2 I/O Type Description 10
3 Signal Description for PCMCIA/IDE Interface 11
4 Signal Description for Flash Memory Interface 17
5 Signal Description for Miscellaneous Part 20
6 Signal Description for Power Signal 21
7 Signal Description for USB Device 21
8 Signal Description for Internal NOR Flash Memory 21
9 Absolute Maximum Ratings 22
10 Recommended Operating Conditions 22
11 Thermal Characteristics 22
12 D.C. Electrical Characteristics (In case of 3.3V Interface I/O) 23
13 D.C. Electrical Characteristics (In case of 5.0V Interface I/O) 24
14 System Clock Timing 25
15 POR(power on reset) Detection Level 25

1.1 INTRODUCTION

Samsung's S3F49FAX is NAND flash memory controller which can control flash memories as solid state disk. It provides PC Card ATA/IDE/USB interface, host and flash transfer rates up to 20.0MB/S. S3F49FAX can control flash memory maximum 8 pieces. The device is designed using 0.35um CMOS process, assembled as 100-TQFP package. It supports operation in both 5.0V and 3.3V.

An outstanding feature of the S3F49FAX flash disk controller is its CPU core: the ARM7TDMI 16/32-bit RISC processor, designed by Advanced RISC Machine (ARM), Ltd. The ARM core is a low-power, general purpose, microprocessor macro-cell that was developed for use in application-specific and customer-specific integrated circuit. It is simple, elegant, and fully static design is particularly suitable for cost and power sensitive application.

- PC Card-ATA/True IDE/CompactFlash/USB compatible host interface
- Automatic sensing of PC Card ATA and IDE
- Full Speed USB Function Controller compatible with the USB Specification Version 1.1
- Included 256-byte CIS RAM
- Five PC Card ATA addressing modes
- Host data transfer rate: 20MB/s
- Flash data transfer rate: 20MB/s
  (It depends on the characteristics of flash memory)
- Host Interface: 8/16-bit Access
- Flash Interface: 8-bit Access
- Support 3 power save mode: SLEEP/ACTIVE mode
  (Auto power down function)
- Support 128/256/512Mbit, 1Gbit, 2Gbit, 4Gbit NAND flash memory made by Samsung

NAND Flash Density	Min. / Max. Capacity (number of flash)
128M/256M/512M/1G bit (512Byte/page)	16MB / 1 G Byte (Up to 8EA)
1G / 2G / 4G bit (2048Byte/page)	256MB / 4 G Byte (Up to 8EA)

- ECC function (Error correction algorithm): 2bit correction
- Available 100-pin TQFP
- Interface Voltage Range : 3.0 to 5.5V
- Interface Support

Controller Part Number	Host interface
S3F49FAXZZ	CompactFlash
S3F49FAXZA	USB 1.1

1.2 FEATURES

Microprocessor Architecture

- 16/32bit RISC architecture
- Efficient and powerful ARM7TDMI CPU core
- Cost-effective JTAG based debug solution

Internal Memory

- Included 48KB internal NOR FLASH
- Included 16KB internal SRAM

DMA Controller

- Two-channel,general-purpose DMA controller
- Data transfer between SRAM and Flash, SRAM and USB without CPU Intervention
- Support for 8/16/32bit data transfers
- Increment or decrement of source or destination address

Programmable Timer

- channel 16bit programmable timer

Interrupts

- 8 interrupt sources
- Normal or fast interrupt modes (IRQ, FIQ)

PC-Card/ATA Interface

- Include 256Bytes SRAM for CIS
- Support memory and I/O addressing mode
- Support True IDE mode

USB Device

- Full Speed USB Function Controller compatible with the USB Specification Version 1.1
- DMA Interface for Bulk Transfer
- 5 Endpoint with FIFO
- Integrated USB Transceiver (ASIC Full speed USB Pad)

ECC Engine

- Correct 2-bit Error

64bit Counter

- 64bit timer by cascading the 32-bit timers.

Interface Voltage Range

- 3.0 to 5.5 volts

Package Type

- 100-TQFP

1.3 BLOCK DIAGRAM

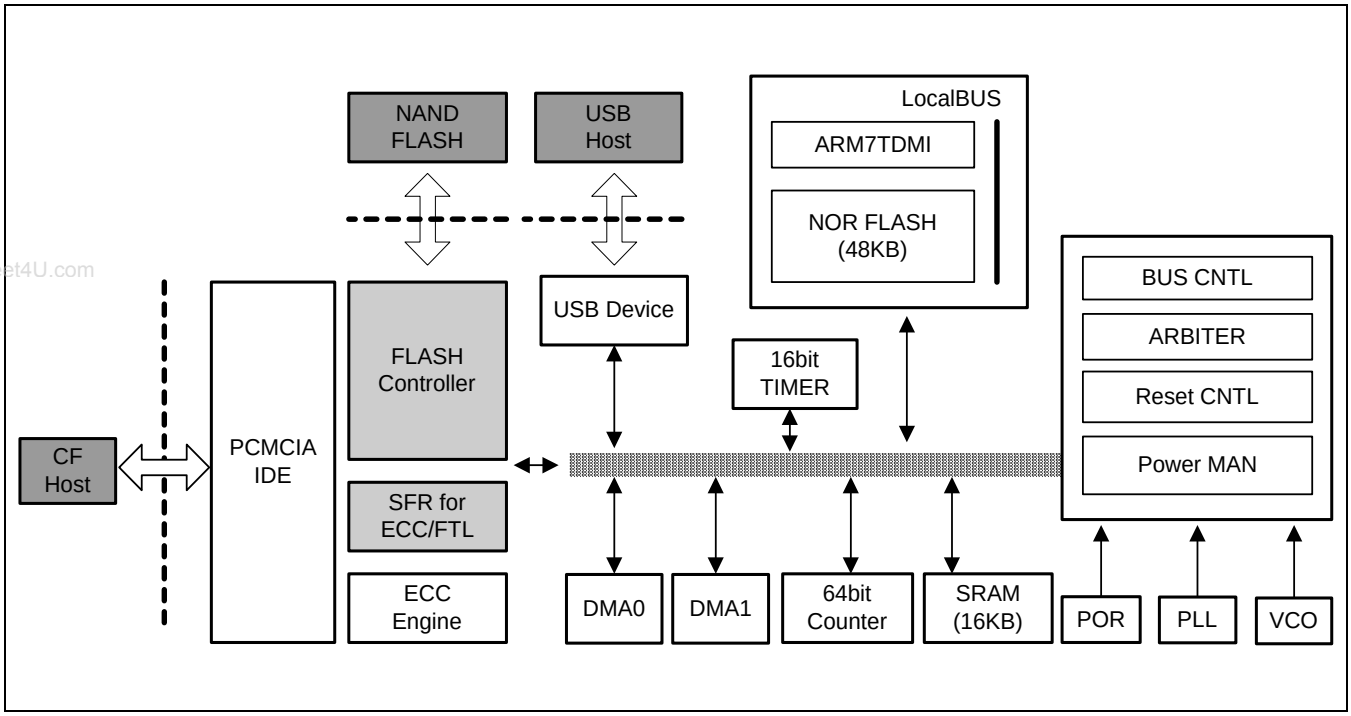

Figure 1. S3F49FAX Block Diagram

2 PIN INFORMATION

2.1 CONTROLLER PACKAGE DRAWING

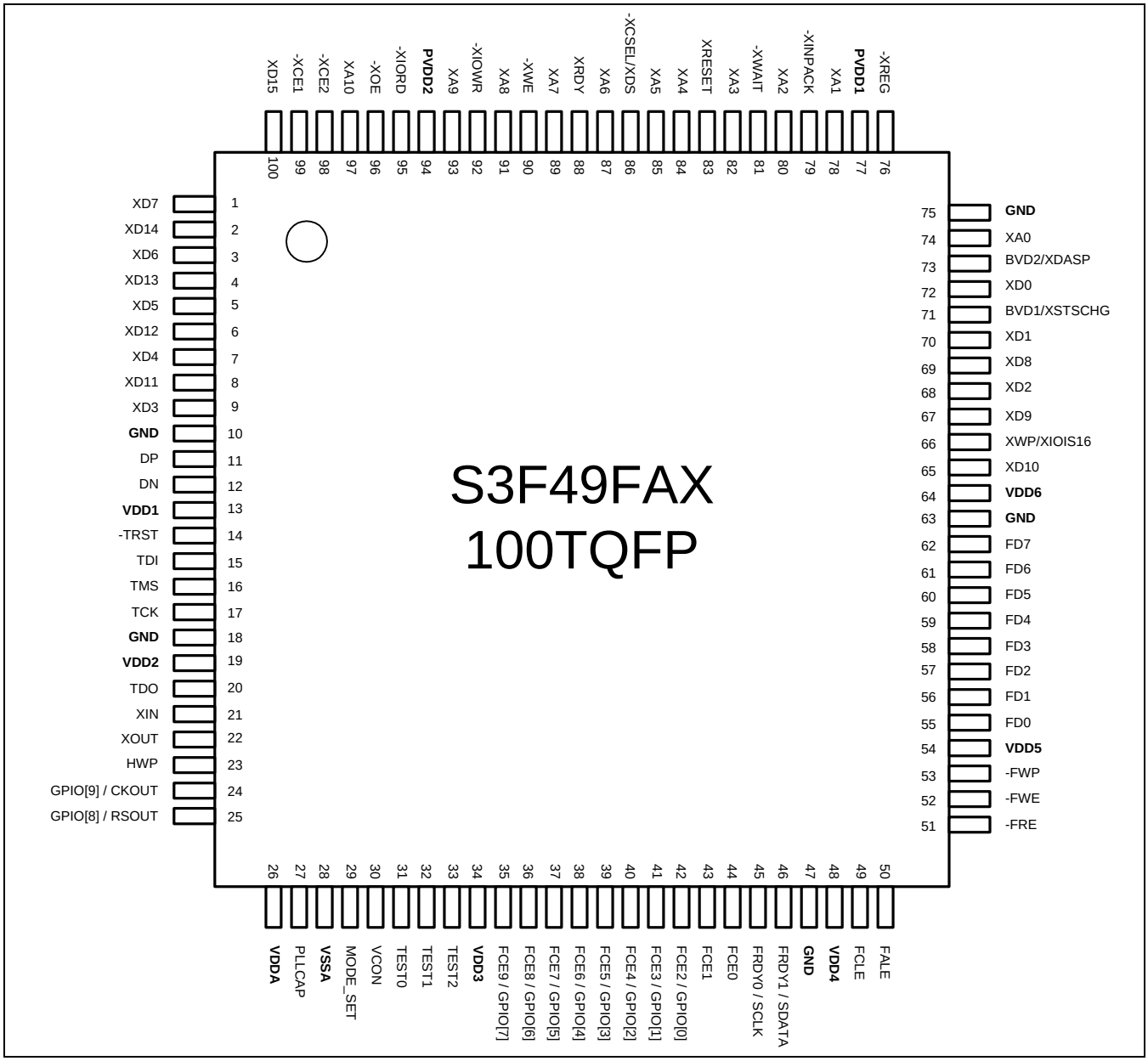

Figure 2. S3F49FAX Pin Assignment

2.2 CONTROLLER PIN ASSIGNMENTS AND PIN TYPE

Table 1. 100-Pin TSOP Pin Assignment

Pin No.	Pin Name	I/O State	I/O Type	Function
1	XD7	I/O	pvbct83	Data bus of PCMCIA
2	XD14	I/O	pvbct83	Data bus of PCMCIA
3	XD6	I/O	pvbct83	Data bus of PCMCIA
4	XD13	I/O	pvbct83	Data bus of PCMCIA
5	XD5	I/O	pvbct83	Data bus of PCMCIA
6	XD12	I/O	pvbct83	Data bus of PCMCIA
7	XD4	I/O	pvbct83	Data bus of PCMCIA
8	XD11	I/O	pvbct83	Data bus of PCMCIA
9	XD3	I/O	pvbct83	Data bus of PCMCIA
10	GND	P		Ground
11	DP	I/O	pbusb1	Positive data for USB
12	DN	I/O	pbusb1	Negative data for USB
13	VDD1	P		Power
14	-TRST	I	pis	Test reset for JTAG
15	TDI	I	pis	Test data input for JTAG
16	TMS	I	pis	Test mode select for JTAG
17	TCK	I	pis	Test clock for JTAG
18	GND	P		Ground
19	VDD2	P		Power
20	TDO	O	pob4	Test data output for JTAG
21	XIN		psoscm26	Crystal Input
22	XOUT		psoscm26	Crystal Output
23	HWP	I	pic	Disable write command
24	CKOUT / *GPIO[9]*	I/O	pbct4	Output of Clock signal / *General I/O pin*
25	RSOUT / *GPIO[8]*	I/O	pbct4	Output of Rest signal / *General I/O pin*

Table 1. 100-Pin TSOP Pin Assignment (Continued)

Pin No.	Pin Name	I/O State	I/O Type	Function
26	VDDA	P		Analog Power for PLL
27	PLLCAP		apad_80	Capacitor for PLL
28	VSSA	P		Analog Ground for PLL
29	MODE_DET	I	pic	Select Interface Mode
30	VCON	I	pica	Reference Voltage for VCO
31	TEST0	I	pic	Select test mode
32	TEST1	I	pic	Select test mode
33	TEST2	I	pifsn	Select test mode
34	VDD3	P		Power
35	FCE9 / *GPIO[7]*	*I/O*	pbct4sm	Enable 9 chip of nand flash / *General I/O PIN*
36	FCE8 / *GPIO[6]*	*I/O*	pbct4sm	Enable 8 chip of nand flash / *General I/O PIN*
37	FCE7/ *GPIO[5]*	*I/O*	pbct4sm	Enable 7 chip of nand flash / *General I/O PIN*
38	FCE6/ *GPIO[4]*	*I/O*	pbct4sm	Enable 6 chip of nand flash / *General I/O PIN*
39	FCE5/ *GPIO[3]*	*I/O*	pbct4sm	Enable 5 chip of nand flash / *General I/O PIN*
40	FCE4/ *GPIO[2]*	*I/O*	pbct4sm	Enable 4 chip of nand flash / *General I/O PIN*
41	FCE3/ *GPIO[1]*	I/O	pbct4sm	Enable 3 chip of nand flash / *General I/O PIN*
42	FCE2 / *GPIO[0]*	I/O	pbct4sm	Enable 2 chip of nand flash / *General I/O PIN*
43	FCE1	O	pob4sm	Enable 1 chip of nand flash
44	FCE0	O	pob4sm	Enable 0 chip of nand flash
45	FRDY0 / SCLK	I	Picu	Ready/Busy signal of nand flash / Serial data for internal flash
46	FRDY1 / SDATA	I/O	Pbcut4	Ready/Busy signal of nand flash / Serial clock for internal flash
47	GND	P		Ground

Table 1. 100-Pin TSOP Pin Assignment (Continued)

Pin No.	Pin Name	I/O State	I/O Type	Function
48	VDD4	P		Power
49	FCLE	O	pob4sm	Command latch enable in nand flash
50	FALE	O	pob4sm	Address latch enable in nand flash
51	-FRE	O	pob8	Read enable in nand flash
52	-FWE	O	pob4	Write enalbe in nand flash
53	-FWP	O	pob4sm	Write protect in nand flash
54	VDD5	P		Power
55	FD0	I/O	pbcdt4	I/O of nand flash memory
56	FD1	I/O	pbcdt4	I/O of nand flash memory
57	FD2	I/O	pbcdt4	I/O of nand flash memory
58	FD3	I/O	pbcdt4	I/O of nand flash memory
59	FD4	I/O	pbcdt4	I/O of nand flash memory
60	FD5	I/O	pbcdt4	I/O of nand flash memory
61	FD6	I/O	pbcdt4	I/O of nand flash memory
62	FD7	I/O	pbcdt4	I/O of nand flash memory
63	GND	P		Ground
64	VDD6	P		Power
65	XD10	I/O	pvbct83	Data bus of PCMCIA
66	XWP / IOIS16	O	pvot83	IOIS16 of PCMCIA (XIOSI16)
67	XD9	I/O	pvbct83	Data bus of PCMCIA
68	XD2	I/O	pvbct83	Data bus of PCMCIA
69	XD8	I/O	pvbct83	Data bus of PCMCIA
70	XD1	I/O	pvbct83	Data bus of PCMCIA
71	BVD1 / XSTSCHG	I/O	pvbcut43	STSCHG of PCMCIA (XIOIS16)
72	XD0	I/O	pvbct83	Data bus of PCMCIA
73	BVD2 / XDASP	I/O	pvbcut43	DASP for IDE (XDASP)
74	XA0	I	pvic3	Address bus of PCMCIA
75	GND	P		Ground

Table 1. 100-Pin TSOP Pin Assignment (Continued)

Pin No.	Pin Name	I/O State	I/O Type	Function
76	-XREG	I	pvisu3	REG of PCMCIA
77	PVDD1	P		Power
78	XA1	I	pvic3	Address bus of PCMCIA
79	-XINPACK	O	pvob43	INPACK of PCMCIA
80	XA2	I	pvic3	Address bus of PCMCIA
81	-XWAIT	O	pvob43	Wait signal of PCMCIA
82	XA3	I	pvic3	Address bus of PCMCIA
83	XRESET	I	pvit3	Host reset signal in PCMCIA
84	XA4	I	pvic3	Address bus of PCMCIA
85	XA5	I	pvic3	Address bus of PCMCIA
86	-XCSEL/XDS	I	pvitu3	Master/Slave selection signal (XDS)
87	XA6	I	pvic3	Address bus of PCMCIA
88	XRDY	O	pvot43	Ready/Busy signal of PCMCIA
89	XA7	I	pvic3	Address bus of PCMCIA
90	-XWE	I	pvisu3	Wrtie enable in PCMCIA
91	XA8	I	pvic3	Address bus of PCMCIA
92	-XIOWR	I	pvisu3	IO write signal in PCMCIA
93	XA9	I	pvic3	Address bus of PCMCIA
94	PVDD2	P		Power
95	-XIORD	I	pvisu3	IO read signal in PCMCIA
96	-XOE	I	pvisu3	Output enable in PCMCIA
97	XA10	I	pvic3	Address bus of PCMCIA
98	-XCE2	I	pvisu3	Card enable 2 in PCMCIA
99	-XCE1	I	pvisu3	Card enable 1 in PCMCIA
100	XD15	I/O	pvbct83	Data bus of PCMCIA

Table 2. I/O Type Description

I/O Type	Description
pic	3.3V LVCMOS Level Input Buffers
picu	3.3V LVCMOS Level Input Buffer with pull-up register
picd	3.3V LVCMOS Level Input Buffer with pull-down register
pica	VCO output frequency control PAD
pvic3	5V/3.3V LVCMOS Level PCMCIA Input Buffer
pvisu3	5V/3.3V LVCMOS Schmitt Trigger Level PCMCIA Input Buffer with Pull-up Resistor
pvitu3	5V/3.3V TTL Level PCMCIA Input Buffer with Pull-up Resistor
pvit3	5V/3.3V TTL Level PCMCIA Input Buffer
pfisn_80	High voltage Input tolerant pad
pob4	4mA LVCMOS Normal Output Buffers
pob4sm	4mA LVCMOS Normal Output Buffers with Medium Slew-Rate
pob8	8mA LVCMOS Normal Output Buffers
pvot43	5V/3.3V 4mA Tri-State PCMCIA Output Buffer without SRC
pvot83	5V/3.3V 8mA Tri-State PCMCIA Output Buffer without SRC
Apad_80	Analog Output for PLL capacitor
Pbct4	3.3V LVCMOS Level Input Buffer and 4mA Tri-State Output Buffers
pbcut4	3.3V LVCMOS Level Input Buffer with Pull-up Resistor and 4mA LVCMOS Tri-State Output Buffer
pbcdt4	3.3V LVCMOS Level Input Buffer with Pull-down Resistor and 4mA LVCMOS Tri-State Output Buffer
pbct4sm	3.3V LVCMOS level input buffer and 4mA tri-state output buffer with Medium Slew-Rate
pbusb1	3.3V USB differential input receiver, a differential output driver.
pvbct83	5V/3.3V LVCMOS Level PCMCIA Input Buffer and 8mA Tri-State PCMCIA Output Buffer without SRC
pvbcut43	5V/3.3V LVCMOS Level PCMCIA Input Buffer with Pull-up Resistor and 4mA Tri-State PCMCIA Output Buffer without SRC
psoscm26	Oscillator cell with enable and register
pvob43	5V/3.3V 4mA PCMCIA Output Buffer witout SRC

2.3 Signal descriptions

Table 3. Signal Description for PCMCIA/IDE Interface

Signal Name	100-Pin Number	I/O	Description
XA0	74	I	ADDRESS BUS[10:0]: These address lines along with the –REG signal are used to select the following: The I/O port address registers within the PC Storage Card, the memory mapped port address registers within the PC Storage Card, a byte in the Card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal in PC Card I/O mode. In True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
XA1	78		
XA2	80		
XA3	82		
XA4	84		
XA5	85		
XA6	87		
XA7	89		
XA8	91		
XA9	93		
XA10	97		
XD0	72	I/O	DATA BUS[15:0]: These lines carry the Data, Commands and Status information between the host and the controller. XDB0 is the LSB of the even byte of the word. XDB8 is the LSB of the odd byte of the word. This signal is the same as the PC Card memory mode signal in PC Card I/O mode. In True IDE mode, all Task File operations occur in byte mode on the low order bus XDB0-XDB7 while all data transfers are 16 bit using XDB0-XDB15
XD1	70		
XD2	68		
XD3	9		
XD4	7		
XD5	5		
XD6	3		
XD7	1		
XD8	69		
XD9	67		
XD10	65		
XD11	8		
XD12	6		
XD13	4		
XD14	2		
XD15	100		

Table 3. Signal Description for PCMCIA/IDE Interface (Continued)

Signal Name	100-Pin Number	I/O	Description
XREG	76	I	ATTRIBUTE MEMORY AREA SELECTION: This signal is used during memory cycles to distinguish between common memory and register (Attribute) memory accesses. High for Common memory, low for attribute memory. The signal must also be active (low) during I/O cycles when the I/O address is on the Bus. In True IDE mode, this input signal is not used and should be connected to VCC by the host.
XCE1 XCE2	99 98	I	CARD ENABLE: These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multi-plexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on XDB0-XDB7. This signal is the same as the PC card memory mode signal in PC Card I/O mode.In the True IDE mode, CS0 is the chip select for the task file registers while CS1 is used to select the alternate status register and the device control register.
XOE	96	I	OUTPUT ENABLE: This is an output enable strobe generated by the host interface. It is used to read data from the PC Card in memory mode and to read the CIS and configuration registers. In PC Card I/O mode, this signal is used to read the CIS and configuration registers. To enable True IDE mode this input should be grounded by the host.

Table 3. Signal Description for PCMCIA/IDE Interface (Continued)

Signal Name	100-Pin Number	I/O	Description
XWE	90	I	WRITE ENABLE: This is a signal driven by the host and used for strobing memory write data to the registers of the PC Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O mode, this signal is used for writing the configuration registers. In True IDE mode, this input signal is not used and should be connected to VCC by the host.
XWAIT	81	O	WAIT: The -WAIT signal is driven low by the PC Card to signal the host to delay completion of a memory or I/O cycle that is in progress. IORDY: In True IDE mode, this output signal may be used as IORDY.
XWP/ XIOIS16	66	O	I/O PORT IS 16 BITS: Memory mode - The PC Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O operation - When the PC Card is configured for I/O operation pin 24 is used for the -I/O selected is 16-Bit Port (-IOIS16) function. A low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE mode, this output signal is asserted low when this device is expecting a word data transfer cycle.

Table 3. Signal Description for PCMCIA/IDE Interface (Continued)

Signal Name	100-Pin Number	I/O	Description
XINPACK	79	O	INPUT PORT ACKNOWLEDGE: This signal is not used in memory mode. The Input acknowledge signal is asserted by the PC Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the PC Card and the CPU. In True IDE mode, this output signal is not used and should be connected at the host.
XRDY	88	O	READY/BUSY: In memory mode, this signal is set high when the PC Card is ready to accept a new data transfer operation and held low when the card is busy. The host memory card socket must provide a pull-up resistor. At power up and at reset, the RDY/-BSY signal is held low (busy) until the PC Card has completed its power up or reset function. No access of any type should be made to the PC Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The PC Card has been powered up with +RESET continuously disconnected or asserted. I/O operation - After the PC Card has been configured for I/O operation, this signal is used as Interrupt request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE mode, this signal is the active high Interrupt request to the host.
XIORD	95	I	I/O READ: This signal is not used in memory mode.This is an I/O read strobe generated by the host. This signal gates I/O data onto the bus from the PC Card when the card is configured to use the I/O interface. In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Table 3. Signal Description for PCMCIA/IDE Interface (Continued)

Signal Name	100-Pin Number	I/O	Description
XIOWR	92	I	I/O WRITE: This signal is not used in memory mode.The I/O write strobe pulse is used to clock I/O data on the card data bus into the PC Card controller registers when the PC Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge). In True IDE mode, this signal has the same function as in PC Card I/O Mode
BVD1 / XSTSCHG	71	I/O	STATUS CHANGED: This signal is asserted high as the BVD1 signal since a battery is not used with this product.This signal is asserted low to alert the host to changes in the RDY/-BSY and write protect states, while the I/O interface is configured. Its use is controlled by the Card config and status. In the True IDE mode, this input / output is the pass diagnostic signal in the Master/Slave handshake protocol.
XCSEL / XDS	86	I	CARD SELECT: In True IDE mode, this signal is used for configure this device as a master or slave. When it is grounded , the device is configured as a master. When this signal is open, the device is configured as a slave. In I/O and memory mode, this signal is not used.
XRESET	83	I	RESET: When the pin is high, this signal resets the PC Card. The PC Card is reset only at Power up if this pin is left high or open from power-up. The PC Card is also reset when the soft reset bit in the Card Configuration Option Register is set. In the True IDE mode, this input pin is the active low hardware reset from the host.

Table 3. Signal Description for PCMCIA/IDE Interface (Continued)

Signal Name	100-Pin Number	I/O	Description
BVD2/XDASP	73	I/O	This output line is always driven to a high state in memory mode since a battery is not required for this product. This output line is always driven to a high state in I/O mode since this product does not support the audio function. In the True IDE mode, this input/output is the disk active/slave present signal in the Master/Slave handshake protocol.

Table 4. Signal Description for Flash Memory Interface

Signal Name	100-Pin Number	I/O	Description
FD0 FD1 FD2 FD3 FD4 FD5 FD6 FD7	55 56 57 58 59 60 61 62	I/O	FLASH DATA BUS[15:0]: These lines are 16-bit data lines to/from the flash memory chip.
FRDY0 FRDY1	45 46	I I/O	FLASH READY: The signal is used for indicate to the controller, which flash memory is ready to accept a command.
FALE	50	O	FLASH ADDRESS LATCH ENABLE: When this signal is asserted the controller can send an address to the flash memory by asserting of FWE pin.
FCLE	49	O	FLASH COMMAND LATCH ENABLE: When this signal is asserted, a command can be to the flash memory.
FRE	51	O	FLASH READ ENABLE: This signal is asserted to enable the reading of data from the flash memory.
FWE	52	O	FLASH WRITE ENABLE: When this signal is asserted , the controller can write data to the flash memory.

Table 4. Signal Description for Flash Memory Interface (Continued)

Signal Name	100-Pin Number	I/O	Description
FCE0	44	O	FLASH CHIP ENABLE: These lines are flash memory enable signal.
FCE1	43	O	
FCE2	42	I/O	
FCE3	41	I/O	
FCE4	40	I/O	
FCE5	39	I/O	
FCE6	38	I/O	
FCE7	37	I/O	
FCE8	36	I/O	
FCE9	35	I/O	
FWP	53	O	PROTECTION OF WRITING FLASH MEMORY: Write protect of flash chips

Table 5. Signal Description for Miscellaneous Part

Signal Name	100-Pin Number	I/O	Description
TCK	17	I	TEST CLOCK: The S3F49FAX contains internally in-circuit emulation block for debugger mode which use standard JTAG protocol. When the controller go into debugger mode, this signal is provided from external debugger tool.
TMS	16	I	TEST MODE SELECT: In the debugger mode, this signal select test mode. This pin should be held to “1’, when do not use the JTAG block.
TDI	15	I	TEST DATA INPUT: In the debugger mode, this signal is used for carry data. from external debugger tool to the controller.
TRST	14	I	TEST RESET: This signal should be sustained LOW first at the begging of normal operation.
TDO	20	O	TEST DATA OUTPUT: In the debugger mode, this signal is used for carry data. from the controller to external debugger tool.
XI	21	–	INPUT CLOCK: This signal is system clock.
XO	22	–	OUTPUT CLOCK: This signal is system output clock.
TEST0 TEST1 TEST2	31 32 33	I	SELECT TEST MODE: Select the test mode of chip
RSOUT	25	I/O	Output Internal Reset Signal
CKOUT	24	I/O	Output the PLL clock signal for checking PLL operation
HWP	23	I	Protect writing/erasing operation

Table 5. Signal Description for Miscellaneous Part (Continued)

Signal Name	100-Pin Number	I/O	Description
VCON	30	I	Define reference voltage for VCO
MODE_SET	29	I	Select Controller Clock mode, INPUT (high): VCO mode INPUT (low): PLL mode
GPIO[0:9]	42 41 40 39 38 37 36 35 25 24	I/O	General Purpose Input/Output Port If you use GPIO, you should set SFR(PortFun, PortDir, PortDat)
PLLCAP	27	–	PLL Capacitor

Table 6. Signal Description for Power Signal

Signal Name	100-Pin Number	I/O	Description
VDD	13 19 34 48 54 64	–	System power supply voltage
PVDD1 PVDD2	77 94	–	PCMCIA power supply voltage
GND	10 18 47 63 75	–	Ground
VDDA	26	–	Analog power supply voltage for PLL
VSSA	28	–	Analog ground for PLL

Table 7. Signal Description for USB Device

Signal Name	100-Pin Number	I/O	Description
DP	11	I/O	Positive data
DN	12	I/O	Negative data

Table 8. Signal Description for Internal NOR Flash Memory

Signal Name	100-Pin Number	I/O	Description
SDATA	46	I/O	Serial data for internal flash
SCLK	45	I	Serial clock for internal flash

3 ELECTRICAL DATA

3.1 DC CHARACTERISTICS

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Ratings		Unit
V_{DD}	DC Supply voltage	– 0.3 to 4.0		V
V_{IN}	DC Input voltage	3.3V I/O	–0.3 to 3.6	V
		5.0V I/O	–0.5 to 5.5	
I_{IN}	DC input current	±10		mA
T_{STG}	Storage temperature	–40 to 125		°C

Table 10. Recommended Operating Conditions

Symbol	Parameter	Ratings	Unit
V_{DD}	DC supply voltage	3.0 to 3.6	V
T_A	Temperature range	–25 to 85	°C

Table 11. Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{ja}	Thermal Impedance of Samsung 100TQFP Package	37-70	°C/W

Table 12. D.C. Electrical Characteristics (In case of 3.3V Interface I/O)

(V_{DD} = 3.3 ± 0.3V, T_A = -25 to 85 °C)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	LVCMOS Interface		2.0			V
V_{IL}	Low level input voltage	LVCMOS Interface				0.8	V
V_T	Switching threshold		LVCMOS		1.4		V
V_{T+}	Switching trigger, positive-going threshold		LVCMOS			2.0	V
V_{T-}	Switching trigger, negative-going threshold		LVCMOS	0.8			V
I_{IH}	High level input current	Input buffer	$V_{IN} = V_{DD}$	–10		10	µA
		Input buffer with pull-down		10	30	60	
I_{IL}	Low level input current	Input buffer	$V_{IN} = V_{SS}$	–10		10	µA
		Input buffer with pull-up		–60	–30	–10	
V_{OH}	High level output voltage	Type B4, B8	I_{OH} = –1 mA	VDD– 0.05			V
		Type B4	I_{OH} = –4 mA	2.4			
		Type B8	I_{OH} = –8 mA				
V_{OL}	Low level output voltage	Type B4, B8	I_{OL} = 1 mA			0.05	V
		Type B4	I_{OL} = 4 mA			0.4	
		Type B8	I_{OL} = 8 mA				
I_{OZ}	Tri-state output leakage current		V_{OUT} = V_{SS} or V_{DD}	–10		10	µA
I_{DD}	Maximum operating current		V_{DD} = 3.3 V, VCON = 2.2 V		45	80	mA
I_{DS}	Stop current				100	150	µA

Table 13. D.C. Electrical Characteristics (In Case of 5V Interface I/O)

(V_{DD} = 5.0 ± 0.5V, T_A = -25 to 85 °C)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	CMOS		3.5			V
		TTL		2.0			
V_{IL}	Low level input voltage	CMOS				1.5	V
		TTL				0.8	
V_T	Switching threshold	CMOS			2.45		V
		TTL			1.45		
V_{T+}	Switching trigger, positive-going threshold	CMOS			3.0	3.5	V
		TTL			1.8	2.0	
V_{T-}	Switching trigger, negative-going threshold	CMOS		1.5	2.0		V
		TTL		0.8	1.1		
I_{IH}	High level input current	Input buffer	$V_{IN} = V_{DD}$	–10		10	µA
		Input buffer with pull-up		10	100	200	
I_{IL}	Low level input current	Input buffer	$V_{IN} = V_{SS}$	–10		10	µA
		Input buffer with pull-up		–200	–100	–10	
V_{OH}	High level output voltage	Type B4	I_{OH} = –4 mA	VDD–0.8			V
		Type B8	I_{OH} = –8 mA				
V_{OL}	Low level output voltage	Type B4	I_{OL} = 4 mA			0.4	V
		Type B8	I_{OL} = 8 mA				
I_{OZ}	Tri-state output leakage current		V_{OUT} = V_{SS} or V_{DD}	–10		10	µA
I_{DD}	Maximum operating current		V_{DD} = 5.0 V, VCON = 2.2 V		55	80	mA
I_{DS}	Stop current				200	250	µA

3.2 AC CHARACTERISTICS

Table 14. System Clock Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_C	Clock cycle time	40	55	75	ns
T_{lpd}	Clock low pulse duration	0.4Tc		0.6Tc	ns
T_{hpd}	Clock high pulse duration	0.4Tc		0.6Tc	ns

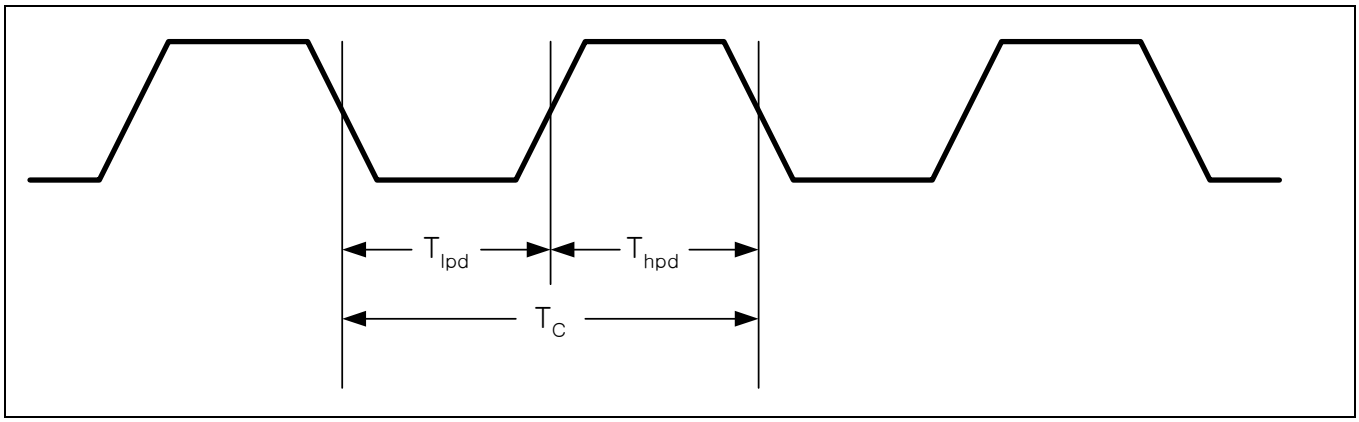

Table 15. POR(Power On Reset) Detection Level

Symbol	Parameter	Min	Typ	Max	Unit
P_D	POR Detection Level	1.3	2.1	2.65	V

4 MECHANICAL DATA

The S3F49FAX disk controller is available in a 100-pin TQFP package (Samsung part number 100-TQFP-1414).

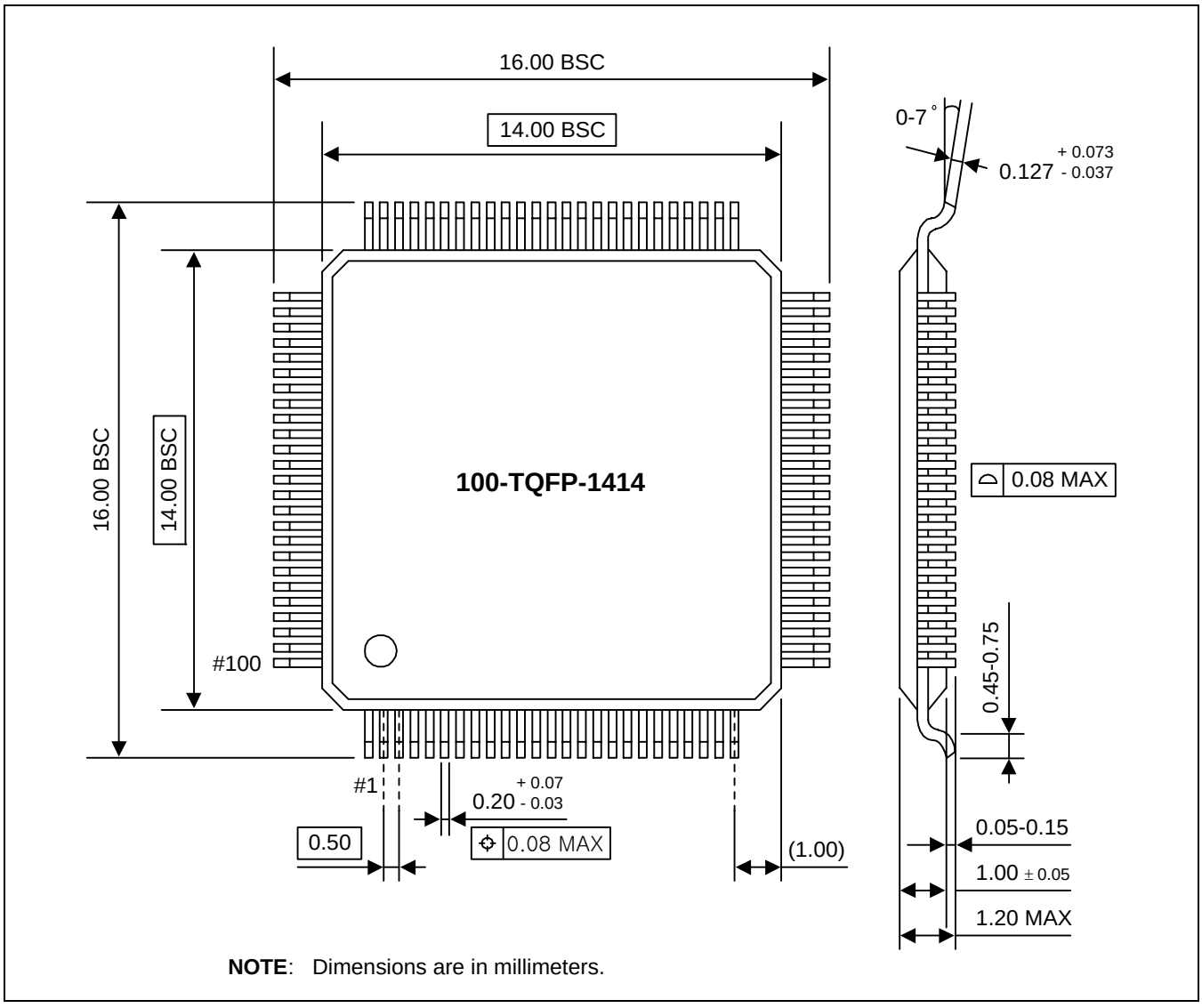

Figure 3. 100-TQFP-1414 Package Dimension