1 PRODUCT OVERVIEW

OVERVIEW

The S3C72C8 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With an up-to-96-dot LCD direct drive capability flexible 16-bit timer/counter, and 4-chanel comparator, the S3C72C8 offers an excellent design solution for a low CDP and a card reader.

Up to 28 pins of the 44-pin QFP or up to 26 pins of the 42-pin SDIP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the S3C72C8's advanced CMOS technology provides for low power consumption.

OTP

The S3C72C8 microcontroller is also available in OTP (One Time Programmable) version, S3P72C8. S3P72C8 microcontroller has an on-chip 8K-byte one-time-programable EPROM instead of masked ROM.
The S3P72C8 is comparable to S3C72C8, both in function and in pin configuration.

FEATURES

Memory

- 512 × 4-bit RAM (including LCD display RAM)
- 8,192 × 8-bit ROM

28 I/O Pins

- I/O: 26 pins (44-pin QFP, 42-pin SDIP)
- Output only: 2 pins (44-pin QFP)

LCD Controller/Driver

- 12 segments and 8 common terminals (3, 4, and 8 common selectable)
- Internal resistor circuit for LCD bias
- All dot can be switched on/off

8-bit Basic Timer

- 4 interval timer functions
- Watch-dog timer

16-bit Timer/Counter 1

- Programmable 16-bit timer/counter
- Arbitrary clock output
- External event counter
- External clock signal divider
- Configurable as two 8-bit timer/counters
- Serial I/O interface clock generator

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 32768 Hz
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Comparator

- 4 channel mode: internal reference (4-bit resolution)
- 3 channel mode: external reference

Interrupts

- Four internal vectored interrupts
- Five external vectored interrupts
- Two quasi-interrupts

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure

- Data memory bank 15

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system oscillation stops)
- Sub system clock stop mode

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 0.4 MHz-6 MHz
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.67, 1.33, 10.7 µs at 6 MHz (main)
- 0.95, 1.91, 15.3 µs at 4.19 MHz (main)
- 122 µs at 32.768 kHz (subsystem)

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Type

- 44-pin QFP, 42-pin SDIP

BLOCK DIAGRAM

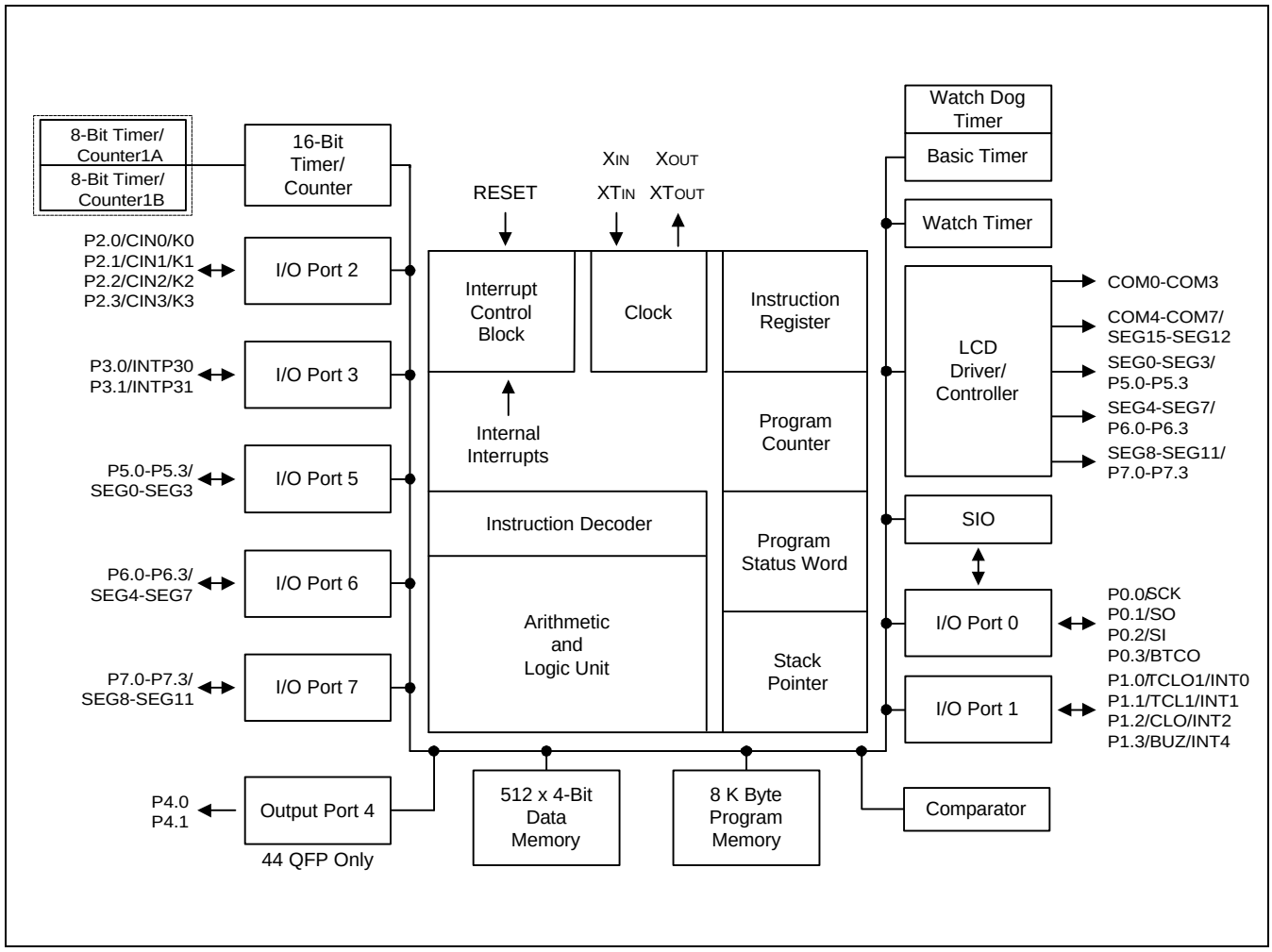


Figure 1-1. S3C72C8 Simplified Block Diagram

PIN ASSIGNMENTS

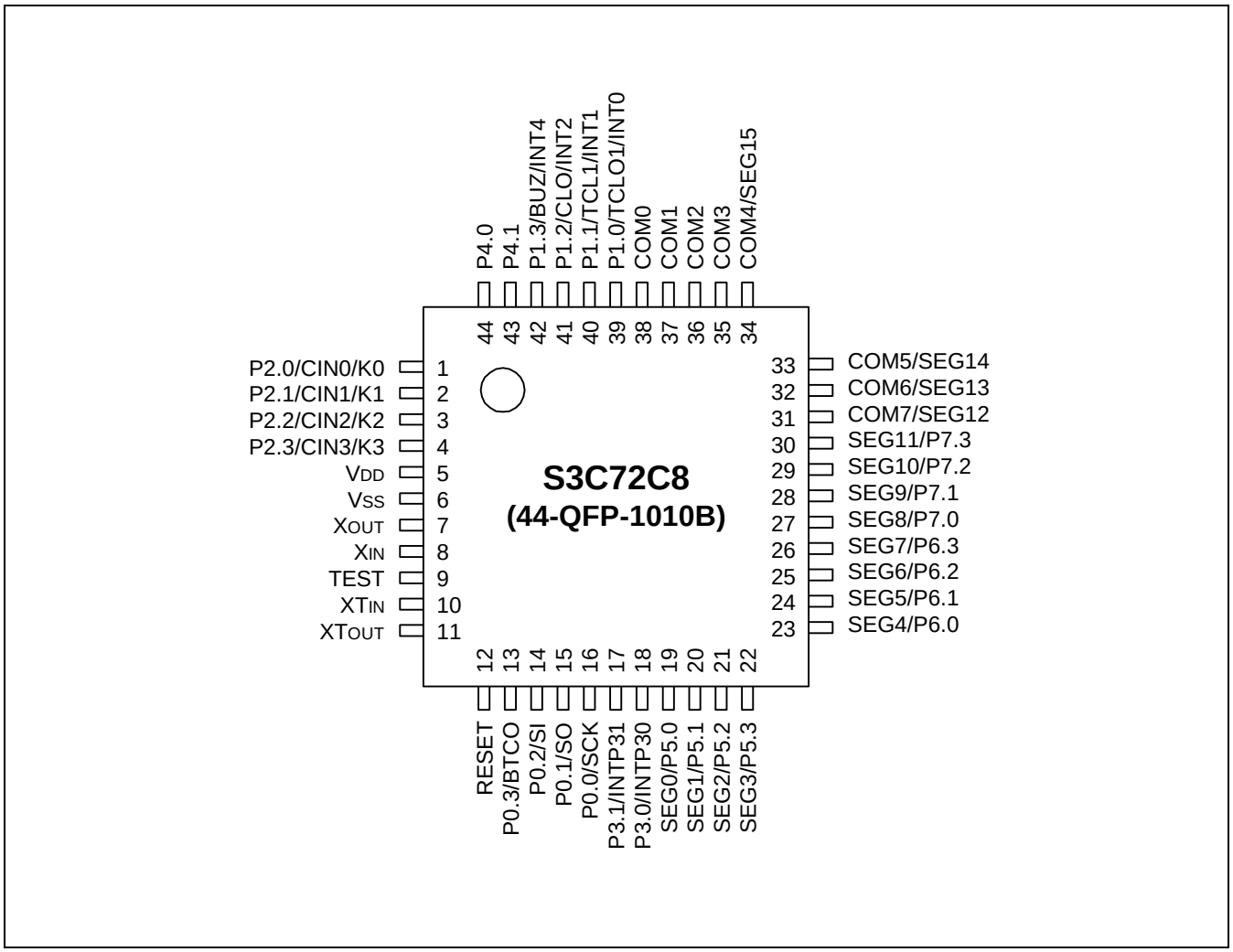


Figure 1-2. S3C72C8 44-QFP Pin Assignment Diagram

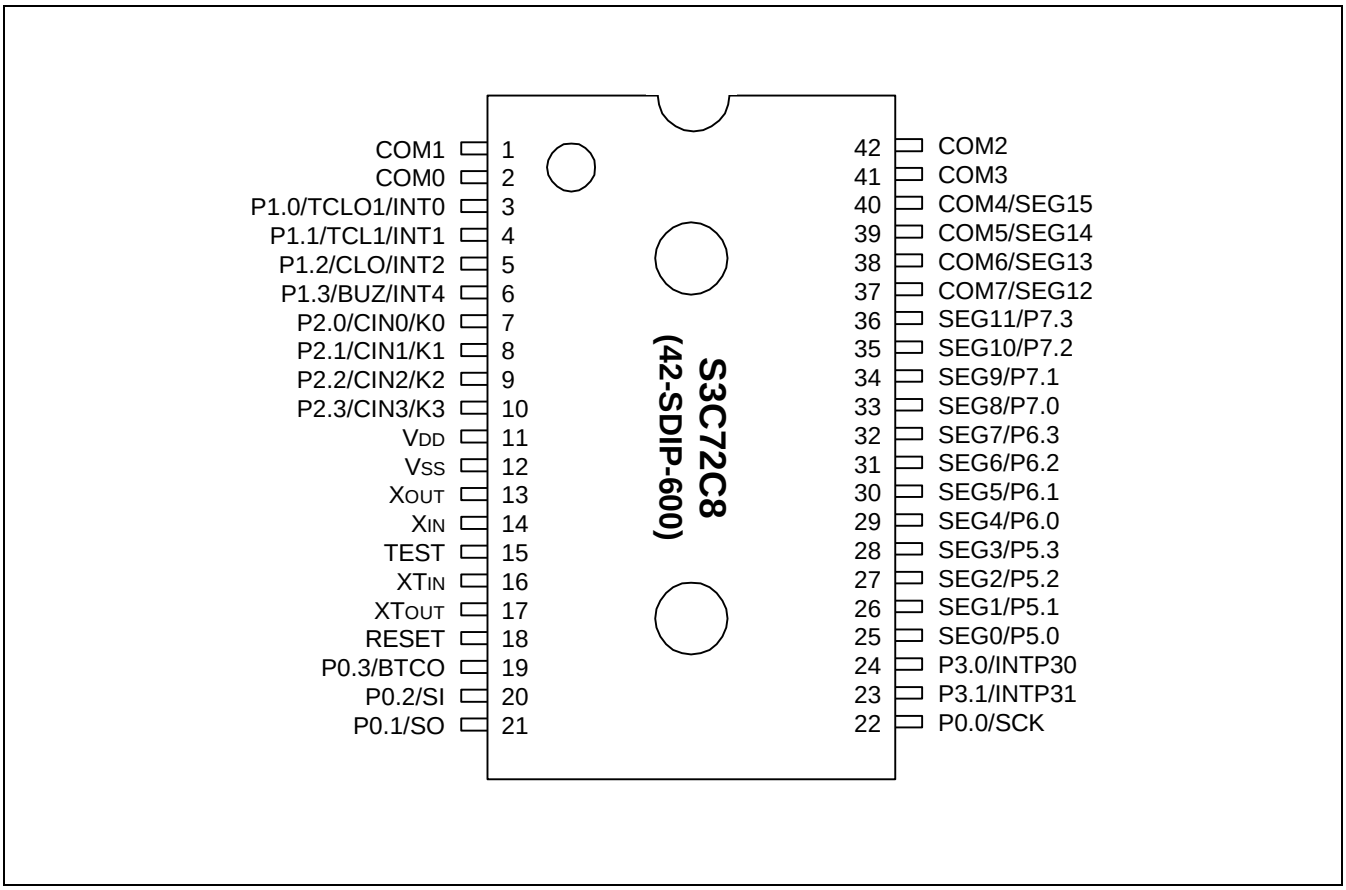


Figure 1-3. S3C72C8 42-SDIP Pin Assignment Diagram

Table 1-1. S3C72C8 Pin Descriptions

Pin Name	Pin Type	Description	Circuit Type	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test are possible. Individual pins are software configurable as input or output; Individual pins are software configurable as open-drain or push-pull output; Individual pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	E–1	16 (22) 15 (21) 14 (20) 13 (19)	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I/O	Same as port 0.	E–1	39 (3) 40 (4) 41 (5) 42 (6)	TCLO1/INT0 TCL1/INT1 CLO/INT2 BUZ/INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0 except that port 2 is not configurable as n-channel open drain and is configurable as analog input pin.	F–8	1 (7) 2 (8) 3 (9) 4 (10)	K0/CIN0 K1/CIN1 K2/CIN2 K3/CIN3
P3.0 P3.1	I/O	2-bit I/O port 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output; Individual pins are software configurable as open-drain or push-pull output; 2-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	E–3	18 (24) 17 (23)	INTP30 INTP31
P4.0 P4.1	O	2-bit output port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as open-drain or push-pull output.	E-2	44 43	
P5.0-P5.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output; Individual pins are software configurable as open-drain or push-pull output; 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	H-13	19-22 (25-28)	SEG0-SEG3
P6.0-P6.3	I/O	Same as port5	H-13	23-26 (29-32)	SEG4-SEG7
P7.0-P7.3	I/O	Same as port5	H-13	27-30 (33-36)	SEG8-SEG11

Table 1-1. S3C72C8 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Circuit Type	Number	Share Pin
SEG0-SEG3	I/O	LCD segment display signal output pins	H–13	19-22 (25-28)	P5.0-P5.3
SEG4-SEG7				23-26 (29-32)	P6.0-P6.3
SEG8-SEG11				27-30 (33-36)	P7.0-P7.3
SEG12-SEG15	O	LCD segment display output pins	H–6	31-34 (37-40)	COM7-COM4
COM0-COM3	O	LCD common signal output pins	H–4	38-35 (2-1, 42-41)	–
COM4-COM7	I/O	LCD common signal output pins	H–6	34-31 (40-37)	SEG12–SEG15
SCK	I/O	Serial interface clock signal	E–1	16 (22)	P0.0
SO	I/O	Serial data output	E–1	15 (21)	P0.1
SI	I/O	Serial data input	E–1	14 (20)	P0.2
BTCO	I/O	Basic timer overflow signal	E–1	13 (19)	P0.3
TCLO1	I/O	Timer/counter external clock output	E–1	39 (3)	P1.0/INT0
TCL1	I/O	Timer/counter external clock input	E–1	40 (4)	P1.1/INT1
CLO	I/O	Clock output	E–1	41 (5)	P1.2/INT2
BUZ	I/O	Frequency output to buzzer	E–1	42 (6)	P1.3/INT4
RESET	I	System RESET pin	B	12 (18)	–
X_{in}, X_{out}	–	Clock input and output pins for main system clock	–	8-7 (14-13)	–
XT_{in}, XT_{out}	–	Clock input and output pins for subsystem clock	–	10-11 (16-17)	–
CIN0–CIN3	I	Analog input port for Comparator	F–8	1-4 (7-10)	P2.0/K0 -P2.3/K3
K0–K3	I/O	External interrupts. The triggering edge is selectable.	F–8	1-4 (7-10)	P2.0/CIN0 -P2.3/CIN3
INT0 INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	E–1	39 (3) 40 (4)	P1.0/TCLO1 -P1.1/TCL1

Table 1-1. S3C72C8 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Circuit Type	Number	Share Pin
INT2	I	Quasi-interrupt with detection of rising or falling edges.	E-1	41 (5)	P1.2/CLO
INT4	I	External interrupt with detection of rising or falling edges.	E-1	42 (6)	P1.3/BUZ
INTP30 INTP31	I	Key scan interrupts inputs.	E-3	18-17 (24-23)	P3.0, P3.1
TEST	I	System test pin	–	9 (15)	–
V_{DD}	–	Power supply pin	–	5 (11)	–
V_{SS}	–	Ground pin	–	6 (12)	–

NOTES:

1. Parentheses indicate pin number for 42-SDIP package.
2. Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.

PIN CIRCUIT DIAGRAMS

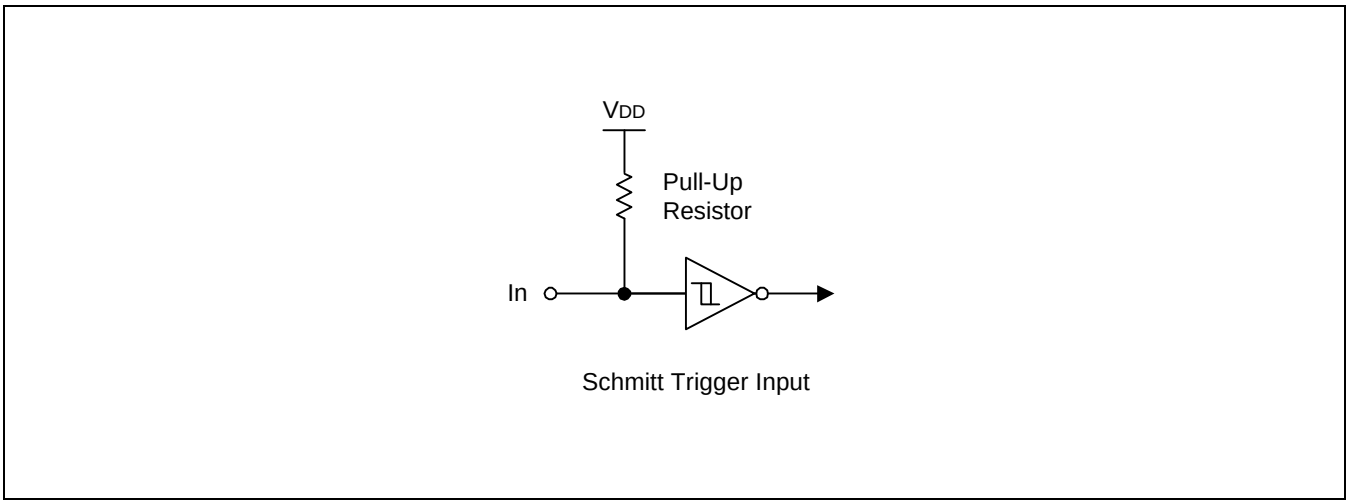


Figure 1-4. Pin Circuit Type B

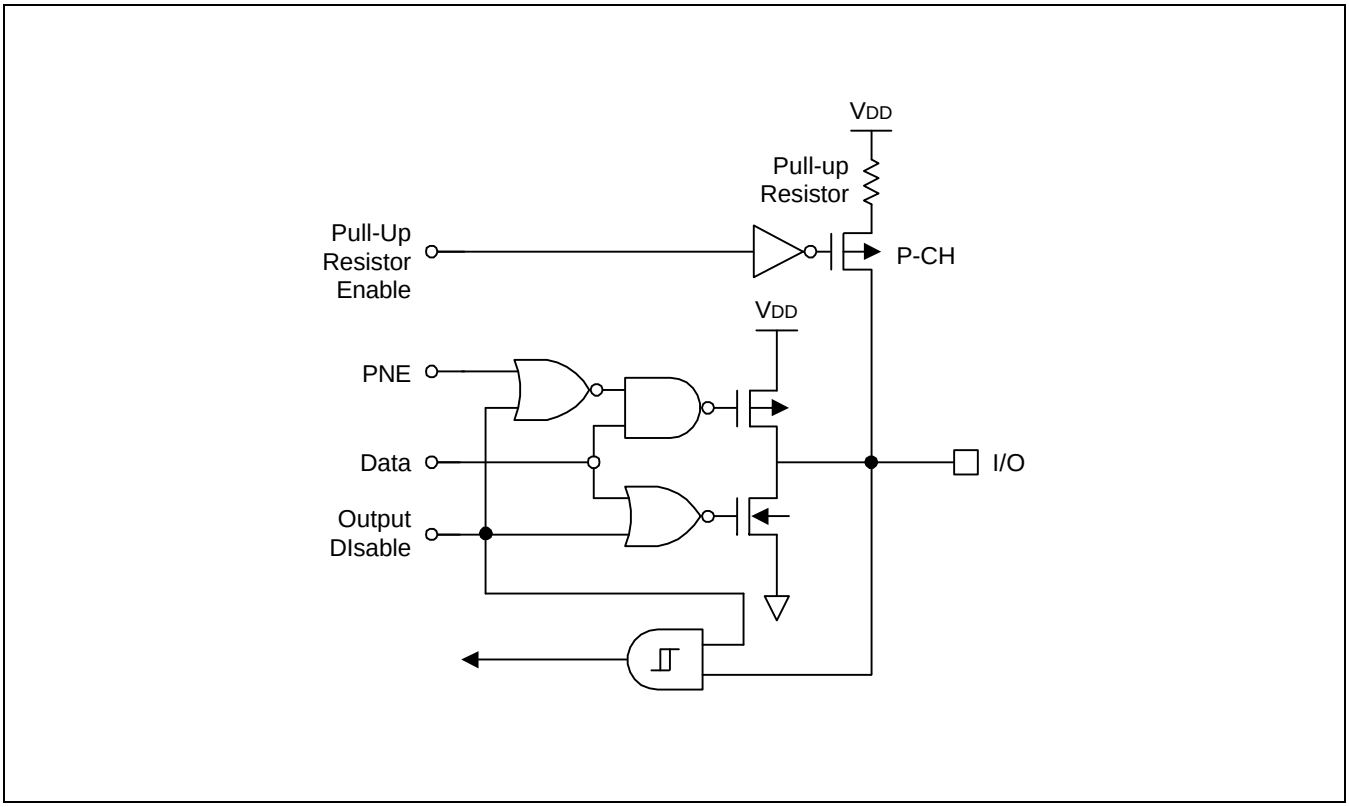


Figure 1-5. Pin Circuit Type E-1

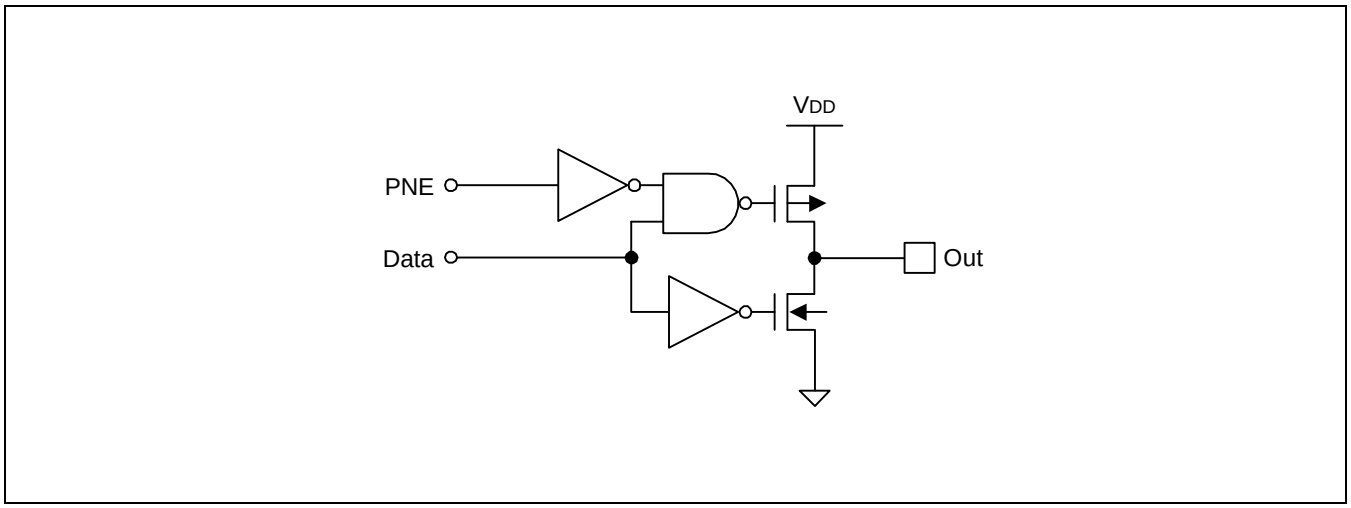


Figure 1-6. Pin Circuit Type E-2

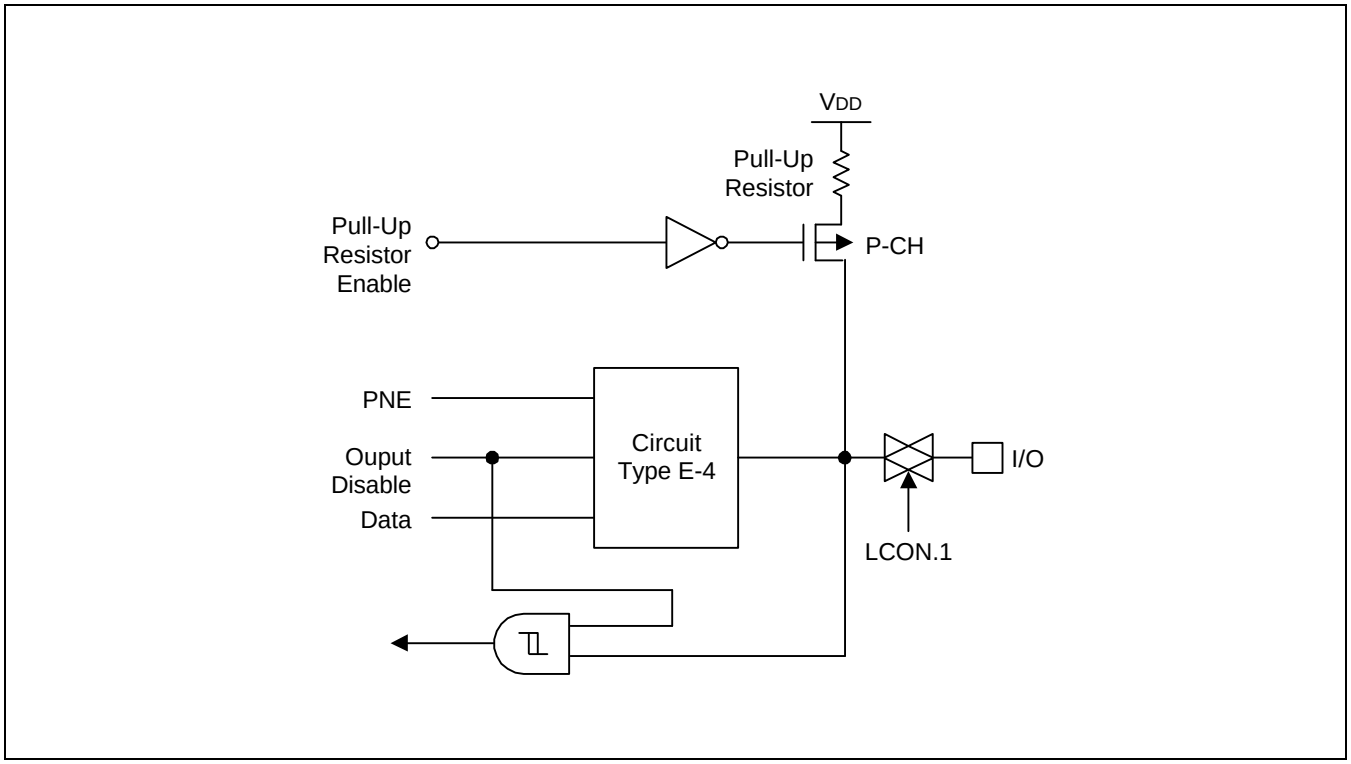


Figure 1-7. Pin Circuit Type E-3

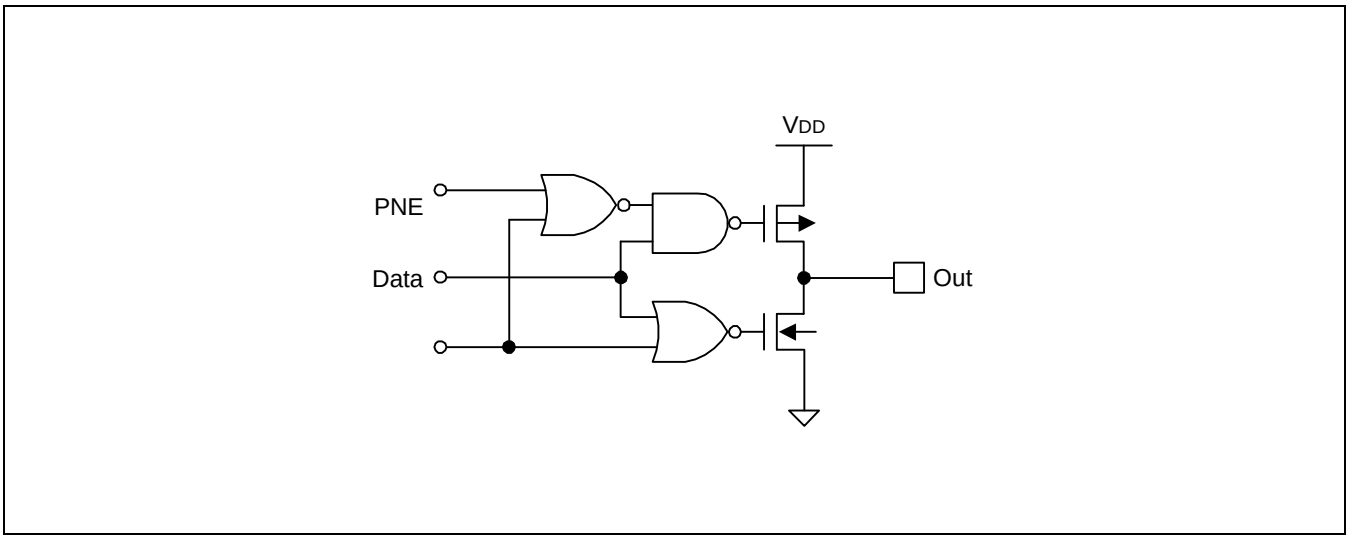


Figure 1-8. Pin Circuit Type E-4

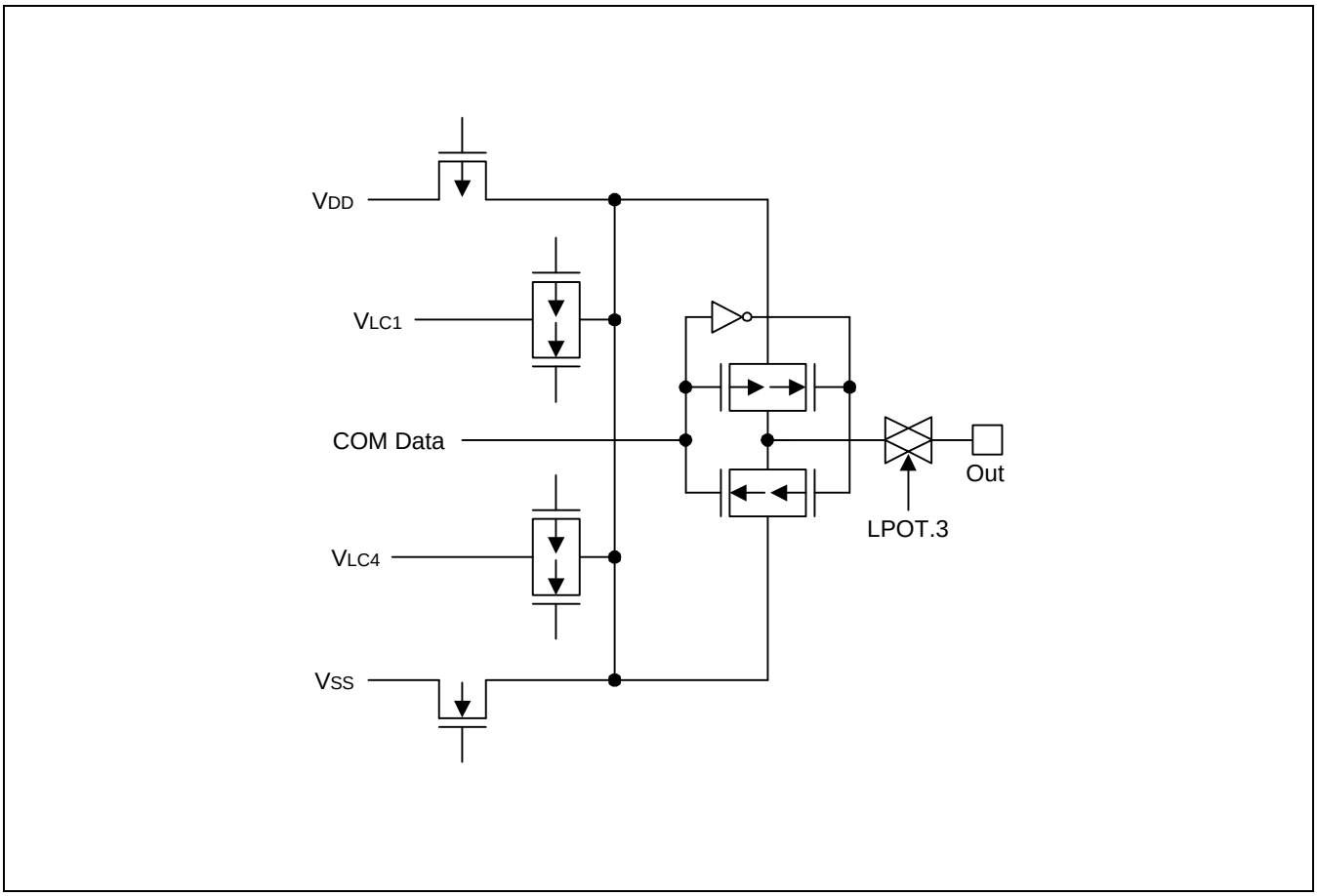


Figure 1-9. Pin Circuit Type H-4

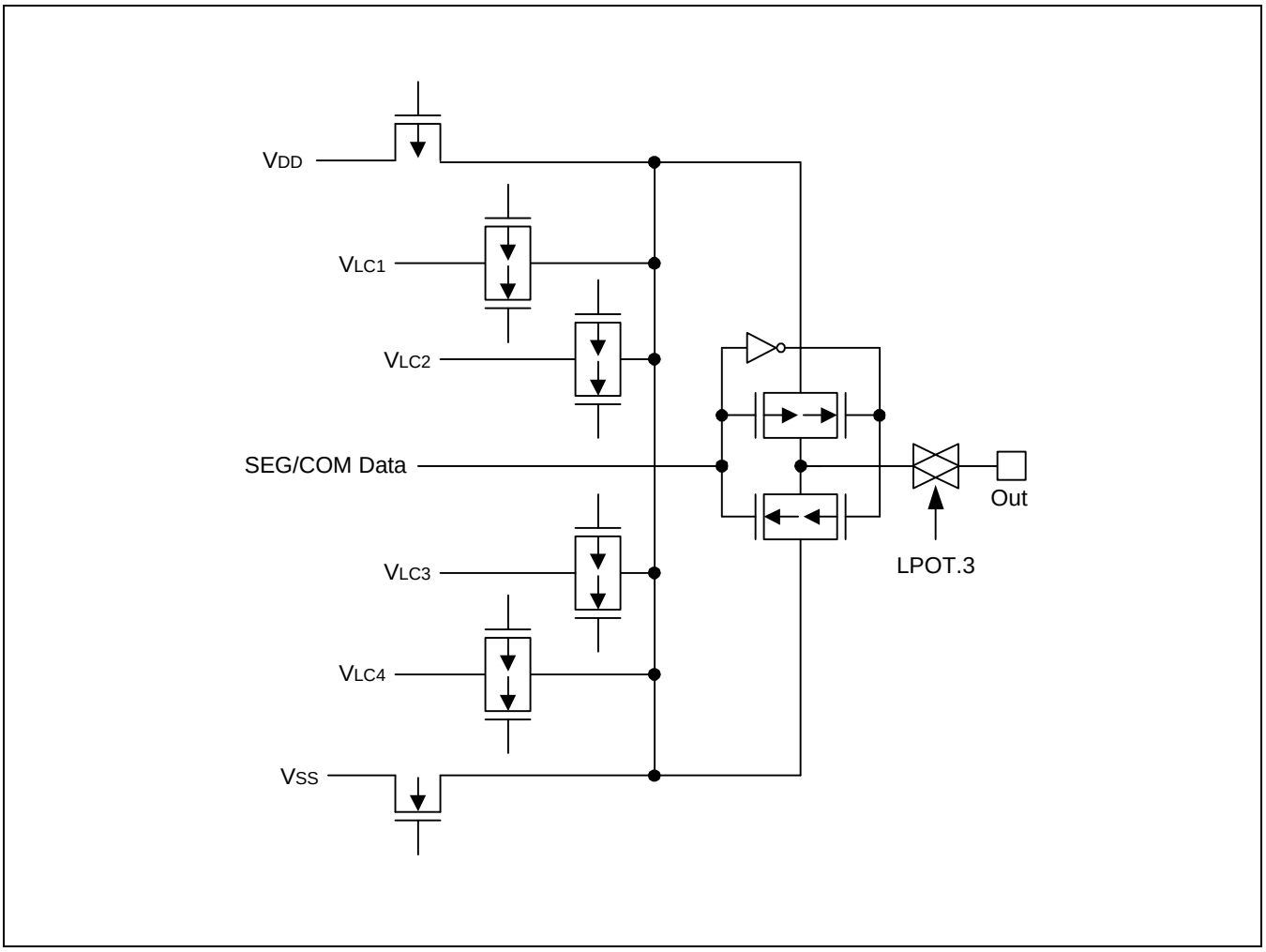


Figure 1-10. Pin Circuit Type H-6

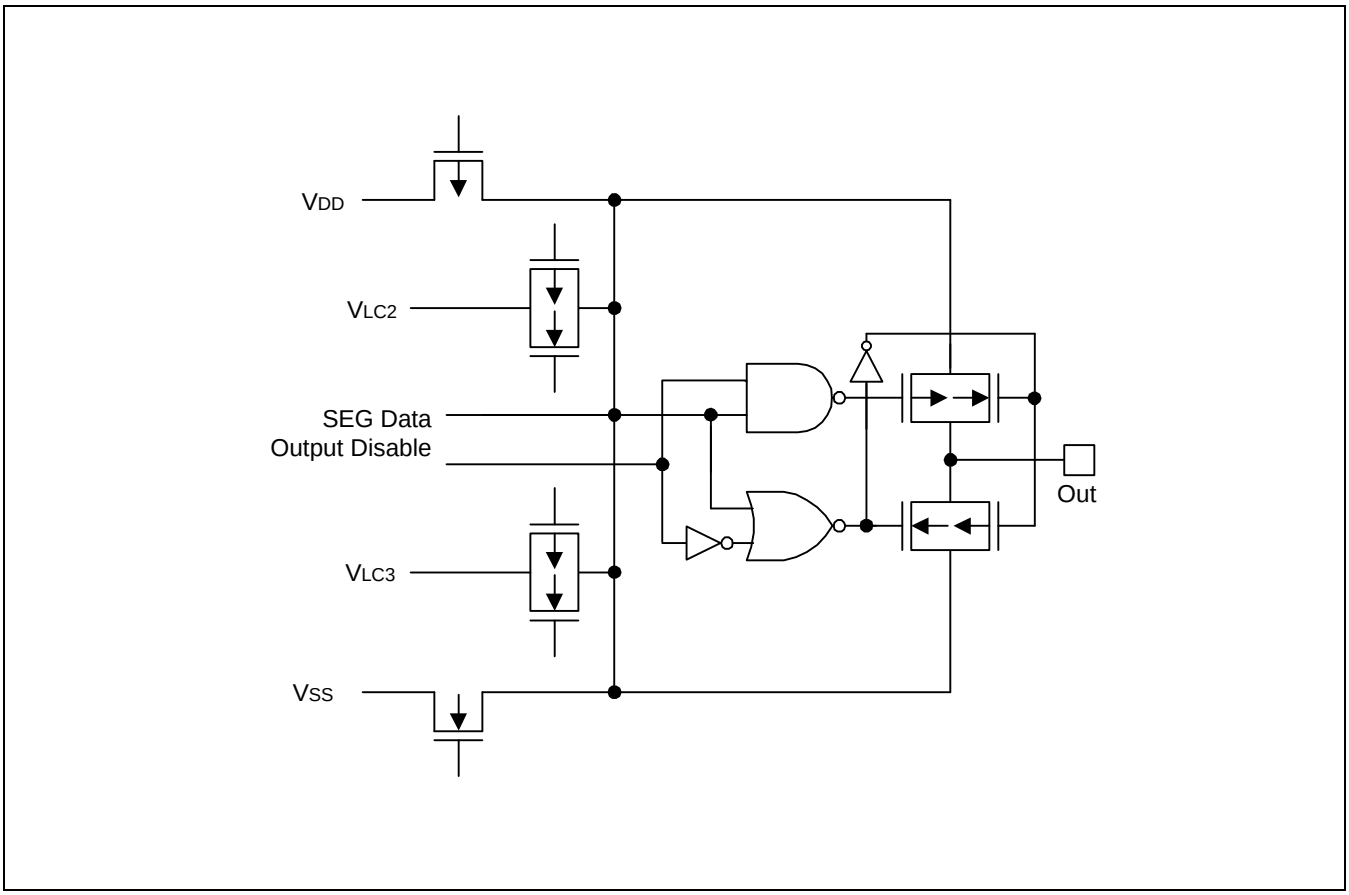


Figure 1-11. Pin Circuit Type H-7

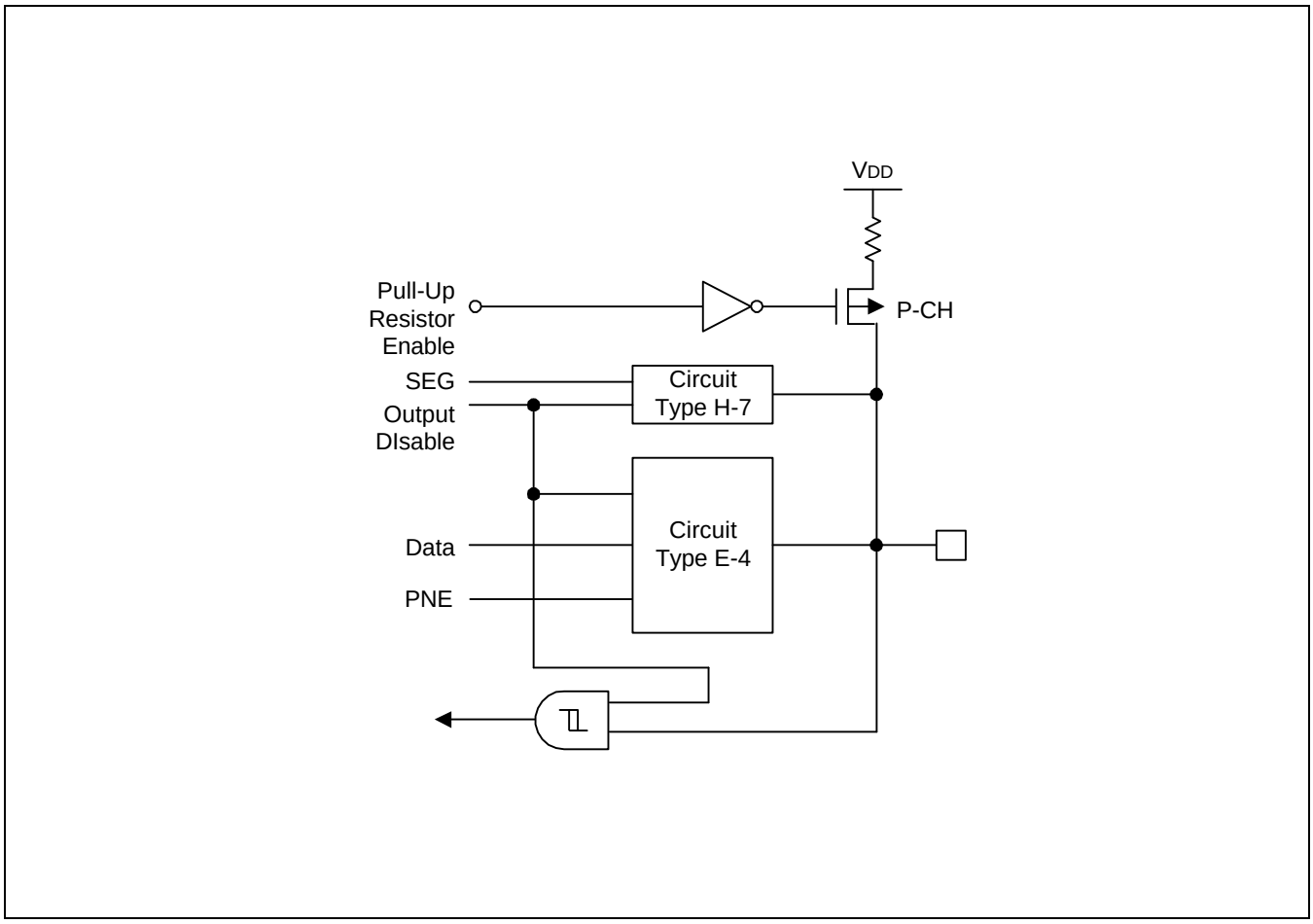


Figure 1-12. Pin Circuit Type H-13

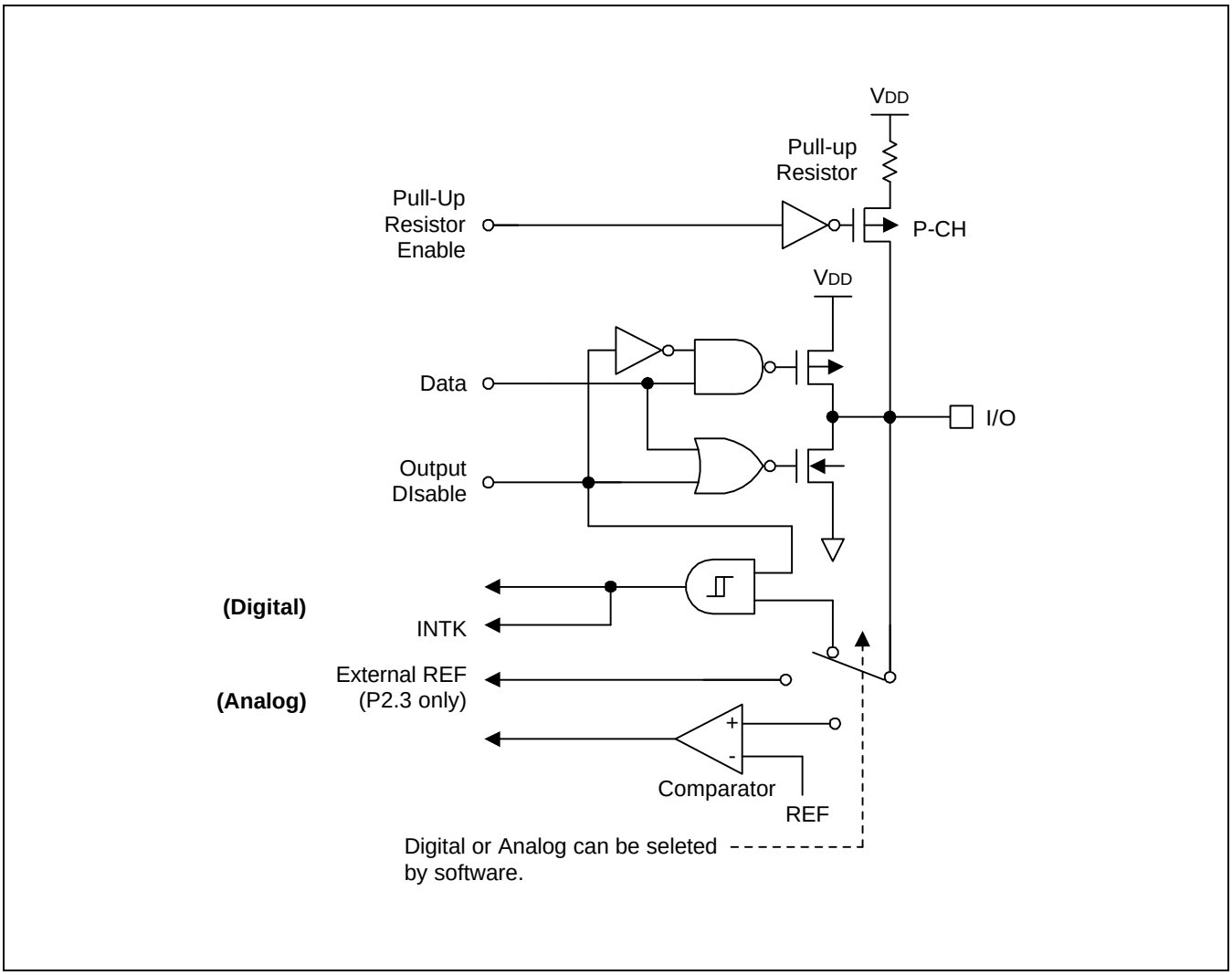


Figure 1-13. Pin Circuit Type F-8

15 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C72C8 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— Main system clock oscillator characteristics
— Subsystem clock oscillator characteristics
— I/O capacitance
— Comparator electrical characteristics
— A.C. electrical characteristics
— Operating voltage range

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Miscellaneous Timing Waveforms

— A.C timing measurement points
— Clock timing measurement at X_{in}
— Clock timing measurement at XT_{in}
— TCL1 timing
— Input timing for RESET signal
— Input timing for external interrupts and quasi-interrupts
— Serial data transfer timing

Table 15-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	All I/O pins active	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 15	mA
		All I/O pins active	– 35	
Output Current Low	I_{OL}	One I/O pin active	+ 30 (Peak value)	mA
			+ 15 *	
		Total for ports 0, 2–9	+ 100 (Peak value)	
			+ 60 *	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

* The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 15-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 0, 1, 2, 3, 5, 6, 7, RESET	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{in}, X_{out}, XT_{in}, and XT_{out}	V_{DD} – 0.1		V_{DD}	
Input Low Voltage	V_{IL1}	Ports 0, 1, 2, 3, 5, 6, 7, RESET	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{in}, X_{out}, XT_{in}, and XT_{out}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA Ports 0, 1, 2, 3, 4, 5, 6, 7	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 0, 1, 2, 3, 4, 5, 6, 7	–	–	2.0	V
		V_{DD} = 1.8 V to 5.5 V I_{OL} = 1.6 mA			0.4	

Table 15-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Leakage Current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	$V_I = V_{DD}$ X_{in}, X_{out}, XT_{in}, and XT_{out}			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except RESET, X_{in}, X_{out}, XT_{in}, and XT_{out}	–	–	– 3	µA
	I_{LIL2}	V_I = 0 V X_{in}, X_{out}, XT_{in}, and XT_{out}			– 20	
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$ All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	µA
Pull-Up Resistor	R_{LI}	V_I = 0 V; V_{DD} = 5 V Ports 0-3, 5-7 expect RESET	25	47	100	kΩ
		V_{DD} = 3 V	50	95	200	
	R_{L2}	V_I = 0 V; V_{DD} = 5 V, RESET	100	220	400	
		V_{DD} = 3 V	200	450	800	
LCD Voltage Dividing Resistor	R_{LCD}	Ta = 25 °C	60	80	100	kΩ
$\|V_{LC1}$-COMi$\|$ Voltage Drop (i = 0–7	V_{DC}	– 15 µA per common pin	–	–	120	mV
$\|V_{LC1}$-SEGx$\|$ Voltage Drop (x = 0–15)	V_{DS}	– 15 µA per segment pin	–	–	120	
V_{LC1} Output Voltage	V_{LC1}	V_{DD} = 1.8 V to 5.5 V, 1/5 bias LCD clock = 0 Hz, $V_{LCD} = V_{DD}$	0.8 V_{DD} – 0.2	0.8 V_{DD}	0.8 V_{DD} + 0.2	V
V_{LC2} Output Voltage	V_{LC2}		0.6 V_{DD} – 0.2	0.6 V_{DD}	0.6 V_{DD} + 0.2	
V_{LC3} Output Voltage	V_{LC3}		0.4 V_{DD} – 0.2	0.4 V_{DD}	0.4 V_{DD} + 0.2	
V_{LC4} Output Voltage	V_{LC4}		0.2 V_{DD} – 0.2	0.2 V_{DD}	0.2 V_{DD} + 0.2	

Table 15-2. D.C. Electrical Characteristics (Concluded)

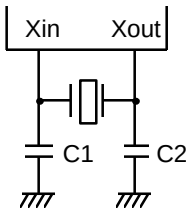
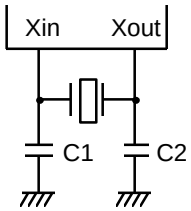
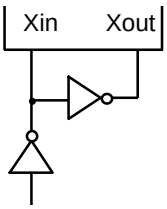
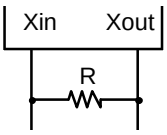
(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1} (2)	V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz	–	3.0 2.3	8.0 5.5	mA
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		1.5 1.0	4.0 3.0	
	I_{DD2} (2)	Idle mode V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz		1.3 1.2	2.5 1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		0.5 0.44	1.5 1.0	
	I_{DD3} (3)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15.0	30	µA
	I_{DD4} (3)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			5.0	15	
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0000B XT_{in} = 0V		2.5	5	
		Stop mode; V_{DD} = 3 V ± 10%			0.5	3	
		V_{DD} = 5 V ± 10%	SCMOD = 0100B		0.2	3	
		V_{DD} = 3 V ± 10%			0.1	2	

NOTES:
1. Currents in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, comparator, output port drive currents.
2. Data includes power consumption for subsystem clock oscillation.
3. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
4. Every values in this table is measured when the power control register (PCON) is set to "0011B".

Table 15-3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range; V_{DD} = 3.0 V.	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	V_{DD} = 2.7 V to 5.5 V	–	–	10	ms
			V_{DD} = 1.8 V to 5.5 V	–	–	30	
External Clock		X_{in} input frequency (1)	–	0.4	–	6.0	MHz
		X_{in} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns
RC Oscillator		Frequency	R = 25 kΩ, V_{DD} = 5 V	–	2	–	MHz
			R = 40 kΩ, V_{DD} = 3 V	–	1	–	

NOTES:
1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 15-4. Recommended Oscillator Constants

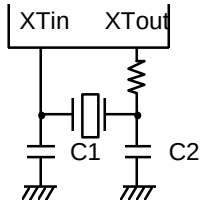
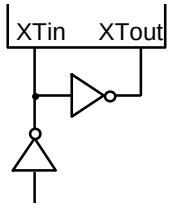
(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Manufacturer	Series Number (1)	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR ðÿM5	3.58 MHz–6.0 MHz	33	33	2.0	5.5	Leaded Type
	FCR ðÿMC5	3.58 MHz–6.0 MHz	(2)	(2)	2.0	5.5	On-chip C Leaded Type
	CCR ðÿMC3	3.58 MHz–6.0 MHz	(3)	(3)	2.0	5.5	On-chip C SMD Type

NOTES:
1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 15-5. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 2.7 V to 5.5 V	–	1.0	2	s
			V_{DD} = 1.8 V to 5.5 V	–	–	10	
External Clock		XT_{in} input frequency (1)	–	32	–	100	kHz
		XT_{in} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µs

NOTES:
1. Oscillation frequency and XT_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

Table 15-6. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 15-7. Comparator Electrical Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 4.0 V to 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range		–	–	0	–	V_{DD}	V
Reference Voltage Range		VREF	–	0	–	V_{DD}	V
Input Voltage Accuracy	Internal	VCIN1	–	–	–	± 150	mV
	External	VCIN2	–	–	–	± 150	mV
Input Leakage Current		ICIN, IREF	–	– 3	–	3	µA

Table 15-8. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (note)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.33		64	
TCL1 Input Frequency	f_{TI1}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			1	
TCL1 Input High, Low Width	t_{TIH1}, t_{TIL1}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V; Input	800	–	–	ns
		Output	650			
		V_{DD} = 1.8 V to 5.5 V; Input	3200			
		Output	3800			
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V; Input	325	–	–	ns
		Output	$t_{KCY}/2 – 50$			
		V_{DD} = 1.8 V to 5.5 V; Input	1600			
		Output	$t_{KCY}/2 – 150$			
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V; Input	100	–	–	ns
		V_{DD} = 2.7 V to 5.5 V; Output	150			
		V_{DD} = 1.8 V to 5.5 V; Input	150			
		V_{DD} = 1.8 V to 5.5 V; Output	500			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V; Input	400	–	–	ns
		V_{DD} = 2.7 V to 5.5 V; Output	400			
		V_{DD} = 1.8 V to 5.5 V; Input	600			
		V_{DD} = 1.8 V to 5.5 V; Output	500			

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.

Table 15-8. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Delay for SCK to SO	t_{KSO}	V_{DD} = 2.7 V to 5.5 V; Input	–	–	300	ns
		V_{DD} = 2.7 V to 5.5 V; Output			250	
		V_{DD} = 1.8 V to 5.5 V; Input			1000	
		V_{DD} = 1.8 V to 5.5 V; Output			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0, INT1, INT2, INT4, K0– K3, INTP30, INTP31	10	–	–	µs
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTE: Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128 / fx as assigned by the IMOD0 register setting.

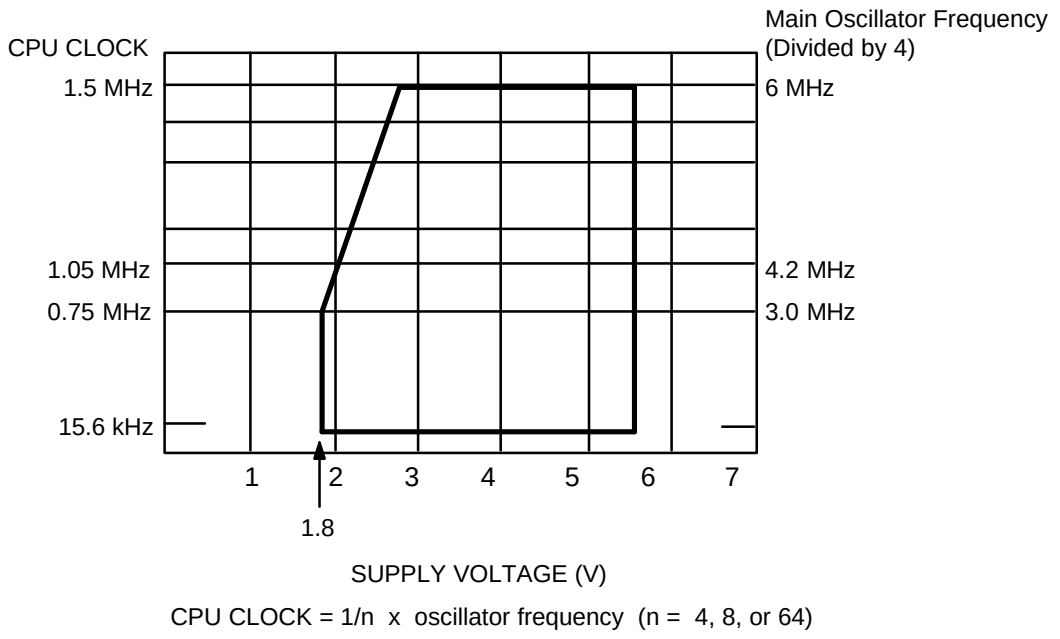


Figure 15-1. Standard Operating Voltage Range

Table 15-9. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17} / fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

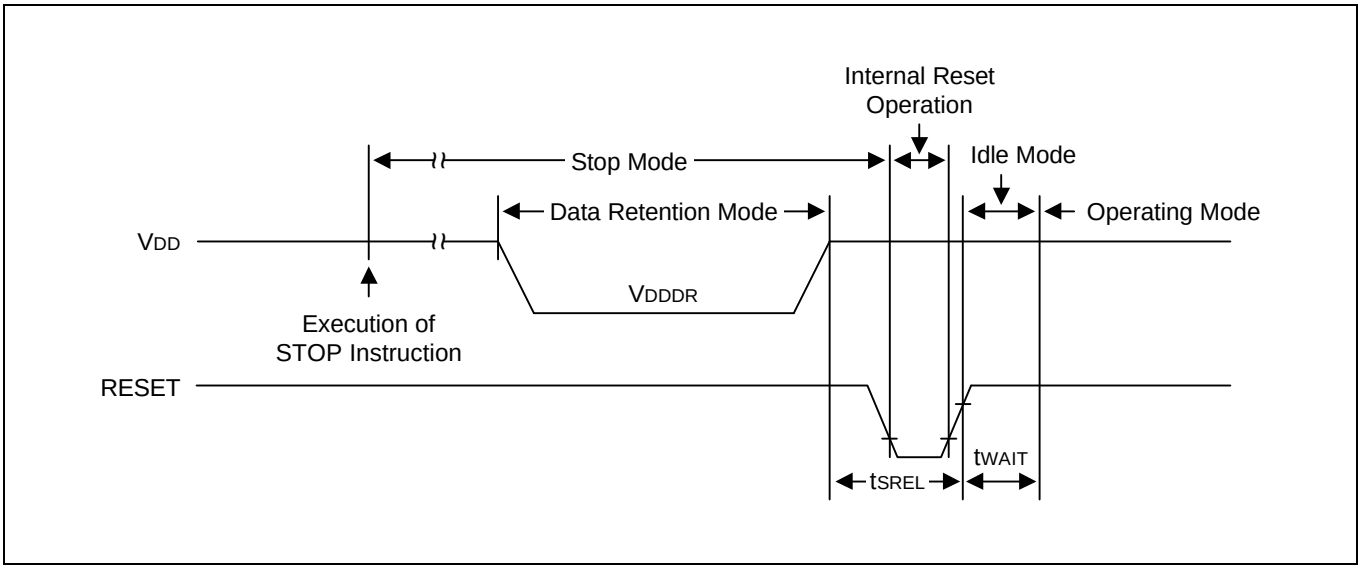


Figure 15-2. Stop Mode Release Timing When Initiated By RESET

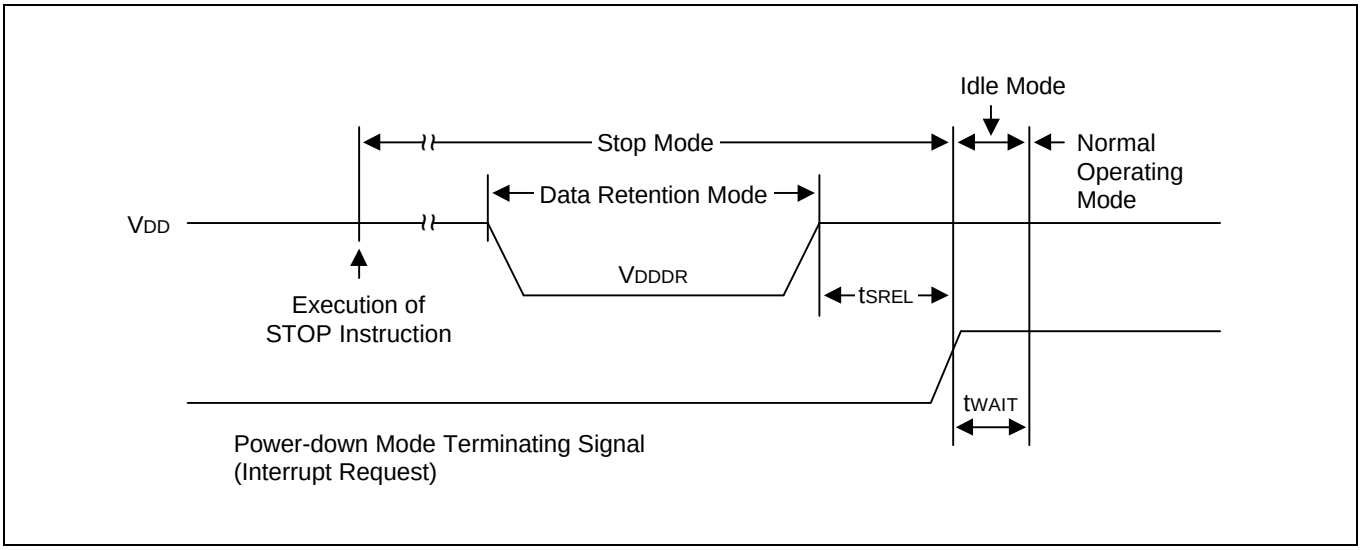


Figure 15-3. Stop Mode Release Timing When Initiated By Interrupt Request

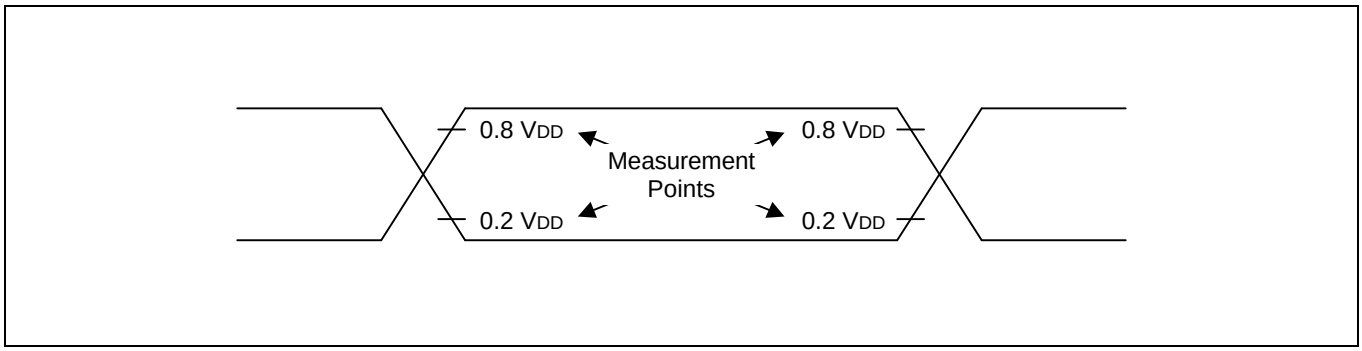


Figure 15-4. A.C. Timing Measurement Points (Except for X_{IN} and XT_{IN})

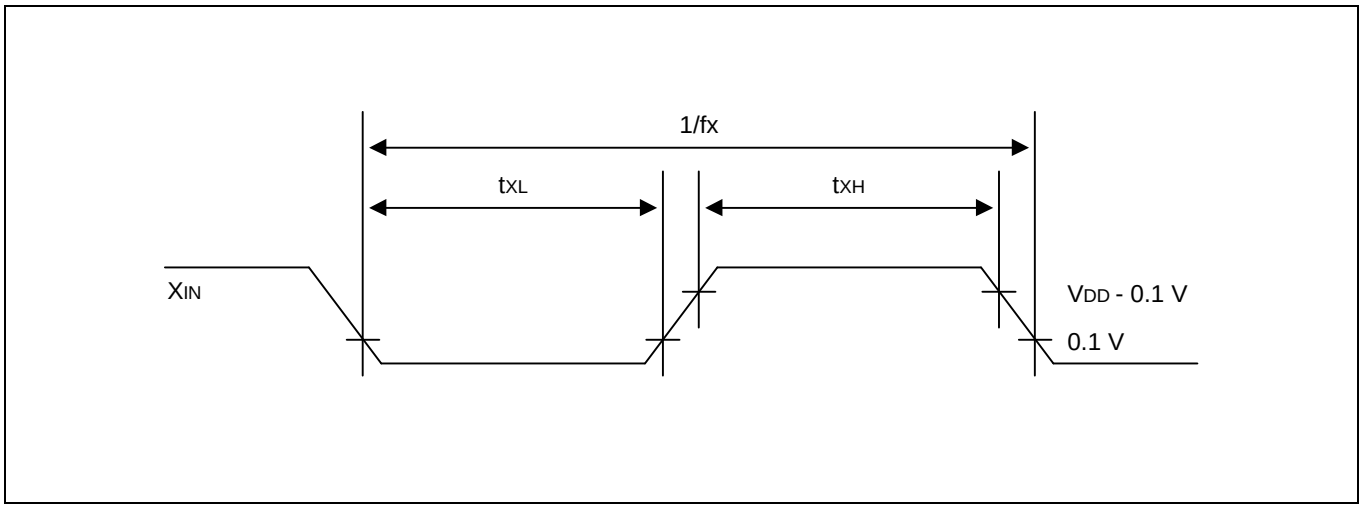


Figure 15-5. Clock Timing Measurement at X_{IN}

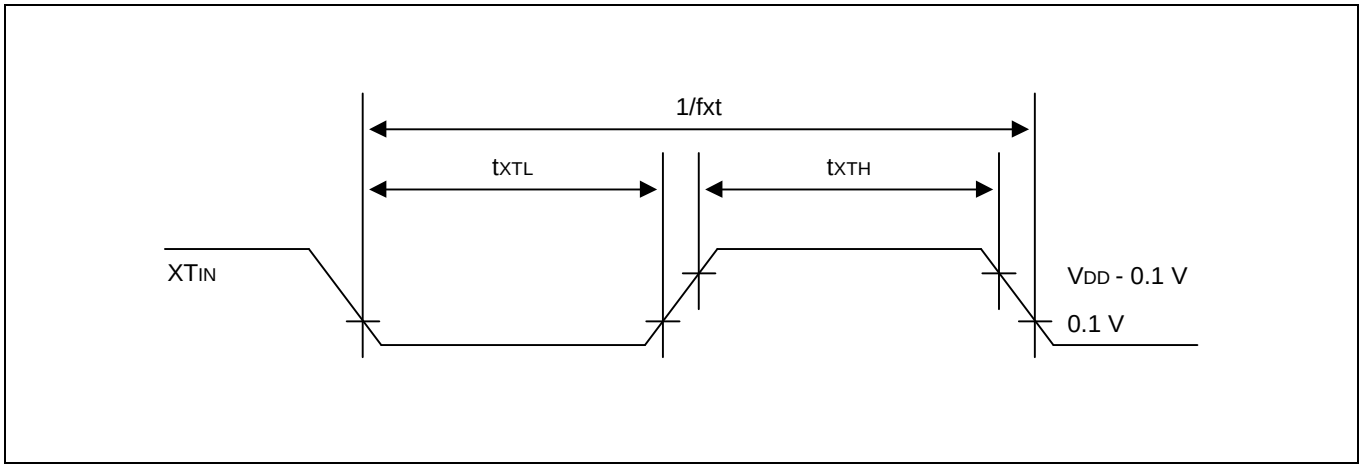


Figure 15-6. Clock Timing Measurement at XT_{IN}

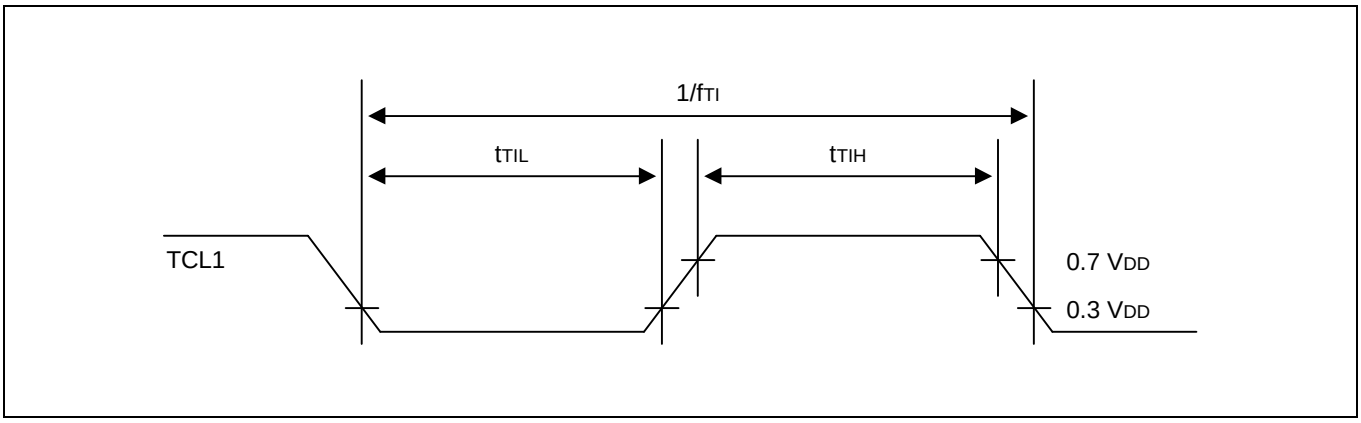


Figure 15-7. TCL1 Timing

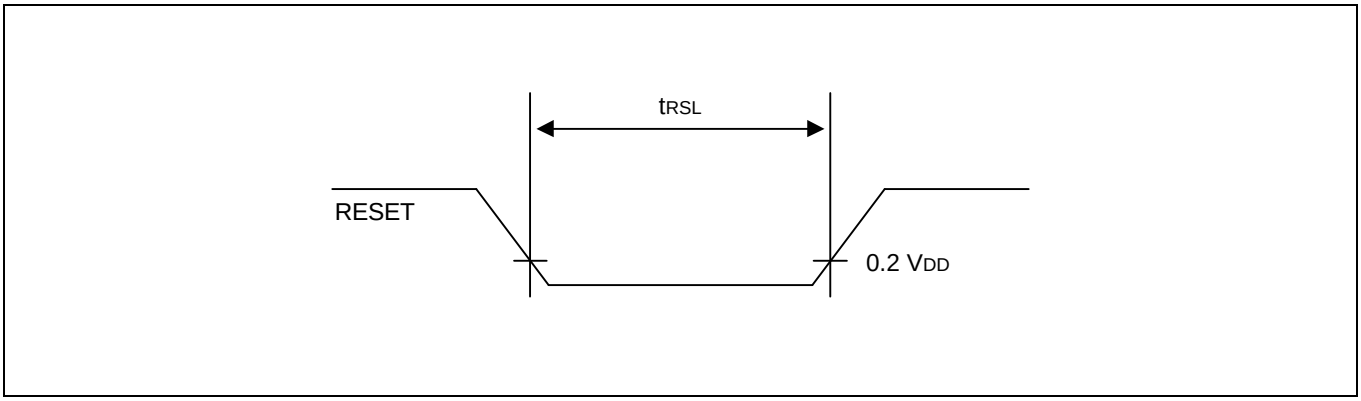


Figure 15-8. Input Timing for RESET Signal

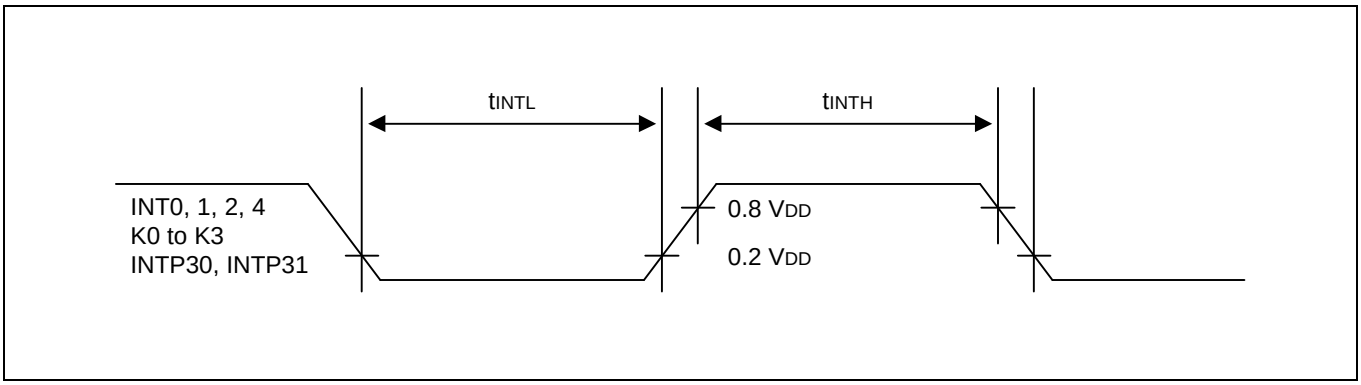


Figure 15-9. Input Timing for External Interrupts and Quasi-Interrupts

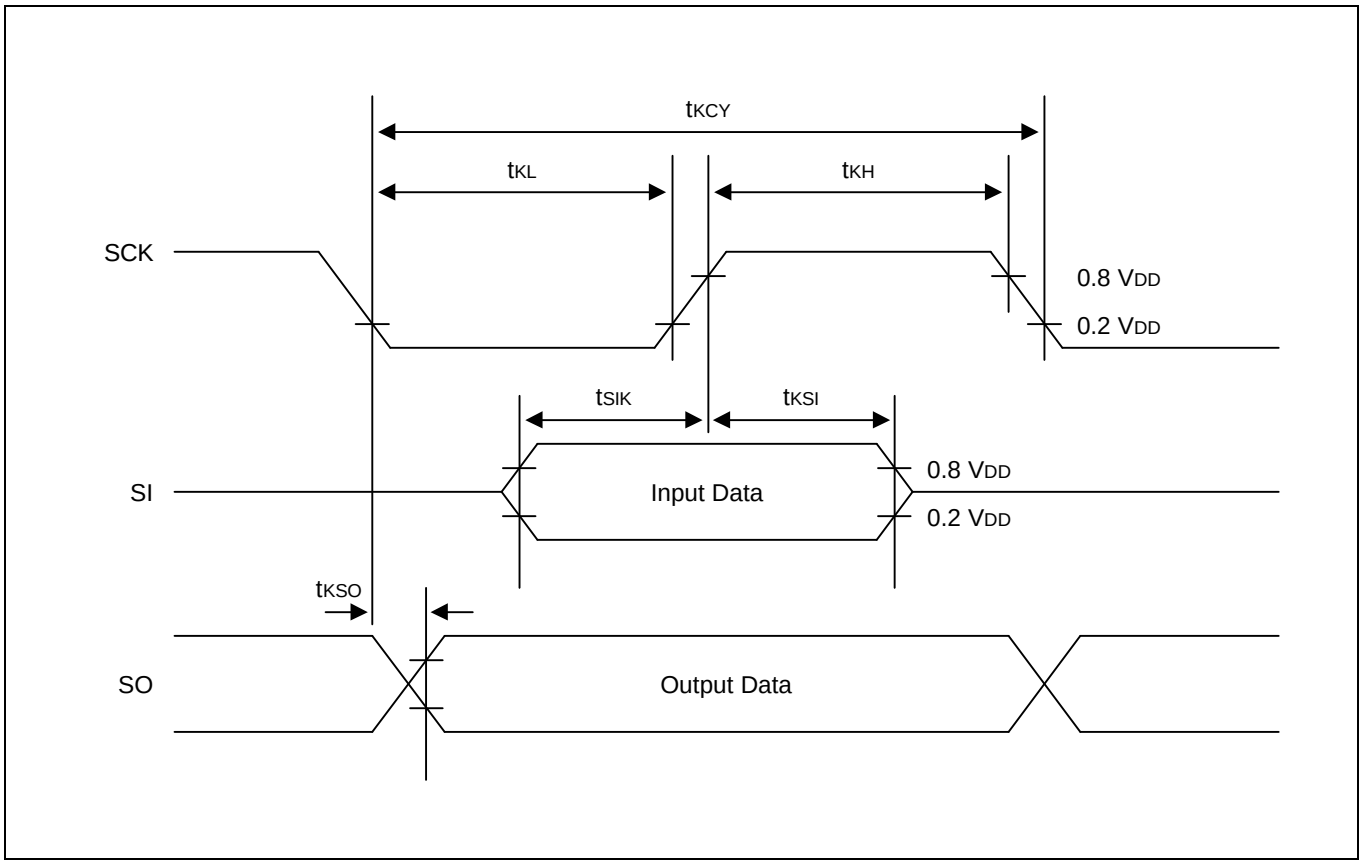


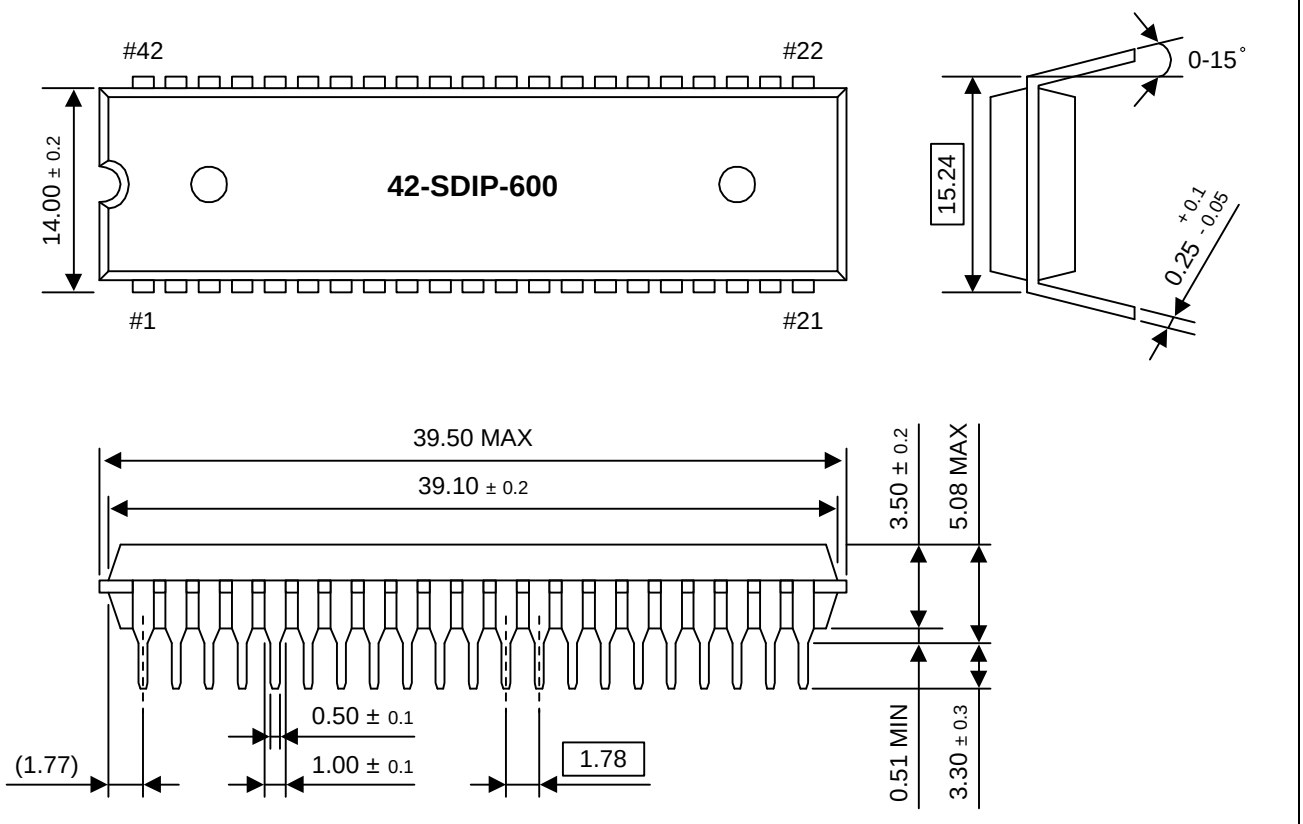
Figure 15-10. Serial Data Transfer Timing

16 MECHANICAL DATA

OVERVIEW

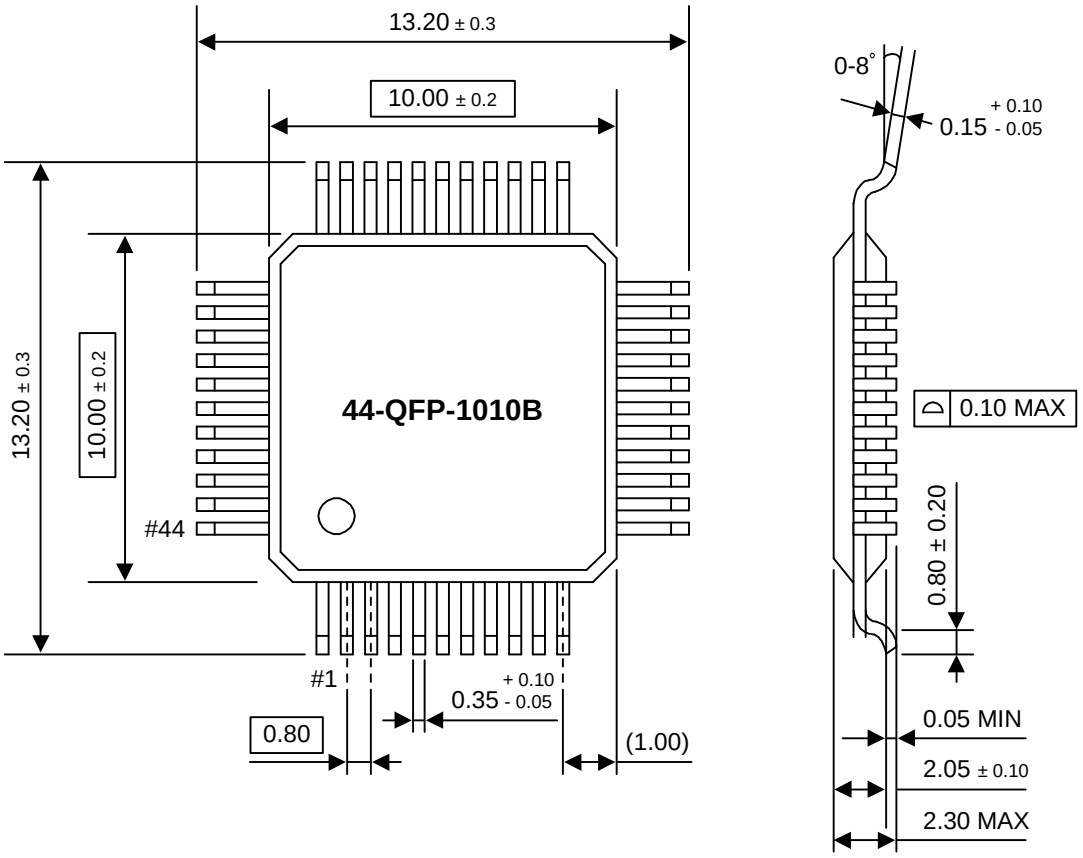
This section contains the following information about the device package:

— Package dimensions in millimeters
— Pad diagram



NOTE: Dimensions are in millimeters.

Figure 16-1. 42-SDIP-600 Package Dimensions



NOTE: Dimensions are in millimeters.

Figure 16-1. 44-QFP-1010B Package Dimensions

17 S3P72C8 OTP

OVERVIEW

The S3P72C8 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C72C8 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P72C8 is fully compatible with the S3C72C8, both in function and in pin configuration. Because of its simple programming requirements, the S3P72C8 is ideal for use as an evaluation chip for the S3C72C8.

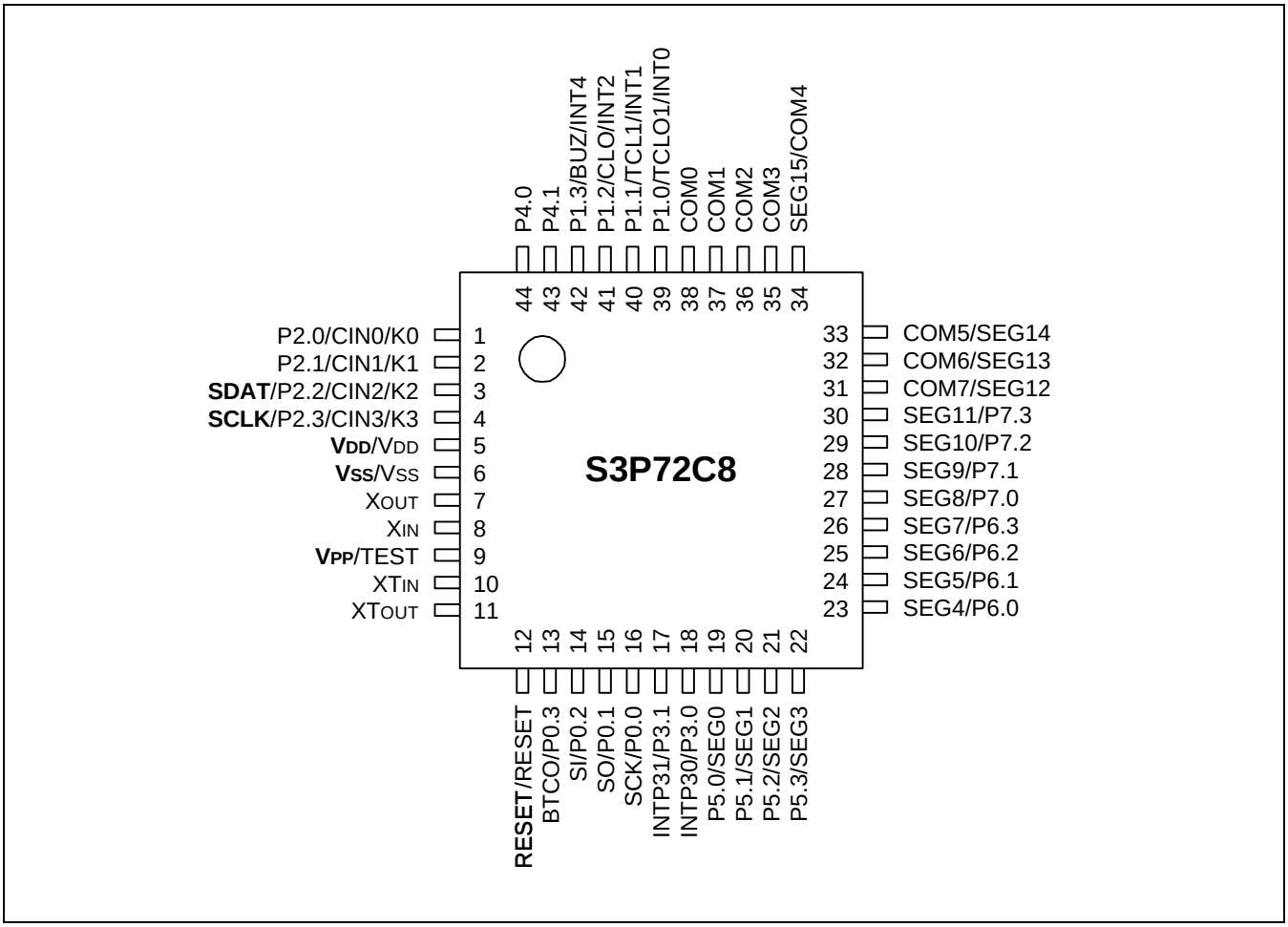


Figure 17-1. S3P72C8 44-QFP Pin Assignments

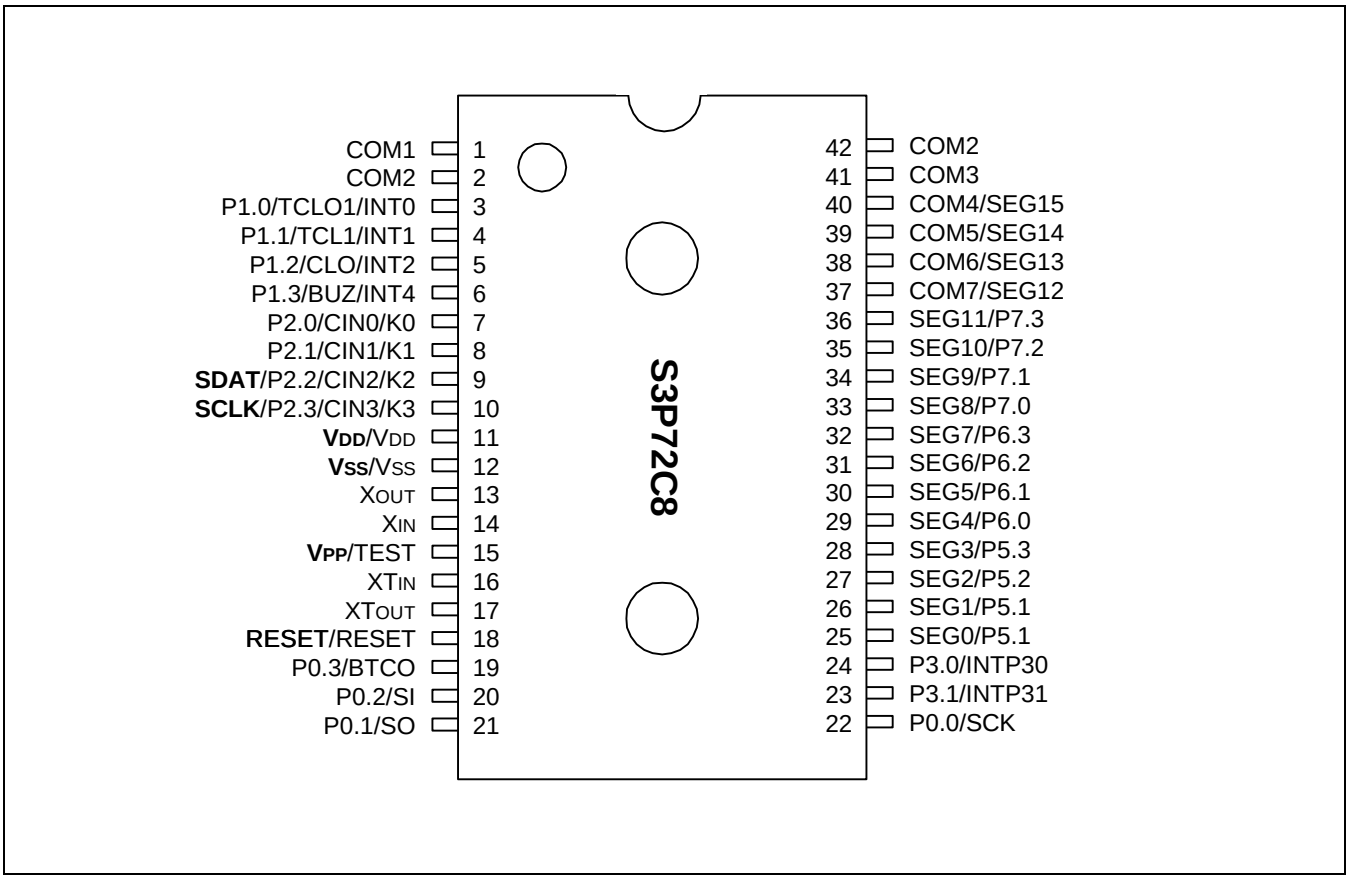


Figure 17-2. S3P72C8 42-SDIP Pin Assignments

Table 17-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P2.2	SDAT	3 (9)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P2.3	SCLK	4 (10)	I/O	Serial clock pin. Input only pin.
TEST	V_{PP}(TEST)	9 (15)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	12 (18)	I	Chip initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	5/6 (11/12)	I	Logic power supply pin. V_{DD} should be tied to + 5 V during programming.

NOTE: Parentheses indicate pin number for 42-SDIP package.

Table 17-2. Comparison of S3P72C8 and S3C72C8 Features

Characteristic	S3P72C8	S3C72C8
Program Memory	8 Kbyte EPROM	8 Kbyte mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP}(TEST)=12.5V	
Pin Configuration	44-QFP, 42-SDIP	44-QFP, 42-SDIP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the S3P72C8, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 17-3 below.

Table 17-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 17-4. D.C. Electrical Characteristics

(T_A = - 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1} (2)	V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz	–	3.0 2.3	8.0 5.5	mA
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		1.5 1.0	4.0 3.0	
	I_{DD2} (2)	Idle mode V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz		1.3 1.2	2.5 1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		0.5 0.44	1.5 1.0	
	I_{DD3} (3)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15.0	30	µA
	I_{DD4} (3)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			5.0	15	
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0000B XT_{IN} = 0V		2.5	5	
		Stop mode; V_{DD} = 3 V ± 10%			0.5	3	
		V_{DD} = 5 V ± 10%	SCMOD = 0100B		0.2	3	
		V_{DD} = 3 V ± 10%			0.1	2	

NOTES:

1. Currents in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, comparator, output port drive currents.
2. Data includes power consumption for subsystem clock oscillation.
3. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
4. Every values in this table is measured when the power control register (PCON) is set to "0011B".

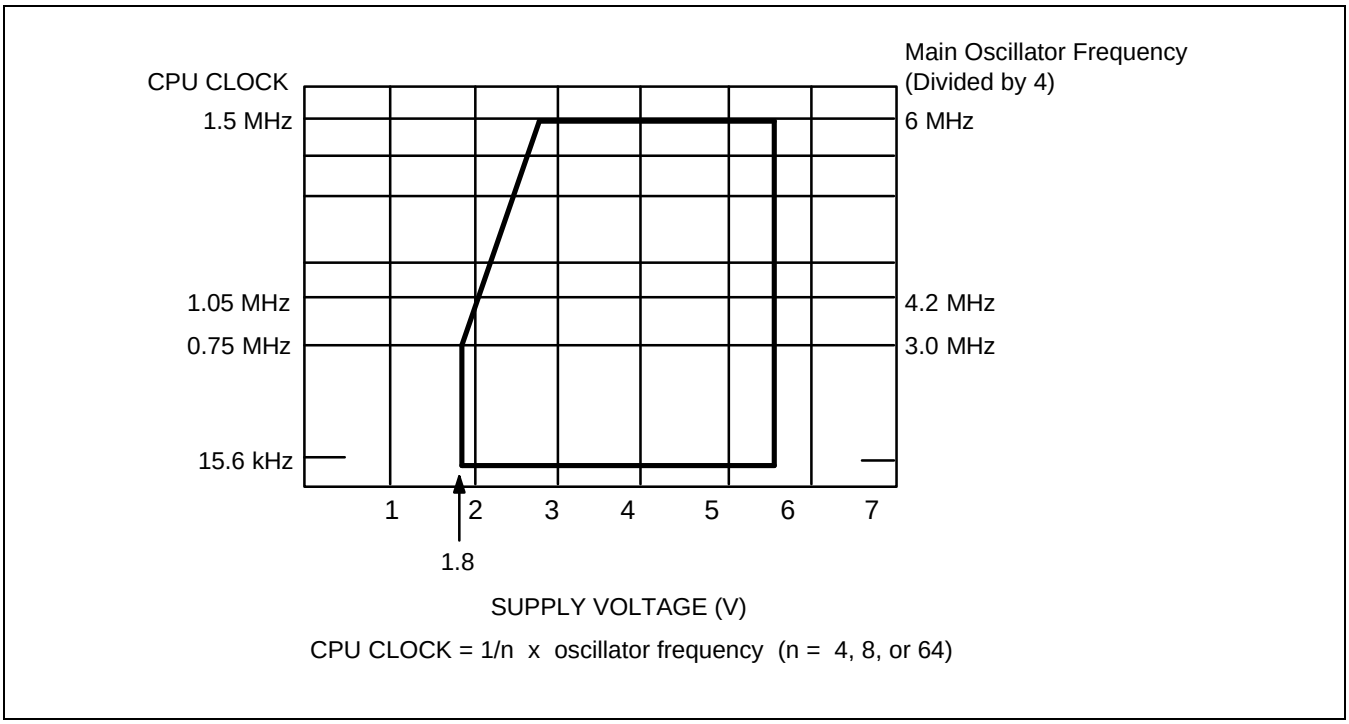


Figure 17-3 Standard Operating Voltage Range

NOTES