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PRODUCT OVERVIEW

SAM87 PRODUCT FAMILY

Samsung's SAM87 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

- Efficient register-oriented architecture
- Selectable CPU clock sources
- Release by interrupt of Idle and Stop power-down modes
- Built-in basic timer circuit with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

S3C8835/C8837/P8837

The S3C8835 microcontroller has 16 K bytes of on-chip program memory and the S3C8837 has 24 K bytes. Both chips have a 272-byte general-purpose internal register file. The interrupt structure has seven interrupt sources with six interrupt vectors. The CPU recognizes six interrupt priority levels.

Using a modular design approach, the following peripherals were integrated with the SAM87 core to make the S3C8835/C8837/P8837 suitable for use in color television and other types of screen display applications:

- Four programmable I/O ports (26 pins total: 16 general-purpose I/O pins; 8 n-channel, open-drain output pins)
- 2 channel A/D converter (4-bit resolution)
- 14-bit PWM output (one channels: push-pull type)
- Basic timer (BT) with watchdog timer function
- One 8-bit timer/counter (T0) with interval timer
- One 8-bit general-purpose timer/counter (TA) with prescalers
- On-screen display (OSD) with a wide range of programmable features including halftone control signal output

The S3C8835/C8837 are available in a versatile 42-pin SDIP package.

OTP

The S3C8835/C8837 microcontroller is also available in OTP (One Time Programmable) version, S3P8837. S3P8837 microcontroller has an on-chip 24K-byte one-time-programmable EPROM instead of masked ROM. The S3P8837 is comparable to S3C8835/C8837, both in function and in pin configuration.

FEATURES

CPU

- SAM87 CPU core

Memory

- 16-K byte (S3C8835) or 24K- byte (S3C8837) internal program memory
- 272-byte general-purpose register area

Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 750 ns (minimum) with an 8-MHz CPU clock

Interrupts

- 7 interrupt sources with 6 vectors
- 6 interrupt levels
- Fast interrupt processing for select levels

General I/O

- Four I/O ports (26 pins total)
- Six open-drain pins for up to 6-volt loads
- Two open-drain pins for up to 5-volt loads

8-Bit Basic Timer

- Three selectable internal clock frequencies
- Watchdog or oscillation stabilization function

Timer/Counters

- One 8-bit timer/counter (T0) with three internal clocks and interval timer mode.
- One general-purpose 8-bit timer/counters with interval timer mode (timer A)

A/D Converter

- Two analog input pins; 4-bit resolution
- 3.125 μ s conversion time (8-MHz CPU clock)

Pulse Width Modulation Module

- 14-bit PWM with one-channel output (push-pull type)
- PWM counter and data capture input pin
- Frequency: 5.859 kHz to 23.437 kHz with a 6-MHz CPU clock

On-Screen Display (OSD)

- Video RAM: 252 \times 12 bits
- Character generator ROM: 256 \times 18 \times 16 bits (256 display characters: fixed: 2, variable: 254)
- 252 display positions (12 rows \times 21 columns)
- 16-dot \times 18-dot character resolution
- 16 different character sizes
- Eight character colors
- Vertical direction fade-in/fade-out control
- Eight colors for character and frame background
- Halftone control signal output; selectable for individual characters
- Synchronous polarity selector for H-sync and V-sync input

Oscillator Frequency

- 5-MHz to 8-MHz external crystal oscillator
- Maximum 8-MHz CPU clock

Operating Temperature Range

- -20°C to $+85^{\circ}\text{C}$

Operating Voltage Range

- 4.5 V to 5.5 V

Package Type

- 42-pin SDIP

BLOCK DIAGRAM

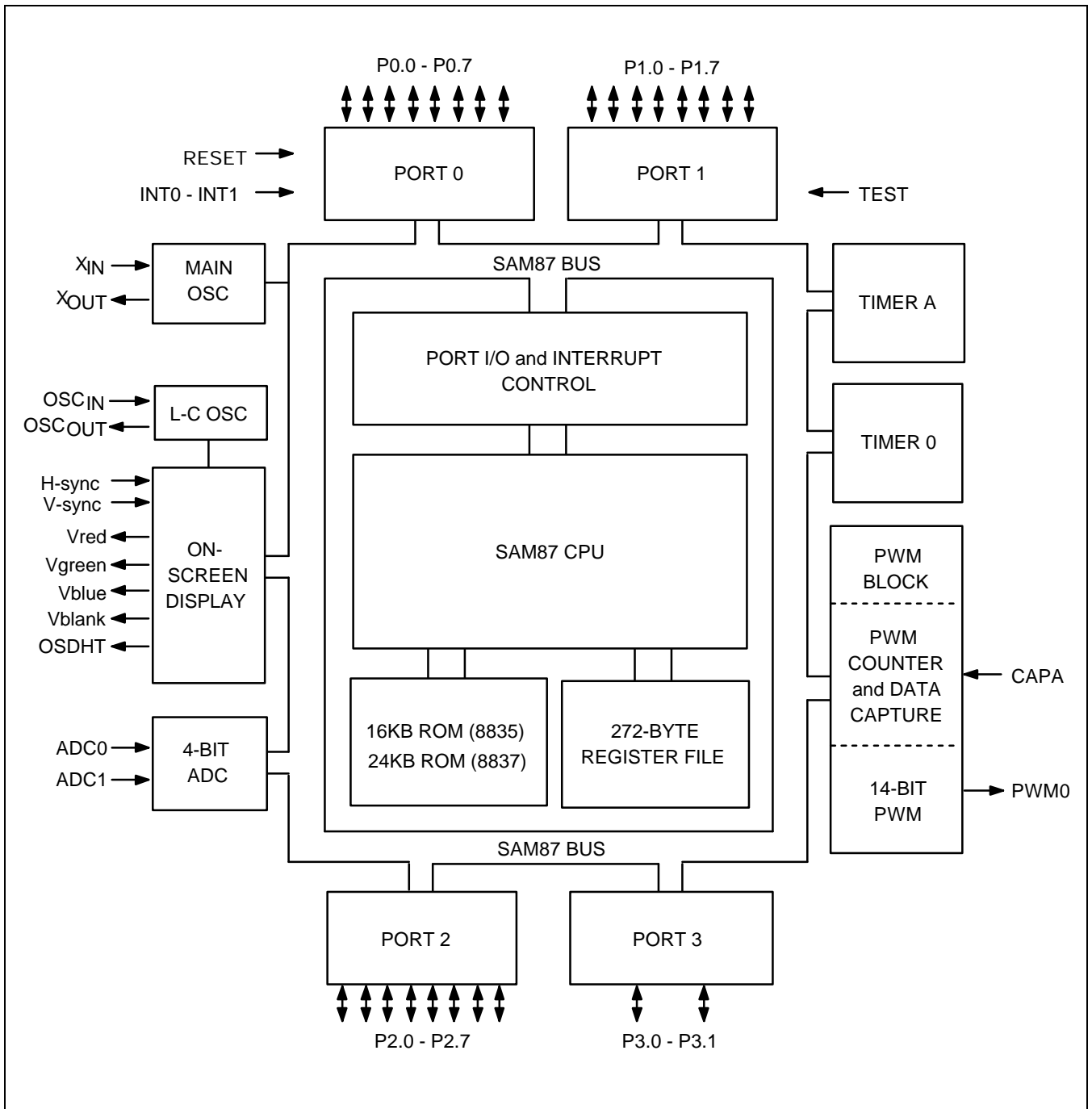


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

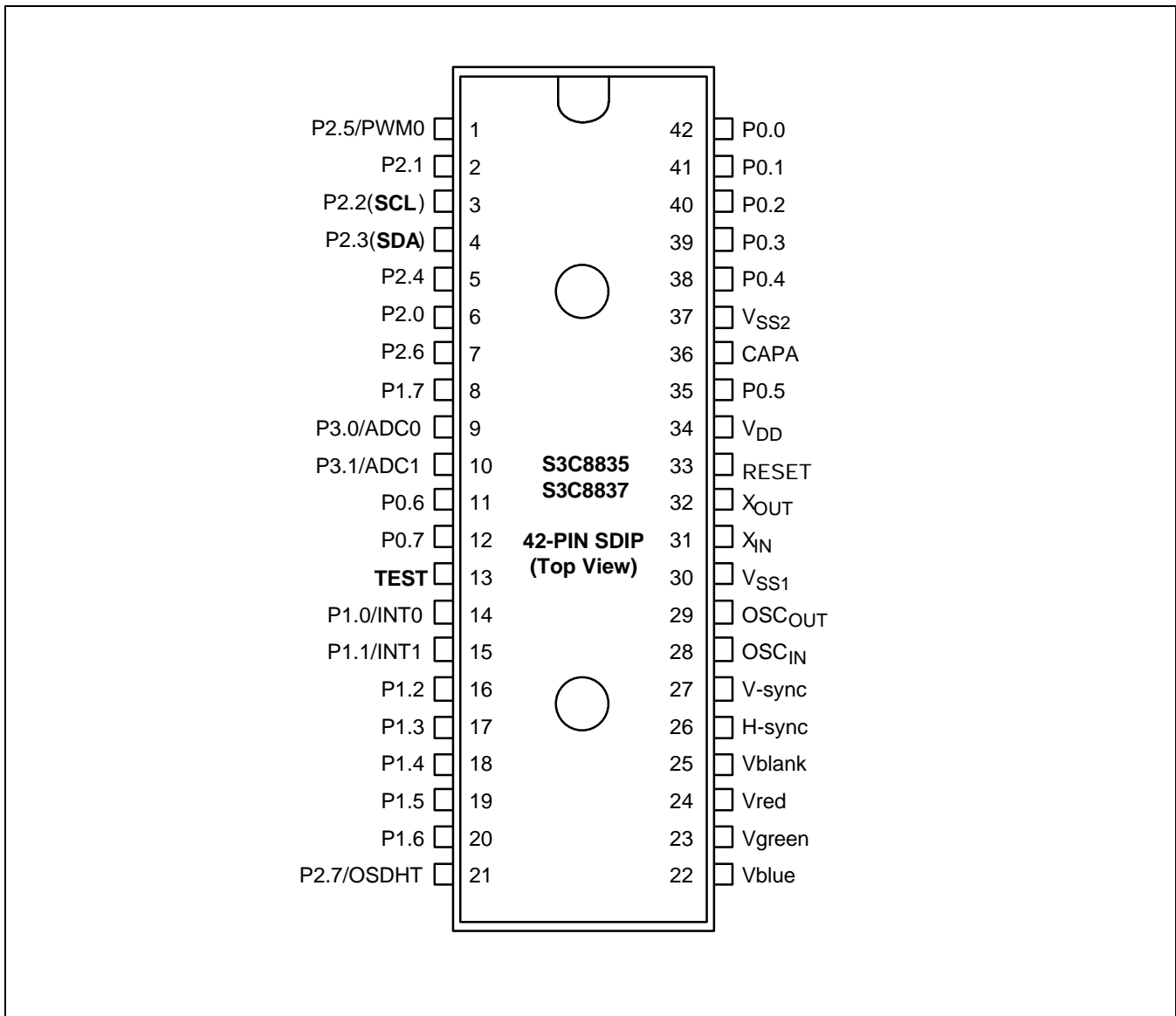


Figure 1-2. S3C8835/C8837/P8837 Pin Assignment Diagram

Table 1-1. S3C8835/C8837 Pin Descriptions

| Pin Name | Pin Type | Pin Description | Circuit Type | Pin Numbers | Share Pins |
|-----------------|----------|---|--------------|------------------|---------------|
| P0.0–P0.7 | I/O | General I/O port (8-bit), configurable for digital input or push-pull output. | 3 | 11–12, 35, 38–42 | |
| P1.0–P1.1 | I/O | General I/O port (2-bit), configurable for digital input or n-channel open-drain output. P1.0–P1.1 can withstand up to 6-volt loads. Multiplexed for alternative use as external interrupt inputs INTO–INT1. | 7 | 14–15 | INT0–INT1 |
| P1.2–P1.5 | | General I/O port (4-bit), configurable for digital input or n-channel open-drain output. P1.2–P1.5 can withstand up to 6-volt loads. High current port (10mA). | 5 | 16–19 | |
| P1.6–P1.7 | | General I/O port (2-bit), configurable for digital input or push-pull output. | 3 | 20, 8 | |
| P2.0–P2.4, P2.6 | I/O | General I/O port (6-bit). I/O mode or n-channel open-drain, push-pull output mode is software configurable. Pins can withstand up to 5-volt loads. P2.2: OTP serial clock pin P2.3: OTP serial data pin | 2 | 2–7 | |
| P2.5, P2.7 | | General I/O port (2-bit). I/O mode or n-channel open-drain, push-pull output mode is software configurable. Pins can withstand up to 5-volt loads. Each pin has an alternative function. P2.5: PWM0 (14-bit PWM output) P2.7: OSDHT (Halftone signal output) | 2 | 1, 21 | PWM0 OSDHT |

Table 1-1. S3C8835/C8837 Pin Descriptions (Continued)

| Pin Name | Pin Type | Pin Description | Circuit Type | Pin Numbers | Share Pins |
|---|----------|---|--------------|-------------|---------------|
| P3.0–P3.1 | I/O | General I/O port (2 bits), configurable for digital input or n-channel open-drain output. P3.0–P3.1 can withstand up to 5-volt loads. Multiplexed for alternative use as external interrupt inputs ADC0–ADC1. | 6 | 9–10 | ADC0 ADC1 |
| PWM0 | O | Output pin for 14-bit PWM0 circuit | 2 | 1 | P2.5 |
| ADC0–ADC1 | I | Analog inputs for 4-bit A/D converter | 6 | 9,10 | P3.0– P3.1 |
| INT0–INT1 | I | External interrupt input pins | 7 | 14,15 | P1.0– P1.1 |
| OSDHT | O | Halftone control signal output for OSD | 2 | 21 | P2.7 |
| Vblue, Vgreen Vred, Vblank | O | Digital blue, green, red, and video blank signal outputs for OSD | 4 | 22–25 | – |
| H-sync | I | H-sync input for OSD | 8 | 26 | – |
| V-sync | | V-sync input for OSD | | 27 | |
| OSC _{IN} , OSC _{OUT} | I, O | L-C oscillator pins for OSD clock frequency generation | – | 28,29 | – |
| TEST | I | 0 V: Normal operation mode 5 V: Factory test mode 12.5 V: OTP write mode | – | 13 | – |
| X _{IN} , X _{OUT} | I, O | System clock pins | – | 31, 32 | – |
| RESET | I | System reset input pin | 1 | 33 | – |
| V _{DD} , V _{SS1} , V _{SS2} | – | Power supply pins | – | 13 | – |
| CAPA | I | Input for capture A module | 8 | 26 | – |

PIN CIRCUITS

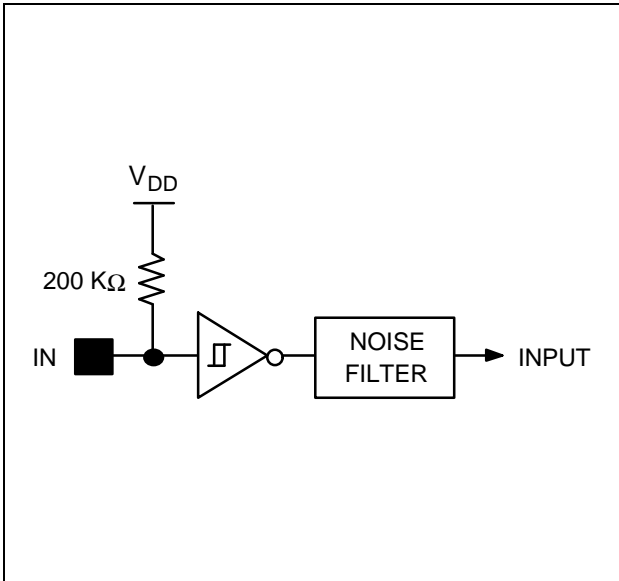


Figure 1-3. Pin Circuit Type 1 (RESET)

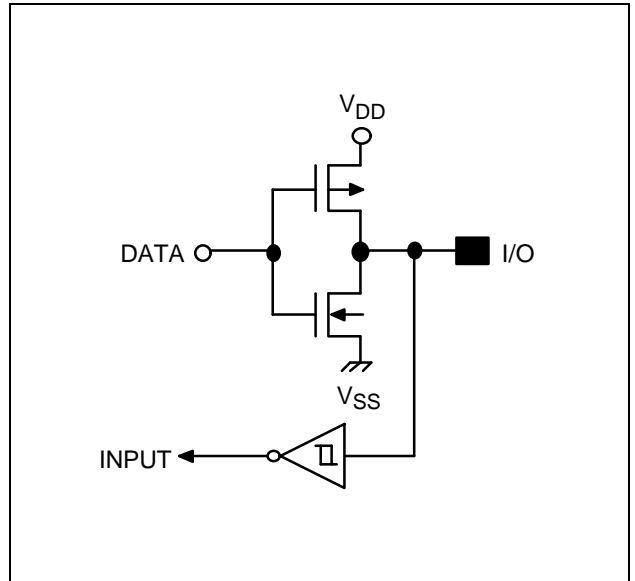


Figure 1-5. Pin Circuit Type 3 (P0.0-P0.7, P1.6-P1.7)

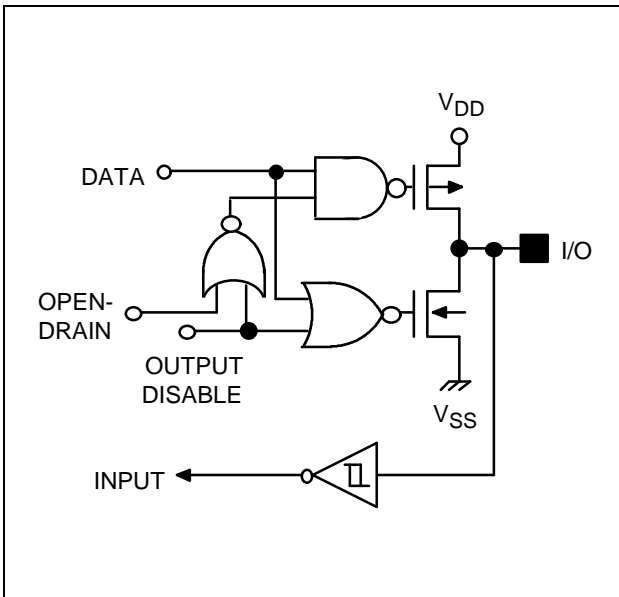


Figure 1-4. Pin Circuit Type 2 (P2.0-P2.7, PWM0, OSDHT)

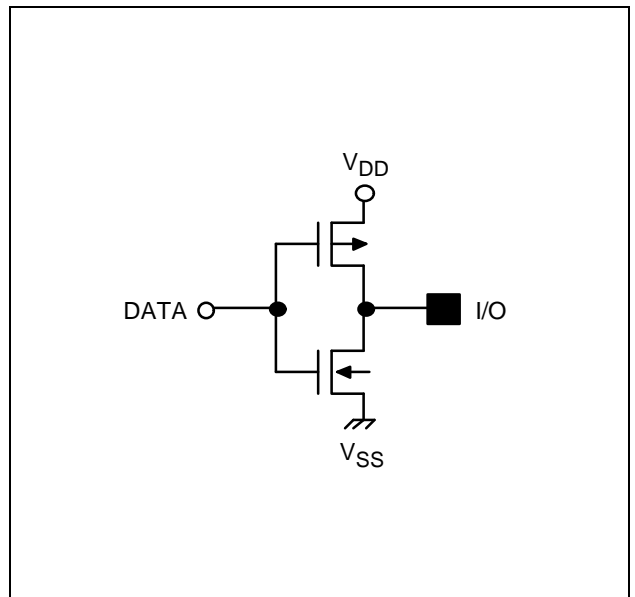


Figure 1-6. Pin Circuit Type 4 (Vblue, Vgreen, Vred, Vblank)

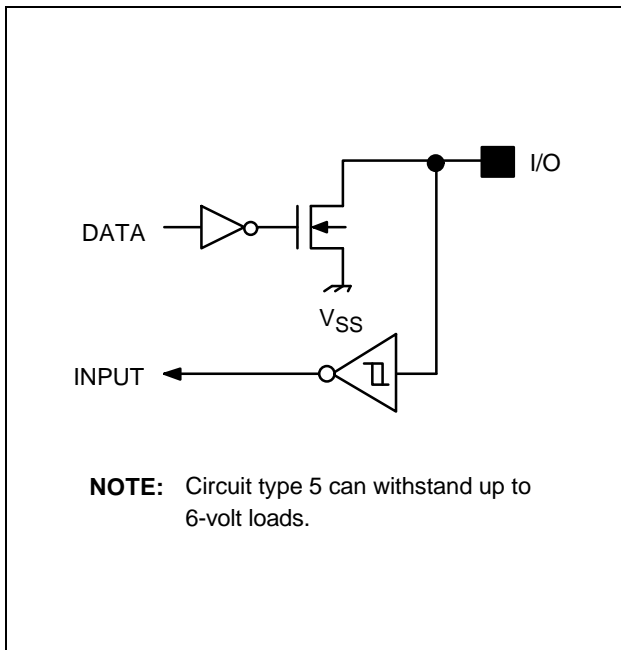


Figure 1-7. Pin Circuit Type 5 (P1.2–P1.5)

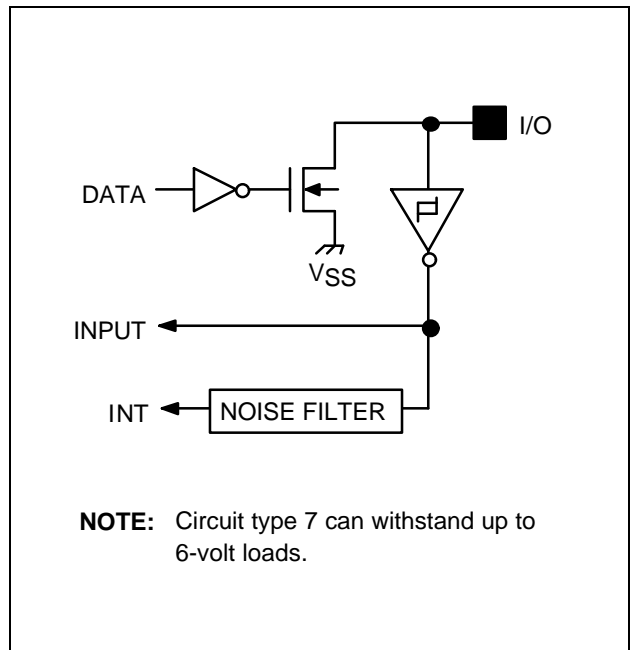


Figure 1-9. Pin Circuit Type 7 (P1.0–P1.1, INT0–INT1)

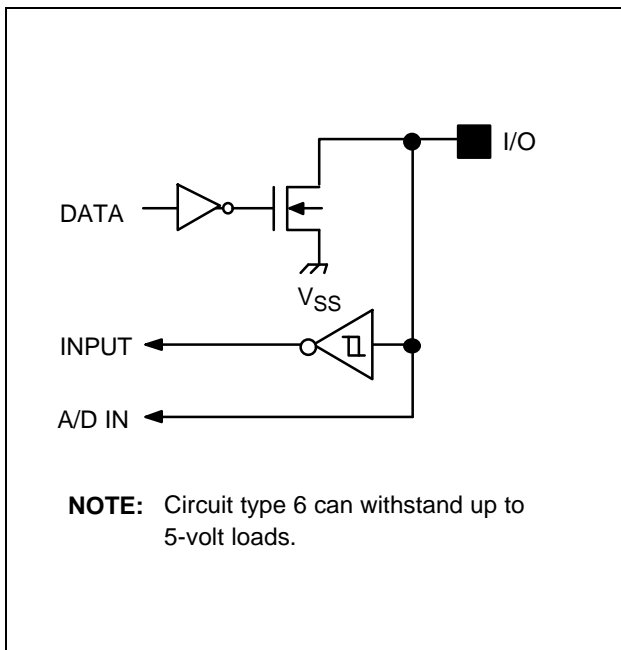


Figure 1-8. Pin Circuit Type 6 (P3.0–P3.1, ADC0–ADC1)

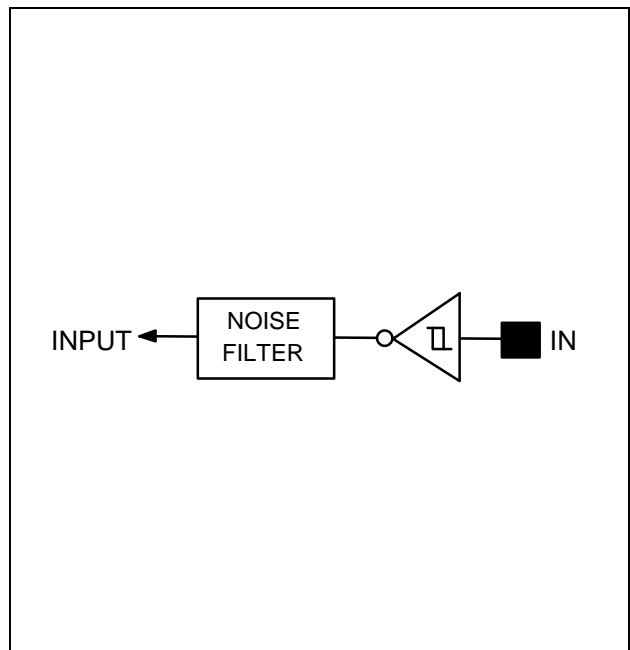


Figure 1-10. Pin Circuit Type 8 (V-Sync H-Sync, CAPA)

15 ELECTRICAL DATA

OVERVIEW

In this section, S3C8835/C8837 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- D.C. electrical characteristics
- I/O capacitance
- A.C. electrical characteristics
- Input timing measurement points for t_{NF1} and t_{NF2}
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by RESET
- Main oscillator and L-C oscillator frequency
- Clock timing measurement points for X_{IN}
- Main oscillator clock stabilization time (t_{ST})
- A/D converter electrical characteristics
- Characteristic curves

Table 15-1. Absolute Maximum Ratings

 $(T_A = 25^\circ\text{C})$

| Parameter | Symbol | Conditions | Rating | Unit |
|-----------------------|-----------|---|-------------------------|------------------|
| Supply Voltage | V_{DD} | – | – 0.3 to + 6.0 | V |
| Input Voltage | V_{I1} | P1.0–P1.5 (open-drain) | – 0.3 to + 7 | V |
| | V_{I2} | All port pins except V_{I1} | – 0.3 to $V_{DD} + 0.3$ | |
| Output Voltage | V_O | All output pins | – 0.3 to $V_{DD} + 0.3$ | V |
| Output Current High | I_{OH} | One I/O pin active | – 18 | mA |
| | | All I/O pins active | – 60 | |
| Output Current Low | I_{OL} | One I/O pin active | + 30 | mA |
| | | Total pin current for port 1 | + 100 | |
| | | Total pin current for ports 0, 2, and 3 | + 100 | |
| Operating Temperature | T_A | – | – 20 to + 85 | $^\circ\text{C}$ |
| Storage Temperature | T_{STG} | – | – 65 to + 150 | $^\circ\text{C}$ |

Table 15-2. D.C. Electrical Characteristics

 $(T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{DD} = 4.5\text{ V}$ to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---------------------|-----------|--|----------------|-----|--------------|------|
| Input High Voltage | V_{IH1} | All input pins except V_{IH2} | $0.8 V_{DD}$ | – | V_{DD} | V |
| | V_{IH2} | X_{IN} , X_{OUT} | 2.7 V | | | |
| Input Low Voltage | V_{IL1} | All input pins except V_{IL2} | – | – | $0.2 V_{DD}$ | V |
| | V_{IL2} | X_{IN} , X_{OUT} | | | 1.0 V | |
| Output High Voltage | V_{OH} | $I_{OH} = -500\ \mu\text{A}$ P0, P1.6–P1.7, P2 R, G, B, Vblank | $V_{DD} - 0.8$ | – | – | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 4\ \text{mA}$ P0, P1.6–P1.7 | – | – | 0.4 | V |
| | V_{OL2} | $I_{OL} = 10\ \text{mA}$ P1.2–P1.5 | – | – | 0.8 | |
| | V_{OL3} | $I_{OL} = 2\ \text{mA}$ P1.0–P1.1, P3.0–P3.1 | – | – | 0.4 | |
| | V_{OL4} | $I_{OL} = 1\ \text{mA}$ R, G, B, Vblank, P2 | – | – | 0.4 | V |

Table 15-2. D.C. Electrical Characteristics (Continued)

(T_A = -20°C to +85°C, V_{DD} = 4.5 V to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------------------------|-------------------|---|------|-----|-----|------|
| Input High Leakage Current | I _{LIH1} | V _{IN} = V _{DD} All input pins except I _{LIH2} and I _{LIH3} | – | – | 3 | μA |
| | I _{LIH2} | V _{IN} = V _{DD} , OSC _{IN} , OSC _{OUT} | | | 10 | |
| | I _{LIH3} | V _{IN} = V _{DD} , X _{IN} , X _{OUT} | 2.5 | 10 | 20 | |
| Input Low Leakage Current | I _{LIL1} | V _{IN} = 0 V All input pins except I _{LIL2} , I _{LIL3} , and RESET | – | – | –3 | μA |
| | I _{LIL2} | V _{IN} = 0 V, OSC _{IN} , OSC _{OUT} | | | –10 | |
| | I _{LIL3} | V _{IN} = 0 V, X _{IN} , X _{OUT} | –2.5 | –10 | –20 | |
| Output High Leakage Current | I _{LOH1} | V _{OUT} = V _{DD} All output pins except I _{LOH2} | – | – | 3 | μA |
| | I _{LOH2} | V _{OUT} = 6 V P1.0–P1.5 | | | 10 | |
| Output Low Leakage Current | I _{LOL} | V _{OUT} = 0 V All output pins | – | – | –3 | μA |
| Supply Current (note) | I _{DD1} | Normal mode; V _{DD} = 4.5 V to 5.5 V 8-MHz CPU clock | – | 7 | 20 | mA |
| | I _{DD2} | Idle mode; V _{DD} = 4.5 V to 5.5 V 8-MHz CPU clock | | 2 | 10 | |
| | I _{DD3} | Stop mode; V _{DD} = 4.5 V to 5.5 V | | 1 | 10 | μA |

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

Table 15-3. Input/Output Capacitance

(T_A = -20°C to +85°C, V_{DD} = 0 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------|------------------|---|-----|-----|-----|------|
| Input capacitance | C _{IN} | f = 1 MHz; unmeasured pins are connected to V _{SS} | - | - | 10 | pF |
| Output capacitance | C _{OUT} | | | | | |
| I/O capacitance | C _{IO} | | | | | |

Table 15-4. A.C. Electrical Characteristics

(T_A = -20°C to +85°C, V_{DD} = 4.5 V to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------|------------------|----------------------------------|-----|------|-----|-------------------|
| V-sync Pulse Width | t _{VW} | - | 4 | - | - | μs |
| H-sync Pulse Width | t _{HW} | - | 3 | - | - | μs |
| Noise Filter | t _{NF1} | P1.0-P1.1, V-sync | - | 350 | - | ns |
| | t _{NF2} | RESET | - | 1000 | | |
| | t _{NF3} | Glitch filter (oscillator block) | - | 15 | | |
| | t _{NF4} | CAPA | - | 5 | - | t _{CAPA} |
| | t _{NF5} | H-sync | - | 650 | - | ns |

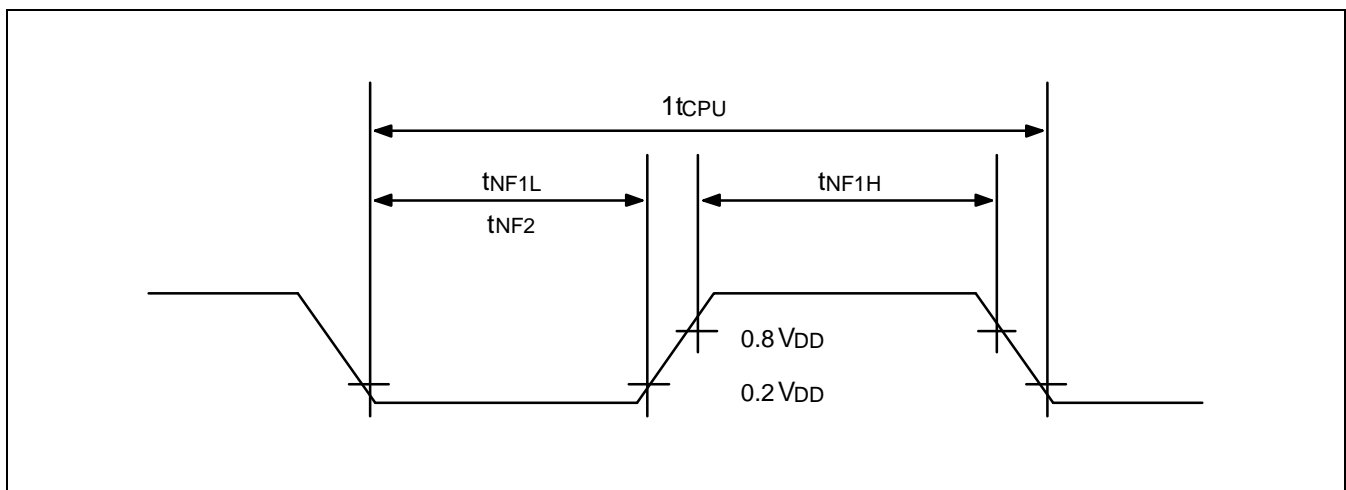
NOTE: t_{CAPA} = f_{OSC}/128.Figure 15-1. Input Timing Measurement Points for t_{NF1} and t_{NF2}

Table 15-5. Data Retention Supply Voltage in Stop Mode

($T_A = -20\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|------------|--------------------------------------|-----|-----|-----|---------------|
| Data Retention Supply Voltage | V_{DDDR} | Stop mode | 2 | – | 6 | V |
| Data Retention Supply Current | I_{DDDR} | Stop mode, $V_{DDDR} = 2.0\text{ V}$ | – | – | 5 | μA |

NOTES:

1. Supply current does not include current drawn through internal pull-up resistors or external output current loads.
2. During the oscillator stabilization wait time (t_{WAIT}), all CPU operations must be stopped.

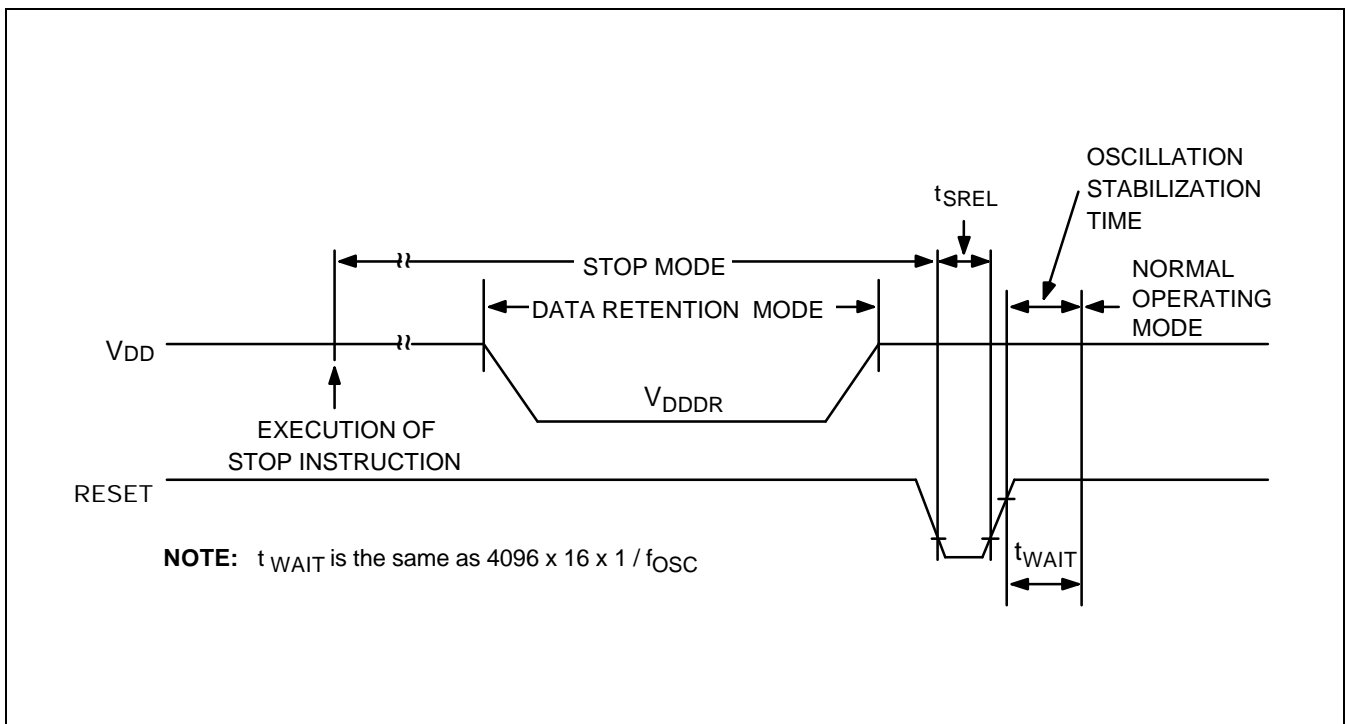
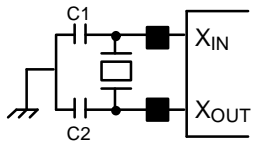
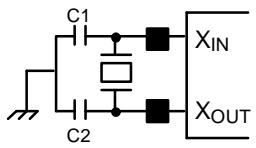
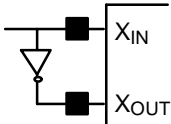
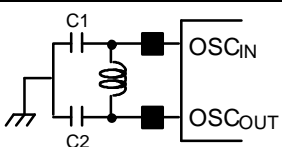


Figure 15-2. Stop Mode Release Timing When Initiated by a Reset

Table 15-6. Main Oscillator and L-C Oscillator Frequency

($T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{DD} = 4.5\text{ V}$ to 5.5 V)

| Oscillator | Clock Circuit | Conditions | Min | Typ | Max | Unit |
|---------------------|---|--|-------|-----|-----|------|
| Crystal |  | OSD block active | 5 | 6 | 8 | MHz |
| | | OSD block inactive | 0.5 | 6 | 8 | |
| Ceramic |  | OSD block active | 5 | 6 | 8 | MHz |
| | | OSD block inactive | 0.5 | 6 | 8 | |
| External Clock |  | OSD block active | 5 | 6 | 8 | MHz |
| | | OSD block inactive | 0.5 | 6 | 8 | |
| L-C Oscillator |  | Recommend value: $C1 = C2 = 20\text{ pF}$ | 5 | 6.5 | 8 | MHz |
| CPU Clock Frequency | | – | 0.032 | 6.0 | 8 | MHz |

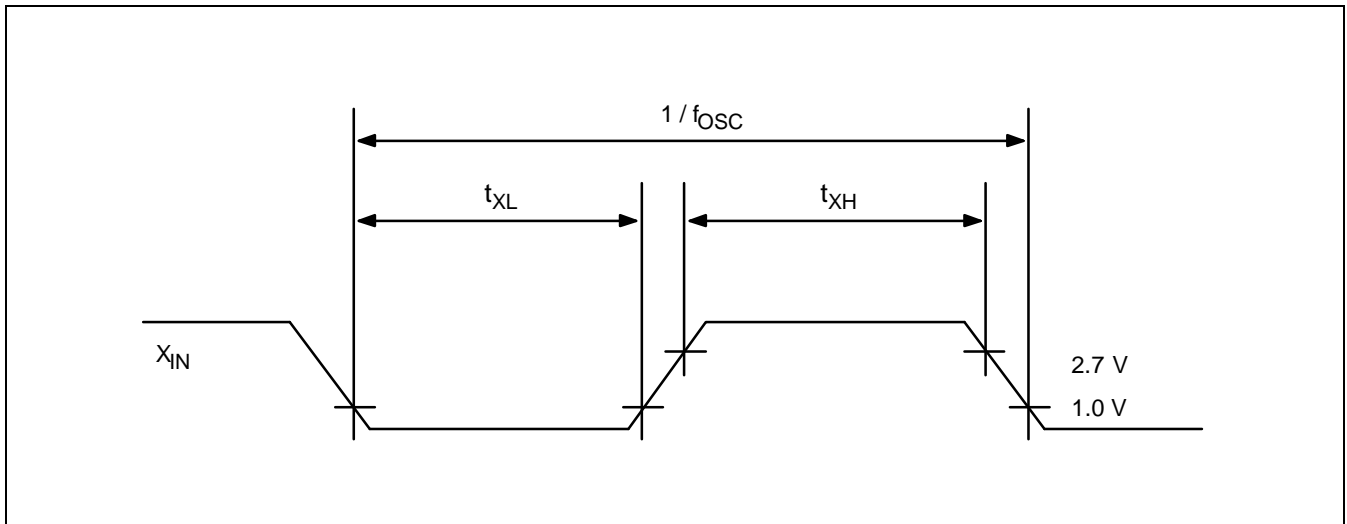


Figure 15-3. Clock Timing Measurement Points for X_{IN}

Table 15-7. Main Oscillator Clock Stabilization Time

(T_A = -20°C to +85°C, V_{DD} = 4.5 V to 5.5 V)

| Oscillator | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------|---|-----|------|-----|------|
| Crystal | - | V _{DD} = 4.5 V to 6.0 V | - | - | 20 | ms |
| Ceramic | | (Oscillation stabilization occurs when V _{DD} is equal to the minimum oscillator voltage range.) | | | 10 | |
| External Clock | | X _{IN} input High and Low level width (t _{XH} , t _{XL}) | | | 65 | - |
| Release Signal Setup Time | t _{SREL} | Normal operation | - | 1000 | - | ns |
| Oscillation Stabilization Wait Time ⁽¹⁾ | t _{WAIT} | CPU clock = 8 MHz; Stop mode released by RESET | - | 8.3 | - | ms |
| | | CPU clock = 8 MHz; Stop mode released by an interrupt | | (2) | | |

NOTES:

- Oscillation stabilization time is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is released.
- The oscillation stabilization interval is determined by the basic timer (BT) input clock setting.

Table 15-8. A/D Converter Electrical Characteristics

(T_A = -20°C to +85°C, V_{DD} = 4.5 V to 5.5 V, V_{SS} = 0 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------------|------------------|-------------------|-----------------|-----|-----------------|--------------------------------------|
| Absolute Accuracy ⁽¹⁾ | - | CPU clock = 8 MHz | - | - | ± 0.5 | LSB |
| Conversion Time ⁽²⁾ | t _{CON} | | | | | t _{CPU} × 25 ⁽³⁾ |
| Analog Input Voltage | V _{IAN} | - | V _{SS} | - | V _{DD} | V |
| Analog Input Impedance | R _{AN} | - | 2 | - | - | MΩ |

NOTES:

- Excluding quantization error, absolute accuracy values are within ± 1/2 LSB.
- 'Conversion time' is the time required from the moment a conversion operation starts until it ends.
- The unit t_{CPU} means one CPU clock period.

16 MECHANICAL DATA

OVERVIEW

The S3C8835/C8837 microcontrollers are available in a 42-pin SIP package (42-SDIP-600).

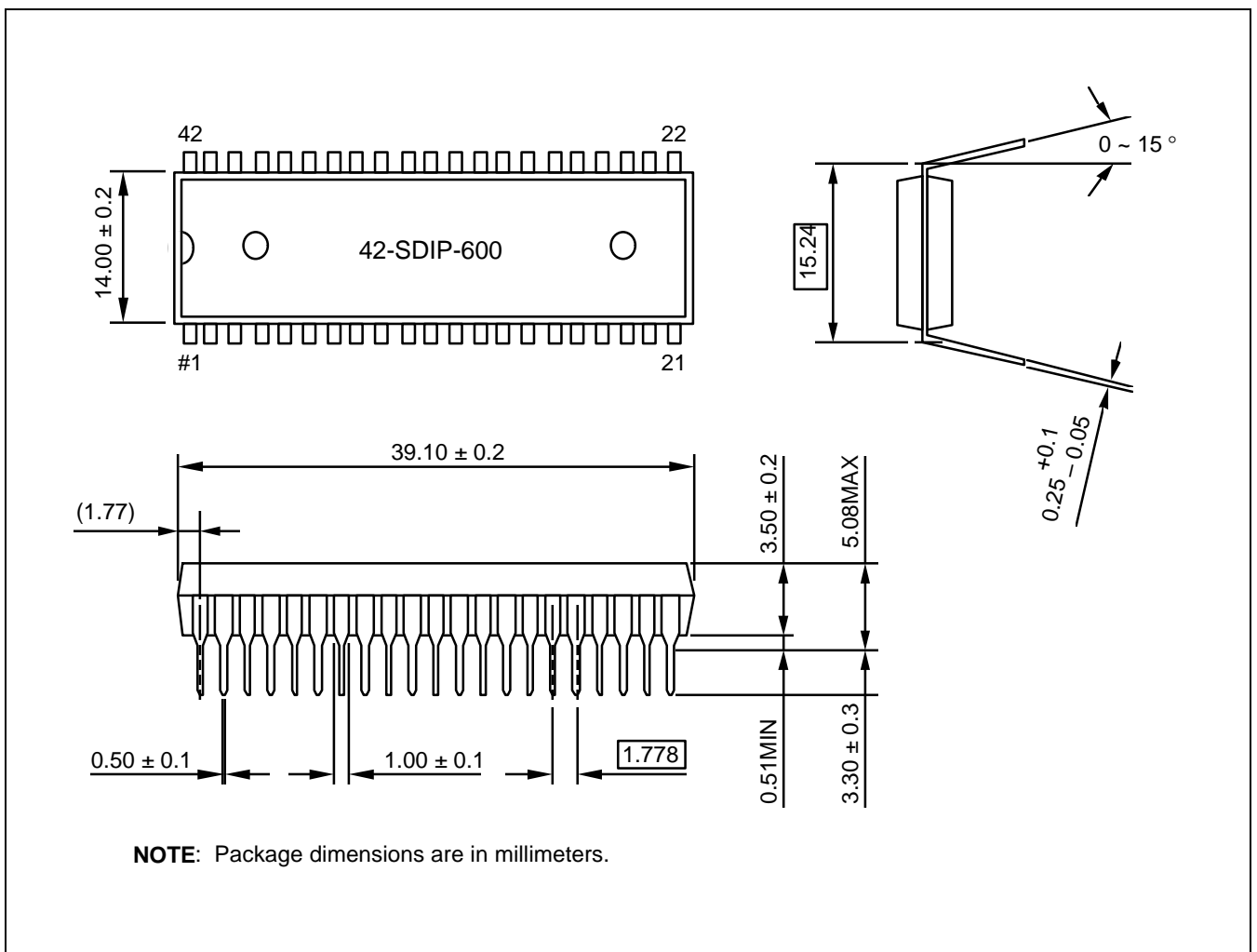


Figure 16-1. 42-Pin SDIP Package Mechanical Data (42-SDIP-600)

17

S3P8837 OTP

OVERVIEW

The S3P8837 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C8835/C8837 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P8837 is fully compatible with the S3C8835/C8837, both in function and in pin configuration. Because of its simple programming requirements, the S3P8837 is ideal for use as an evaluation chip for the S3C8835/C8837.

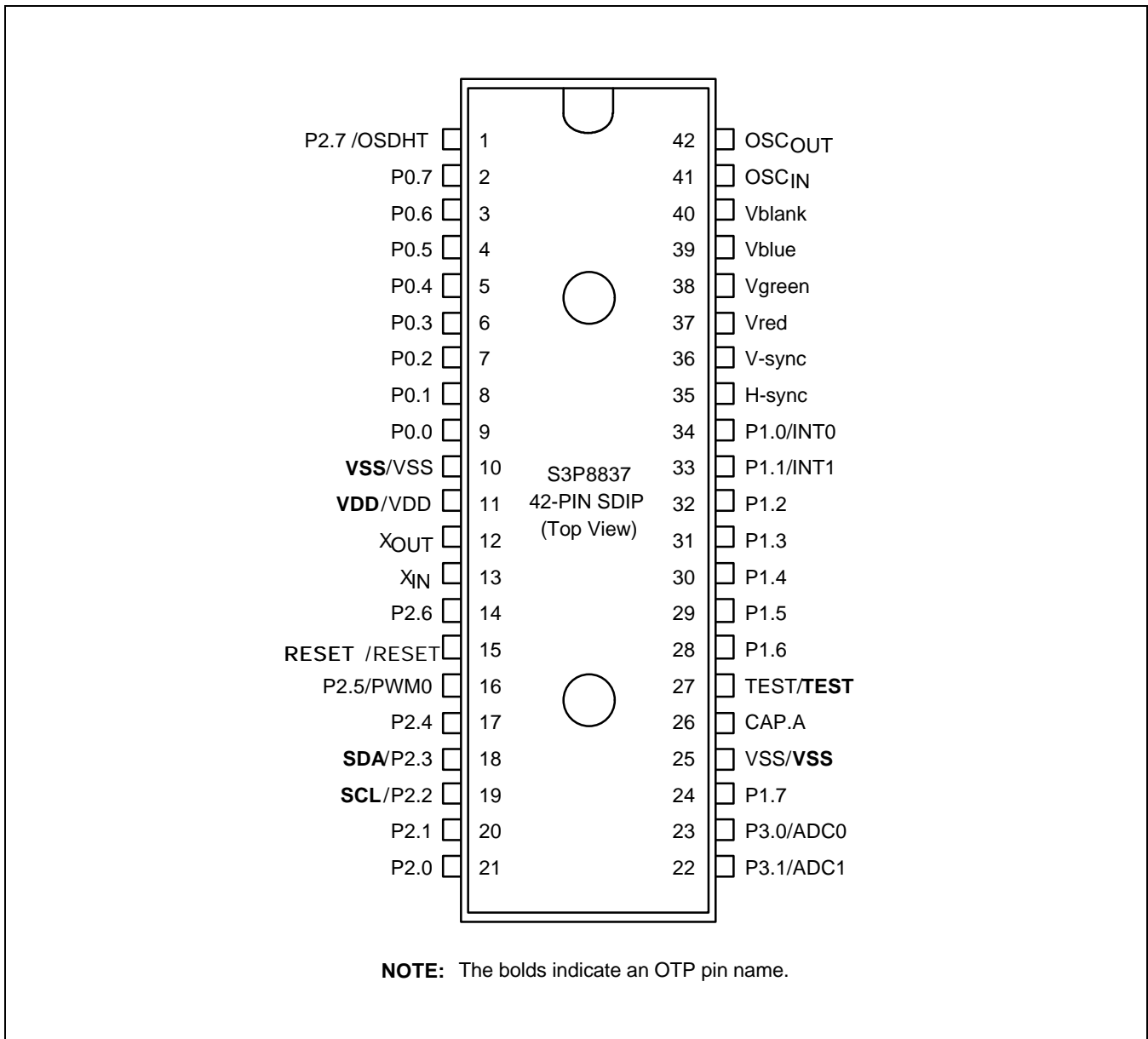


Figure 17-1. S3P8837 Pin Assignments (42-SDIP)

Table 17-1. Descriptions of Pins Used to Read/Write the EPROM

| Main Chip Pin Name | During Programming | | | |
|-----------------------|--------------------|-----------|-----|---|
| | Pin Name | Pin No. | I/O | Function |
| P2.3 (Pin 4) | SDAT | 4 | I/O | Serial data Pin (Output when reading, Input when writing) Input and Push-pull Output Port can be assigned |
| P2.2 (Pin 3) | SCLK | 3 | I/O | Serial clock Pin (Input Only Pin) |
| TEST | V_{PP} (TEST) | 13 | I | 0 V: Operating mode 5 V: Test mode 12.5 V: OTP mode |
| RESET | RESET | 33 | I | 0 V: Chip initialization, OTP mode 5 V: Operating mode |
| V_{DD}/V_{SS} | V_{DD}/V_{SS} | 34/30, 37 | I | Logic Power Supply Pin. |

Table 17-2. Comparison of S3P8837 and S3C8835/C8837 Features

| Characteristic | S3P8837 | S3C8835/C8837 |
|--------------------------------|---|---------------------------|
| Program Memory | 24K-byte EPROM | 24K-byte mask ROM |
| Operating Voltage (V_{DD}) | 4.5 V to 5.5 V | 4.5 V to 5.5 V |
| OTP Programming Mode | $V_{DD} = 5 V$, V_{PP} (TEST) = 12.5 V | – |
| Pin Configuration | 42-SDIP | 42-SDIP |
| EPROM Programmability | User Program 1 time | Programmed at the factory |