1 PRODUCT OVERVIEW

SAM88RCRI PRODUCT FAMILY

Samsung's SAM88RCRI family of 8-bit single-chip CMOS microcontrollers offer fast and efficient CPU, a wide range of integrated peripherals, and supports OTP device.

A dual address/data bus architecture and bit- or nibble-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations.

S3C921F/P921F MICROCONTROLLER

The S3C921F can be used for dedicated control functions in a variety of applications, and is especially designed for application with voice synthesizer or etc.

The S3C921F/P921F single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM88RCRI CPU core.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The S3C921F/P921F has 64 Kbytes of program ROM and 192 Kbytes of data ROM on-chip (S3C921F), and 720 bytes of RAM including 16 bytes of working register and 128 bytes of LCD display RAM.

Using the SAM88RCRI design approach, the following peripherals were integrated with the SAM88RCRI core:

— Four configurable I/O ports including ports shared with segment/common drive outputs
— 8-bit programmable pins for external interrupts
— One 8-bit basic timer for oscillation stabilization and watch-dog functions
— One 8-bit and one 16-bit timer/counter with selectable operating modes
— Watch timer for real time
— Two PWM modules for direct speaker drive

OTP

The S3C921F microcontroller is also available in OTP (One Time Programmable) version. S3P921F microcontroller has an on-chip 256 Kbyte one-time-programmable EPROM instead of masked ROM. The S3P921F is comparable to S3C921F, both in function and in pin configuration.

FEATURES

CPU

- SAM88RCRI CPU core

Memory

- 64K × 8 bits program memory(ROM)
- 192K × 8 bits data memory(ROM)
- 592 × 8 bits data memory(RAM)
  (Excluding LCD data memory)

Instruction Set

- 41 instructions
- Idle and Stop instructions added for power-down modes

32 I/O Pins

- I/O: 8 pins
- I/O: 24 pins(Sharing with segment drive outputs)

Interrupts

- 15 interrupt source and 1 vector
- One interrupt level

8-Bit Basic Timer

- Watchdog timer function
- 3 kinds of clock source

One 8-Bit Timer/Counter 0

- Programmable interval timer
- External event counter function
- PWM and Capture function

One 16-bit Timer/Counter 1

- One 16-bit Timer/Counter mode
- Two 8-bit Timer/Counters A/B mode

Watch Timer

- Interval time: 3.91mS, 0.25S, 0.5S, and 1S at 32.768 kHz
- 2/4/8/16 kHz Selectable buzzer output

LCD Controller/Driver

- 64 segments and 16 common terminals
- 8, 12, and 16 common selectable
- Internal resistor circuit for LCD bias

Two PWM Modules

- 5/6/7/8-bits PWM Selectable
- Direct speaker drive
- 2-bit extendable

Voltage Level Detector

- Programmable low voltage detector
- Two criteria voltage(2.7 V, 4.0 V)

Two Power-Down Modes

- Idle: only CPU clock stops
- Stop: selected system clock and CPU clock stop

Oscillation Sources

- Crystal, ceramic, or RC for main clock
- Main clock frequency: 0.4 MHz - 8MHz
- 32.768 kHz crystal oscillation circuit for sub clock

Instruction Execution Times

- 500nS at 8 MHz fx(minimum)

Operating Voltage Range

- 2.4 V to 5.5 V at 0.4 - 3MHz
- 2.7 V to 5.5 V at 0.4 - 4MHz
- 4.5 V to 5.5 V at 0.4 - 8MHz

Operating Temperature Range

- -40 °C to +85 °C

Package Type

- 100-pin QFP Package

BLOCK DIAGRAM

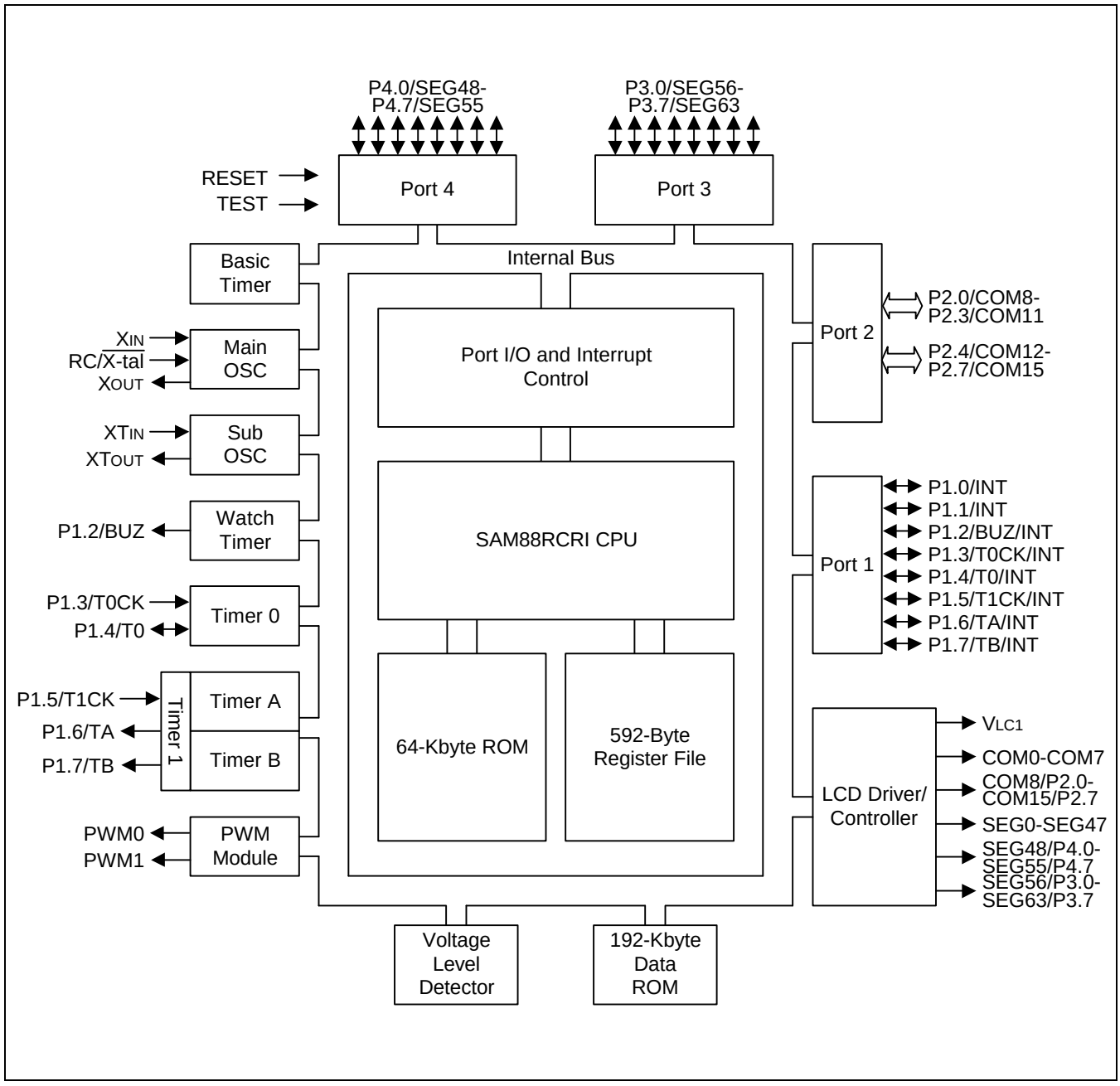


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

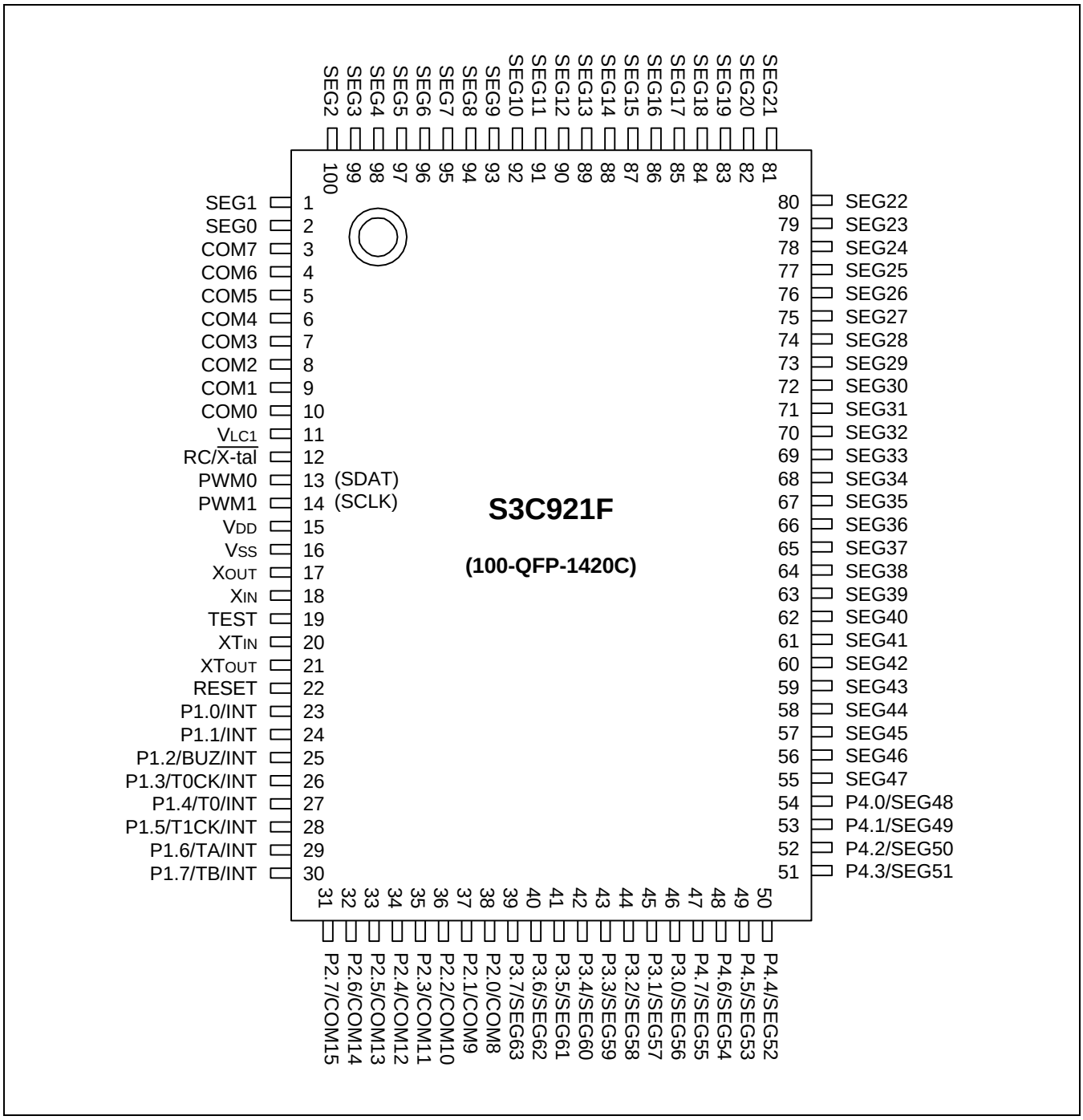


Figure 1-2. Pin Assignment (100 Pin)

Table 1-1. Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Number	Pin Numbers	Share Pins
P1.0, P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7	I/O	I/O port with bit-programmable pins; Schmitt trigger input or push-pull, open-drain output and software assignable pull-ups; Alternately used for external interrupt input(noise filters, interrupt enable and pending control).	E-2	23, 24 25 26 27 28 29 30	INT BUZ/INT T0CK/INT T0/INT T1CK/INT TA/INT TB/INT
P2.0 - P2.7	I/O	I/O port with nibble-programmable pins; Schmitt trigger input or push-pull, open-drain output and software assignable pull-ups.	H-9	38 - 31	COM8-COM15
P3.0 - P3.7	I/O	I/O port with bit-programmable pins; Schmitt trigger input or push-pull, open-drain output and software assignable pull-ups.	H-8	46 - 39	SEG56-SEG63
P4.0 - P4.7	I/O	I/O port with nibble-programmable pins; Schmitt trigger input or push-pull output and software assignable pull-ups.	H-10	54 - 47	SEG48-SEG55
PWM0 PWM1	O	PWM output pins.	C	13 14	–
V_{LC1}	I	LCD power supply pin.	–	11	–
INT	I/O	External interrupt input pins.	E-2	23, 24 25 26 27 28 29 30	P1.0, P1.1 P1.2/BUZ P1.3/T0CK P1.4/T0 P1.5/T1CK P1.6/TA P1.7/TB
BUZ	I/O	Output pin for buzzer signal.	E-2	25	P1.2/INT
T0CK	I/O	Timer 0 clock input.	E-2	26	P1.3/INT
T0	I/O	Capture input or interval/PWM output.	E-2	27	P1.4/INT
T1CK	I/O	Timer 1/A external clock input.	E-2	28	P1.5
TA	I/O	Timer 1/A clock output.	E-2	29	P1.6
TB	I/O	Timer B clock output.	E-2	30	P1.7
COM0-COM7	O	LCD common data outputs.	H-4	10 - 3	–
COM8-COM15	I/O	LCD common data outputs.	H-9	38 - 31	P2.0 - P2.7
SEG0-SEG47	O	LCD segment data outputs.	H-5	2-1 100-55	–
SEG48-SEG55 SEG56-SEG63	I/O	LCD segment data outputs.	H-10 H-8	54 - 47 46 - 39	P4.0 - P4.7 P3.0 - P3.7

Table 1-1. Pin Descriptions (Continued)

Pin Names	Pin Type	Pin Description	Circuit Number	Pin Numbers	Share Pins
RESET	I	System reset pin	B	22	–
XT_{IN},XT_{OUT}	–	Crystal oscillator pins for sub clock.	–	20, 21	–
X_{IN},X_{OUT}	–	Main oscillator pins.	–	18, 17	–
RC/$\overline{\text{X-tal}}$	–	Main oscillator type selection pin ("High" for RC osc. and "Low" for X-tal)	–	12	–
TEST	I	Test input: it must be connected to V_{SS}	–	19	–
V_{DD},V_{SS}	–	Power input pins	–	15, 16	–

PIN CIRCUIT DIAGRAMS

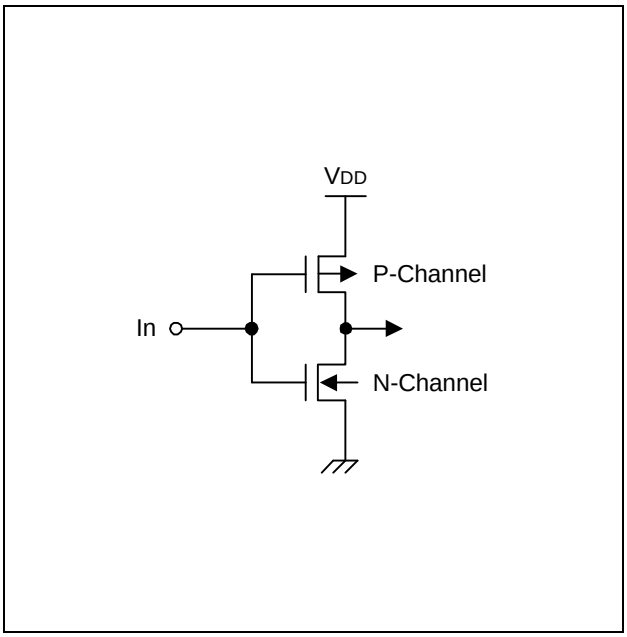


Figure 1-3. Pin Circuit Type A

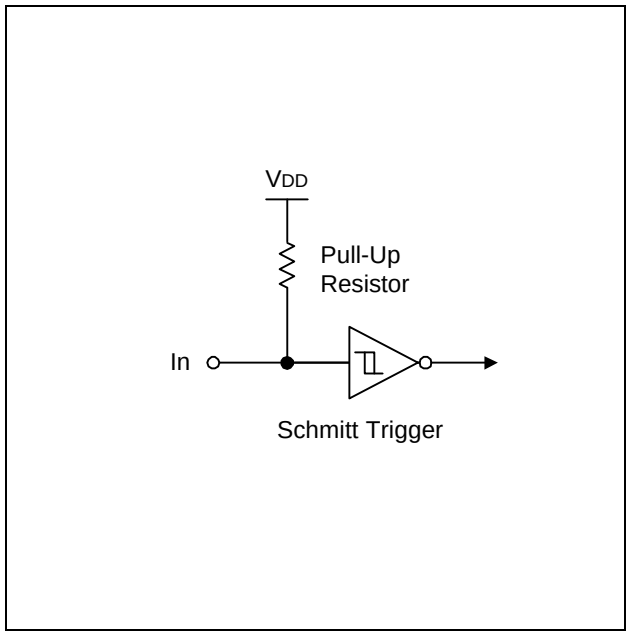


Figure 1-4. Pin Circuit Type B

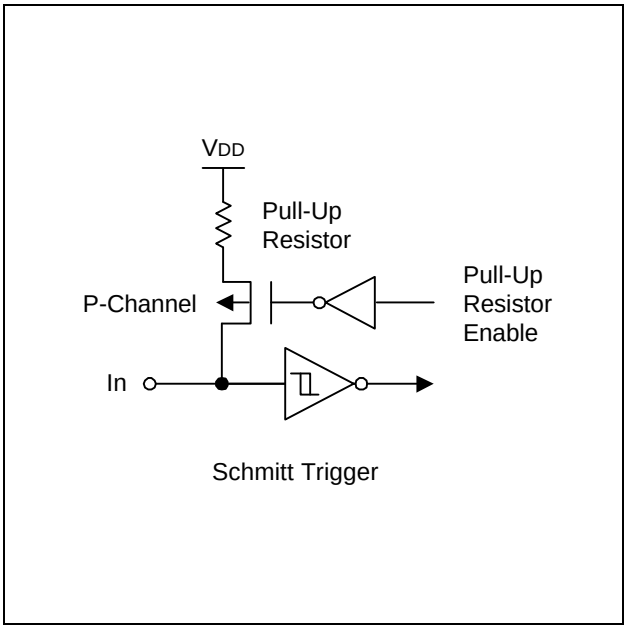


Figure 1-5. Pin Circuit Type A-3

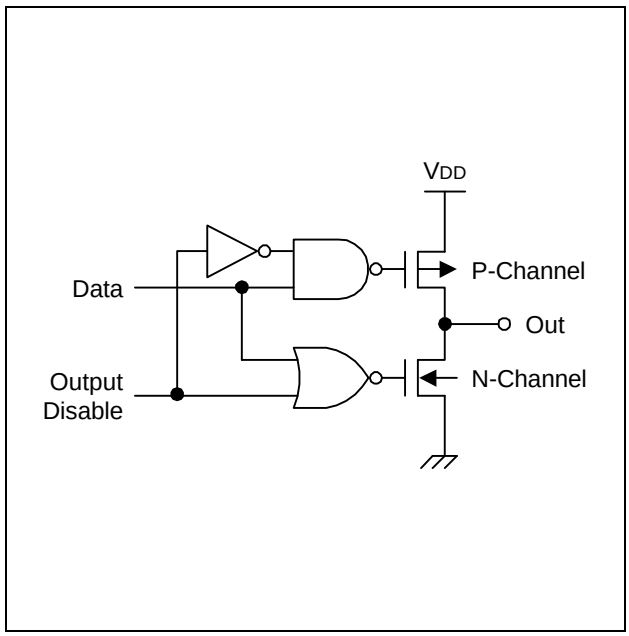


Figure 1-6. Pin Circuit Type C

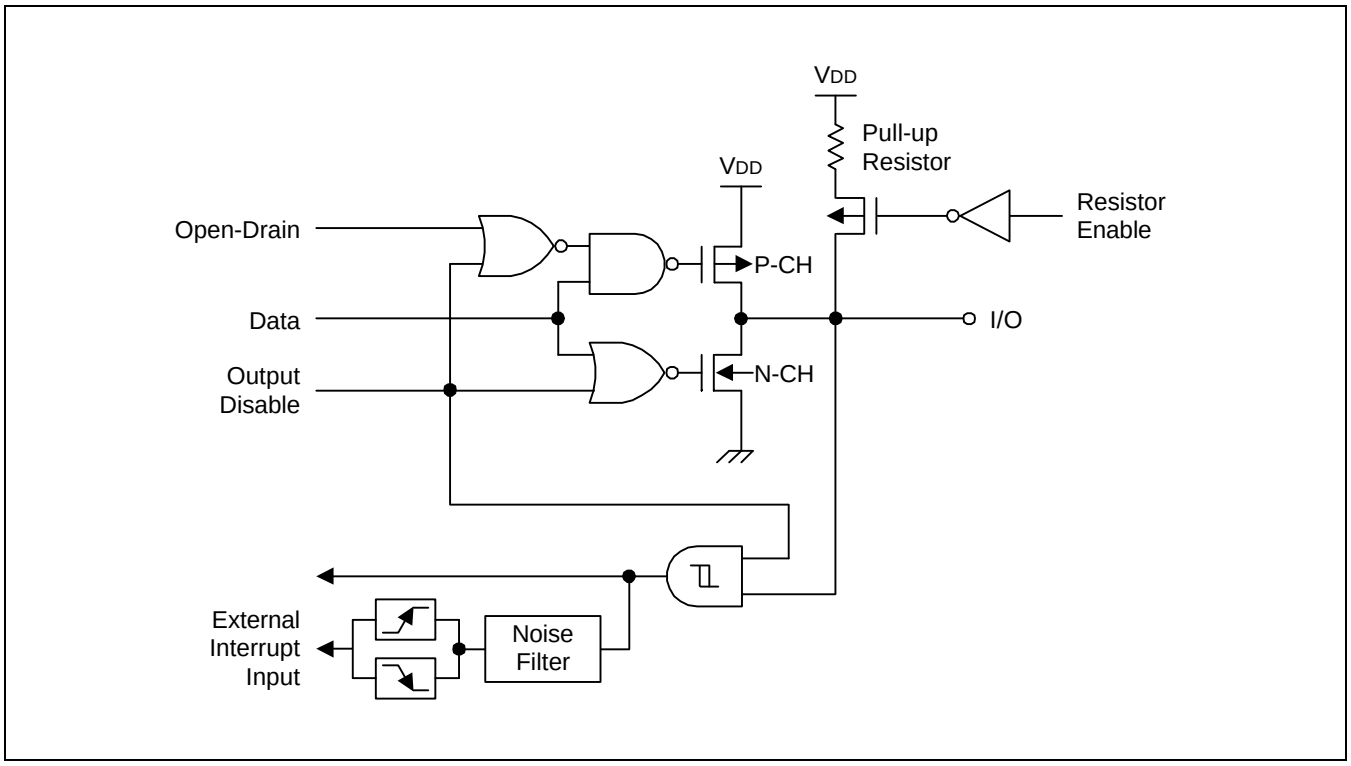


Figure 1-7. Pin Circuit Type E-2

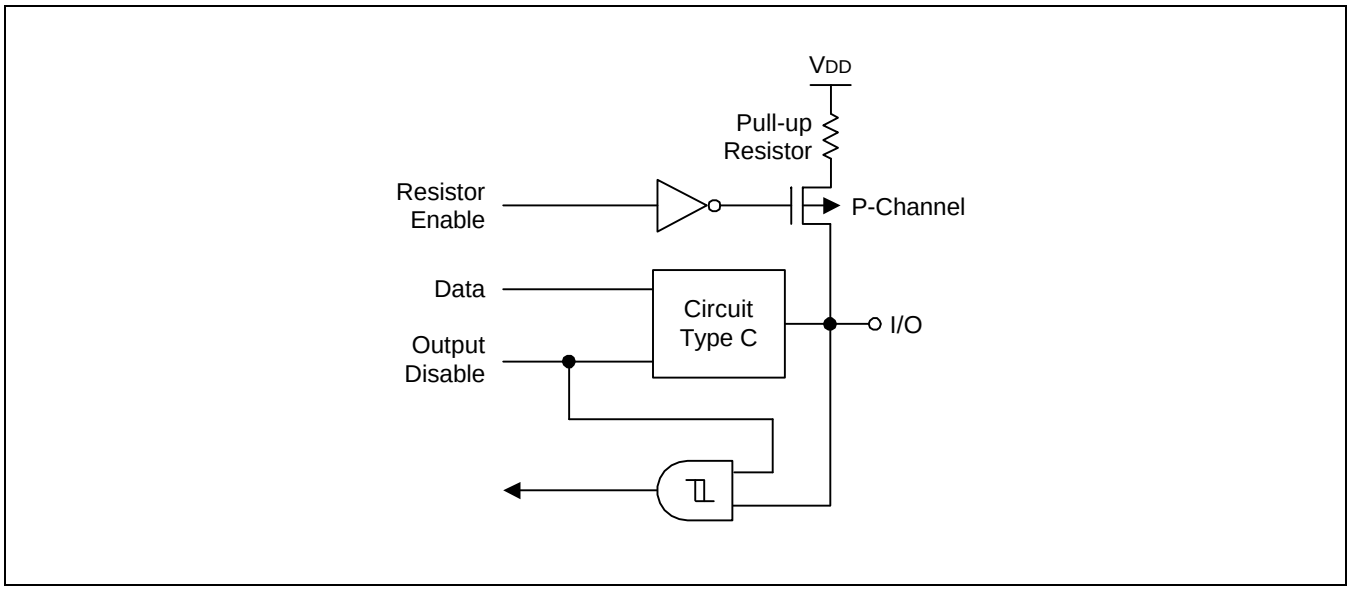


Figure 1-8. Pin Circuit Type E-3

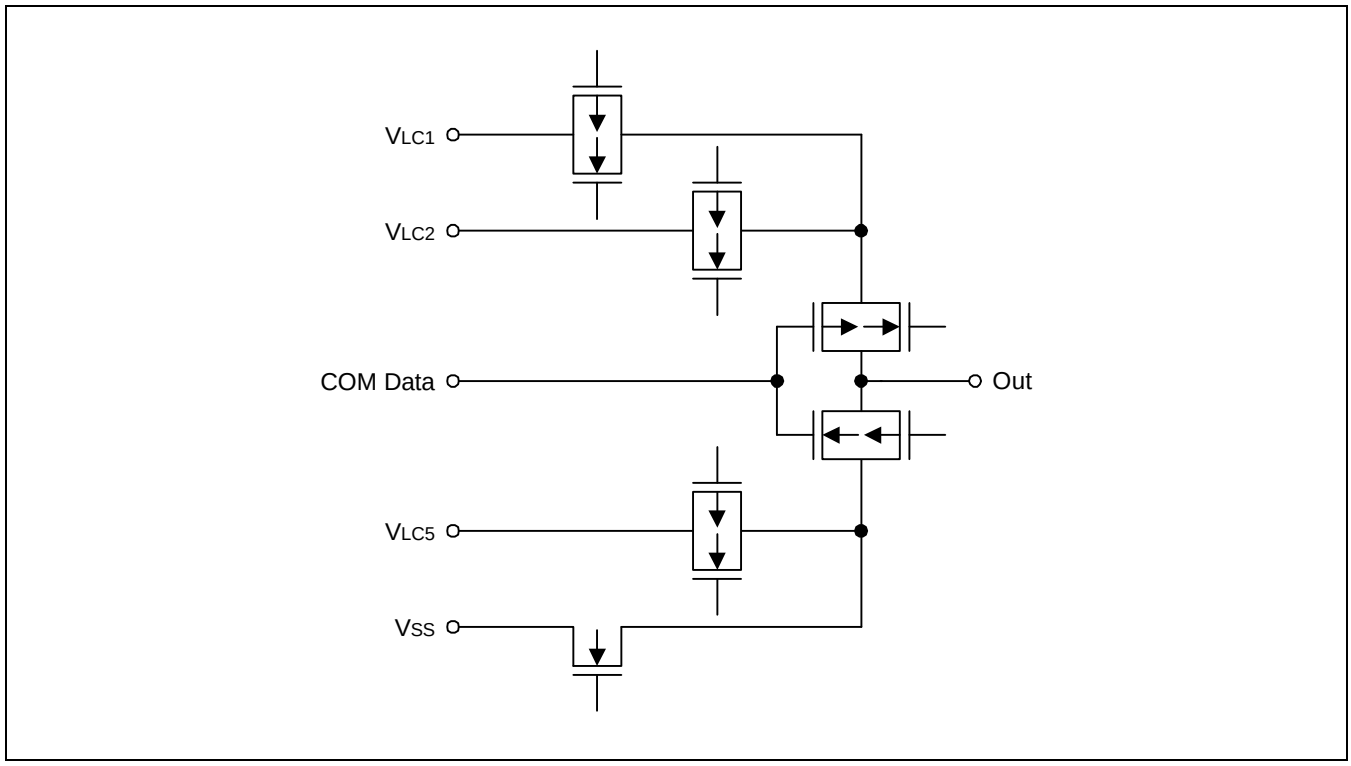


Figure 1-9. Pin Circuit Type H-4

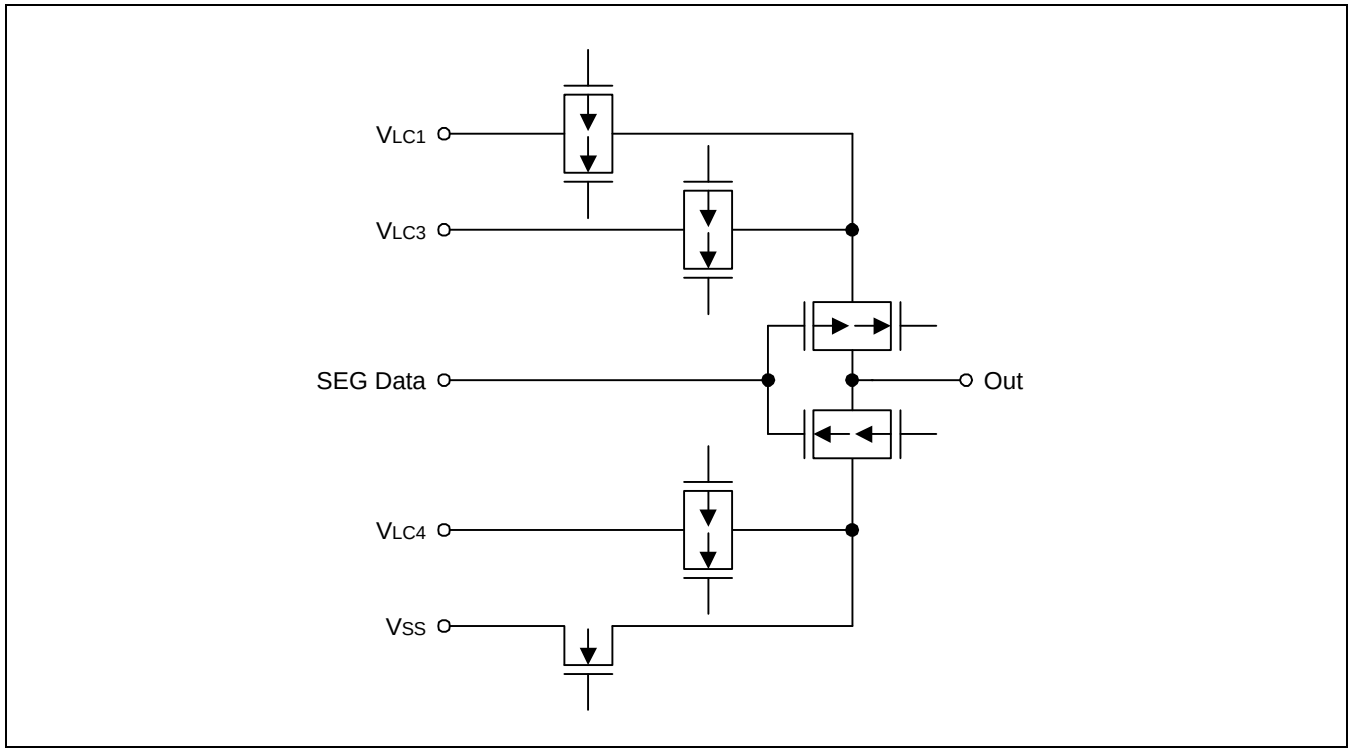


Figure 1-10. Pin Circuit Type H-5

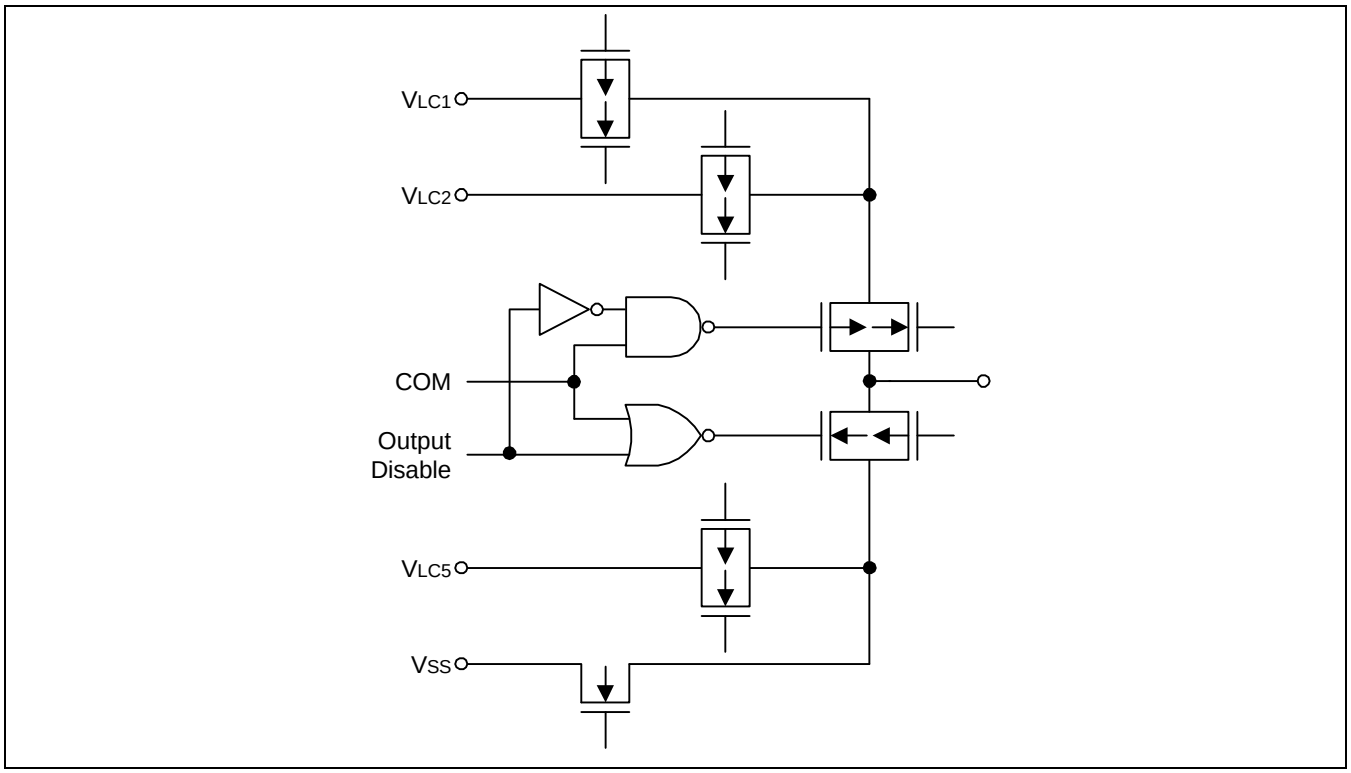


Figure 1-11. Pin Circuit Type H-6

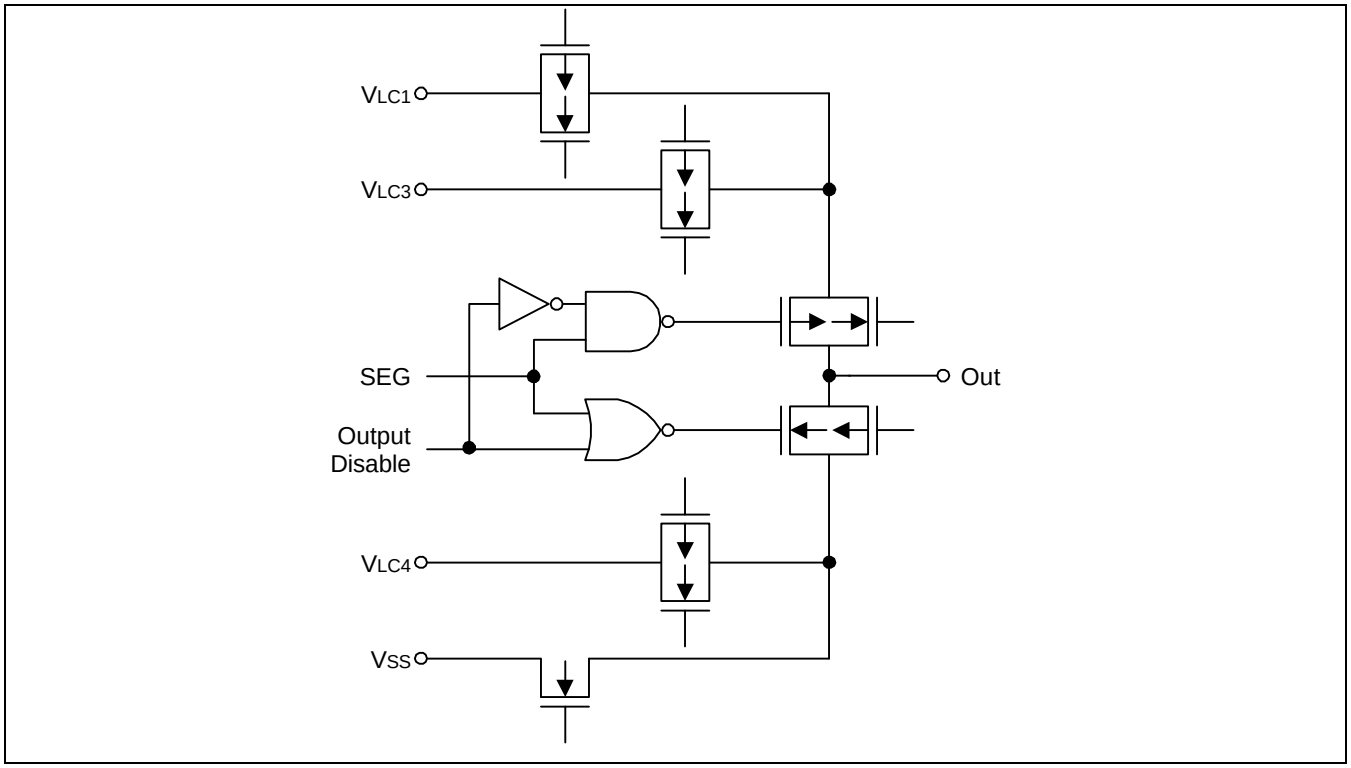


Figure 1-12. Pin Circuit Type H-7

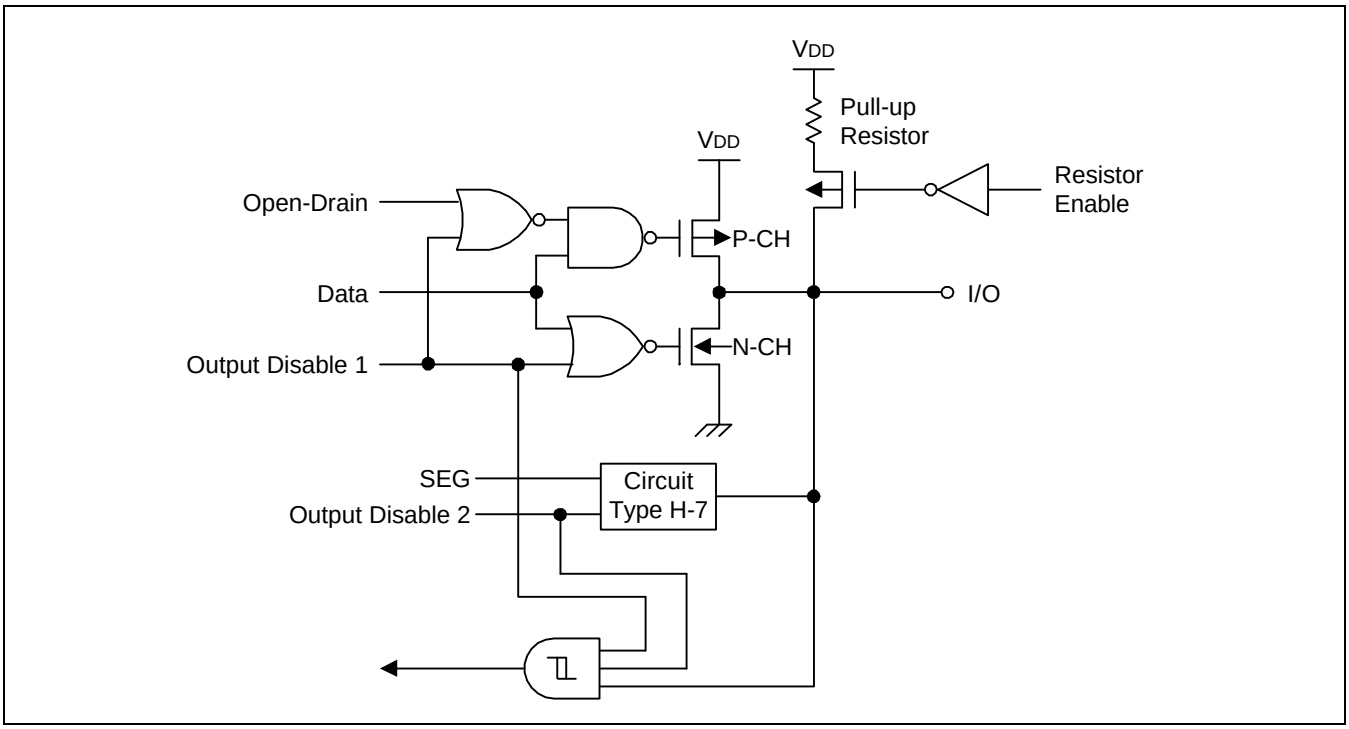


Figure 1-13. Pin Circuit Type H-8

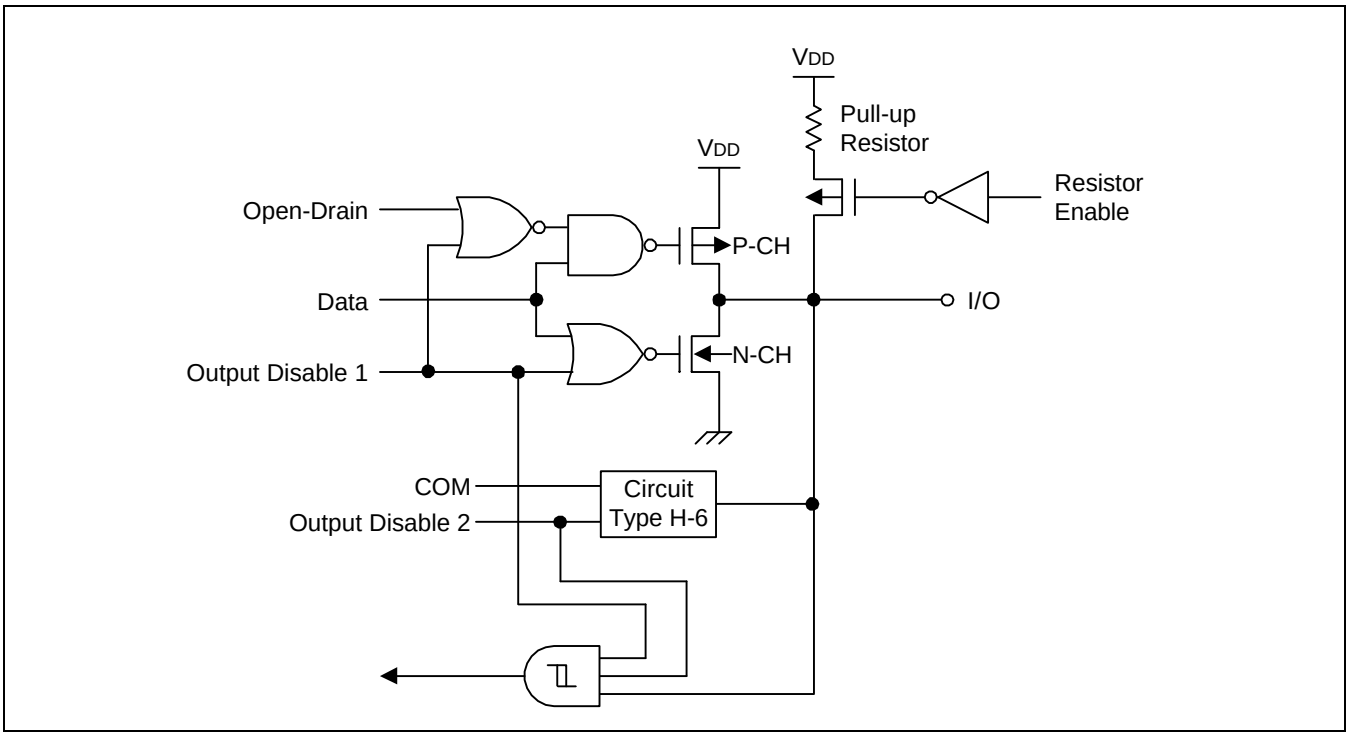


Figure 1-14. Pin Circuit Type H-9

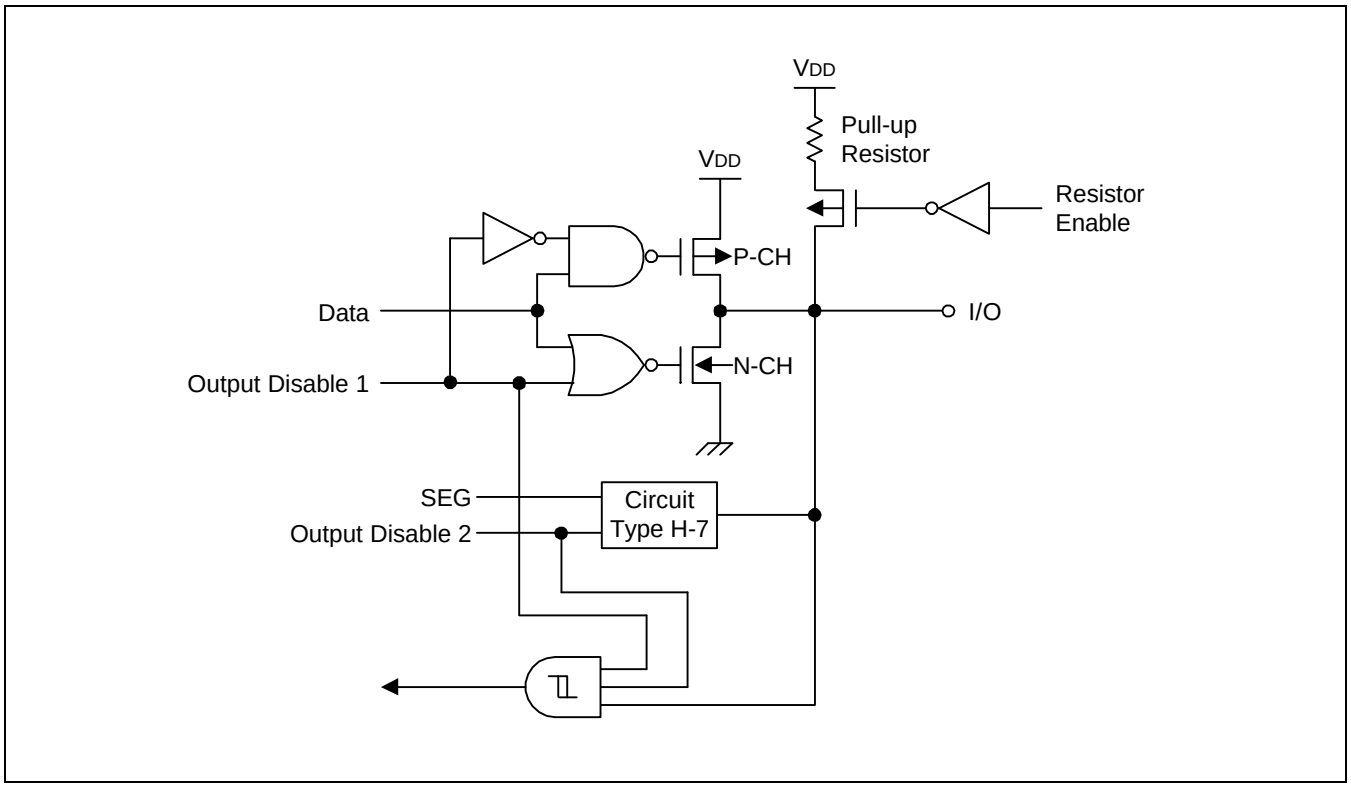


Figure 1-15. Pin Circuit Type H-10

17 ELECTRICAL DATA

OVERVIEW

In this chapter, S3C921F electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— D.C. electrical characteristics
— Data retention supply voltage in Stop mode
— Stop mode release timing when initiated by an external interrupt
— Stop mode release timing when initiated by a Reset
— I/O capacitance
— A.C. electrical characteristics
— Input timing for external interrupts (port 1)
— Input timing for RESET
— Oscillation characteristics
— Oscillation stabilization time

Table 17-1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input voltage	V_{IN}	Ports 1, 2, 3 and 4	– 0.3 to V_{DD} + 0.3	V
Output voltage	V_O	All output pins	– 0.3 to V_{DD} + 0.3	V
Output current High	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current Low	I_{OL}	One I/O pin active	+ 30 (Peak Value)	mA
		Total pin current for ports 1-4	+ 100 (Peak Value)	
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C

Table 17-2. D.C. Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.4 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	fx = 8MHz (Instruction clock = 2.0MHz)	4.5	–	5.5	V
		fx = 4MHz (Instruction clock = 1.0MHz)	2.7	–	5.5	
		fx = 3MHz (Instruction clock = 0.75MHz)	2.4	–	5.5	
Input High voltage	V_{IH1}	Ports 1-4	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	RESET	0.7 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT} and XT_{IN}	V_{DD} – 0.1		V_{DD}	
Input Low voltage	V_{IL1}	Ports 1-4	–	–	0.2 V_{DD}	V
	V_{IL2}	RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT} and XT_{IN}			0.1	
Output High voltage	V_{OH}	V_{DD} = 4.5 to 5.5 V; I_{OH} = –1 mA Ports 1-4	V_{DD} – 1.0	–	–	V
Output Low voltage	V_{OL}	V_{DD} = 4.5 to 5.5 V; I_{OL}= 10 mA Ports 1-4	–	–	2.0	V
		V_{DD} = 2.4 to 5.5 V; I_{OL}= 1.6 mA			0.4	
Input High leakage current	I_{LIH1}	V_I = V_{DD}; All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	V_I = V_{DD}; X_{IN}, X_{OUT}, XT_{IN}			20	
Input Low leakage current	I_{LIL1}	V_I = 0 V; All input pins except RESET, X_{IN}, X_{OUT}, XT_{IN}	–	–	–3	
	I_{LIL2}	V_I = 0 V; X_{IN}, X_{OUT}, XT_{IN}			–20	
Output High leakage current	I_{LOH}	V_O = V_{DD} All output pins	–	–	3	
Output Low leakage current	I_{LOL}	V_O = 0 V All output pins	–	–	–3	

Table 17-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40°C to + 85°C, V_{DD} = 2.4 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pull-Up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5V Ports 1-4	25	50	75	kΩ
		V_{DD} = 3V	50	100	150	
	R_{L2}	V_I = 0 V; V_{DD} = 5V; RESET	150	250	350	
		V_{DD} = 3V	250	500	750	
LCD Voltage Dividing Resistor	R_{LCD1}	T_A = + 25 °C When LCON.1 = "0"	38	54	70	kΩ
	R_{LCD2}	T_A = + 25 °C When LCON.1 = "1"	19	27	35	
$\lvert V_{LCD}\text{-COMi} \rvert$ Voltage Drop (i = 0-15)	V_{DC}	–15 uA per common pin	–	–	120	mV
$\lvert V_{LCD}\text{-SEGx} \rvert$ Voltage Drop (x = 0–63)	V_{DS}	–15 uA per common pin	–	–	120	
Middle Output Voltage (note)	V_{LC2}	V_{DD} = 2.4 V to 5.5 V, 1/5 bias LCD clock = 0Hz, V_{LC1} = V_{DD}	$0.8V_{DD}$–0.2	$0.8V_{DD}$	$0.8V_{DD}$+ 0.2	V
	V_{LC3}		$0.6V_{DD}$–0.2	$0.6V_{DD}$	$0.6V_{DD}$+ 0.2	
	V_{LC4}		$0.4V_{DD}$–0.2	$0.4V_{DD}$	$0.4V_{DD}$+ 0.2	
	V_{LC5}		$0.2V_{DD}$–0.2	$0.2V_{DD}$	$0.2V_{DD}$+ 0.2	

NOTE: It is middle output voltage when LCD controller/driver is 1/16 duty and 1/5 bias.

Table 17-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40°C to + 85°C, V_{DD} = 2.4 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Supply current (1)	I_{DD1}(2)	V_{DD} = 5 V ± 10% Crystal oscillator	8 MHz	–	5.0	10.0	mA
		C1 = C2 = 22pF	4.19 MHz		3.0	6.4	
		V_{DD} = 3 V ± 10%	4.0 MHz		1.4	2.8	
	I_{DD2}(2)	Idle mode V_{DD} = 5 V ± 10%	8 MHz	–	1.0	2.0	
		Crystal oscillator C1 = C2 = 22pF	4.19 MHz		0.8	1.6	
		V_{DD} = 3 V ± 10%	4 MHz		0.3	0.6	
	I_{DD3}(3)	V_{DD} = 3 V ± 10%, 32 kHz crystal oscillator		–	15	30	µA
	I_{DD4}(3)	Idle mode; V_{DD} = 3 V ± 10%, 32 kHz crystal oscillator		–	6	15	
	I_{DD5}	Stop mode; V_{DD}=5 V ± 10%,	OSCCON.2="1"	–	0.3	3	
		V_{DD}=3 V ± 10%,			0.1	1	

NOTES:

1. Supply current does not include current drawn through internal pull-up resistors, PWM, or external output current loads.
2. I_{DD1} and I_{DD2} include power consumption for sub clock oscillation.
3. I_{DD3} and I_{DD4} are current when main clock oscillation stops and the sub clock is used.
4. Every values in this table is measured when bits 4-3 of the system clock control register (CLKCON.4-.3) is set to 11B.

Table 17-3. Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	2.2	–	5.5	V
Data retention supply current	I_{DDDR}	Stop mode, V_{DDDR}=2.2 V	–	–	1	µA
Oscillator stabilization wait time	t_{WAIT}	Released by RESET	–	2^{16}/fx (1)	–	ms
		Released by interrupt	–	(2)	–	

NOTES:
1. fx is the main oscillator frequency.
2. The duration of the oscillation stabilization time (t_{WAIT}) when it is released by an interrupt is determined by the setting in the basic timer control register, BTCON.

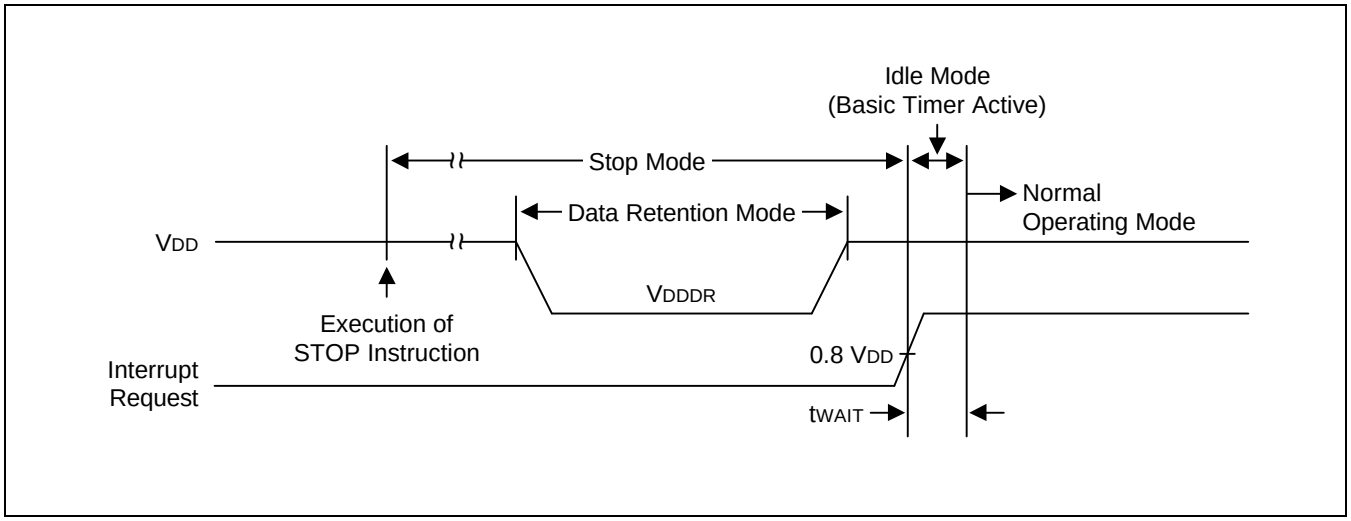


Figure 17-1. Stop Mode Release Timing When Initiated by an External Interrupt

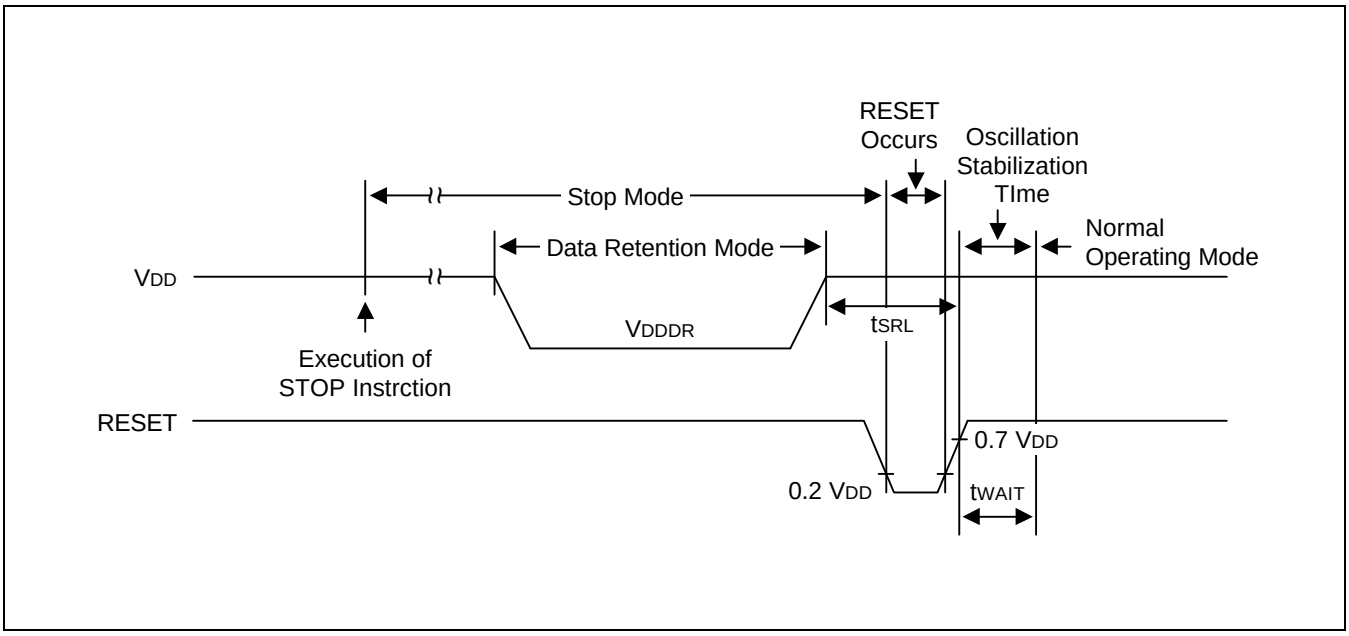


Figure 17-2. Stop Mode Release Timing When Initiated by a RESET

Table 17-4. Input/Output Capacitance

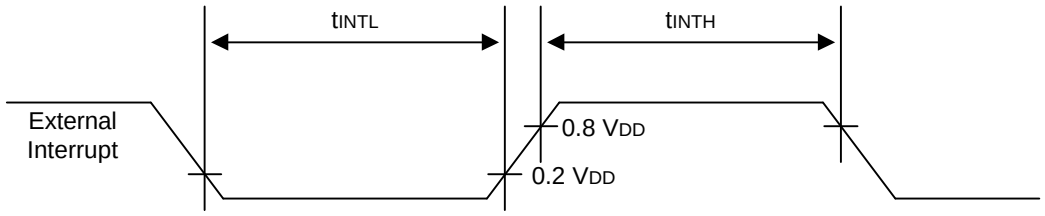
(T_A = – 40°C to + 85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 17-5. A.C. Electrical Characteristics

(T_A = – 40°C to + 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input, High, Low width	t_{INTH}, t_{INTL}	P1.0 – P1.7 V_{DD} = 5 V	150	200	–	ns
RESET input Low width	t_{RSL}	Input V_{DD} = 5 V	10	–	–	µs



NOTE: The unit tCPU means one CPU clock period.

Figure 17-3. Input Timing for External Interrupts (P1.0–P1.7)

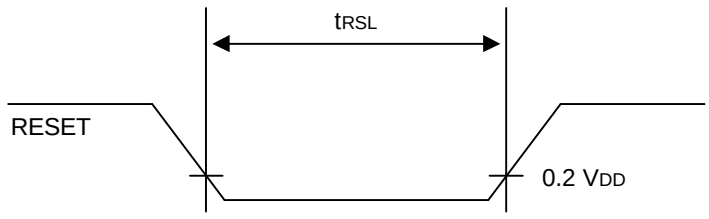
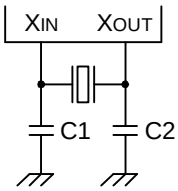
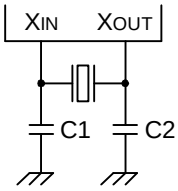
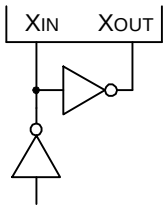
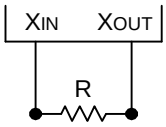


Figure 17-4. Input Timing for RESET

Table 17-6. Main Oscillation Characteristics

(T_A = – 40°C + 85°C)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency(1)	RC/X-tal = 0 V	0.4	–	8.0	MHz
		Stabilization time(2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
Crystal Oscillator		Oscillation frequency(1)	RC/X-tal = 0 V	0.4	–	8.0	MHz
		Stabilization time(2)	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
			V_{DD} = 1.8 V to 5.5 V	–	–	30	
External Clock		X_{IN} input frequency(1)	RC/X-tal = 0 V	0.4	–	8.0	MHz
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	62.0	–	1250	ns
RC Oscillator		Frequency(1)	V_{DD} = 2.7 V to 5.5 V RC/X-tal = V_{DD}	–	4	–	MHz
			V_{DD} = 2.4 V to 5.5 V RC/X-tal = V_{DD}	–	2	–	

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

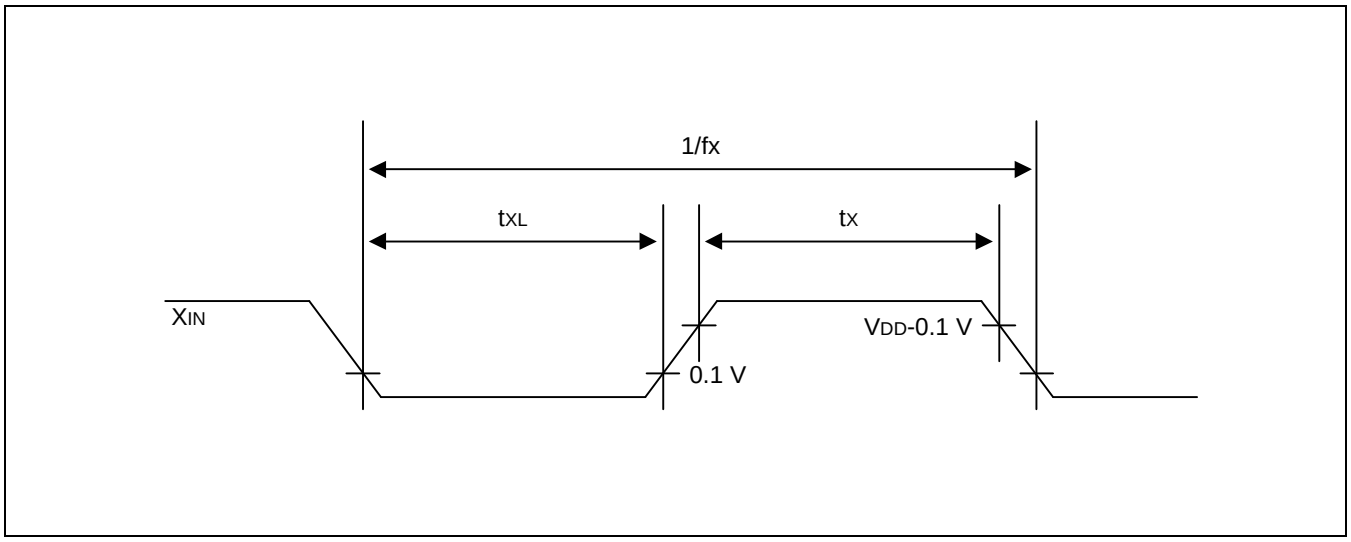
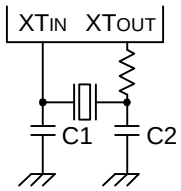
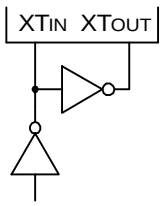


Figure 17-5. Clock Timing Measurement at X_{IN}

Table 17-7. Sub Oscillation Characteristics

(T_A = – 40°C + 85°C, V_{DD} = 2.4 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency(1)	–	32	32.768	35	kHz
		Stabilization time(2)	V_{DD} = 4.5 V to 5.5 V	–	1.0	2	s
			V_{DD} = 2.4 V to 4.5 V	–	–	10	
External Clock		XT_{IN} input frequency(1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	us

NOTES:
1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs .

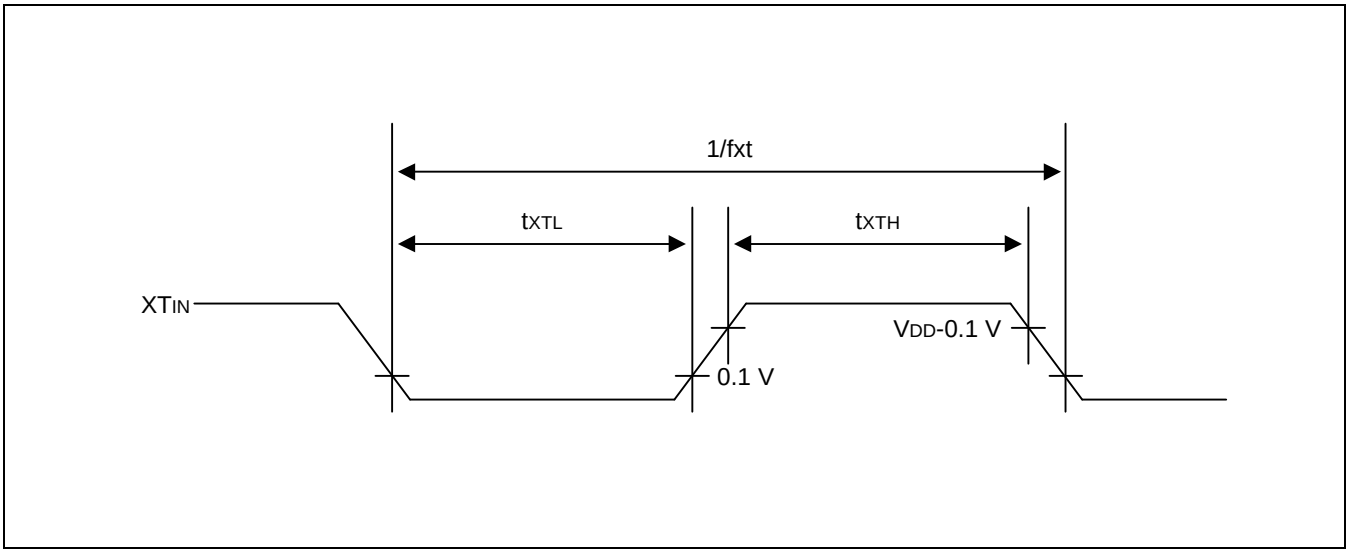


Figure 17-6. Clock Timing Measurement at XT_{IN}

Table 17-8. PWM0/PWM1 Electrical Characteristics

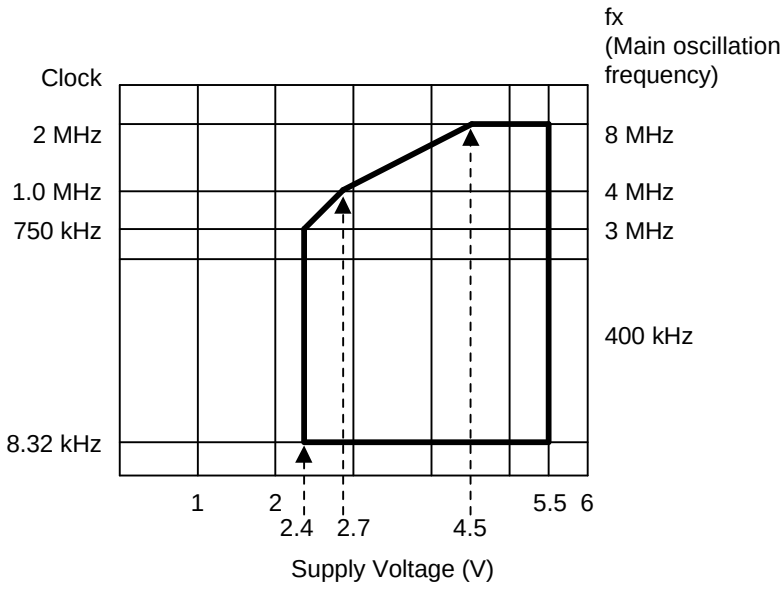
(T_A = – 40 °C + 85 °C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
PWM Output Voltage	V_{PWM0}	V_{DD} = 2.4 V	I_{PWMh0} = –8mA	V_{DD} – 0.5	–	–	V
			I_{PWMl0} = 15 mA	–		0.5	
	V_{PWM1}	V_{DD} = 2.4 V	I_{PWMh1} = –12mA	V_{DD} – 0.5		–	
			I_{PWMl1} = 20 mA	–		0.5	
	V_{PWM2}	V_{DD} = 2.4 V	I_{PWMh2} = –16mA	V_{DD} – 0.5		–	
			I_{PWMl2} = 25 mA	–		0.5	
	V_{PWM3}	V_{DD} = 2.4 V	I_{PWMh3} = –20mA	V_{DD} – 0.5		–	
			I_{PWMl3} = 30 mA	–		0.5	

Table 17-9. VLD Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.4 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VLD Voltage	V_{VLD}	BLDCON.4 = 0B	2.4	2.7	3.0	V
		BLDCON.4 = 1B	3.7	4.0	4.3	
VLD Circuit Response Time	TB	fw = 32.768 kHz	–	–	1.0	mS
VLD Operating Current	IBL		–	50	100	uA



Instruction Clock = 1/4n x oscillator frequency (n = 1, 2, 8, 16)

Figure 17-7. Operating Voltage Range

18 MECHANICAL DATA

OVERVIEW

The S3C921F microcontroller is currently available in a 100-pin QFP package.

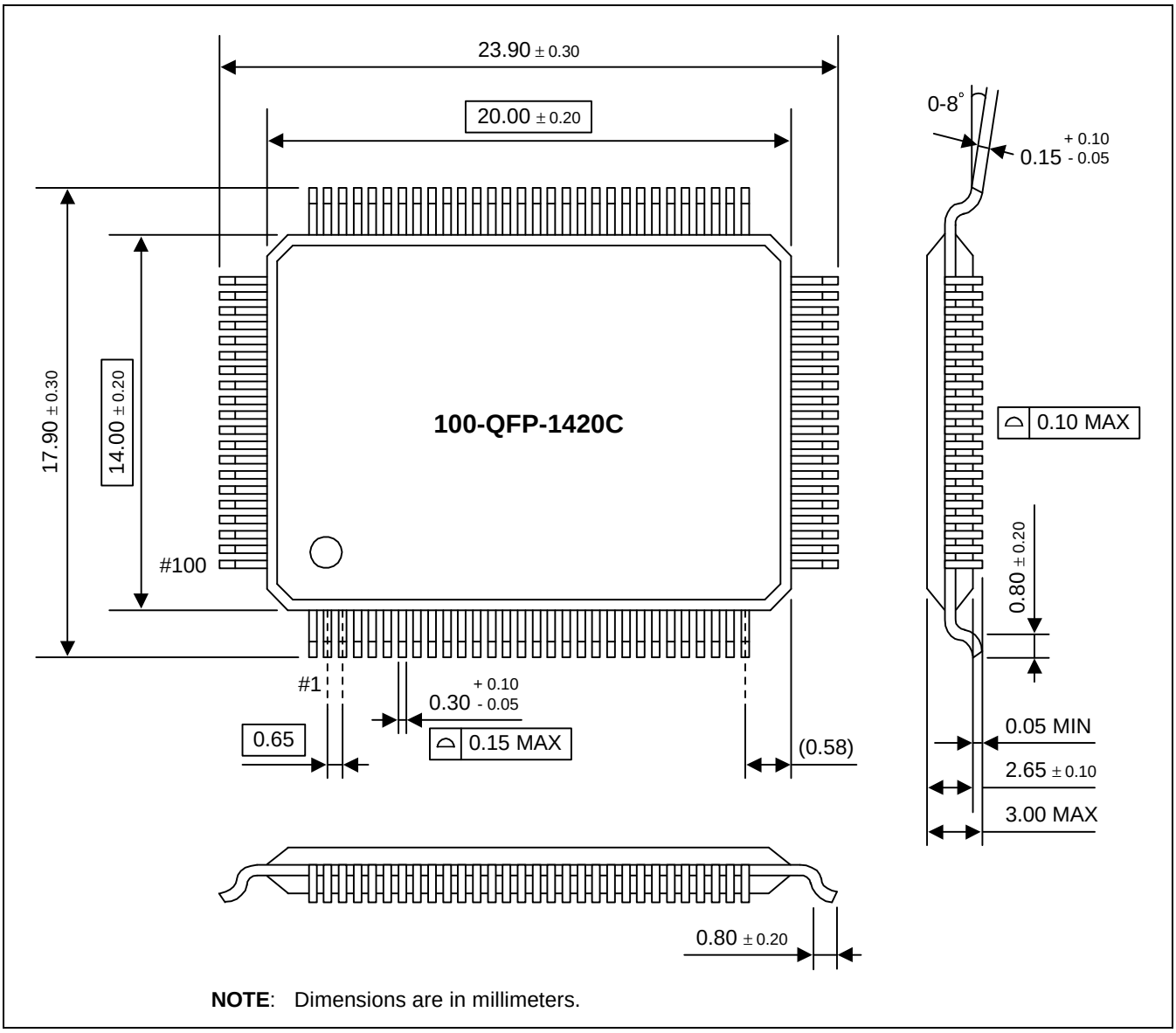


Figure 19-1. 100-QFP-1420C Package Dimensions

19 S3P921F OTP

OVERVIEW

The S3P921F single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C921F microcontroller. It has an on-chip OTP ROM instead of a masked ROM. The EPROM is accessed by serial data format.

The S3P921F is fully compatible with the S3C921F, both in function in D.C. electrical characteristics and in pin configuration. Because of its simple programming requirements, the S3P921F is ideal as an evaluation chip for the S3C921F.

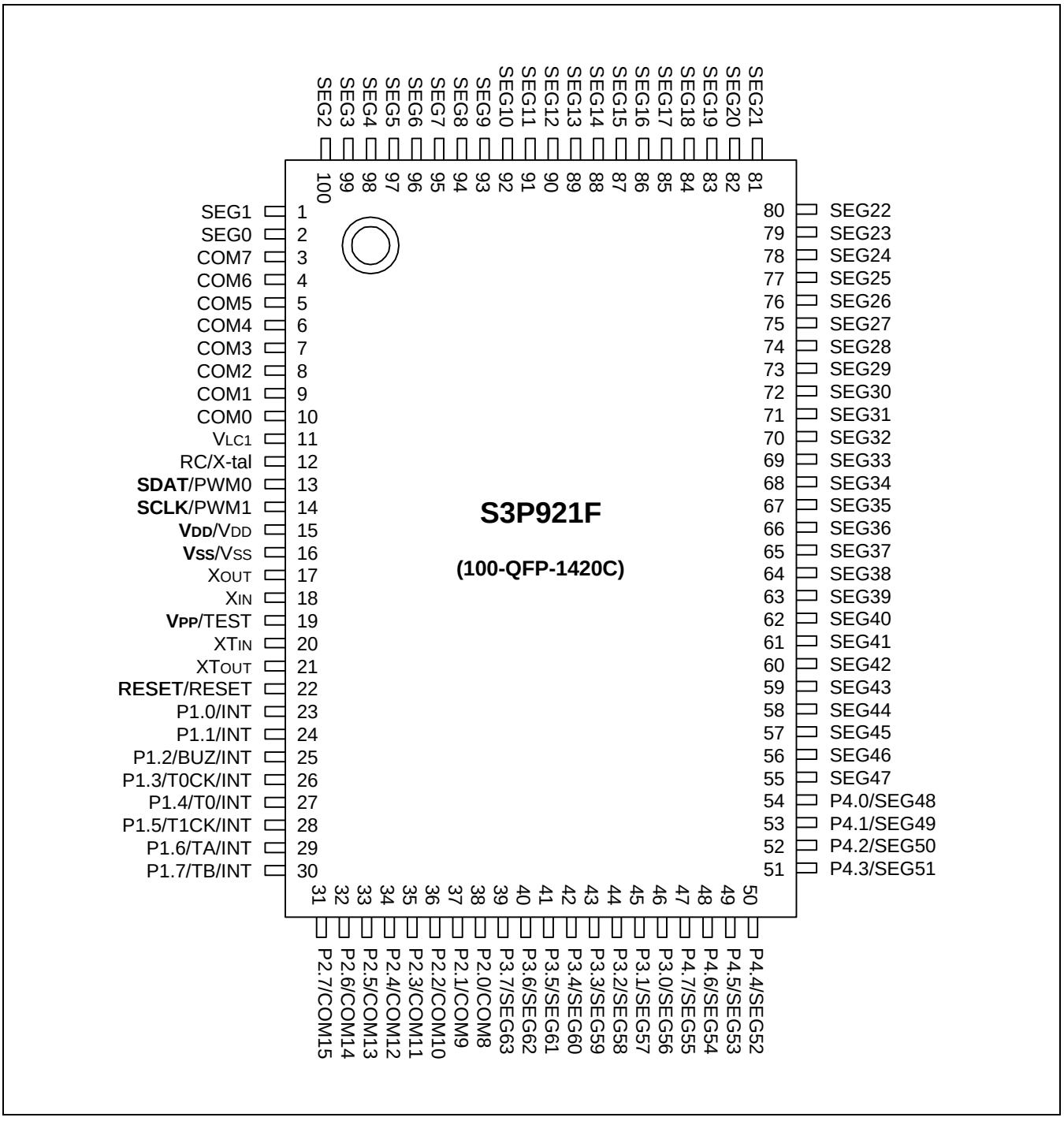


Figure 19-1. S3P921F Pin Assignments (100-Pin QFP Package)

Table 19-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
PWM0	SDAT	13	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
PWM1	SCLK	14	I	Serial clock pin. Input only pin.
TEST	V_{PP}	19	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	22	I	Chip Initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	15/16	–	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

Table 19-2. Comparison of S3P921F and S3C921F Features

Characteristic	S3P921F	S3C921F
Program Memory	64-Kbyte EPROM	64-Kbyte mask ROM
Data Memory	192-Kbyte EPROM	192-Kbyte mask ROM
Operating Voltage (V_{DD})	2.4 V to 5.5 V	2.4 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (EA) = 12.5 V	
Pin Configuration	100 QFP	100 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

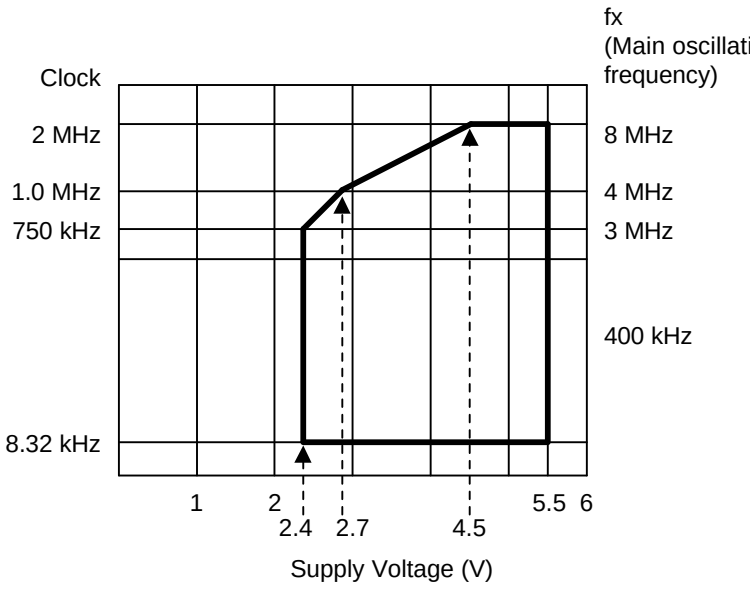
OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (EA) pin of the S3P921F, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 21-3 below.

Table 19-3. Operating Mode Selection Criteria

VDD	VPP (EA)	REG/ MEM	Address (A17–A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.



Instruction Clock = 1/4n x oscillator frequency (n = 1, 2, 8, 16)

Figure 19-2. Operating Voltage Range