SAMSUNG SDI

FOR MESSRS: DATE: February. 16. 2004

# THOMSON

## TENTATIVE SPECIFICATIONS

106cm (42 Inch) Wide Plasma Display Module

MODEL : **S42AX-XD02**

(PAL/NTSC)

* This specification will be approved by both **THOMSON** and Samsung SDI Co.,Ltd.
* Please return one of this specification with your signature for approval.

| Proposed by: | Approved by: |
|---|---|
| **Signature** | **Signature** |
| **General Manager. Yeon-Yong Choo** | **THOMSON** |
| Customer Quality Group, | |
| PDP Business Division, | |
| Samsung SDI Co., Ltd | |

## SAMSUNG SDI CO.,LTD.

CONFIDENTIAL

# Revision History

| Revision | Date | Description Of Changes | Approval |
|---|---|---|---|
| 1 | February. 16. 2004 | Newly established | - |
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## 1. DESCRIPTION

The S42AX-XD02 is a 42-inch wide full color plasma display Module with a resolution of 1,024(H) × 768(V) pixels. The display module includes the Plasma Display Panel(PDP), the Panel driving electronics, the Logic Control Board, and the SMPS(PSU) . PSU consists of two pieces of board (main supply & image board supply).

## 2. FEATURES

- Wide aspect ratio(16:9) 42 inch diagonal display screen. The display area is 933.89㎜ wide and 532.24㎜ high.
- Slim and light weight. The display Module is 64.1㎜(TBD) in depth and weight only approx.20.7㎏ including power supply.
- 16.77 million colors by combination of 8 bits R,G and B digital data
- High Luminance, High contrast, Wide viewing angle. The screen has a white peak Luminance of typical 1,000 cd/㎡, contrast of typical 3,000:1 and a viewing angle (of) greater than 160° comparable to those of CRTs.

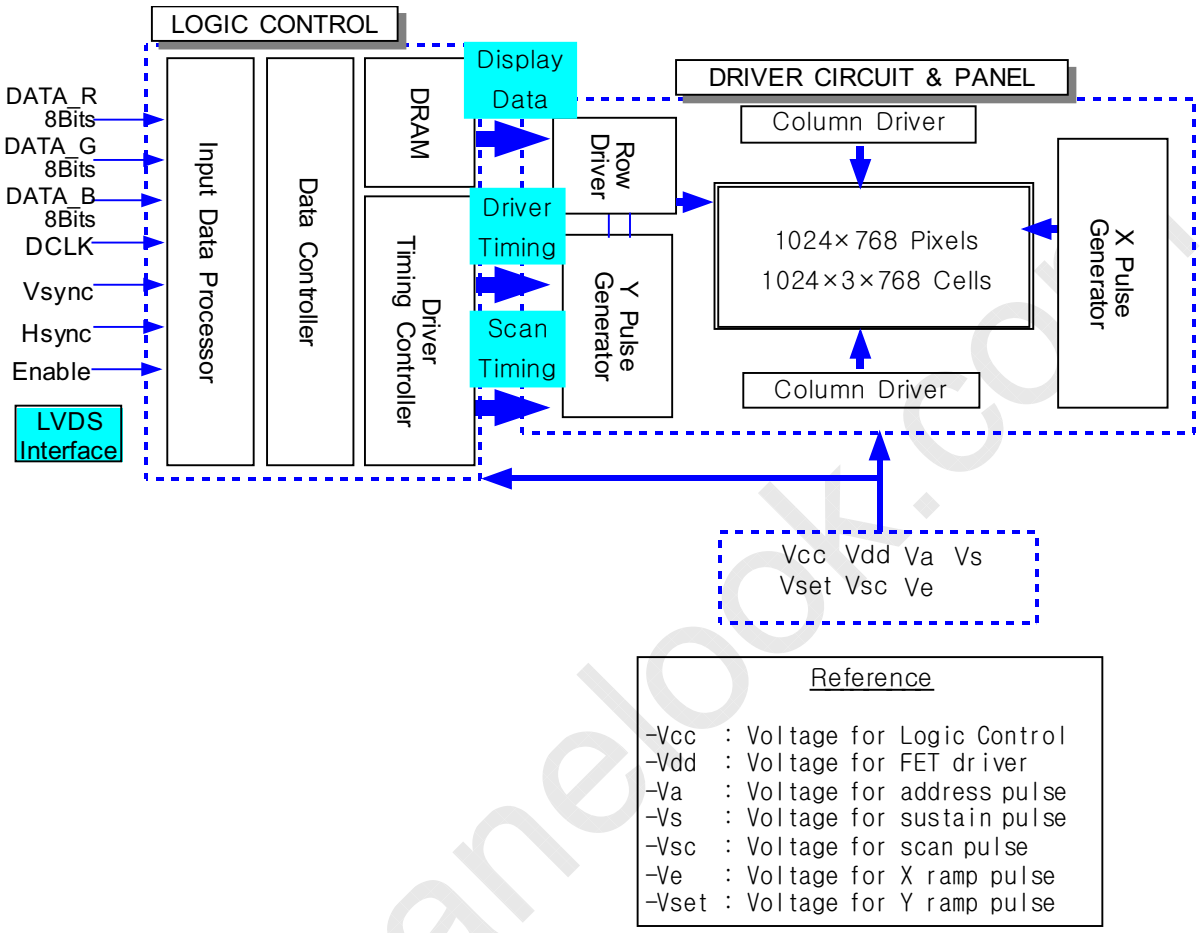
## 3. PRODUCT NAME AND MODEL NUMBER

- Product name : 42-inch Full Color Plasma Display Module3 (abbreviation : PDP Module3)
- Model number : S42AX-XD02

## 4. FUNCTION OUTLINE

- The plasma display Module has an APC(Automatic Power Control) function which restricts power consumption within the certain value with regard to each display load ratio.
- The plasma display Module is operated by following digital video signals; Vertical synchronous signal, Horizontal synchronous signal, Enable signal and 8bits data signal of each R,G, and B color. All signals are based on LVDS level.
- The plasma display Module is operated at 50Hz or 60Hz frame rate. An external frame rate conversion is required in order to display the other formats.
- The plasma display Module requires 8 types of input power voltages; voltage for LOGIC, voltage for COF driver IC, voltage for gate driver, voltage for sustain, erase, address, set and scan.
- The plasma display Module is operated at progressive signal only. An external progressive scan conversion is required in order to display the other formats.
- The plasma display Module requires rated 100~240V, 50~60Hz of input power voltage. Maximum input voltage rating is AC 90~264V.

## 5. BLOCK DIAGRAM



# 6. DISPLAY CHARACTERISTICS

## 6.1 Display Performance

| No | Item | Rating | |
|---|---|---|---|
| 1 | Display Pixels | Horizontal 1.024 × Vertical 768 pixels<br>(1 pixel = 1 R,G,B cells) | |
| 2 | Display Cells | Horizontal 3,072 × Vertical 768 cells | |
| 3 | Pixel Pitch | Horizontal 912㎛ × Vertical 693㎛ | |
| 4 | Cell Size | R | Horizontal 0.304㎛ × Vertical 693㎛ |
| | | G | Horizontal 0.304㎛ × Vertical 693㎛ |
| | | B | Horizontal 0.304㎛ × Vertical 693㎛ |
| 5 | Pixel Type | R, G, B Matrix (refer to Figure-2) | |
| 6 | Effective Display Size | Horizontal 933.89㎜ × Vertical 532.24㎜ | |
| 7 | Number of color | 16.77 million colors | |
| 8 | Peak Luminance *1 | typical 1,000cd/㎡ | |
| 9 | Contrast Ratio *2<br>(in dark room) | typical 3,000:1 | Calculated value Refer to note *2 |
| 10 | Color Coordinates<br>(Typical value) | White : X= 0.285±0.02 , Y= 0.290±0.02 | |
| 11 | Viewing Angle *3 | Over 160° | |

(Note)

* 1. Luminance and Color Coordinates are the values that were measured with 1% load ratio white pattern. The condition for measurement is shown in Figure-3.
* 2. Contrast Ratio is calculated from the display Luminance and the non-display Luminance value. Display condition is shown in Figure-4.
* 3. Viewing angle is a critical angle at which the Luminance is reduced to 50% to the Luminance perpendicular to the PDP Module. The Luminance is measured by a contact luminance meter CA-100(plus).

6.2 Display Cell Arrangement

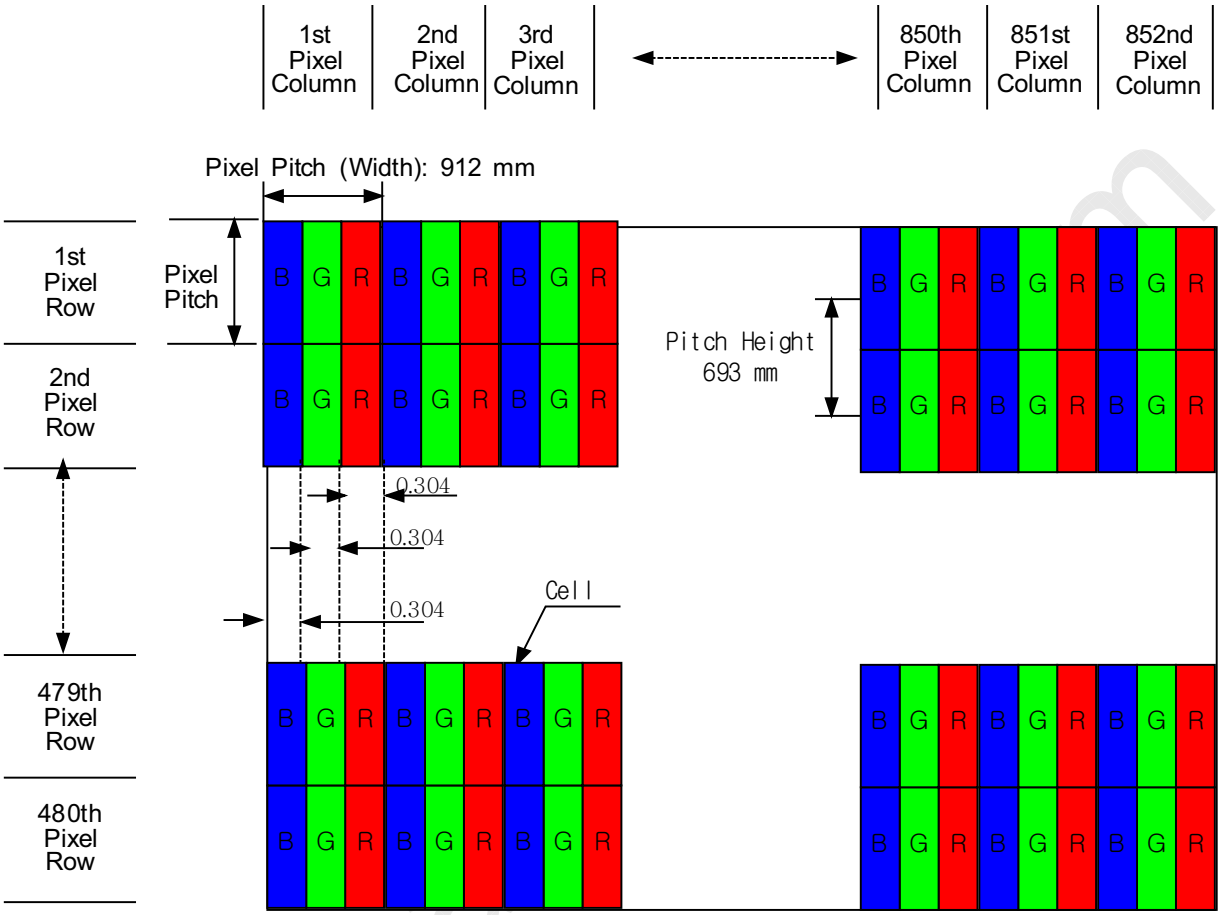



Figure-2. Display Cell Arrangement

6.3 Luminance Measurement Condition

(1) Display Pattern

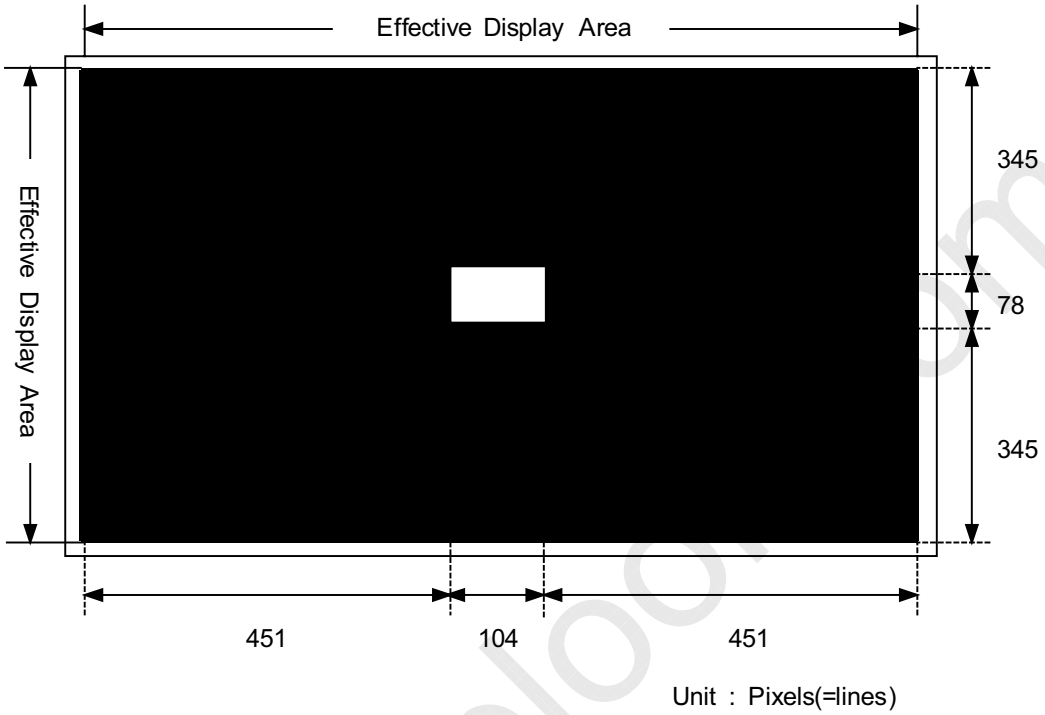



Figure-3. Display Pattern for Brightness & Contrast Ratio Measurement

(2) Display Area ratio : 1% white window

(3) Vsync : 16.7ms or 20ms

(4) Measuring equipment : MINOLTA CA-100

(5) Ambient Temperature : Room Temperature

(6) Ambient Luminance : Dark Room (<2 lux)

6.4 Contrast Measurement Condition

(1) Measuring point

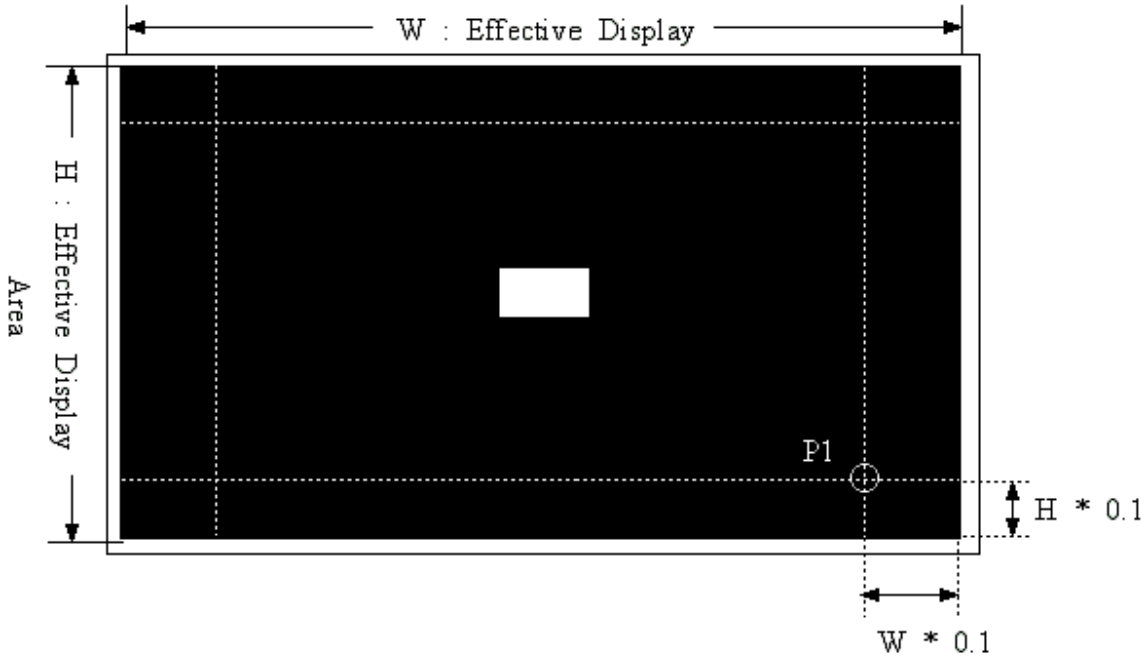



Figure-4. Measurement point

(2) Vsync : 16.7 ms or 20ms

(3) Measuring Equipment : MINOLTA CA-100(plus)
Pattern Generator(VG-828, LVDS Output).

(4) Contrast Calculation formula

$$\text{Contrast ratio} = \frac{\text{Luminance of 1\% white window Area at the center of the screen}}{\text{Luminance of Black Area *1}}$$

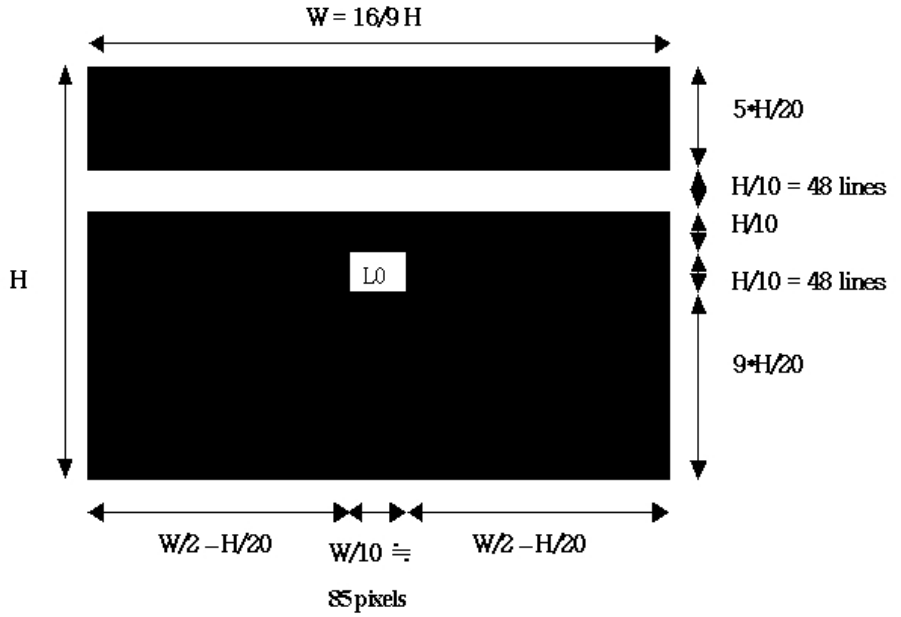
【 Note 】

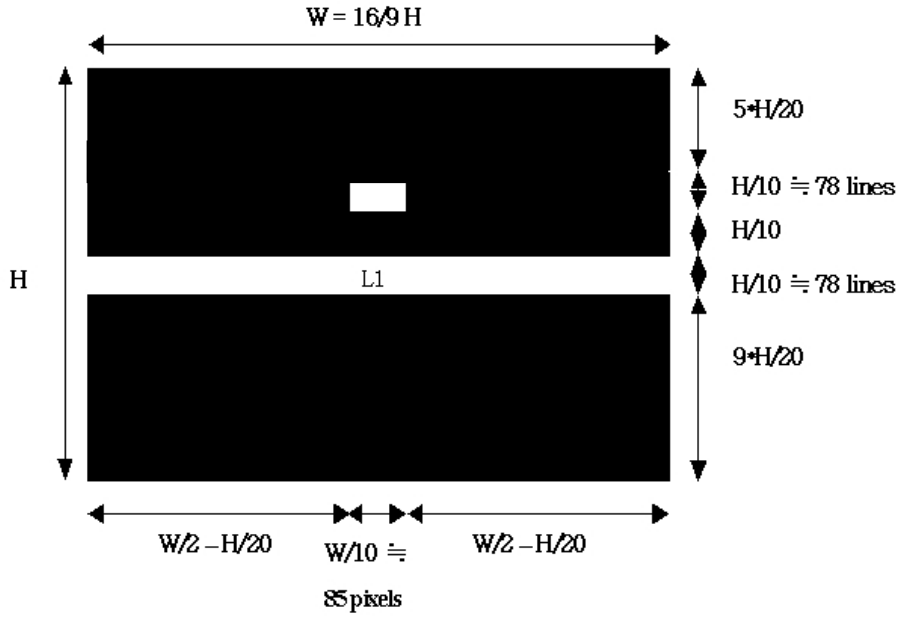
1. For mass production test purposes, it is recommended to measure just 1 point, P1 of Figure.-4 on display pattern of Fig.-3.

(5) Ambient Light : Dark Room (<2 lux)

6. 5 Image Streaking

(1) Measurement locations




(2) Image Streaking Calculation formula

Image Streaking [%] = 100 * (L0 – L1) / L0 ( ≤ 10% )

6.6 Display Cell Defect Specification (TBD)

In some cases, a panel may have defective cells that cannot be controlled.
These defective cells can be categorized into three types;
(1) Non-lighting cell defect : defect in which the cell is always off
(2) Non-extinguishing cell defect : defect in which the cell is always on.
(3) Flickering cell defect : defect in which the cell is flickering.
(4) High intensity cell defect : defect in which the cell is brighter than other cells
(5) Test Pattern : Full White, Full Red, Full Green and Full Blue with 255 gray level.

The display cell defect specifications define the allowed limits for display cell defects and are used as the criteria in determining whether a panel should be shipped.

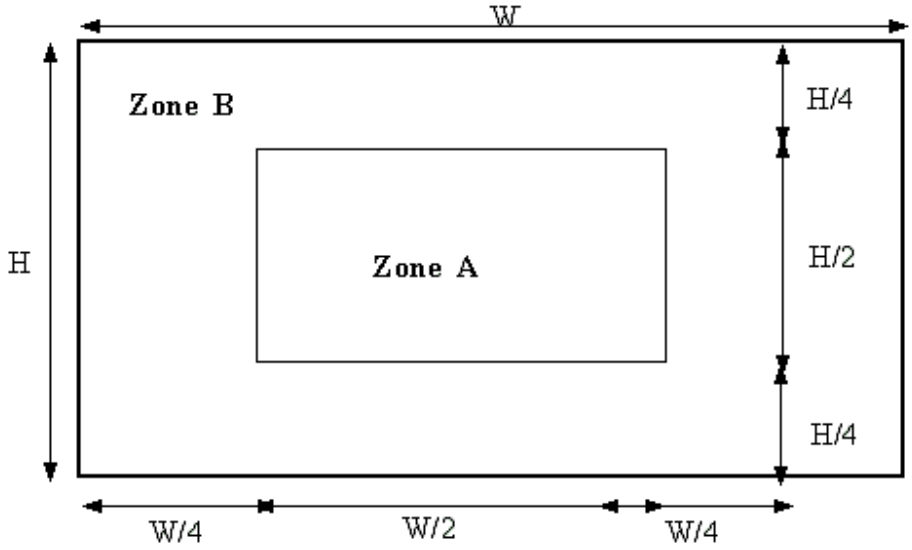



Figure-5. Measuring Area

| Item | Specification | |
|---|---|---|
| | Zone A | Zone B |
| Non-lighting cell defect | **4 and less** | **10 and less** |
| Non-extinguishing cell defect | **1 and less** | **3 and less** |
| Flickering cell defect | **1 and less** | **3 and less** |
| Continuous Cell Defect | **1 and less** | **2 and less** |
| **Total defect** | **Total number of cell defects in Zone A and B is less than 14** | |

6.7 **Luminance** Variation Specification

The color-PDP uses ultraviolet light produced by gas discharge to illuminate phosphor. Uneven phosphor coating and inconsistent discharge characteristics cause slight difference in Luminance among the sections in a panel.

| Item | Definition | Specification |
|---|---|---|
| Panel Speading | Full white luminance difference between panels | TBD |
| Full white Luminance variation | The Luminance is measured at 9 points (A1~A9 of Fig-6) on full white pattern. The full white Luminance variation as then calculated from the following equations. $\frac{Max - \bar{x}}{\bar{x}} \times 100\%$ & $\frac{\bar{x} - Min}{\bar{x}} \times 100\%$ | 10% and less |
| Chromaticity Variation | ABS(x(i)-x(average)) ABS(y(i)-y(average)) | 0.02 and less |

The Luminance variation specifications define the allowed limits for Luminance differences and are used as the criteria in determining whether a panel should be shipped.

【 Notes 】 There should be no noticeable/visible luminance and/or brightness variations observed from a distance of 3 times the screen height.

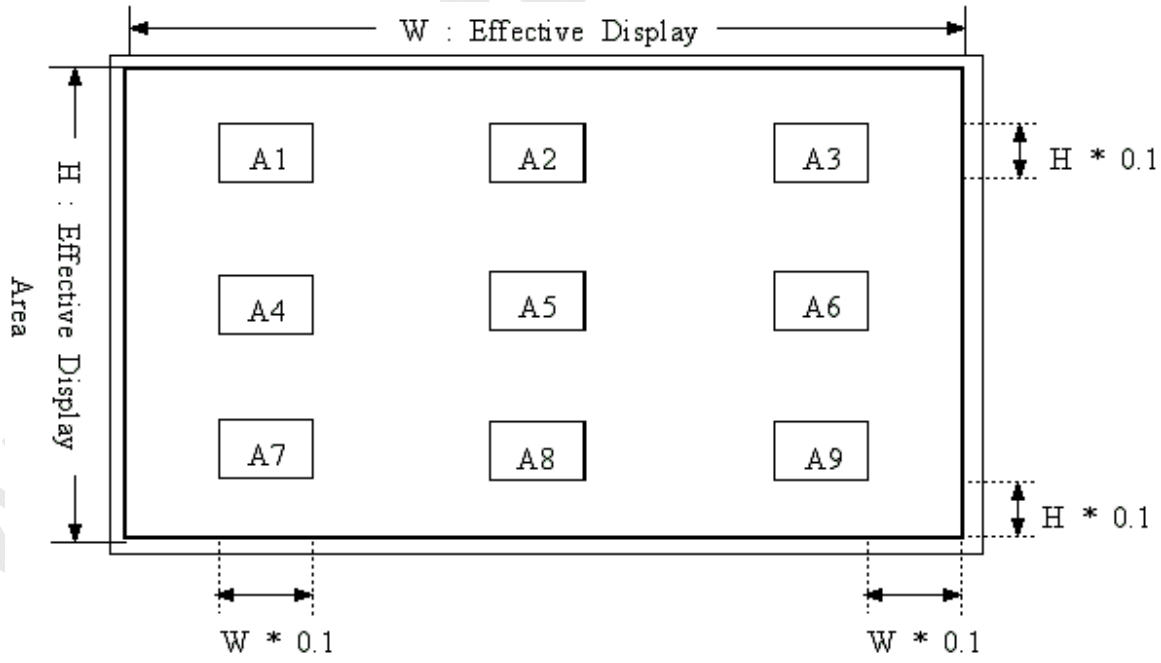



Figure-6. Measuring areas

6.8 Color Specification

The color-PDP displays a white color by mixing the lights produced by Red, Green, and Blue phosphor. This white color specification is defined by the following two categories based on chromaticity coordinates

| Items | Chromaticity Coordinates *1) | | Luminance (Minimum value) | Comments |
|---|---|---|---|---|
| | x | y | | |
| Low Light (20IRE) | 0.285 ±0.02 | 0.290 ±0.02 | To be included | W/B Pattern *1) |
| High Light (57IRE) | 0.285 ±0.02 | 0.290 ±0.02 | To be included | |

【 Notes 】

1. This specification is allowed among the PDP Modules.
   See Figure-7. Measuring points are T1(High Light) and T2(Low Light).
2. This specification is allowed in a PDP Module.
   It is measured at 9sections (A1~A9 of Figure-6) on a full white pattern
3. This specification is modifiable upon deliberation between **THOMSON** and SDI.

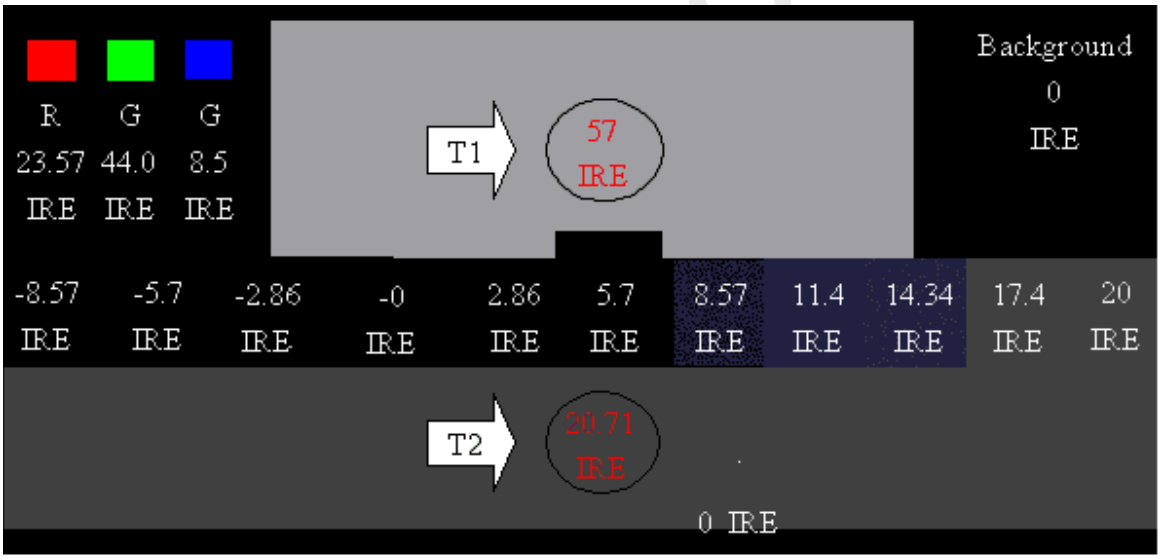



Figure-7. White Balance Tuning Pattern

6.9 Power consumption

(1) APC (Automatic Power Control) Function

The PDP has an APC (Automatic Power Control) function for the panel driver power source. If the total display load ratio exceeds approximately 11%, total power consumption will not exceed certain level. Measurement results below include gamma (=2.2) function.

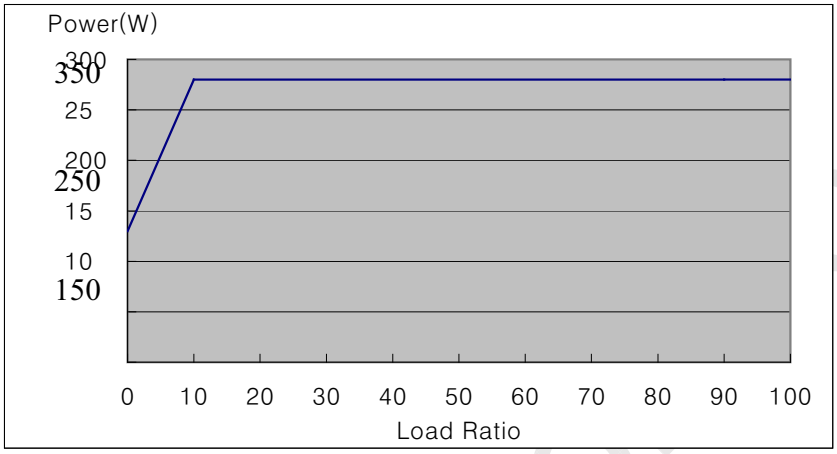


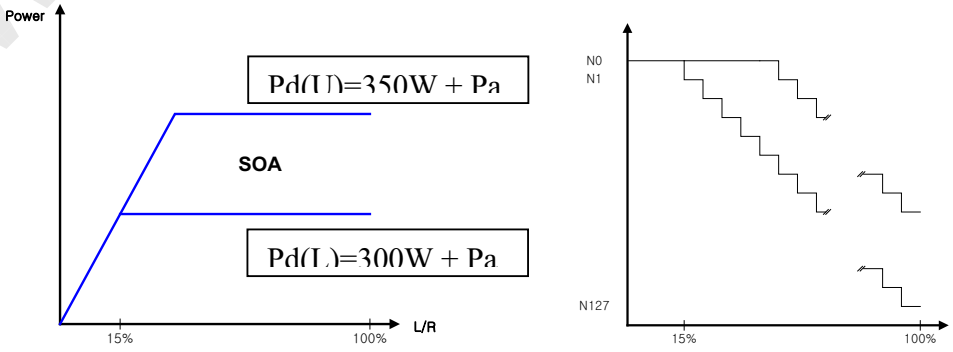

Figure-8. Display Load Ratio vs. power consumption

(2) Power consumption specification

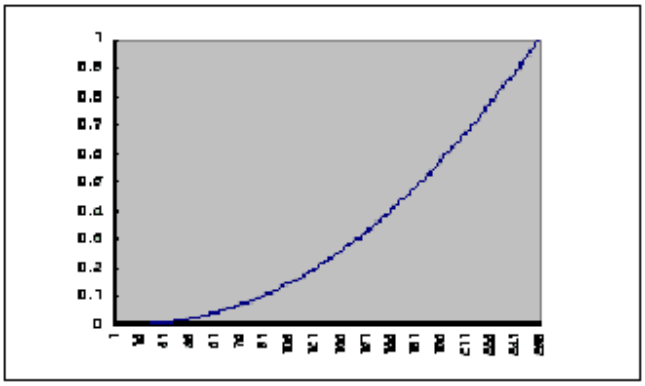
| Power consumption | Power sources |
|---|---|
| 330 + 10%W and less | AC 120V, 220V 60Hz |

【 Note 】

1. This is the case that the PDP Module includes SMPS made by Danam communications inc. (Model : 42SD-PH-REV**)
2. It is measured on a full screen white pattern.
3. PAL and NTSC are almost same for Power consumption.
4. APC Operation
   ① SDI uses slow varying sustain algorithm(called by slow APC). PDP doesn't work at Pd(L) but in SOA(Safe Operating Area). Regardless of input data, Power converges on lower boundary(see the picture below, Pa=address power).
   ② Transition Time(t) : They vary according to the Load Ratio(from UL to LL=15~5 step). It takes 0.25sec per every 1 level shift . For example, if the input data has the L/R of 100%, PDP converges on lower boundary within 1.25sec(=5*0.25).



6.10 Gamma characteristics

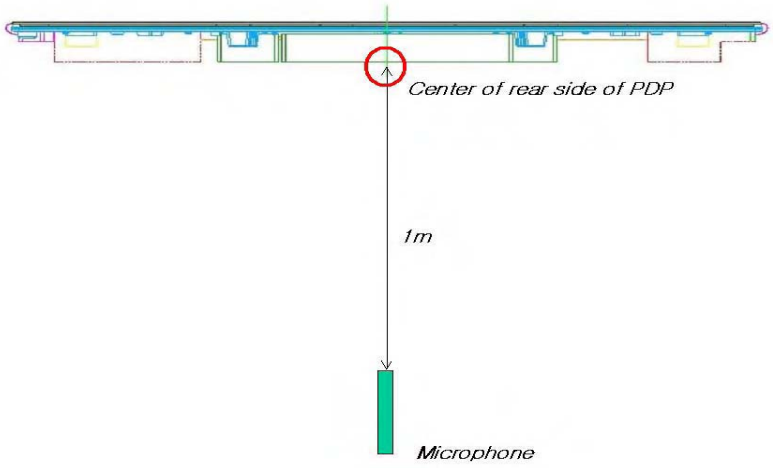


- This specification is modifiable after deliberation between **THOMSON** and SDI on the basis of 2.2 gain.

## 7. SOUND PRESSURE LEVEL SPECIFICATION

7.1 Measurement Condition

(1) Background Noise Level : less than 18dBA
(2) Measuring Pattern : Dynamic Images **(only, Full Black to Full White)**
(3) Measuring Equipment : Sound level meter Type 2827 made by B&K
(4) Measuring Distance : 1m from the rear side of PDP Module
(5) Measuring point




7.2 Sound Pressure Level : Typical 32dB

- Frequency Range : 50Hz ~ 8kHz
- Bandwidth : ⅓ Octave
- Weighting Filter : A-weighting network

【 Note 】

1. Sound Pressure Level is **the overall level** calculated from the individual band levels of 50Hz ~ 8kHz.
2. PSU must be included in this measurement.
3. Most noisy dynamic patterns are used in this measurement.

# 8. MECHANICAL CHARACTERISTICS

## 8.1 Mechanical Specifications

| No | Item | Rating |
|---|---|---|
| 1 | Outer Dimensions | Width 1000㎜ × Height 600㎜ × Thickness 64.1㎜ (include with FPC, COF) *see Appendix (Mechanical Dimensions Drawing) |
| 2 | Weight | Approx. 20.7 kg |

* Appendix A1 is included in section 12.1
* Appendix A2 is included in section 12.2.

## 8.2 Mechanical Characteristics

| No | Item | Rating |
|---|---|---|
| 1 | Vibration | Frequency : 10 to 55Hz<br>Sweep rate : 1 octave/min<br>Stroke : x,y direction : 0.35㎜<br>z-direction : 0.175㎜ |
| 2 | Shock | Acceleration : less than 20G (X,Y-direction)<br>less than 10G (Z-direction)<br>Duration : 11 ms |

* Notes: ( Test condition ) Non-Packaging, Operational
* Test time of Vibration Test is 30 minutes every direction(x,y,z)
* The number of times for shock test is 6 times every direction(x,y,z).

# 9. ENVIRONMENTAL CONDITIONS

## 9.1 Absolute Maximum Ratings

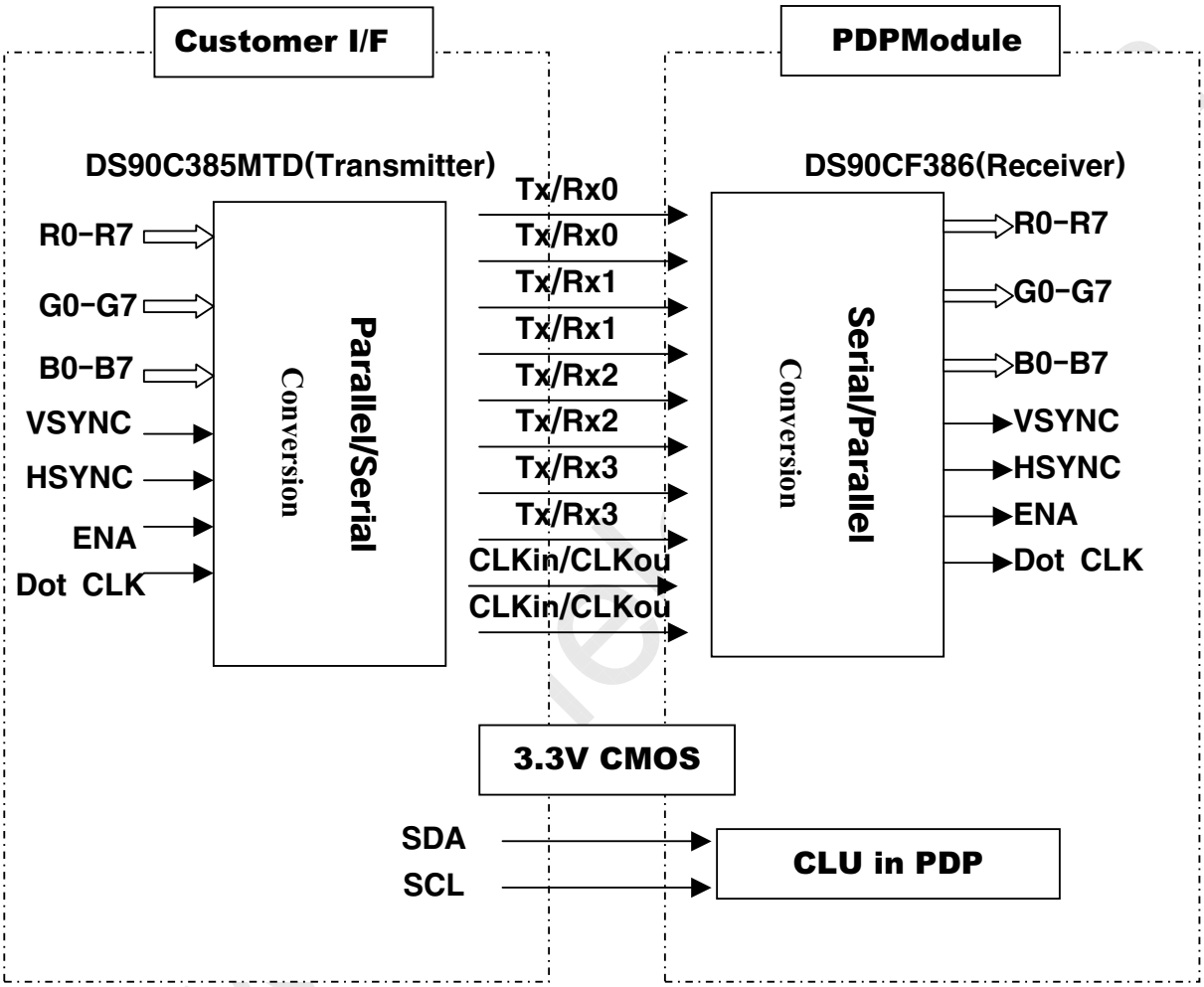
| No. | Item | Rating | |
|---|---|---|---|
| 1 | Temperature | Operational | -5 to 65℃ |
| | | Storage | -20 to 70℃ |
| 2 | Humidity | Operational | 5 to 90 % RH (no condensation) |
| | | Storage | 5 to 95 % RH (no condensation) |
| 3 | Pressure | Operational | 700 to 1114 hPa (0~3,000m) |
| | | Storage | 300 to 1114 hPa (0~9,000m) |

## 9.2 Recommended Environmental Condition

| No. | Item | Rating | |
|---|---|---|---|
| 1 | Temperature | Operational | 0 to 55℃ |
| | | Storage | -15 to 60℃ |
| 2 | Humidity | Operational | 20 to 85 % RH (no condensation) |
| | | Storage | 20 to 85 % RH (no condensation) |
| 3 | Pressure | Operational | 800 to 1114 hPa (0~2,000m) |
| | | Storage | 600 to 1114 hPa (0~4,500m) |

# 10. Interface Signal Specifications

10. 1. Configuration Context



10. 2. Interface Function Specifications (input data and display processing)

- 1,024-dot data signals are inputted to this product to display data.
- The Video signal and control signal input section uses a low voltage differential signaling (LVDS) interface.
- An I2C bus serial data interface is used for the communication between MPU of FTV side and the CLU (Control LOGIC Module) of this PDP Module.

10. 3. Input Signal Definition

| No | Item | Signal name | | Q | I/O | Method | Definition |
|---|---|---|---|---|---|---|---|
| 1 | Display Signal | Video Signal | RXIN0-<br>RXIN0+<br>RXIN1-<br>RXIN1+<br>RXIN2-<br>RXIN2+<br>RXIN3-<br>RXIN3+ | 1<br>1<br>1<br>1<br>1<br>1<br>1<br>1 | Input | LVDS Differentials | Differential serial data signal.<br>Input video and timing signals after differential serial conversation using a dedicated transceiver. The serial data signal is transmitted seven times faster than the base signal. |
| | | Dot Clock | RXCLKIN-<br>RXCLKIN+ | 1<br>1 | Input | LVDS Differential | Differential clock signal.<br>Input the clock signal after differential conversation using a dedicated transceiver. The clock signal is transmitted at the same speed as the base signal. |
| 2 | MPU Communication | Communication | SDA<br>SCL | 1<br>1 | Input | LVTTL (I2C) | I2C bus serial data communication signal. Communication with the CLU (Control Logic Module) of this product is enabled. |

10. 4. LVDS Signal Definition and Function

A video signal (display data signal and control signal) is converted from parallel data to serial data with the LVDS transmitter and further converted into four sets of differential signals before inputted to this PDP Module. These signals are transmitted seven times faster than the dot clock signals. The dot clock signal is converted into one set of differential signals.
The LVDS signal definitions and functions are as follows (in Italic)::

| Interface Signal Function | | | |
|---|---|---|---|
| **Symbol** | **I/O** | **Function** | **Remarks** |
| *RxIN0-* | I | Display Data Signal: R0, R1, R2, R3, R4, R5, G0 | LVDS signal |
| *RxIN0+* | I | | LVDS signal |
| *RxIN1-* | I | Display Data Signal: G1, G2, G3, G4, G5, B0, B1 | LVDS signal |
| *RxIN1+* | I | | LVDS signal |
| *RxIN2-* | I | Display Data Signal: B2, B3, B4, B5, Hsync, Vsync, BLANK | LVDS signal |
| *RxIN2+* | I | | LVDS signal |
| *RxIN3-* | I | Display Data Signal and Control Signal: R6, R7, G6, G7, B6, B7, PARITY | LVDS signal |
| *RxIN3+* | I | | LVDS signal |
| *RxCLKin-* | I | Dot Clock Signal: CLK | LVDS signal |
| *RxCLKin+* | I | | LVDS signal |
| SDA | I | I2C serial data | 3.3V CMOS |
| SCL | I | Clock signal for SDA | 3.3V CMOS |

10. 5. Video Signal Definition and Function

The table below indicates the definitions and functions of input video signals before LVDS conversion.

| Interfaces Signal Functions | | |
|---|---|---|
| **Symbol** | **Function** | **Remarks** |
| R7 to R0 | 8 bits red video signal (note 1) | Display data signal:<br>R7: MSB*, R0: LSB** |
| G7 to G0 | 8 bits green video signal (note 1) | Display data signal:<br>G7: MSB*, G0: LSB** |
| B7 to B0 | 8 bits blue video signal (note 1) | Display data signal:<br>B7: MSB*, B0: LSB** |
| HSYNC | Horizontal synchronous signal | This signal specifies the data period for one horizontal line. Control of the next line begins at the rising edge of Hsync. |
| VSYNC | Vertical synchronous signal | Timing signal that controls the start of the screen. Control of the next screen begins at the rising edge of Vsync. |
| Dot CLK | Clock for video signal | Latch the video signal at falling edge. |

* MSB: Most Significant Bit (Highest Intensity Bit)
**LSB: Least Significant Bit (Lowest Intensity Bit)
**Note 1**: The RGB signal may be compensated with Inverse γ circuit (E/D (=Error Diffusion) must be included) before inputted to the PDP Module. In order to obtain good characteristic of low level's gray scale, inverse γ correction and E/D process are advisory to be performed after inputted to the PDP Module.

10.6. Electrical Condition of Interface Signal

10.6. 1. Maximum Ratings

Common conditions : Ta = 25℃, Vcc = 3.3V

| Absolute Ratings | | | | | | |
|---|---|---|---|---|---|---|
| **Item** | | | **Parameter** | **Symbol** | **Ratings** | **Module** |
| Input Signals | LVDS | Rx0-/+,Rx1-/+, Rx2-/+,Rx3-/+, CLKin-/+ | Input Voltage | Vi | -0.3~3.6 | V |
| | | | Input Current | Ii | - | mA |
| | 3.3V CMOS | SDA, SCL, | Input Voltage | Vi | -0.3~3.6 | V |
| | | | Input Current | Ii | -15 | mA |

10. 6. 2. Electrical Characteristics

Common conditions : Ta =25℃, Vcc = 3.3V

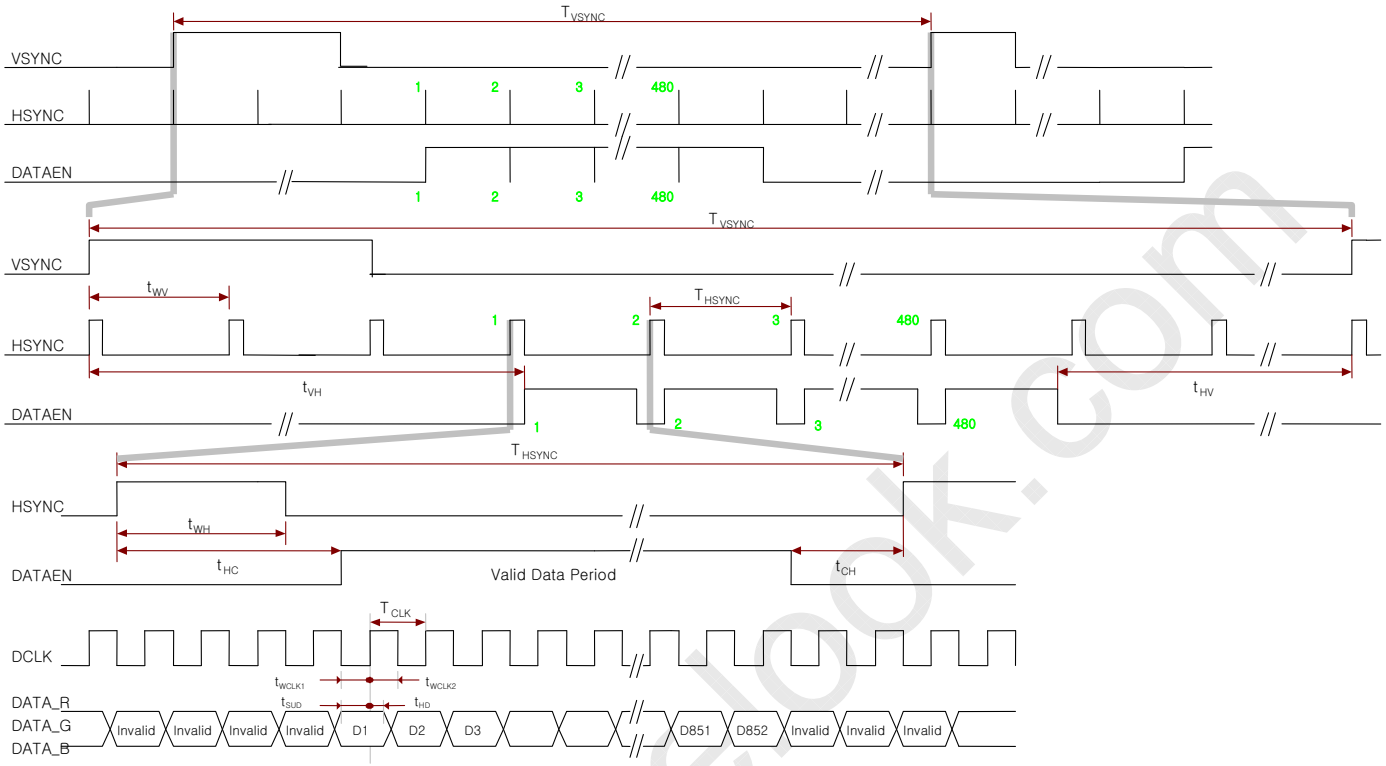
| Electrical Characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Signal** | **Item** | **Symbol** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Module** |
| LVDS | High level input voltage | $V_{th}$ | $V_{CM}$=1.2V | - | - | 100 | mV |
| | Low level input voltage | $V_{tl}$ | $V_{CM}$=1.2V | -100 | - | - | mV |
| | Input current | $I_{in}$ | $V_{IN}$=+2.4/GND | -10 | - | +10 | μA |
| I2C | Input Voltage | $V_{ih}$ | | 0.7*Vcc | - | Vcc+0.5 | V |
| | | $V_{il}$ | | -0.5 | - | 0.3*Vcc | V |
| | Input Capacitance | $V_{in}$ | - | - | - | 8 | pF |
| | Output Voltage | $V_{oh}$ | $I_{oh}$ = 8 mA | 2.4 | - | - | V |
| | | $V_{ol}$ | - | - | - | 0.4 | V |
| | Output Current | $I_{ol}$ | - | - | - | 10 | mA |
| 3.3V CMOS | High level input voltage | $V_{ih}$ | - | 2.0 | - | - | V |
| | Low level input voltage | $V_{il}$ | - | - | - | 0.8 | V |
| | Input current | $I_i$ | $V_I$=Vcc or GND | - | - | ±5.0 | μA |
| | High level output voltage | $V_{oh}$ | Io = -1 mA | 2.4 | - | - | V |
| | Low level output current | $V_{ol}$ | $I_o$ = 1 mA | - | - | 0.4 | V |

10. 7. Video Signal Interface Timing Conditions

The table below indicates the conditions of input video signal before LVDS conversion. These conditions must be satisfied. Refer to the figure of the timing chart.

| Video Input Signal Timing (NTSC/PAL) | | | |
|---|---|---|---|
| **Symbol** | **Timing** | **Unit** | **Remarks** |
| Tvsync | Refer to 'Remark' | Hz | - PAL Normal Mode: 30 ~ 52<br>- PAL FF Mode: 52 ~ 53<br>- NTSC Normal Mode: 53 ~ 62<br>- NTSC FF Mode: 62 ~ 63<br>- NTSC Mask Mode: 63↑<br>* FF Mode<br>☞ Reduction of luminance makes image darker than usual case.<br>* Mask Mode<br>☞ Disregard of Vsync which is over than 63Hz. But image is still working on PDP module in this case because one of two unstable Vsync is recognized as effective Vsync for normal image data processing in PDP module.<br>* V total = 820 H(NT) / 984(PAL) |
| Twv | 6 | H | |
| Tvh | 16 | H | * Tvh = Twv + V Back Porch |
| Thv | - | H | Don't Care<br>* Thv = V total – Tvh – 768H |
| Thsync | - | DCLK | * H total = 1,504 DCLK |
| Twh | 22 | DCLK | |
| Thc | 70 | DCLK | * Thc = Twh + H Back Porch |
| Tch | - | DCLK | Don't Care<br>* Tch = H total – Thc – 1,024DCLKs |
| Tclk | 74 | MHz | Recommended range is 54~76MHz. |
| Tsud | 5 | ns | 2ns as minimum |
| Thd | 5 | ns | 2ns as minimum |

## Video Input Signal Timing Chart



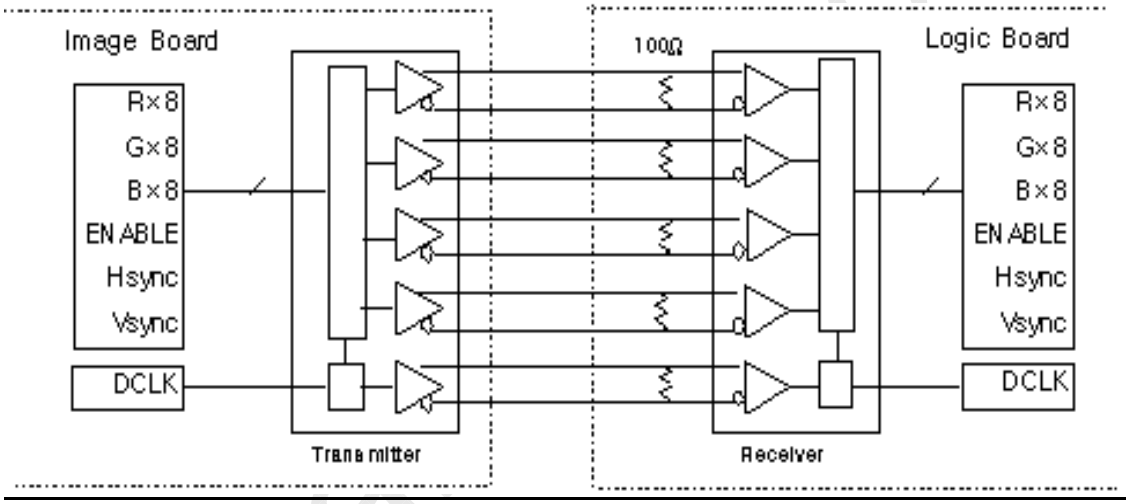
10. 8. LVDS Interface Timing Conditions

This PDP Module uses an LVDS interface for the signal input. For details of the input signal timing conditions, refer to the data sheets prepared by the LVDS transmitter IC maker. This PDP Module uses National Semiconductor's DS90CF386.

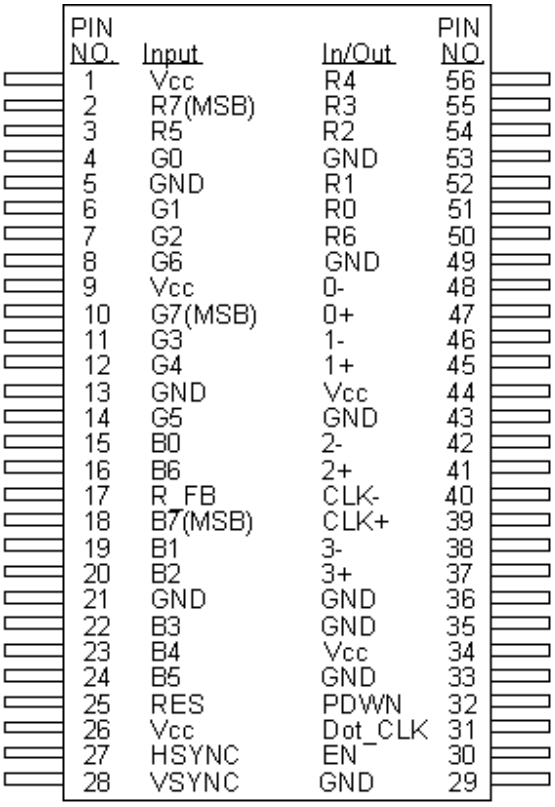
10. 9. LVDS Connection Specifications

The following Figure shows the connection specifications and signal assignments of the LVDS interface IC. Do not connect or disconnect the connector when the system power in on. Otherwise, the LVDS interface IC could be damaged.

**LVDS Interface Connection**



## LVDS Transmitter Pin Assignment



| PIN NO. | Input | In/Out | PIN NO. |
|---|---|---|---|
| 1 | Vcc | R4 | 56 |
| 2 | R7(MSB) | R3 | 55 |
| 3 | R5 | R2 | 54 |
| 4 | G0 | GND | 53 |
| 5 | GND | R1 | 52 |
| 6 | G1 | R0 | 51 |
| 7 | G2 | R6 | 50 |
| 8 | G6 | GND | 49 |
| 9 | Vcc | 0- | 48 |
| 10 | G7(MSB) | 0+ | 47 |
| 11 | G3 | 1- | 46 |
| 12 | G4 | 1+ | 45 |
| 13 | GND | Vcc | 44 |
| 14 | G5 | GND | 43 |
| 15 | B0 | 2- | 42 |
| 16 | B6 | 2+ | 41 |
| 17 | R_FB | CLK- | 40 |
| 18 | B7(MSB) | CLK+ | 39 |
| 19 | B1 | 3- | 38 |
| 20 | B2 | 3+ | 37 |
| 21 | GND | GND | 36 |
| 22 | B3 | GND | 35 |
| 23 | B4 | Vcc | 34 |
| 24 | B5 | GND | 33 |
| 25 | RES | PDWN | 32 |
| 26 | Vcc | Dot_CLK | 31 |
| 27 | HSYNC | EN | 30 |
| 28 | VSYNC | GND | 29 |

**DS90C385T**

## 10. 10. I2C Interface Conditions

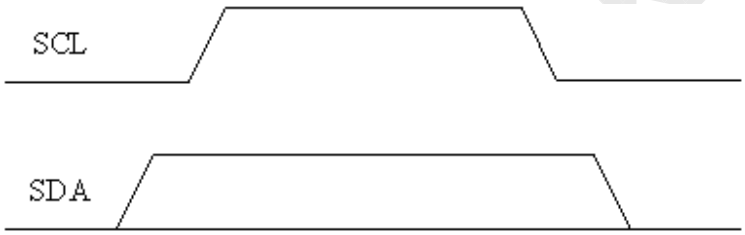
### 10. 10. 1. Basic Specifications

This PDP Module has the I2C bus serial data communication function.
The customer may use this function to make settings for PDP Module characteristics of several items.

| No | Parameter | Specifications |
|---|---|---|
| 1 | Transfer Rate | 100 kbps |
| 2 | Device Status | Slave Receiver |
| 3 | Slave Address | CC(Write), CD(Read) |

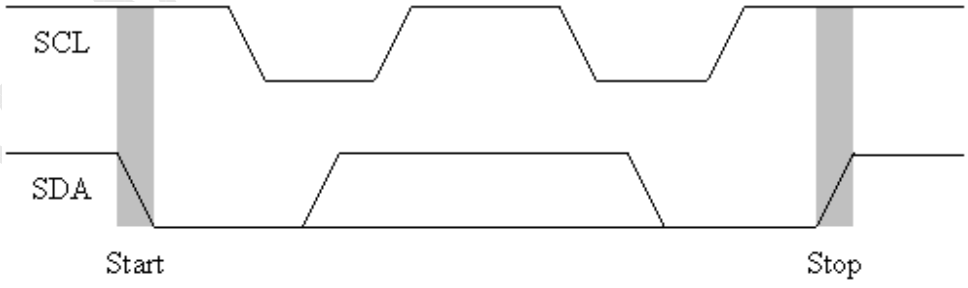
### 10. 10. 2. Data Validity

Amount of data that is transferred is 1-Bit per 1 SCL cycle. Data is valid when SCL is high and recognized as to state of SDA.



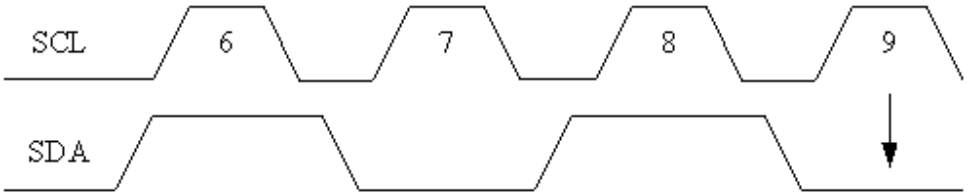

### 10. 10. 3. Start & Stop Condition

Start /Stop condition is generated by Master (=Image B'D). Before start condition or after stop condition, a SDA cannot be recognized as valid data.
Start condition ☞ SCL high & SDA transition from H to L
Stop condition ☞ SCL high & SDA transition from L to H



10. 10. 4. Acknowledge

When Master (=Image B'D ( )) needs to stop reading data, the master should give NO ACK signal to salve by SDA. Slave (=PDP Module) gives ACK whenever 8-bit transfer is done.




10. 10. 5. 7-Bit Addressing for Device address(with example of **CC or CD**)

Master could choose slave by 7-bit slave address and decide what procedure is by R/W bit (H=Read procedure, L=Write procedure).

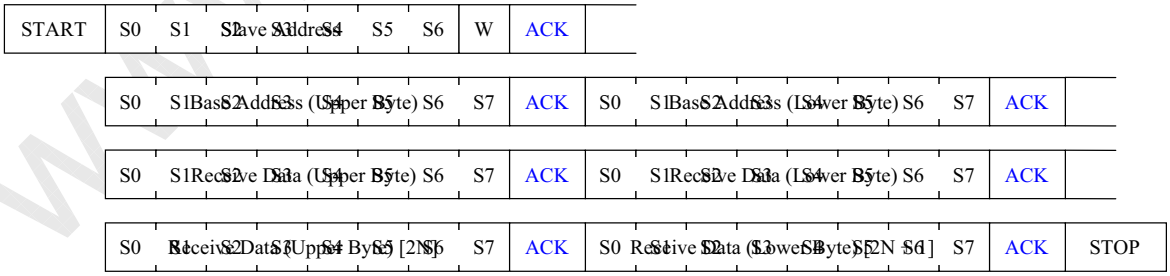
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **1** | **1** | **0** | **0** | **1** | **1** | **0** | R/W | ACK |

10. 10. 6. 16-Bit Mode

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

10. 10. 7. Data Transfer Sequence (Write)

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').
**Note 1**: Black letters mean master (=Image B'D)'s bus occupation.
**Note 2**: Blue letters mean slave (=PDP Module)'s bus occupation.



10.10. 8. Data Transfer Sequence (Read)

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

**Note 1**: In advance, master should initialize writing sequence by giving base address and stop condition.

**Note 2**: After start condition and slave addressing, master could receive data from slave.

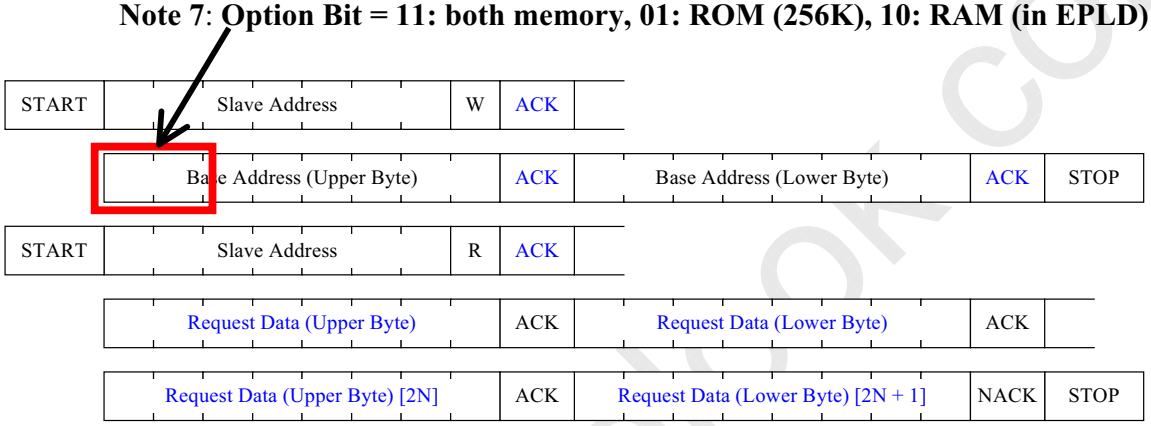
**Note 3**: Master should give acknowledge whenever 8-bit data is received.

**Note 4**: 'No acknowledge' could make master give stop condition on bus. Therefore, NACK is used for master to stop receiving data from slave.

**Note 5**: Black letters mean master (=Image B'D ( ))'s bus occupation.

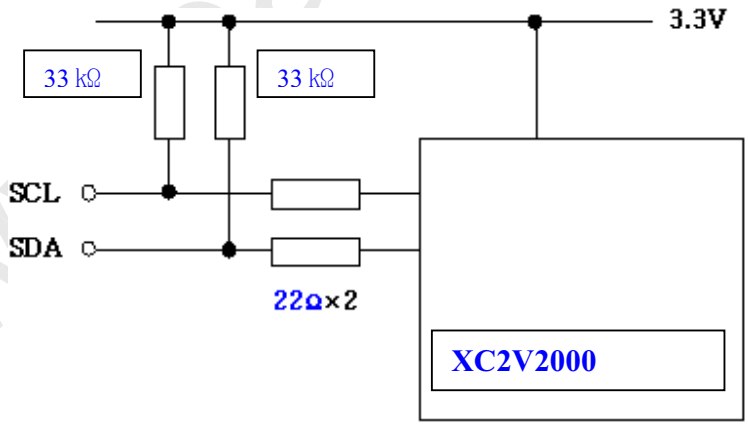
**Note 6**: Blue letters mean slave (=PDP Module)'s bus occupation.

**Note 7**: **Option Bit = 11: both memory, 01: ROM (256K), 10: RAM (in EPLD)**



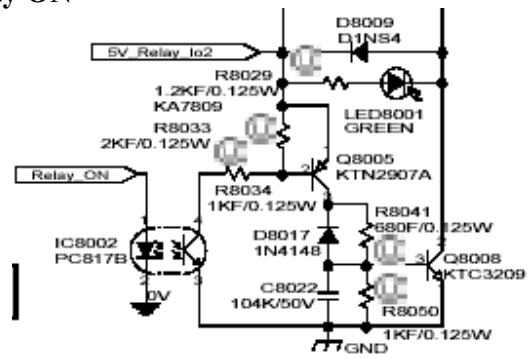

10. 10. 9. Interface Circuit

(1) This PDP Module uses EPLD EP20K400EBC652-1 of ALTERA. For the electric characteristics, refer to the data sheet that is issued by ALTERA Co.ltd.

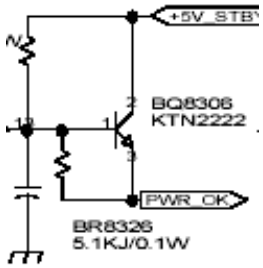


(2) Power OK & STAND_BY signals are used to make power_up sequence.
Please refer to following diagram to make PDP start operation stable & rightful.

*** Relay ON**



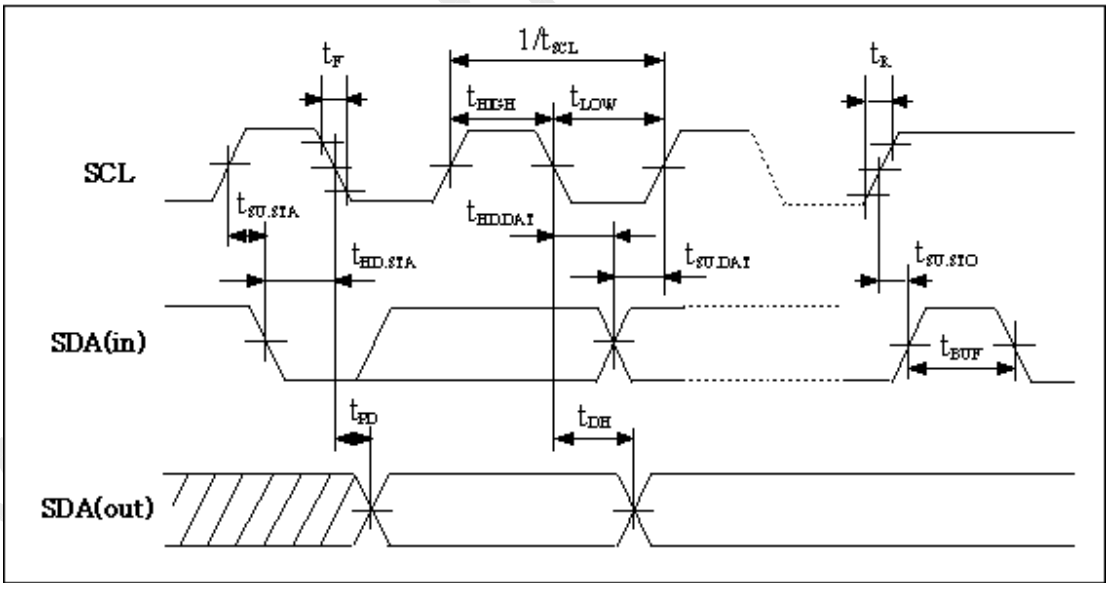

*** Relay ON**



10. 10. 10. I2C Bus Timing Specifications

* Refer to the following data merely as sample data.

| No | Item | Symbol | Standard | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Module |
| 1 | SCL Input Frequency | $f_{SCL}$ | - | 50 | 200 | kHz |
| 2 | SCL Input "HIGH" Period | $t_{HIGH}$ | 0.3 | - | - | μs |
| 3 | SCL Input "Low" Period | $t_{LOW}$ | 0.5 | - | - | μs |
| 4 | Start Condition Set Up Time | $t_{SU.STA}$ | 0.3 | - | - | μs |
| 5 | Start Condition Hold Time | $t_{HD.STA}$ | 0.3 | - | - | μs |
| 6 | Data Input Set Up Time | $t_{SU.DAT}$ | 0.1 | - | - | μs |
| 7 | Data Input Hold Time | $t_{HD.DAT}$ | 0 | - | - | μs |
| 8 | Stop Condition Set Up Time | $t_{SU.STO}$ | 0.3 | - | - | μs |
| 9 | Data Output Delay Time | $t_{PD}$ | 0.1 | - | - | μs |
| 10 | Data Output Hold Time | $t_{DH}$ | 0.1 | - | - | μs |
| 11 | SDA Bus Free Time | $t_{BUF}$ | 0.5 | - | - | μs |
| 12 | SCL, SDA Input Rising Time | $t_R$ | - | - | 0.8 | μs |
| 13 | SCL, SDA Input Falling Time | $t_F$ | - | - | 0.3 | μs |
| 14 | SCL, SDA Line Capacitor | $C_b$ | - | - | 400 | pF |



10. 10. 11. Address Map

The address map is shown below. It could be changed in the next version. Always refer to 'address Map Version'. There are two regions of address map and one is for NTSC and the other is for PAL. Sub address that is shown below is for NTSC. Sub address region for PAL is 2000h~3FFFh. Basically address map for PAL is same as NTSC's beside sub address. For example, 0080h for NTSC is correspondent to 2080h for PAL. Specially region of 0000h~007Fh is used commonly for NTSC & PAL.

* Slave Address ☞ Write: 66 (hex), Read: 66 (hex)

| Sub Address | Data | | | | | | | | | | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AF~0 | DF | DE | DD | DC | DB | DA | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0001 | | | | | | | | | | | | | | | NP | | R/W |
| 0078 | Display Version in Hex(=00) | | | | | | | | Display Size in Hex (42"=2A) | | | | | | | | R |
| 0079 | 256K Version in Hex(=00) | | | | | | | | FPGA Version in Hex(=00) | | | | | | | | R |
| 0080 | | Pattern Select | | | | | | | | | | | | | | | R/W |
| 0081 | Data Level | | | | | | | | | | | | | | | | R/W |
| 009C | | | | | | | | DF | | | | | | | | | R/W |
| 00C4 | | APC_Data Hold Time | | | | | | | | | | | | | | | R/W |
| 00DE | | | | | | | | IE | | | | | | | | | R/W |
| 20DE | | | | | | | | IE | | | | | | | | | R/W |

**Note 1.** The region except the table that is shown above is system area.
Customers are not recommended to control or write data on system area without any notice to SDI..

**Note 2**. 0001~007F : common area for NTSC & PAL.
0080~1FFF : Area for NTSC system.
2080~3FFF : Area for PAL system.

## Details of Settings

| Sub Address | Data Bit | Symbol | Item / Function | Setting [hex] | | Note |
|---|---|---|---|---|---|---|
| | | | | Range | Initial | |
| 0001 | 0~1 | NP | NTSC/PAL Select<br>(valid only when internal pattern is activated ) | 10 / 01 | 10 | *(a) |
| 0080<br>2080 | 8~D | PS | Pattern Select<br>☞ Patterns below are valid when **IE** (Internal clk or External clk) is set to '1'.<br>00: Full Window (Black)<br>01~04: Full Window (White, Red, Green, Blue)<br>05~08: 9 Point Box (White, Red, Green, Blue)<br>09: 4% Window , 0A: Color Bar<br>0B~0E: Cross Bar (White, Red, Green, Blue)<br>0F: Cross Hatch 10: Dot Array<br>11: 50% Gray<br>12~13: Gray Bar (Vertical, Horizontal)<br>14~15: Vertical Ramp Pattern (Stay, Scroll)<br>16~17: Horizontal Ramp Pattern ( 〃 ) | 00~17 | 01 | *(a) |
| 0081<br>2081 | 8~F | DL | Data Level<br>☞ Patterns below are valid when **IE** (Internal clk or External clk) is set to '1'.<br>01~FF: 0~255 Gray Level. | 00~FF | FF | *(a) |
| 009C<br>209C | 8 | DF | **Diffusion Filter Enable**<br>(1=ON, 0=OFF)<br>* Initial value : 00(NTSC), **00**(PAL) | 0 or 1 | 0(NT)<br>1(PA) | *(c) |
| 00C4<br>20C4 | 8~F | APC_DHT | **APC Level Shift Speed**<br>(00=0sec, **0F=0.25sec, 0C=0.24sec)**<br>* Initial value : 0F(NTSC), 0C(PAL)) | 00~1E | 1E | *(b) |
| 00DE<br>20DE | 8 | IE | **Internal Pattern Enable**<br>(1=ON, 0=OFF)<br>☞ If you set 00DE and 20DE all to '1', you can drive internal pattern with external CLK for both NTSC and PAL by switching '0001' as '10' or '01'. | 0 or 1 | 0 | *(a) |

*(a): Please access these address for test use only.
For ordinary operating conditions, values if these address should be set to initial values.
*(b): Customers can set these values considering their specifications.
*(c): Diffusion Filter – This filter disperses dynamic false contour at continuous gray level of input data(for example, human body). SDI Module uses same number of SF(12) for NTSC and PAL. By using this option, dynamic false contours of SDI Module in PAL could be decreased a little.

10. 11. Connector Specifications

| Pin No. | Pin Name(LA03) |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | RxIN0- |
| 4 | RxIN0+ |
| 5 | GND |
| 6 | GND |
| 7 | RxIN1- |
| 8 | RxIN1+ |
| 9 | GND |
| 10 | GND |
| 11 | RxIN2- |
| 12 | RxIN2+ |
| 13 | GND |
| 14 | GND |
| 15 | RxCLKIN- |
| 16 | RxCLKIN+ |
| 17 | GND |
| 18 | GND |
| 19 | RxIN3- |
| 20 | RxIN3+ |
| 21 | GND |
| 22 | Dedicated Pin |
| 23 | Dedicated Pin |
| 24 | Dedicated Pin |
| 25 | Dedicated Pin |
| 26 | GND |
| 27 | SCL |
| 28 | GND |
| 29 | SDA |
| 30 | GND |
| 31 | NC |

1.LA03 connector is located in Logic Board.

2. Pin to Pin pitch of connector LA03 is 0.625mm.

3. Connector LA03(parts #:1554A-3141R ) is supplied by UJU Electronics. This Item is compatible with FI-WE*P.HF(JAE, JAPAN)
   -. Module side connector: FI-WE*P.HF or 1554A-3141R.
   -. Matching connector: GT121-HS (housing), GT121-TS (contact)
   -. Connector supplier: FI-WE*P.HF(JAE, Japan Aviation Industry, JAPAN)
   -.1554A-3141R(UJU Electronics, KOEA)
   -. GT121-HS/TS(LG cable, KOREA)
   -. Fitting Cable: AWG#28 to 32 twist pair cable

4. The length of mating cable to LA03 is recommended to be not longer than 25.0cm.

5. Pin numbering order : Right to Left view from component side of Logic Board.

6. Reserved for factory use only. This pin should be disconnected in case of customer's use.

**[Note]**

**1** : If using a long cable, applied voltage may be dropped because of its resistance. Specified voltage should be applied correctly at the input of the module side connector.

## 11. SMPS Specifications

### SCOPE

The scope of the document is limited to the requirements of a power supply with 17DC outputs for SAMSUNG SDI PDP Module or TV set.

The power supply will have the following features : free input capability, remote ON/OFF, standby voltage and electrical characteristics in Table

### SUPPLY OVERVIEW

The **-***-** is a power supply designed to be used in SDI 42"HD PDP Module and TV

Table 1) TBD- To be Updated

| Items | Comments |
|---|---|
| Output Power | 320 Watt max. continuous<br>500 Watt peak load |
| Efficiency | 82%minimum at 100Vac,maximum load(*1)(*2) |

*1.Test condition shall be defined in section 3.2.5 Efficiency

*2.The efficiency can be decreased to 80% depending on the proto Modules test results

Display Supply Output Capabilities

Table 2) TBD- To be Updated

| Output Name | Nominal Voltage(V) | Output Current | | | Regulation (%) | Variable Range(V)(*1) | Remark |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Peak | | | |
| Vs | +170V | 0.1A | 2.5 A | 5.0A | ±5 | ± 7V | Iopk:Ton(5ms), Tprd(16ms) |
| Va | +70V | 0.1A | 2.0A | 3.0A | ±5 | ±7V | Iopk:Ton(8ms), Tprd(16ms) |
| Vscan (*2) | -60V | 0.01A | 0.25A | 0.2A | ±5 | ± 10V | Iopk:Ton(100us), Tprd(1.5ms) |
| Vset (*2) | +160V | 0.01A | 0.1A | 0.2A | ±5 | ± 10V | Iopk:Ton(100us), Tprd(1.5ms) |
| Ve (*2) | +155V | 0.01A | 0.2A | 0.3A | ±5 | ± 10V | Iopk:Ton(100us), Tprd(1.5ms) |
| Vg | +15V | 0.1A | 1.0A | 1.0A | ±5 | Fixed | |
| D5V | +5V | 0.2A | 3.5A | 4.0A | ±5 | 5~5.6V | |
| D3.3V | + 3.3V | 0.2A | 3.0A | 3.5A | ±5 | 2.8V~3.7V | |

*1.The output voltages for Vs, Va, Vscan, Vset, Ve, D5V should be varied within the variable ranges by feedback variable resistors.

*2.DC/DC converters(Vscan, Vset, Ve) are non-isolated type from Va or Vs.

EMG*TOP2K4 outputs (TBD, To be Updated)

| *Pin number* | *Voltage or signal name* | *Value (if relevant)* | *Consumption* | *Tolerance* |
|---|---|---|---|---|
| 1 | GND | | | |
| 2 | GND | | | |
| 3 | 8V6 | 8.6V | **0.8A** | **+/- 0.45V** |
| 4 | 12V | 12V | 2A | **+/- 5%** |
| 5 | 5V_Sw | **5.3V** | 800mA | **Min 5.1, max 5.6** |
| 6 | GND | | | |
| 7 | 5V2 | **5.4V** | 200mA (or1A if 5V_sw coupled with 5V2) | **Min 5.1, max 5.7** |
| ***8*** | ***Vtun*** | ***33V in application*** | ***10mA max*** | **33V** |
| 9 | 12V | See pin 4 | See pin 4 | |
| **10** | **9V_standby** | **9V** | **5mA** | |
| **11** | **NC** | | | |
| 1 | NC | | | |
| 2 | NC | | | |
| 3 | NC | | | |
| 4 | GND | | | |
| 5 | Fan Speed | | | |
| 6 | Temp sensor | | | |
| 7 | Standby | | | |
| 8 | DC prot | | | |
| ***9*** | ***5V_relay_Io2*** | ***9V (*)*** | ***10mA*** | |
| 10 | Power_OK | | | |
| 1 | GND | | | |
| 2 | GND | | | |
| 3 | GND | | | |
| 4 | GND | | | |
| 5 | VSND_Pos | +14V | 2A peak | **Min 15V, Max 19.5V** |
| 6 | VSND_Pos | +14V | | |
| 7 | DC prot (*) | | | |
| 1 | 12V | 12V | 2A | **10%** |
| 2 | 12V | 12V | 2A | |
| 3 | GND | | | |
| 4 | GND | | | |

## ELECTRICAL SPECIFICATION

* AC INPUT REQUIREMENTS

The power supply shall be able to supply full rated output power over the free voltage ranges that are rated input voltage(90 to 264Vac)

| Parameter | Min. | Nominal | Max | Module |
|---|---|---|---|---|
| Frequency | 47 | 50/60 | 63 | Hz |
| Voltage | 90 | 100 to 240 | 264 | V |

1) INPUT OVERCURRENT PROTECTION

The **-***-** shall incorporate primary fusing for input over-current protection. A fuse shall be located to live line.

2) INRUSH CURRENT LIMITING

Peak inrush current shall not exceed 50A in cold & hot start conditions and must be limited to the extent that no damage done to the supply under any specified line, load, and temperature conditions

3) POWER FACTOR CORRECTION

The **-***-** shall comply with the regulation EN61000-3-2 that mandates the maximum allowable input AC current harmonic distortion. Compliance to this regulation shall be tested at Max-load and at input 75watts.

* DC OUTPUT REQUIREMENTS

1) DC VOLTAGE REGULATION

See the table 2), 3), 4), 5)

2) DC OUTPUT CURRENT

See the table 2), 3), 4), 5)

3) OUTPUT POWER

The power supply shall be capable of continuously supplying when installed in PDT TV system, 380watts under all specified conditions. . The power supply shall be cable of supplying 500watts peak output power

4) EFFICIENCY

The power supply shall be a minimum 82% efficiency under maximum load for Vs,Va, 3.3V , 5V, 9V_STBY 5V_STBY_SW, no load for Vscan,Vset,Ve,Vg, 8.6V, VSND_POS, VSND_NEG, FANSP, 3.3V_STBY_SW at 100V/60Hz and 230V/50Hz, In the suspend mode, the 5V_STBY_SW shall be loaded to 0.04A and the outputs shall be "OFF" condition by AC Line relay "OFF" and input power shall be less than 1.5watts..

| AC Input Power | 5V_STBY_SW |
|---|---|
| 1.5watt max | 0.04A |

5) RIPPLE AND NOISE (TBD, To be included)

| Output | Ripple & Noise | Output | Ripple & Noise |
|---|---|---|---|
| Vs | TBD | 5V | TBD |
| Va | TBD | 3.3V | TBD |
| Vscan | TBD | 5v2 | TBD |
| Vset | TBD | 12V | TBD |
| Ve | TBD | 8.6V | TBD |
| Vg | TBD | 9V_STBY | TBD |
| D5V | TBD | | |

6) OUTPUT TRANSIENT RESPONSE

The outputs shall not undershoot or overshoot beyond the specified voltage tolerances after applying the following load changes with the stated slew rate on the measured output. The transient response measurements shall be made with a load changing repetition rate of 50Hz to 10kHz.

| Voltage Tolerance Limit | Slew Rate | Load Change |
|---|---|---|
| +/- 3% | 0.2A/us | min to 50% load and 50% to max load |
| +/- 5% | 0.2A/us | min. to max. load |

7) OUTPUT SEQUENCING

Vs_on the signal came out from Logic Board and then Vs will rise. Following Vs, Vscan,Ve and Vset will rise in order.

8) HOLD_UP TIME

The **-***-** shall maintain output regulation with respect to table 2 for a minimum 20ms under following conditions:

When the input voltage is 90Vrms at 47Hz, (and) the output load is maximum

To test the hold-up time, the input voltage will be turned off (close) to the 0 deg of AC input. The measurement shall be made from the point at which the voltage is turned off (AC interrupt) and the output voltage drops below the static regulation.

9) LINE DROP-OUT IMMUNITY

The PS-422-PH maintains its output regulation during AC line 3cycle off in every 5s condition.

* OUTPUT PROTECTION

No damage, fire and smoke shall occur during faults

1) OVER VOLTAGE PROTECTION

The power supply shall provide a latch-mode above the voltage protection

| Output | Over Voltage Limit |
|---|---|
| Vs | TBD |
| Va | TBD |
| 5V | TBD |
| 3.3V | TBD |

2) UNDER VOLTAGE PROTECTION

The power supply shall have an auto-recovery mode above the current protection

| Output | Under Voltage Limit |
|---|---|
| Vs | TBD |
| Va | TBD |
| Vset | TBD |
| Ve | TBD |
| Vscan | TBD |
| 3.3V | TBD |
| 5V | TBD |

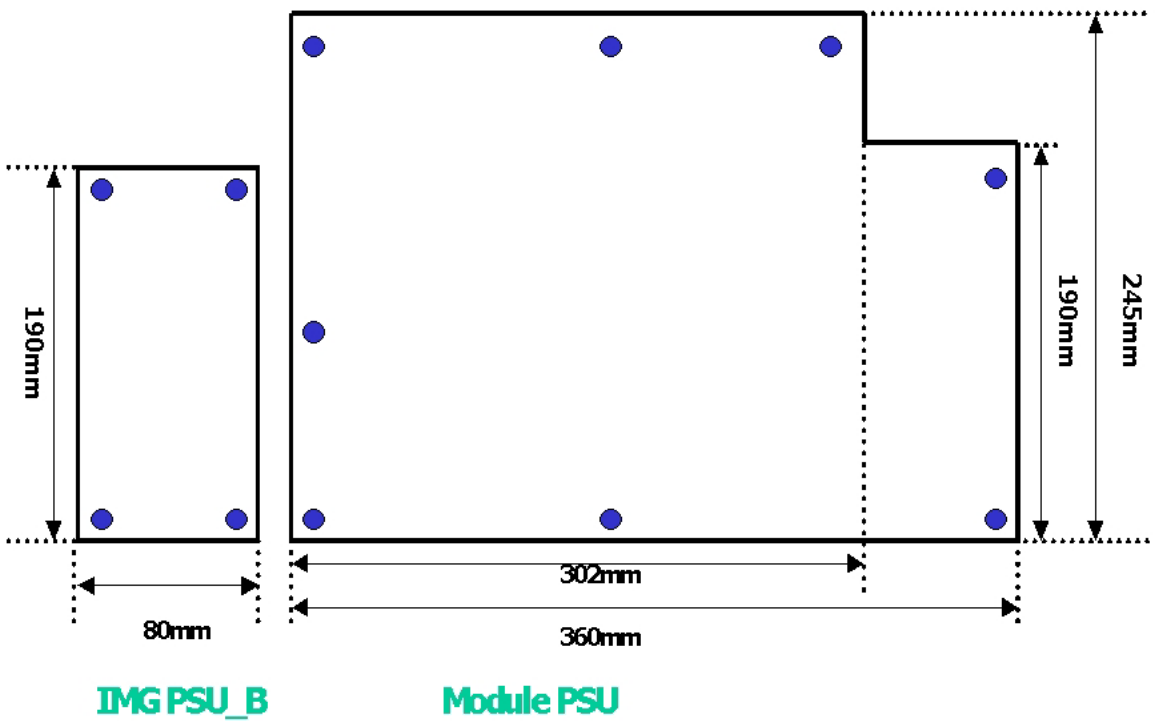
3) SHORT CIRCUIT PROTECTION

If any output is shorted to the secondary return(R<0.03ohm), no damage shall occur.

4) SMPS BEHAVIOUR OF OUTPUT PROTECTION

No damage and hazardous condition will occur in any condition, including the no load condition.

* MECHANICAL REQUIREMENTS (TBD, To be updated, it will be designed as two boards)




* AC INPUT (CN8004, TBD, To be Updated) CONNECTOR

Part number : (TBD, To be updated)

| Pin # | Signal |
|---|---|
| 1 | AC Line |
| 2 | N.C |
| 3 | AC Neutral |

* DC OUTPUT CONNECTORS

1) IMAGE_ANALOG (CN8001, TBD, To be updated) CONNECTOR

Part number : JST-Top Through 2mm PH

| ***Pin number*** | ***Voltage or signal name*** |
|---|---|
| 1 | NC |
| 2 | NC |
| 3 | NC |
| 4 | GND |
| 5 | Fan Speed |
| 6 | Temp sensor |
| 7 | Standby |
| 8 | DC prot |
| ***9*** | ***5V_relay_Io2*** |
| 10 | Power_OK |

2) IMAGE_DIGITAL (CN8002, TBD, To be updated) CONNECTOR

Part number : JST Top Through 2mm PH

| ***Pin number*** | ***Voltage or signal name*** |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | 8V6 |
| 4 | 12V |
| 5 | 5V_Sw |
| 6 | GND |
| 7 | 5V2 |
| ***8*** | ***Vtun*** |
| 9 | 12V |
| **10** | **9V_standby** |
| **11** | **NC** |

*SCL_1 : I2C signal from/to
*SDA_1 : I2C signal from/to
POWER_OK : signal indicating all outputs are being operated as the specification

3) Audio (CN8003, TBD, To be updated) CONNECTOR

Part number : JST top through 2.5mm EH

| ***Pin number*** | ***Voltage or signal name*** |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | GND |
| 4 | GND |

| | |
|---|---|
| 5 | VSND_Pos |
| 6 | VSND_Pos |
| 7 | DC prot (*) |

4) Logic (CN8009) CONNECTOR

Part number : Molex 35312-10

| Pin# | Signal |
|---|---|
| 1 | D3.3V1 |
| 2 | D3.3V1 |
| 3 | GND |
| 4 | GND |
| 5 | D5V |
| 6 | GND |
| 7 | PDP_GO |
| 8 | 3.3V_STBY_SW |
| 9 | Vs_ON |
| 10 | GND |

5) X Drive (CN8007) CONNECTOR

Part number : Molex 35313-09

| Pin# | Signal |
|---|---|
| 1 | D5V |
| 2 | Vg |
| 3 | GND |
| 4 | GND |
| 5 | Ve |
| 6 | GND |
| 7 | GND |
| 8 | Vs |
| 9 | Vs |

6 ) XXX Board (TBD, To be updated) CONNECTORS

Part number : JST top through 2mm PH

| *Pin number* | *Voltage or signal name* |
|---|---|
| 1 | 12V |
| 2 | 12V |
| 3 | GND |
| 4 | GND |

7) Y Drive (CN8008) CONNECTOR

Part number : Molex 35313-10

| Pin# | Signal |
|---|---|
| 1 | D5V |
| 2 | Vg |
| 3 | GND |
| 4 | Vscan |
| 5 | GND |
| 6 | Vset |
| 7 | GND |
| 8 | GND |
| 9 | Vs |
| 10 | Vs |

8) Buffer (CN8004) & (CN8005) CONNECTORS

Part number : Molex 35313-05

| Pin# | Signal |
|---|---|
| 1 | Va |
| 2 | Va |
| 3 | N.C |
| 4 | GND |
| 5 | GND |

* ENVIRONMENTAL REQUIREMENTS

1) TEMPERATURE

| Condition | Power Supply Ambient Temperature | |
|---|---|---|
| | Minimum | Maximum |
| Operation within specification | -15 deg.C | 60 deg.C |
| Storage | -40 deg.C | 80 deg.C |

2) HUMIDITY(NON-CONDENSING)

| Condition | Relative Humidity | | Temperature |
|---|---|---|---|
| | Minimum | Maximum | |
| Operation of the specification | 10% | 90% | 60 deg.C |
| Non-operation | 5% | 95% | 75 deg.C |

3) ALTITUDE

| Condition | Temperature | | Pressure |
|---|---|---|---|
| | Minimum | Maximum | |
| Operation of the specification | 10 deg.C | 50 deg.C | 0-10000ft |
| Shipping Altitude | -40 deg.C | N/A | 0-50000ft |

4) MECHANICAL SHOCK

Non-operating : 50G trapezoidal wave, velocity change=170in./sec. Three drops in each of the six directions are applied to each of the samples.

5) RANDOM VIBRATION

Non-operating : 0.01G^2 per Hz at 5Hz, slopping to 0.02^2 per Hz at 20Hz and maintaining. 0.01G^2 per Hz from 20Hz to 500Hz. The area under the PSD curve is 3.13g rms. The duration shall be 10 minute per axis for all three axes of all samples.

## * ELECTROMAGNETIC COMPATIBILITY

The power supply itself complies with the EMC requirements set forth below.

Finally a vendor will do the co-work to satisfy the requirements when installed in a fully configured PDP system.

| Requirements | Relevant Standard | Test Level | Remarks |
|---|---|---|---|
| Conducted and Radiated Emission | FCC Part 15<br>ANSI C63.4<br>EN55022:1998<br>CISPR22:1997 | Class B limits with 4dB minimum margin | |
| Harmonics | EN61000-3-2 | Class D limits | |
| Flicker | EN61000-3-3 | | |
| Electro Static Discharge(ESD) | IEC 61000-4-2 | | |
| Radiated Immunity | IEC 61000-4-3 | | |
| Electrical Fast Transient | IEC 61000-4-4 | | |
| Surges | IEC 61000-4-5 | | |
| Conducted Immunity | IEC 61000-4-6 | | |
| Voltage Dips | IEC 61000-4-11 | | |
| Voltage Interruptions | IEC 61000-4-11 | | |

## * RELIABILITY

1) COMPONENT DERATING

The power supply shall comply with the Samsung electronics derating guideline.

- Semiconductor junction temperature shall not exceed 110 deg. C with an ambient temperature of 50 deg. C. Any exception is subject to the final approval.
- Coils temperature shall not exceed 120deg. C at the ambient temperature 60deg.C
- Capacitor temperature shall not exceed 95% of the rated temperature.
- Resistor wattage derating shall be 50%
- Component voltage and current derating shall be >10% at 50 deg C. Any exceptions are subject to final approval.
- Magnetic saturation of component will not be allowed under any line, load, start-up, or transient condition including 100% transients on the outputs.

2) MTBF

The power supply shall have a minimum Bellcore calculated MTBF of 200kh hours of operation at 90% confidence level at 25 deg.C , normal input and max load.

* REGULATORY COMPLIANCE

The power supply shall be designed and manufactured in compliance with the requirements of the following safety standards: UL1950,CSA C22.2 No.234.VDE,

1) LEAKAGE CURRENT

The leakage current shall not exceed 0.25mA at 90V ~ 264V.

2) DIELECTRIC STRENGTH

There is no flash during the test when 3kVac voltage is applied to between primary and secondary

*** TIMING AND CONTROL**

1) REMOTE ON/OFF CONTROL

By using functional switch, PSU can enter the stand by mode.

At this mode, PSU makes 5V_relay_Io2 as 'H' and waits 'Remote ON' signal.

2) POWER ON TIME

By making STBY as 'L', PSU starts the fuction.

3) RISE TIME

The output voltages shall rise from 10% to 90% of their output voltage at 500ms maximum for Vs,Va at maximum load.

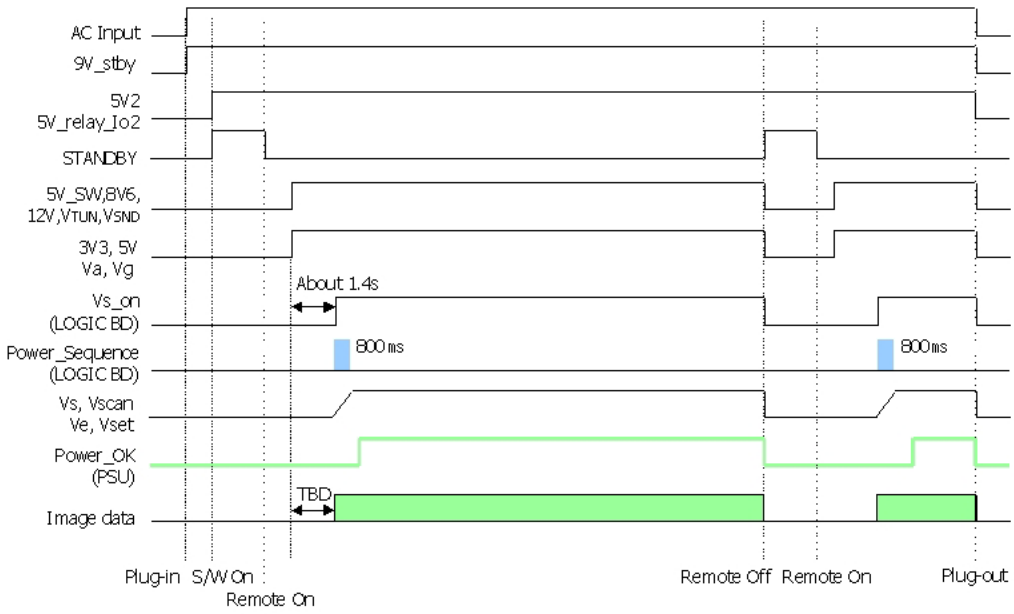
4) Vs_ON

In order to prevent the turn-on inrush current going through the output load of Vs outputs, Vs outputs shall be enable with Vs_on signal (Active high) after Va outputs is turned-on With having 5 ~ 10ms. delay time. ( Following timing diagram describes its operational sequence)
And Vs outputs shall have 300~500ms turn-on rising time.

5) OVERSHOOT AT TURN-ON/TURN-OFF

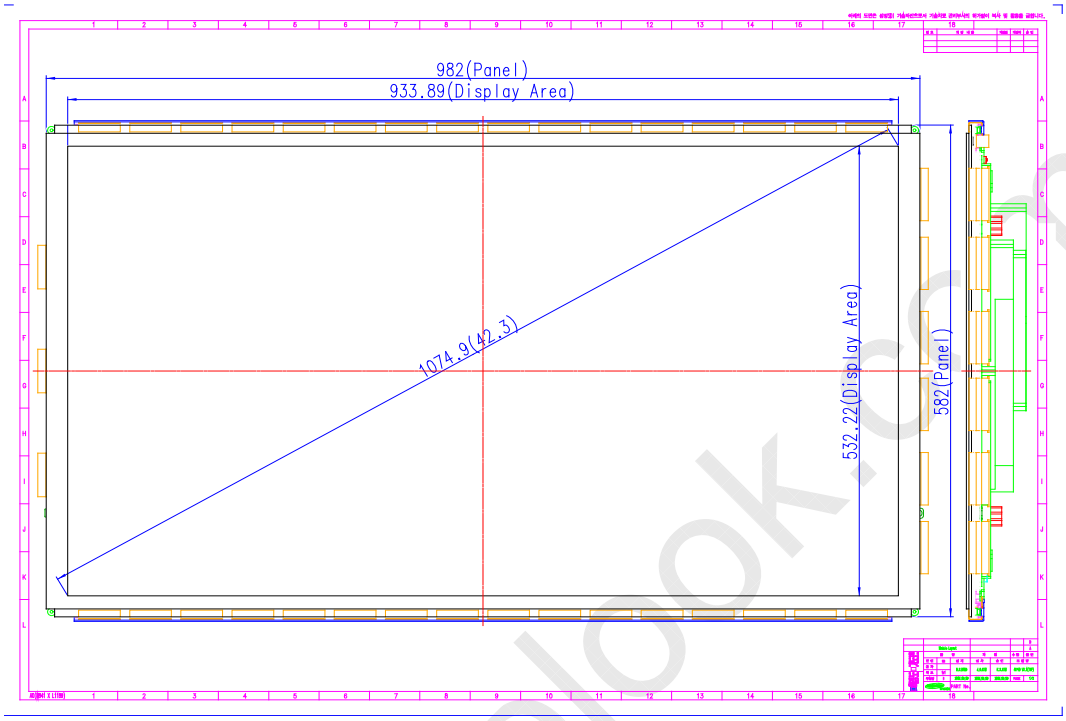
Any output overshoot at start-up or shutdown, during AC power loss, or output short circuit shall not exceed 10% of normal voltage value

# Power Sequence



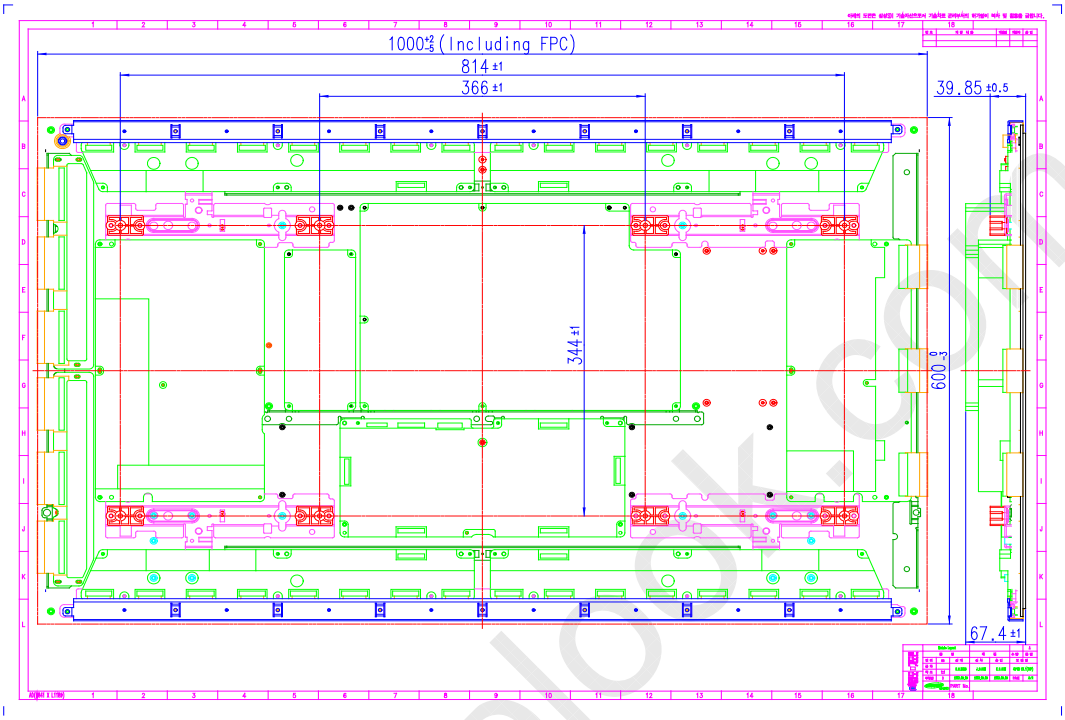
## 12. Mechanical Dimension Drawing

### 12.1. Front Side (To be updated)




Appendix A1

**12.2. Rear Side (To be updated)**




Appendix A2

## 13. Label

### 13.1 Label Type

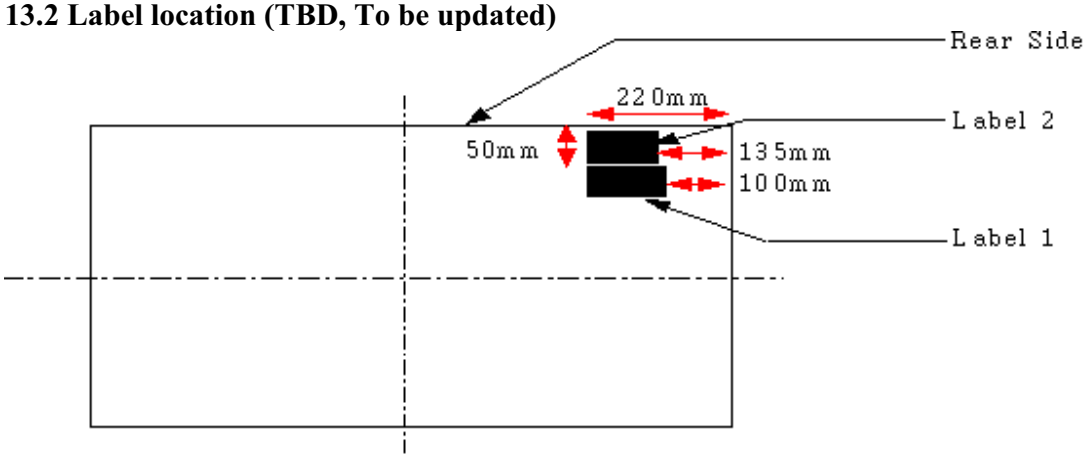
**(1) Label for the PDP Module**

(To be included)

**(2) Label for power specification**

(To be included)

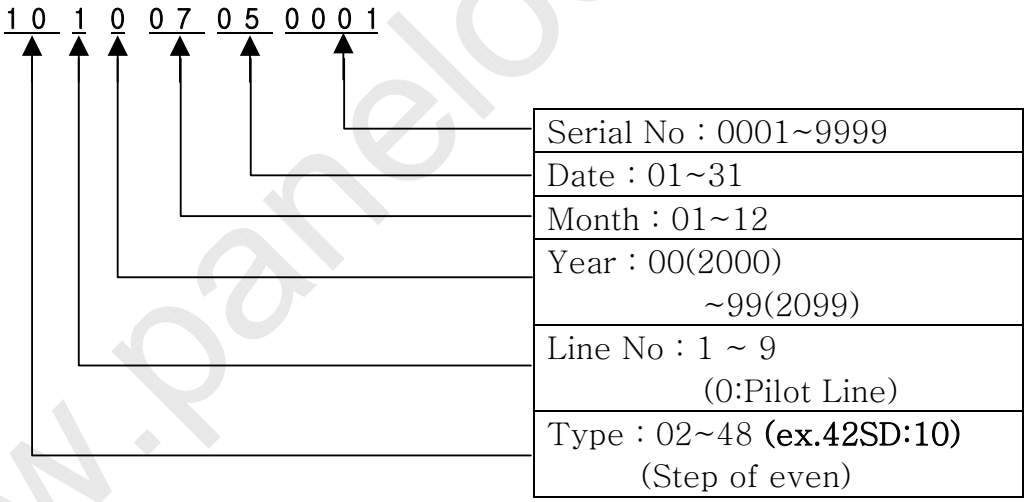
**13.2 Label location (TBD, To be updated)**




【 Notes 】

1. Label-1 is a label for the PDP Module.
2. Label-2 is a label for the power specification.

**13.3 Serial No.**



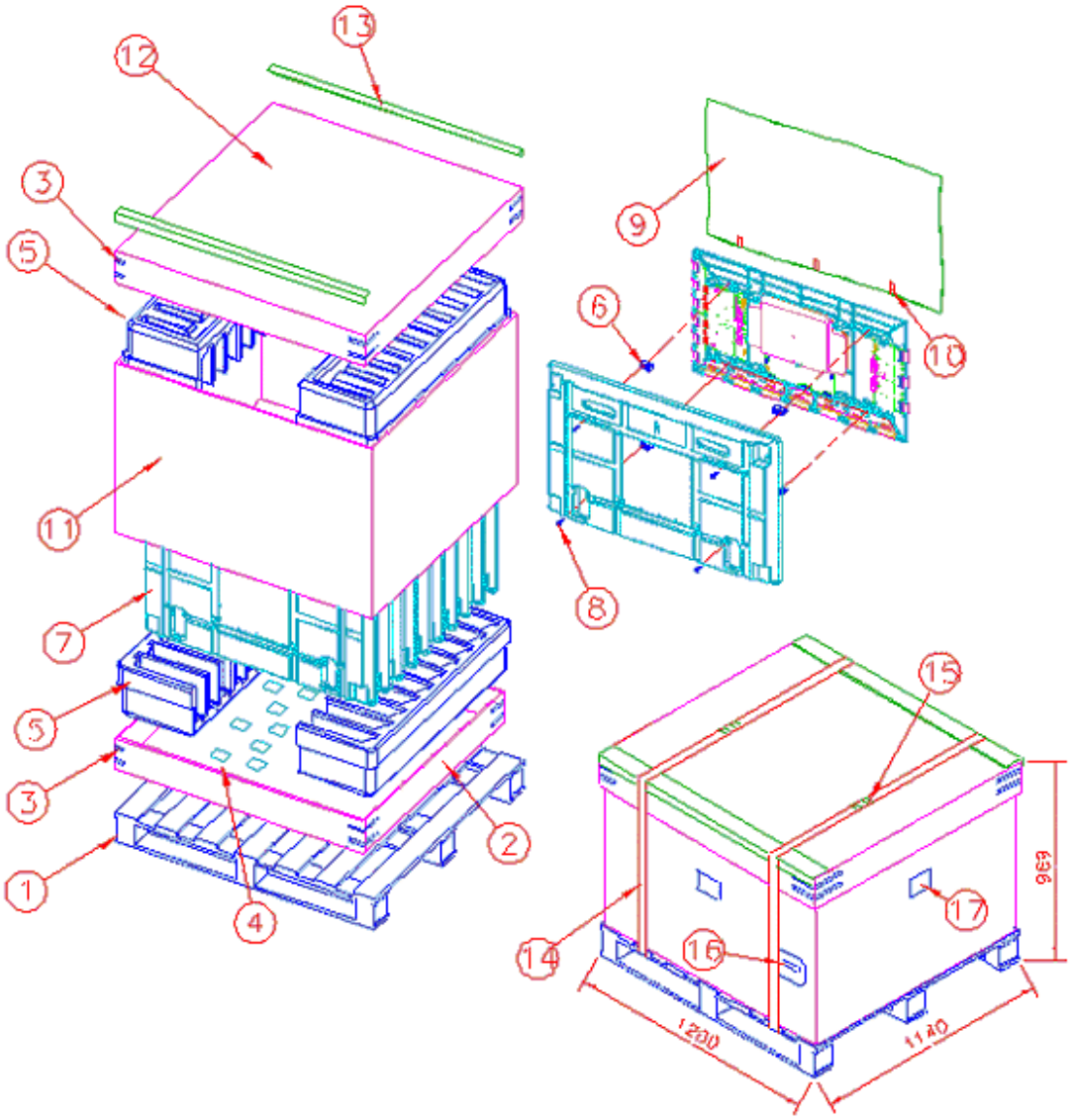
## 14. Packing

### 14.1 Packing Dimension and Parts List (TBD)

- Number of Module in 1 package: 10 Modules
- Packing dimensions (W*L*H): 1200*1140* 969 (mm) (Including Pallet :145mm)
- Weight: About 280 ± 5 (Kg)

| NO | CODE-NO | Item | SPEC | Q'ty |
|---|---|---|---|---|
| 1 | LJ69-00470A | PALLET | S2.0,PINE TREE,W1200,L1140,H145 | 100 |
| 2 | LJ69-00538A | PACKING-COVER,BOT | 42S2.0,CARTON-BOX,DW,T1.0,W1072,L1146,H150 | 100 |
| 3 | 0203-001320 | TAPE-FILAMENT | #8915,T0.15,W24,L55000,NTR | 8.7 |
| 4 | LJ69-00328A | CHEMICALS | W115XL90,DRY PACK,100G | 1000 |
| 5 | LJ69-00537A | CUSHION-SET | 42S2.0,EPP,W304,L1080,H242 | 100 |
| 6 | LJ60-00110A | SPACER-HOLDER,P | 42S2.0,ABS HB,BLK,H36.5 | 4000 |
| 7 | LJ69-00527A | PACKING-MODULE | S2.0,HIPS,T3,W685,L1060,H76,BLK,HB | 1000 |
| 8 | 6006-001185 | SCREW-ASS'Y MACH | WSP,PH,+,M8,L53,ZPC(YEL),SWRCH18A | 4000 |
| 9 | 6902-000404 | BAG-ANTISTATIC | LDPE,T0.5,W1260,L950,WHT | 1000 |
| 10 | 0203-001321 | TAPE-ACETATE | #810,T0.06,W18,L65000,NTR | 4.2 |
| 11 | LJ69-00474A | PACKING-BOX-CENTER | S2.0,TW,W1150,L818,H818 | 100 |
| 12 | LJ69-00472A | PACKING-COVER | S2.0,DW,T10,W1420,L1480 | 100 |
| 13 | LJ61-00568A | GUIDE-PACK | PAPER-ANG,T5.0,W1190,L50 | 200 |
| 14 | LJ69-00330A | BAND-PP | PP,T0.9,W17.5,WHT,15.6KG | 5.2 |
| 15 | LJ64-00026A | LOCKER-BAND,CLIP | SPC,18MM,T0.5 | 400 |
| 16 | LJ68-00115A | LABEL-SHOCKWATCH | 42S2.0,ART 120G,T0.08,W97,L97,YEL,25G,L-65 | 100 |
| 17 | LJ68-00114A | LABEL-INSPECTION | 63HD,ART PAPER,-,W206,L146,BLK,WHT | 400 |

14.2 **Packing Assay drawing**



## 15. RELIABLITY

### 15.1 MTBF Value

Mean Time Between Failure is dependent on the overall PDP Module design.

MTBF : 20,000hours (environmental temperature : 25℃)

※ Condition : 25℃, Used moving Picture Signal

### 15.2 Expected Service Life

#1. Definition

The expected service life is defined by the following two categories.
And the life time is defined by either (1) or (2), whichever occurs first.

(1) The white color Luminance level becomes half (50%) of its initial value, which is determined by the phosphor characteristics.

(2) The number of display cell defects increases to double the specification value, which is depending on the discharge characteristics.

#2. Test condition and life time

The expected service life time varies depending on the display conditions set forth below.

(1) Full screen white color display

Life time : 30,000 hours

* Test condition : 8Hr/Day

## 16. WARNING / CAUTION / NOTICE

TO PREVENT POSSIBLE DANGER, DAMAGE, AND BODILY HARM, PLEASE CONSIDER AND OBSERVE ALL WARNINGS AND CAUTIONS CONTAINED IN THIS PARAGRAPH.

### 16.1 Warning

If you do not consider the following warnings, it could result in death or serious injury

(1) The S42AX-XD02 Module is controlled by high voltage about 350V. If you need to handle the Module during operation or just after power-off, you must take proper precautions against electric shock and must not touch the drive circuit portion and metallic part of S42AX-XD02 Module within 5 minutes.
The capacitors in the drive circuit portion remain temporarily charged even after the power is turned off. After turning off the power, you must be sure to wait at least one minute before touching the Module. If the remain voltage is strong enough, it could result in electric shock.

(2) Do not use any other power supply voltage other than the voltage specified in this product specifications. If you use power voltage deviated from the specifications, it could result in product failure.

(3) Do not operate or install under the deviated surroundings from the environmental specification set for the below; in moisture, rain or near water-for example, bath tub, laundry tub, kitchen sink; in a wet basement; or near a swimming pool; and also near fire or heater - for example, near or over radiator or heat resistor; or where it is exposed to direct sunlight; or somewhere like that. If you use the S42AX-XD02 Module in places mentioned above, it could result in electric shock, fire hazard or product failure.

(4) If any foreign objects (e.g. water, liquid and metallic chip or dust) entered the S42AX-XD02 Module, the power supply voltage to the S42AX-XD02 Module must be turned off immediately. Also, never push objects of any kind into the S42AX-XD02 Module as they may touch dangerous voltage point or make short circuits that could result in fire hazard or electric shock.

(5) If smoke, offensive smell or unusual noise should come from the S42AX-XD02 Module, the power supply voltage to the S42AX-XD02 Module must be turned off immediately. Also, when the S42AX-XD02 screen fails to display any picture after the power-on or during operation, the power supply must be turned off immediately. Do not continue to operate the S42AX-XD02 Module under these conditions.

(6) Do not disconnect or connect the S42AX-XD02 Module's connector while the power supply is on, or immediately after power off. Because the S42AX-XD02 Module is operated by high voltage, and the capacitors in drive circuit remain temporarily charged even after the power is turned off. If you need to disconnect or reconnect it, you have to wait at least one minute after power off.

(7) Do not disconnect or connect the power connector by a wet hand. The voltage of the product may be strong enough to cause an electric shock.

(8) Do not damage the power cable of the S42AX-XD02 Module, also do not modify it.

(9) When the power cable or connector is damaged or frayed, do not use it.

(10) When the power connector is covered with dust, please wipe it out with a dry cloth before the power on.

### 16.2 Caution

If you do not consider the following cautions, it may result in personal injury or damage facilities.

(1) Do not set the S42AX-XD02 Module on an unstable place, vibrating place and inclined place. The S42AX-XD02 Module may fall or collapse, and it may cause serious injury to a person, and serious damage to the product.

(2) If you need to remove the S42AX-XD02 Module to another place, you must turn off the power supply and detach the interface cable and power cable from the S42AX-XD02 Module beforehand, and watch your steps not to step on the cables during the operation. If the cables are damaged during the transport, it may result in fire hazard or electric shock. Also if the S42AX-XD02 Module is dropped or fallen, it may cause a serious injury to a person.

(3) When you draw or insert the S42AX-XD02 's cable, you must turn off the power supply and do it (with) holding the connector. If you forcibly draw the cable, the electric wire in the cable can be exposed or broken. It may result in fire hazard or electric shock.

(4) When you carry the S42AX-XD02 Module, it should be done with at least two workers in order to avoid any unexpected accidents.

(5) The S42AX-XD02 Module has a glass-plate. If the S42AX-XD02 Module is inflicted with excessive stress - for example; shock, vibration, bending or heat-shock, the glass plate could be broken. It may result in a personal injury. Also, do not press or strike the glass surface.

(6) If the glass panel was broken, do not touch it with bare hand. It may result in a cut injury.

(7) Do not place any object on the glass panel. It may be the cause of the scratch or break of the glass panel.

(8) Do not place any object on the S42AX-XD02 Module. It may result in a personal injury due to fall or drop.

**16.3 Notice**

When you apply the S42AX-XD02 Module to your system or handle it, you must make sure to follow the notices set forth below.

☐ ***Notice to your system design***

(1) The S42AX-XD02 Module radiates the infrared rays of between 800 and 1000㎚. It may bring an error in operating the IR-remote controller or another electric system. Please consider (to) providing the IR absorb filter in your system, and evaluating it.

(2) The S42AX-XD02 Module has a high-voltage switching circuit and a high-speed clock circuit. Therefore, you have to apply and evaluate the EMC consideration of your system.

(3) The S42AX-XD02 Module has a glass plate. In your mechanical design, please (consider to) avoid any excessive shock and stress to the glass surface. Also be careful not to demage the tip-tube at the corner of glass plate. If the glass plate and tip-tube are damaged, the S42AX-XD02 &Module may fail.

(4) In your system, for your safety, please have the remaining voltage of the S42AX-XD02 Module leaked immediately after power-off.

(5) As the S42AX-XD02 Module generates heat during operation, please make sure the well-radiation and well-ventilation are provided for your system design. The S42AX-XD02 Module may be defected by the usage out of the specified ambient temperature.

(6) The ventilation design in your system should have a back-cover that is able to prevent moisture and dust from getting into the inside of the electric circuit, because the S42AX-XD02 Module has high-density electric parts with high-voltage. If the driver circuit has condensation or dusts, it may cause a short circuit or dielectric breakdown.

(7) If the S42AX-XD02 Module displays a fixed pattern on the screen for are extended period of time, it could make the differences in Luminance and chromaticity between fixed pattern area and other areas. It is because the Luminance of the fixed pattern area becomes lower than the other areas due to the degradation of the phosphor, but this phenomenon is not a failure.
On the other hand, when the display pattern is changed, the illuminated areas may maintain their Luminance temporarily (for few minutes). This phenomenon is a characteristic from color S42AX-XD02 itself due to the activation of the discharge surface in the S42AX-XD02 panel, which is normal. If you have an intention of displaying the fixed pattern, the screen-saver technique should be applied to your systems in order to minimize the image retention.

(8) The S42AX-XD02 Module is not intended for the equipments that require extremely high reliability such as aerospace equipments, nuclear control systems or medical equipments for life support.

(9) Based on the requirements of the safety standard (UL, EN etc.), be sure to add the filter that come up to the impact test to the glass pate.

☐ ***Notice to the operation and handling of the S42AX-XD02 Module***.

(1) To prevent defect or failure, please check the cable connections and power-supply condition before power-on.

(2) The S42AX-XD02 Module is controlled by high voltage. Not only during operation but also immediately after power-off, do not disconnect or reconnect the S42AX-XD02 Module's connector because it may result in failure. If you need to disconnect or reconnect, you have to wait at least one minute after power-off.

(3) The S42AX-XD02 Module is equipped with various protection circuits that automatically stop the Module operation, if an interface signal or the power voltage becomes abnormal during operation. If the S42AX-XD02 Module stops suddenly during operation, please check the conditions of input signal or power source before restarting.

(4) For the protection of the circuit, if an abnormal situation is occurred, the high output voltage will be shut down by (watching) the internal input voltage (Vs/ Va/ Vcc). In this case, the Module power resetting is necessary to recover.
There are also fuses in the Vs and Va power supply system to prevent smoking and firing by the excessive current. The protecting function of the address driver of keeping a supervisory device for the internal current is provided in the Va power supply system. Therefore, the number of sub-frames decreases to a proper value when the Ia current exceeds a constant value occasionally.

(5) If an abnormal situation such as disconnecting of the input connector occurs, this Module will be on stand-by, which the supply of high output voltage is stopped even if an external power is being supplied. If a normal signal is inputted after this, normal operation state, operations can be restarted again by re-inputting a normal signal. However, it is necessary to rest the Module power when tVH and/or tHV are less than the minimum value provided in the specification

(6) To ensure reliable operation of the S42AX-XD02 Module and to protect it from overheating, do not wrap or cover it with a cloth or like a sheet during power-on period. Also, do not place the S42AX-XD02 Module in a confined space or any other places of poor ventilation.

(7) If you continue to watch the naked S42AX-XD02 screen(without filter glass) for a long time, your eyes could be fatigued. We recommend you rest your eyes occasionally.

(8) The S42AX-XD02 screen is controlled with the display-data signals and synchronized signals. If noise interferes with those signals, the S42AX-XD02 screen could become unstable and, in some case, would cause a failure. Do not place any equipment that generates excessive EMI/RFI noise near the interface cable of the S42AX-XD02 Module, and keep the cables as short as possible.

(9) Be careful not to break the glass panel when you handle the S42AX-XD02 Module. Also, when handling the S42AX-XD02 Module, you must wear gloves or other hand protection to prevent injuries that can occur in case when the glass panel is broken.

(10) The glass panel section and drive circuit section of the S42AX-XD02 Module are closely

connected and they function as a pair. If the Module is arbitrarily recombined, restructured, or disassembled, SDI will not be responsible for the function, quality, or operational integrity of the modified Module. Do not recombine, restructure, or disassemble it.
(only, the Module for A/S is allowed to be recombined, restructured, or disassembled.)

(11) To avoid a possible electric shock, you must make sure that the power supply voltage of S42AX-XD02 Module is turned off before cleaning. To clean the S42AX-XD02 's glass panel, apply water or a natural detergent to a piece of soft cloth or gauze, and wring the cloth tightly before wiping the screen. Make sure that no water comes in contact with the connecting terminals on the side of the glass panel. Do not use chemical solvents, such as paint thinner or benzene, to clean the glass panel.

(12) The drive circuit section of S42AX-XD02 Module uses C-MOS integrated circuits that must be protected from static electricity. Therefore when transporting or delivering the Module, be sure to put the Module in an antistatic bag. When handling the S42AX-XD02 Module, take adequate grounding precautions to prevent static electricity.

(13) When delivering or transporting the S42AX-XD02 Module, you must take special precautions because excessive vibration or shock should not be applied to it. If the Module is dropped, or (if) excessive vibration/shock is applied, the glass panel of the S42AX-XD02 Module may be broken and the drive circuit may be damaged. The packing for delivering or transporting should be made with strict instructions.

(14) When storing the S42AX-XD02 Module, you must select an environmentally controlled place. Avoid any environment in which the temperature or humidity exceeds the specification values. If you are storing it for a long period of time, We recommend that you place the Module together with a dehumidifying agent, such as silica gel, in a moisture-proof bag and keep it in an environmentally controlled place.

(15) The S42AX-XD02 Module is composed of various kinds of materials such as glass plate, metals and plastics. A qualified service technician is required for the disposal of the S42AX-XD02 Module.

### ☐ *Notice of the S42AX-XD02 Module performance*

The S42AX-XD02 Module is the newest display device utilizing the gas discharge technology and digital signal processing technology, and its performances are mostly similar to those of CRT. However, some display performances of the S42AX-****Module are different from the CRT's. Please consider the following notices when you watch the S42AX-XD02 screen.

(1) There is (a) slight Neon luminance shown outside of the effective display area on the glass panel. Conceal this part so that it may not be seen on the display surface.

(2) Depending on the type and time of usage, there may be a slight change in the Luminance and color. There may be an increase of both X-value and Y-value by 0.05 at the maximum in chromaticity. In this case, adjust it using the external data signal.

(3) Because the S42AX-XD02 Module uses phosphor to emit a light, the phosphor, like a CRT,

will be deteriorated in proportion to the display signal and Luminance settings. If the same pattern is displayed continuously (fixed display) for an extended period of time, the Luminance of that area will be decreased over non-lit areas due to the fact that the discharge surface will be more activated comparing to the other areas.

(4) When the Vsync signal timing becomes shorter right after the changing of Vsync frequency (e.g. from 50㎐ to 60H / from 60㎐ to 70㎐) depending on the Multi-Vsync function, an initial Vsync signal of the changed frequency will be disregarded and the S42AX-XD02 screen will be interrupted for 1 frame period in maximum.

(5) Because the S42AX-XD02 Module is a digital processing display device, this Module is equipped with the Error diffusion technology and a Duplicated Sub-Frame method to display the grayscale and false contour improvement. However, you may sometimes find a color false contour, especially in human facial contour, in moving picture due to the difference of display performance comparing to the TV-tube.

(6) If the S42AX-XD02 Module displays some video test patterns that are mostly used in a laboratory or inspection process of the manufacturing facilities, you may find the following subjects. But these subjects sould not be recognized in the failure or defects because the display performance of the S42AX-XD02 Module is equipped with Error diffusion technology and Duplicated Sub-Frame method(for PAL) based on digital processing technique.

<a> Linearity in the grayscale test pattern

If the S42AX-****Module displays the grayscale test pattern (e.g. white color Luminance is gradually changed horizontally or vertically) in a screen, you may find the disparity of Luminance at adjacent grayscale patterns. This behavior is caused by duplicated sub-frame condition(for PAL), display load correction and electrode dependency.

<b> Color contouring and dithering at the stationary picture

If the stationary picture such as a human face or the like is shown in the S42AX-XD02 screen, you may feel some unstable noise at the contour area. This behavior is called the color contouring or dithering, and is caused by the error diffusion condition, display load correction and electroad dependency.

(6) If the S42AX-XD02 Module is operated under inadequate conditions or harsh environment, the screen may become unstable or noisy. This instability is mostly related to ambient temperature, air pressure, input signal instability (include signal noise), input power voltage and strong magnetic field such as MRI/NMR application or superconducting magnet application. Please do not apply the S42AX-XD02 Module to inadequate conditions or harsh environment mentioned above.

## Disclaimer

**This Specification stipulates the final and comprehensive requirements for the respective products hereof. Beyond this Specification, it is the responsiblity of the customer to explicitly disclose any additional requirements, information or reservations regarding these requirements to Samsung SDI prior to implementation, where any and all disclosures of the customer shall be with an authorized representative of Samsung SDI in writing. Samsung SDI shall not be responsible for safety, performance, functionality or compatability of the system with which the Samsung SDI-supplied components are intergrated unless such features have been expressly communicated and described in the Specification. SAMSUNG SDI MAKES NO GUARANTY OR WARRANTY, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, TO ANY PARTY. Moreover, any party should do their own due diligence regarding these requirements prior to implementation.**