FOR MESSRS:

SAMSUNG SDI

DATE: 03, 03, 2012

China STD

CUSTOMER'S SPECIFICATIONS

(Approval Edition)

108.89cm (43 Inch) Wide Plasma Display Module

MODEL : S43SD-YD01

(NTSC/PAL)

* This specification will be approved by both China STD and Samsung SDI Co.,Ltd.
* Please return one of this specification with your signature for approval.

Proposed by:

Approved by:

Signature _____

Signature _____.

Genral Manager. Changsub, Son

PDP Development Team,

PDP Business Division,

Samsung SDI Co., Ltd

SAMSUNG SDI CO.,LTD.

Revision History

No	Date	Description Of Changes	Rev. no	Approval
1				-
2				-

TABLE OF CONTENTS

1. DESCRIPTION

The S43SD-YD01 is a 43-inch wide full color plasma display Module with a resolution of 852(H) × 480(V) pixels. The display module includes the Plasma Display Panel, the Panel Driving Electronics, the Logic Control Board.

2. FEATURES

- Wide aspect ratio(16:9) 43 inch diagonal display screen. The display area is 945.94mm wide and 539.59mm high.
- Slim and light weight. The display Module is 49mm in depth and weight only approx. 10.0kg.
- 1073.7 million colors(10Bit), or 16.77 million colors(8Bit) combination of R,G and B digital data.(According to LVDS input selection)
- High Luminance, High contrast, Wide viewing angle. The screen has in Film **transmissivity 47.0%,** NTSC/PAL), contrast of typical 1000,000:1 (NTSC,PAL) And a viewing angle of greater than 160° comparable to that achieved

3. PRODUCT NAME AND MODEL NUMBER

- Product name : 43 inch Full Color Plasma Display Module (abbreviation : PDP Module)
- Model number : S43SD-YD01 (Project name : EV)
- Product Code : PP43SF003A

4. FUNCTION OUTLINE

- The plasma display module has an APC(Automatic Power Control) function which restricts power consumption within the certain value with regard to each display load ratio.
- The plasma display module is operated by following digital video signals; Vertical synchronous signal, Horizontal synchronous signal, Enable signal and 8~10bit data signals of each R, G and B color. All signals are based on LVDS level.
- The plasma display module is operated at 50Hz60Hz/100Hz frame rate. An external frame rate conversion is required in order to display the other formats.
- The plasma display module requires several types of input power voltages ; voltage for logic IC, voltage for Gate Driver, voltage for Sustain and voltage for Address.
- The plasma display module is operated at progressive signal only. An external progressive scan conversion is required in order to display the other formats.

5. BLOCK DIAGRAM

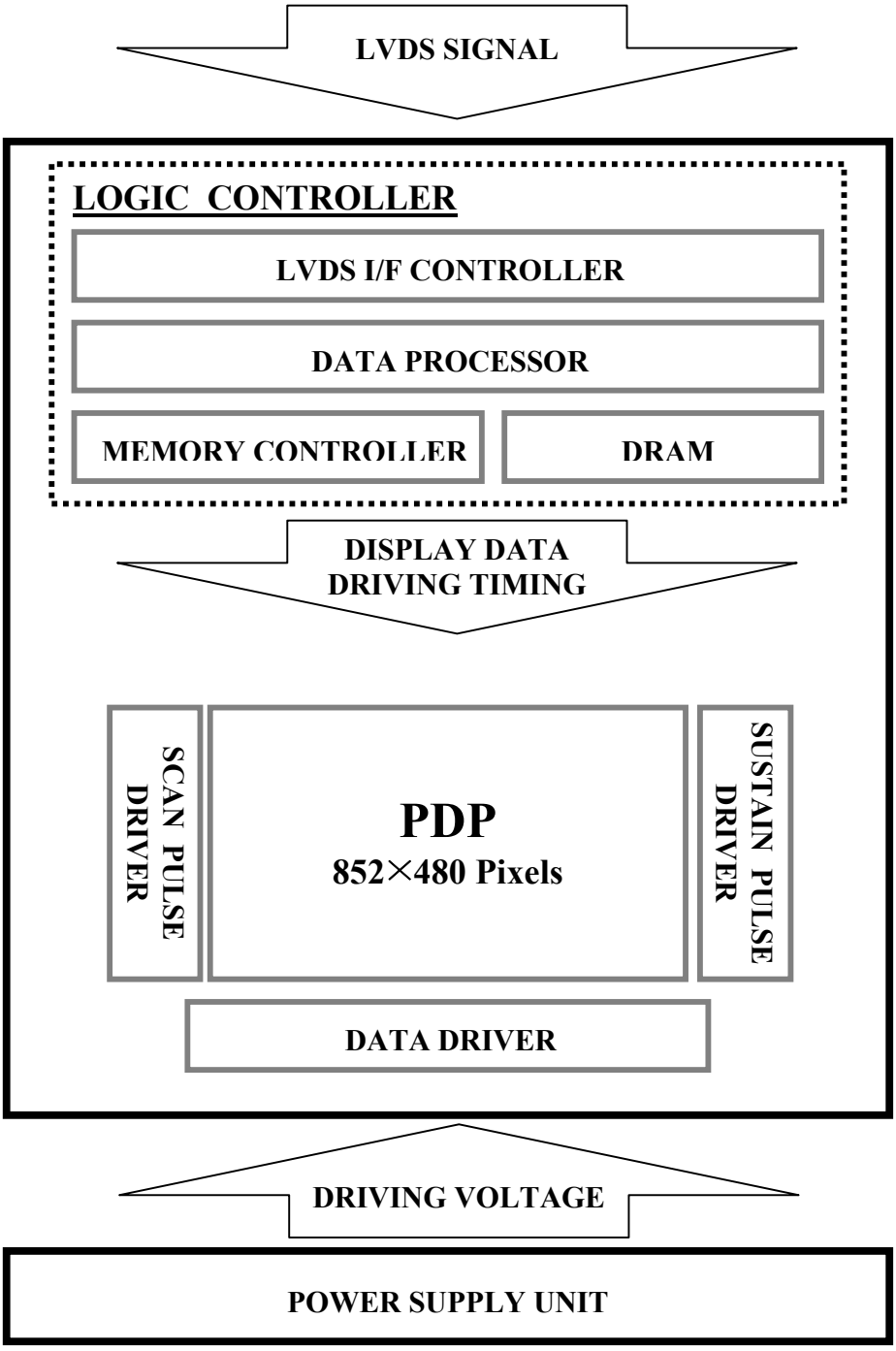


Figure-1. Block Diagram of PDP module

6. DISPLAY CHARACTERISTICS

6.1 Display Performance

No	Item	Rating	
1	Display Pixels	Horizontal 852 × Vertical 480 pixels (1 pixel = 1 R,G,B cells)	
2	Display Cells	Horizontal 2,556 × Vertical 480 cells	
3	Pixel Pitch	Horizontal 1110㎛ × Vertical 1124㎛	
4	Cell Size	R	Horizontal 370㎛ × Vertical 1124㎛
		G	Horizontal 370㎛ × Vertical 1124㎛
		B	Horizontal 370㎛ × Vertical 1124㎛
5	Pixel Type	R, G, B Non stripe (refer to Figure-2)	
6	Effective Display Size	Horizontal 945.94㎜ × Vertical 539.59㎜ [37.24 inch × 21.24 inch]	
7	Number of color	1073.7 million colors (10Bit) 16.77 million colors (8Bit)	
8	Contrast Ratio *1 (in dark room, peak algorithm on)	Typical 100,000:1	
9	Brightness (30% Load Brightness)	Typical 150cd/㎡	
10	Brightness (100% Load Brightness)	Typical 52cd/㎡	
11	Black Brightness (Normal mode)	Typical 0.06cd/㎡(NTSC), Typical 0.10cd/㎡(PAL)	
12	Viewing Angle *2	Over 160˚	

(Note)

*1. Contrast Ratio is calculated from the display Luminance and the non-display Luminance value. Display condition is shown in Figure-4.

*2. Viewing angle is a critical angle at which the Luminance is reduced to 50% to the Luminance perpendicular to the PDP Module. The Luminance is measured by a non-contact luminance meter MINOLTA CA-210.

6.2 Display Cell Arrangement

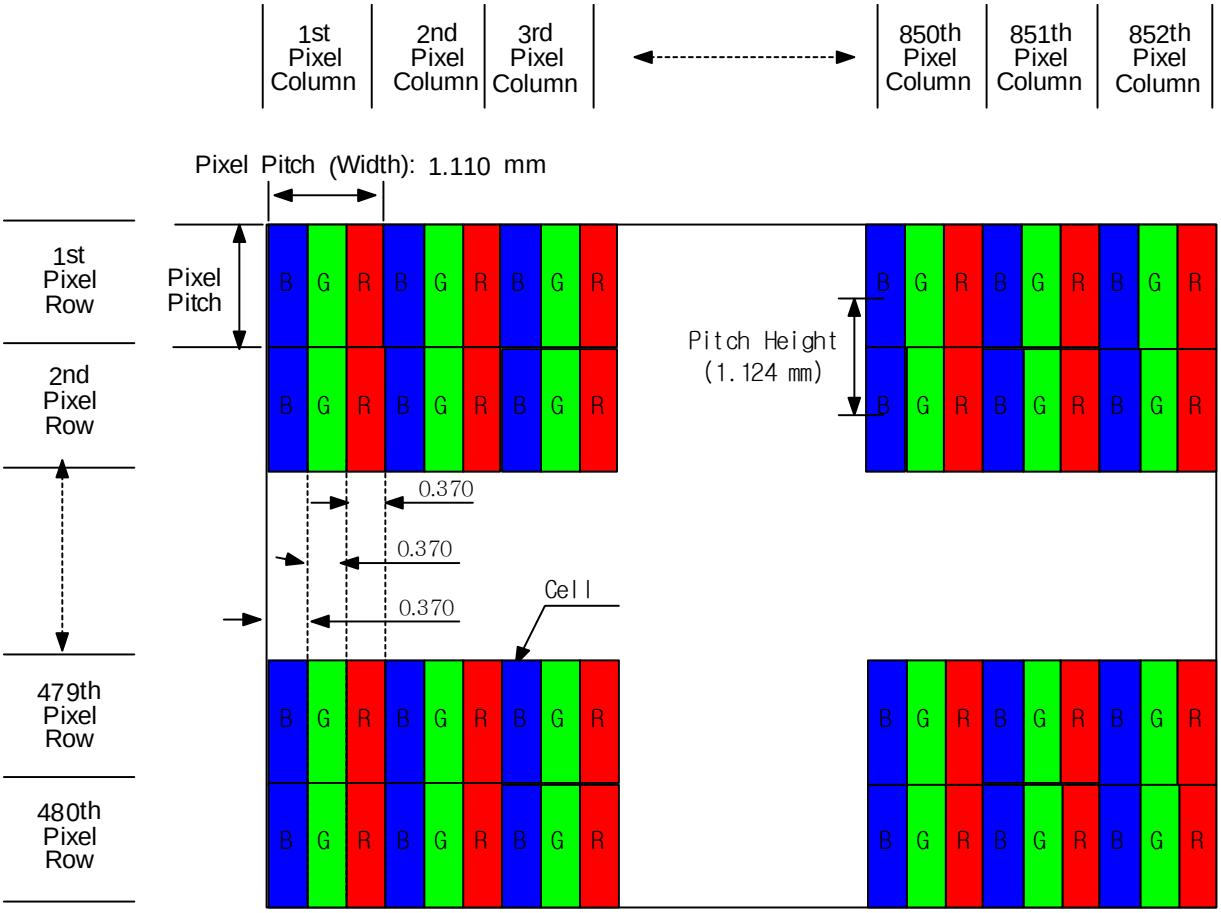


Figure-2.Display Cell Arrangement

6.3 Luminance Measurement Condition

(1) Display Pattern

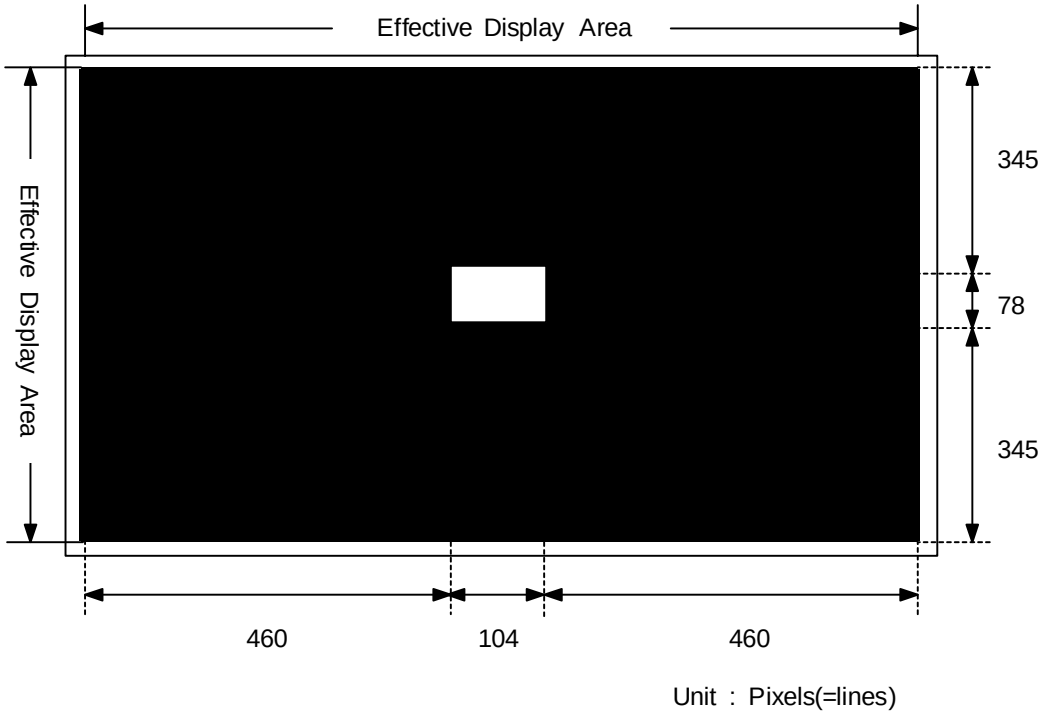


Figure-3. Display Pattern for Brightness & Contrast Ratio Measurement

(2) Display Area ratio : 1% white window
(3) Vsync : 16.7ms
(4) Measuring equipment : MINOLTA CA-210
Pattern Generator(VG-828, LVDS Output).
(5) Ambient Temperature : Room Temperature
(6) Ambient Luminance : Dark Room (<2 lux)

[Note]

1. Measurement is done within 30 seconds after Power On. The temperature of panel before measurement is room temperature (25℃).
2. Measurement is done within 3 seconds after Display Pattern(Figure-3) On

6.4 Contrast Measurement Condition

(1) Measuring point

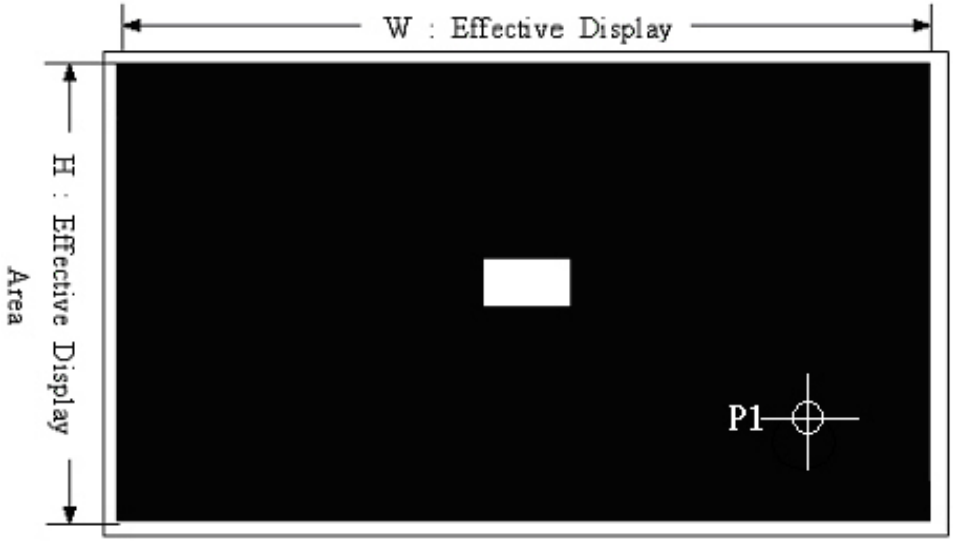


Figure-4. Measurement point

(2) Vsync : 16.7 ms
(3) Measuring Equipment : MINOLTA CA-210
Pattern Generator(VG-828, LVDS Output).
(4) Contrast Calculation formula

$$\text{Contrast ratio} = \frac{\text{Luminance of 1\% white window Area at the center of the screen}}{\text{Luminance of Black Area *1}}$$

【 Note 】

1. For mass production test purposes, it is recommended to measure just 1 point, P1 of Figure 4 on display pattern of Figure 3.
2. Measuring point _P1 is that minimum luminance point from among effective display area

(5) Ambient Light : Dark Room (<2 lux)

6.5 Display Cell Defect Specification

In some cases, a panel may have defective cells that cannot be controlled.
These defective cells can be categorized into three types;
(1) Non-lighting cell defect : defect in which the cell is always off
(2) Non-extinguishing cell defect : defect in which the cell is always on.
(3) Flickering cell defect : defect in which the cell is flickering.
(4) High intensity cell defect : defect in which the cell is brighter than other cells
(5) Test Pattern : Full White, Full Red, Full Green and Full Blue with 1024 gray level.

The display cell defect specifications define the allowed limits for display cell defects and
are used as the criteria in determining whether a panel should be shipped.

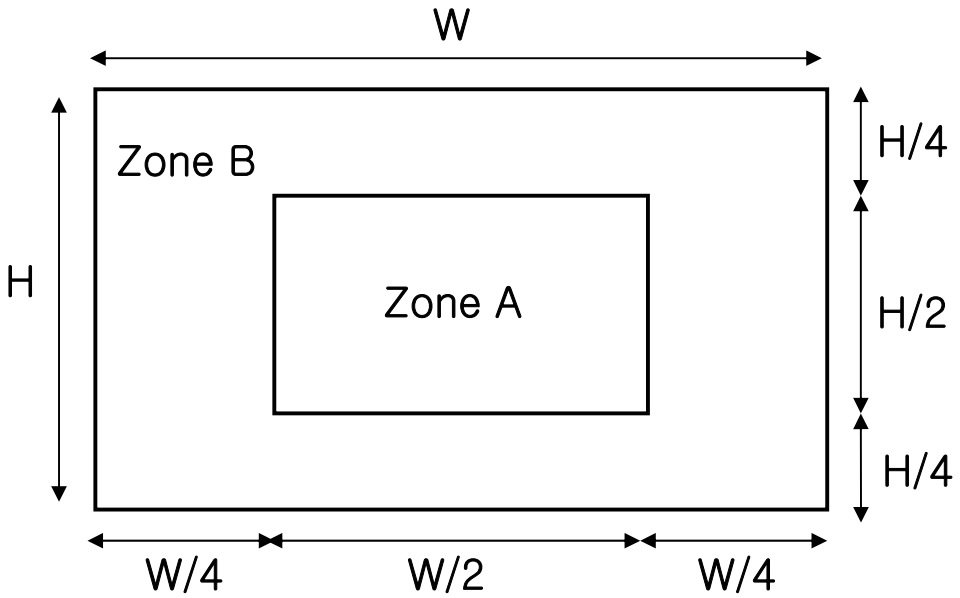


Figure-5. Measurement Area

Item	Number of cell defects		Remark
	A Zone	B Zone	
Non-lighting cell	3 and less	10 and less	Regardless of A and B Zone, Maximum 1 Cell Defect in an area of 50*50mm is allowed.
Non-extinguishing cell	1 and less	2 and less	
Flickering cell (the W/R/G/B screen)	2 and less	3 and less	
Flickering cell (the other pattern)	1 and less	2 and less	
High Intensity Cell	1 and less	2 and less	
Continuous Cell	1 and less	1 and less	
Total defect	14 and less		

6.6 Uniformity Specifications

The color-PDP uses ultraviolet light produced by gas discharge to illuminate phosphor. Uneven phosphor coating and inconsistent discharge characteristics cause slight difference in brightness among the sections in a panel.

Item	Definition	Specification
Full white brightness variation	The brightness is measured at 9 points (A1~A9 of Fig-6) on full white pattern. The full white brightness variation as then calculated from the following equations.	15% and less
Equation	$\frac{Max - \bar{x}}{\bar{x}} \times 100\%$ & $\frac{\bar{x} - Min}{\bar{x}} \times 100\%$	

The brightness variation specifications define the allowed limits for brightness differences and the criteria in determining whether a panel is shipped.

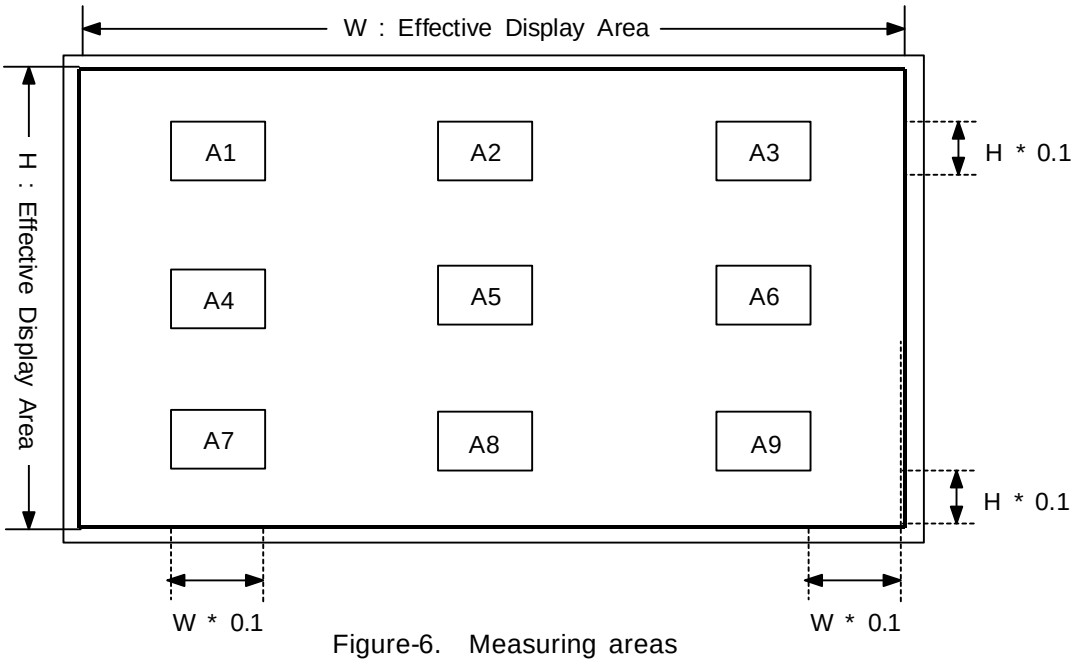


Figure-6. Measuring areas

6.7 Power consumption

6.7.1 APC (Automatic Power Control) Function

The PDP has an APC (Automatic Power Control) function for the panel driver power source. When the total display load ratio exceeds approximately 10%, total power consumption is limited within a specified level (=Lower Power Limit) by APC function.
The operation behavior of APC function is called as SLOW-APC. When the display load-ratio changes from low to high value, the power-consumption rises instantly to "Upper Power Limit" and gradually decreases until it reaches to the "Lower Power Limit."
[Note] Number of steps may Power vary as a function of the load ratio.

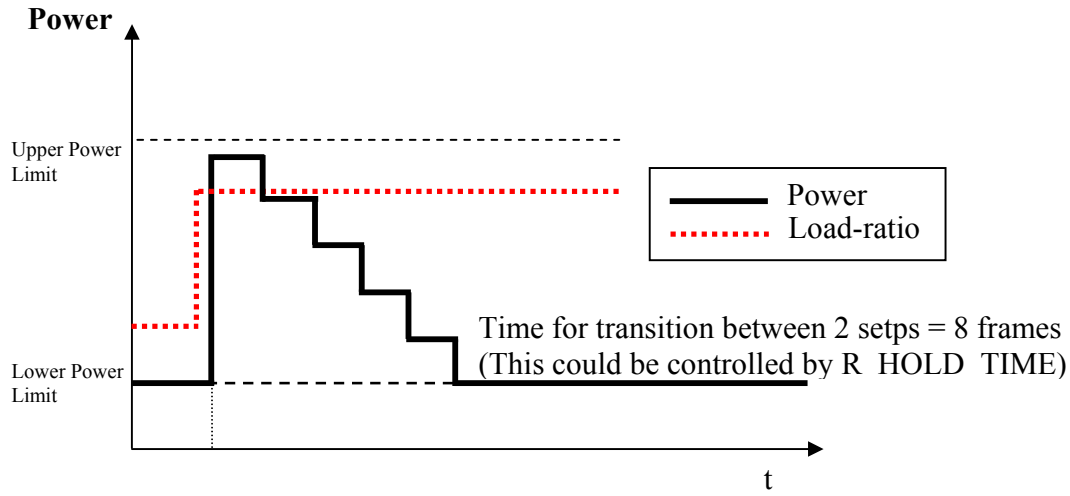


Figure 7. Slow APC Behavior

6.7.2 Brightness and Power Mode Control

This PDP module offsers two methods for Brightness and Power mode control.
One is APCO(APC Offset) for Peak-Brightness control, and the others are PUG and PLG
for power mode control. APCO, PUG and PLG are registers controllable through I2C communication from image B'd. For a detailed address and data bits of these registers , refer to the Chapter 11. Address Map.
(1) Peak-Brightness Control(APCO)
- controls the max.sustain number
- APCO variable range : 0010h~01FFh (cf. 00C8h~01F4h @3D Mode)

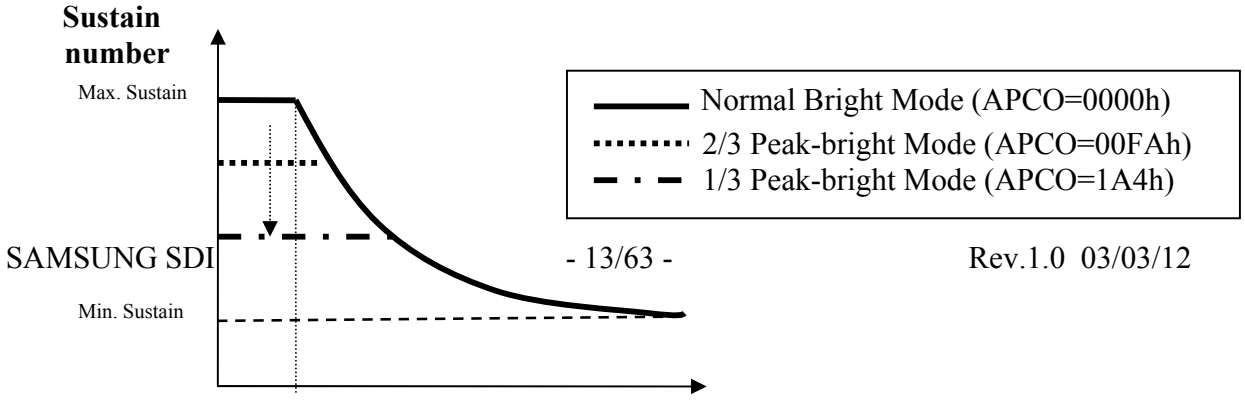


Figure-8. APCO Behavior

(2) ASLG (Power-Mode Control using ASL gain function)

- ASLG variable range : 80~FFh
- Maximum available power decrease by increasing ASLG above 80h(NTSC)

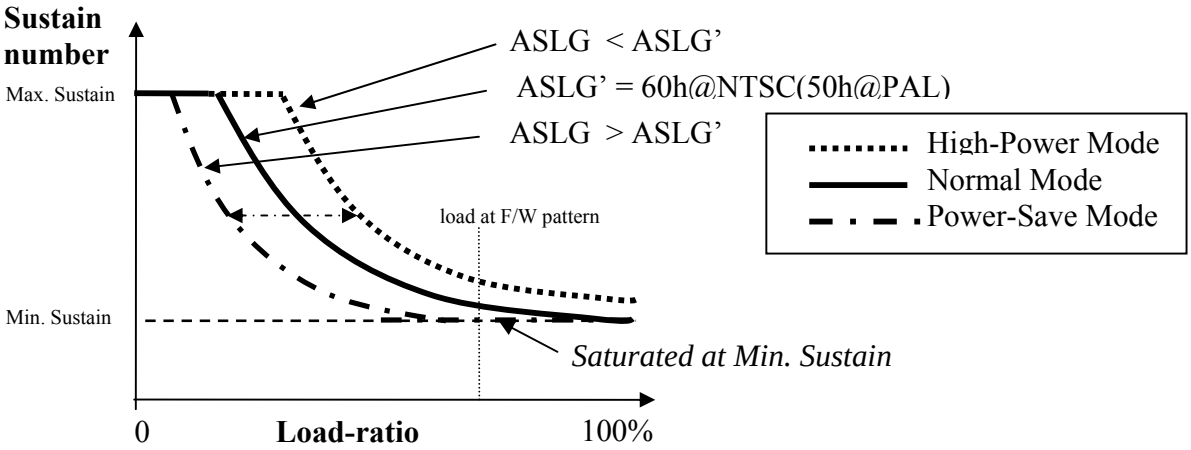


Figure-9. ASLG Behavior

(3) Power-Mode Control (PLG)

- PLG(Power Lower Gain control register)
- Variable range : 00h ~ FFh(Tentative) , Default Value : 80h
- PLG is for lower power level.
- PLG value : smaller than the default in order to make less power consumption.

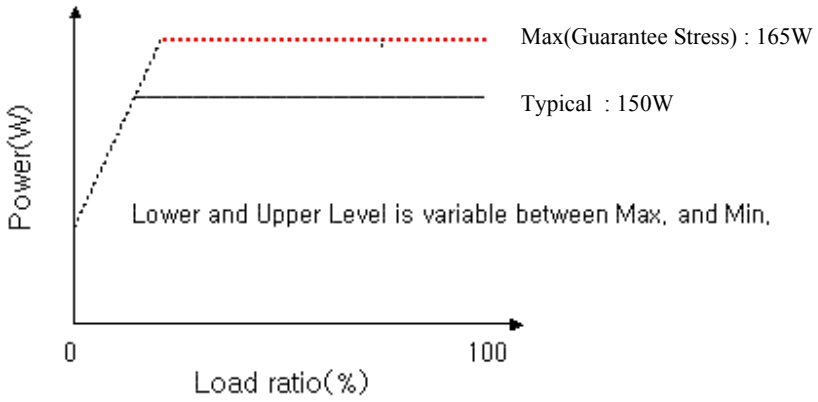


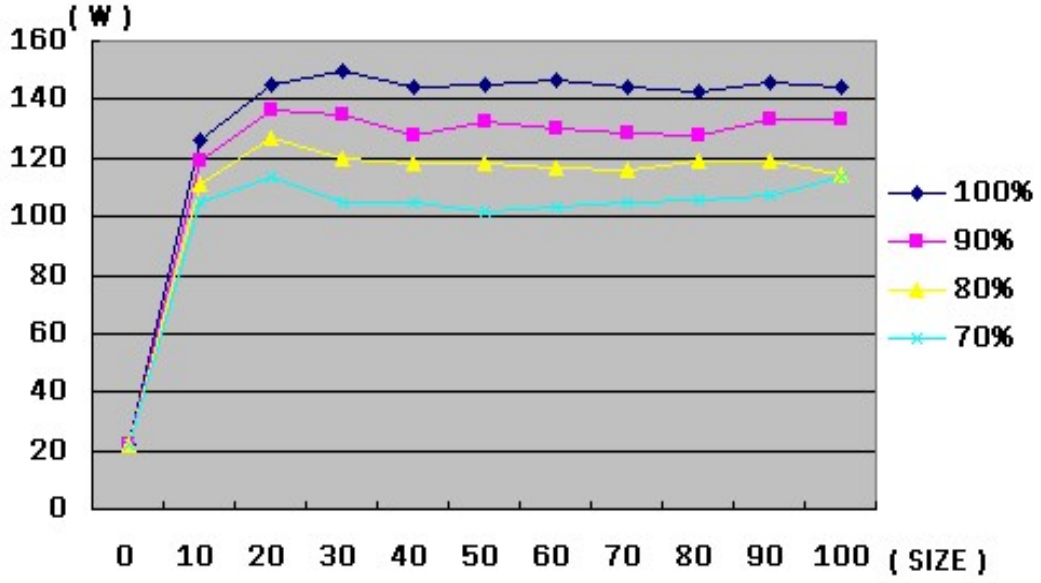
Figure-10. APCL Behavior(PLG Adjust,F/W Pattern)

(4)Power- Consumption Ratio(BY ASLG, PLG)

PLG	ASLG	ASLG_SW	Power- Consumption Ratio
80	80	OFF	100%
73	80	OFF	90%
6A	87	ON	80%
6A	A2	ON	70%

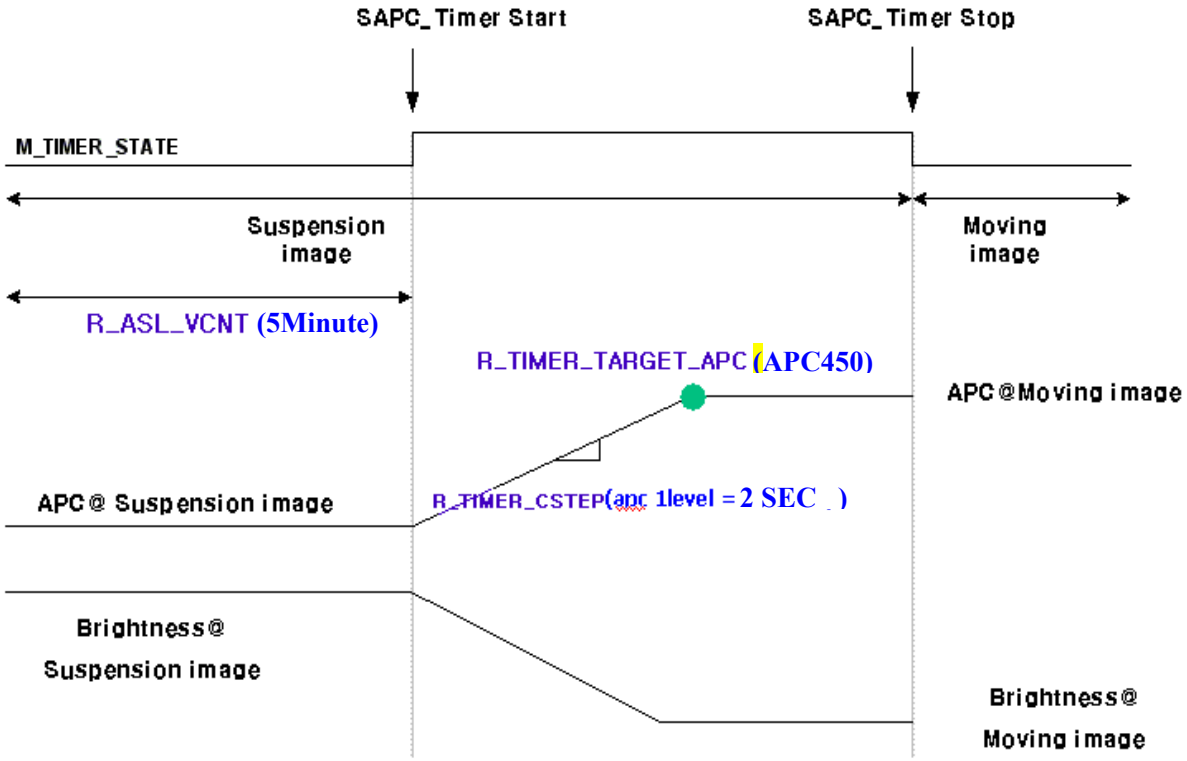
【 Note 】 Condition By Moving Picture(30% Window Size)

Figure 11. Power- Consumption Ratio ByWindowsize(Load)



(5) SAPC_Timer

The module is equipped with the APC Timer function to reduce the amount of image retention. If the input image is not varying for at least one minutes, the fuction starts to operate and reduce the intial APC level one step down to a predefined target level in every three seconds. The fuction is immediately turned off when the input image starts varying.



6.8 Gamma characteristics

6.8.1 Basis of Gamma Curve

This PDP module is normally applied to the 2.2 gamma curve (refer to Figure-12)
But this specification could be modified on the request of the customer

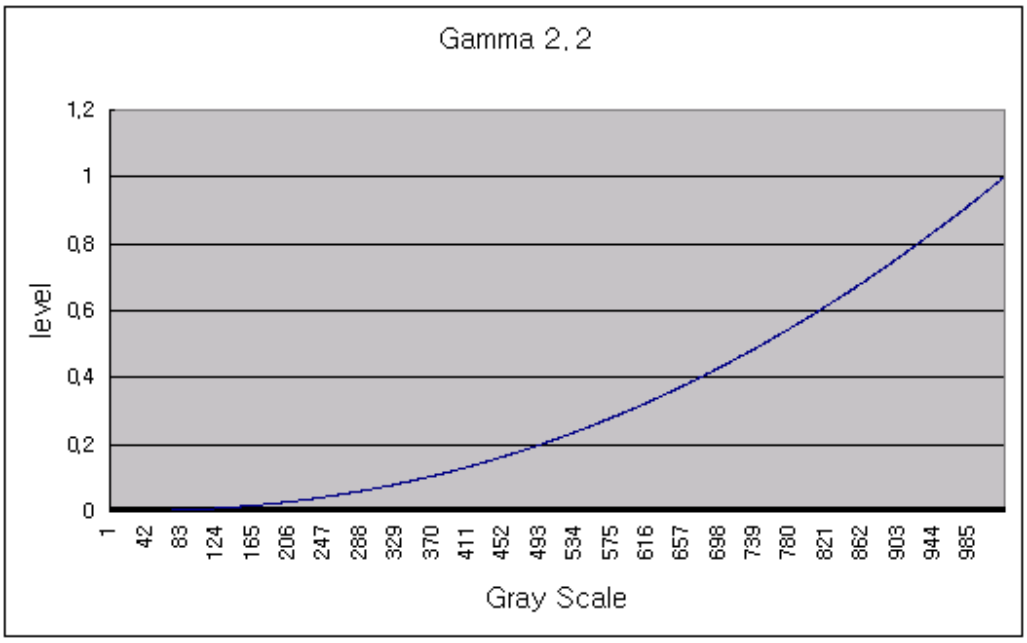
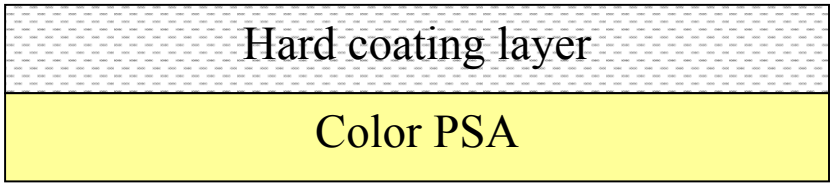


Figure-12. Default Gamma Curve

6.9 Film filter

6.9.1 Structure of the PDP FF

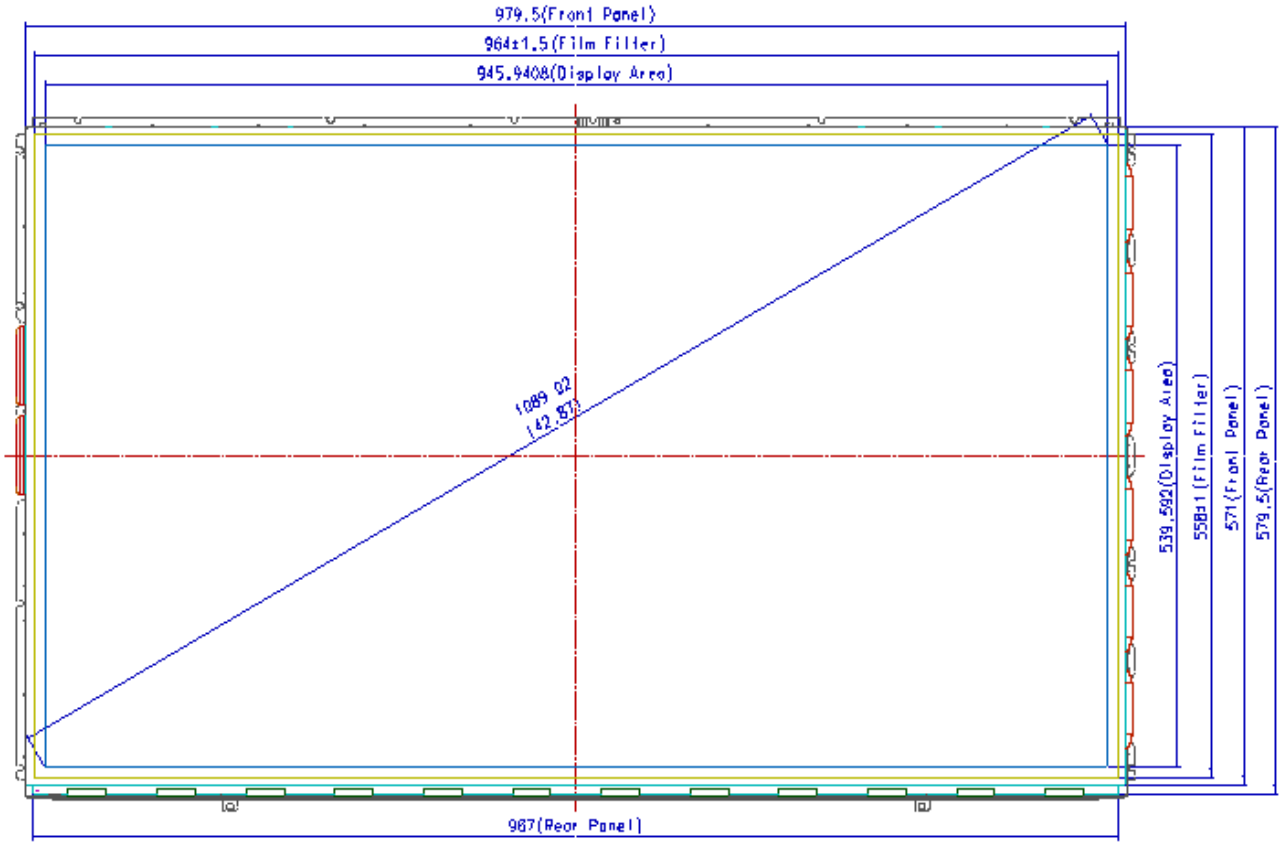


Film **transmissivity 47%**

6.9.2 Characteristics of the PDP FF

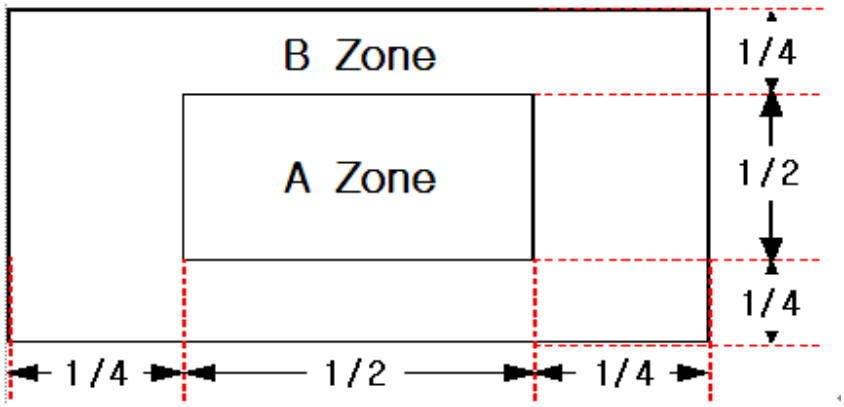
(1) Attached with a Hard coating film on the View side.
(2) Attached with a Near Infrared (NIR) cut off function in the Color PSA to shield them.

6.9.3 Dimension Specifications



6.9.4 Film Filter Defect specifications

<table>
<tr><th>Items</th><th colspan="4">Specification</th></tr>
<tr><td rowspan="4">Point Defects</td><td colspan="2" rowspan="2">Point Defects Size (mm)</td><td colspan="2">Allow Defects</td></tr>
<tr><td>Area A</td><td>Area B</td></tr>
<tr><td colspan="2">φ<0.5</td><td colspan="2" rowspan="2">unlimited</td></tr>
<tr><td colspan="2">0.5≤φ<1.0</td></tr>
<tr><td colspan="2">1.0≤φ≤1.5</td><td>1</td><td>2</td></tr>
<tr><td colspan="2">1.5< ø</td><td colspan="2">none</td></tr>
<tr><td rowspan="6">Linear Defects</td><td colspan="2">Linear Defects Size (mm)</td><td colspan="2">Allow Defects</td></tr>
<tr><td>Width</td><td>Length</td><td>Area A</td><td>Area B</td></tr>
<tr><td>0.1≤W<0.15</td><td>10<L≤20</td><td>0</td><td>5</td></tr>
<tr><td>0.05≤W<0.1</td><td>10<L≤20</td><td>3</td><td>5</td></tr>
<tr><td>0.05≤W<0.1</td><td>L<10</td><td rowspan="2">10</td><td rowspan="2">20</td></tr>
<tr><td>W<0.05</td><td>10<L≤20</td></tr>
<tr><td colspan="2">W<0.05</td><td>L<10</td><td colspan="2">35</td></tr>
<tr><td colspan="5">* Distance between defect ≧30 ㎜</td></tr>
</table>



[Note]

1. When power off the defect is the appearance NG.
2. When power Colored defects treated Cell defect specification Management.

6.10 White Balance

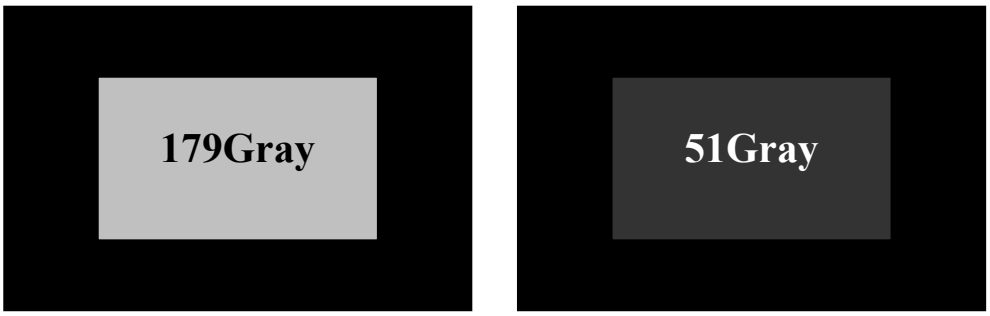


Figure. Measurement pattern(30% Window)

(2) Measuring condition : After 1hour aging , 50℃
(3) Measuring Equipment : MINOLTA CA-210
Pattern Generator(VG-828, LVDS Output).
(4) Ambient Light : Dark Room (<2 lux)
(5) Default data

	ΔX	ΔY	Luminance
51Gray	0.278	0.285	20.8
179Gray	0.278	0.285	108

(6) Specification

Type	ΔX	ΔY	T
M1	0.285	0.290	9,500
M3F (With filter)	0.278	0.285	10,500

7. SOUND PRESSURE LEVEL SPECIFICATION

7.1 Measuring Condition

(1) Background noise level : less than 20dBA under anechoic chamber environment
(2) Pattern : Full White
(3) Equipment : FFT Analyzer
- PULSE Analyzer Type 3560C made by B&K or,
- PAK System v5.3 above made by MÜLLER-BBM

(4) Distance : 1 m from the center of rear side of PDP Module (M3)
(5) Bandwidth : ⅓ octave band, Weighting Filter : A-weighting

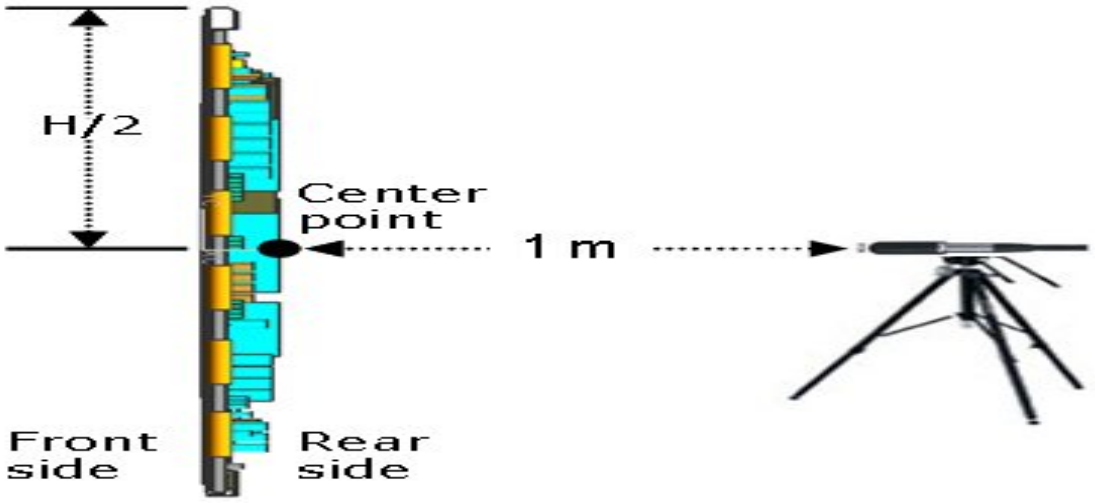


Figure-13. Measuring Point

7.2 Sound Pressure Level

7.2.1 Level Ground (Land)

- Measuring Condition : 0 m
- Sound Pressure Level is overall level calculated from the individual band levels of 250Hz ~ 8kHz.
- Specification : 31.xx dB max.

7.2.2 High Ground

-. Measuring Condition : 1,600 meter
-. Sound Pressure Level is overall level calculated from the individual band levels of 4 kHz ~ 12.5 kHz.
-. Specification : 28.xx dB max.

【 Note 】

[Note]

1. SDI recommends that the back cabinet of a TV has the ventilation holes of less than 2.7 mm in diameter.
2. Audible noise is guaranteed till the altitude of 1,600 meter.
3. In order to guarantee audible noise at higher altitude than 1,600 meter, a special module has to be used.

※ Overall value is calculated as follows,

$$\text{Overall(dB)} = 10\log_{10}\left(10^{\frac{dB_{@250Hz}}{10}} + 10^{\frac{dB_{@315Hz}}{10}} + \cdots + 10^{\frac{dB_{@8kHz}}{10}}\right)$$

$$dB_{@Freq.} = 20\log_{10}\left(\frac{P}{P_0}\right) \text{where, } P_0 = 20\times10^{-6}\text{Pa}$$

8. MECHANICAL CHARACTERISTICS

8.1 Mechanical Specifications

No	Item	Rating
1	Outer Dimension	Width 995.5±2 mm × Height 593.6±2 mm × Thickness 47.28±2mm (include FPC and TCP) *see Appendix : Mechanical Dimension Drawing
2	Weight	Approximatly 10 kg(Without SMPS)

8.2 Mechanical Characteristics

No	Item	Rating
1	Vibration	Frequency : 0 ~ 256 Hz Sweep Rate : 1 Octave/min Acceleration Value : 0.85Grms Duration Time : 1.5 hr
2	Module drop	Panel not broken in less than 10cm.(3 pcs)
3	Torsion	Panel not broken in less than 20kgf.(3 pcs)

* Notes: (Test condition) Non-Packaging, Operational (only for Vibration)
* Test time of Vibration Test is 30 minutes every direction(x,y,z)

9. ENVIRONMENTAL CONDITIONS

9.1 Operational Environmental Condition

No	Item	Rating	
1	Ambient Temperature	Function Operation	-5℃ ~ 60℃
		Temperature Slope	Below 1.5 ℃/minute
2	Panel Surface Temperature *3	Small Size Pattern Full White Pattern	~ 120 ℃ ~ 85 ℃
		Temperature Slope	Below 20 ℃/cm
3	Humidity	Function Operation	20 ~ 80 RH (no condensation)
4	Pressure	Function Operation	717 ~ 1,013 hPa (0 ~ 2,800 m)

[NOTE]

1. Functional Operation means that the PDP module is operated only its electrical function.
2. Panel Surface Temperature means the surface temperature of panel that is just increased due to the loss of power inside Panel during the image display at a normal display mode and a ambient temprature defined in this table.
   The judgement of display defects (e.g. weak discharge, missing discharge) should be done when the panel is operated at a ambient temperature defined in this table.

9.2 Storage Environmental Condition *1

No	Item	Rating
1	Ambient Temperature	-20℃ ~ 70℃
2	Humidity	5 ~ 95 RH (no condensation)
3	Pressure	1,013 ~ 307hPa (0~10,000m)

[NOTE]

1. Storage means the short term period. (e.g. transportation, relocation and so on)

9.3 Panel Surface Condition

9.3.1. Panel surface temperature specification

The panel surface temperature should be kept as below in order to get stable display of image.

- Tp= below 120℃ (Absolute Maximum Rating); when small size of image is displayed
- Tp= below 85℃; when Full White is displayed.

If the temperature exceeds above level, it may cause the defects of display image like dot missing, line missing and/or poor image. As the surface temperature of panel has tendency to rise with deduction of display rate, the relation with temperature can be describe as below :

85℃ (display load rate is high : large area) ~ 120℃ (display load rate is low : small area)

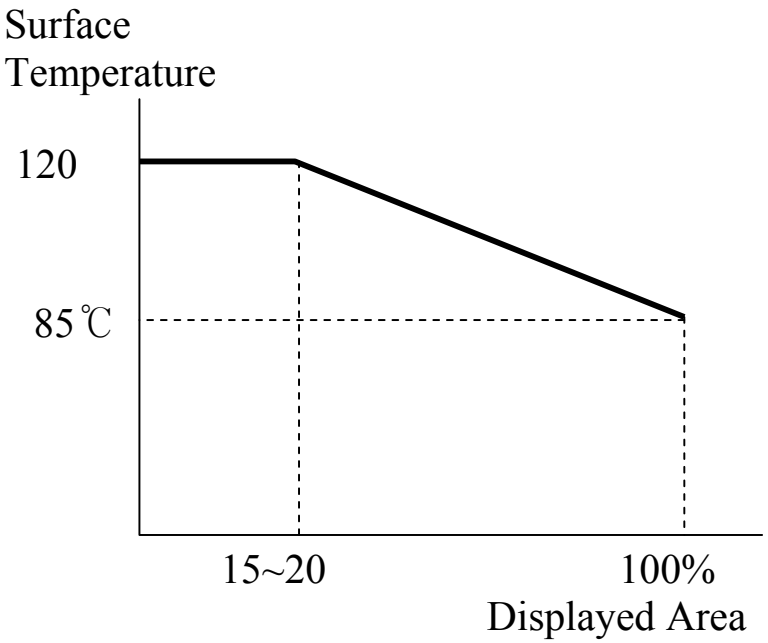


Figure-14. Surface Temperature Vs Displayed Area

It is strongly recommended that the panel surface temperature should be kept as low as possible, eventhought its maximium rating is descreibed as above.

9.3.2. Panel Surface Temperature for Breaking

The temperature uniformity across panel should be maintained below 20℃/㎝ not to occure panel breaking by temperature difference.

This breaking temperature is not absolute temperature, because it depends on condition of panel production and panel scratch. Please take this value as a reference.

9.3.3. Panel Surface Temperature specification for Conditin of Stable Moving Image

- Tm= below 50℃(Whole Displayed Area, SET State)

10. INTERFACE SIGNAL SPECIFICATIONS

10.1 Configuration Context

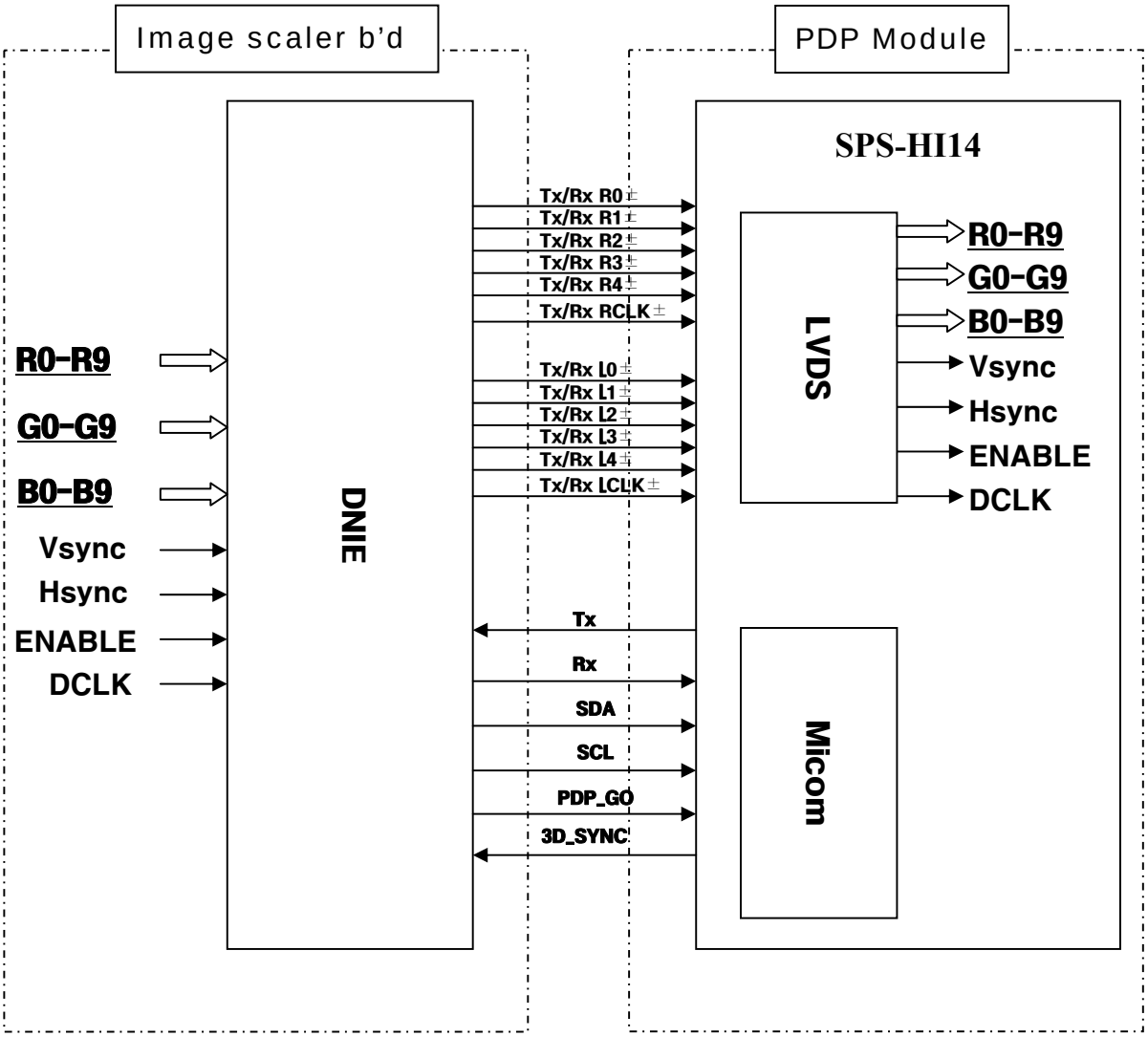


Figure-14. Interface Block Diagram

10.2 Interface Function Specifications (input data and display processing)

- 852x480-dot data signals are inputted to this product to display data.
- The Video signal and control signal input section uses a low voltage differential signaling (LVDS) interface.
- An I2C bus serial data interface is used for the communication between MPU of FTV side and the CLU (Control LOGIC Unit) of this PDP Module.

10.3 Input Signal Definition

No	Item	Signal name		Q	I/O	Method	Definition
1	Display Signal	Video Signal	Rx_IN R0± Rx_IN R1± Rx_IN R2± Rx_IN R3± Rx_IN R4± Rx_IN L0± Rx_IN L1± Rx_IN L2± Rx_IN L3± Rx_IN L4±	2 2 2 2 2 2 2 2 2 2	Input	LVDS Differentials	Differential serial data signal. Input video and timing signals after differential serial conversation using a dedicated transceiver. The serial data signal is transmitted seven times faster than the base signal.
		Dot Clock	Rx_CLK RIN± Rx_CLK LIN±	2 2	Input	LVDS Differential	Differential clock signal. Input the clock signal after differential conversation using a dedicated transceiver. The clock signal is transmitted at the same speed as the base signal.
2	MPU Communication	Communication	SDA SCL PDP_GO Rx Tx 3D_SYNC	1 1 1 1 1 1	Input Input Input Input Output Output	LVTTL(I2C) LVTTL(I2C) LVTTL UART UART LVTTL	I2C bus serial data/Uart bus serial data communication signal. Communication with the CLU (Control Logic Unit) of this product is enabled. *3D_SYNC : 3D Mode Control

10.4 LVDS Signal Definition and Function

A video signal (display data signal and control signal) is converted from parallel data to serial data with the LVDS transmitter and further converted into four sets of differential signals before inputted to this PDP Module. These signals are transmitted seven times faster than the dot clock signals. The dot clock signal is converted into one set of differential signals.
The LVDS signal definitions and functions are described as follows: (LVDS Default is 10Bit)

10.4.2 10 BIT Application

Table 2. Input signal definition and pin assignments of LVDS Receiver (10 Bit)

Signal	I/O	Function	Remarks
Rx_IN R0-/ Rx_IN L0-	I	Display Data Signal: R2, R3, R4, R5, R6, R7, G2	
Rx_IN R0+/ Rx_IN L0+	I		
Rx_IN R1-/ Rx_IN L1-	I	Display Data Signal: G3, G4, G5, G6, G7, B2, B3	
Rx_IN R1+/ Rx_IN L1+	I		
Rx_IN R2-/ Rx_IN L2-	I	Display Data Signal: B4, B5, B6, B7, Hsync, Vsync, DEN	
Rx_IN R2+/ Rx_IN L2+	I		
Rx_IN R3-/ Rx_IN L3-	I	Display Data Signal: R8, R9, G8, G9, B8, B9,reserved	
Rx_IN R3+/ Rx_IN L3+	I		
Rx_IN R4-/ Rx_IN L4-	I	Display Data Signal: R0, R1, G0, G1, B0, B1,N/C	
Rx_IN R4+/ Rx_IN L4+	I		
Rx_CLK RIN- Rx_CLK LIN-	I	Dot Clock Signal: CLK	
Rx_CLK RIN+ Rx_CLK LIN+	I		

10.4.3 8 BIT Application

Table 3. Input signal definition and pin assignments of LVDS Receiver (8 Bit)

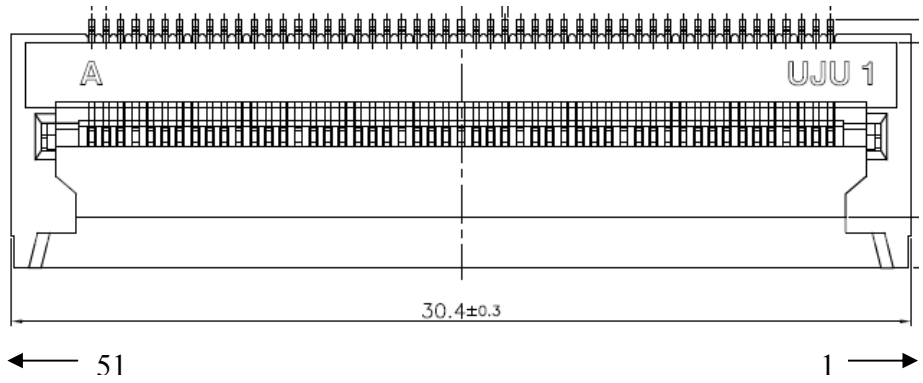
Signal	I/O	Function	Remarks
Rx_IN R0-/ Rx_IN L0-	I	Display Data Signal: R0, R1, R2, R3, R4, R5, G0	
Rx_IN R0+/ Rx_IN L0+	I		
Rx_IN R1-/ Rx_IN L1-	I	Display Data Signal: G1, G2, G3, G4, G5, B0, B1	
Rx_IN R1+/ Rx_IN L1+	I		
Rx_IN R2-/ Rx_IN L2-	I	Display Data Signal: B2, B3, B4, B5, Hsync, Vsync, DEN	
Rx_IN R2+/ Rx_IN L2+	I		
Rx_IN R3-/ Rx_IN L3-	I	Display Data Signal: R6, R7, G6, G7, B6, B7,reserved	
Rx_IN R3+/ Rx_IN L3+	I		
Rx_CLK RIN- Rx_CLK LIN-	I	Dot Clock Signal: CLK	
Rx_CLK RIN+ Rx_CLK LIN+	I		

10.5 LVDS Signal Pin Assignment

The table below indicates pin assignment of the LVDS IC(Transmitter & Receiver).
In the 10bit input mode, for other input bit mode, refer to technical references

Table 4. Pin assignment of receiver

PIN No	PIN NAME	PIN No	PIN NAME	PIN No	PIN NAME
1	GND	18	GND	35	Rx_CLKINL-
2	UART_Tx	19	Rx_CLKINR+	36	GND
3	GND	20	Rx_CLKINR-	37	Rx_IN_L2+
4	SDA	21	GND	38	Rx_IN_L2-
5	GND	22	Rx_IN_R2+	39	Rx_IN_L1+
6	SCL	23	Rx_IN_R2-	40	Rx_IN_L1-
7	GND	24	Rx_IN_R1+	41	Rx_IN_L0+
8	UART_Rx	25	Rx_IN_R1-	42	Rx_IN_L0-
9	GND	26	Rx_IN_R0+	43	GND
10	GND	27	Rx_IN_R0-	44	GND
11	GND	28	GND	45	GND
12	NC	29	Rx_IN_L4+	46	GND
13	GND	30	Rx_IN_L4_	47	GND
14	Rx_IN_R4+	31	Rx_IN_L3+	48	GND
15	Rx_IN_R4-	32	Rx_IN_L3-	49	3D_SYNC
16	Rx_IN_R3+	33	GND	50	GND
17	Rx_IN_R3-	34	Rx_CLKINL+	51	GND



YEONHO (UJU) 51P LVDS Connector (Top View)

10.6 Video Signal Definition and Function

The table below indicates the definitions and functions of input video signals before LVDS conversion.

Interfaces Signal Functions		
Symbol	**Function**	**Remarks**
R9(7) to R0	10(8) bits red video signal (note 1)	Display data signal: R9(7): MSB*, R0: LSB**
G9(7) to G0	10(8) bits green video signal (note 1)	Display data signal: G9(7): MSB*, G0: LSB**
B9(7) to B0	10(8) bits blue video signal (note 1)	Display data signal: B9(7): MSB*, B0: LSB**
Hsync	Horizontal synchronous signal	This signal specifies the data period for one horizontal line. Control of the next line begins at the rising edge of Hsync.
Vsync	Vertical synchronous signal	Timing signal that controls the start of the screen. Control of the next screen begins at the rising edge of Vsync.
DEN	Data Enable	Valid data enable signal
DCLK	Clock for video signal	Latch the video signal at falling edge.

* MSB: Most Significant Bit
**LSB: Least Significant Bit

Note 1: The RGB signal may be compensated with Inverse γ circuit [Halftoning Algorithm (Error Diffusion, Dither) must be included] before inputted to the PDP Module. In order to obtain good characteristic of low level's gray scale, inverse γ correction and E/D process are advisory to be performed after inputted to the PDP Module.

10.7 Electrical Condition of Interface Signal

10.7. 1. Maximum Ratings

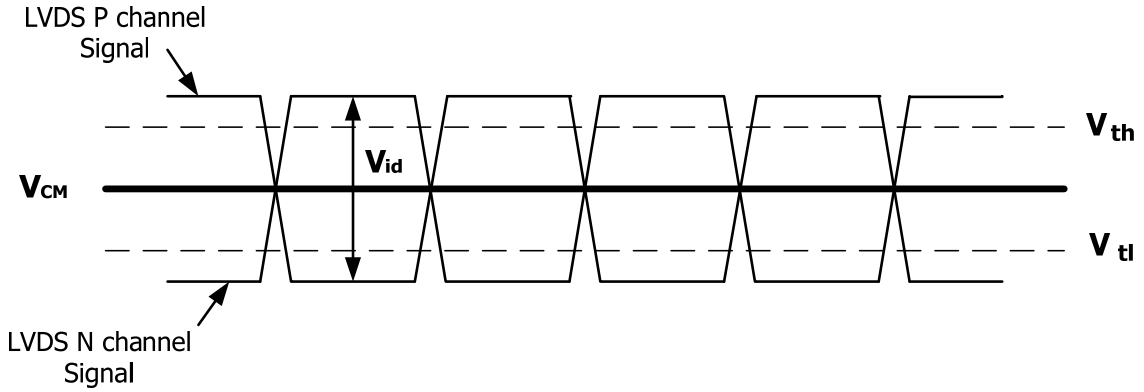
Common conditions : Ta = 25℃, Vcc = 3.3V

Absolute Ratings						
Item			**Parameter**	**Symbol**	**Ratings**	**Module**
Input Signals	LVDS	Rx_IN_R0-/+, Rx_IN_R1-/+ Rx_IN_R2-/+, Rx_IN_R3-/+ Rx_IN_R4-/+, Rx_CLKINR-/+ Rx_IN_L0-/+, Rx_IN_L1-/+ Rx_IN_L2-/+, Rx_IN_L3-/+ Rx_IN_L4-/+, Rx_CLKINL-/+	**Input Voltage**	**Vi**	**-0.3~ 3.6**	**V**
			Input Current	**Ii**	**-10~10**	**㎂**
	3.3V CMOS	SDA, SCL	Input Voltage	Vi	**-0.5~3.5**	V
			Input Current	**I**i	**8**	**㎃**

10.7. 2. Electrical Characteristics

Common conditions : Ta = 25℃, Vcc = 3.3V

Electrical Characteristics							
Signal	**Item**	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Module**
LVDS	Differential input high threshold voltage	V_{th}	V_{CM}=1.2V	-	-	+100	mV
	Differential input low threshold voltage	V_{tl}	V_{CM}=1.2V	-100	-	-	mV
	Differential Input Voltage	Vid		100		600	mV
	Common Mode Voltage	V_{CM}	Vid = 100mV	0.2	1.2	2.2	V
	Input current	I_{in}	V_{IN} = +2.4V/0V Vcc = 3.6V	-	-	±20.0	μA
I2C	Input Voltage	V_{ih}		0.7*Vcc	-	3.5	V
		V_{il}		-0.5	-	0.8	V
	Input Capacitance	V_{in}	-	-	-	8	pF
	Output Voltage	V_{oh}	I_{oh} = 8 mA	2.4	-	-	V
		V_{ol}	-	-	-	0.8	V
	Output Current	I_{ol}	-	-	-	8	mA
Vs_On 3D_SYNC	High level input voltage	V_{ol}	-	2.4	-	-	V
	Low level input voltage	I_{ol}	-	-	-	0.3*Vcc	V
PS_ON	High level input voltage	V_{ih}	-	2.5	-	3.5	V
	Low level input voltage	I_{il}	-	-0.5	-	0.3*Vcc	V



If above specifications are not meet, the output could be an abnormal Data

10.8 Video Signal Interface Timing Conditions

The table below indicates the conditions of input video signal before LVDS conversion. These conditions must be satisfied. Refer to the figure of the timing chart.

HSYNC must be risen up within 1 clock after the rising edge of VSYNC.

8 bits LVDS ~10 bit LVDS belong to one timing table below.

Video Input Signal Timing (NTSC/PAL)							
ITEM	**SYMBOL**		**Min**	**Typ**	**Max**	**Units**	**Remarks**
DCLK	Period	T_{clk}	14.08	13.50	12.82	ns	
	Frequency		71.2	74	78	MHz	
Hsync	Period		20.0	20.32	-	us	
	Frequency	F_h	50.25	49.26	-	KHz	
	Width	T_{wh}	6	10	-	T_{clk}	
Vsync	Period	T_{vp}	794/947*	820/984*	895/1094*	T_{hp}	NTSC/PAL
	Frequency	F_v	62/52	60/50	55/45	Hz	NTSC/PAL
	Width	T_{wv}	2	6	10	T_{hp}	
Data Enable	Horizontal Valid	T_{hv}	852	852	852	T_{clk}	
	Horizontal Back Porch	T_{hbp}	56	76	-	T_{clk}	
	Horizontal Front Porch	T_{hfp}	-	-	-	T_{clk}	
	Vertical Valid	T_{vv}	480	480	480	T_{hp}	
	Vertical Back Porch	T_{vbp}	20	30	-	T_{hp}	
	Vertical Front Porch	T_{vfp}	8	-	-	T_{hp}	NTSC/PAL

* Hsync period :
  - Min : 20.0 us (1480Tclk @DCLK 74MHz)
  - Typ : 20.32 us (1504 Tclk @DCLK 74MHz)
* Vsync Period :
  - Min : 794/947 (@Hsync Period : Typ value)
  - Typ : 820/984 (@Hsync Period : Typ value)
  - Max : 895/1094(@Hsync Period : Typ value)

Tvsync :
- PAL Long Mode : Below 48Hz
- PAL Normal Mode : 48~52Hz
- PAL LB Mode : 52~55Hz
- NTSC Long Mode : 55 ~ 58 Hz
- NTSC Normal Mode : 58 ~ 62 Hz
- NTSC LB Mode : 62 ~ 65 Hz
- NTSC Mask Mode : above 65 Hz

* LB Mode(=Low Brightness Mode) : By decreasing sustain period on the Tvsync shorter than normal, brightness is reduced.
* 1`Mask(or Flicker) Mode : Masks abnormally short Vsync, and displays at the frame period twice as input Vsync period.
* Long Mode : mode change is not occurred in this period, the display is normally operation by increasing the Vsync period.

10.9 LVDS Interface Timing Conditions

This PDP Module uses an LVDS interface for the signal input

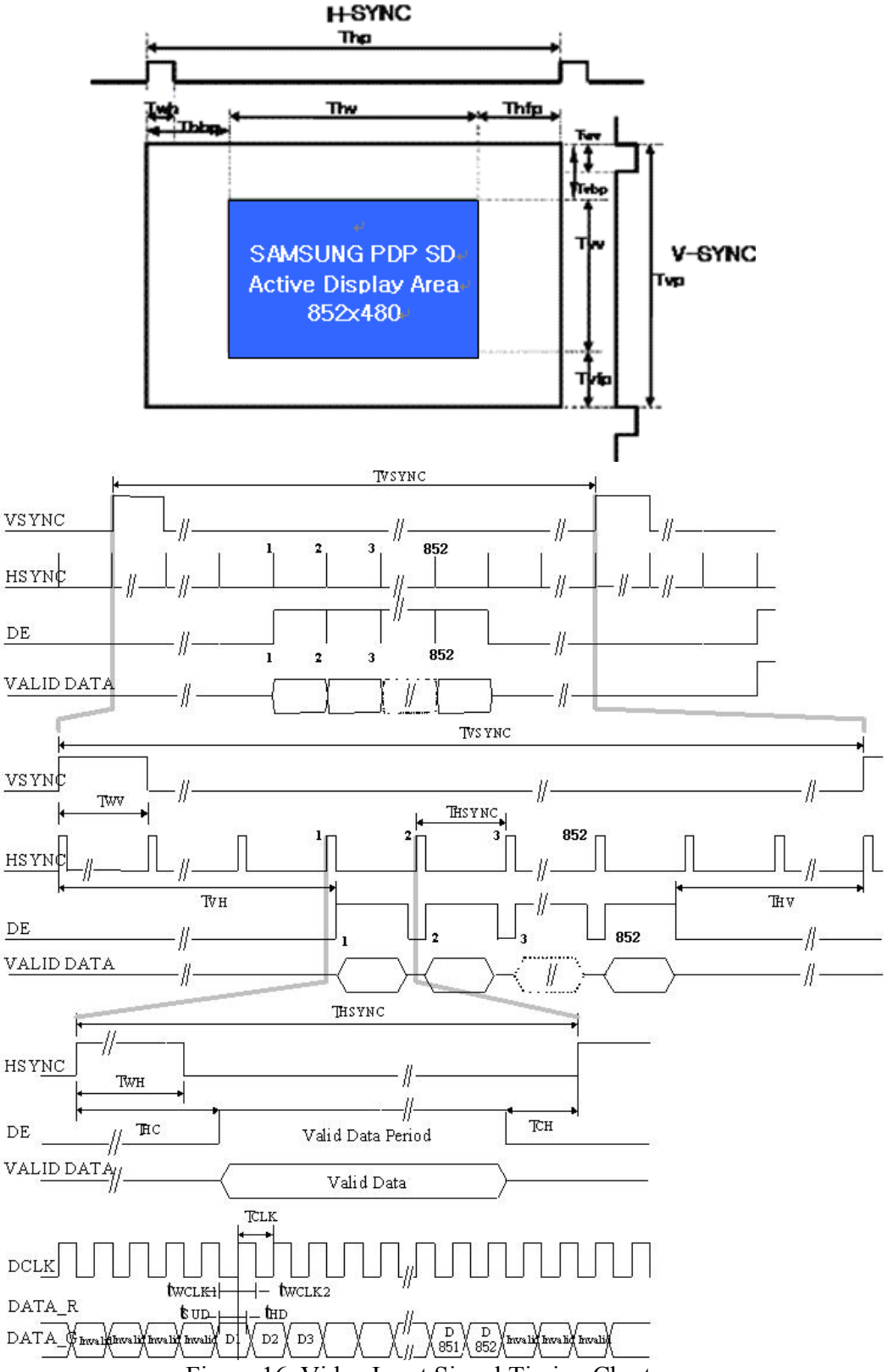


Figure 16. Video Input Signal Timing Chart

10.10 LVDS Connection Specifications

The following Figure shows the connection specifications and signal assignments of the LVDS interface IC. Do not connect or disconnect the connector when the system power in on. Otherwise, the LVDS interface IC could be damaged.

LVDS Interface Connection

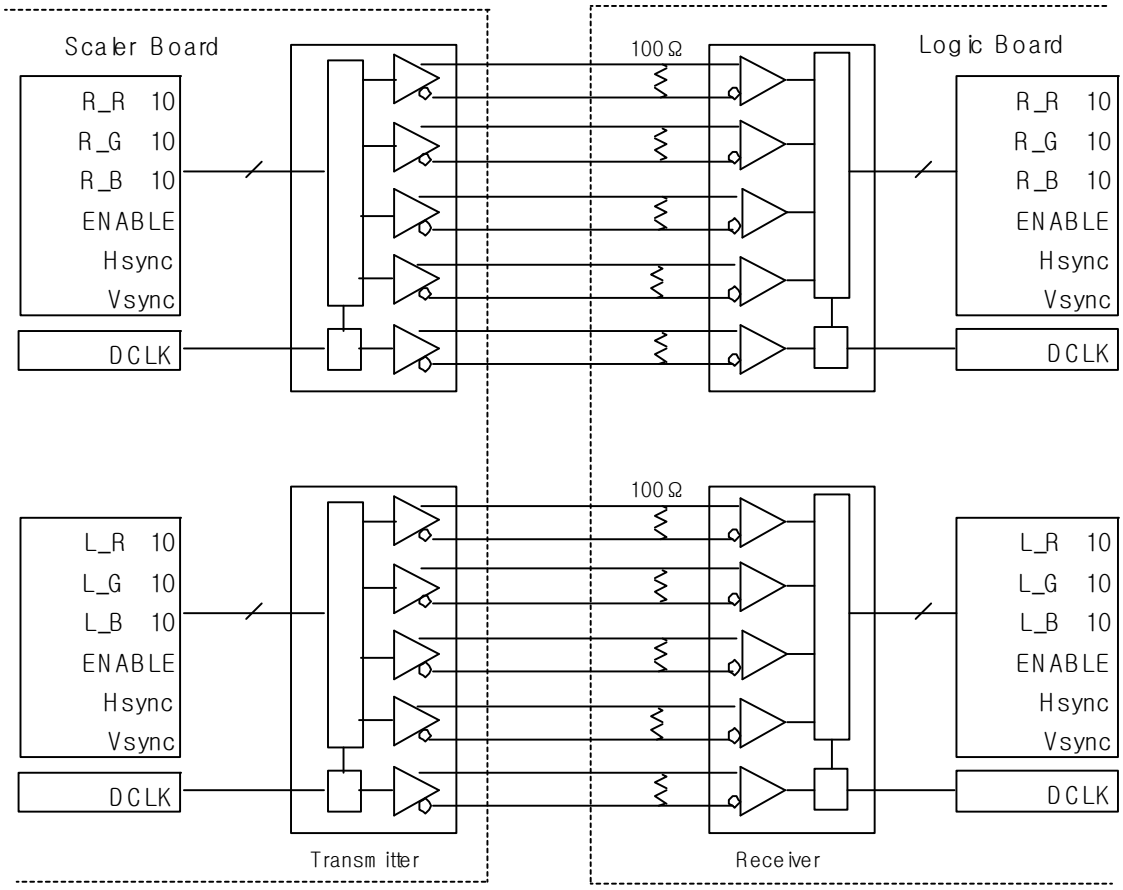


Figure-17. LVDS Interface Connection

10.11 I2C Interface Conditions

10. 11. 1 Basic Specifications

This PDP Module has the I2C bus serial data communication function.
The customer may use this function to make settings for PDP Module characteristics of several items.

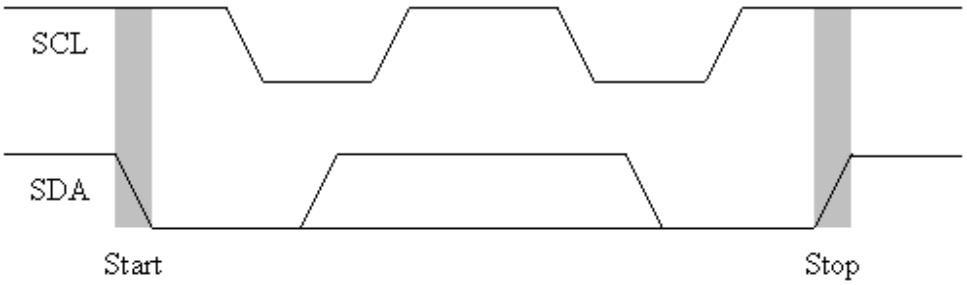
No	Parameter	Specifications
1	**Recommended** Transfer Rate	**100 kbps**
2	Device Status	Slave Receiver
3	Slave Address	CC(Write), CD(Read)

10. 11. 2 Data Validity

Amount of data that is transferred is 1-Bit per 1 SCL cycle. Data is valid when SCL is high and recognized as to state of SDA.

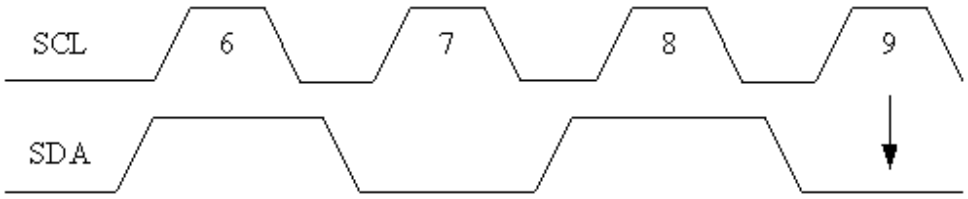
10. 11. 3 Start & Stop Condition

Start /Stop condition is generated by Master (=Image B'D). Before start condition or after stop condition, a SDA cannot be recognized as valid data.
Start condition ☞ SCL high & SDA transition from H to L
Stop condition ☞ SCL high & SDA transition from L to H



10. 11. 4. Acknowledge

When Master (=Image B'D) needs to stop reading data, the master should give NO ACK signal to slave by SDA. Slave (=PDP Module) gives ACK whenever 8-bit transfer is done.



10. 11. 5. 7-Bit Addressing for Device address(with example of CC or CD)

Master could choose slave by 7-bit slave address and decide what procedure is by R/W bit (H=Read procedure, L=Write procedure).

10. 11. 6. 16-Bit Mode

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

10. 11. 7 . Data Transfer Sequence (Write)

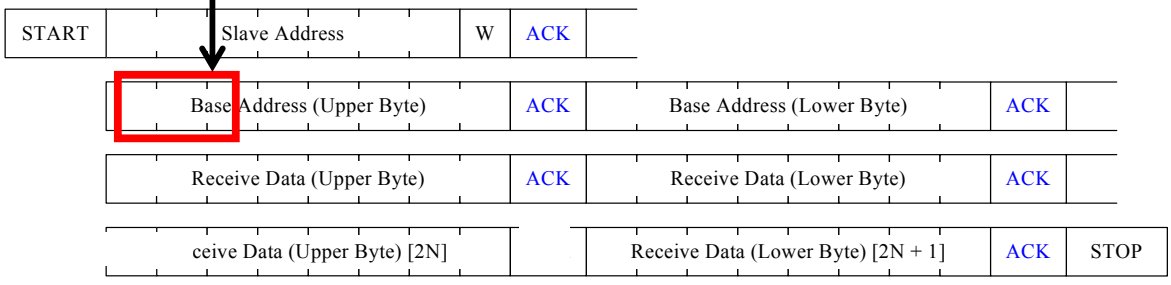
The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

Note 1: Black letters mean master (=Image B'D)'s bus occupation.

Note 2: Blue letters mean slave (=PDP module)'s bus occupation.

Note 3: Option Bit = 01: ROM , 10: RAM , 11: both Memory(ROM and RAM)

If ROM mode is very slow, it is impossible to use normal I2C communication. **The image board can only use RAM mode.**



10.11. 8. Data Transfer Sequence (Read)

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

Note 1: In advance, master should initialize writing sequence by giving base address and stop condition.

Note 2: After start condition and slave addressing, master could receive data from slave.

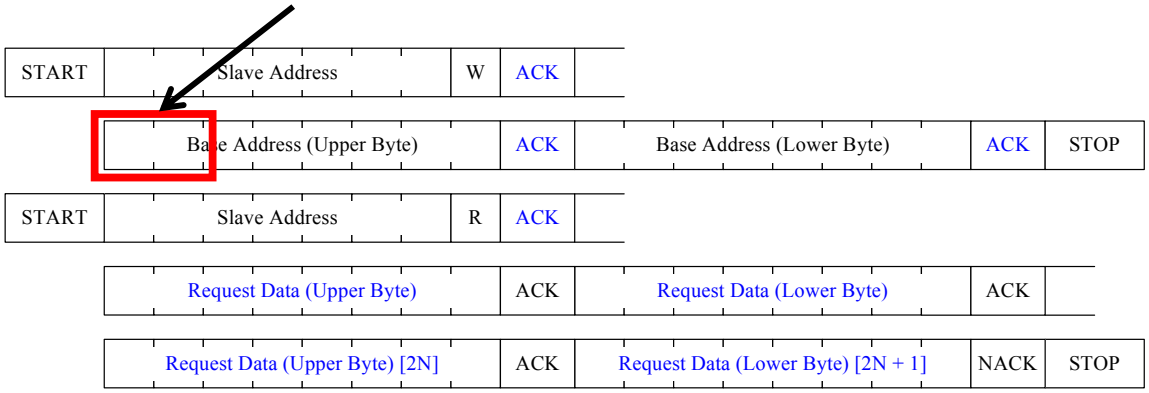
Note 3: Master should give acknowledge whenever 8-bit data is received.

Note 4: 'No acknowledge' could make master give stop condition on bus. Therefore, NACK is used for master to stop receiving data from slave.

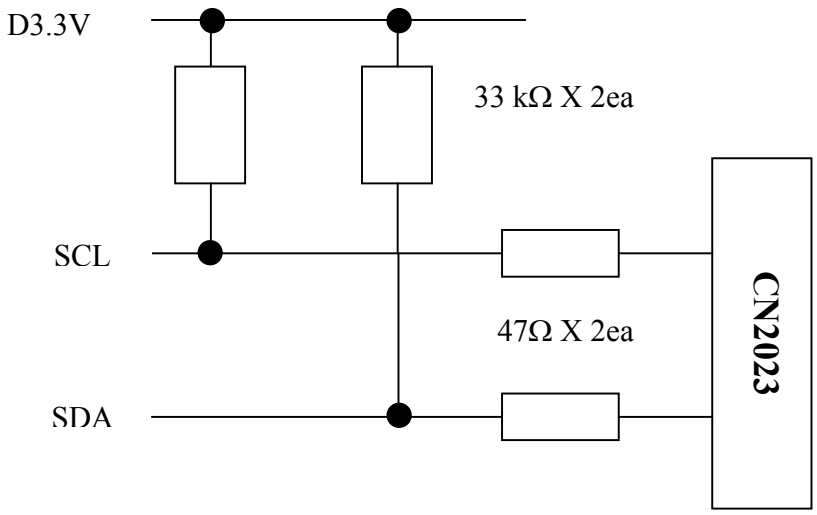
Note 5: Black letters mean master (=Image B'D)'s bus occupation.

Note 6: Blue letters mean slave (=PDP Module)'s bus occupation.

Note 7: **Option Bit = 11: both memory, 01: ROM (FLASH), 10: RAM (in ASIC)**



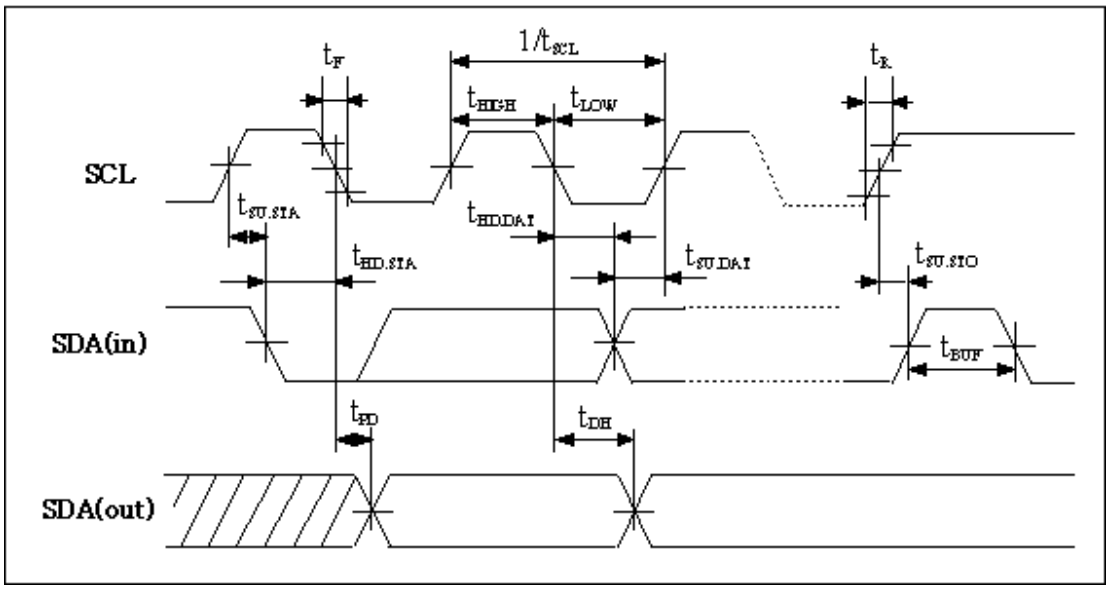
10.11.9. I2C Interface Circuit



10. 11. 11. I2C Bus Timing Specifications

* Refer to the following data merely as sample data.

No	Item	Symbol	Standard			
			Min.	Typ.	Max.	Module
1	SCL Input Frequency	f_{SCL}	5	100	200	kHz
2	SCL Input "HIGH" Period	t_{HIGH}	2.5	-	-	μs
3	SCL Input "Low" Period	t_{LOW}	2.5	-	-	μs
4	Start Condition Set Up Time	$t_{SU.STA}$	3.0	-	-	μs
5	Start Condition Hold Time	$t_{HD.STA}$	2.3	-	-	μs
6	Data Input Set Up Time	$t_{SU.DAT}$	0.2	-	-	μs
7	Data Input Hold Time	$t_{HD.DAT}$	0.1	-	3.45	μs
8	Stop Condition Set Up Time	$t_{SU.STO}$	2.3	-	-	μs
9	Data Output Delay Time	t_{PD}	0.1	-	-	μs
10	Data Output Hold Time	t_{DH}	0.1	-	-	μs
11	SDA Bus Free Time	t_{BUF}	4.0	-	-	μs
12	Packet Timeout *1	t_{PT}	1.0	-	-	sec
13	SCL, SDA Input Rising Time	t_R	-	-	1.0	μs
14	SCL, SDA Input Falling Time	t_F	-	-	0.3	μs
15	SCL, SDA Line Capacitor	C_b	-	-	400	pF



[Note]

1. Packet Timeout is minimum delay time from Start to Stop

10.12 Connector Specifications

Connector Name	Pin #	Signal Name	
CN2023	1	GND	NOTES: 1. CN2023connector is located in Logic Board. 2. Pin to Pin pitch of connector CN2023 is 0.5m 3. The length of mating cable to CN2023 is recommended to be not longer than 25.0 ㎝. 4. Pin numbering order : left to right view from component side of Logic Board. 5. All the other pins are GND. 6. Reserved for factory use only. This pin should be disconnected in case of customer's use. 7. PDP GO is operating DPMS (Display Power Management Signaling). If this pin is not used, it should be N.C.
	2	RTX	
	3	GND	
	4	SDA	
	5	GND	
	6	SCL	
	7	GND	
	8	RRX	
	9.10.11	GND	
	12	NC	
	13	GND	
	14	TxROUT4+/RxRIN4+	
	15	TxROUT4-/RxRIN4-	
	16	TxROUT3+/RxRIN3+	
	17	TxROUT3-/RxRIN3-	
	18	GND	
	19	TxRCLKOUT+/RxRCLKin+	
	20	TxRCLKOUT-/RxRCLKin-	
	21	GND	
	22	TxROUT2+/RxRIN2+	
	23	TxROUT2-/RxRIN2-	
	24	TxROUT1+/RxRIN1+	
	25	TxROUT1-/RxRIN1-	
	26	TxROUT0+/RxRIN0+	
	27	TxROUT0-/RxRIN0-	
	28	GND	
	29	TxLOUT4+/RxLIN4+	
	30	TxLOUT4-/RxLIN4-	
	31	TxLOUT3+/RxLIN3+	
	32	TxLOUT3-/RxLIN3-	
	33	GND	
	34	TxLCLKOUT+/RxLCLKin+	
	35	TxLCLKOUT-/RxLCLKin-	
	36	GND	
	37	TxLOUT2+/RxLIN2+	
	38	TxLOUT2-/RxLIN2-	
	39	TxLOUT1+/RxLIN1+	
	40	TxLOUT1-/RxLIN1-	
	41	TxLOUT0+/RxLIN0+	
	42	TxLOUT0-/RxLIN0-	
	43	GND	
	44	GND	
	45	GND	
	46	GND	
	47	GND	
	48	GND	
	49	3D SYNC	
	50	GND	
	51	GND	

10.13.Mode change

10.13.1. Mode

It has four kinds of mode that is divied NT and PAL by input sync.

Mode	NT	PAL
Normal	Normal_NT	Normal_PAL

10.13.2. Mode Control Register

Register	Address	Bit	Data	Mode	Access
PDP_DRIVING_MODE	806F	bit[8]	0 or 1	Vsync Flag	R
		bit[4:0]	0x11	Normal Mode	R / W

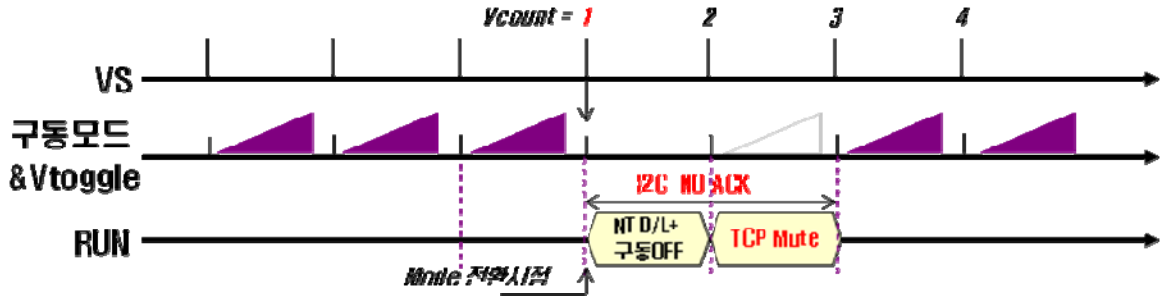


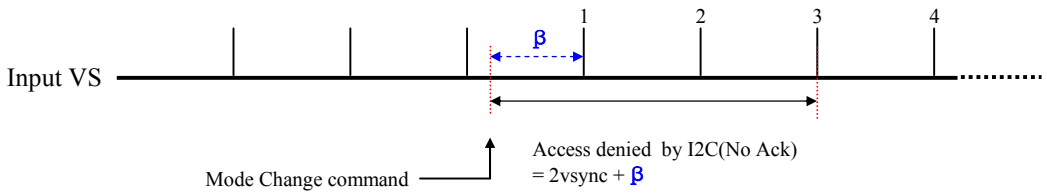
Figure . I2C communication between Disabled

10.13.3. Mode Change

NT, PAL, including the conversion of 2 different Mode is available to each other.

10.13.4. I2C access specification while mode change

If the I2C command input about mode change, the I2C communication could not work while 2 frame + β .



11.ADDRESS MAP

I2C Slave Address ☞ Write: CC (hex), Read: CD (hex)

Sub Address	Data Bit	Symbol	Item / Function	Setting [hex]			Note
				Range	Initial		
					NT	PAL	
8114(NT) A114(PAL)	0~5	R_PAT T_SEL	**Pattern Select** ☞ Patterns below are valid when IE (Internal clk or External clk) is set to '1'. 00: Full Window (Black) 01~04: Full Window (White,Red,Green,Blue) 05 : 1 point Box(White, Windows size) 0B: Color Bar 0C : Half Gray 0D: Cross Hatch 0E : Dot Array 0F : 30% Window 10~13 : Gray Bar (Horizontal, Vertical) 14~16: Horizontal Ramp Pattern (Stay, Scroll) 17~19: Vertical Ramp Pattern (Stay, Scroll) 1A : Horizontal Gray Color Bar 1B : Dot Array, 1C : IRE, 1D : Scroll, 1E : Half Gray, 1F : Moving Scroll	00~1E	00	00	*(a)
89DA(NT) A9DA(PAL)	0~7	PLG	**Power Lower Gain Control** ☞ Control the power lower level of PDP module.	00~FF	80	80	*(c)
89C6(NT) A9C6(PAL)	8~15	ASLG	**ASL Constant Gain** ☞ Control the ASL Gain of PDP module.	80~FF	80	80	*(c)
89C6(NT) A9C6(PAL)	0	ASLG_ SW	**ASL Constant Operation on/off S/W** ☞ '1' = On, '0' = Off	0/1	00	00	*(c)
89C0(NT) A9C0(PAL)	0~8	APCO	**APC Offset Level** ☞ Adjusts peak luminance for customer's specifications.	10~1FF	00	00	*(c)

[Note]

1. Only sub-addresses shown in above table are allowable for access. An access to the any other address than shown in above sub-address table may lead to an abnormal system down or permanent damage.
2. Above table contain the option bits of memory access, MSB and MSB-1 bit in Base address(Upper byte)

*(a) Please access these address for test use only.
For ordinary operating conditions, values of these address should be set to initial values.
Patterns that From 06 to 0A and 0F are activated by setting the value to 0001 of address 4F0Ch

*(b) Customers can set these values considering their specifications.

*(c) APCO , ASLG, PLG is used for control the "Brightness and Power Mode" of PDP Module. For a detailed behavior and variable range, refer to the Chapter 6.7 Power Consumption**.**

12. INPUT POWER VOLTAGE SPECIFICATIONS

12.1 Electrical Characteristic Overview

Power Name	Voltage(V)	Max Load (A)	Regulation(%)	Ripple & Noise (mV)	Remarks
Vs	210	15	±2.0	2000	Sustain voltage
Va	58	10	±1.5	700	Address voltage
Vg	15	1.0	-	150	Drive gate in FET
D5V	5.2	3.5	±5	100	Drive TTL in X,Y driving, Logic

***1. This means nominal voltage stability when current is changed from min to max.**

***2. The output voltages for Vs, Va, could be varied within variable range by feedback variable resistors.**

***3. This spec guaranteed when no changed luminance and power consumption spec**

■ Above voltage levels are norminal value. They are adjustable to drive Panel.

12.2 Pin assignment of connectors for Power Supply

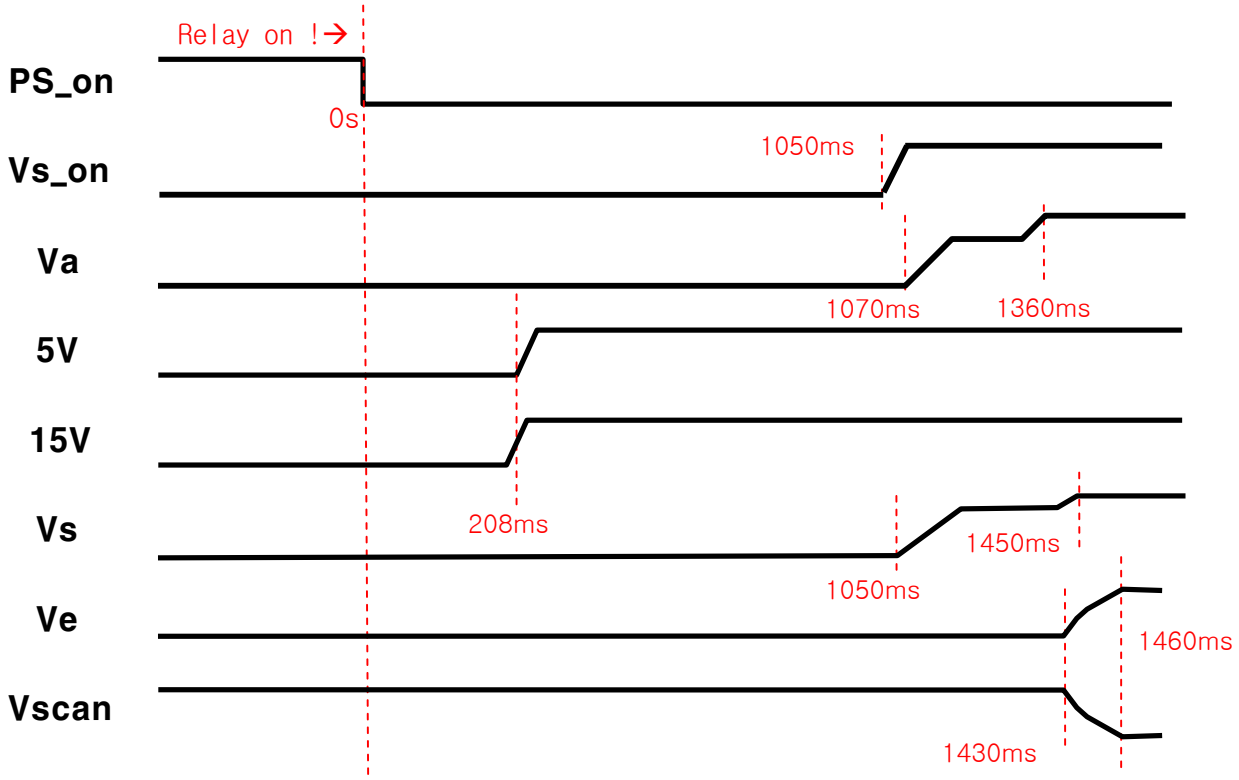
Location No	CN4005
Function	X-BUFFER
Pin Num.	12 pin
Type	Yoen-ho (SMW250-12) 3711-000654
Pin No.	Pin Name
1	Vs
2	Vs
3	NC
4	Va
5	GND
6	Vg
7	D5V
8	GND
9	Vs_on *2
10	Vs_CON
11	Ps_on *1
12	GND

*1. This is a signal(Active High) from Logic main to PSU. (High : 3.3V, Low : 0V)
PSU relay on/off function is controlled by Logic micom.

*2. This is a signal(Active High) from Logic main to PSU. (High : 3.3V, Low : 0V)

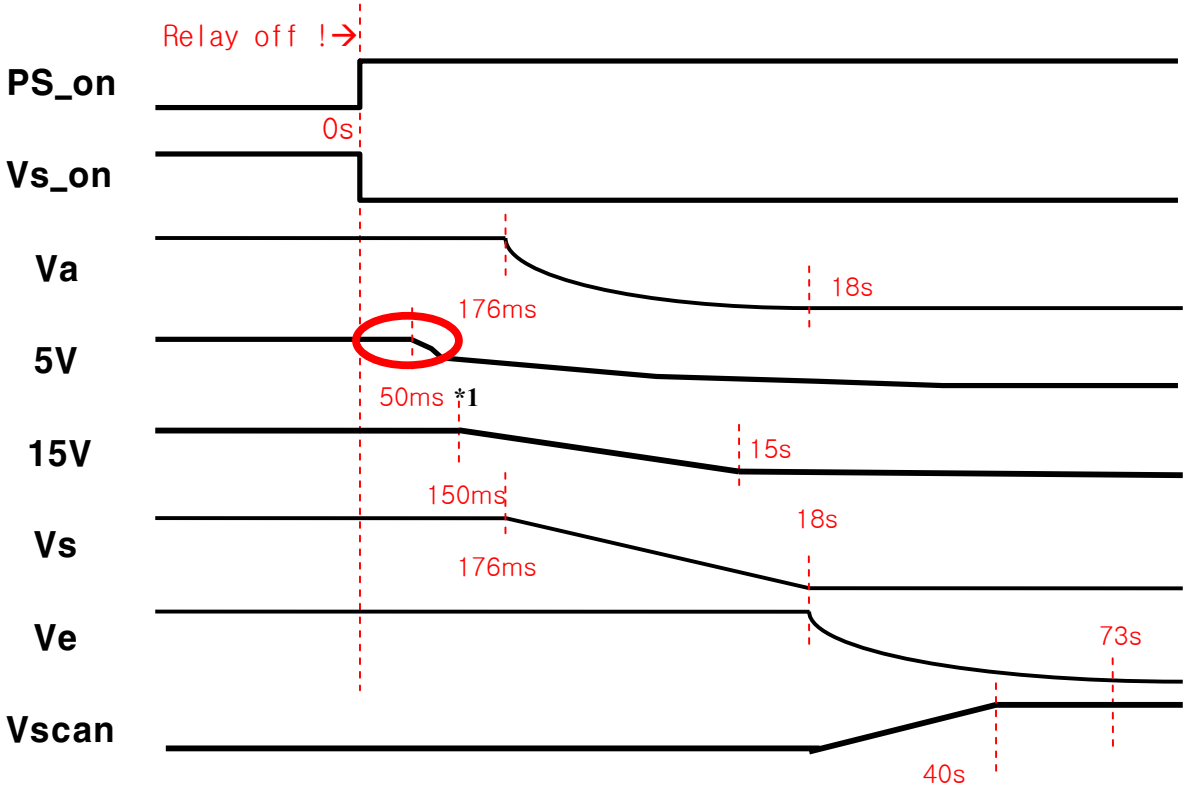
12.3 Power Applying Sequence

► **Relay_on Sequence**



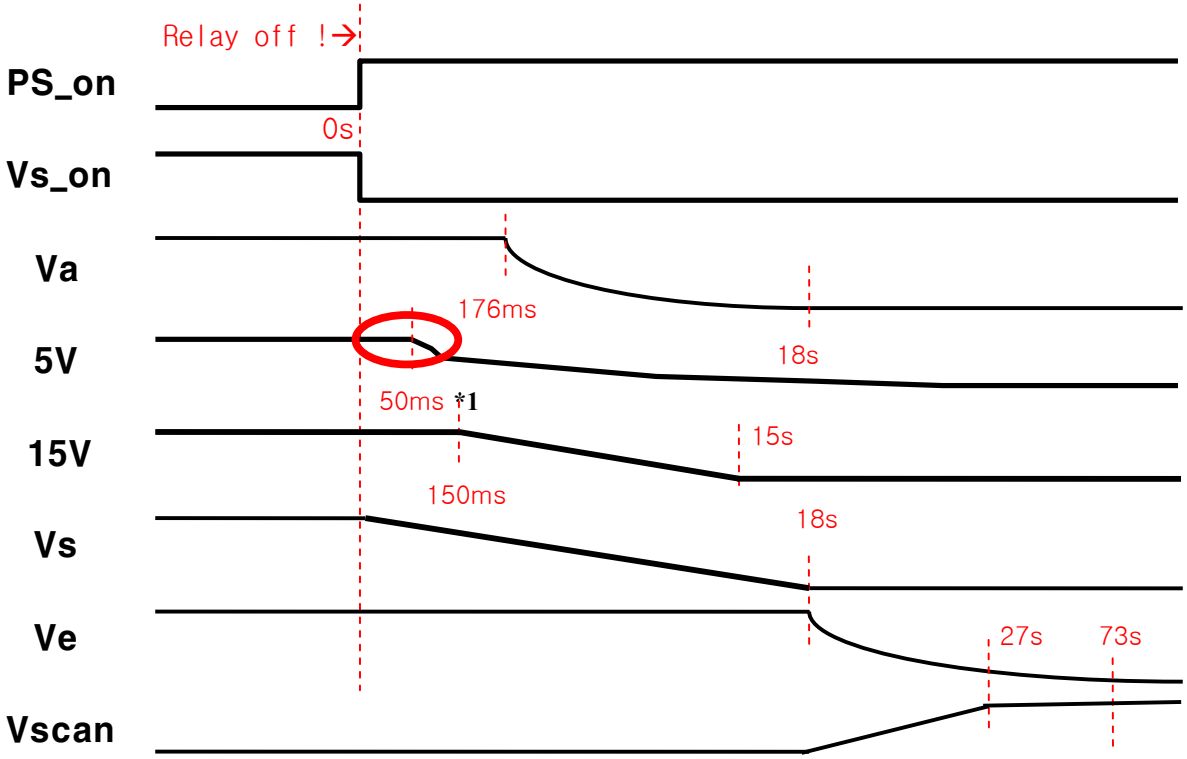
***1. Reference value**
***2. D3V3 needs to start with 5~50ms rising time. And at least 500mA is needed for rising time.**
***3. Vs_on signal is output from Logic board to PSU.**
***4. Vs should be enabling with Vs_on signal(Active High) from Logic.**
***5. Vs should be always higher than Ve while D3V3 is alive.**
***6. I2C Ready signal is output from Logic board to Image board.**
***7. POS : Power ON Sequence.**

► **Relay_off Sequence**



***1.** From the time controlled by the High PS_ON, the 5V should be maintained for more than 30ms.

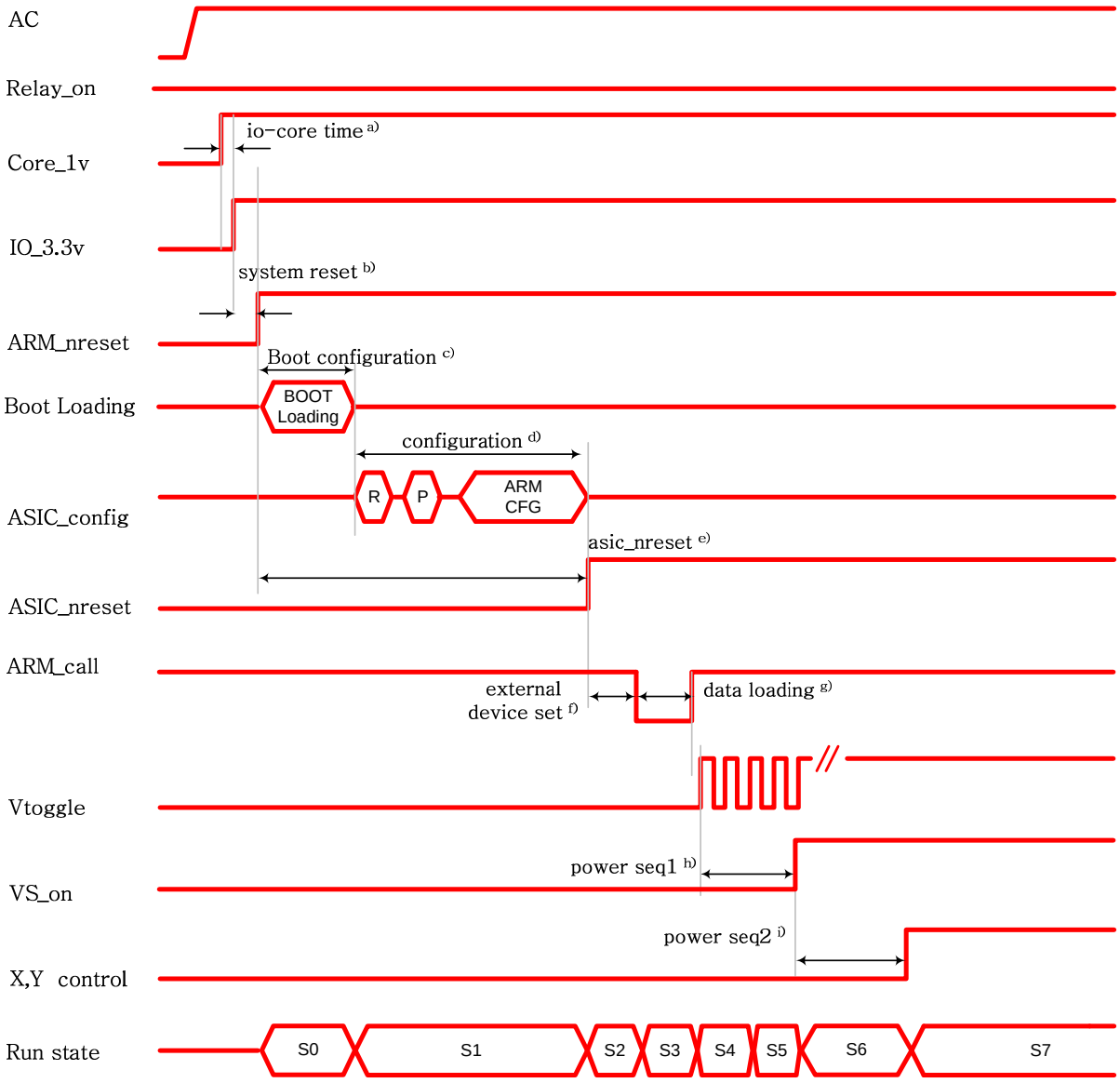
► **AC_off Sequence**



***1.** From the time controlled by the High PS_ON, the 5V should be maintained for more than 30ms.

▶ Logic Start Sequence – Controlled by Vsync

▶ AC on, Relay on



***1. ASIC config "R", "P" is initialization for ASIC.**
***2. ASIC config "ARM CFG" is initialization for arm processor.**
***3. States that from s0 to s6 are setions of power on after system operation.**
***4. ARM_call is measured by cpu counter.**

▶ Timing description.

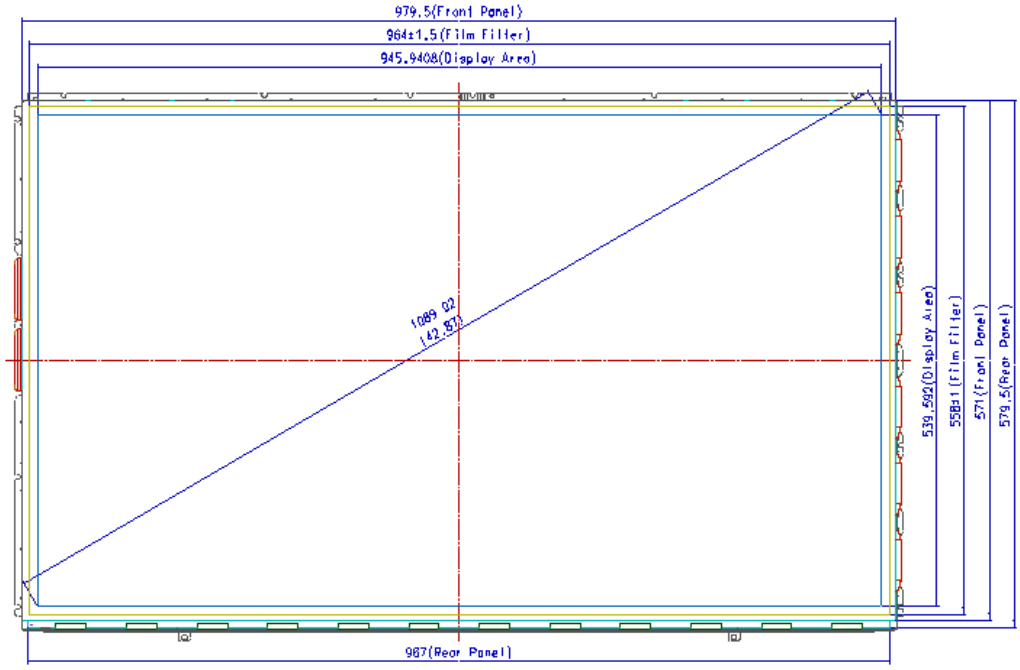
Parameter	Description	Min	Typ	Max	Unit
a. IO-Core time delay	Delay time to io from core	0.1	1.24	–	ms
b. System reset	Reset time for chip	10	53	–	ms
c. boot configuration	Boot configuration time	–	273	–	ms
d. configuration	Glogic configuration time	–	563	–	ms
e. asic nreset	Glogic Reset time to System reset	–	835	–	ms
f. external device set	External device setting time	–	6.4	–	ms
g. data loading	Data loading time		7.2	–	ms
h. power sequence1		–	–	–	ms
i. power sequence2		–	–	–	ms

▶ Stat description.

Stat	Description
S0	Register(PLL, MEM Ctrl, I/O spec, Etc) setting period for chip after system reset or configuration
S2	Data loading period from External flash memory to ASIC sram
S3	VS_ON output activating after S2
S4	Power ON Sequence. Ypn bootstrap capacitor charging and Startup discharge stabilization
S5	Temperature mode setting, holding data restoration, FRC mode setting, etc.
S6	Normal operation(Internal/External switchover, 50/60Hz detect)

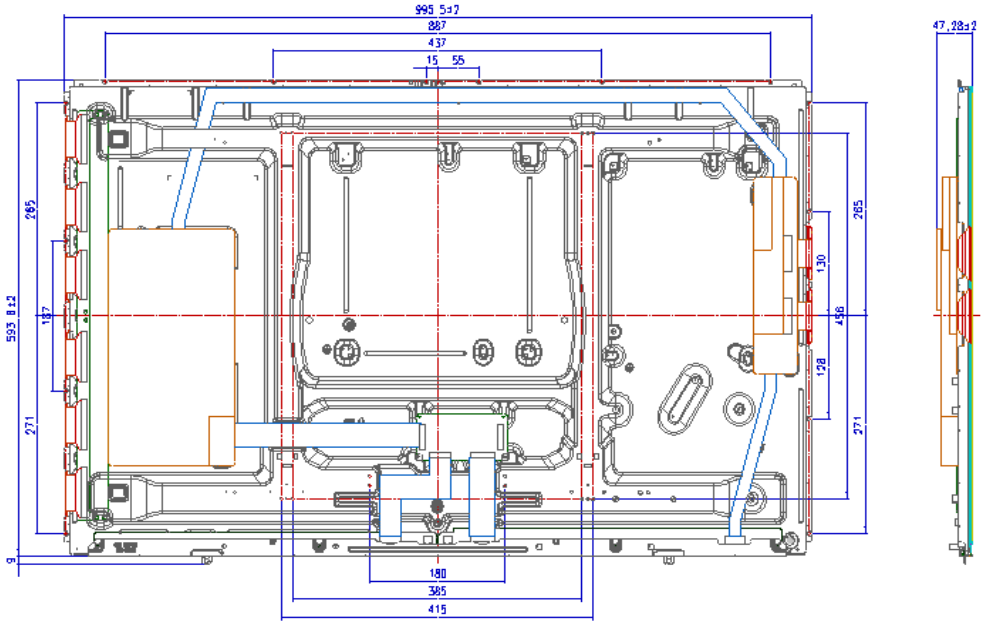
13. MECHANICAL DIMENSION DRAWING

13.1 Front Side



Appendix A1

13.2 Rear Side

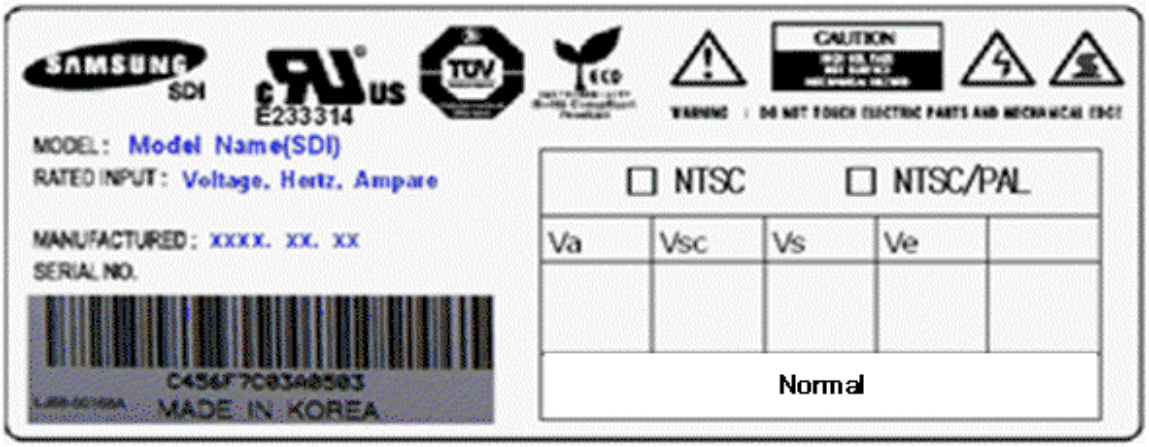


Appendix A2

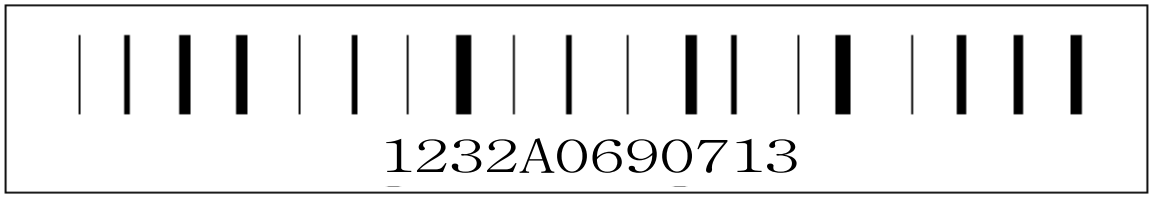
14. LABEL

14.1 Label Type

(1) Integrated Label for the PDP Module

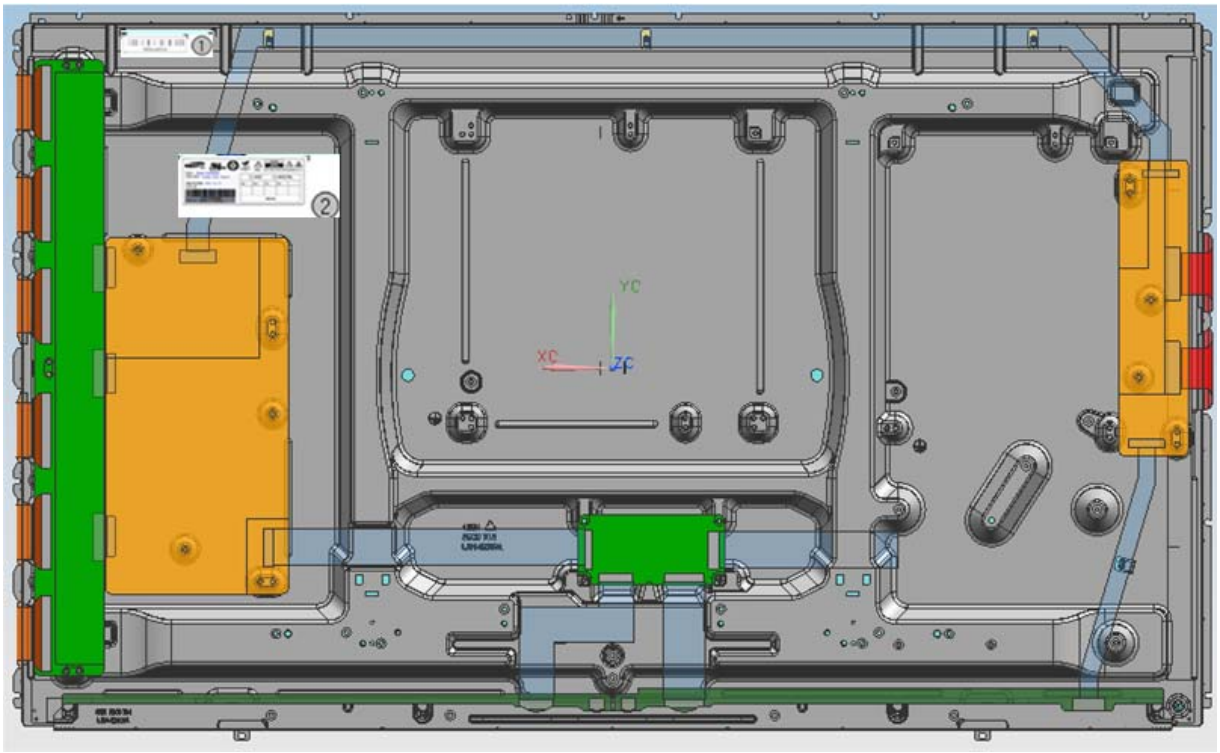


(2) Label for PANEL Serial Number



12	3	2	A	06	90713
Model Type	Production Line	Production Year	Production Month	Production Date	Production Number
43SD EV	3nd Line	2012	01~12	1~30	00000~99999

14.2 Label location



NOTE Label 1 for Panel Serial Number
Label 2 for Product/Caution/Voltage

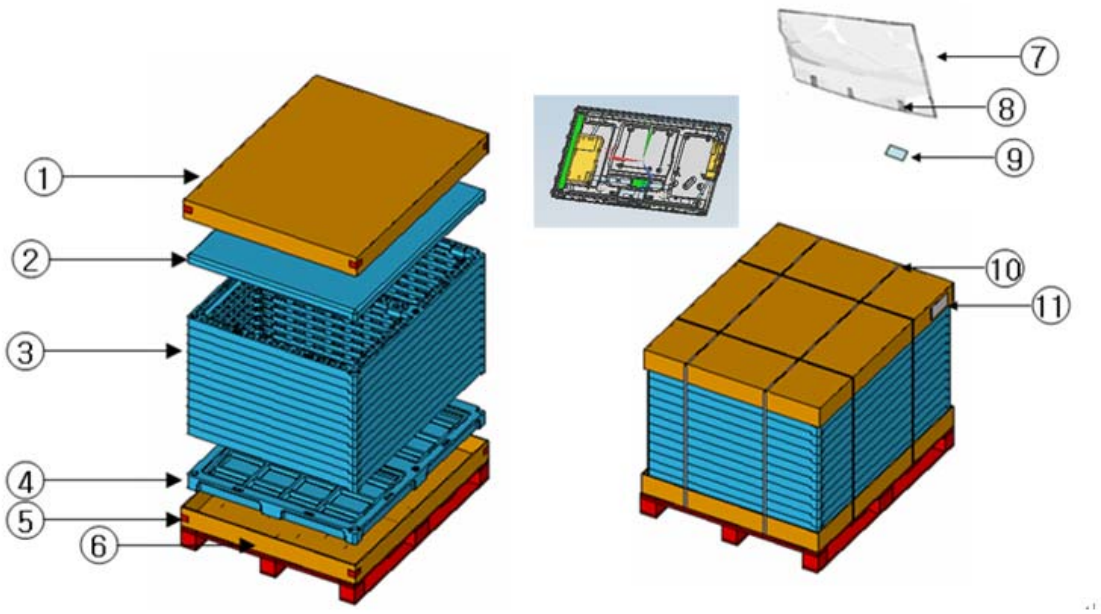
15. PACKING

15.1 Packing Dimension and Parts List

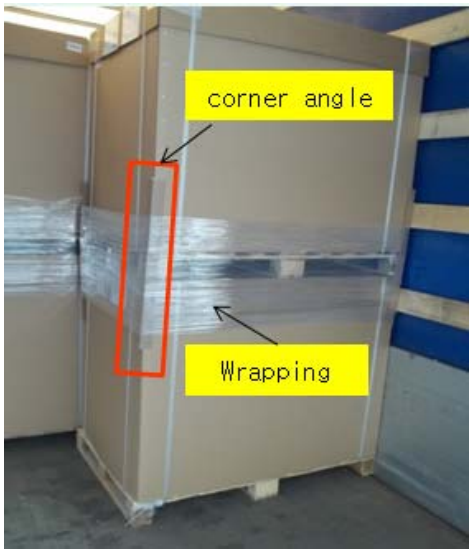
- Number of Module in 1 package: 26Modules
- Packing dimensions (W*L*H): 1460*1140* 1085 (mm) (Including Pallet :125mm)
- Weight: 269 ± 10 kg(26ea)

NO	Item	NO	Item
1	PACKING BOX-TOP	7	BAG-PE
2	CUSHION-TOP	8	TAPE-ACETATE
3	CUSHION-MIDDLE	9	CHEMICALS
4	CUSHION-BOTTOM	10	BAND-PP
5	TAPE-FILAMENT	11	LABEL-INSPECTION
6	PALLET		

15.2 Packing Assembly Drawing



15.3 Exportation Packing Assembly

	A grade	B grade
Region	**China, Russia, Thailand**	**Except for A grade's region**
Specifications		
Corner angle	**O**	**X**
Wrapping	**O**	**X**
Pallete	**Timber**	**Timber (but SEDA and domestic use MDF)**
Note	**For SLIP prevention, - The corner angle is fixed the corner of up/down pallete - The vinyl wrapping between up/down pallete**	**No changes**

16. RELIABLITY

16.1 MTBF Value

Mean Time Between Failure is dependent on the overall PDP Module design.

MTBF : 60,000hours (Excluding Electrolytic Capacitor)

※ Condition : 25℃, Used moving Picture Signal

16.2 Expected Service Life

Expected Life tme : about 100,000 hours.

Expected life refers to the time span in whitch display white brightness decays to 50% of the initial brightness.
The above mentioned value is a referance value, and this value cannot be guaranteed.
Image sticking and other defects are off the subject.

16.3 Disclaimer

This Specification stipulates the final and comprehensive requirements for the respective products hereof. Beyond this Specification, it is the responsibility of the customer to explicitly disclose any additional requirements, information or reservations regarding these requirements to Samsung SDI prior to implementation, where any and all disclosures of the customer shall be with an authorized representative of Samsung SDI in writing. Samsung SDI shall not be responsible for safety, performance, functionality or compatibility of the system with which the Samsung SDI-supplied components are integrated unless such features have been expressly communicated and described in the Specification. SAMSUNG SDI MAKES NO GUARANTY OR WARRANTY, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, TO ANY PARTY. Moreover, any party should do their own due diligence regarding these requirements prior to implementation

16.4 Certificate

We verify that we never use or include the restricted substances under the level 1 of SEC's management requirement (SS-00259) in parts and components, subsidiary material, materials used for unit parts, and packing materials or substances added during manufacturing process.

17. WARNING / CAUTION / NOTICE

TO PREVENT POSSIBLE DANGER, DAMAGE, AND BODILY HARM, PLEASE CONSIDER AND OBSERVE ALL WARNINGS AND CAUTIONS CONTAINED IN THIS PARAGRAPH.

17.1 Warning

If you do not consider the following warnings, it could result in death or serious injury

(1) The Module is controlled by high voltage about 350V. If you need to handle the Module during operation or just after power-off, you must take proper precautions against electric shock and must not touch the drive circuit portion and metallic part of Module within 5 minutes. The capacitors in the drive circuit portion remain temporarily charged even after the power is turned off. After turning off the power, you must be sure to wait at least one minute before touching the Module. If the remain voltage is strong enough, it could result in electric shock.

(2) Do not use any other power supply voltage other than the voltage specified in this product specifications. If you use power voltage deviated from the specifications, it could result in product failure.

(3) Do not operate or install under the deviated surroundings from the environmental specification set for the below; in moisture, rain or near water-for example, bath tub, laundry tub, kitchen sink; in a wet basement; or near a swimming pool; and also near fire or heater - for example, near or over radiator or heat resistor; or where it is exposed to direct sunlight; or somewhere like that. If you use the Module in places mentioned above, it could result in electric shock, fire hazard or product failure.

(4) If any foreign objects (e.g. water, liquid and metallic chip or dust) entered the Module, the power supply voltage to the Module must be turned off immediately. Also, never push objects of any kind into the Module as they may touch dangerous voltage point or make short circuits that could result in fire hazard or electric shock.

(5) If smoke, offensive smell or unusual noise should come from the Module, the power supply voltage to the Module must be turned off immediately. Also, when the screen fails to display any picture after the power-on or during operation, the power supply must be turned off immediately. Do not continue to operate the Module under these conditions.

(6) Do not disconnect or connect the Module's connector while the power supply is on, or immediately after power off. Because the Module is operated by high voltage, and the capacitors in drive circuit remain temporarily charged even after the power is turned off. If you need to disconnect or reconnect it, you have to wait at least one minute after power off.

(7) Do not disconnect or connect the power connector by a wet hand. The voltage of the product may be strong enough to cause an electric shock.

(8) Do not damage the power cable of the Module, also do not modify it.
(9) When the power cable or connector is damaged or frayed, do not use it.

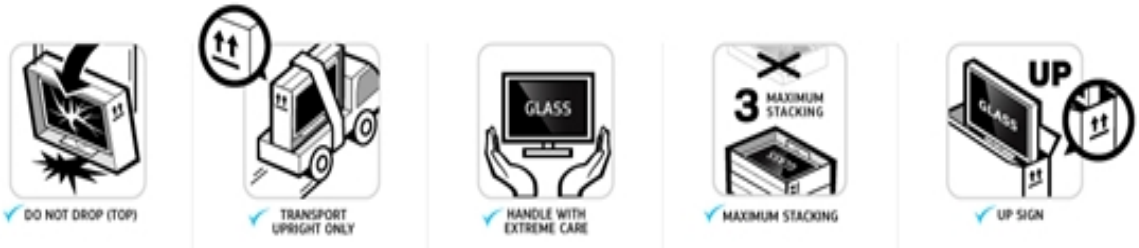
(10) When the power connector is covered with dust, please wipe it out with a dry cloth before power on.

(11) Regarding to Product safty of consumer, If you need, Please consider below actions.

Ex1) Add Protector(Acryl sheet)

Ex2) Warning sticker “No Throw, No shock”

EX3) Handling sticker



17.2 Caution

If you do not consider the following cautions, it may result in personal injury or damage in property.

(1) Do not set the Module on an unstable, vibrating or inclined place. The Module may fall or collapse and it may cause a serious injury to a person, and/or damage to the product.

(2) If you need to remove the Module to another place, you must turn off the power supply and detach the interface cable and power cable from the Module beforehand, and watch your steps not to step on the cables during the operation. If the cables are damaged during the transport, it may result in fire hazard or electric shock. Also if the Module is dropped or fallen, it may cause a serious injury to a person and /or damage to the product.

(3) When you draw or insert the module's cable, you must turn off the power supply and do it (with) holding the connector. If you forcibly draw the cable, the electric wire in the cable can be exposed or broken. It may result in fire hazard or electric shock.

(4) When you carry the Module, it should be done with at least two workers in order to avoid any unexpected accidents.

(5) Be careful not to touch the panel glass surface while the PDP module is operating because there is a possibility of getting a burn injury due to its very high temperature.

(6) The Module has a glass-plate. If the Module is inflicted with excessive stress - for example; shock, vibration, bending or heat-shock, the glass plate could be broken. It may result in a personal injury. Also, do not press or strike the glass surface.

(7) If the glass panel was broken, do not touch it with bare hand. It may result in a cut injury.

(8) Do not place any object on the glass panel. It may be the cause of the scratch or break of the glass panel.

(9) Do not place any object on the Module. It may result in a personal injury due to fall or drop.

(10) PDP is a product, which generates heat during operation. Therefore, do not use the materials which make corrode the PDP module by the chemical reaction that takes place in high temperature and humidity conditions.

(11) Exposing to corrosive gases or contact with the materials, which may cause corrosions, could lead to chemical reactions that will adversely affect on the device. If you were to

use the PDP in such conditions, consider ways to avoid such exposure or to protect the PDP module.

17.3 Notice

When you apply the Module to your system or handle it, you must make sure to follow the notices set forth below.

□ Notice to your system design

(1) The Module radiates the infrared rays of between 800 and 1000 ㎚. It may bring an error in operating the IR-remote controller or another electric system. Please consider (to) providing the IR absorb filter in your system, and evaluating it.

(2) The Module has a high-voltage switching circuit and a high-speed clock circuit. Therefore, you have to apply and evaluate the EMC consideration of your system.

(3) The Module has a glass plate. In your mechanical design, please (consider to) avoid any excessive shock and stress to the glass surface. Also be careful not to damage the exhaust pipe at the corner of glass plate. If the glass plate and exhaust pipe are damaged, the &Module may fail.

(4) Since PDP module is controlled by high voltage, all voltage should be discharged immediately after the power is turned off.

(5) PDP module generates heat during operation. Heatproof design (radiation and ventilation) should be considered from design stage. If the PDP module is used out of the specified temperature range, it can result in a defect.

(6) The ventilation design in your system should have a back-cover that is able to prevent moisture and dust from getting into the inside of the electric circuit, because the Module has high-density electric parts with high-voltage. If the driver circuit has condensation or dusts, it may cause a short circuit or dielectric breakdown.

(7) If an excessive stress (more than specified absolute maximum ratings in the voltage, current, temperature etc.) is applied to the PDP module, it could cause a serious damage. Do not use the module out of the ratings.

(8) Recommended usage condition of PDP module is limited to the general usage. Within this range, the electrical characteristics of all components are guaranteed. Semiconductors should be used within specified usage range. Usage out of the range will result in decrease of reliability and defects in devices. If the usage or operating condition is out of specification specified on the data sheet, it will be not covered from the

guaranteed range. If you were to use the product in the environment not stated in the list, you should consult with SAMSUNG SDI prior to the usage.

(9) When the PDP module shows fixed pattern, there are possibilities of having the image retention (the difference in brightness between turned-on and turned-off portion of screen due to the different temperature and discharge) and image sticking (the difference in brightness due to phosphor deterioration). To ensure the screen performance, we suggest using the visual display area of PDP module and performing the following methods.

A. If the customer is required to use the fixed pattern, reduce the maximum brightness as low as possible, change the position of the displayed area or display the screen saver or moving picture periodically.
B. If possible, change the displayed color to equalize the total displayed time for each cell.

(10) In system design and evaluation process, you should consider the maximum brightness level (image retention and image sticking).

(11) The PDP screen is displayed by image data signals and synchronized signals. If noise interferes with the signals, the PDP screen could be unstable. Thus, when you design, you should take measures to minimize the affects of noise

(12) For preventing from occurring condensation that consists of small drops of water which form when warm water vapor in the air touches a cold surface such as a panel glass moved from cold condition, the module need to be left in the room temperature for minimum 8 hours in box condition before use.

(13) The customer has to consider their packing box to prevent from occurring condensation during delivery to the End User from their packing material design stage.

(14) SAMSUNG SDI PDP module is a product for the computer, office automation, other office supplies, industry and communication, measurement devices, personal and home appliances. However, if you need to use the PDP module in particular situations, such as defective or abnormal operations can directly affect human life, injuries and damages in property could be caused, and high level of reliability is required (aerospace equipments, nuclear control systems, vehicle controls, life-supporting medical devices, etc.), you should consult with SAMSUNG SDI beforehand. SAMSUNG SDI will not take any responsibility for the problems and defects occurred in the course of usage without prior approval of SAMSUNG SDI

(15) Based on the requirements of the safety standard (UL, EN etc.), be sure to add the filter that come up to the impact test to the glass plate

□ *Notice to the operation and handling of the Module*

(1) To prevent defect or failure, please check the cable connections and power-supply condition before power-on.

(2) The Module is controlled by high voltage. Not only during operation but also immediately after power-off, do not disconnect or reconnect the Module's connector because it may result in failure. If you need to disconnect or reconnect, you have to wait at least one minute after power-off.

(3) The Module is equipped with various protection circuits that automatically stop the Module operation, if an interface signal or the power voltage becomes abnormal during operation. If the Module stops suddenly during operation, please check the conditions of input signal or power source before restarting.

(4) For the protection of the circuit, if an abnormal situation is occurred, the high output voltage will be shut down by (watching) the internal input voltage (Vs/ Va/ Vcc). In this case, the Module power resetting is necessary to recover. There are also fuses in the Vs and Va power supply system to prevent smoking and firing by the excessive current. The protecting function of the address driver of keeping a supervisory device for the internal current is provided in the Va power supply system. Therefore, the number of sub-frames decreases to a proper value when the Ia current exceeds a constant value occasionally.

(5) If an abnormal situation such as disconnecting of the input connector occurs, this Module will be on stand-by, which the supply of high output voltage is stopped even if an external power is being supplied. If a normal signal is inputted after this, normal operation state, operations can be restarted again by re-inputting a normal signal. However, it is necessary to rest the Module power when tVH and/or tHV are less than the minimum value provided in the specification

(6) To ensure reliable operation of the Module and to protect it from overheating, do not wrap or cover it with a cloth or like a sheet during power-on period. Also, do not place the Module in a confined space or any other places of poor ventilation.

(7) If you continue to watch the naked screen (without filter glass) for a long time, your eyes could be fatigued. We recommend you rest your eyes occasionally. However, according to the information currently available, watching PDP module for a long time does not cause a direct harm to your eyes.

(8) The screen is controlled with the display-data signals and synchronized signals. If noise interferes with those signals, the screen could become unstable and, in some case, would cause a failure. Do not place any equipment that generates excessive EMI/RFI noise near the interface cable of the Module, and keep the cables as short as possible.

(9) Be careful not to break the glass panel when you handle the Module. Also, when handling the Module, you must wear gloves or other hand protection to prevent injuries that can occur in case when the glass panel is broken.

(10) The glass panel section and drive circuit section of the Module are closely connected and they function as a pair. If the Module is arbitrarily recombined, restructured, or disassembled, SDI will not be responsible for the function, quality, or operational integrity of the modified Module. Do not recombine, restructure, or disassemble it. (Only, the Module for A/S is allowed to be recombined, restructured, or disassembled.)

(11) To avoid a possible electric shock, you must make sure that the power supply voltage of Module is turned off before cleaning. To clean the module's glass panel, apply water or a natural detergent to a piece of soft cloth or gauze, and wring the cloth tightly before wiping the screen. Make sure that no water comes in contact with the connecting terminals on the side of the glass panel. Do not use chemical solvents, such as paint thinner or benzene, to clean the glass panel.

(12) The drive circuit section of Module uses C-MOS integrated circuits that must be protected from static electricity. Therefore, when transporting or delivering the Module, be sure to put the Module in an antistatic bag. When handling the Module, take adequate grounding precautions to prevent static electricity.

(13) When delivering or transporting the Module, you must take special precautions because excessive vibration or shock should not be applied to it. If the Module is dropped, or (if) excessive vibration/shock is applied, the glass panel of the Module may be broken and the drive circuit may be damaged. The packing for delivering or transporting should be made with strict instructions.

(14)The information and schematics shown in this specification are just examples of display applications; it does not mean that they must be applied to your device for the actual use. SAMSUNG SDI does not take any responsibility for the infringement of patent or any other intellectual rights arising from the use of the information or schematics in the document.

(15)If any part or technology of the product described in this specification become subject to restrictions on export or any related laws or regulations, a prior permission is required before exporting.

(16) The PDP module uses semiconductor devices. Since semiconductors are very sensitive to static electricity, the following requirements should be conformed during delivering, transferring and handling the PDP module: Remove the static electricity on your body by wearing the earth-ring which must be connected to the ground through high resistor (about 1M Ohm). It is recommended to wear the conductive clothes and shoes, use conductive floor mats, and take other measures to minimize the static electricity. All the equipments and tools must be connected to the ground and protected from static electricity. When you deliver or transfer the PDP module, always use anti-static bag.

(17) If any device that can generate the high-voltage is located nearby the PDP module, it could cause an abnormal operation. In such a case, you should take a countermeasure to prevent against static electricity and discharges.

(18) If the PDP module is exposed to corrosive gases or contacted to oil, it could cause chemical reactions and give unfavorable effects on the devices. If you intend to use the PDP module under such conditions, you must consider the ways to avoid exposure or to protect the PDP module before using it.

(19) The PDP module is not designed to endure radiation or cosmic radiation. Users must install the proper shielding.

(20) The PDP module uses thermo-plastic devices. Since these devices are easy to be damaged, do not use the PDP module nearby inflammable substances. If they are burnt, poisonous gas will be emitted.

(21) To ensure the normal operation of the PDP module, the recommended operating range should be required. The electrical properties of the PDP module are guaranteed only when it is used within the recommended operating range. The PDP module must be used within the range at all time. If you use it out of the range, it could give adverse effects on its reliability or cause defects.

(22) Flexible cables connect electrodes on the panel glass and PCBs. Thus, do not apply too much stress such as shock, vibration, pressure, or bending, to the surface of panel glass, PCBs and flexible cables.

(23) If there is no special notice, the contents of this specification describe the product with the initial parameters after shipment.

(24) Even if the panel glass is cleaned before shipping, there is a possibility of particle remained on the panel. In this case, remove it prior to the usage. When you clean the surface of the panel glass, use a piece of soft cloth with detergent to wipe off. Do not use any chemical substances such as acid, alkali or organic detergent.

(25) The Module is composed of various kinds of materials such as glass, metals and plastics. A qualified service technician is required for the disposal of the Module

.

☐ *Notice to the storage of the Module*

(1) When storing the Module, you must select an environmentally controlled place. Avoid any environment in which the temperature or humidity exceeds the specification values. If you are storing it for a long period of time, we recommend that you place the Module together with a dehumidifying agent, such as silica gel, in a moisture-proof bag and keep it in an environmentally controlled place.

(2) If the module is stored for a long time, the discharge might not take place smoothly. In this case, aging approximately for minimum 2 hours with a full white pattern is suggested. Do aging once in every 6 months.

(3) Do not place the PDP module in the environment with a rapid temperature change in order to avoid the condensation inside of the module.

(4) Do not open the packages at dusty place or the place where corrosive gases exist.

(5) Only qualified person can transfer the PDP module with a forklift or crane.

☐ *Notice to the repairing and fixing of the Module*

The PDP module is a product made with various tests and adjustments hence, repairing and

fixing of PDP module is not allowed to conduct at customer's place. The issue must be handled separately from the specifications.

□ *Notice of the Module performance*

The Module is the newest display device utilizing the gas discharge technology and digital signal processing technology, and its performances are mostly similar to those of CRT. However, some display performances of the PDP module are different from the CRT's. Please consider the following notices when you watch the screen.

(1) There is (a) slight Neon luminance shown outside of the effective display area on the glass panel. Conceal these parts so that it may not be seen on the display surface.

(2) Depending on the type and time of usage, there may be a slight change in the Luminance and color. There may be an increase of both X-value and Y-value by 0.05 at the maximum in chromaticity. In this case, adjust it using the external data signal.

(3) Because the Module uses phosphor to emit a light, the phosphor, like a CRT, will be deteriorated in proportion to the display signal and Luminance settings. If the same pattern is displayed continuously (fixed display) for an extended period of time, the Luminance of that area will be decreased over non-lit areas due to the fact that the discharge surface will be more activated comparing to the other areas.

(4) When the Vsync signal timing becomes shorter right after the changing of Vsync frequency (e.g. from 50㎐ to 60㎐) depending on the Multi-Vsync function, an initial Vsync signal of the changed frequency will be disregarded and the screen will be interrupted for 1 frame period in maximum.

(5) Because the Module is a digital processing display device, this Module is equipped with the Error diffusion technology and a Duplicated Sub-Frame method to display the grayscale and false contour improvement. However, you may sometimes find a color false contour, especially in human facial contour, in moving picture due to the difference of display performance comparing to the TV-tube.

(6) If the Module displays some video test patterns that are mostly used in a laboratory or inspection process of the manufacturing facilities, you may find the following subjects. But these subjects should not be recognized in the failure or defects because the display performance of the Module is equipped with Error diffusion technology and Duplicated Sub-Frame method (for PAL) based on digital processing technique.

<a> Linearity in the grayscale test pattern
If the PDP module displays the grayscale test pattern (e.g. white color Luminance is gradually changed horizontally or vertically) in a screen, you may find the disparity of Luminance at adjacent grayscale patterns. This behavior is caused by duplicated sub-frame condition (for PAL), display load correction and electroad dependency.

<b> Color contouring and dithering at the stationary picture

If the stationary picture such as a human face or the like is shown in the screen, you may feel some unstable noise at the contour area. This behavior is called the color contouring or dithering, and is caused by the error diffusion condition, display load correction and electroad dependency.

(7) If the Module is operated under inadequate conditions or harsh environment, the screen may become unstable or noisy. This instability is mostly related to ambient temperature, air pressure, input signal instability (include signal noise), input power voltage and strong magnetic field such as MRI/NMR application or superconducting magnet application. Please do not apply the Module to inadequate conditions or harsh environment mentioned above.

□ *PDP DESIGN GUIDELINES AGAINST CORROSIVE GASES/HIGH HUMIDITY*

During the PDP development stage , some materials which may generate corrosive gas(es) or ions such as sulfur, sodium, and clorine, etc must not be allowed to use in the modules. If the material mentioned above is used or located close to the address terminals, chemical reaction may occur and cause the modules to fail.

If customer wishes to use some materials due to unavoidable cause, then safe gap between address terminals and the material(s) which may generate corrosive gas(es) is minimum 5mm or customer must keep or deliver PDP always in room temperature and room humidity state at any cases.

It is a mandatory guide line to protect the modules from corrosive gases or ions.

If some material contains sulfer (sulfur) ,Natrium (sodium) and Cloride , then Samsung SDI strongly suggests customer to keep the guidelines.

The weight of material containing sulfer must be no more than 300ppm .

The analysis of the sulfur weight is based on the noramlized " ICP-AES" method.