FOR MESSRS:

DATE: November. 15. 2005

STANDARD

CUSTOMER'S SPECIFICATIONS
(Approval Edition)

1,269cm (50 Inch) Wide Plasma Display Module

MODEL : **S50HW-YD01**

(NTSC / PAL)

* This specification will be approved by both Customer and Samsung SDI Co.,Ltd.
* Please return one of this specification with your signature for approval.

Proposed by:

Signature _____

Vice President Sung Do Kim

Quality Innovation Team,

PDP Business Division,

Approved by:

Signature _____ .

SAMSUNG SDI CO.,LTD.

Revision History

Revision	Date	Description Of Changes	Rev. No	Approval
1	2005-09-29	Newly established	Rev.0.0	-
2	2005-11-15	P7. 6.1 Display Performance P21 10.3 Input Signal Definition P24 10.5 LVDS Signal Pin Assignment P28 10.8 Video Signal Interface Timing Conditions P34 10.11.9 Data Transfer Sequence(Read) P39 12.2 Electrical Characteristic Overview for Image Voltage	Rev. 1.0	

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1. DESCRIPTION

The S50HW-YD01 is a 50-inch wide full color plasma display Module with a resolution of 1366(H) × 768(V) pixels. The display module includes the Plasma Display Panel, the Panel Driving Electronics, the Logic Control Board, and the Power Supply Unit(PSU).

2. FEATURES

- Wide aspect ratio(16:9) 50 inch diagonal display screen. The display area is 1106.46mm wide and 622.08mm high.
- Slim and light weight. The display Module is 63.5mm in depth and weight only approx. 24.8kg include power supply.
- 68719.47 million colors(12Bit), 1073.7 million colors(10Bit), or 16.77 million colors(8Bit) combination of R,G and B digital data.(according to LVDS input selection)
- High Luminance, High contrast, Wide viewing angle. The screen has a white peak Luminance of Typical 1,200 cd/㎡(NTSC), Contrast of Typical 10,000:1(NTSC). And a viewing angle of greater than 160° comparable to those of CRTs.

3. PRODUCT NAME AND MODEL NUMBER

- Product name : 50 inch Full Color Plasma Display Module3 (abbreviation : PDP Module3)
- Model number : S50HW-YD01

4. FUNCTION OUTLINE

- The plasma display Module has an APC(Automatic Power Control) function which restricts power consumption within the certain value with regard to each display load ratio.
- The plasma display Module is operated by following digital video signals; Vertical synchronous signal, Horizontal synchronous signal, Enable signal and 8~12bits data signal of each R,G, and B color. All signals are based on LVDS level.
- The plasma display Module is operated at 50Hz or 60Hz frame rate. An external frame rate conversion is required in order to display the other formats.
- The plasma display Module requires several types of input power voltages ; voltage for LOGIC, voltage for TCP, voltage for Gate Driver, voltage for Sustain, Address, Set, Scan and X-bias.
- The plasma display Module is operated at progressive signal only. An external progressive scan conversion is required in order to display the other formats.
- The plasma display Module requires rated 100~240V, 50~60Hz of input power voltage.

5. BLOCK DIAGRAM

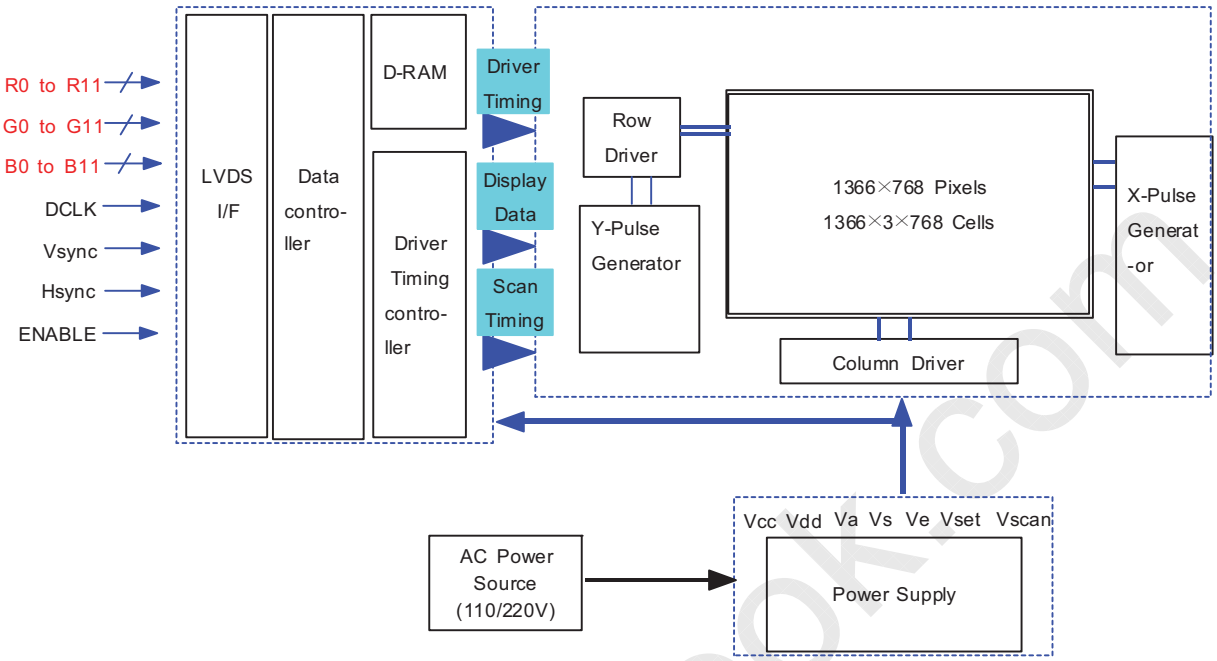


Figure-1. Block Diagram of PDP module

6. DISPLAY CHARACTERISTICS

6.1 Display Performance

No	Item	Rating	
1	Display Pixels	Horizontal 1366 × Vertical 768 pixels (1 pixel = 1 R,G,B cells)	
2	Display Cells	Horizontal 4,098 × Vertical 768 cells	
3	Pixel Pitch	Horizontal 810㎛ × Vertical 810㎛	
4	Cell Size	R	Horizontal 270㎛ × Vertical 810㎛
		G	Horizontal 270㎛ × Vertical 810㎛
		B	Horizontal 270㎛ × Vertical 810㎛
5	Pixel Type	R, G, B Non stripe (refer to Figure-2)	
6	Effective Display Size	Horizontal 1106.46㎜ × Vertical 622.08㎜ [43.54 inch × 24.49 inch]	
7	Number of color	68719.47 million colors (12Bit) 1073.7 million colors (10Bit) 16.77 million colors (8Bit)	
8	Peak Luminance *1 (peak algorithm on)	NTSC : Typical 1,200 cd/㎡ PAL : Typical 1,100 cd/㎡	
9	Contrast Ratio *2 (in dark room, peak algorithm on)	NTSC : Typical 10,000:1 PAL : Typical 5,000:1	
10	Brightness (Full white Brightness)	NTSC / PAL : Typical 165 cd/㎡	
11	Viewing Angle *3	Over 160°	

(Note)

* 1. Luminance and Color Coordinates are the values that were measured with Full load ratio white pattern. The condition for measurement is shown in Figure-3.
* 2. Contrast Ratio is calculated from the display Luminance and the non-display Luminance value. Display condition is shown in Figure-4.
* 3. Viewing angle is a critical angle at which the Luminance is reduced to 50% to the Luminance perpendicular to the PDP Module. The Luminance is measured by a non-contact luminance meter CA-100Plus.

6.2 Display Cell Arrangement

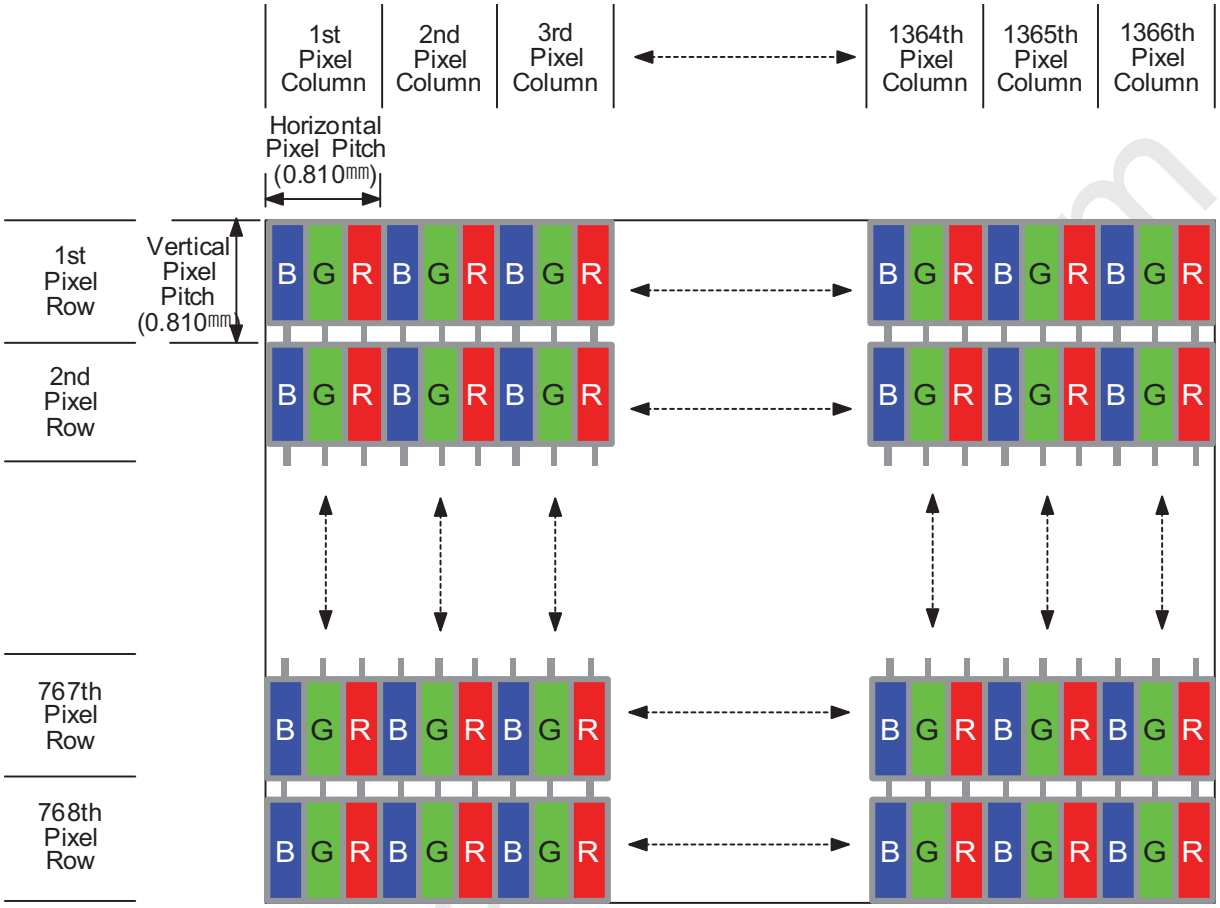


Figure-2.Display Cell Arrangement

6.3 Luminance Measurement Condition

(1) Display Pattern

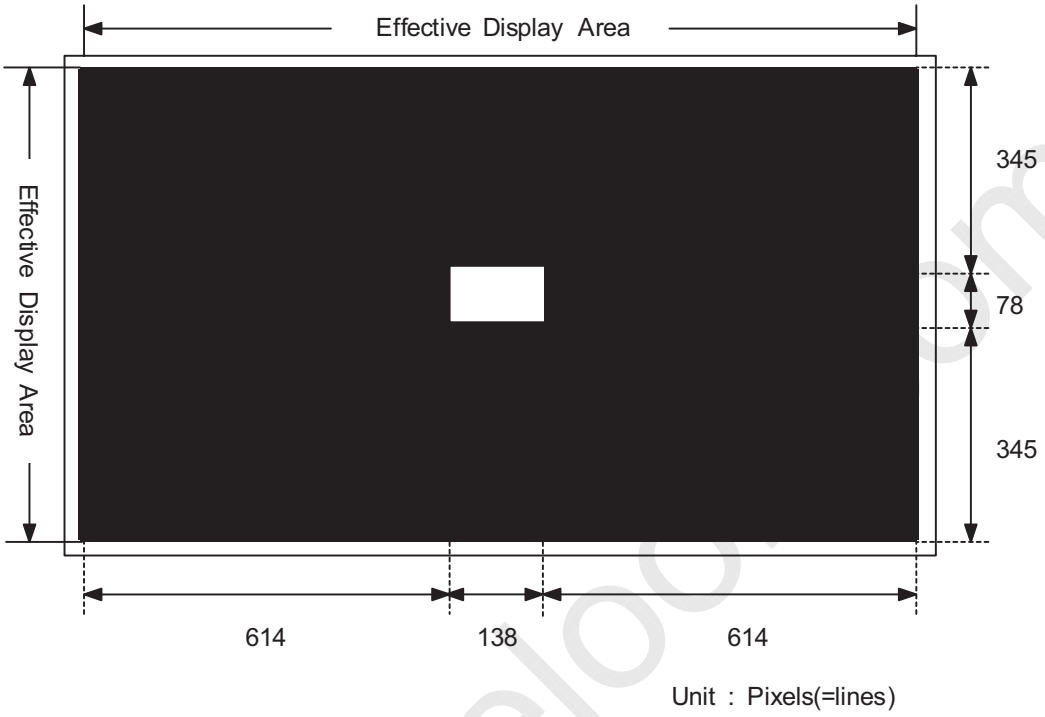


Figure-3. Display Pattern for Brightness & Contrast Ratio Measurement

(2) Display Area ratio : 1% white window

(3) Vsync : 16.7ms or 20ms

(4) Measuring equipment : MINOLTA CA-100Plus
Pattern Generator(VG-828, LVDS Output).

(5) Ambient Temperature : Room Temperature

(6) Ambient Luminance : Dark Room (<2 lux)

[Note]

1. Measurement is done within 3 seconds after Power On. The temperature of panel before measurement is room temperature (25℃).

6.4 Contrast Measurement Condition

(1) Measuring point

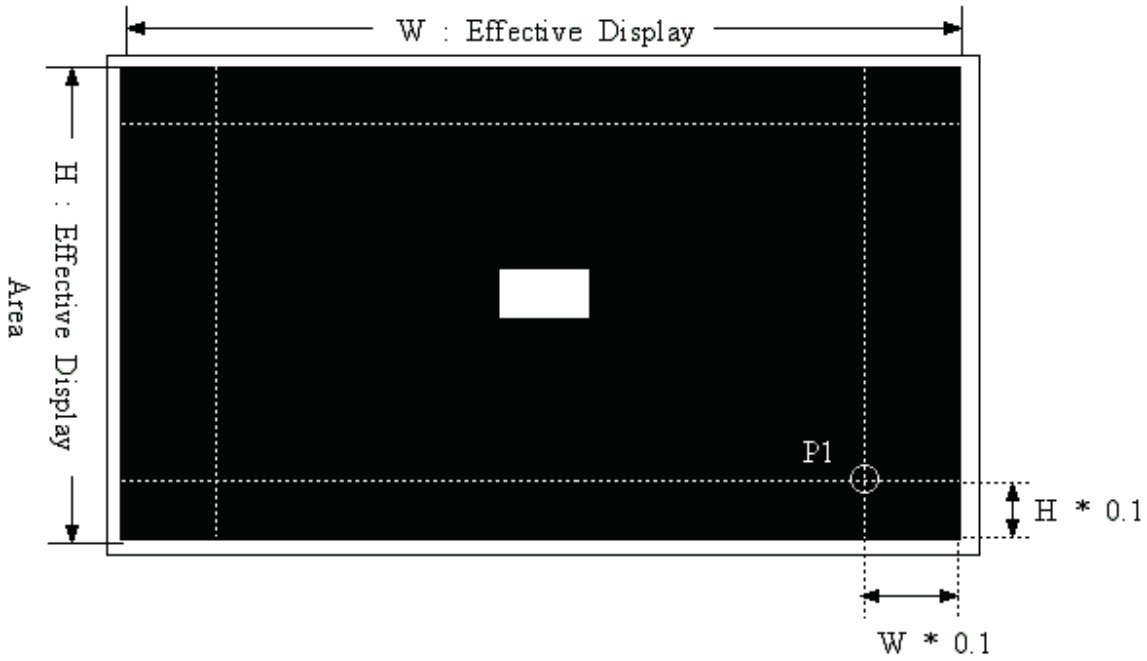


Figure-4. Measurement point

(2) Vsync : 16.7 ms or 20ms

(3) Measuring Equipment : MINOLTA CA-100Plus
Pattern Generator(VG-828, LVDS Output).

(4) Contrast Calculation formula

$$\text{Contrast ratio} = \frac{\text{Luminance of 1\% white window Area at the center of the screen}}{\text{Luminance of Black Area *1}}$$

【 Note 】

1. For mass production test purposes, it is recommended to measure just 1 point, P1 of Figure.-4 on display pattern of Fig.-3.
2. Measurement is done within 3 seconds after Power On. The temperature of panel before measurement is room temperature (25℃).

(5) Ambient Light : Dark Room (<2 lux)

6.5 Display Cell Defect Specification

In some cases, a panel may have defective cells that cannot be controlled.
These defective cells can be categorized into three types;
(1) Non-lighting cell defect : defect in which the cell is always off
(2) Non-extinguishing cell defect : defect in which the cell is always on.
(3) Flickering cell defect : defect in which the cell is flickering.
(4) High intensity cell defect : defect in which the cell is brighter than other cells
(5) Test Pattern : Full White, Full Red, Full Green and Full Blue with 1023 gray level.

The display cell defect specifications define the allowed limits for display cell defects and are used as the criteria in determining whether a panel should be shipped.

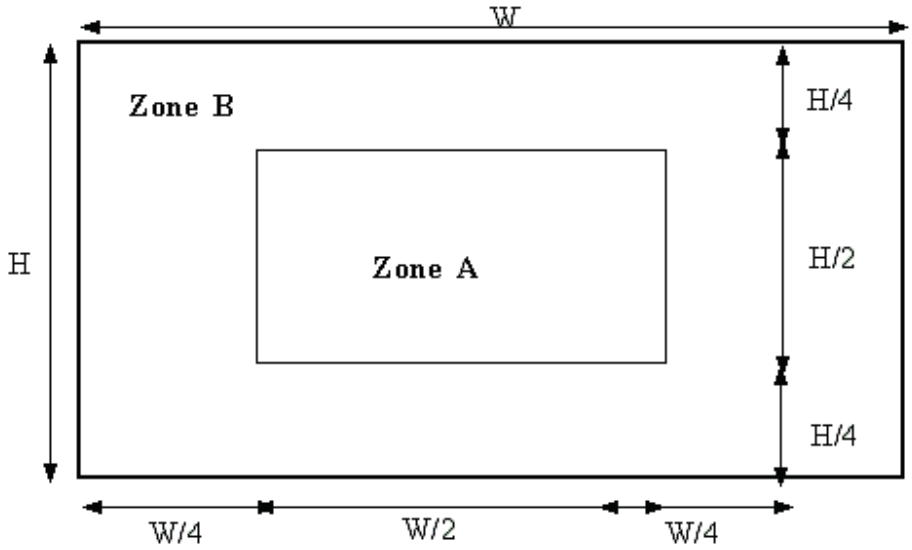


Figure-5. Measurement Area

Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 4 and less Zone B: 9 and less	Regardless of A and B zone, Maximum 1 Cell Defect in an area of 50mm*50mm is allowed.
Non-extinguishing cell defect	Zone A: 2 Zone B: 3 and less	
Flickering cell defect	Zone A: 2 Zone B: 3 and less	
Continuous Cell defect	Zone A: 1 Zone B: 2	
Total defect	Total number of cell defects in Zone A and B is less than 16	

6.6 Brightness Variation Specification

The color-PDP uses ultraviolet light produced by gas discharge to illuminate phosphor. Uneven phosphor coating and inconsistent discharge characteristics cause slight difference

Item	Definition	Specification
Full white brightness variation	The brightness is measured at 9 points (A1~A9 of Fig-6) on full white pattern. The full white brightness variation as then calculated from the following equations.	10% and less
Equation	$\frac{Max - \bar{x}}{\bar{x}} \times 100\%$ & $\frac{\bar{x} - Min}{\bar{x}} \times 100\%$	

in brightness among the sections in a panel.

The brightness variation specifications define the allowed limits for brightness differences and the criteria in determining whether a panel is shipped.

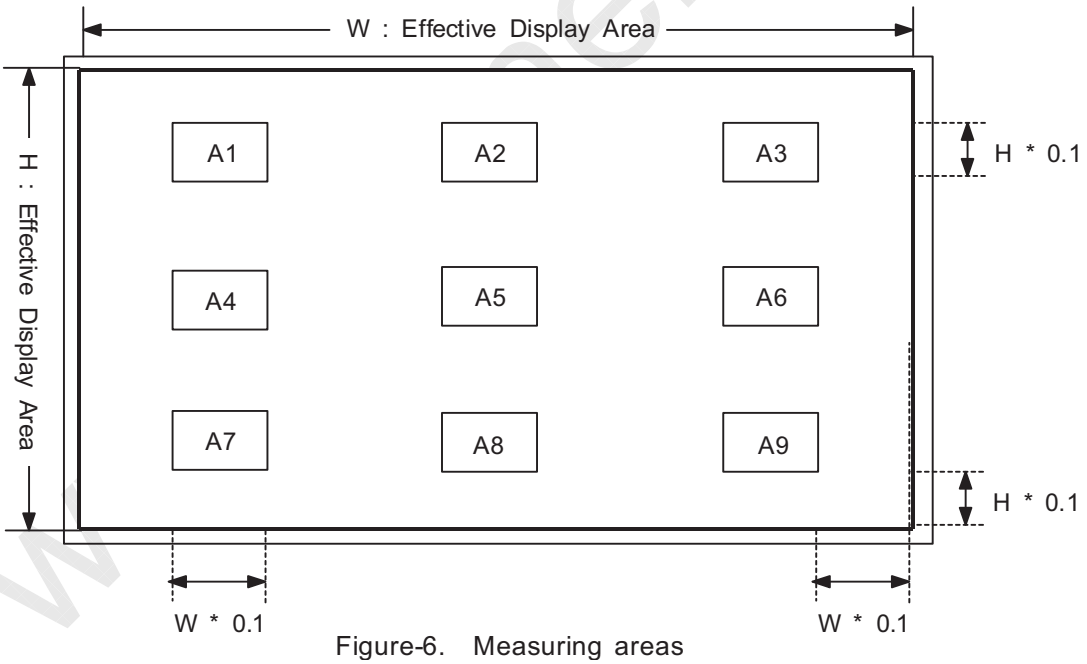


Figure-6. Measuring areas

6.7 Power consumption

6.7.1 APC (Automatic Power Control) Function

The PDP has an APC (Automatic Power Control) function for the panel driver power source. When the total display load ratio exceeds approximately 10%, total power consumption is limited within a specified level(=Lower Power Limit) by APC function. The operation behaviour of APC function is called as SLOW-APC. When the display load-ratio changes from low to high value, the power-consumption rises instantly to "Upper Power Limit" and gradually decreases until it reachs to the "Lower Power Limit".

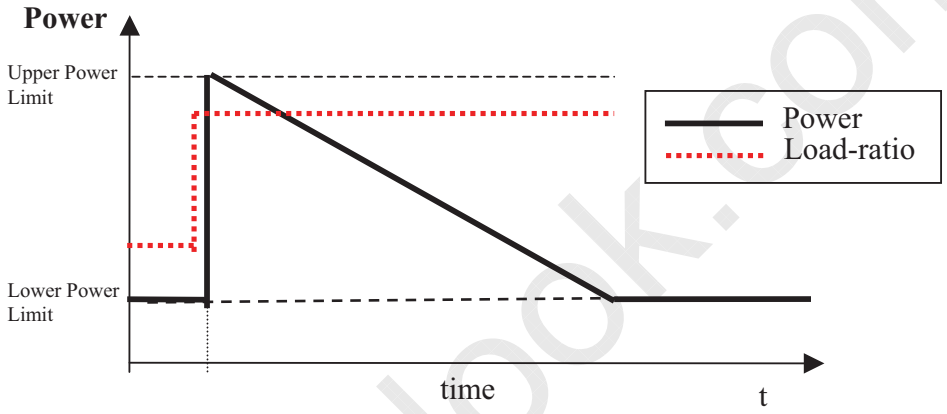


Figure-7 Slow APC Behaviour

6.7.2 Brightness and Power Mode Control

This PDP module offsers two methods for Brightness and Power mode control. APCO(APC Offset) is for Peak-Brightness control. APCO is register controllable through I2C communication from image B'd.

1) Peak-Brightness Control(APCO)
   - controls the max.sustain number
   - APCO variable range : 00~C7h

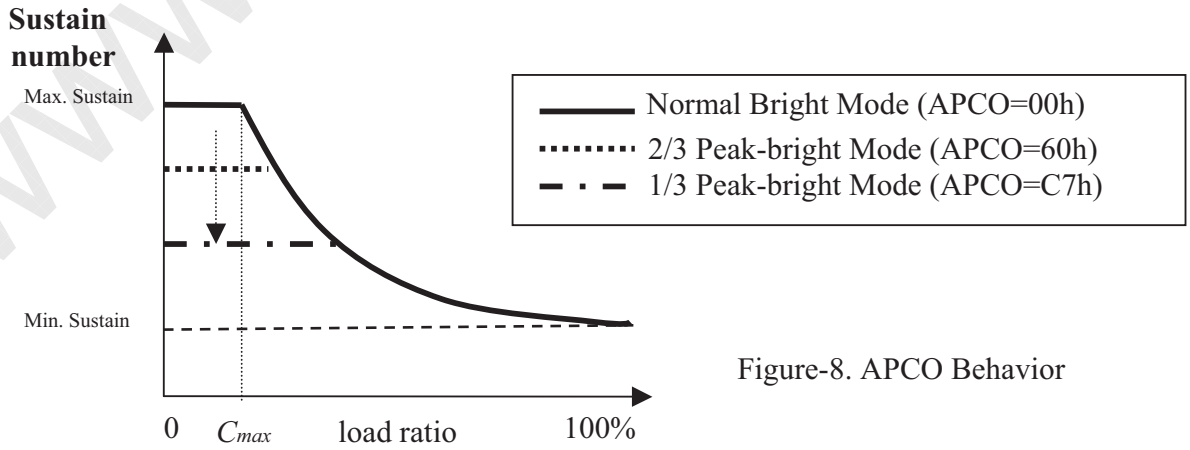


Figure-8. APCO Behavior

6.7.3 Power Consumption Specification

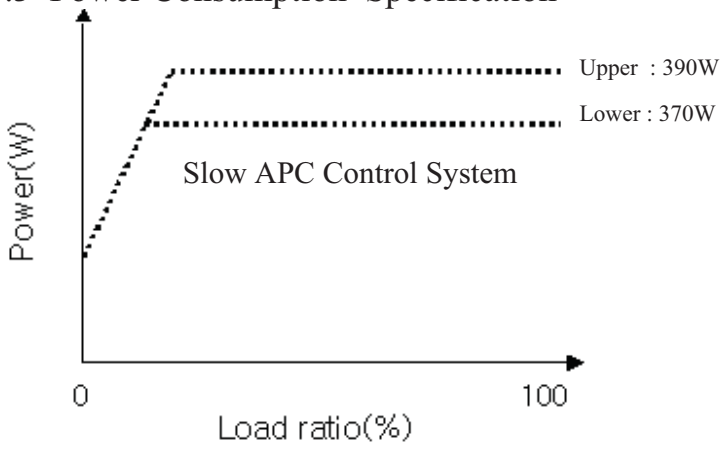


Figure-9. Display load ratio vs. Power consumption

[Note]

1. This is the case that the PDP Module includes SDI's Main PSU at AC 100V, 60Hz.
   It is measured on full screen white pattern with input gray-level 1024(10Bit) in module.
2. Power consumption is same for PAL and NTSC mode.

6.8 Gamma characteristics

6.8.1 Basis of Gamma Curve

This PDP module is normally applied to the 2.0 gamma curve (refer to Figure-10)
But this specification could be modified on the request of the customer

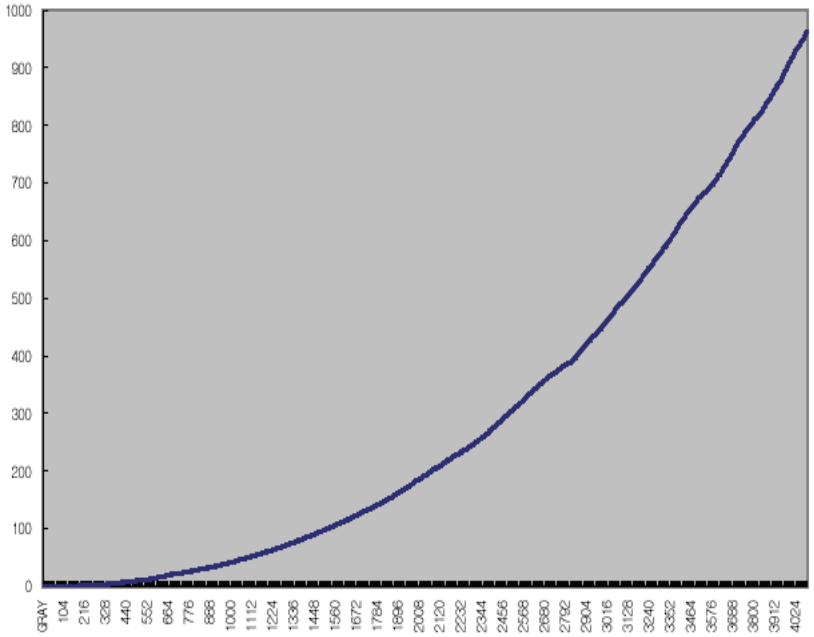


Figure-10. Default Gamma Curve

7. SOUND PRESSURE LEVEL SPECIFICATION

7.1 Measurement Condition

(1) Background Noise Level : less than 20dBA
(2) Measuring Pattern : Dynamic Images (only, Full Black to Full White)
(3) Measuring Equipment : Sound level meter Type 2827 made by B&K
(4) Measuring Distance : 1m from the rear side of PDP Module
(5) Measuring point

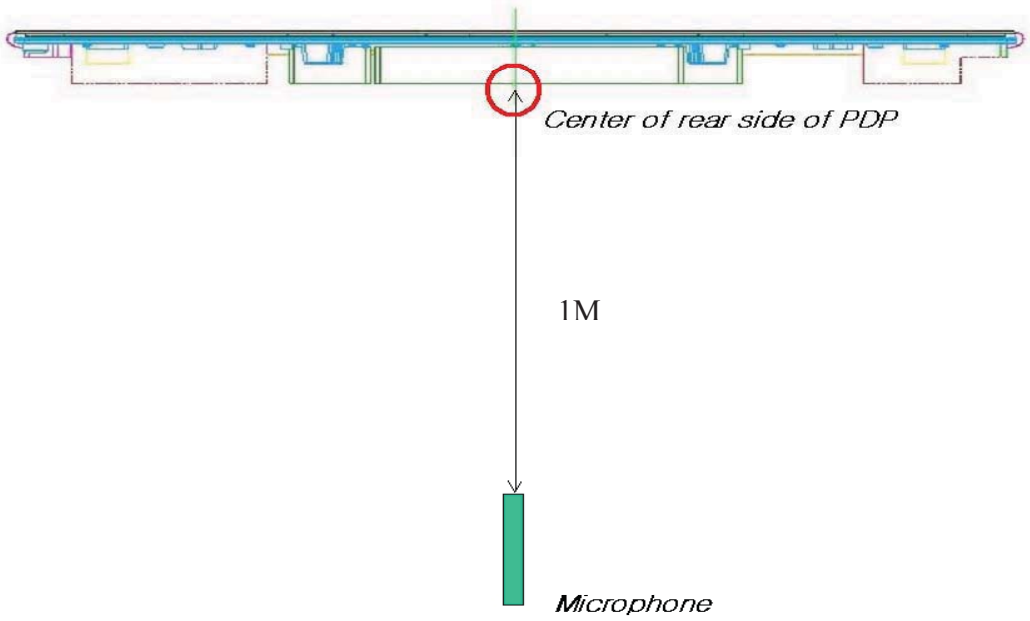


Figure-11. Measuring Point

7.2 Sound Pressure Level :

Sound Pressure Level : Max.33dB (50Hz ~ 8kHz)

- Bandwidth : ⅓ Octave
- Weighting Filter : A-weighting network

【Note】

1.PSU must be included in this measurement.
2.Measrurement pattern : Full White

8. MECHANICAL CHARACTERISTICS

8.1 Mechanical Specifications

No	Item	Rating
1	Outer Dimension	Width 1,175 mm × Height 682 mm × Thickness 63.5 mm (include FPC and TCP) *see Appendix : Mechanical Dimension Drawing
2	Weight	Approximatly 24.8 kg

8.2 Mechanical Characteristics

No	Item	Rating
1	Vibration	Frequency : 10 ~ 55 Hz Sweep Rate : 1 Octave/min Stroke : x,y direction : 0.35 mm Z direction : 0.175 mm
2	Shock	Acceleration : less than 20 G (x,y direction) less than 10 G (z direction) Duration Time : 11 ms

* Notes: (Test condition) Non-Packaging, Operational (only for Vibration)
* Test time of Vibration Test is 30 minutes every direction(x,y,z)
* The number of times for shock test is 6 times every direction(x,y,z).

9. ENVIRONMENTAL CONDITIONS

9.1 Operational Environmental Condition

No	Item	Rating	
1	Ambient Temperature	Display Operation *2	0℃ ~ 50℃
		Temperature Slope	Below 1.5 ℃/minute
2	Panel Surface Temperature *3	Small Size Pattern Full White Pattern	~ 110 ℃ ~ 75 ℃
		Temperature Slope	Below 20 ℃/cm
3	Humidity	Display Operation *2	20 ~ 70 RH (no condensation)
4	Pressure	Display Operation *2	1,013 ~ 845 hPa (0 ~ 2,000 m)

[NOTE]

1. Functional Operation means that the PDP module is operated only its electrical function.
2. Display Operation means that the PDP module is operated in its full specifications.
3. Panel Surface Temperature means the surface temperature of panel that is just increased due to the loss of power inside Panel during the image display at a normal display mode and a ambient temprature defined in this table.
   The judgement of display defects (e.g. weak discharge, missing discharge) should be done when the panel is operated at a ambient temperature defined in this table.

9.2 Storage Environmental Condition *1

No	Item	Rating
1	Ambient Temperature	-20℃ ~ 70℃
2	Humidity	5 ~ 85 RH (no condensation)
3	Pressure	300 ~ 1,013 hPa (0~10,000m)

[NOTE]

1. Storage means the short term period. (e.g. transportation, relocation and so on)

9.3 Panel Surface Condition

9.3.1. Panel surface temperature specification

The panel surface temperature should be kept as below in order to get stable display of image.

- Tp= below 110℃ (Absolute Maximum Rating); when small size of image is displayed
- Tp= below 75℃; when Full White is displayed.

If the temperature exceeds above level, it may cause the defects of display image like dot missing, line missing and/or poor image.

As the surface temperature of panel has tendency to rise with deduction of display rate, the relation with temperature can be describe as below:

75℃ (display load rate is high : Large Area)
~ 110℃ (display load rate is low : Small Area)

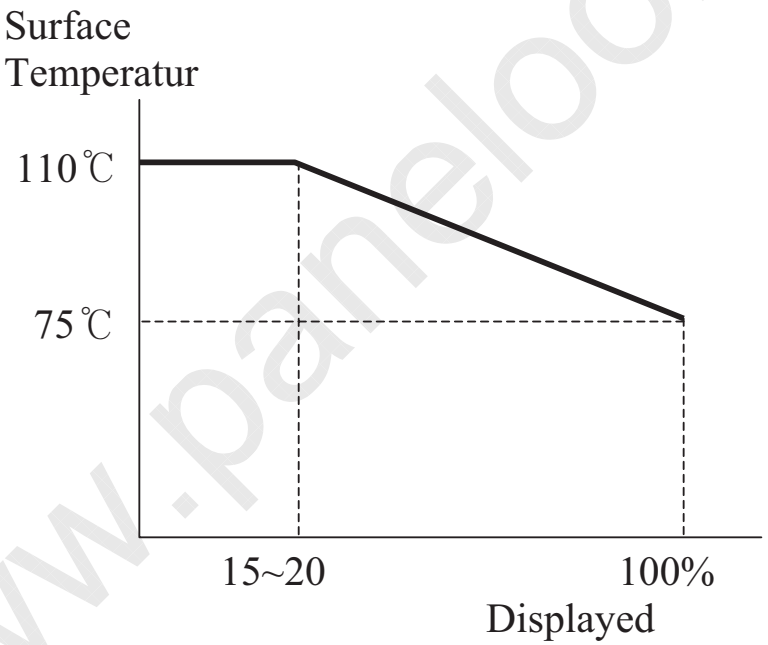


Figure-12. Surface Temperature Vs Displayed Area

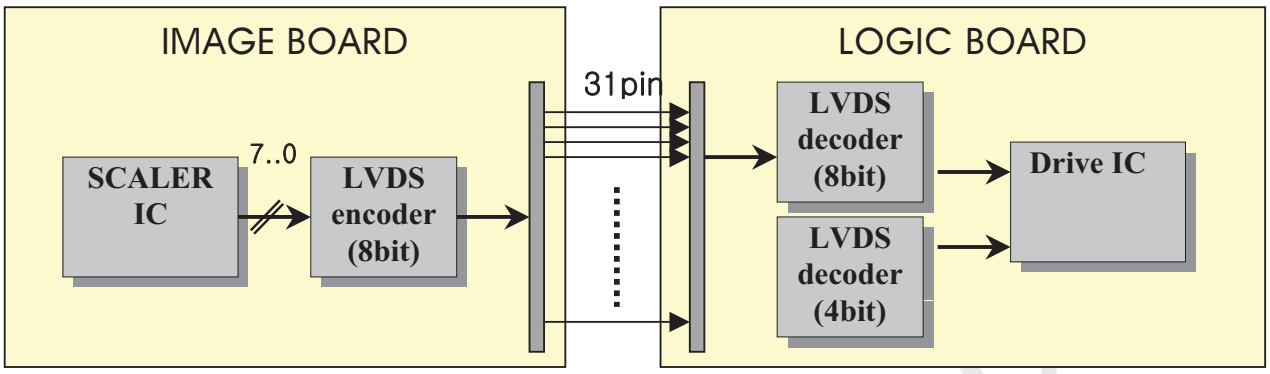
It is strongly recommended that the panel surface temperature should be kept as low as possible, eventhought its maximium rating is descreibed as above.

9.3.2. Panel Surface Temperature for Breaking

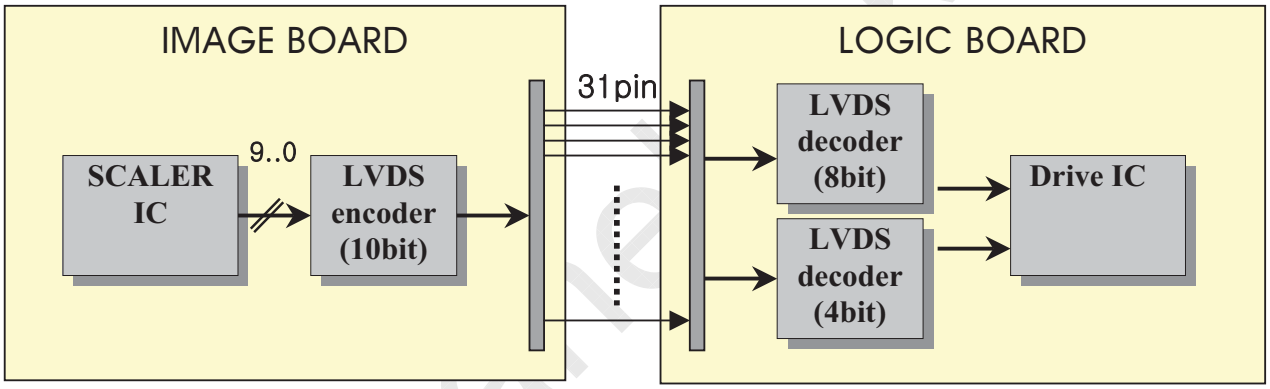
The temperature uniformity across panel should be maintained below 20℃/㎝ not to occure panel breaking by temperature difference.
This breaking temperature is not absolute temperature, because it depends on condition of panel production and panel scratch. Please take this value as a reference.

10. INTERFACE SIGNAL SPECIFICATIONS

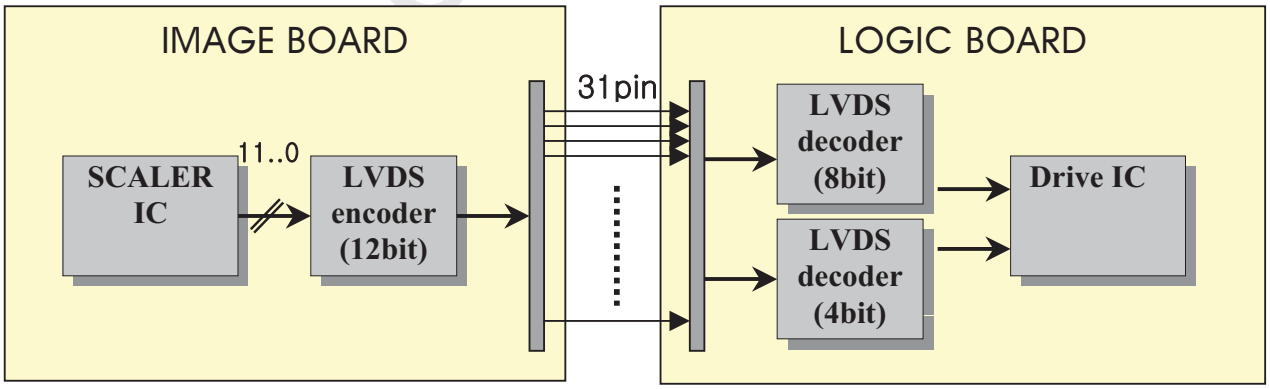
10.1 Configuration Context



[8Bit Interface]



[10Bit Interface]



[12Bit Interface]

10.2. Interface Function Specifications (input data and display processing)

- 1366-dot data signals are inputted to this product to display data.
- The Video signal and control signal input section uses a low voltage differential signaling (LVDS) interface.
- An I2C bus serial data interface is used for the communication between MPU of FTV side and the CLU (Control LOGIC Module) of this PDP Module.
- I2C_READY signal is used that the CLU(Control LOGIC Unit) of PDP module inform image scale b'd that CLU is ready for I2C communication.(1 : ready, 0 : not ready)

10.3. Input Signal Definition

No	Item	Signal name		Q	I/O	Method	Definition
1	Display Signal	Video Signal	RXIN0- RXIN0+ RXIN1- RXIN1+ RXIN2- RXIN2+ RXIN3- RXIN3+	1 1 1 1 1 1 1 1	Input (LVDS1)	LVDS Differentials	Differential serial data signal. Input video and timing signals after differential serial conversation using a dedicated transceiver. The serial data signal is transmitted seven times faster than the base signal.
			RXIN0- RXIN0+ RXIN1- RXIN1+	1 1 1 1	Input (LVDS2)		
		Dot Clock	RXCLKIN- RXCLKIN+	1 1	Input (LVDS1)	LVDS Differential	Differential clock signal. Input the clock signal after differential conversation using a dedicated transceiver. The clock signal is transmitted at the same speed as the base signal.
			RXCLKIN- RXCLKIN+	1 1	Input (LVDS2)		
2	MPU Communication	Communication	SDA SCL I2C_READY	1 1 1	Input	LVTTL (I2C)	I2C bus serial data communication signal. Communication with the CLU (Control Logic Module) of this product is enabled.

10.4. LVDS Signal Definition and Function

A video signal (display data signal and control signal) is converted from parallel data to serial data with the LVDS transmitter and further converted into four sets of differential signals before inputted to this PDP Module. These signals are transmitted seven times faster than the dot clock signals. The dot clock signal is converted into one set of differential signals.The LVDS signal definitions and functions are as follows (in Italic)::

(LVDS Default is 10Bit)

[8~12 Bit LVDS Interface]

Interface Signal Function			
Symbol	I/O	Function	Remarks
RxIN0-	I	Display Data Signal: R0, R1, R2, R3, R4, R5, G0	LVDS signal
RxIN0+	I		LVDS signal
RxIN1-	I	Display Data Signal: G1, G2, G3, G4, G5, B0, B1	LVDS signal
RxIN1+	I		LVDS signal
RxIN2-	I	Display Data Signal: B2, B3, B4, B5, Hsync, Vsync, Enable	LVDS signal
RxIN2+	I		LVDS signal
RxIN3-	I	Display Data Signal and Control Signal: R6, R7, G6, G7, B6, B7	LVDS signal
RxIN3+	I		LVDS signal
RxCLKin-	I	Dot Clock Signal: CLK	LVDS signal
RxCLKin+	I		LVDS signal
SDA	I	I2C serial data	3.3V CMOS
SCL	I	Clock signal for SDA	3.3V CMOS
RESET	I	No LVDS No Picture Flag	3.3V CMOS
I2C Ready	O	It indicates CLU ready for communication	3.3V CMOS

[8Bit LVDS Interface]

Interface Signal Function			
Symbol	I/O	Function	Remarks
RxIN0-	I	Display Data Signal: R2, R3, R4, R5, R6, R7,G2	LVDS signal
RxIN0+	I		LVDS signal
RxIN1-	I	Display Data Signal: G3, G4, G5, G6, G7, B2, B3	LVDS signal
RxIN1+	I		LVDS signal
RxIN2-	I	Display Data Signal: B4, B5, B6, B7, Hsync, Vsync, Enable	LVDS signal
RxIN2+	I		LVDS signal
RxIN3-	I	Display Data Signal and Control Signal: R8, R9, G8, G9, B8, B9	LVDS signal
RxIN3+	I		LVDS signal
RxIN0b-	I	Display Data Signal and Control Signal: R0, R1, G0, G1, B0, B1	LVDS signal
RxIN0b+	I		LVDS signal
RxCLKin-	I	Dot Clock Signal: CLK	LVDS signal
RxCLKin+	I		LVDS signal
SDA	I	I2C serial data	3.3V CMOS
SCL	I	Clock signal for SDA	3.3V CMOS
RESET	I	No LVDS No Picture Flag	3.3V CMOS

I2C Ready	O	It indicates CLU ready for communication	3.3V CMOS

[10Bit LVDS Interface]

Interface Signal Function			
Symbol	I/O	Function	Remarks
RxIN0-	I	Display Data Signal: R4, R5, R6, R7, R8, R9, G4	LVDS signal
RxIN0+	I		LVDS signal
RxIN1-	I	Display Data Signal: G5, G6, G7, G8, G9, B4, B5	LVDS signal
RxIN1+	I		LVDS signal
RxIN2-	I	Display Data Signal: B6, B7, B8, B9, HYNC, VSYNC, DEN	LVDS signal
RxIN2+	I		LVDS signal
RxIN3-	I	Display Data Signal and Control Signal: R10, R11, G10, G11, B10, B11	LVDS signal
RxIN3+	I		LVDS signal
RxCLKIN-	I	Dot Clock Signal: CLK	LVDS signal
RxCLKIN+			LVDS signal
RxIN0b-	I	Display Data Signal: R2, R3, G2, G3, B3, B3	LVDS signal
RxIN0b+			LVDS signal
RxIN1b-		Display Data Signal: R0, R1, G0, G1, B0, B1	LVDS signal
RxIN1b+			LVDS signal
RxCLKINb-		Dot Clock Signal: CLKb	LVDS signal
RxCLKINb+			LVDS signal
SDA	I	I2C serial data(Bi-direction)	3.3V CMOS
SCL	I	Clock signal for SDA	3.3V CMOS
RESET	I	No LVDS No Picture Flag	3.3V CMOS
I2C Ready	O	It indicates CLU ready for communication	3.3V CMOS

[12Bit LVDS Interface]

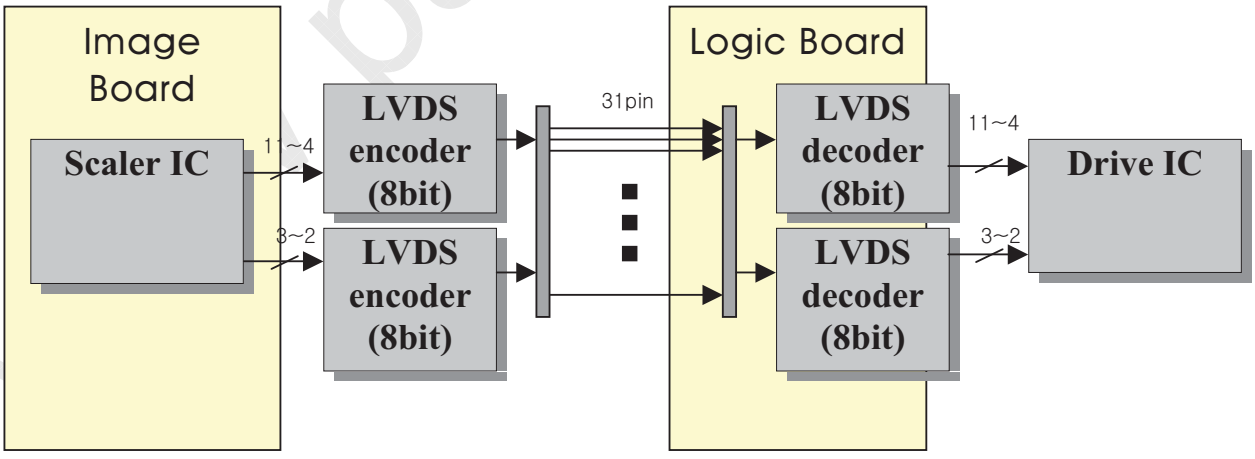


Figure-14. LVDS 10bit application(Default)

10.5 LVDS Signal Pin Assignment

The table below indicates pin assignment of the LVDS IC(Receiver).

Rx SIGNAL(Logic Board) (DS90CF386x2 ,National)						
Rx_Connector(CN2006)		LOGIC BOARD LVDS				
PIN	PIN Name	PIN No	PIN NAME	SIGNAL		
1	GND	26	RxCLKOUT	Dot Clock	LVDS1	OUTPUT
2	GND	27	RxOUT0	R(4)		
3	RxIN0-	29	RxOUT1	R(5)		
4	RxIN0+	30	RxOUT2	R(6)		
5	GND	32	RxOUT3	R(7)		
6	GND	33	RxOUT4	R(8)		
7	RxIN1-	34	RxOUT5	R(11)		
8	RxIN1+	35	RxOUT6	R(9)		
9	RxIN1b-	37	RxOUT7	G(4)		
10	RxIN1b+	38	RxOUT8	G(5)		
11	RxIN2-	39	RxOUT9	G(6)		
12	RxIN2+	41	RxOUT10	G(10)		
13	GND	42	RxOUT11	G(11)		
14	GND	43	RxOUT12	G(7)		
15	RxCLKIN-	45	RxOUT13	G(8)		
16	RxCLKIN+	46	RxOUT14	G(9)		
17	N.C	47	RxOUT15	B(4)		
18	N.C	49	RxOUT16	B(10)		
19	RxIN3-	50	RxOUT17	B(11)		
20	RxIN3+	51	RxOUT18	B(5)		
21	GND-	53	RxOUT19	B(6)		
22	I2C_READY	54	RxOUT20	B(7)		
23	RxIN0b-	55	RxOUT21	B(8)		
24	RxIN0b+	1	RxOUT22	B(9)		
25	IMG_EINT	2	RxOUT23	N.C.		
26	GND	3	RxOUT24	HSYNC		
27	SCL	5	RxOUT25	VSYNC		
28	GND	6	RxOUT26	DEN		
29	SDA	7	RxOUT27	R(10)		
30	GND	26	RxCLKOUT	Dot Clock		
31	N.C	27	RxOUT0	R(2)	LVDS2	
		29	RxOUT1	R(3)		
		30	RxOUT2	G(2)		
		32	RxOUT3	G(3)		
		33	RxOUT4	B(2)		
		34	RxOUT5	N.C.		

	35	RxOUT6	B(3)		
	37	RxOUT7	N.C.		
	38	RxOUT8	R(0)		
	39	RxOUT9	R(1)		
	41	RxOUT10	N.C.		
	42	RxOUT11	N.C.		
	43	RxOUT12	G(0)		
	45	RxOUT13	G(1)		
	46	RxOUT14	B(0)		
	47	RxOUT15	B(1)		
	49	RxOUT16	N.C.		
	50	RxOUT17	N.C.		
	51	RxOUT18	N.C.		
	53	RxOUT19	HSYNC		
	54	RxOUT20	VSYNC		
	55	RxOUT21	DEN		
	1	RxOUT22	N.C.		
	2	RxOUT23	N.C.		
	3	RxOUT24	N.C.		
	5	RxOUT25	N.C.		
	6	RxOUT26	N.C.		
	7	RxOUT27	N.C.		
	17	RxCLKIN−	Dot Clock	LVDS1	INPUT
	18	RxCLKIN+			
	9	RxINA−	R4~R9,G4		
	10	RxINA+			
	11	RxINB−	G5~G9,B4,B5		
	12	RxINB+			
	15	RxINC−	B6~B9,HSYNC,VSYNC,DEN		
	16	RxINC+			
	19	RxIND−	R10,R11,G10,G11,B10,B11		
	20	RxIND+			
RxINE− => RxINA− RxINE+ => RxINA+ RxINF− => RxINB− RxINF+ => RxINB+	9	RxINA−	R2,R3,G2,G3,B2,B3		
	10	RxINA+			
	11	RxINB−	R0,R1,G0,G1,B0,B1		
	12	RxINB+			

10. 6 Video Signal Definition and Function

The table below indicates the definitions and functions of input video signals before LVDS conversion.

Interfaces Signal Functions		
Symbol	**Function**	**Remarks**
R11(7) to R0	12(8) bits red video signal (note 1)	Display data signal: R12(8): MSB*, R0: LSB**
G11(7) to G0	12(8) bits green video signal (note 1)	Display data signal: G12(8): MSB*, G0: LSB**
B11(7) to B0	12(8) bits blue video signal (note 1)	Display data signal: B12(8): MSB*, B0: LSB**
Hsync	Horizontal synchronous signal	This signal specifies the data period for one horizontal line. Control of the next line begins at the rising edge of Hsync.
Vsync	Vertical synchronous signal	Timing signal that controls the start of the screen. Control of the next screen begins at the rising edge of Vsync.
DCLK	Clock for video signal	Latch the video signal at falling edge.

* MSB: Most Significant Bit
**LSB: Least Significant Bit

Note 1: The RGB signal may be compensated with Inverse γ circuit (E/D (=Error Diffusion) must be included) before inputted to the PDP Module. In order to obtain good characteristic of low level's gray scale, inverse γ correction and E/D process are advisory to be performed after inputted to the PDP Module.

Note 2 : Reommended Transmitter → DS90CF385x2

10.7 Electrical Condition of Interface Signal

10.7. 1. Maximum Ratings

Common conditions : Ta = 25℃, Vcc = 3.3V

Absolute Ratings						
Item			Parameter	Symbol	Ratings	Module
Input Signals	LVDS	Rx0-/+,Rx1-/+,Rx2-/+, Rx3-/+, Rx4/+, CLKin-/+	**Input Voltage**	**Vi**	**-0.3~3.6**	**V**
			Input Current	**Ii**	**-10~10**	**㎂**
	3.3V CMOS	SDA, SCL	Input Voltage	Vi	**-0.5~3.6**	V
			Input Current	**Ii**	**-15**	**㎃**

10.7. 2. Electrical Characteristics

Common conditions : Ta = 0℃ ~ +70℃, Vcc = 3.0V ~ 3.6V

Electrical Characteristics							
Signal	Item	Symbol	Conditions	Min.	Typ.	Max.	Module
LVDS	High level input voltage	V_{th}	V_{CM}=1.2V	-	-	100	㎷
	Low level input voltage	V_{tl}	V_{CM}=1.2V	-100	-	-	㎷
	Input current	I_{in}	V_{IN} = +2.4V/0V Vcc = 3.6V	-	-	±20.0	㎂
I2C	Input Voltage	V_{ih}		0.5*Vcc	-	4.1	V
		V_{il}		-0.5	-	0.3*Vcc	V
	Input Capacitance	V_{in}	-	-	-	8	pF
	Output Voltage	V_{oh}	I_{oh} = 8 ㎃	2.4	-	-	V
		V_{ol}	-	-	-	0.4	V
	Output Current	I_{ol}	-	-	-	10	㎃
3.3V CMOS	High level input voltage	V_{ih}	-	2.0	-	-	V
	Low level input voltage	V_{il}	-	GND	-	0.8	V
	Input current	I_i	V_I=Vcc or GND	-	-	±10.0	㎂
	High level output voltage	V_{oh}	Io = -1 ㎃	2.4	-	-	V
	Low level output current	V_{ol}	I_o = 1 ㎃	-	-	0.4	V

10. 8 Video Signal Interface Timing Conditions

The table below indicates the conditions of input video signal before LVDS conversion. These conditions must be satisfied. Refer to the figure of the timing chart.

8 bits LVDS ~12 bit LVDS belong to one timing table below.

Video Input Signal Timing (NTSC/PAL)			
Symbol	**Timing**	**Unit**	**Remarks**
TVSYNC	Refer to 'Remark'	Hz	- PAL long mode : below 48Hz - PAL Normal Mode : 48 ~ 52Hz - PAL LB Mode : 52 ~ 55 Hz - NTSC long Mode : 55 ~ 58 Hz - NTSC Normal Mode : 58 ~ 62 Hz - NTSC LB Mode : 62 ~ 65 Hz - NTSC Mask Mode : above 65 Hz * LB Mode(=Low Brightness Mode) : By decreasing sustain period on the Tvsync shorter than normal, brightness is reduced. * Mask(or Flicker) Mode : Masks abnormally short Vsync, and displays at the frame period twice as input Vsync period. * long mode : mode change is not occurred in this peried, the display is normally operation by increasing the Vsync period.

60Hz(NT)						
ITEM	SYMBOL		Min	Typ	Max	Unit
DCLK	Period	Tclk	13.5	—	14.08	ns
	Frequency		71	-	74	MHz
Hsync	Period	Thp	1451	—	—	Tclk
	Frequency	Fh	.	—	—	KHz
	Width	Twh	6	—	—	Tclk
Vsync	Period	Tvp	810	—	—	Thp
	Frequency	Fv	58	60	62	Hz
	Width	Twv	2	—	—	Thp
Data Enable	Horizontal Valid	Thv	1366	—	—	Tclk
	Horizontal Back Porch	Thc	56	-	-	Tclk
	Horizontal Front Porch	Tch	28	-	-	Tclk
	Vertical Valid	Tvv	768	—	—	Thp
	Vertical Back Porch	Tvh	8	—	—	Thp
	Vertical Front Porch	Thv	34	—	—	Thp

50Hz(PAL)						
ITEM	SYMBOL		Min	Typ	Max	Unit
DCLK	Period	Tclk	13.5	—	14.08	ns
	Frequency		71	-	74	MHz
Hsync	Period	Thp	1451	—	—	Tclk
	Frequency	Fh	.	—	—	KHz
	Width	Twh	6	—	—	Tclk
Vsync	Period	Tvp	810	—	—	Thp
	Frequency	Fv	48	50	52	Hz
	Width	Twv	2	—	—	Thp
Data Enable	Horizontal Valid	Thv	1366	—	—	Tclk
	Horizontal Back Porch	Thc	56	-	-	Tclk
	Horizontal Front Porch	Tch	28	-	-	Tclk
	Vertical Valid	Tvv	768	—	—	Thp
	Vertical Back Porch	Tvh	8	—	—	Thp
	Vertical Front Porch	Thv	34	—	—	Thp

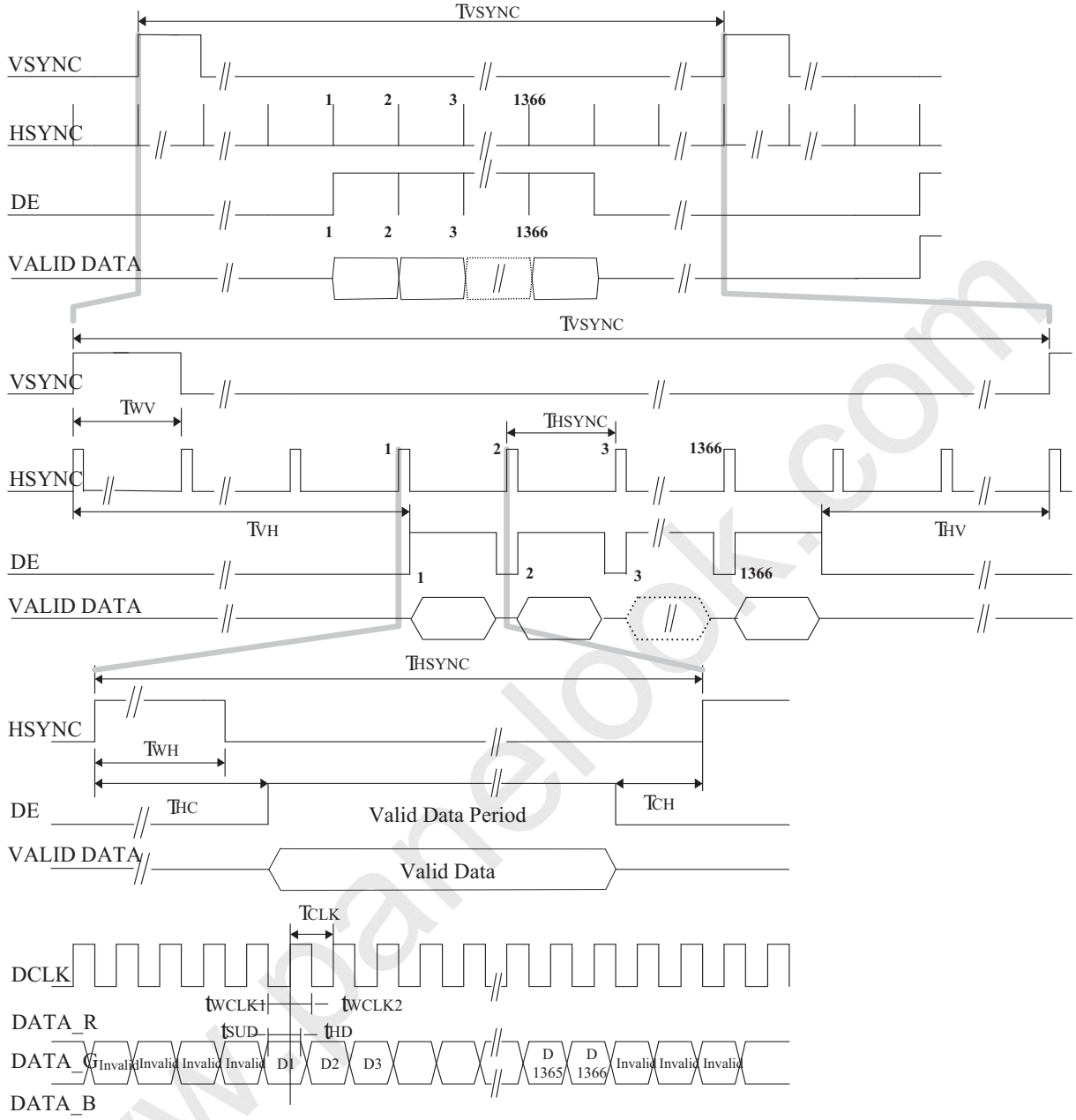


Figure-15. Video Input Signal Timing Chart

10. 9 LVDS Interface Timing Conditions

This PDP Module uses an LVDS interface for the signal input. For details of the input signal timing conditions, refer to the data sheets prepared by the LVDS transmitter IC maker. This PDP Module uses **National Semiconductor (www.national.com)**'s DS90CF386

10. 10 LVDS Connection Specifications

The following Figure shows the connection specifications and signal assignments of the LVDS interface IC. Do not connect or disconnect the connector when the system power in on. Otherwise, the LVDS interface IC could be damaged.

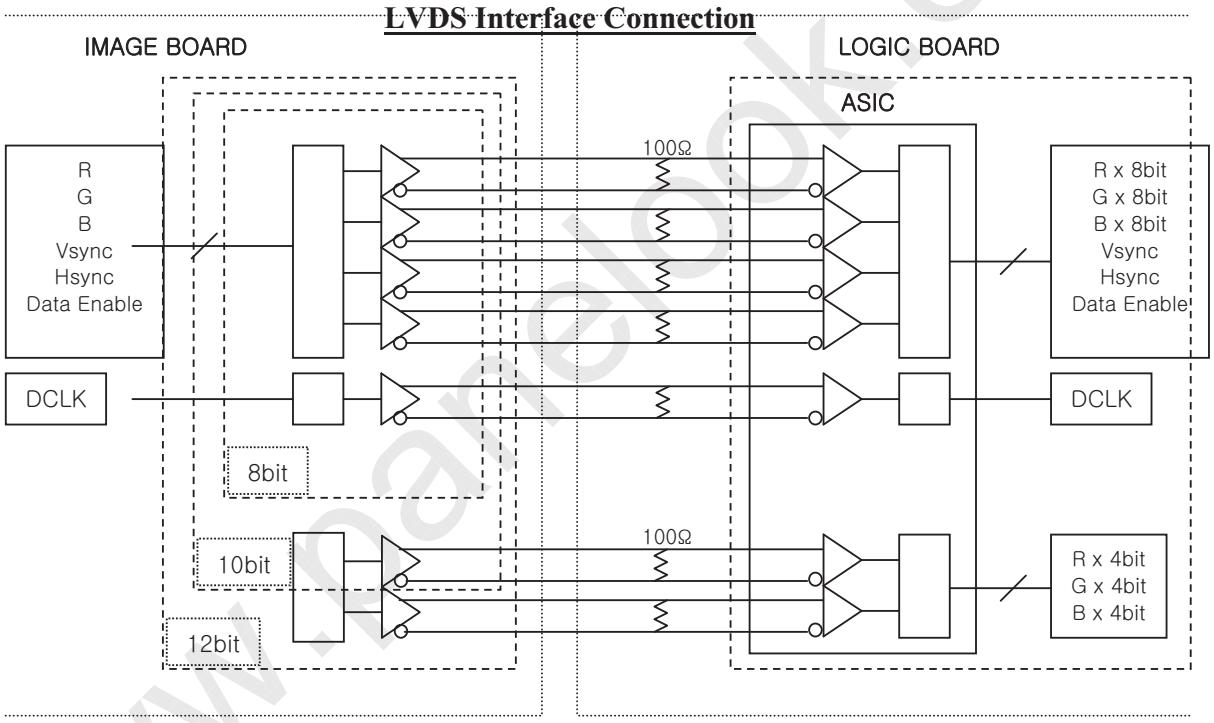


Figure-16. LVDS Interface Connection

10. 11 I2C Interface Conditions

10. 11. 1 Basic Specifications

This PDP Module has the I2C bus serial data communication function.
The customer may use this function to make settings for PDP Module characteristics of several items.

No	Parameter	Specifications
1	**Recommended** Transfer Rate	**50 kbps**
2	Device Status	Slave Receiver
3	Slave Address	CC(Write), CD(Read)

10. 11. 2 I2C–Ready Signal

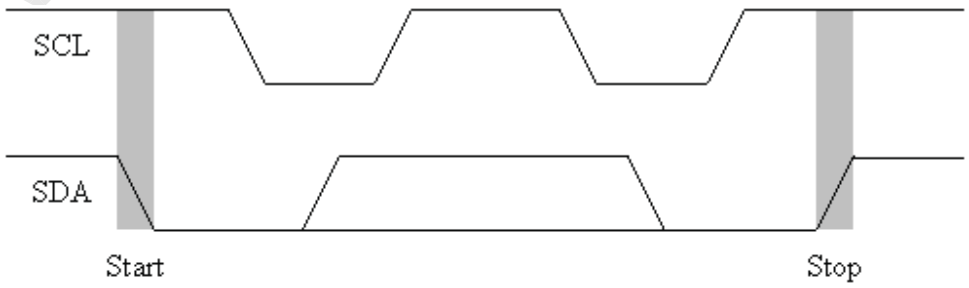
I2C control is available only when I2C-Ready signal is 'High' state.
I2C-Ready signal is assigned to pin number 22 of CN2020

10. 11. 3 Data Validity

Amount of data that is transferred is 1-Bit per 1 SCL cycle. Data is valid when SCL is high and recognized as to state of SDA.

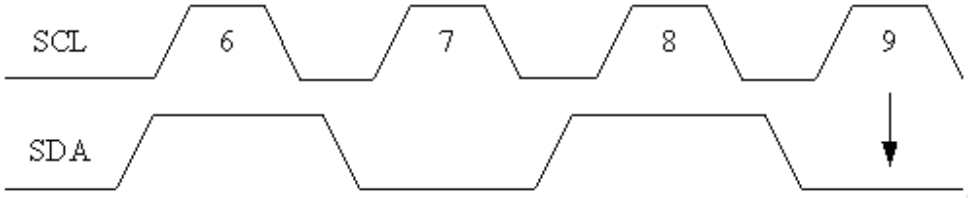
10. 11. 4 Start & Stop Condition

Start /Stop condition is generated by Master (=Image B'D). Before start condition or after stop condition, a SDA cannot be recognized as valid data.
Start condition ☞ SCL high & SDA transition from H to L
Stop condition ☞ SCL high & SDA transition from L to H



10. 11. 5. Acknowledge

When Master (=Image B'D) needs to stop reading data, the master should give NO ACK signal to salve by SDA. Slave (=PDP Module) gives ACK whenever 8-bit transfer is done.



10. 11. 6. 7-Bit Addressing for Device address(with example of CC or CD)

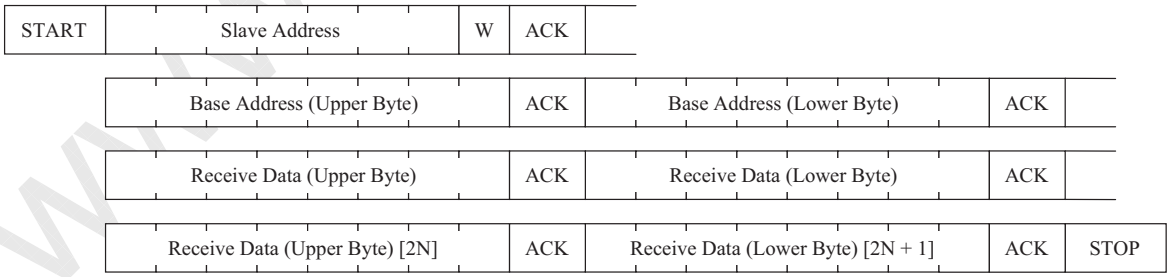
Master could choose slave by 7-bit slave address and decide what procedure is by R/W bit (H=Read procedure, L=Write procedure).

10. 11. 7. 16-Bit Mode

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

10. 11. 8 . Data Transfer Sequence (Write)

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').
Note 1: Black letters mean master (=Image B'D)'s bus occupation.
Note 2: Blue letters mean slave (=PDP Module)'s bus occupation.



10.11. 9. Data Transfer Sequence (Read)

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

Note 1: In advance, master should initialize writing sequence by giving base address and stop condition.

Note 2: After start condition and slave addressing, master could receive data from slave.

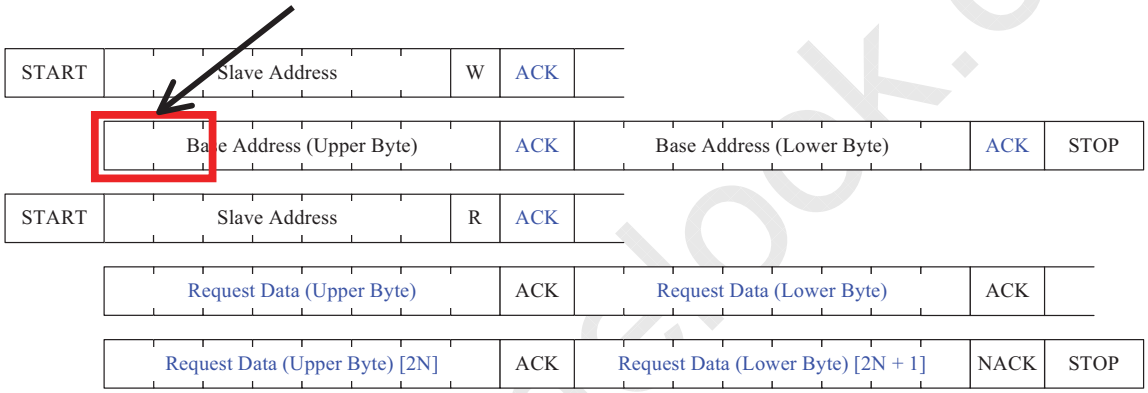
Note 3: Master should give acknowledge whenever 8-bit data is received.

Note 4: 'No acknowledge' could make master give stop condition on bus. Therefore, NACK is used for master to stop receiving data from slave.

Note 5: Black letters mean master (=Image B'D)'s bus occupation.

Note 6: Blue letters mean slave (=PDP Module)'s bus occupation.

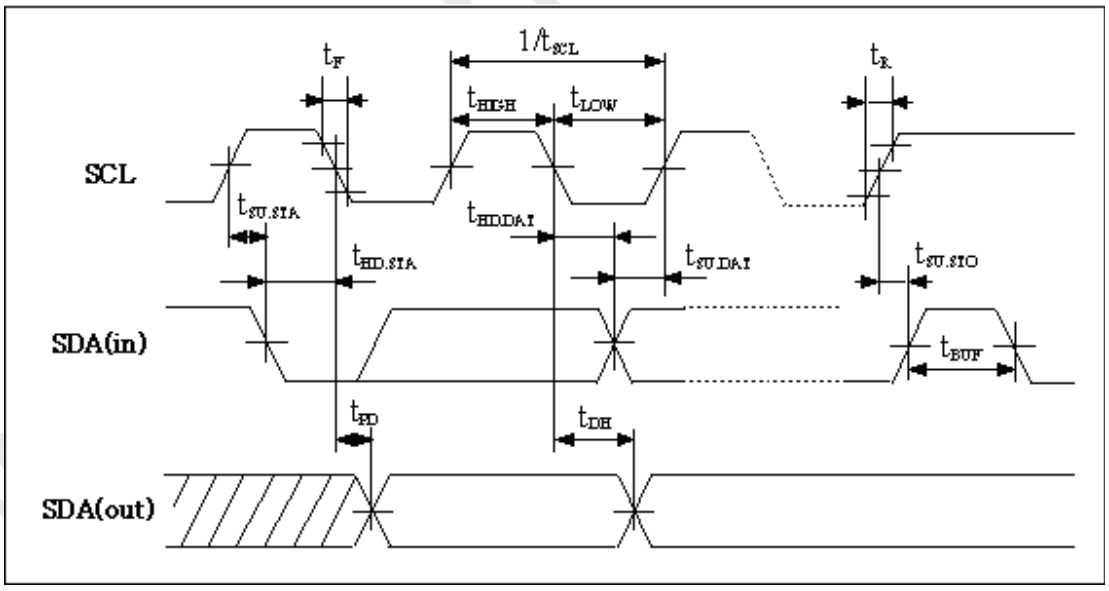
Note 7: **Option Bit = 10: RAM (in ASIC)**



10. 11. 10. I2C Bus Timing Specifications

* Refer to the following data merely as sample data.

No	Item	Symbol	Standard			
			Min.	Typ.	Max.	Module
1	SCL Input Frequency	f_{SCL}	-	50	**75**	kHz
2	SCL Input "HIGH" Period	t_{HIGH}	0.3	-	-	μs
3	SCL Input "Low" Period	t_{LOW}	0.5	-	-	μs
4	Start Condition Set Up Time	$t_{SU.STA}$	0.3	-	-	μs
5	Start Condition Hold Time	$t_{HD.STA}$	0.3	-	-	μs
6	Data Input Set Up Time	$t_{SU.DAT}$	0.1	-	-	μs
7	Data Input Hold Time	$t_{HD.DAT}$	0	-	-	μs
8	Stop Condition Set Up Time	$t_{SU.STO}$	0.3	-	-	μs
9	Data Output Delay Time	t_{PD}	0.1	-	-	μs
10	Data Output Hold Time	t_{DH}	0.1	-	-	μs
11	SDA Bus Free Time	t_{BUF}	0.5	-	-	μs
12	SCL, SDA Input Rising Time	t_R	-	-	0.8	μs
13	SCL, SDA Input Falling Time	t_F	-	-	0.3	μs
14	SCL, SDA Line Capacitor	C_b	-	-	400	pF

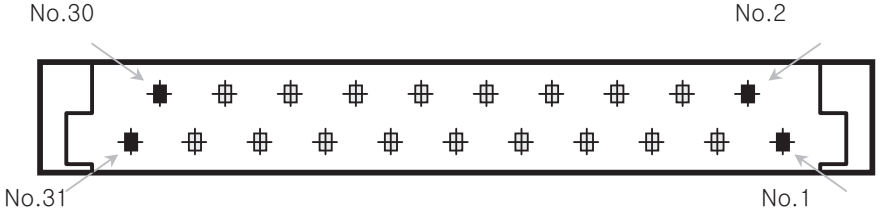


10. 12. Connector Specifications

Connector Name	Pin #	Signal Name
CN2006	3	TxOUT0-/RxIN0-
	4	TxOUT0+/RxIN0+
	7	TxOUT1-/RxIN1-
	8	TxOUT1+/RxIN1+
	9	TxOUT2-/RxIN1b-
	10	TxOUT2+/RxIN1b+
	11	TxOUT3-/RxIN2-
	12	TxOUT3+/RxIN2+
	15	TxCLKOUT0-/RxCLKIN-
	16	TxCLKOUT0+/RxCLKIN+
	17	TxCLKOUT1-/RxCLKINb-
	18	TxCLKOUT1+/RxCLKINb+
	19	TxOUT4-/RxIN3-
	20	TxOUT4+/RxIN3+
	22	I2C-READY
	23	TxOUT5-/RxIN0b-
	24	TxOUT5+/RxIN0b+
	25	IMG_EINT
	27	SCL (SEE notes 6)
	29	SDA (SEE notes 6)

NOTES:

1. CN2006 connector is located in Logic Board.
2. Pin to Pin pitch of connector CN2006 is 0.625㎜.
3. The length of mating cable to CN2006 is recommended to be not longer than 25.0㎝.
4. Pin numbering order :
   right to left view from component side of Logic Board.
5. All the other pins are GND.
6. Reserved for factory use only. This pin should be disconnected in case of customer's use.
7. This pin is output pin. In case of fan failure, this signal becomes high.



11. ADDRESS MAP

11.1 Address Map

The I2C address map has three regions, i.e. NTSC / PAL common system area, NTSC-only system area and PAL-only system area..
The sub-address table shown below is for NTSC. The sub-address region for NTSC is 0000h~1FFFh, and that of PAL is 2000h~3FFFh
Basically address map for PAL is same as that of NTSC except the offset address. For example, 0080h for NTSC is correspondent to 2080h for PAL.

- I2C Slave Address ☞ Write: 66 (hex), Read: 66 (hex)

Sub Address	Data																Note
AF~0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0080			PS														R/W
0081					DL												R/W
00E1									APCO								R/W

[Note]

1. Only sub-addresses shown in above table are allowable for access. An access to the any other address than shown in above sub-address table may lead to an abnormal system down or permanent damage.
2. 0000~007F : Area for NTSC/PAL common system registers .
   0080~1FFF : Area for NTSC-only system.
   2080~3FFF : Area for PAL-only system.

11.2 Details of Settings

Sub Address	Data Bit	Sym bol	Item / Function	Setting [hex]			Note
				Range	Initial		
					NT	PAL	
0080(NT) 2080(PAL)	8~13	PS	**Pattern Select** ☞ Patterns below are valid when IE (Internal clk or External clk) is set to '1'. 00: Full Window (Black) 01~04: Full Window (White,Red,Green,Blue) 05 : 1 point Box(White, Windows size) 06~09: 9 Point Box (White,Red,Green,Blue) 0A : 1% Window , 0B: Color Bar 0C~0D: Gray Bar (Horizontal, Vertical) 0E: Half Gray, 0F:Cross Hatch, 10:Dot Array, 11:3% widow 12~13: 16step Gray Bar (Vertical, Horizontal) 14~15: Vertical Ramp Pattern (Stay, Scroll) 16~17: Horizontal Ramp Pattern (Stay, Scroll) 18 : Horizontal Ramp WRGB Pattern	00~17	01	01	*(a)
0081	8~15	DL	**Data Level** ☞ Patterns below are valid when **IE** (Internal clk or External clk) is set to '1'. 00~FFF : 0~ 4095 Gray Level.	000~FFF	FFF	FFF	*(a)
00E1(NT) 20D1(PAL)	0~7	APCO	**APC Offset Level** ☞ Adjusts peak luminance for customer's specifications.	00~C7	00	00	*(c)

*(a) Please access these address for test use only.
For ordinary operating conditions, values of these address should be set to initial values.
*(b) Customers can set these values considering their specifications.
*(c) APCO is used for control the "Brightness" of PDP Module. For a detailed behavior and variable range, refer to the Chapter 6.

12. INPUT POWER VOLTAGE SPECIFICATIONS

12.1 Electrical Characteristic Overview for PDP Module Voltages

Output Name	Nominal Voltage(V)	Output Current			(*1)Load Regulation (%)	(*2)Variable Range(V)	Remark
		Min.	Nor.	Max			
Vs	+198V	0.1A	1.3A	1.6A	±1.5	190V~215V	Sustain voltage
Va	+60V	0.1A	1.6A	2.0A	±1.5	50V~72V	Address voltage
Vscan	-190V	0.01A	0.08A	0.15A	±1.5	-220V~-180V	Scan voltage
Vset	+190V	0.01A	0.05A	0.07A	±1.5	180V~220V	Reset voltage
Ve	+120V	0.01A	0.05A	0.07A	±1.5	90V~130V	Bias voltage
Vg	+15V	0.1A	0.5A	1.5A	±5	Fixed	Drive gate in FET
D5V	+5.2V	0.1	-	2.5	±5	Fixed	Logic in X,Y driving
D3V3	+3.4V	0.1	2.0A	4.0A	±5	Fixed	Drive IC in Logic

*1. This means nominal voltage stability when current is changed from min to max.

*2. The output voltages for Vs, Va, Vscan, Vset, Ve could be varied within variable range by feedback variable resistors.

■ Above voltage levels are norminal value. They are adjustable to drive Panel.

12.2 Electrical Characteristic Overview for Image voltages

Output Name	Nominal Voltage(V)	Output Current			Load Regulation (%)	Variable Range(V)	Remark
		Min.	Nor.	Max			
D5V	+5.2V	0.1A	1.0A	2.0A	±5	Fixed	Image Board
D3V3	+3.4V	0.1A	2.0A	4.0A	±5	Fixed	Image Board
A12V	+12V	0.1A	1.6A	2.0A	±5	Fixed	Image Board
Vamp (*3)	+12V	0.1A	3.1A	4.0A	±5	Selectable 12V or 24V	Image Board (Defalt 12V)
	+24V	0.1A	1.4A	2.0A			
33Vt	+33V	-	0.01A	0.01A	±10	Fixed	Image Board
5VSB	+5.2V	0.1A	1.0A	2.0A	±5	Fixed	Image Board

*3. Vamp: Default 12V setting, Do not change 12/24V Jumper setting.

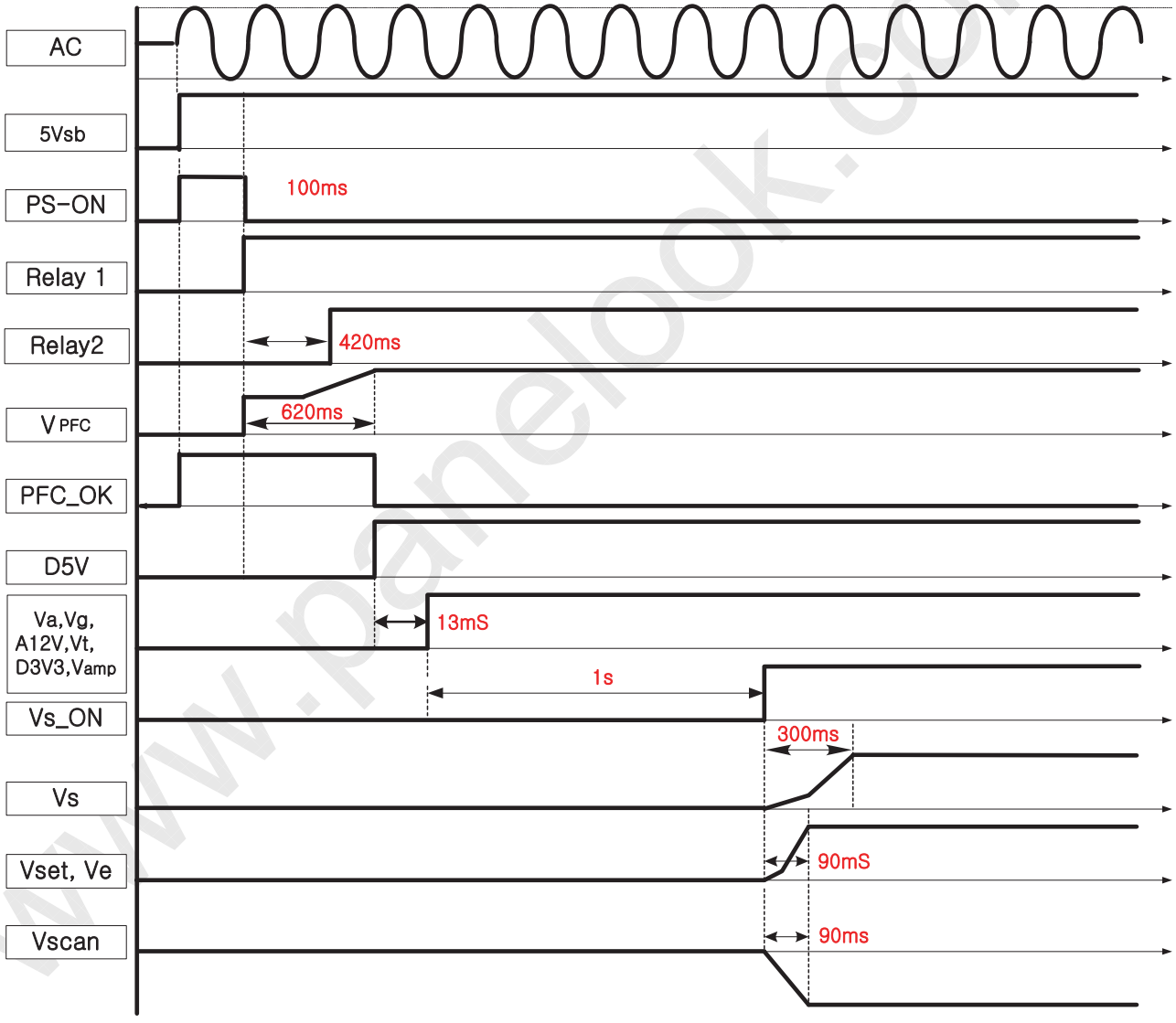
Notice: Confirm 12V/24V Jumper position before use.

12.3 Out Dimension for reference

Length(mm)	Width(mm)	Height(mm)	Remark
360mm	245mm	Max. 42mm	From PCB top

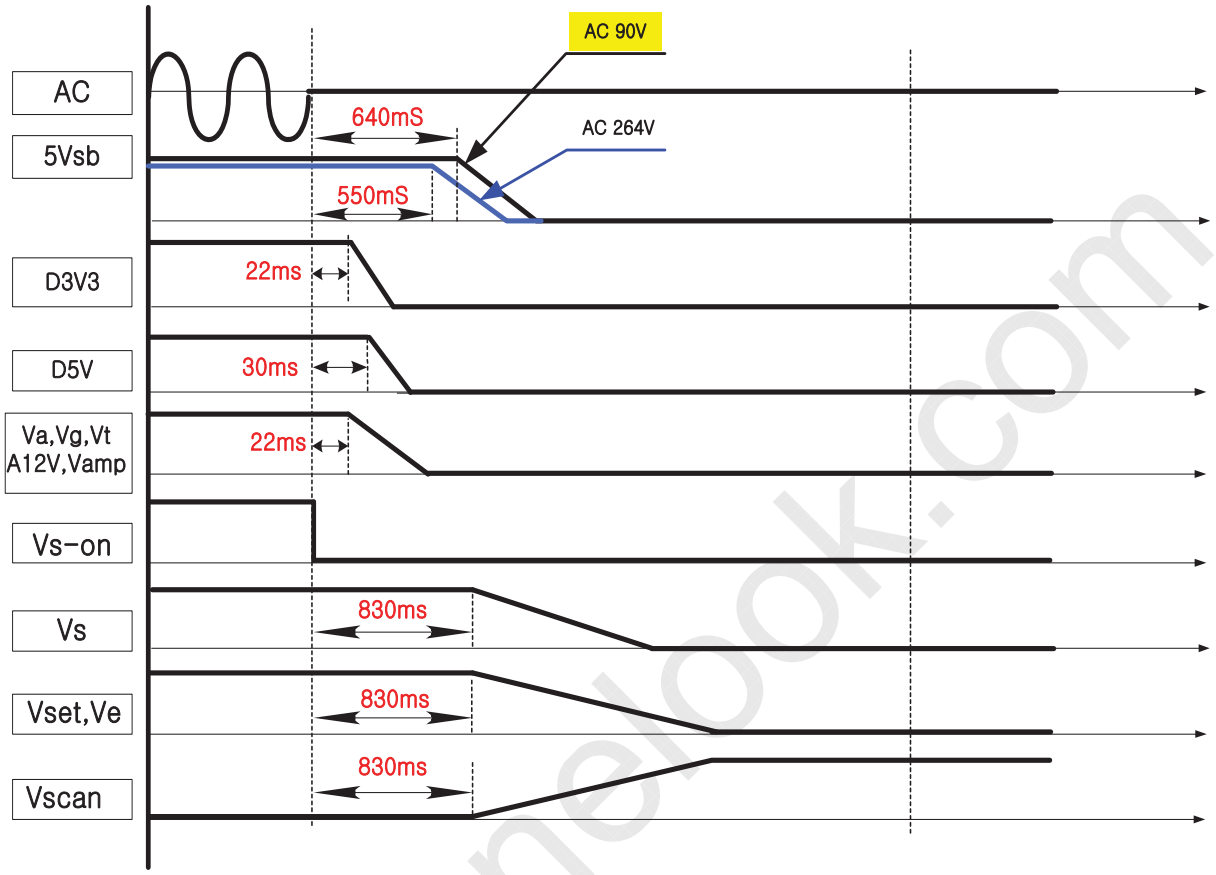
12.4 Power Applying Sequence

► AC_ on Sequence



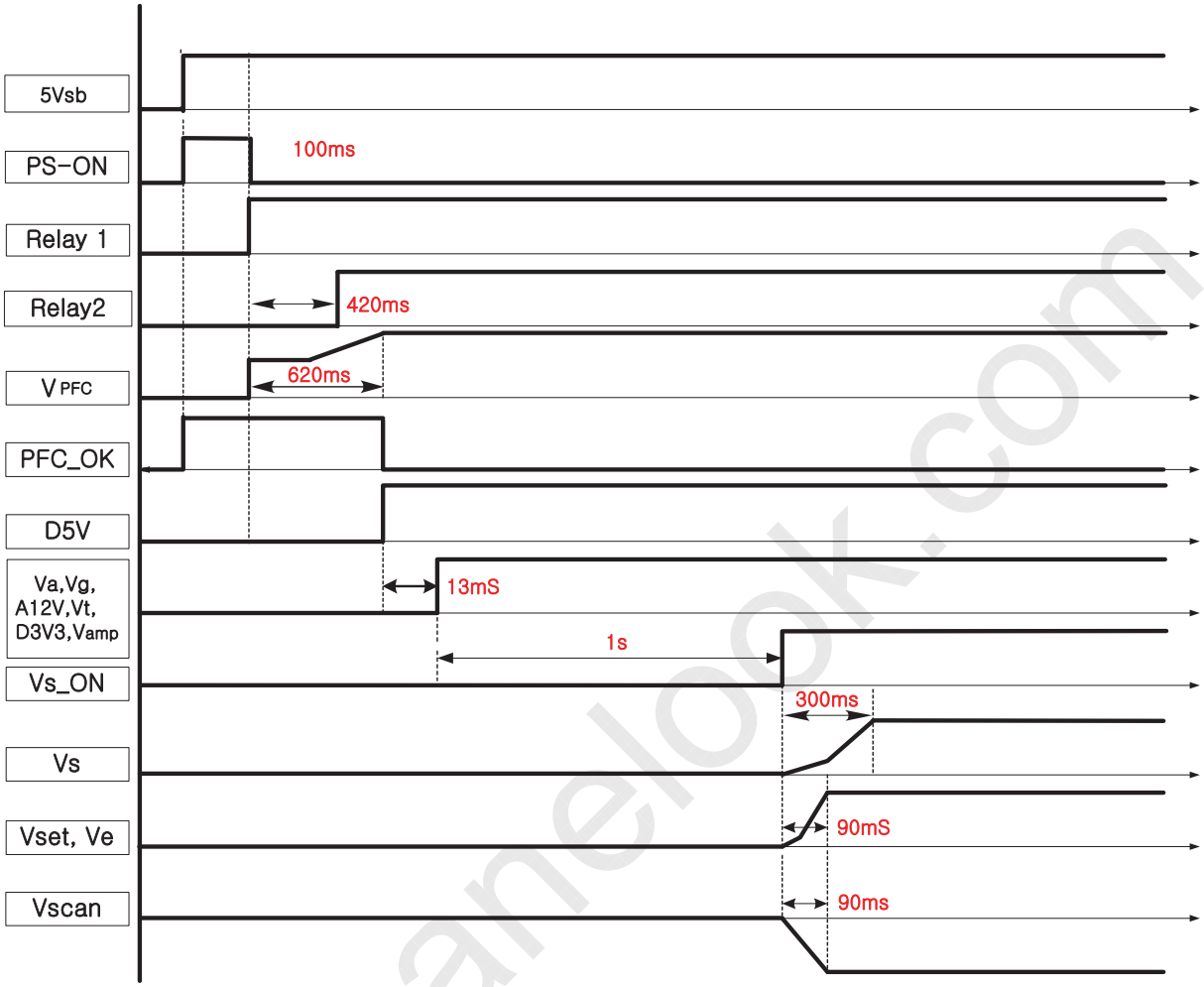
*1. Reference value.
*2. Vs_on signal is output from Logic board to PSU.
*3. Vs should be enable with Vs_on signal(Active High) from Logic.
*4. Vs should be always higher than Ve while D3V3 is alive.
*5. I2C Ready signal is output from Logic board to Image board.

► **AC_off Sequence**

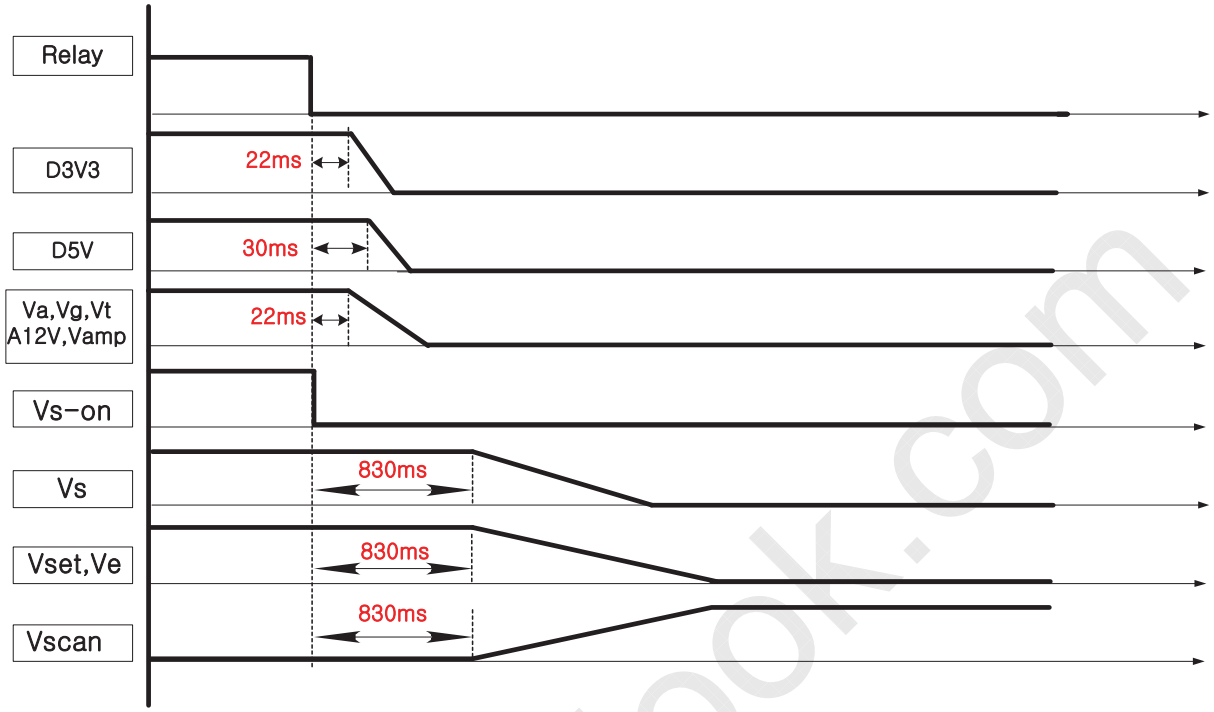


***1. D3V3 discharge should be faster than other voltages.**
D3V3 should discharge before Vg voltage level is 11V and Vs voltage level is lower than Ve.
■ Either spontaneous discharge or active discharge is available for PFC, Vs, Va, Vset, Vscan, Ve as long as D3V3 has discharged before other voltages.

► **Relay_on Sequence**



► **Relay_off Sequence**



12.5 Pin assignment of connectors for Power Supply

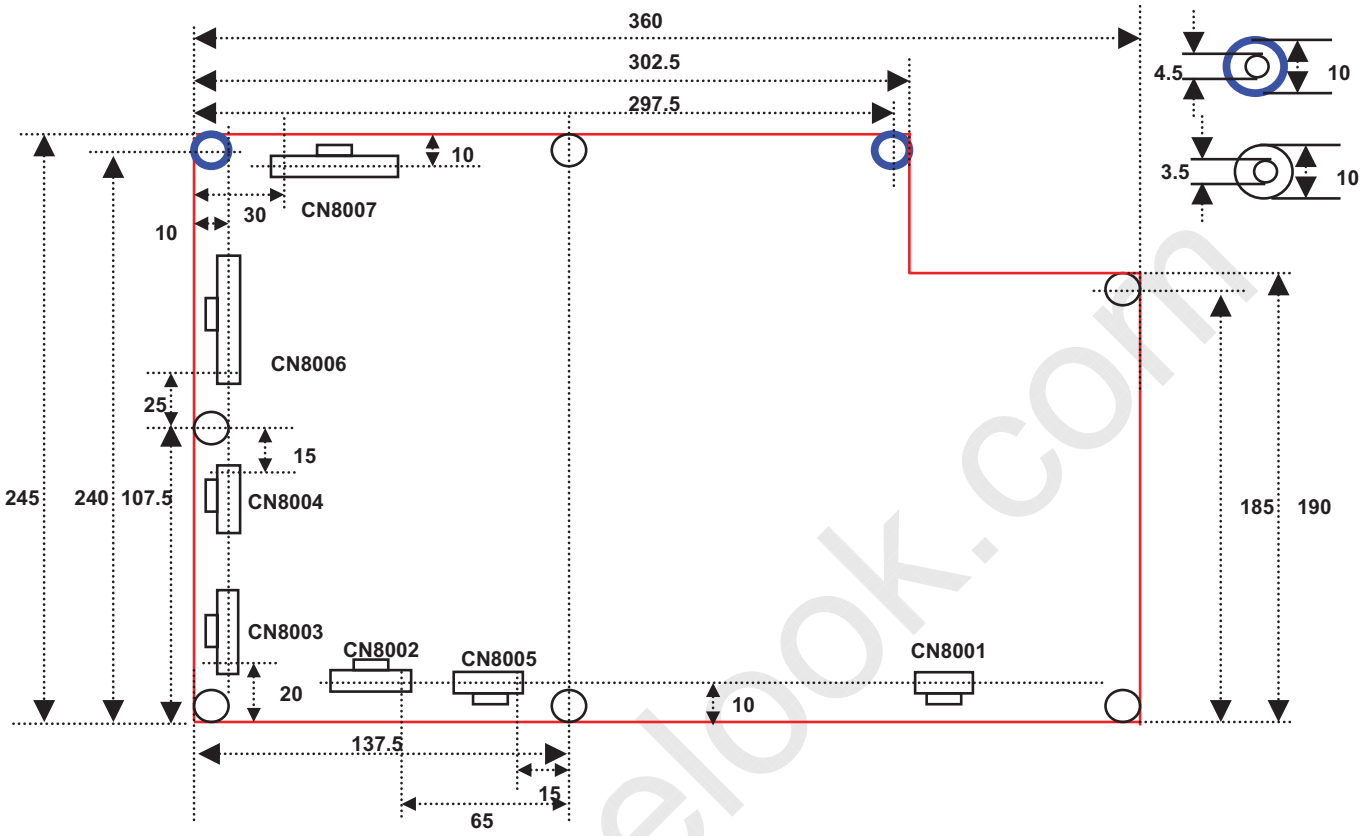
Location No.	CN8001	CN8007	CN8006	CN8004	CN8005	CN8003	CN8002
Function	AC Input	X-Main	Y-Main	Image	Buffer	Image	Logic
No. of Pin	3 pins	8 pins	9 pins	10 pins	5 pins	11 pins	10 pins
Con. Type	JST B2P3-VH	Molex 35313-0960	Molex 35313-1060	Molex 35312-1060	Molex 35313-0560	Molex 35312-1160	Molex 35312-1060
Pin No.	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**
1	Netural	D5V	D5V	D5V	Va	D5V	D3V3
2	N.C	Vg	Vg	GND	N.C	GND	D3V3
3	Live	GND	GND	A12V	D5V	D3V3	GND
4		GND	Vscan	GND	N.C	D3V3	GND
5		Ve	GND	Vamp	GND	GND	D5V
6		GND	Vset	Vamp		GND	GND
7		GND	GND	GND		**A12V**	Relay
8		Vs	GND	GND		**(*1)**PS-ON	AC_DET
9		Vs	Vs	Vt		GND	Vs_on
10			Vs	GND		Vsb	D5V
11						**(*2)**THEM_DET	

***1. This is a signal(Active low) from image board to Logic main. (High : 3.3V, Low : 0V)**

***2. Stand By Power Consumption**
Max. 0.65W (condition : Module M3, Input Voltage 240Vac/60Hz)

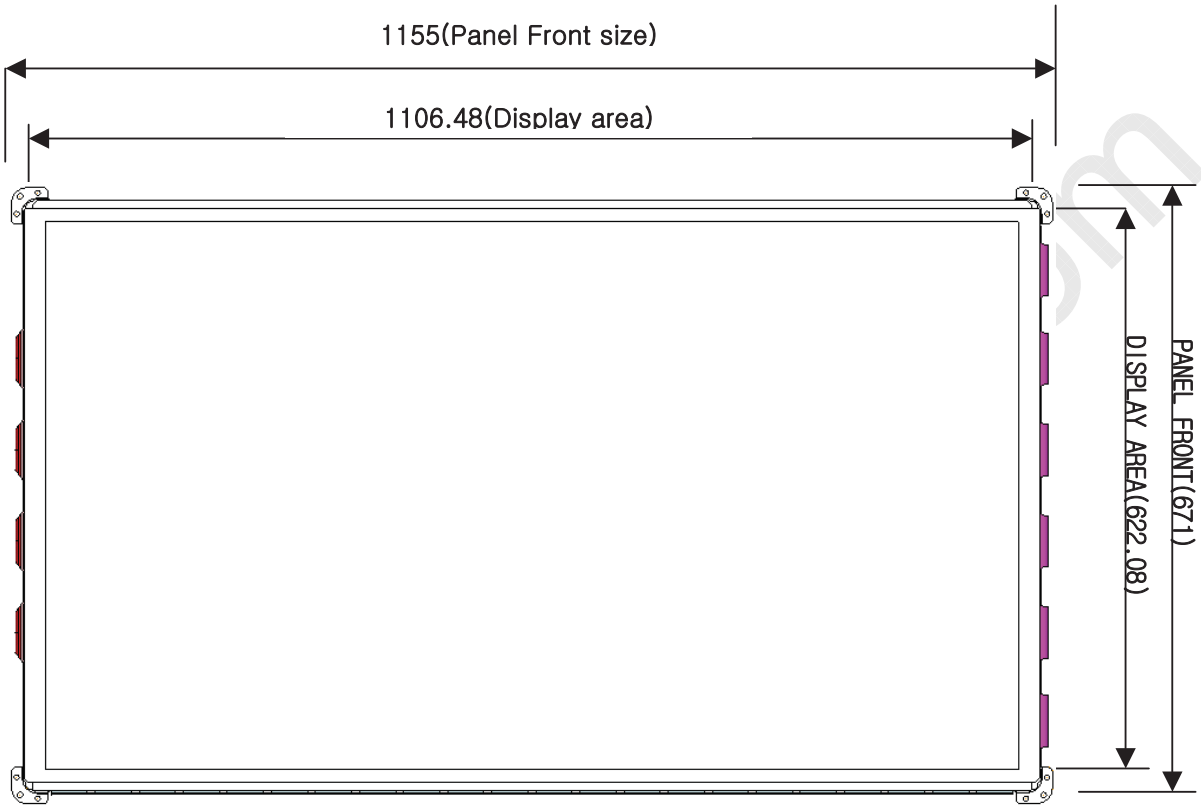
***3. This is a signal from PSU to image board (Overheat : 5V, normal : 0V)**
It stop the PSU when THEM_DET is high.

12.6 Mechanical Out Drawing



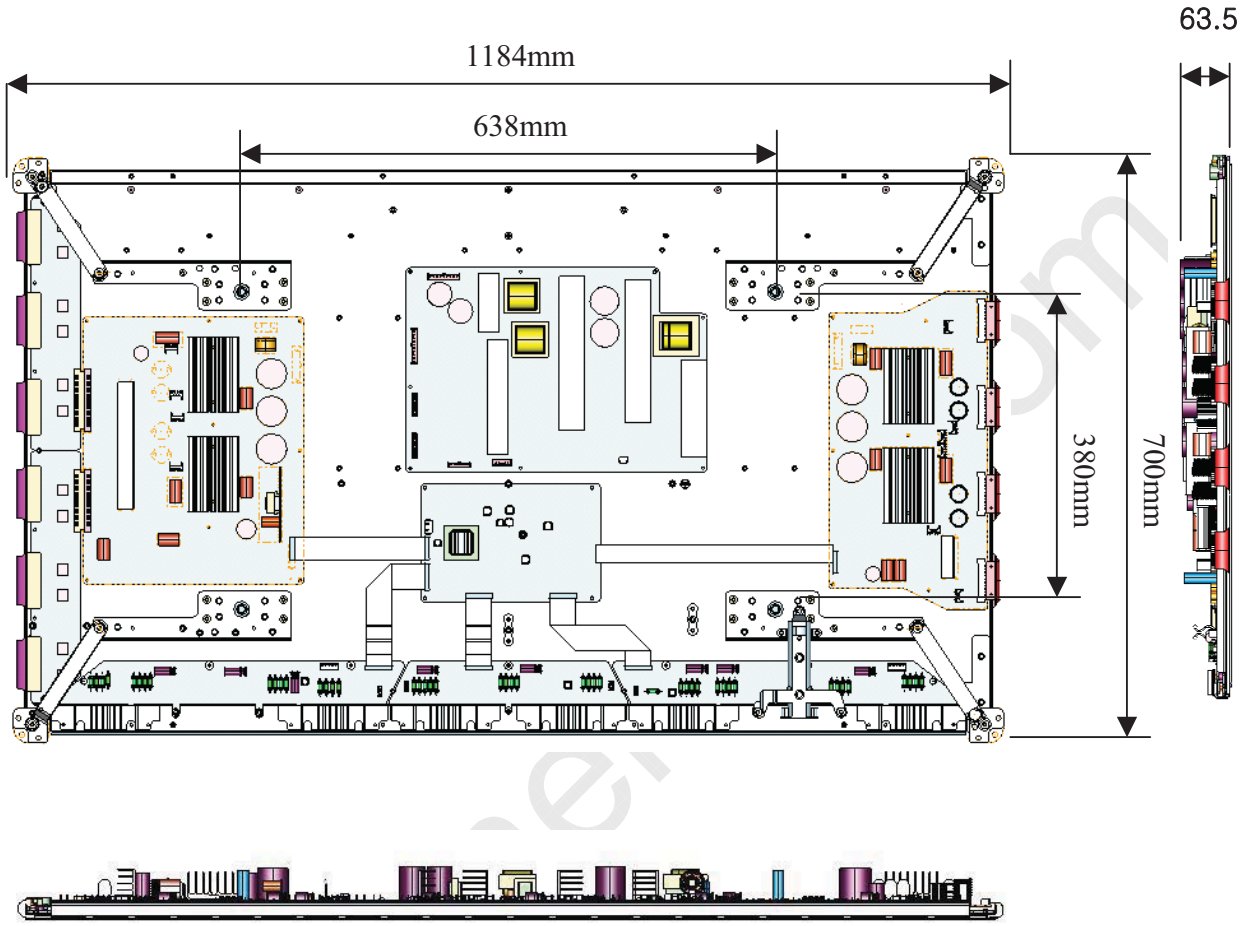
13. MECHANICAL DIMENSION DRAWING

13.1. Front Side



Appendix A1

13.2. Rear Side

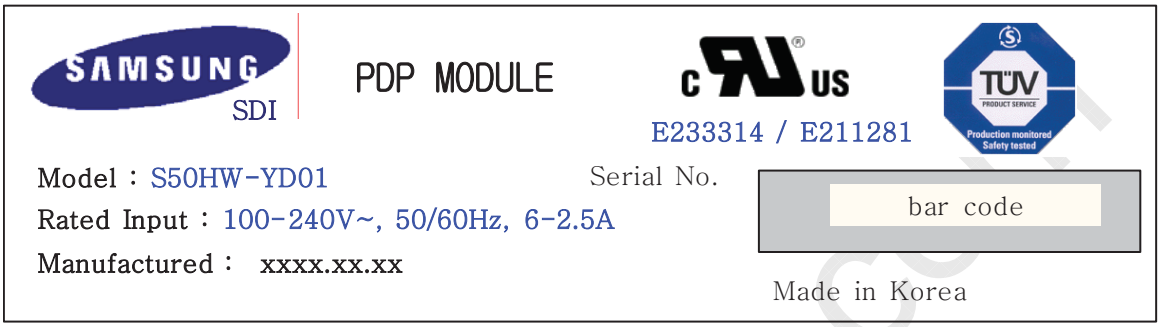


Appendix A2

14. LABEL

14.1 Label Type

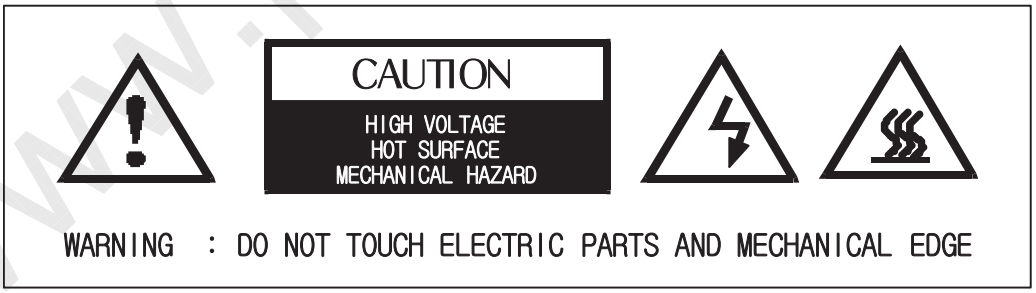
(1) Label for the PDP Module



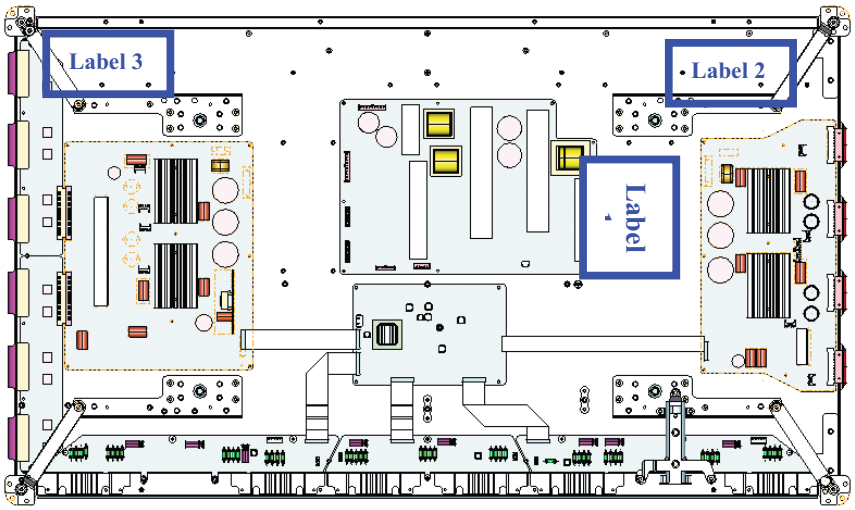
(2) Label for power specification

☐ NTSC			☑ NTSC/PAL	
Va	Vsc	Vs	Ve	Vset
65	-190	198	120	190

(3) Caution Label



14.2 Label location



【 Notes 】

1. Label-1 is a label for the PDP Module.
2. Label-2 is a label for the power specification.
3. Label-3 is a lable for the Caution Label

14.3 Serial No.

Panel ID

12	1	4	A	03	00001
Model	Line	Year	Month	Date	No.

Model (50HD_V5 : 55)

Month (Hex: 1~9 digit (Oct.- A , Nov.- B, Dec.- C))

Module ID

C	001	A	4	9	03	A	0001
Area	Model	Line No.	Year	Month	Date	Group	No.

① Area(C: Chonan factory , S: Shenzhen factory)
② Model: 3 digit
③ Module production line : A ~ Z
④ Year : 1 digit,Rotate every decade
⑤ Month (Hex: 1~9 digit (Oct. -A , Nov.-B, Dec.-C))
⑥ Group : A Group, B Group, C Group

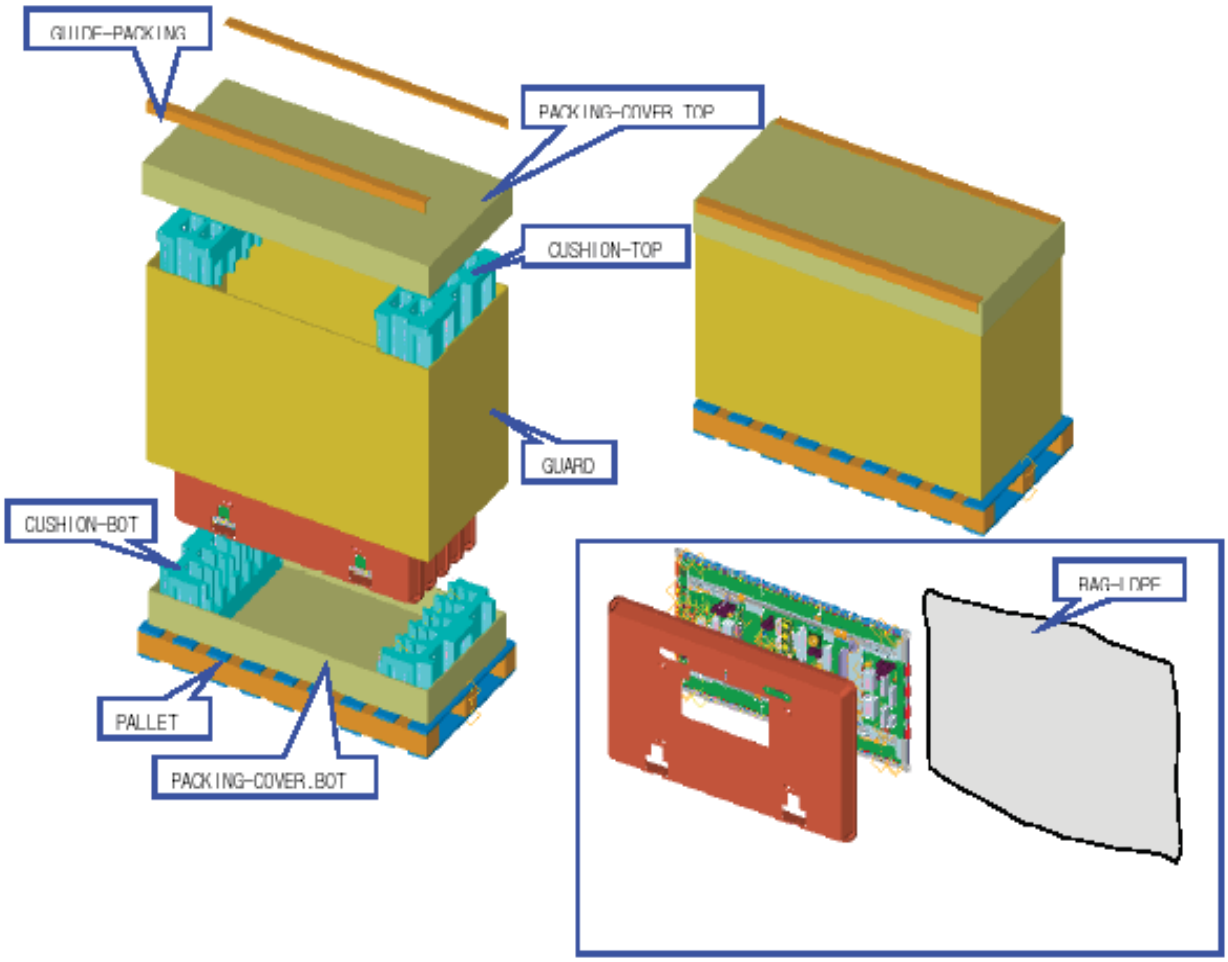
15. PACKING

15.1 Packing Dimension and Parts List

- **Number of Module in 1 package: 5Modules**
- **Packing dimensions (W*L*H): 1465*760*1106 (mm) (Including Pallet :136mm)**
- **Weight: About 209 ± 5 (Kg)**

No.	Parts	Specification	Q'ty	Remarks
1	Bag PE	W1229,L723,T0.5	1,000	(Unit: Module 1,000 pcs)
2	Silicagel(DRY-PAK)	100g	2,000	
3	Packing-Module	HIPS,HB,BLK	1,000	
4	Screw,Machine	PH,+,M8,L25	4,000	
5	Pallet	L1465,W728,H136	200	
6	Packing-Cover-Top	DW 1745 × 1007 × 10T	200	
7	Packing-Cover-Bot	DW 1745 × 1007 × 10T	200	
8	Cushion-Set	50HD,EPP,C=0.022	200	
9	Band,PE	T1,W18mm	800M	
10	Guide,Pack	L1465,D50,T5	400	

15.2 Packing Assembly Drawing



16. RELIABLITY

16.1 Expected Service Life

#1. Definition

The expected service life is defined by the following two categories.
And the life time is defined by either (1) or (2), whichever occurs first.

(1) The white color Luminance level becomes half (50%) of its initial value, which is determined by the phosphor characteristics.

(2) The number of display cell defects increases to double the specification value, which is depending on the discharge characteristics.

#2. Test condition and life time

The expected service life time varies depending on the display conditions set forth below.

(1) Full screen white color display

Life time : 60,000 hours (include PCBA)

16.2 Disclaimer

This Specification stipulates the final and comprehensive requirements for the respective products hereof. Beyond this Specification, it is the responsibility of the customer to explicitly disclose any additional requirements, information or reservations regarding these requirements to Samsung SDI prior to implementation, where any and all disclosures of the customer shall be with an authorized representative of Samsung SDI in writing. Samsung SDI shall not be responsible for safety, performance, functionality or compatibility of the system with which the Samsung SDI-supplied components are integrated unless such features have been expressly communicated and described in the Specification. SAMSUNG SDI MAKES NO GUARANTY OR WARRANTY, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, TO ANY PARTY. Moreover, any party should do their own due diligence regarding these requirements prior to implementation

17. WARNING / CAUTION / NOTICE

TO PREVENT POSSIBLE DANGER, DAMAGE, AND BODILY HARM, PLEASE CONSIDER AND OBSERVE ALL WARNINGS AND CAUTIONS CONTAINED IN THIS PARAGRAPH.

17.1 Warning

If you do not consider the following warnings, it could result in death or serious injury

(1) The Module is controlled by high voltage about 350V. If you need to handle the Module during operation or just after power-off, you must take proper precautions against electric shock and must not touch the drive circuit portion and metallic part of Module within 5 minutes. The capacitors in the drive circuit portion remain temporarily charged even after the power is turned off. After turning off the power, you must be sure to wait at least one minute before touching the Module. If the remain voltage is strong enough, it could result in electric shock.

(2) Do not use any other power supply voltage other than the voltage specified in this product specifications. If you use power voltage deviated from the specifications, it could result in product failure.

(3) Do not operate or install under the deviated surroundings from the environmental specification set for the below; in moisture, rain or near water-for example, bath tub, laundry tub, kitchen sink; in a wet basement; or near a swimming pool; and also near fire or heater - for example, near or over radiator or heat resistor; or where it is exposed to direct sunlight; or somewhere like that. If you use the Module in places mentioned above, it could result in electric shock, fire hazard or product failure.

(4) If any foreign objects (e.g. water, liquid and metallic chip or dust) entered the Module, the power supply voltage to the Module must be turned off immediately. Also, never push objects of any kind into the Module as they may touch dangerous voltage point or make short circuits that could result in fire hazard or electric shock.

(5) If smoke, offensive smell or unusual noise should come from the Module, the power supply voltage to the Module must be turned off immediately. Also, when the screen fails to display any picture after the power-on or during operation, the power supply must be turned off immediately. Do not continue to operate the Module under these conditions.

(6) Do not disconnect or connect the Module's connector while the power supply is on, or immediately after power off. Because the Module is operated by high voltage, and the capacitors in drive circuit remain temporarily charged even after the power is turned off. If you need to disconnect or reconnect it, you have to wait at least one minute after power off.

(7) Do not disconnect or connect the power connector by a wet hand. The voltage of the product may be strong enough to cause an electric shock.

(8) Do not damage the power cable of the Module, also do not modify it.

(9) When the power cable or connector is damaged or frayed, do not use it.

(10) When the power connector is covered with dust, please wipe it out with a dry cloth before power on.

17.2 Caution

If you do not consider the following cautions, it may result in personal injury or damage in property.

(1) Do not set the Module on an unstable, vibrating or inclined place. The Module may fall or collapse and it may cause a serious injury to a person, and/or damage to the product.

(2) If you need to remove the Module to another place, you must turn off the power supply and detach the interface cable and power cable from the Module beforehand, and watch your steps not to step on the cables during the operation. If the cables are damaged during the transport, it may result in fire hazard or electric shock. Also if the Module is dropped or fallen, it may cause a serious injury to a person and /or damage to the product.

(3) When you draw or insert the module's cable, you must turn off the power supply and do it (with) holding the connector. If you forcibly draw the cable, the electric wire in the cable can be exposed or broken. It may result in fire hazard or electric shock.

(4) When you carry the Module, it should be done with at least two workers in order to avoid any unexpected accidents.

(5) Be careful not to touch the panel glass surface while the PDP module is operating because there is a possibility of getting a burn injury due to its very high temperature.

(6) The Module has a glass-plate. If the Module is inflicted with excessive stress - for example; shock, vibration, bending or heat-shock, the glass plate could be broken. It may result in a personal injury. Also, do not press or strike the glass surface.

(7) If the glass panel was broken, do not touch it with bare hand. It may result in a cut injury.

(8) Do not place any object on the glass panel. It may be the cause of the scratch or break of the glass panel.

(9) Do not place any object on the Module. It may result in a personal injury due to fall or drop.

(10) PDP is a product, which generates heat during operation. Therefore, do not use the

materials which make corrode the PDP module by the chemical reaction that takes place in high temperature and humidity conditions.

(11) Exposing to corrosive gases or contact with the materials, which may cause corrosions, could lead to chemical reactions that will adversely affect on the device. If you were to use the PDP in such conditions, consider ways to avoid such exposure or to protect the PDP module.

17.3 Notice

When you apply the Module to your system or handle it, you must make sure to follow the notices set forth below.

□ Notice to your system design

(1) The Module radiates the infrared rays of between 800 and 1000 ㎚. It may bring an error in operating the IR-remote controller or another electric system. Please consider (to) providing the IR absorb filter in your system, and evaluating it.

(2) The Module has a high-voltage switching circuit and a high-speed clock circuit. Therefore, you have to apply and evaluate the EMC consideration of your system.

(3) The Module has a glass plate. In your mechanical design, please (consider to) avoid any excessive shock and stress to the glass surface. Also be careful not to damage the exhaust pipe at the corner of glass plate. If the glass plate and exhaust pipe are damaged, the &Module may fail.

(4) Since PDP module is controlled by high voltage, all voltage should be discharged immediately after the power is turned off.

(5) PDP module generates heat during operation. Heatproof design (radiation and ventilation) should be considered from design stage. If the PDP module is used out of the specified temperature range, it can result in a defect.

(6) The ventilation design in your system should have a back-cover that is able to prevent moisture and dust from getting into the inside of the electric circuit, because the Module has high-density electric parts with high-voltage. If the driver circuit has condensation or dusts, it may cause a short circuit or dielectric breakdown.

(7) If an excessive stress (more than specified absolute maximum ratings in the voltage, current, temperature etc.) is applied to the PDP module, it could cause a serious damage. Do not use the module out of the ratings.

(8) Recommended usage condition of PDP module is limited to the general usage. Within this range, the electrical characteristics of all components are guaranteed. Semiconductors should be used within specified usage range. Usage out of the range will result in decrease of reliability and defects in devices. If the usage or operating condition is out of specification specified on the data sheet, it will be not covered from the

guaranteed range. If you were to use the product in the environment not stated in the list, you should consult with SAMSUNG SDI prior to the usage.

(9) When the PDP module shows fixed pattern, there are possibilities of having the image retention (the difference in brightness between turned-on and turned-off portion of screen due to the different temperature and discharge) and image sticking (the difference in brightness due to phosphor deterioration). To ensure the screen performance, we suggest using the visual display area of PDP module and performing the following methods.

A. If the customer is required to use the fixed pattern, reduce the maximum brightness as low as possible, change the position of the displayed area or display the screen saver or moving picture periodically.

B. If possible, change the displayed color to equalize the total displayed time for each cell.

(10) In system design and evaluation process, you should consider the maximum brightness level (image retention and image sticking).

(11) The PDP screen is displayed by image data signals and synchronized signals. If noise interferes with the signals, the PDP screen could be unstable. Thus, when you design, you should take measures to minimize the affects of noise

(12) For preventing from occurring condensation that consists of small drops of water which form when warm water vapor in the air touches a cold surface such as a panel glass moved from cold condition, the module need to be left in the room temperature for minimum 8 hours in box condition before use.

(13) The customer has to consider their packing box to prevent from occurring condensation during delivery to the End User from their packing material design stage.

(14) SAMSUNG SDI PDP module is a product for the computer, office automation, other office supplies, industry and communication, measurement devices, personal and home appliances. However, if you need to use the PDP module in particular situations, such as defective or abnormal operations can directly affect human life, injuries and damages in property could be caused, and high level of reliability is required (aerospace equipments, nuclear control systems, vehicle controls, life-supporting medical devices, etc.), you should consult with SAMSUNG SDI beforehand. SAMSUNG SDI will not take any responsibility for the problems and defects occurred in the course of usage without prior approval of SAMSUNG SDI

(15) Based on the requirements of the safety standard (UL, EN etc.), be sure to add the filter that come up to the impact test to the glass plate

☐ ***Notice to the operation and handling of the Module***

(1) To prevent defect or failure, please check the cable connections and power-supply condition before power-on.

(2) The Module is controlled by high voltage. Not only during operation but also immediately after power-off, do not disconnect or reconnect the Module's connector because it may result in failure. If you need to disconnect or reconnect, you have to wait at least one minute after power-off.

(3) The Module is equipped with various protection circuits that automatically stop the Module operation, if an interface signal or the power voltage becomes abnormal during operation. If the Module stops suddenly during operation, please check the conditions of input signal or power source before restarting.

(4) For the protection of the circuit, if an abnormal situation is occurred, the high output voltage will be shut down by (watching) the internal input voltage (Vs/ Va/ Vcc). In this case, the Module power resetting is necessary to recover. There are also fuses in the Vs and Va power supply system to prevent smoking and firing by the excessive current. The protecting function of the address driver of keeping a supervisory device for the internal current is provided in the Va power supply system. Therefore, the number of sub-frames decreases to a proper value when the Ia current exceeds a constant value occasionally.

(5) If an abnormal situation such as disconnecting of the input connector occurs, this Module will be on stand-by, which the supply of high output voltage is stopped even if an external power is being supplied. If a normal signal is inputted after this, normal operation state, operations can be restarted again by re-inputting a normal signal. However, it is necessary to rest the Module power when tVH and/or tHV are less than the minimum value provided in the specification

(6) To ensure reliable operation of the Module and to protect it from overheating, do not wrap or cover it with a cloth or like a sheet during power-on period. Also, do not place the Module in a confined space or any other places of poor ventilation.

(7) If you continue to watch the naked screen (without filter glass) for a long time, your eyes could be fatigued. We recommend you rest your eyes occasionally. However, according to the information currently available, watching PDP module for a long time does not cause a direct harm to your eyes.

(8) The screen is controlled with the display-data signals and synchronized signals. If noise interferes with those signals, the screen could become unstable and, in some case, would cause a failure. Do not place any equipment that generates excessive EMI/RFI noise near the interface cable of the Module, and keep the cables as short as possible.

(9) Be careful not to break the glass panel when you handle the Module. Also, when handling the Module, you must wear gloves or other hand protection to prevent injuries that can occur in case when the glass panel is broken.

(10) The glass panel section and drive circuit section of the Module are closely connected and they function as a pair. If the Module is arbitrarily recombined, restructured, or disassembled, SDI will not be responsible for the function, quality, or operational integrity of the modified Module. Do not recombine, restructure, or disassemble it. (Only, the Module for A/S is allowed to be recombined, restructured, or disassembled.)

(11) To avoid a possible electric shock, you must make sure that the power supply voltage of Module is turned off before cleaning. To clean the module's glass panel, apply water or a natural detergent to a piece of soft cloth or gauze, and wring the cloth tightly before wiping the screen. Make sure that no water comes in contact with the connecting terminals on the side of the glass panel. Do not use chemical solvents, such as paint thinner or benzene, to clean the glass panel.

(12) The drive circuit section of Module uses C-MOS integrated circuits that must be protected from static electricity. Therefore, when transporting or delivering the Module, be sure to put the Module in an antistatic bag. When handling the Module, take adequate grounding precautions to prevent static electricity.

(13) When delivering or transporting the Module, you must take special precautions because excessive vibration or shock should not be applied to it. If the Module is dropped, or (if) excessive vibration/shock is applied, the glass panel of the Module may be broken and the drive circuit may be damaged. The packing for delivering or transporting should be made with strict instructions.

(14)The information and schematics shown in this specification are just examples of display applications; it does not mean that they must be applied to your device for the actual use. SAMSUNG SDI does not take any responsibility for the infringement of patent or any other intellectual rights arising from the use of the information or schematics in the document.

(15)If any part or technology of the product described in this specification become subject to restrictions on export or any related laws or regulations, a prior permission is required before exporting.

(16) The PDP module uses semiconductor devices. Since semiconductors are very sensitive to static electricity, the following requirements should be conformed during delivering, transferring and handling the PDP module: Remove the static electricity on your body by wearing the earth-ring which must be connected to the ground through high resistor (about 1M Ohm). It is recommended to wear the conductive clothes and shoes, use conductive floor mats, and take other measures to minimize the static electricity. All the equipments and tools must be connected to the ground and protected from static electricity. When you deliver or transfer the PDP module, always use anti-static bag.

(17) If any device that can generate the high-voltage is located nearby the PDP module, it could cause an abnormal operation. In such a case, you should take a countermeasure to prevent against static electricity and discharges.

(18) If the PDP module is exposed to corrosive gases or contacted to oil, it could cause chemical reactions and give unfavorable effects on the devices. If you intend to use the PDP module under such conditions, you must consider the ways to avoid exposure or to protect the PDP module before using it.

(19) The PDP module is not designed to endure radiation or cosmic radiation. Users must

install the proper shielding.

(20) The PDP module uses thermo-plastic devices. Since these devices are easy to be damaged, do not use the PDP module nearby inflammable substances. If they are burnt, poisonous gas will be emitted.

(21) To ensure the normal operation of the PDP module, the recommended operating range should be required. The electrical properties of the PDP module are guaranteed only when it is used within the recommended operating range. The PDP module must be used within the range at all time. If you use it out of the range, it could give adverse effects on its reliability or cause defects.

(22) Flexible cables connect electrodes on the panel glass and PCBs. Thus, do not apply too much stress such as shock, vibration, pressure, or bending, to the surface of panel glass, PCBs and flexible cables.

(23) If there is no special notice, the contents of this specification describe the product with the initial parameters after shipment.

(24) Even if the panel glass is cleaned before shipping, there is a possibility of particle remained on the panel. In this case, remove it prior to the usage. When you clean the surface of the panel glass, use a piece of soft cloth with detergent to wipe off. Do not use any chemical substances such as acid, alkali or organic detergent.

(25) The Module is composed of various kinds of materials such as glass, metals and plastics. A qualified service technician is required for the disposal of the Module

.

☐ ***Notice to the storage of the Module***

(1) When storing the Module, you must select an environmentally controlled place. Avoid any environment in which the temperature or humidity exceeds the specification values. If you are storing it for a long period of time, we recommend that you place the Module together with a dehumidifying agent, such as silica gel, in a moisture-proof bag and keep it in an environmentally controlled place.

(2) If the module is stored for a long time, the discharge might not take place smoothly. In this case, aging approximately for minimum 2 hours with a full white pattern is suggested. Do aging once in every 6 months.

(3) Do not place the PDP module in the environment with a rapid temperature change in order to avoid the condensation inside of the module.

(4) Do not open the packages at dusty place or the place where corrosive gases exist.

(5) Only qualified person can transfer the PDP module with a forklift or crane.

☐ ***Notice to the repairing and fixing of the Module***

The PDP module is a product made with various tests and adjustments hence, repairing and fixing of PDP module is not allowed to conduct at customer's place. The issue must be handled separately from the specifications.

☐ *Notice of the Module performance*

The Module is the newest display device utilizing the gas discharge technology and digital signal processing technology, and its performances are mostly similar to those of CRT. However, some display performances of the PDP module are different from the CRT's. Please consider the following notices when you watch the screen.

(1) There is (a) slight Neon luminance shown outside of the effective display area on the glass panel. Conceal these parts so that it may not be seen on the display surface.

(2) Depending on the type and time of usage, there may be a slight change in the Luminance and color. There may be an increase of both X-value and Y-value by 0.05 at the maximum in chromaticity. In this case, adjust it using the external data signal.

(3) Because the Module uses phosphor to emit a light, the phosphor, like a CRT, will be deteriorated in proportion to the display signal and Luminance settings. If the same pattern is displayed continuously (fixed display) for an extended period of time, the Luminance of that area will be decreased over non-lit areas due to the fact that the discharge surface will be more activated comparing to the other areas.

(4) When the Vsync signal timing becomes shorter right after the changing of Vsync frequency (e.g. from 50 ㎐ to 60H / from 60 ㎐ to 70 ㎐) depending on the Multi-Vsync function, an initial Vsync signal of the changed frequency will be disregarded and the screen will be interrupted for 1 frame period in maximum.

(5) Because the Module is a digital processing display device, this Module is equipped with the Error diffusion technology and a Duplicated Sub-Frame method to display the grayscale and false contour improvement. However, you may sometimes find a color false contour, especially in human facial contour, in moving picture due to the difference of display performance comparing to the TV-tube.

(6) If the Module displays some video test patterns that are mostly used in a laboratory or inspection process of the manufacturing facilities, you may find the following subjects. But these subjects should not be recognized in the failure or defects because the display performance of the Module is equipped with Error diffusion technology and Duplicated Sub-Frame method (for PAL) based on digital processing technique.

<a> Linearity in the grayscale test pattern

If the PDP module displays the grayscale test pattern (e.g. white color Luminance is gradually changed horizontally or vertically) in a screen, you may find the disparity of Luminance at adjacent grayscale patterns. This behavior is caused by duplicated sub-frame condition (for PAL), display load correction and electroad dependency.

<b> Color contouring and dithering at the stationary picture

If the stationary picture such as a human face or the like is shown in the screen, you may feel some unstable noise at the contour area. This behavior is called the color contouring or dithering, and is caused by the error diffusion condition, display load correction and electrod dependency.

(7) If the Module is operated under inadequate conditions or harsh environment, the screen may become unstable or noisy. This instability is mostly related to ambient temperature, air pressure, input signal instability (include signal noise), input power voltage and strong magnetic field such as MRI/NMR application or superconducting magnet application. Please do not apply the Module to inadequate conditions or harsh environment mentioned above.

□ *PDP DESIGN GUIDELINES AGAINST CORROSIVE GASES/HIGH HUMIDITY*

During the PDP development stage , some materials which may generate corrosive gas(es) or ions such as sulfur, sodium, and clorine, etc must not be allowed to use in the modules. If the material mentioned above is used or located close to the address terminals, chemical reaction may occur and cause the modules to fail.
If customer wishes to use some materials due to unavoidable cause, then safe gap between address terminals and the material(s) which may generate corrosive gas(es) is minimum 5mm or customer must keep or deliver PDP always in room temperature and room humidity state at any cases.
It is a mandatory guide line to protect the modules from corrosive gases or ions.
If some material contains sulfer (sulfur) ,Natrium (sodium) and Cloride , then Samsung SDI strongly suggests customer to keep the guidelines.
The weight of material containing sulfer must be no more than 300ppm .
The analysis of the sulfur weight is based on the noramlized " ICP-AES" method.