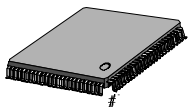
PRODUCT SUMMARY

100-TQFP-1414



INTRODUCTION

S5C7320X01 receives digital data from CCD-using video camera systems such as MMPC and surveillance cameras, and outputs combined video signals. It also runs algorithms for AE/AWB and transmits them to MICOM, or carries out AE/AWB independently. S5C7320X01 has the following features;

FEATURES

- NTSC/PAL, 360H/510H/720H/760H CCD compatible
- Able to detect and correct 64 CCD white defects
- Built-in digital clamp feature
- 3-line processing using 2 line memories
- Luminance signal process
- Chrominance signal process
- Color difference signal modulation using quadrature subcarrier generation (DTO) method
- Built-in timing and sync signal generator
- External synchronization compatible (Line-lock, H-reset/V-reset, H-PLL/V-reset)
- Built-in ability to determine if in external synchronization mode
- Serial MICOM interface
- Built-in algorithm for AE/AWB
- MICOMless (stand-alone) full AE/AWB
- Partial linear approximation method's γ compensation feature for R, G, B and luminance
- Built-in 2CH DAC for combined Y/C analog output
- EEPROM interface for register setting without MICOM
- Built-in EVR interface for controlling CDS/AGC, and CCD

ORDERING INFORMATION

Device	Package	Operating Tempertature
S5C7320X01-T0R0	100-TQFP-1414	0 °C – 70 °C

APPLICATIONS

- Camcorder
- Surveillance camera
- Multimedia PC (MMPC) camera

PIN CONFIGURATION

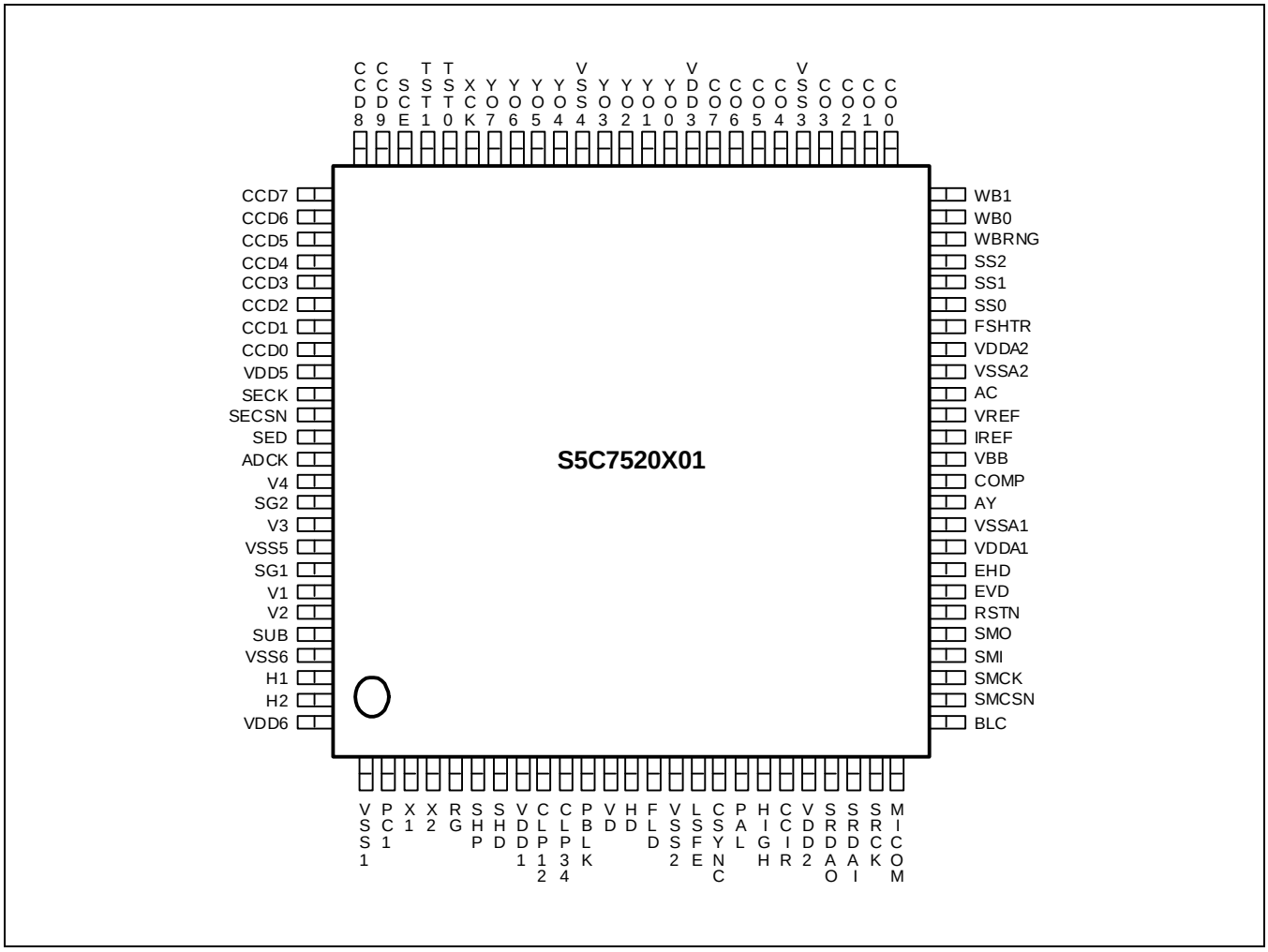


Figure 1. Pin Configuration

PIN DESCRIPTION

Table 1. Pin Description

No	Name	I/O	Description	Note
1	VSS1	G	Ground	
2	PC1	O	Phase comparator output for main clock PLL	
3	X1	I	Main X-TAL input	
4	X2	O	Main X-TAL output	
5	RG	O	Reset gate pulse	
6	SHP	O	Precharge sample & hold pulse	
7	SHD	O	Data sample & hold pulse	
8	VDD1	P	Power	
9	CLP12	O	Clamp pulse 12 (CLP1/CLP2 multiplexing)	
10	CLP34	O	Clamp pulse 34 (CLP3/CLP4 multiplexing)	
11	PBLK	O	Pre-blank pulse	
12	VD	O	Vertical drive pulse	
13	HD	O	Horizontal drive pulse	
14	FLD	O	Field ID signal	
15	VSS2	G	Ground	
16	LSFE	O	Low shutter enable signal (or Vsynco)	
17	CSYNC	O	Composite sync (or Hsynco)	
18	PAL	I	PAL mode (L: NTSC, H: PAL)	P-down
19	HIGH	I	High mode (L: Normal, H:HI8)	P-down
20	CCIR	I	CCIR format mode (L: CIF, H: CCIR)	P-down
21	VDD2	P	Power	
22	SRDAO	O	EEPROM data output	
23	SRDAI	I	EEPROM data input	
24	SRCK	O	EEPROM control clock	
25	MICOM	I	Stand-alone/MICOM IF selection (L: stand-alone)	P-down
26	BLC	I	Back light compensation enable	P-down
27	SMCSN	I	Serial MICOM chip select enable (active "L")	Schmitt
28	SMCK	I	Serial MICOM input clock	Schmitt
29	SMI	I	Serial MICOM data input	Schmitt
30	SMO	O	Serial MICOM data output	
31	RSTN	I	Master reset (active low)	
32	EVD	I	EXT. sync. VD input (line-lock/V-reset mode)	P-up

Table 1. Pin Description (Continued)

No	Name	I/O	Description	Note
33	EHD	I	EXT. sync. HD input (separate sync., composite sync. locking mode.)	P-up
34	VDDA1	P	Analog power for DAC	
35	VSSA1	G	Analog ground for DAC	
36	AY	O(A)	Analog luminance output	
37	COMP	I(A)	Compensation terminal for DAC	
38	VBB	G	DAC bulk bias (ground)	
39	IREF	I(A)	Current reference terminal	
40	VREF	I(A)	Voltage reference terminal	
41	AC	O(A)	Analog CHROMA output	
42	VSSA2	G	Analog ground for DAC	
43	VDDA2	P	Analog power for DAC	
44	FSHTR	I	Fixed high speed shutter mode (active H)	P-down
45	SS0	I	Fixed high speed shutter control 0	P-down
46	SS1	I	Fixed high speed shutter control 1	P-down
47	SS2	I	Fixed high speed shutter control 2	P-down
48	WBRNG	I	White balance range selection	P-down
49	WB0	I	White balance mode 0	P-down
50	WB1	I	White balance mode 1	Pull-up
51	CO0	O	Digital CHROMA output (LSB)	
52	CO1	O	Digital CHROMA output	
53	CO2	O	Digital CHROMA output	
54	CO3	O	Digital CHROMA output	
55	VSS3	G	Ground	
56	CO4	O	Digital CHROMA output	
57	CO5	O	Digital CHROMA output	
58	CO6	O	Digital CHROMA output	
59	CO7	O	Digital CHROMA output (MSB)	
60	VDD3	P	Power	
61	YO0	O	Digital luminance output (LSB)	
62	YO1	O	Digital luminance output	
63	YO2	O	Digital luminance output	
64	YO3	O	Digital luminance output	

Table 1. Pin Description (Continued)

No	Name	I/O	Description	Note
65	VSS4	G	Ground	
66	YO4	O	Digital luminance output	
67	YO5	O	Digital luminance output	
68	YO6	O	Digital luminance output	
69	YO7	O	Digital luminance output (MSB)	
70	XCK	I	Encoder external clock input for line-lock	"L"
71	TST0	I	Test pin 0 (active high)	"L"
72	TST1	I	Test pin 1(active high)	"L"
73	SCE	I	Scan enable for test (active high)	"L"
74	CCD9	I	CCD data input [MSB]	
75	CCD8	I	CCD data input	
76	CCD7	I	CCD data input	
77	CCD6	I	CCD data input	
78	CCD5	I	CCD data input	
79	CCD4	I	CCD data input	
80	CCD3	I	CCD data input	
81	CCD2	I	CCD data input	
82	CCD1	I	CCD data input	
83	CCD0	I	CCD data input [LSB]	
84	VDD5	P	Power	
85	SECK	O	CDS/AGC, EVR clock	
86	SECSN	O	CDS/AGC, EVR chip select (acitve low)	
87	SED	O	CDS/AGC, EVR data line	
88	ADCK	O	ADC sampling clock	
89	V4	O	Vertical drive pulse 4 for CCD	
90	SG2	O	CCD sensor read out pulse 2	
91	V3	O	Vertical drive pulse 3 for CCD	
92	VSS5	G	Ground	
93	SG1	O	CCD sensor read out pulse 1	
94	V1	O	Vertical drive pulse 1 for CCD	
95	V2	O	Vertical drive pulse 2 for CCD	
96	SUB	O	CCD discharge pulse	
97	VSS6	G	Ground for H1, H2	

Table 1. Pin Description (Continued)

No	Name	I/O	Description	Note
98	H1	O	Horizontal driving pulse 1 for CCD	
99	H2	O	Horizontal driving pulse 2 for CCD	
100	VDD6	P	Power supply for H1, H2	

NOTE: Fixed mode shutter speed control

System	S2	S1	S0	Shutter Speed	
				Expected	Real
NTSC	0	0	0	1/60	1/60
	0	0	1	1/250	1/251
	0	1	0	1/500	1/513
	0	1	1	1/1000	1/1006
	1	0	0	1/2000	1/1936
	1	0	1	1/5000	1/5034
	1	1	0	1/10000	1/10489
	1	1	1	Flickerless	Flickerless
PAL	0	0	0	1/50	1/50
	0	0	1	1/250	1/249
	0	1	0	1/500	1/510
	0	1	1	1/1000	1/999
	1	0	0	1/2000	1/1923
	1	0	1	1/5000	1/5000
	1	1	0	1/10000	1/10416
	1	1	1	Flickerless	Flickerless

NOTE: White Balance Mode

WB1	WB0	White Balance Mode
0	0	Normal (auto)
0	1	Cool color temp.
1	0	One-shot W/B mode
1	1	Warm color temp.

BLOCK DIAGRAM

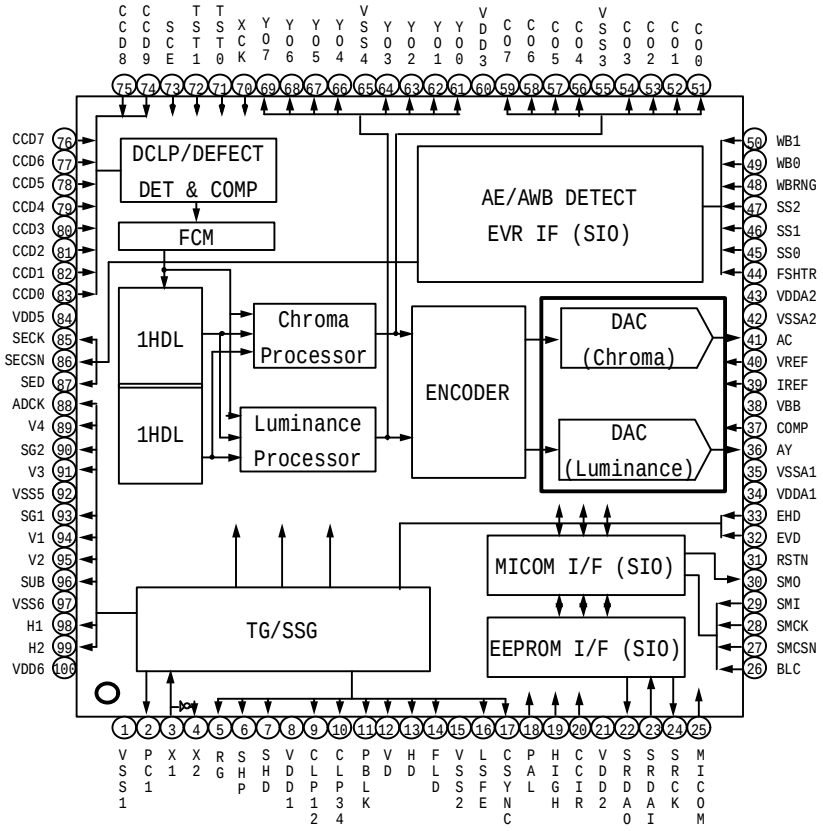


Figure 2. Block Diagram

CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit	Remark
DC supply voltage (digital)	V_{DD}	-0.3 — 3.8	V	-
DC supply voltage (analog)	V_{DDA}	-0.3 — 3.8	V	DAC power
DC input voltage	V_{IN}	-0.3 — V_{DD} + 0.3	V	-
Storage temperature	T_{STG}	-40 — 125	°C	-
Latch-up current	I_{LU}	±100	mA	-

OPERATION TEMPERATURE (0 °C — +70 °C)

ELECTRO-STATIC CHARACTERISTICS

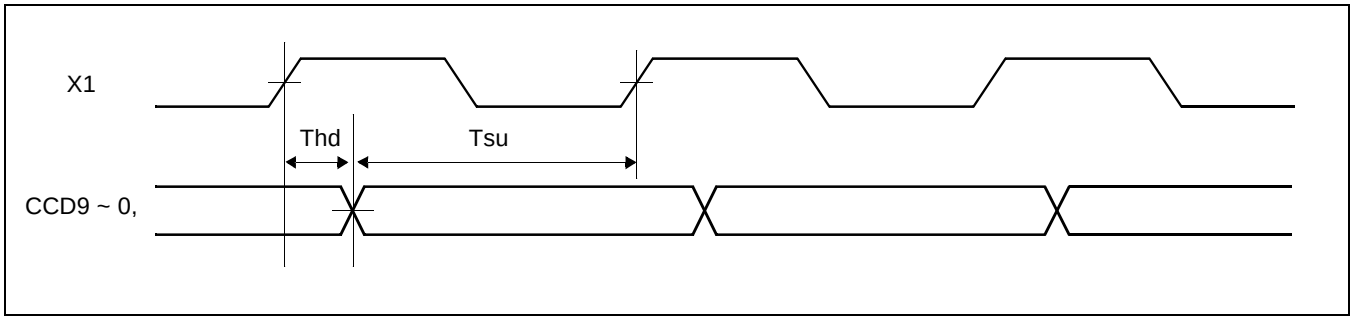
Item	Electrostatic Standard		Unit	Remark
	Pin No	Design Goal		
Human body model (HBM)	All	± 2000V	V	
Machine model (MM)		± 300V	V	

ELECTRICAL CHARACTERISTICS (AC)

V_{SS} = 0V, V_{DD} = 3.3V ±10%, Ta = 0 — 70°C

Table 2. Electrical Characteristics (AC)

Item	Signal	Symbol	Design Goal			Unit	Remark
			Min	Typ	Max		
Input data setup time	CCD9 – CCD 0	Tsu	5	-	-	ns	V_{DD} = 3.3V ±10% Ta = 0 – 70 °C
Input data hold time	CCD9 – CCD 0	Thd	5	-	50	ns	V_{DD} = 3.3V ±10% Ta = 0 – 70 °C



Appendix: External Synchronization Configuration

Example of Internal Reset Mode (NTSC)

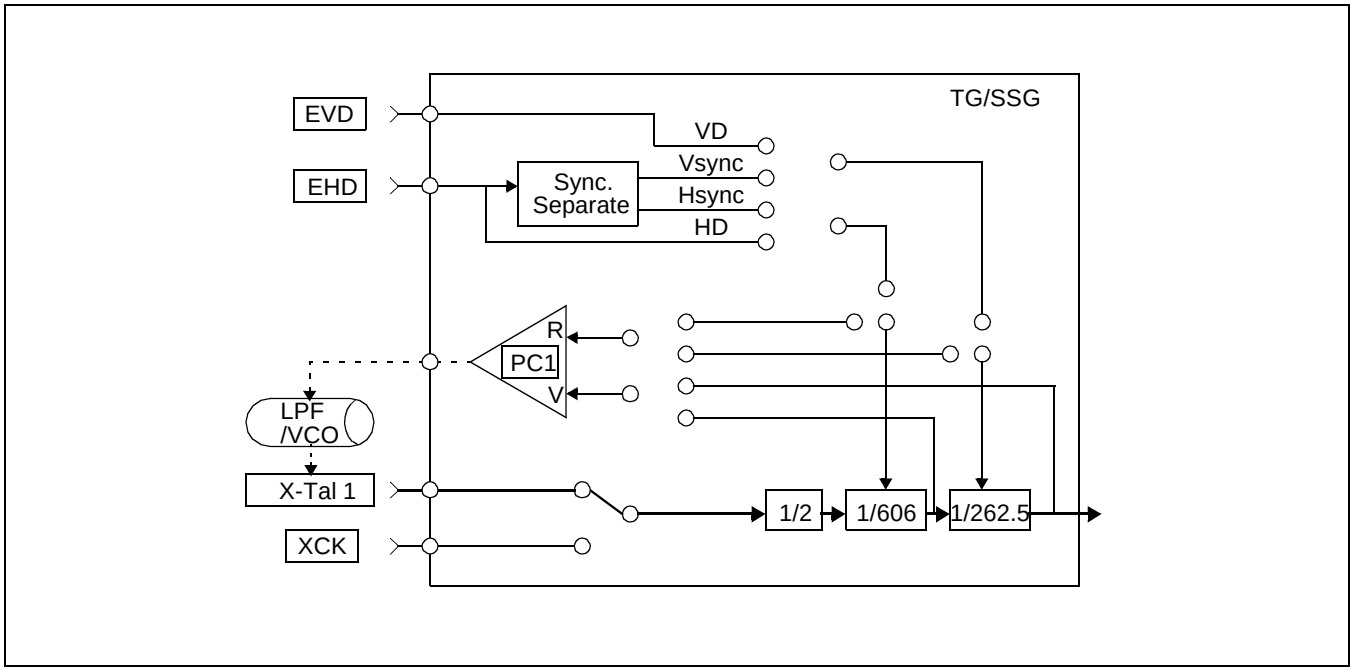


Figure 3. Example of Internal Reset Mode (NTSC)

Example of Line Lock Mode (NTSC)

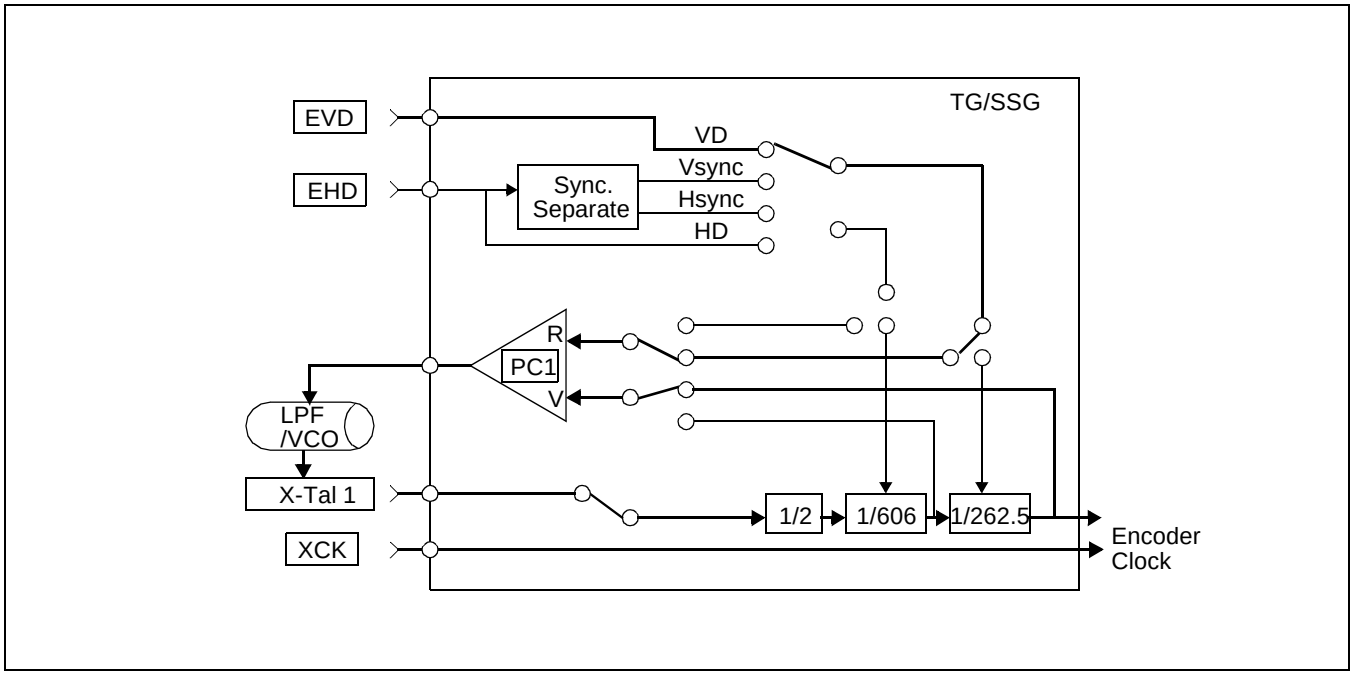


Figure 4. Example of Line Lock Mode (NTSC)

Example of H Reset, V Reset Mode (NTSC)

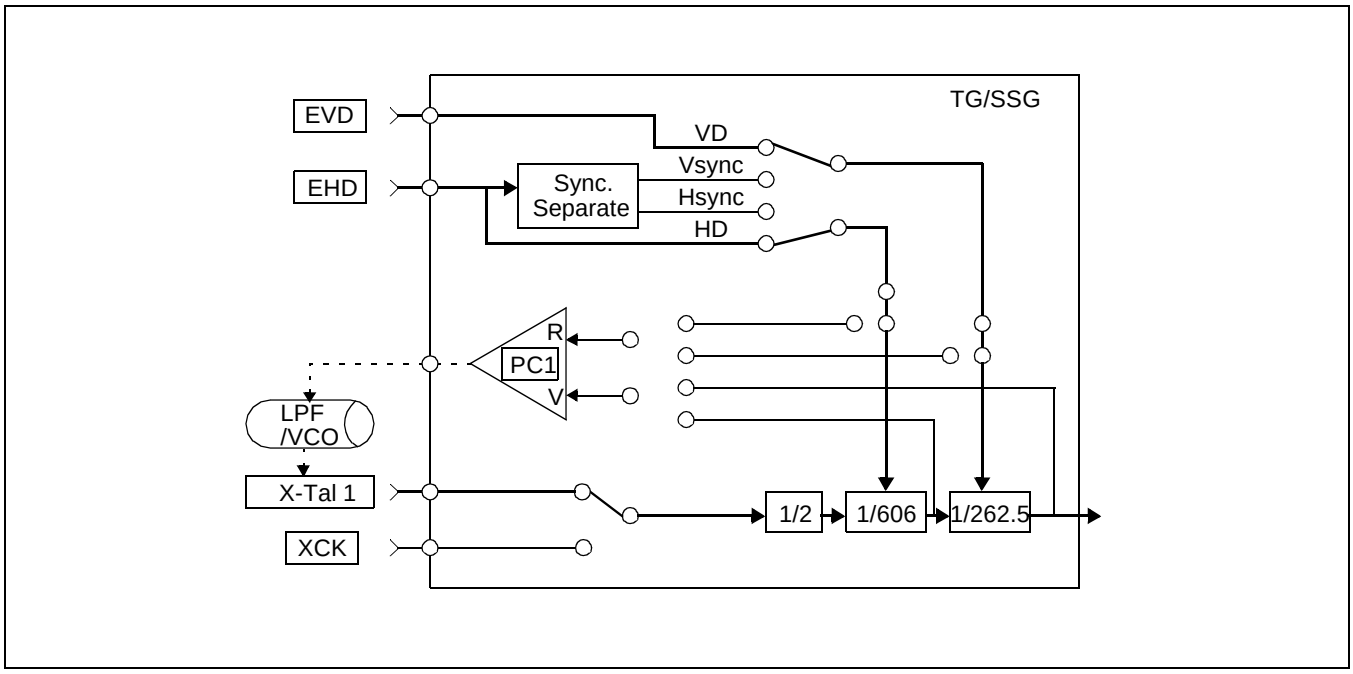


Figure 5. Example of H Reset, V Reset Mode (NTSC)

Example of H PLL, V Reset Mode (NTSC)

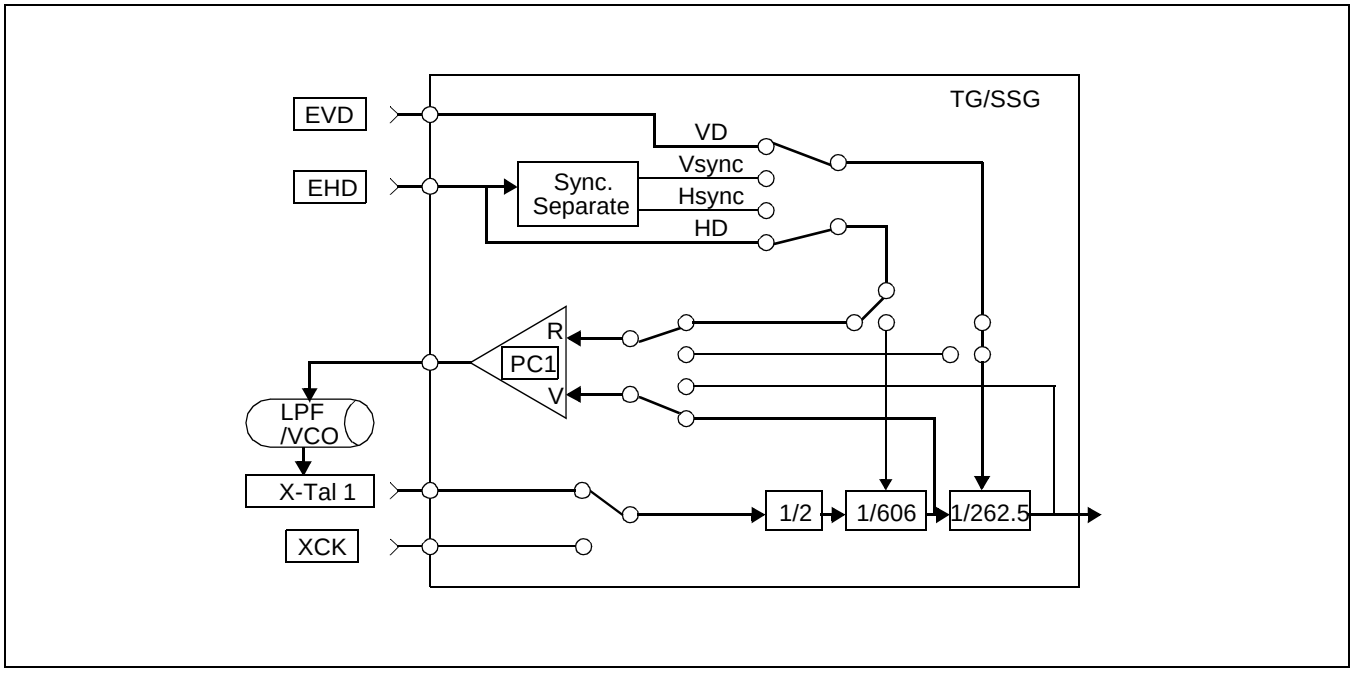


Figure 6. Example of H PLL, V Reset Mode (NTSC)

Example of Csync Reset (H PLL, V Reset) Mode (NTSC)

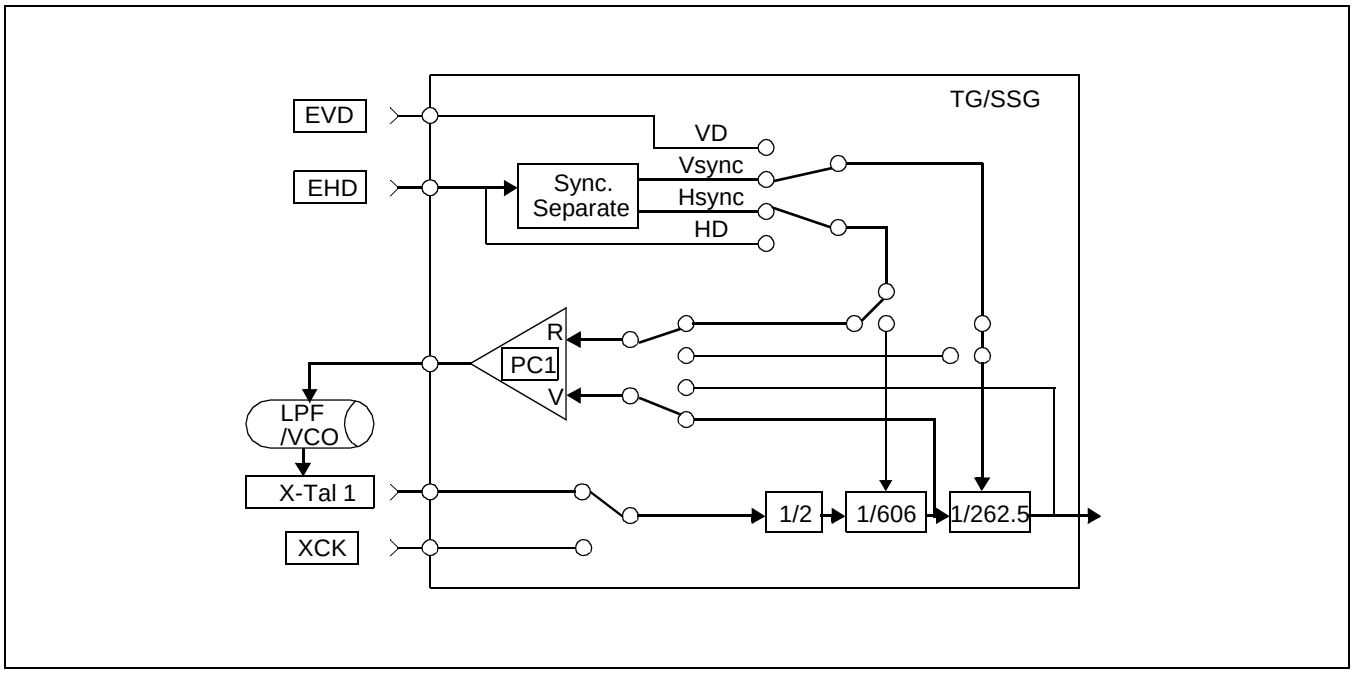


Figure 7. Example of Csync Reset (H PLL, V Reset) Mode (NTSC)

PLL Application Circuit

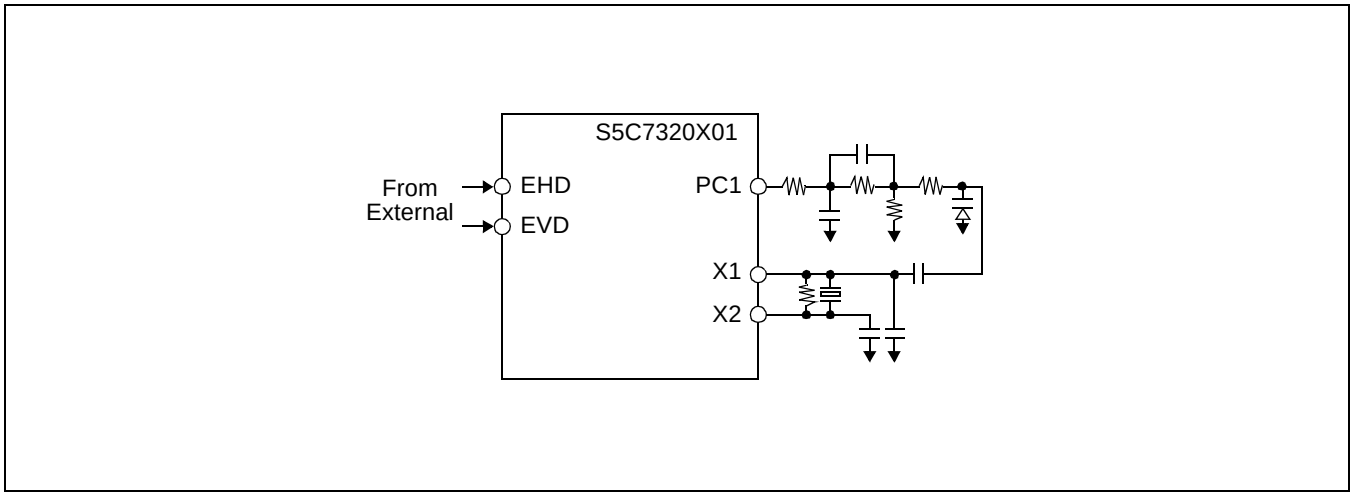


Figure 8. PLL Application Circuit

APPLICATION CIRCUIT DIAGRAM

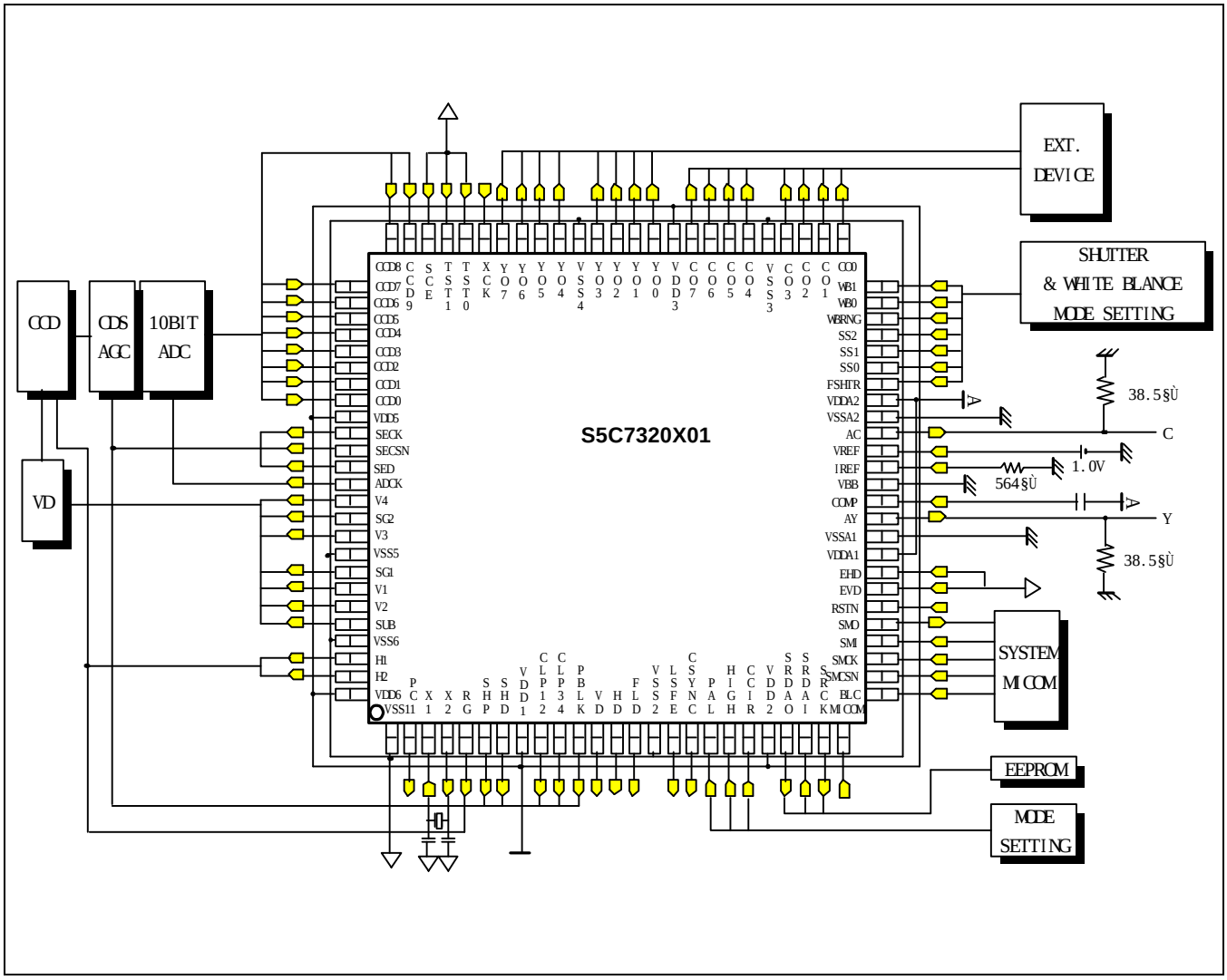


Figure 9. Application Circuit Diagram

PACKAGE DIMENSIONS

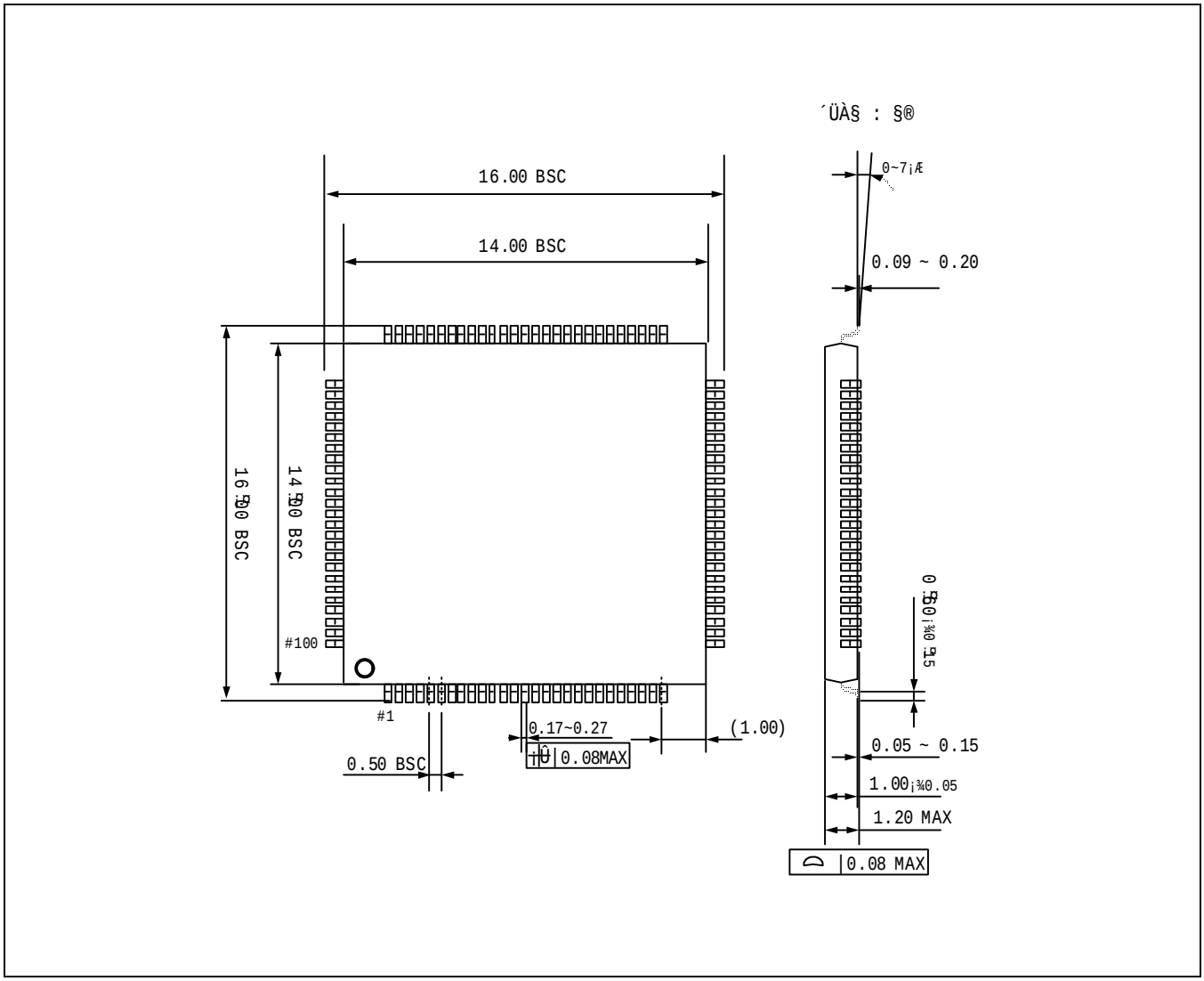


Figure 10. Package Dimensions

SAMSUNG ELECTRONICS